SPECIFICATION

FSP700-70RGHBE1

PS/2 Redundant Power Supply

Rev1.2

Revision History

Rev.	Description of Changes	Author / Owner	Date
1.0	Public release	Danny	2015/07/29
1.1	Update Section : 4.5.1 Voltage Hold-up Time (100%=>80%) 4.6 EFFICIENCY 4.10 AC Line Transient Specification (0 to 1 AC cycle 100%=>70%) 6.1.1 Over Current and Short Circuit Protection (12V / 17.5A~20.5A =>18.5A~21.5A) 7.1 PSON#(PSON<=0.8V) Add Section : 6.3 Leakage current 6.4 Over Temperature Protection (OTPAR) Delete Section 5.12 Power Distribution Board Fail (B/P Fail) Function	Jack Wu	2015/11/19
1.2	Add Section : 5.12 Power Distribution Board Fail (B/P Fail) Update Section: 7.2 Power Supply LED Indicators	Jack Wu	2017/01/18

CONTENTS

1. Purpose

This Power Supply Design Guide defines a common redundant power sub-system for use in Pedestal servers and workstation systems. The power sub-system is made up of a cage (with a power distribution board) and hot-swap redundant power modules. This design guide covers the mechanical and electrical requirements of this power sub-system, which may range from 700 watts and is used in a hot-swap redundant configuration. The parameters of this supply are defined in this design guide for open industry use.

All outputs and shall communicate to external devices through Inter-Integrated (I^2C) Circuit protocol. The power supply will have an EEPROM for storing powers supply FRU information, and meet PMBus Revision 1.2 requirement.(It is define in PMBus specification

2. Mechanical Overview

The ATX PS/2 redundant is a power sub-system made up of a cage and redundant, hot swappable power supply modules. A mechanical drawing of the cage is shown below in Figure 1. The cage is intended to be mounted in the system and not redundant or hot swappable. The exterior face of the cage accepts hot swappable power supply modules. The distribution board within the cage distributes output power from the modules to a wire harness. Cooling fans, EMI filtering, and IEC inlet connector(s) may be located in the modules.

The detail data need to reference M/E speccificatin.

Dimensions: 150mm (W) × 86mm (H) × 190mm (L)

2.1 Temperature Requirements

The operation ambient temperature shall be 0°C to 50°C.

The non-operation ambient temperature shall be -20°C to 80°C.

2.2 Relative Humidity

Operating: 5% to 90 % relative humidity (non-condensing)

Non-operating: 5% to 90 % relative humidity (non-condensing)

3. Definitions/Terms/Acronyms

Table 1:

Required	The status given to items within this design guide, which are required to meet SSI guidelines and a large majority of system applications.
Recommended	The status given to items within this design guide which are not required to meet SSI guidelines, however, are required by many system applications.
Optional	The status given to items within this design guide, which are not required to meet SSI guidelines, however, some system applications may optionally use these features.
Autoranging	A power supply that automatically senses and adjusts itself to the proper input voltage range (110 VAC or 220 VAC). No manual switches or manual adjustments are needed.
Dropout	A condition that allows the line voltage input to the power supply to drop to below the minimum operating voltage.
Latch Off	A power supply, after detecting a fault condition, shuts itself off. Even if the fault condition disappears, the supply does not restart unless manual or electronic intervention occurs. Manual intervention commonly includes briefly removing and then reconnecting the supply, or it could be done through a switch. Electronic intervention could be done by electronic signals in the Server System.
Monotonically	A waveform changes from one level to another in a steady fashion, without intermediate retracement or oscillation.
Noise	The periodic or random signals over frequency band of 0 Hz to 20 MHz.
Overcurrent	A condition in which a supply attempts to provide more output current than the amount for which it is rated. This commonly occurs if there is a "short circuit" condition in the load attached to the supply.
PFC	Power Factor Corrected.
Ripple	The periodic or random signals over a frequency band of 0 Hz to 20 MHz.
Rise Time	Rise time is defined as the time it takes any output voltage to rise from 10% to 95% of its nominal voltage.
Sag	The condition where the AC line voltage drops below the nominal voltage conditions.
Surge	The condition where the AC line voltage rises above nominal voltage.
VSB or Standby Voltage	An output voltage that is present whenever AC power is applied to the AC inputs of the supply.
MTBF	Mean time between failure
PWOK	A typical logic level output signal provided by the supply that signals the Server System that all DC output voltages are within their specified range.

4. AC Input Requirements

The power supply modules shall incorporate universal power input with active power factor correction, which shall reduce line harmonics in accordance with the EN61000-3-2 and JEIDA MITI standards.

4.1 AC Inlet Connector

The AC input connector shall be an *IEC 320 C-14* power inlet. This inlet is rated for 10A/250 VAC.

4.2 Redundant AC Inlets

The power supply assembly have dual redundant AC inlets. The power supply shall be able to operate over its full, specified range of requirements with either or both AC input powered. If there is a loss of one AC inlet the power supplies shall continue to operate with no interruption of performance. It is required that all redundant power supply modules be present to support redundant AC inlets.

4.3 AC Input Voltage Specification

The power supply must operate within all specified limits over the following input voltage range.

Table 2: AC Input Rating

PARAMETER	MIN	RATED	MAX
Voltage (110)	90	100-127 Vrms	140 Vrms
Voltage (220)	180	200-240 Vrms	264 Vrms
Frequency	47 Hz		63 Hz

4.4 Power Factor

The power factor shall be greater than 0.95 at full load / 100 Vrms input voltage conditions

, and 0.9 at full load / 240Vrms input voltage conditions

4.5 Input Under Voltage

Brown-out(AC UVP)

The power supply shall power off if the AC input is below VAClow_limit and shall start (auto recover) if VACrecover is reached. Input of VAC below VACrecover shall not cause
any damage to the power supply, including the input fuse.

$VAC_{recover\ (Brownin)}$	$VAC_{low\_limit\ (Brownout)}$
82VAC ±4VAC	75VAC ±5VAC

4.5.1 Voltage Hold-up Time

The power supply holdup time requirements to 80% of maximum load.

4.6 Efficiency

Efficiency shall be tested at AC input voltages of 115VAC and 230VAC. And only insert one power module into the power cage. The voltage should measure on the back plane.

Table 3: 700W Efficiency

Loading	+12V1	+12V2	+12V3	+5V	+3.3V	-12V	+5Vsb	Efficiency
Full Load	15.6	15.6	15.6	14.37	14.37	0.46	2.75	84%

4.7 AC Line Dropout

An AC line dropout is defined to be when the AC input drops to 0 VAC at any phase of the AC line for any length of time. During an AC dropout of one cycle or less the power supply must meet dynamic voltage regulation requirements up to 75% of the rated output load. An AC line dropout of one cycle or less shall not cause any tripping of control signals or protection circuits. If the AC dropout lasts longer than one cycle or the load is greater than 75%, the power supply should recover and meet all turn on requirements. The power supply must meet the AC dropout requirement over rated AC voltages, frequencies, and output loading conditions. Any dropout of the AC line shall not cause damage to the power supply. In the case of redundant AC inputs, the AC line dropout may occur on either or both AC inlet.

4.8 AC Line Fuse

The power supply shall incorporate one input fuse on the LINE side for input over-current protection to prevent damage to the power supply and meet product safety requirements. Fuses should be slow blow type or equivalent to prevent nuisance trips. AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

4.9 AC Inrush

An additional inrush current limit is recommended for some system applications that require multiple systems on a single AC circuit. Under all other conditions , power supply should not be damaged.

(Cold start – 25 deg. C)

115V	40A
230V	80A

4.10 AC Line Transient Specification

AC line transient conditions shall be defined as “sag” and “surge” conditions. Sag conditions (also referred to as “brownout” conditions) will be defined as the AC line voltage dropping below nominal voltage. Surge conditions will be defined as the AC line voltage rising above nominal voltage.

The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 4: AC Line Sag Transient Performance

AC Line Sag				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltage ranges	50/60 Hz	No loss of function or performance
0 to 1 AC cycle	70%	Nominal AC Voltage ranges	50/60 Hz	No loss of function or performance
>1 AC cycle	>10%	Nominal AC Voltage ranges	50/60 Hz	Loss of function acceptable, self recoverable

Table 5: AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60 Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60 Hz	No loss of function or performance

4.11 AC Line Fast Transient Specification

The power supply shall meet the *EN61000-4-5* directive and any additional requirements in *IEC1000-4-5:1995* and the Level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.
- The surge-withstand test must not produce damage to the power supply.
- The supply must meet surge-withstand test conditions under maximum and minimum DC-output load conditions.

5. DC Output Specification

5.1 Output Power/Currents

The following tables define the power and current ratings for different recommended power levels. Depending upon the system design, the power supply modules may have less outputs than required by the system (example: +12V and 5VSB). If there are less outputs than required by the system on the module, the cage shall have additional DC/DC converters to generate the voltages not produced by the modules (example: +12V/+5V, +12V/+3.3V, +12V/-12V). The combined output power of all outputs from the cage shall not exceed the rated output power. The power assembly shall meet both static and dynamic voltage regulation requirements over the full load ranges. The power sub-assembly shall supply redundant power over the full load ranges.

Table 6: 700 W Load Ratings

Voltage	Minimum Continuous	Maximum Continuous	Peak
+3.3 V	0 A	20.0 A	
+5 V	0 A	20.0 A	
+12V1	1A	17.0 A	
+12V2	0 A	17.0A	
+12V3	0A	17.0A	
-12 V	0 A	0.5A	
+5 VSB	0 A	3 A	

1. Maximum continuous total DC output power should not exceed 700 W.
2. Maximum continuous combined load on +3.3 VDC and +5 VDC outputs shall not exceed 130 W.

5.1.1 Standby Outputs

The 5 VSB output shall be present when an AC input greater than the power supply turn on voltage is applied.

5.2 Voltage Regulation

The power assembly output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise specified in Section 5.10. All outputs are measured with reference to the return remote sense (ReturnS) signal. The 5 V, 12V, –12 V, and 5 VSB outputs are measured at the power assembly connectors referenced to ReturnS. The +3.3 V is measured at its remote sense signal (3.3VS) located at the signal connector.

Table 7: Voltage Regulation Limits

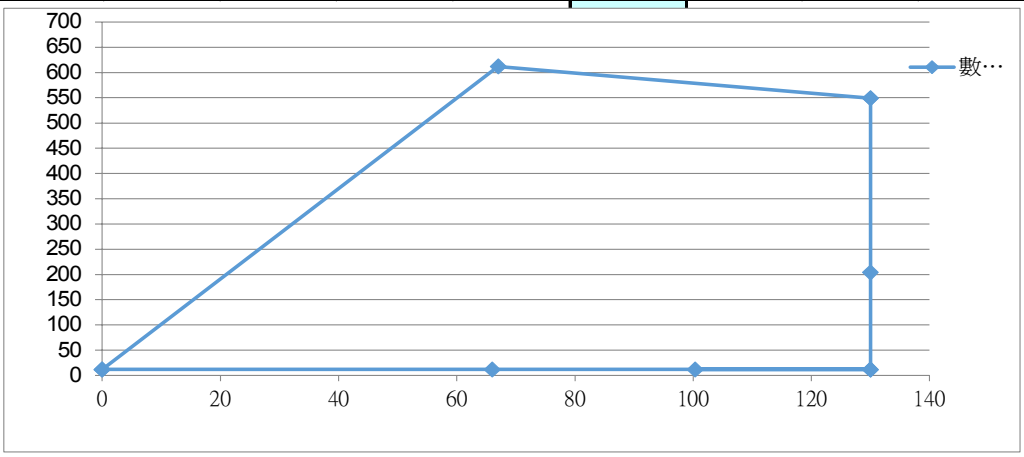
Parameter	MIN	NOM	MAX	Units	Tolerance
+3.3 V	+3.135	+3.30	+3.46	Vrms	+5/-5%
+5 V	+4.75	+5.00	+5.25	Vrms	+5/-5%
+12V1	+11.40	+12.00	+12.60	Vrms	+5/-5%
+12V2	+11.40	+12.00	+12.60	Vrms	+5/-5%
+12V3	+11.40	+12.00	+12.60	Vrms	+5/-5%
-12 V	-10.80	-12.00	-13.20	Vrms	+10/-10%
+5 VSB	+4.75	+5.00	+5.25	Vrms	+5/-5%

5.3 Cross Regulation

Each output shall remain within the specified limits for the +5V, +3.3V , +12V1,+12V2,+12V3, -12V and 5Vsb which acceptable load combinations are in the following table.

Table 8:700W Cross Regulation Table

700W Cross regulation table								
Loading	+3.3V/A	+5V/A	+3.3 & +5V Combine Power	+12V/A Combine	+12V Power	-12V/A	+5Vsb/A	Total Power
L-1	0	0	0	1	12	0.	0	12
L-2	20	0	66	1	12	0.	0	78
L-3	20	12.8	130	1	12	0.	0	142
L-4	0.1	20	100	1	12	0.	3	127
L-5	9.09	20	130	1	12	0.	0	142
L-6	9.09	20	130	17	204	0.5	2	350
L-7	9.09	20	130	45.7	549	0.5	3	700
L-8	20	12.8	130	45.7	549	0.5	3	700
L-9	10.1	6.7	67	51	612	0.5	3	700



5.4 Dynamic Loading

The output voltages shall remain within the limits specified in Table 9 for the step loading and within the limits specified in for the capacitive loading. The load transient repetition rate shall be tested between 50 Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The . step load may occur anywhere within the MIN load to the MAX load shown in Table 6.

Table 9: Transient Load Requirements

Output	. Step Load Size	Load Slew Rate	Capacitive Load
+3.3 V	20% of max load	0.5 A/µs	1000 µF
+5 V	20% of max load	0.5 A/µs	1000 µF
+12V	30% of max load	0.5 A/µs	2200 µF
+5 VSB	25% of max load	0.5 A/µs	1 µF

5.5 Capacitive Loading

The power supply shall be stable and meet all requirements, except dynamic loading requirements, with the following capacitive loading ranges.

Note: Up to 10,000 µF of the +12V capacitive loading may be on the +12V output.

Table 10: Capacitive Loading Conditions

Output	MIN	MAX	Units
+3.3 V	10	12,000	µF
+5 V	10	12,000	µF
+12 V1	10	11,000	µF
+12V2	10	11000	µF
+12V3	10	11000	µF
-12 V	1	350	µF
+5 VSB	1	350	µF

5.6 Ripple / Noise

The maximum allowed ripple/noise output of the power supply is defined in Table 11. This is measured over a bandwidth of 0 Hz to 20 MHz at the power supply output connectors. A 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor are placed at the point of measurement.

Table 11: Ripple and Noise

+3.3 V	+5 V	+12 V	-12 V	+5 VSB
50 mVp-p	50 mVp-p	120 mVp-p	200 mVp-p	50 mVp-p

5.7 Load sharing

The +12 V output shall have active load sharing. When operating at 50% of full load, the output current of any 1+1 power supplies shall be within (+/-10%). For example, if power supply #1 is operating at 20A, then all other power supplies within the system shall be operating between 18A to 22A (+/- 10% of 20A).

5.8 Hot Swap Requirements

The power supply modules shall be hot swappable. Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits specified in Table 7 with the capacitive load specified . The hot swap test must be conducted when the sub-system is operating under both static and dynamic conditions. The sub-system shall not exceed the maximum inrush current as specified in Table 6. The power supply can be hot swapped by the following methods:

AC connecting separately to each module. Up to two power supplies may be on a single AC power source. Extraction: The AC power will be disconnected from the power supply first and then the power supply is extracted from the sub-system. This could occur in standby mode or powered on mode. Insertion: The module is inserted into the cage and then AC power will be connected to the power supply module.

For power modules with AC docking at the same time as DC. Extraction: The module is extracted from the cage and both AC and DC disconnect at the same time. This could occur in standby or power on mode. No damage or arcing shall occur to the DC or AC contacts which could cause damage. Insertion: The AC and DC connect at the same time as the module is inserted into the cage. No damage to the connector contacts shall occur. The module may power on or come up into standby mode.

Many variations of the above are possible. Supplies need to be compatible with these different variations depending upon the sub-system construction. In general, a failed (off by internal latch or external control) supply may be removed, then replaced with a good power supply, however, hot swap needs to work with operational as well as failed power supplies. The newly inserted power supply may get turned on by inserting the supply into the system or by system management recognizing an inserted supply and explicitly turning it on.

5.9 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 1 to 70ms. The +3.3V, +5V and +12V output voltages should start to rise approximately at the same time. All outputs must rise monotonically. Each output voltage shall reach regulation within 50ms (T_{vout_on}) of each other during turn on of the power supply. Each output voltage shall fall out of regulation within 400msec (T_{vout_off}) of each other during turn off. Refer to Figure 2 Power Supply Timing. Figure 3 Turn-on Turn-off Timing shows the timing requirements for the power supply being turned on and off via the AC input with PSON held low, and the power supply being turned on and off with the PSON signal after AC input is applied.

Table: 12 Output Voltage Timing

ITEM	DESCRIPTION	MIN	MAX	UNITS
T_{vout_rise}	Output voltage rise time from each main output.	1	70	msec
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	msec
T_{vout_off}	All main outputs must leave regulation within this time.		400	msec

Figure 2: Power Supply Timing

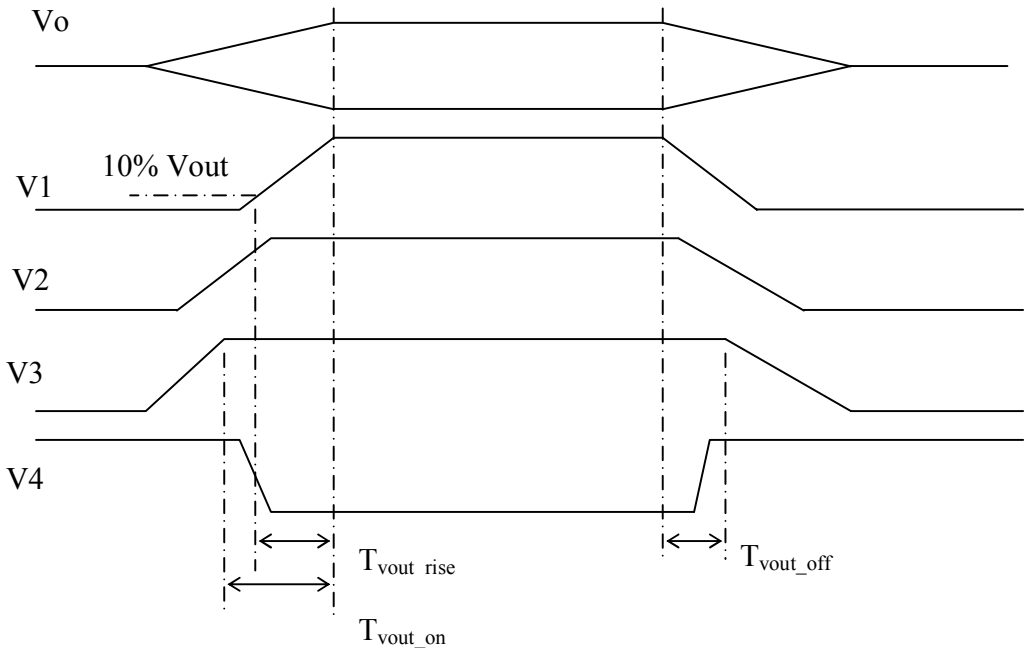
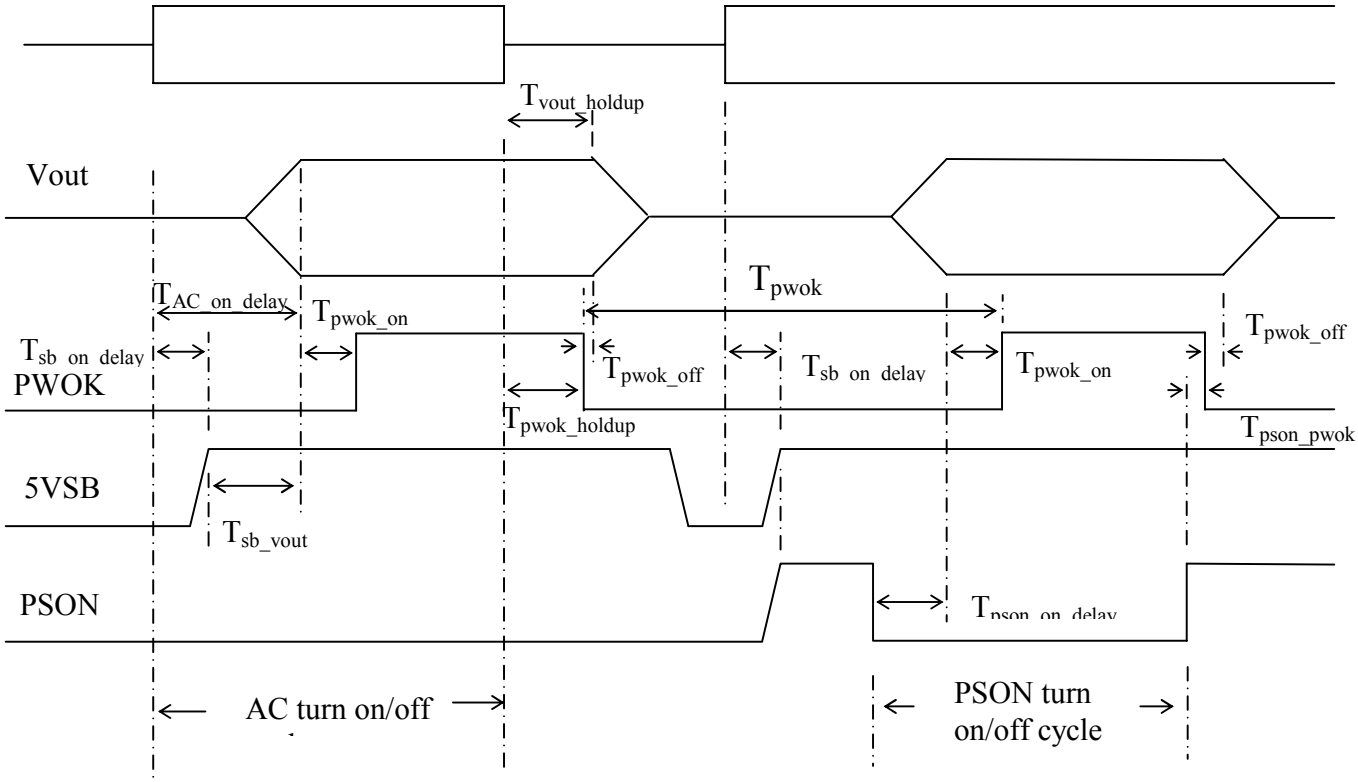


Table 13: Turn On/Turn Off Timing

ITEM	DESCRIPTION	MIN	MAX	UNIS
$T_{sb\_on\_delay}$	Delay from AC being applied to 5VSB being within regulation.		3000	msec
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		4500	msec
T_{vout_holdup}	Time all output voltages stay within regulation after loss of AC.	17		msec
T_{pwok_holdup}	Delay from loss of AC to deassertion of PWOK	16		msec
$T_{pson\_on\_delay}$	Delay from $PSON^{\#}$ active to output voltages within regulation limits.	5	400	msec

T_{pson_pwok}	Delay from PSON# deactive to PWOK being deasserted.		100	msec
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	msec
T_{pwok_off}	Delay from PWOK deasserted to output voltages (3.3V, 5V, 12V) dropping out of regulation limits.	1		msec
T_{pwok_low}	Duration of PWOK being in the deasserted state during an off/on cycle using AC or the PSON signal.	100		msec
T_{sb_vout}	Delay from 5VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	msec

Figure 3 Timing Diagram



5.10 PSKILL Input Signal

The purpose of the PSKILL pin is to allow for hot swapping of the power supply. The PSKILL pin on the power supply is shorter than the other signal pins. When a power supply is operating in parallel with other power supplies and then extracted from the system, the PSKill pin will quickly turn off the main output to prevent arcing of the DC output contacts. TPSKill is the minimum time delay from the PSKill pin un-mating to when the power pins un-mate. The power supply must discharge its output inductor within this time from the un-mating of PSKill pin. When the PSKill signal pin is not pulled down or left open (power supply is extracting from the system or had not been inserted to the system), the power supply should shut down regardless of the condition of the PSON# signal. The mating pin of this signal in the system shall be tied to ground. Internal to the power supply, the PSKILL pin shall be connected to a standby voltage through a pull-up resistor. Upon receiving a LOW state signal at the PSKILL pin, a PSON# signal shall enable the power supply to turn on. See Table 14.

Table 14: PSKILL signal characteristics

Signal Type (Input Signal to Supply)	**Accepts a ground input from the system. Pull- up to Vsb located in the power supply.**	
PSKILL = Low, $PSON^{\#}$ = Low	ON	
PSKILL = Low or Open, $PSON^{\#}$ = Open	OFF	
PSKILL = Open , $PSON^{\#}$ = Low	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	0.4V
Logic level high (power supply OFF)	2.4V	5.25V
Source current, V_{pskill} = low		4mA
Delay from PSKILL=High to power supply turned off (T_{PSKill})		100µsec

5.11 (PSAlert) Output Signal Pin

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

5.11.1 Thermal CLST

SMBAlert# shall also be utilized for warning of critical thermal component temperatures. The Thermal CLST shallassert when the component temperature, which shall be reported by a dedicated thermal probe, is reaching below specified ΔT to critical shut down. The power supply shall report the temperature in addition to Thermal CLST through PMBus to the system, in order to increase fan speed to cool down environmental temperature.

This signal is to be asserted in parallel with LED turning solid red or blinking red/blue. See Table 15.

Table 15: PSAlert# signal characteristics

Signal Type	**Open collector/drain output from power supply.** **Pull-up to Vsb located in power supply.**	
Alert#=High	Power OK	
Alert#=Low	Power Alert to system	
	MIN	MAX
Logic level low voltage, I_{sink}=4mA	0V	0.4V
Logic level high voltage, I_{sink} = 50A	2.4V	3.46V
Sink current, Alert#=low		4mA
Sink current, Alert#=high		4mA

5.12 Power Distribution Board Fail (B/P Fail)

This B/P Fail is a function from the PDB MCU firmware, to remotely shut of the main output of the power supply in a critical or failed state situation caused by the PDB. B/P_Fail will be asserted when the PDB or the system experience any problem like over-current, over-voltage, under-voltage, short-circuit, over-temperature or the system operating in environmental condition exceeding the operation conditions. The power Supply will shutdown and latch off.

6. Protection Circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15 s and a PSON# cycle HIGH for 1 s must be able to reset the power supply.

6.1 240VA Protection

Overload currents applied to each tested output rail will cause the output to trip before reaching or excee ding 240VA. For testing purposes, the overload currents should be ramped at a minimum rate of 10A/s starting from full load.

6.1.1 Over Current and Short Circuit Protection (OCP/SCPmain & OCP/SCPauxilary AR)

The Over Current Condition shall be measured internal to the power supply on all outputs (Main and Auxiliary $Output_{AR}$), and preventing outputs to exceed current limits specified in below table. The power supply shall shutdown and latch off after an Over Current condition on main outputs, the auxiliary output shall be auto recover (VsB_{AR}) after the OCP/SCP had been removed.

The latch on the main output can be cleared by asserting $PSON^{\#}$ signal or by an Input Power interruption.

The power supply shall alert the system of the OCP/SCP condition via $SMBAlert^{\#}$ and fail LED indicator.

The power supply shall not be damaged from repeated power cycling in this condition.

Table 16: Over Current/Short Circuit Protection

Voltage	Over Current Limit (Iout limit)
+3.3 V	24A---32A
+5 V	24A---32A
+12 V1,+12V2,+12V3	18.5A---21.5A

6.2 Over Voltage Protection

The power supply over voltage protection shall be locally sensed in the hot swap modules. The power supply shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. Table 17 contains the over voltage limits. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels when measured at the power pins of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power pins of the power supply connector.

Table 17: Over Voltage Limits

Output Voltage	MIN (V)	MAX (V)
+3.3 V	3.5	4.5
+5 V	5.5	6.82
+12V	13.4	15.6

6.3 Leakage current

The leakage current from AC to safety ground will not exceed 3.5 mA-rms at 264Vac, 50 Hz.

6.4 Over Temperature Protection (OTPAR)

The power supply shall have minimum of two thermal sensors to measure the environmental (T_{env}) and critical component (T_{comp}) temperature. The thermal sensors shall be part of a protection circuit to protected against overtemperature conditions caused by loss of fan cooling or excessive ambient temperature. In an critical Over temperature condition, specified in below table, the PSU shall be shutdown with the exception of the auxiliary output (VsB_{AR}).

The Thermal CLST shall be part of the OTP_{AR}.

The power supply shall alert the system of the OTP_{AR} condition via $SMBAlert^{\#}$ and fail LED indicator. The power supply will auto recover from this condition, when the temperature is dropping within specification again. If the OTP_{AR} is caused due to a defective fan, the power supply shall latch off and not auto recover.

Table 18: Over Temperature Protection$_{AR}$

Condition	Warning in °C	Critical in°C	Timing for SMBAlert#/LED
Tenv	75	80	1msec

The thermal sensors shall have an accuracy of max. 1°C per step and a tolerance of ± 2%.

Ambient temperature: 50°C

6.5 Fan Failure ProtectionAR

The power supply shall have a circuit internal to monitor the power supply internal fan. The fan failure protection shall monitor the fan speed and should assert SMBAlert# in case the fan Rotation Per Minute (RPM) drop lower threshold or set PWM Δ as defined in below table.

The protection circuit shall shutoff the main outputs only and let them auto recover when the fan failure had been cleared.

Table 19: Fan Failure Protection$_{AR}$

Condition	FAN RPM	Timing for SMBAlert#/LED
Warning	1800	2sec
Critical	1500	2sec

7. Control and Indicator Functions

The following sections define the input and output signals from the power supply.

Signals that can be defined as low true use the following convention:

signal# = low true

7.1 PSON#

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +3.3 V, +5 V, +12 V, and -12 V power rails. When this signal is not pulled low by the system, or left open, the outputs (except the +5 VSB and Vbias) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer to *Figure 3* for timing diagram.

Table 20: PSON# Signal Characteristic

Signal Type	Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply.	
PSON# = Low, PSKILL = Low	ON	
PSON# = Open, PSKILL = Low or Open	OFF	
PSON# = Low, PSKILL = Open	OFF	
	MIN	**MAX**
Logic level low (power supply ON)	0V	0.8V
Logic level high (power supply OFF)	2.0V	5.25V
Source current, Vpson = low		4mA
Power up delay: $T_{pson\_on\_delay}$	5msec	400msec
PWOK delay: T_{pson_pwok}		50msec

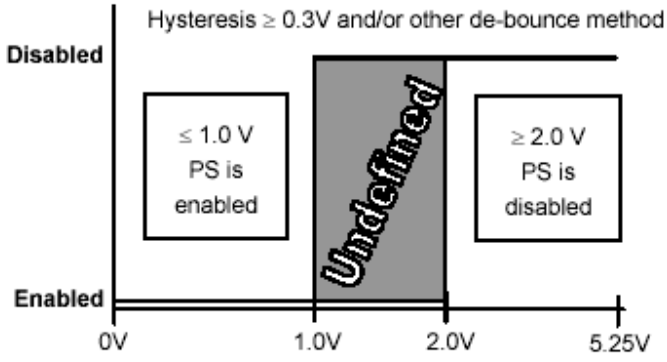


Figure 4: PSON# Signal Characteristics

7.2 PWOK (Power OK)

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be pull to a LOW state. See *Figure 3* for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall be inhibited as long as any power supply output is in current limit.

Table 21: PWOK Signal Characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located in power supply.	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	MIN	**MAX**
Logic level low voltage, Isink=4mA	0V	0.4V
Logic level high voltage, Isource=200µA	2.4V	5.25V
Sink current, PWOK = low		4mA
Source current, PWOK = high		2mA
PWOK delay: $T_{pwok\ on}$	100ms	500ms
PWOK rise and fall time		100µsec
Power down delay: $T_{pwok\ off}$	1ms	200msec

7.3 Power Supply LED Indicators

There will be a single bi-color LED to indicate power supply status. Refer to Table 22 LED Indicators for conditions of the LED.

Table 22: LED and buzzer control rules

Event	**Green LED (on module)**	**Red LED (on module)**	**Buzzer (on cage)**
No AC power plug in.	OFF	Every sec. blink once.	OFF
No AC power plug in, power turn-on	OFF	Every sec. blink once.	ON
AC ok + power turn-off.	Every sec. blink once.	OFF	OFF

AC ok + power turn-on, no failure event.	ON	OFF	OFF
AC ok + power turn-on, module failure event.	OFF	ON	ON
AC ok + power turn-on, warning event.	Green and Red led on every sec exchange of blink.	Green and Red led on every sec exchange of blink.	OFF
AC ok + power turn-on, cage failure event.	OFF	ON	ON

The LED shall be visible on the power supply's exterior face. The LED location shall meet ESD
requirements. LED shall be securely mounted in such a way that incidental pressure on the LED
shall not cause it to become displaced.

7.4 Alarm Sound (RESET BUTTON)

This is an alarm to report the one of the single module is fail in redundant mode. It will be to sound the alarm till the PGIB signal is recovery or push the RESET button.

8. MTBF

Using ***Bellcore***, the calculated MTBF＞100,000 Hrs at 25° C, nominal input..