## **MS-98H7**

## COM Express Type-6 Basic Module



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## Trademarks

All trademarks are the properties of their respective owners.

## **Revision History**

 Revision
 Date

 V1.0
 2018/11

## **Technical Support**

If a problem arises with your system and no solution can be obtained from the user's manual, please contact your place of purchase or local distributor. Alternatively, please visit the MSI website for technical guide, BIOS updates, driver updates and other information, or contact our technical staff via http://www.msi. com/support/

## **Safety Instructions**

- Always read the safety instructions carefully.
- Keep this User's Manual for future reference.
- Keep this equipment away from humidity.
- Lay this equipment on a reliable flat surface before setting it up.
- The openings on the enclosure are for air convection hence protects the equipment from overheating. DO NOT COVER THE OPENINGS.
- Make sure the voltage of the power source and adjust properly 110/220V before connecting the equipment to the power inlet.
- Place the power cord such a way that people can not step on it. Do not place anything over the power cord.
- Always Unplug the Power Cord before inserting any add-on card or module.
- All cautions and warnings on the equipment should be noted.
- Never pour any liquid into the opening that could damage or cause electrical shock.
- If any of the following situations arises, get the equipment checked by service personnel:
  - The power cord or plug is damaged.
  - Liquid has penetrated into the equipment.
  - The equipment has been exposed to moisture.
  - The equipment does not work well or you can not get it work according to User's Manual.
  - The equipment has dropped and damaged.
  - The equipment has obvious sign of breakage.
- DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT UNCONDI-TIONED, STORAGE TEMPERATURE ABOVE 60°C (140°F), IT MAY DAM-AGE THE EQUIPMENT.

## **Chemical Substances Information**

In compliance with chemical substances regulations, such as the EU REACH Regulation (Regulation EC No. 1907/2006 of the European Parliament and the Council), MSI provides the information of chemical substances in products at:

http://www.msi.com/html/popup/csr/evmtprtt\_pcm.html

## **Battery Information**



European Union:

Batteries, battery packs, and accumulators should not be disposed of as unsorted household waste. Please use the public collection system to return, recycle, or treat them in compliance with the local regulations.



Taiwan:

For better environmental protection, waste batteries should be collected separately for recycling or special disposal.



California, USA:

The button cell battery may contain perchlorate material and requires special handling when recycled or disposed of in California.

For further information please visit:

http://www.dtsc.ca.gov/hazardouswaste/perchlorate/

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer.

## **CE Conformity**

Hereby, Micro-Star International CO., LTD declares that this device is in compliance with the essential safety requirements and other relevant provisions set out in the European Directive.

## FCC-B Radio Frequency Interference Statement



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This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver.

- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

- Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1) this device may not cause harmful interference, and

2) this device must accept any interference received, including interference that may cause undesired operation.

## WEEE Statement

Under the European Union ("EU") Directive on Waste Electrical and Electronic Equipment, Directive 2002/96/EC, which takes effect on August 13, 2005, products of "electrical and electronic equipment" cannot be discarded as municipal waste anymore and manufacturers of covered electronic equipment will be obligated to take back such products at the end of their useful life.



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## 1 Overview

Thank you for choosing the MS-98H7, an excellent COM (computeron-module) Express Type-6 Basic Module. Integrating core CPU and memory functionality, it is the entry-level model for applications looking to transition from other small form factor solutions to COM Express<sup>®</sup> and offers full PCI Express, USB, SATA, graphics and network support.

## Specifications

#### Processor

- Intel® Coffee Lake Embedded Mobile Xeon® E/ Core™ i7/ i5/ i3 Processor
  - Intel® Xeon® E-2176M Processor
  - Intel<sup>®</sup> Core™ i7-8850H Processor
  - Intel<sup>®</sup> Core™ i5-8400H Processor
  - Intel<sup>®</sup> Core™ i3-8100H Processor

#### Chipsets

- Mobile Intel<sup>®</sup> PCH-H CM246 Series for Intel<sup>®</sup> Xeon<sup>®</sup> Processor
- Mobile Intel<sup>®</sup> PCH-H QM370 Series

#### Memory

- 2 \* DDR4 SO-DIMM slots
- Supports DDR4 2400/2666 MHz frequency
- Supports ECC Memory (CM246 SKU only)
- Supports non-ECC Memory
- Up to 32 GB

#### LAN

Intel® I219LM GbE-PHY LAN (iAMT 12.x supported)

#### Graphics

- Graphics integrated in Intel<sup>®</sup> processor
- 1 \* LVDS 18/24-Bit Dual Channel
  - LVDS resolution up to 1920x1200 @ 60 Hz
- 3 \* DDI ports support HDMI1.4 or DP1.2 multiplexed (BIOS modification needed)
  - HDMI1.4 up to 4096x2160 @ 24 Hz
  - DP up to 4096x2304 @ 60Hz
  - DVI up to 1920x1200 @ 60Hz
- 1 \* VGA port
  - Resolution up to 1920 x 1080
- 2 Independent Displays supported
  - DDI1+DDI2, DDI1+DDI3, DDI2+DDI3
  - DDI1+LVDS, DDI1+VGA,
  - DDI2+LVDS, DDI2+VGA,
  - DDI3+LVDS, DDI3+VGA
- 3 Independent Displays supported
  - DDI1+DDI2+DDI3
  - DDI1+DDI2+LVDS or VGA
  - DDI1+LVDS+VGA
  - DDI2+LVDS+VGA
  - DDI3+LVDS+VGA

Note: 1. DDI3 default is HDMI (DP by option)

2. VGA is not useable when DDI3 option to DP from HDMI.

#### EC

ITE IT8528 controller chip

#### Storage

- Controller integrated in Intel<sup>®</sup> processor
- Supports 4 Serial ATA interfaces
  - 4 \* SATA 6Gb/s ports
  - AHCI & RAID0/1/5/10

#### USB

- Controller integrated in Intel<sup>®</sup> processor
- 4 \* USB 3.1 (to carrier board)
- 8 \* USB 2.0 (to carrier board)

#### **PCI Express Interface**

- PEG
  - 1 \* PCIe x16 (supports 1 x16 or 2 x8 or 1 x8 or 2 x4)
- PCIe (supports up to 5 devices and 8 lanes)
  - 5 \* PCle x1 or
  - 4 \* PCle x1 + 1 \* PCle x4 or
  - 3 \* PCle x1 + 2 \* PCle x2

#### TPM

Infineon SLB9665TT 2.0 (optional)

#### **Form Factor**

COM Express Type-6 Basic: 125mm x 95mm

#### Environment

- Operating Temperature: -10 ~ 60°C
- Storage Temperature: -20 ~ 80°C
- Humidity: 10% ~ 90% RH, non-condensing

## Layout

DDR4 SO-DIMMs



CPU FAN





# **2** Hardware Setup

This chapter provides you with the information about hardware setup procedures. While doing the installation, be careful in holding the components and follow the installation procedures. For some components, if you install in the wrong orientation, the components will not work properly.

Use a grounded wrist strap before handling computer components. Static electricity may damage the components.

## Memory

The SO-DIMM slot is intended for memory modules.



3. To uninstall the DIMM, flip the slot levers outwards and the DIMM will be released instantly.

#### Important

You can barely see the golden finger if the DIMM is properly inserted in the DIMM slot.

## Connector

#### Fan Power Connector: CPUFAN1

The fan power connectors support system cooling fan with +12V. When connecting the wire to the connectors, always note that the red wire is the positive and should be connected to the +12V; the black wire is Ground and should be connected to GND. If the motherboard has a System Hardware Monitor chipset onboard, you must use a specially designed fan with speed sensor to take advantage of the CPU fan control.



#### Important

Please refer to the recommended CPU fans at processor's official website or consult the vendors for proper CPU cooling fan.

#### **COM Express Connectors**

The COM Express connectors are used to interface the COM Express module board to a carrier board. Connect the COM Express connectors located on the solder side of the module board (as indicated below) to the COM Express connectors on the carrier board.



	Bow A		Bow B		Bow C		Bow D
A1		D1	CND (EIXED)	C1	CND (EIXED)	D1	
Δ2	GRE0 MDI3-	B2	GRE0 ACT#	C2	GND (FIXED)	D2	GND (TIXED)
A2	GBE0_MDI3+	D2 D2	IDC EDAME#	C2		D2	LISB SSTVA
A4	GBE0_NDI3+	D3		C4		D3	
A4	CDE0_LINK1000#	04		04	CND	04	CND
AG	GBE0_LINK1000#	DO	LPC_AD1	65		05	USB SETVA
A0	GBE0_MDI2-	D0	LPC_AD2	C0		00	
A/	GBE0_INDI2+	D/	LPC_AD3	C7	CND	D7	
AO	GBE0_LINK#	DO		0	USB CODY2	00	USB SSTV2
A9	GBE0_MDI1-	B9	1.00.011	69	USB_SSRX2-	D9	USB_SSTX2-
A10	GBEU_MDI1+	B10		C10	USB_SSRX2+	D10	USB_551X2+
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBIN#	C12	USB_SSRX3-	D12	USB_SSTX3-
A13	GBE0_MDI0+	B13	SMB_CK	C13	USB_SSRX3+	D13	USB_SS1X3+
A14	GBE0_CTREF	B14	SMB_DAT	C14	GND	D14	GND
A15	SUS_S3#	B15	SMB_ALERT#	C15		D15	DDI1_CTRLCLK_AUX+
A16	SATA0_TX+	B16	SATA1_TX+	C16		D16	DDI1_CTRLDATA_AUX-
A17	SATA0_TX-	B17	SATA1_TX-	C17	RSVD*	D17	RSVD*
A18	SUS_S4#	B18	SUS_STAT#	C18	RSVD*	D18	RSVD*
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCIE_RX6+	D19	PCIE_TX6+
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCIE_RX6-	D20	PCIE_TX6-
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	SATA2_TX+	B22	SATA3_TX+	C22	PCIE_RX7+	D22	PCIE_TX7+
A23	SATA2_TX-	B23	SATA3_TX-	C23	PCIE_RX7-	D23	PCIE_TX7-
A24	SUS_S5#	B24	PWR_OK	C24	DDI1_HPD	D24	RSVD*
A25	SATA2_RX+	B25	SATA3_RX+	C25		D25	RSVD*
A26	SATA2_RX-	B26	SATA3_RX-	C26		D26	DDI1_PAIR0+
A27	BATLOW#	B27	WDT	C27	RSVD*	D27	DDI1_PAIR0-
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2	C28	RSVD*	D28	RSVD*
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1	C29		D29	DDI1_PAIR1+
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0	C30		D30	DDI1_PAIR1-
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	AC/HDA_BITCLK	B32	SPKR	C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+
A33	AC/HDA_SDOUT	B33	I2C_CK	C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-
A34	BIOS_DIS0#	B34	I2C_DAT	C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL
A35	THRMTRIP#	B35	THRM#	C35	RSVD*	D35	RSVD*
A36	USB6-	B36	USB7-	C36	DDI3 CTRLCLK AUX+	D36	DDI1 PAIR3+
A37	USB6+	B37	USB7+	C37	DDI3 CTRLDATA AUX-	D37	DDI1 PAIR3-
A38	USB 6 7 OC#	B38	USB 4 5 OC#	C38	DDI3 DDC AUX SEL	D38	RSVD*
A39	USB4-	B39	USB5-	C39	DDI3 PAIR0+	D39	DDI2 PAIR0+
A40	USB4+	B40	USB5+	C40	DDI3 PAIR0-	D40	DDI2 PAIR0-
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	C42	DDI3 PAIR1+	D42	DDI2 PAIR1+
A43	USB2+	B43	USB3+	C43	DDI3 PAIR1-	D43	DDI2 PAIR1-
A44	USB 2 3 0C#	B44	USB 0 1 0C#	C44	DDI3 HPD	D44	DDI2 HPD
A45	USB0-	B45	USB1-	C45	RSVD*	D45	RSVD*
A46	USB0+	B46	USB1+	C46	DDI3 PAIR2+	D46	DDI2 PAIR2+
A47	VCC RTC	B47	EXCD1 PERST#	C47	DDI3 PAIR2-	D47	DDI2 PAIR2-
A48	EXCD0 PERST#	B48	EXCD1_CPPE#	C48	RSVD*	D48	RSVD*
A40	EXCD0_CPPE#	B40	SVS RESET#	C49	DDI3 PAIR3+	D49	DDI2 PAIR3+
450		B50	CB RESET#	C50	DDI3 PAIR3.	D50	DDI2 PAIR3-
A51	GND (EIXED)	B51	GND (EIXED)	C51	GND (FIXED)	D51	GND (FIXED)
452	POIE TY5+	B52	POIE RX5+	C52	PEG RX0+	D52	PEG TX0+
A52		D52	POIE DYS	C52	PEG_RX0+	D52	PEG_TX0
A54	GPI0	B54	GPO1	C54	TVPE0#	D54	1 20_1/0-
A55	PCIE TX4+	B55	PCIE RX4+	C55	PEG RX1+	D55	PEG TX1+
456	PCIE TX4	B56	PCIE RX4	C56	PEG RY1-	D56	PEG TX1-
457	GND	B57	GPO2	C57	TVPE1#	D57	TVPE2#
A50	PCIE TX3+	B50	PCIE RX3+	C50	PEG RY2+	D50	PEG TY2+
A50	PCIE TX3	B50	POIE RY3	C50	PEG RY2	D50	PEG TY2
460	GND (EIXED)	B60		C60		D60	GND (FIXED)
A61		D61		C61	DEC DY2+	D61	DEC TY2+
A01		DUI		001	DEC DY2	001	PEG TY2
A62	POIE_TA2-	D02	CDO2	062	PEG_RA3-	D62	PEG_1A3-
A64	POIE TV1+	D03		000	DSVD*	D03	DSVD*
A04		D04		005	RSVD	D04	RSVD
CON	PUIE_IX1-	D00		000	PEG_KX4+	000	
ADD	CDI2	D67	WAREU#	000	PEG_KA4-	000	PEG_1X4-
A07	DOIE TYO	D60	NARE 1#	007	ROVU.	D60	
Age		808		068	PEG_KAS+	068	
A69		869		059		D69	
A/0	GND (FIXED)	B/0	GND (FIXED)	070	GND (FIXED)	D/0	GND (FIXED)
A/1	EDP_D0+/LVDS_A0+	B/1	LVDS_B0+	070	PEG_RX6+	D/1	PEG_1X6+
A/2	EDP_D0-/LVDS_A0-	B/2	LVDS_B0-	072	PEG_RX6-	D/2	PEG_IX6-
A/3	eur_D1+/LVDS_A1+	B/3	LVDS_B1+	073	GND	D/3	GND
A74	eUP_D1-/LVDS_A1-	B74	LVUS_B1-	C74	PEG_RX7+	D74	PEG_TX7+
A75	eDP_D2+/LVDS_A2+	B75	LVDS_B2+	C75	PEG_RX7-	D75	PEG_TX7-
A76	eDP_D2-/LVDS_A2-	B76	LVDS_B2-	C76	GND	D76	GND
A77	eDP_LVDS_VDD_EN	B77	LVDS_B3+	C77	RSVD*	D77	RSVD*
A78	LVDS A3+	B78	LVDS B3-	C78	PEG RX8+	D78	PEG TX8+

	11/20.10			0.80	850 BV/8		DE0 TV0
A/9	LVDS_A3-	B/9	eDP_LVDS_BKL1_EN	C79	PEG_RX8-	D79	PEG_1X8-
A80	GND (FIXED)	B80	GND (FIXED)	C80	GND (FIXED)	D80	GND (FIXED)
A81	eDP_D3+/LVDS_A_CK+	B81	LVDS_B_CK+	C81	PEG_RX9+	D81	PEG_TX9+
A82	eDP_D3-/LVDS_A_CK-	B82	LVDS_B_CK-	C82	PEG_RX9-	D82	PEG_TX9-
A83	eDP_AUX+ / LVDS_I2C_CK	B83	eDP_LVDS_BKLT_CTRL	C83	RSVD*	D83	RSVD*
A84	eDP_AUX-/LVDS_I2C_DAT	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85	PEG_RX10+	D85	PEG_TX10+
A86	SLP_SUS# / RSVD*	B86	VCC_5V_SBY	C86	PEG_RX10-	D86	PEG_TX10-
A87	eDP_HPD / RSVD*	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	PCIE_CLK_REF+	B88	BIOS_DIS1#	C88	PEG_RX11+	D88	PEG_TX11+
A89	PCIE_CLK_REF-	B89	VGA_RED	C89	PEG_RX11-	D89	PEG_TX11-
A90	GND (FIXED)	B90	GND (FIXED)	C90	GND (FIXED)	D90	GND (FIXED)
A91	SPI_POWER	B91	VGA_GRN	C91	PEG_RX12+	D91	PEG_TX12+
A92	SPI_MISO	B92	VGA BLU	C92	PEG RX12-	D92	PEG TX12-
A93	GP00	B93	VGA HSYNC	C93	GND	D93	GND
A94	SPI CLK	B94	VGA VSYNC	C94	PEG RX13+	D94	PEG TX13+
A95	SPI MOSI	B95	VGA I2C CK	C95	PEG RX13-	D95	PEG TX13-
A96	TPM PP	B96	VGA I2C DAT	C96	GND	D96	GND
A97	TYPE10#	B97	SPI_CS#	C97	RSVD*	D97	RSVD*
A98	SER0_TX	B98	RSVD*	C98	PEG_RX14+	D98	PEG_TX14+
A99	SER0_RX	B99	RSVD*	C99	PEG RX14-	D99	PEG TX14-
A100	GND (FIXED)	B100	GND (FIXED)	C100	GND (FIXED)	D100	GND (FIXED)
A101	SER1_TX	B101	FAN_PWMOUT	C101	PEG_RX15+	D101	PEG_TX15+
A102	SER1_RX	B102	FAN_TACHIN	C102	PEG_RX15-	D102	PEG_TX15-
A103	LID#	B103	SLEEP#	C103	GND	D103	GND
A104	VCC 12V	B104	VCC 12V	C104	VCC 12V	D104	VCC 12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC 12V	B107	VCC 12V	C107	VCC 12V	D107	VCC 12V
A108	VCC 12V	B108	VCC 12V	C108	VCC 12V	D108	VCC 12V
A109	VCC 12V	B109	VCC 12V	C109	VCC 12V	D109	VCC 12V
A110	GND (FIXED)	B110	GND (FIXED)	C110	GND (FIXED)	D110	GND (FIXED)

\* RSVD pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

## **Hardware Installation**

### > Installing Module Board onto Carrier Board

#### Important

The illustrations are provided to guide users on how to install the module board onto the carrier board of their choice and should be held for reference only.

1. Remove the protection cover of COM Express connectors on the module board (if there is one).



2. Remove the protection cover of COM Express slot on the carrier board (if there is one).



- 3. Locate the threaded standoffs on the carrier board.

4. Install the module board to the carrier board via the COM Express connectors. Press the module board down firmly.



5. Flip the heat spreader over and remove the protective film from its thermal paste. Mount the heat spreader onto the module board with mounting holes aligned.



6. Use the provided mounting screws to secure the heat spreader to the module board and the carrier board.





# **3** BIOS Setup

This chapter provides information on the BIOS Setup program and allows users to configure the system for optimal use.

Users may need to run the Setup program when:

- An error message appears on the screen at system startup and requests users to run SETUP.
- Users want to change the default settings for customized features.

#### Important

- Please note that BIOS update assumes technician-level experience.
- As the system BIOS is under continuous update for better system performance, the illustrations in this chapter should be held for reference only.

## **Entering Setup**

Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <DEL> key to enter Setup.

Press <DEL> to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system by turning it OFF and On or pressing the RESET button. You may also restart the system by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys.

#### Important

The items under each BIOS category described in this chapter are under continuous update for better system performance. Therefore, the description may be slightly different from the latest BIOS and should be held for reference only.

#### **Control Keys**

$\leftarrow \rightarrow$	Select Screen
$\uparrow \downarrow$	Select Item
Enter	Select
+ -	Change Option
F1	General Help
F7	Previous Values
F9	Optimized Defaults
F10	Save & Reset
Esc	Exit

#### **Getting Help**

After entering the Setup menu, the first menu you will see is the Main Menu.

#### Main Menu

The main menu lists the setup functions you can make changes to. You can use the arrow keys ( $\uparrow\downarrow$ ) to select the item. The on-line description of the highlighted setup function is displayed at the bottom of the screen.

#### Sub-Menu

If you find a right pointer symbol appears to the left of certain fields that means a sub-menu can be launched from this field. A sub-menu contains additional options for a field parameter. You can use arrow keys ( $\uparrow\downarrow$ ) to highlight the field and press <Enter> to call up the sub-menu. Then you can use the control keys to enter values and move from field to field within a sub-menu. If you want to return to the main menu, just press the <Esc >.

#### General Help <F1>

The BIOS setup program provides a General Help screen. You can call up this screen from any menu by simply pressing <F1>. The Help screen lists the appropriate keys to use and the possible selections for the highlighted item. Press <Esc> to exit the Help screen.

## The Menu Bar



#### ► Main

Use this menu for basic system configurations, such as time, date, etc.

#### Advanced

Use this menu to set up the items of special enhanced features.

#### ▶ Boot

Use this menu to specify the priority of boot devices.

#### ▶ Security

Use this menu to set supervisor and user passwords.

#### ▶ Chipset

This menu controls the advanced features of the onboard chipsets.

#### ▶ Power

Use this menu to specify your settings for power management.

#### ► Save & Exit

This menu allows you to load the BIOS default values or factory default settings into the BIOS and exit the BIOS setup utility with or without changes.

## Main

Aptio Setup Ut: Main Advanced Boot Secur:	il <mark>ity – Copyright (C) 2018 America</mark> ity Chipset Power Save & Exit	n Megatrends, Inc.			
System Date System Time	[Thu 11/15/2018] [13:23:41]	Set the Date. Use Tab to switch between Date elements.			
SATA1 SATA2 SATA3 SATA4	Empty Empty Empty Empty				
SATA Mode Selection	(AHCI)				
USB Devices: 1 Drive, 1 Keyboard, 1	Mouse				
Intel(R) Core(TM) i5-8400H CF	²U @ 2.50GHz	++: Select Screen			
Processor ID BIOS Version	0x906EA E98H7IMS V1.0b11 111518	f∔: Select Item Enter: Select			
EC Version	EC98H7MS V1.0b7	+/-: Change Opt.			
Total Memory	8192 MB (DDR4)	1: deneratives F7: Previous Values F9: Optimized Defaults F10: Save & Reset ESC: Exit			
Version 2.20.1271. Copyright (C) 2018 American Megatrends, Inc.					

#### ► System Date

This setting allows you to set the system date. The date format is <Day>, <Month> <Date> <Year>.

#### ► System Time

This setting allows you to set the system time. The time format is <Hour> <Minute> <Second>.

#### ► SATA Mode Selection

This setting specifies the SATA controller mode.

## Advanced

Aptio Setup Utility – Main Advanced Boot Security Chi	Copyright (C) 2017 American pset Power Save & Exit	Megatrends, Inc.
Full Screen Logo Display Bootup NunLock State Option ROM Messages CPU Configuration Super ID Configuration I T18528 Jayer ID Configuration I T18528 Samert Fan Configuration PCL/PCIE Device Configuration GPID Group Configuration	(Disbled) [Dn] [Fonce BIDS]	Enables or disables Full Screen Logo Display option ++: Select Screen 14: select Item Enter: Select
		+/-: Change Opt. F1: General Help F7: Previous Values F9: Optimized Defaults F10: Save & Reset ESC: Exit
Version 2.18.1263. Co	)pyright (C) 2017 American M	legatrends, Inc.

#### ▶ Full Screen Logo Display

This BIOS feature determines if the BIOS should hide the normal POST messages with the motherboard or system manufacturer's full-screen logo.

When it is enabled, the BIOS will display the full-screen logo during the boot-up sequence, hiding normal POST messages.

When it is disabled, the BIOS will display the normal POST messages, instead of the full-screen logo.

Please note that enabling this BIOS feature often adds 2-3 seconds of delay to the booting sequence. This delay ensures that the logo is displayed for a sufficient amount of time. Therefore, it is recommended that you disable this BIOS feature for a faster boot-up time.

#### Bootup NumLock State

This setting is to set the Num Lock status when the system is powered on. Setting to [On] will turn on the Num Lock key when the system is powered on. Setting to [Off] will allow users to use the arrow keys on the numeric keypad.

#### Option ROM Messages

This item is used to determine the display mode when an optional ROM is initialized during POST. When set to [Force BIOS], the display mode used by AMI BIOS is used. Select [Keep Current] if you want to use the display mode of optional ROM.

#### ► CPU Configuration



#### Intel Virtualization Technology

Virtualization enhanced by Intel Virtualization Technology will allow a platform to run multiple operating systems and applications in independent partitions. With virtualization, one computer system can function as multiple "Virtual" systems.

#### Active Processor Cores

This setting specifies the number of active processor cores.

#### ► Hyper-Threading

The processor uses Hyper-Threading technology to increase transaction rates and reduces end-user response times. The technology treats the two cores inside the processor as two logical processors that can execute instructions simultaneously. In this way, the system performance is highly improved. If you disable the function, the processor will use only one core to execute the instructions. Please disable this item if your operating system doesn't support HT Function, or unreliability and instability may occur.

#### Intel(R) SpeedStep(TM)

EIST (Enhanced Intel SpeedStep Technology) allows the system to dynamically adjust processor voltage and core frequency, which can result in decreased average power consumption and decreased average heat production. When disabled, the processor will return the actual maximum CPUID input value of the processor when queried.

#### ► C States

C-state performance indicates the ability to run the processor in lower power states when the PC is idle. This setting enables/disables the C-State Configuration for power saving purposes.



#### Super IO Configuration (the Carrier Board)

#### Serial Port 1, Serial Port 2

This setting enables/disables the specified serial port.

#### Change Settings

This setting is used to change the address & IRQ settings of the specified serial port.

#### ► Mode Select

Select an operation mode for the serial port 1/2.

#### Parallel Port

This setting enables/disables the parallel port.

#### ► Change Settings

This setting is used to change the address & IRQ settings of the parallel port.

#### ► Device Mode

Select an operation mode for the parallel port.

#### ► FIFO Mode

This setting controls the FIFO data transfer mode.

#### ► Shared IRQ Mode

This setting provides the system with the ability to share interrupts among its serial ports.

#### Watch Dog Timer

You can enable the system watch-dog timer, a hardware timer that generates a reset when the software that it monitors does not respond as expected each time the watch dog polls it.

#### ▶ IT8528 Super IO Configuration



#### Serial Port 3, Serial Port 4

This setting enables/disables the specified serial port.

#### ► Change Settings

This setting is used to change the address & IRQ settings of the specified serial port.

#### ► Watch Dog Timer

You can enable the system watch-dog timer, a hardware timer that generates a reset when the software that it monitors does not respond as expected each time the watch dog polls it.

#### ► IT8528 H/W Monitor (the Compact Module)

These items display the current status of all monitored hardware devices/ components such as voltages, temperatures and all fans' speeds.

Advanced	
PC Health Status	
CPU Temprature	: +57 C
CPUFAN1 Speed	: N/A
12V 5VSB VSB3 VCore VBAT	: +12.090 V : +5.202 V : +3.336 V : +0.840 V : +3.036 V

Advanced	
IT8528 Smart Fan Configuration	

► IT8528 Smart Fan Configuration (the Compact Module)

#### ► CPUFAN1

These settings enable/disable the Smart Fan function. Smart Fan is an excellent feature which will adjust the CPU/system fan speed automatically depending on the current CPU/system temperature, avoiding the overheating to damage your system.

#### ▶ PCI/PCIE Device Configuration



#### ► Legacy USB Support

Set to [Enabled] if you need to use any USB 1.1/2.0 device in the operating system that does not support or have any USB 1.1/2.0 driver installed, such as DOS and SCO Unix.

#### ► Audio Controller

This setting enables/disables the onboard audio controller.

#### Launch Onboard LAN OpROM

This setting enables/disables the initialization of the specified LAN Boot ROM during bootup. Selecting [Disabled] will speed up the boot process.

• GPIO Group Configuration (the Carrier Board)

Aptio Setup Advanced	Utility – Copyright (C) 2018
GPIO Group Configuration	
JGP101: GP00 GP01 GP02 GP03	(Low) (Low) (Low) (Low)
JGP102: GP00 GP01 GP02 GP03	[Low] [Low] [Low] [Low]

▶ JGPIO1/ 2: GPO0 ~ GPO3

These settings control the operation mode of the specified GPIO.

## Boot



#### ► CSM Support

This setting enables/disables the support for Compatibility Support Module, a part of the Intel Platform Innovation Framework for EFI providing the capability to support legacy BIOS interfaces.

#### ▶ Video

Select the type of primary video for your system.

#### Boot Option Priorities

This setting allows users to set the sequence of boot devices where BIOS attempts to load the disk operating system.

#### Hard Drive BBS Priorities

This setting allows users to set the priority of the specified devices. First press <Enter> to enter the sub-menu. Then you may use the arrow keys ( $\uparrow\downarrow$ ) to select the desired device, then press <+>, <-> or <PageUp>, <PageDown> key to move it up/down in the priority list.

## Security

Aptio Setup Utility – Copyright (C) 2018 Main Advanced Boot <mark>Security </mark> Chipset Power Save &	American Megatrends, Inc. Exit
Administrator Password User Password Intel Bios Gward Support [Disabled] Intel Trusted Execution Technology [Disabled] > PCH-FN Configuration > Trusted Computing > Serial Port Console Redirection	Set Administrator Password
	<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F7: Previous Values F9: Optimized Defaults F10: Save &amp; Reset ESC: Exit</pre>

#### Administrator Password

Administrator Password controls access to the BIOS Setup utility.

#### ► User Password

User Password controls access to the system at boot and to the BIOS Setup utility.

#### ▶ Intel BIOS Guard Support

Intel BIOS Guard Support ensures that updates to system BIOS flash are secure.

#### Intel Trusted Execution Technology

Intel Trusted Execution Technology provides highly scalable platform security in physical and virtual infrastructures.

#### PCH-FW Configuration

This menu provides settings for PCH-FW Configuration.



► Firmware Update Configuration



#### ME FW Image Re-Flash

This setting enables/disables the ME FW image reflash.

#### ▶ PTT Configuration

Intel Platform Trust Technology (PTT) is a platform functionality for credential storage and key management used by Microsoft Windows.



#### ► ME Debug Configuration

This menu provides settings for ME Debug Configuration.

Secur.	ity
HECI Timeouts	
Force ME DID Init Status CPU Replaced Polling Disable ME DID Message HECI Retry Disable HECI Message check Disable MBP HOG Skip HECI2 Interface Communication KT Device End Of Post Message DOIS Setting for HECI Disable MCTP Broadcast Cycle	[Disabled] [Disabled] [Enabled] [Disabled] [Disabled] [Disabled] [Enabled] [Enabled] [Send in OXE] 2 [Disabled] [Disabled]

#### ► AMT Configuration

Intel Active Management Technology (AMT) is hardware-based technology for remotely managing and securing PCs out-of-band.



#### Trusted Computing



#### Security Device Support

This setting enables/disables BIOS support for security device. When set to [Disable], the OS will not show security device. TCG EFI protocol and INT1A interface will not be available.

#### SHA-1 PCR Bank, SHA256 PCR Bank

These settings enable/disable the SHA-1 PCR Bank and SHA256 PCR Bank.

#### Pending Operation

This setting shows pending operation.

#### ▶ Platform Hierarchy, Storage Hierarchy, Endorsement Hierarchy

These settings enable/disable the Platform Hierarchy, Storage Hierarchy and Endorsement Hierarchy.

#### TPM2.0 UEFI Spec Version, Physical Presence Spec Version

This settings show the TPM2.0 UEFI Spec Version and Physical Presence Spec Version.

#### ► TPM2.0 Interface Type

This setting shows the TPM2.0 Interface Type.

#### ▶ Serial Port Console Redirection



#### ► Console Redirection

Console Redirection operates in host systems that do not have a monitor and keyboard attached. This setting enables/disables the operation of console redirection. When set to [Enabled], BIOS redirects and sends all contents that should be displayed on the screen to the serial COM port for display on the terminal screen. Besides, all data received from the serial port is interpreted as keystrokes from a local keyboard.

#### Console Redirection Settings (COM1)



#### ► Terminal Type

To operate the system's console redirection, you need a terminal supporting ANSI terminal protocol and a RS-232 null modem cable connected between the host system and terminal(s). This setting specifies the type of terminal device for console redirection.

#### Bits per second, Data Bits, Parity, Stop Bits

This setting specifies the transfer rate (bits per second, data bits, parity, stop bits) of Console Redirection.

#### ► Flow Control

Flow control is the process of managing the rate of data transmission between two nodes. It's the process of adjusting the flow of data from one device to another to ensure that the receiving device can handle all of the incoming data. This is particularly important where the sending device is capable of sending data much faster than the receiving device can receive it.

#### ▶ VT-UTF8 Combo Key Support

This setting enables/disables the VT-UTF8 combination key support for ANSI/VT100 terminals.

#### ▶ Recorder Mode, Resolution 100x31

These settings enable/disable the recorder mode and the resolution 100x31.

#### ► Putty Keypad

PuTTY is a terminal emulator for Windows. This setting controls the numeric keypad for use in PuTTY.

#### ▶ Legacy Console Redirection Settings



#### Redirection COM Port

This setting selects a COM port to display redirection of Legacy OS and Legacy OPROM Messages

#### Resolution

In Legacy OS, this setting selects the Number of Rows and Columns supported redirection.

#### ▶ Redirect After POST

When Boot loader is selected, Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, Legacy Console Redirection is enabled for legacy OS.

 Console Redirection Settings (Serial port for Out-of-Band Management/ Windows Emergency Management Services)

	Security
Out-of-Band Mgmt Port	[COM1]
Terminal Type	[VT-UTF8]
Bits per second	[[115200]
Flow Control	[None]
Data Bits	8
Parity	None
Stop Bits	1

#### ▶ Out-of-Band Mgmt Port

Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.

#### ► Terminal Type

VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100.

#### Bits per second

This setting selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

#### ► Flow Control

Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.

## Chipset

Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc. Main Advanced Boot Security <mark>Chipset</mark> Power Save & Exit			
Primary Display DWHT Pre-Allocated DWHT Total Gfx Mem Primary IGFX Boot Display LVDS LCDP Panel Type LVDS Backlight Control	[Auto] [32M] [256M] [M3IOS Default] [Enabled] [800x 600 & 18bit] [Level 3]	Select which of Auto/IGFX/PEG Braphics device should be Primary Display for Switchable Gfx.	
		++: Select Screen 14: Select Item Enter: Select +/-: Charge Opt. F1: General Help F7: Previous Values F9: optimized Defaults F10: Save & Reset ESC: Exit	
Version 2.20.1271. Copyright (C) 2018 American Megatrends, Inc.			

#### Primary Display

This setting selects the primary display.

#### DVMT Pre-Allocated

This setting defines the DVMT pre-allocated memory. Pre-allocated memory is the small amount of system memory made available at boot time by the system BIOS for video. Pre-allocated memory is also known as locked memory. This is because it is "locked" for video use only and as such, is invisible and unable to be used by the operating system.

#### DVMT Total Gfx Mem

This setting specifies the memory size for DVMT.

#### Primary IGFX Boot Display

Use the field to select the type of device you want to use as the display(s) of the system.

#### LVDS

This setting enables/disables the LVDS interface.

#### ► LCD Panel Type

This setting specifies the LCD panel type.

#### LVDS Backlight Control

This setting controls the intensity of the LVDS backlight.

### Power

Aptio Setup Utility Main Advanced Boot Security	y – Copyright (C) 2017 Ame Chipset Power Save & Ex	erican Megatrends, Inc. Kit
Restore AC power Loss Deep Sleep Mode	[Last State] [S5]	Select AC power state when power is re-applied after a
Advanced Resume Events Control OnChild BGE/USB PCIE PME/Ring RTC	[Enabled] [Disabled] [Disabled]	
		<pre>+: Select Screen 1: Select Item Enter: Select +/-: Change Opt. F1: General Help F7: Previous Values F9: Optimized Defaults F10: Save &amp; Reset ESC: Exit</pre>
Version 2,18,1269.	. Copyright (C) 2017 Ameri	ican Mexatrends. Inc.

#### ▶ Restore AC Power Loss

This setting specifies whether your system will reboot after a power failure or interrupt occurs. Available settings are:

[Power Off]	Leaves the computer in the power off state.
[Power On]	Leaves the computer in the power on state.
[Last State]	Restores the system to the previous status before power failure or interrupt occurred.

#### ► Deep Sleep Mode

The setting enables/disables the Deep S5 power saving mode. S5 is almost the same as G3 Mechanical Off, except that the PSU still supplies power, at a minimum, to the power button to allow return to S0. A full reboot is required. No previous content is retained. Other components may remain powered so the computer can "wake" on input from the keyboard, clock, modem, LAN, or USB device.

#### \*\* Advanced Resume Events Control \*\*

#### ► OnChip GbE/USB

This field specifies whether the system will be awakened from power saving modes when the activity of USB devices or input signal of onchip LAN is detected.

#### ► PCIE PME/Ring

This field specifies whether the system will be awakened from power saving modes when input signals on the serial Ring Indicator (RI) line or input signals of onboard PCIE PME are detected.

#### ► RTC

When [Enabled], your can set the date and time at which the RTC (real-time clock) alarm awakens the system from suspend mode.

## Save & Exit

Aptio Setup Utility - Copyright (C) 2017 America Main Advanced Prot Copyright Chicago Pryon Source & Suit	n Megatrends, Inc.
Hain Huvanced Boot Security Chipset Power save & Exit	
Save Dhanges and Reset Discard Changes and Exit Discard Changes	Reset the system after saving the changes.
Load Optimized Defaults Save as User Defaults Restore User Defaults	
Launch EFI Shell from filesystem device	
	++: Select Screen ↑↓: Select Item
	Enter: Select +/-: Change Opt.
	F1: General Help F7: Previous Values
	F9: Optimized Defaults F10: Save & Reset
	ESC: Exit
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#### ▶ Save Changes and Reset

Save changes to CMOS and reset the system.

#### Discard Changes and Exit

Abandon all changes and exit the Setup Utility.

#### Discard Changes

Abandon all changes.

#### Load Optimized Defaults

Use this menu to load the default values set by the motherboard manufacturer specifically for optimal performance of the motherboard.

#### Save as User Defaults

Save changes as the user's default profile.

#### Restore User Defaults

Restore the user's default profile.

#### ► Launch EFI Shell from filesystem device

This setting helps to launch the EFI Shell application from one of the available file system devices.



## Appendix GPIO WDT BKL Programming

This appendix provides WDT (Watch Dog Timer), GPIO (General Purpose Input/ Output) and LVDS Backlight programming guide.

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LVDS Backlight Brightness Control	A-6
SMBus Access	A-7
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## Abstract

In this document, code examples based on C programming language are provided for customer interest. **Inportb**, **Outportb**, **Inportl** and **Outportl** are basic functions used for access IO ports and defined as following.

Inportb: Read a single 8-bit I/O port.
Outportb: Write a single byte to an 8-bit port.
Inportl: Reads a single 32-bit I/O port.
Outportl: Write a single long to a 32-bit port.

## **General Purposed IO**

#### 1. General Purposed IO – GPIO/DIO

The associated access method (EC\_ReadByte, EC\_WriteByte) are provided in part 5. The GPIO port configuration offset in EC and addresses are listed in the following table:

Name	OFFSET	IO address	Name	OFFSET	IO address
N_GPI0	0x97	Bit 0	N_GPO0	0x97	Bit 4
N_GPI1	0x97	Bit 1	N_GPO1	0x97	Bit 5
N_GPI2	0x97	Bit 2	N_GPO2	0x97	Bit 6
N_GPI3	0x97	Bit 3	N_GPO3	0x97	Bit 7

#### 1.1 Set output value of GPO

- 1. Read the value from the OFFSET in EC RAM of GPO.
- 2. Set the value of GPO address.
- 3. Write the value back to the OFFSET in EC RAM of GPO.

#### Example: Set N\_GPO0 output "high"

val = EC_ReadByte (0x97);	// Read value from <b>N_GPO0</b> .
val = val   (1<<4);	// Set N_GPO0 address (bit 4) to 1 (output "high").
EC_WriteByte (0x97, val);	// Write back to N_GPO0.

#### Example: Set N\_GPO1 output "low"

val = EC_ReadByte (0x97);	// Read value from N_GPO1.
val = val & (~(1<<5));	// Set N_GPO1 address (bit 5) to 0 (output "low").
EC_WriteByte (0x97, val);	// Write back to <b>N_GPO1</b> .

#### 1.2 Read input value from GPI

- 1. Read the value from the OFFSET in EC of GPI.
- 2. Get the value of GPI address.

#### Example: Get N\_GPI2 input value.

val = EC_Re	eadByte ( <mark>0x97</mark> );		// Read value from N_GPI2.
val = val &	(1<< <mark>2</mark> );		// Check N_GPI2 address (bit 2).
if (val)	printf ("Input of	N_GPI2	is High");
else	printf ("Input of	N_GPI2	is Low");

## Watchdog Timer

#### 2. Watchdog Timer – WDT

The watchdog timer unit is in second. It starts immediately after setting time. The counter value will increase per second. When the counter value equals the setting time, WDT will reset the system. Associated access method (**EC\_ReadByte** and **EC\_WriteByte**) are provided in part 5.

#### 2.1 Set WDT Time and Enable WDT

EC_WriteByte (0x98, <u>Time</u> );	// Enable WDT immediately after setting WDT time, value 1 to 255.
EC_WriteByte (0x99, 0);	// Set counter to 0. WDT start all over

#### 2.2 Disable WDT

EC_WriteByte (0x99, 0);	// Set counter to 0
EC_WriteByte (0x98, 0);	// Disable WDT after setting WDT time to 0

## LVDS Backlight Brightness Control

#### 3. LVDS Backlight Brightness Control

The LVDS controller support 17 level of backlight brightness value from 0 (30%) to 16 (100%) and it is accessible through SMBus. The associated access method (SMBus\_ReadByte, SMBus\_WriteByte) are provided in part 4.

#### 3.1 Set the Level of LVDS Backlight

- 1. Write **0xED** into address **0x7F** on SMBus device **0x42**.
- Write desired backlight level from 0x0 (30%) to 0x10 (100%) into address 0x6E on SMBus device 0x42.

Example: Set LVDS backlight level to 0x10 (100%) SMBus\_WriteByte (0x42, 0x7F, 0xED); SMBus WriteByte (0x42, 0x6E, 0x10); // Set brightness to 100%

#### 3.2 Read the Level of LVDS Backlight

1. Write 0xED into address 0x7F on SMBus device 0x42.

2.Read current backlight level from address 0x6E on SMBus device 0x42.

Example: Get LVDS backlight level

SMBus\_WriteByte (0x42, 0x7F, 0xED);

BKL\_Value = SMBus\_ReadByte (0x42, 0x6E);

### **SMBus Access**

#### 4. SMBus Access

The base address of SMBus must be known before access. The relevant bus and device information are as following.

#define IO_SC	0xCF8
#define IO_DA	0xCFC
#define PCIBASEADDRESS	0x8000000
#define PCI_BUS_NUM	0
#define PCI_DEV_NUM	31
#define PCI_FUN_NUM	4

#### 4.1 Get SMBus Base Address

int SMBUS\_BASE; int DATA\_ADDR = PCIBASEADDRESS + (PCI\_BUS\_NUM<<16) + (PCI\_DEV\_NUM<<11) + (PCI\_FUN\_NUM<<8); Outporti (DATA\_ADDR + 0x20, IO\_SC); SMBUS\_BASE = Inporti (IO\_DA) & 0xffffff0;

#### 4.2 SMBus\_ReadByte (char DEVID, char OFFSET)

 Read the value of OFFSET from SMBus device DEVID.

 Outportb (LOWORD (SMBUS\_BASE), 0xFE);

 Outportb (LOWORD (SMBUS\_BASE) + 0x04, DEVID + 1);
 // out Base + 04, (DEVID + 1)

 Outportb (LOWORD (SMBUS\_BASE) + 0x03, OFFSET);
 // out Base + 03, OFFSET

 Outportb (LOWORD (SMBUS\_BASE) + 0x02, 0x48);
 // out Base + 02, 48H

 mdelay (20);
 // delay 20ms to let data ready

 while ((InportI (SMBUS\_BASE) & 0x01) != 0);
 // wait SMBus ready

 SMB\_DATA = Inportb (LOWORD (SMBUS\_BASE) + 0x05);
 // input Base + 05

#### 4.3 SMBus\_WriteByte (char DEVID, char OFFSET, char DATA)

 Write DATA to OFFSET on SMBus device DEVID.

 Outportb (LOWORD (SMBUS\_BASE), 0xFE);

 Outportb (LOWORD (SMBUS\_BASE) + 0x04, DEVID);
 // out Base + 04, (DEVID)

 Outportb (LOWORD (SMBUS\_BASE) + 0x03, OFFSET);
 // out Base + 03, OFFSET

 Outportb (LOWORD (SMBUS\_BASE) + 0x05, DATA);
 // out Base + 05, DATA

 Outportb (LOWORD (SMBUS\_BASE) + 0x02, 0x48);
 // out Base + 02, 48H

 mdelay (20);
 // wait 20ms

## **Embedded Controller**

#### 5. Embedded Controller – EC Access

The relevant control information are as following.

#EC_CMD_PORT	0x66	// EC command por
#EC_DATA_PORT	0x62	// EC data port
#EC_DELAY	100	
#EC_STAT_OBF	0x1	// bit 0: OBF
#EC_STAT_IBF	0x2	// bit 1: IBF

#### 5.1 WaitPortStatus (char BITS, bool ONOFF)

```
int time=0, tick= EC_DELAY;
bool state;
for (time = 0; time < EC_DELAY*100; time += tick) // *100 is the loop count to avoid infinite wait
{
    udelay (EC_DELAY); // Delay 100us to let data ready
    char data= Inportb (EC_CMD_PORT);
    state = ((data & BITS) !=0 ); // Check EC status of desired bits
    if (state == ONOFF) {
        break;
    }
}
```

#### 5.2 EC\_ReadByte (char OFFSET)

Read the value from <b>OFFSET</b> of EC RAM.	
WaitPortStatus (EC_STAT_IBF, false);	// Wait IBF = 0
Outportb (EC_CMD_PORT, 0x80);	// 0x80: EC read command
WaitPortStatus (EC_STAT_IBF, false);	// Wait IBF = 0
Outportb (EC_DATA_PORT, <b>OFFSET</b> );	// Write OFFSET to EC_DATA_PORT
WaitPortStatus (EC_STAT_OBF, true);	// Wait OBF = 1
EC_DATA = Inportb (EC_DATA_PORT);	// Get value from EC_DATA_PORT

#### 5.3 EC\_WriteByte (char OFFSET, char DATA)

Write DATA to OFFSET of EC RAM. WaitPortStatus (EC\_STAT\_IBF, false); Outportb (EC\_CMD\_PORT, 0x81); WaitPortStatus (EC\_STAT\_IBF, false); Outportb (EC\_DATA\_PORT, OFFSET); WaitPortStatus (EC\_STAT\_IBF, false); Outportb (EC\_DATA\_PORT, DATA); WaitPortStatus (EC\_STAT\_IBF, false);

// Wait IBF = 0
// Ox81: EC write command
// Wait IBF = 0
// Write OFFSET to EC\_DATA\_PORT
// Wait IBF = 0
// Write DATA to EC\_DATA\_PORT
// Wait IBF = 0