電氣規格書

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FSP2000-20FM

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全漢企業股份有限公司
FSP TECHNOLOGY INC.

SPECIFICATION

FSP2000-20FM

2000W Redundant Power Supply Module

CRPS V2.0

Feb.26.2020

全漢企業股份有限公司
FSP TECHNOLOGY INC.

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1. REVISION LOG

This section contains the release history of this document:

Date	Revision	Section	Issue
2019/08/27	1.0		Origin
2020/02/26	1.1		Modify 3.2.2 Output rating Modify 4.2 Over Current Warning, Over Current & Over Power Protection (OCW, OCP & OPP) Modify 4.3 Over Temperature Protection (OTP)

APPROVE	Jerry Tsai	CHECK	Jacky Chen	PREPARE	Fen Lin

2. GENERAL SCOPE

This specification describes the performance characteristic of a 2000W AC-DC or HVDC switching redundant power supply.

2.1 Mechanical Overview

The physical size of the power supply enclosure is intended to accommodate the power range of up to 2000W. The physical size is 39/40mm x 73.5mm x185mm (height x width x length).

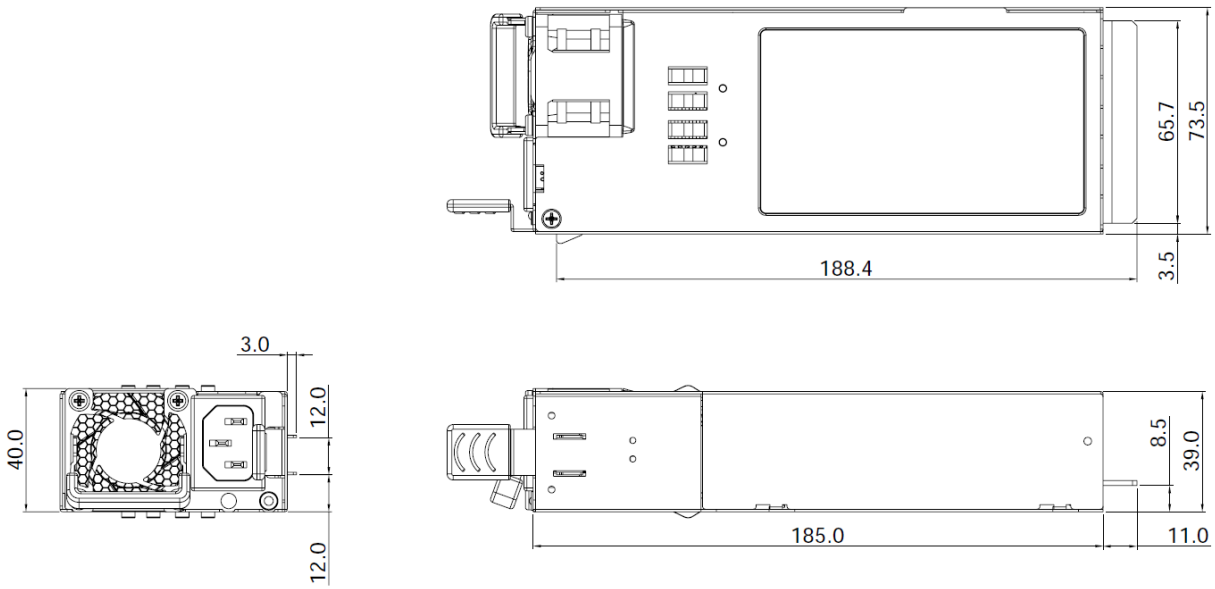


Figure 1 – Power Supply Dimension

2.2 LED Marking and Identification

The power supply shall have LED for indication of the power supply status.

Table 1 – LED Status Information

Power supply condition	Power supply LED
Output ON and OK	Green
No AC power to all PSU	OFF
AC present/only standby output on	1Hz Flashing Green (0.5s:OFF、0.5s : Green)
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	Amber
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber (0.5s:OFF、0.5s : Amber)
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	Amber
Smart Redundant state	0.33Hz Blink Green (1s:OFF、2s : Green)
Power supply FW update mode	2Hz Blink Green

2.3 Environmental Requirements

The power supply shall operate within all specified limits over specified conditions in 2.3.

The defined operation condition includes temperature, humidity, altitude, shock and vibration.

2.3.1 Temperature and Humidity Requirements

The power supply shall operate within all specified limits over T_{op} temperature range and specified humidity Range. All airflow shall pass through the power supply and not over the exterior surfaces of the power supply.

The power supply shall withstand thermal storage specified in $T_{non\text{-}OP}$ without any damage.

Table 2 – Temperature Requirements

Item	Description	MIN	MAX	Unit
T_{OP}	Operating temperature range.	0	55	℃
$T_{non\text{-}OP}$	Non-Operating temperature range.	-40	70	℃
H_{OP}	Operating humidity range, non-condensing		90	%
$H_{non\text{-}OP}$	Non-Operating humidity range, non-condensing		95	%

2.3.2 Altitude Requirements

The power supply shall operate within all specified limits over A_{op} Altitude range. The change pressure condition shall not harm the power supply and the operation within specified regulations shall be assured.

The power supply shall withstand Altitude storage specified in $A_{non\text{-}OP}$ without any damage.

Table 3 – Altitude Requirements

Item	Description	MIN	MAX	Unit
A_{OP}	Operating Altitude range.	0	5000	m
$A_{non\text{-}OP}$	Non-Operating Altitude range.	0	15000	m

3. ELECTRICAL PERFORMANCE

3.1 AC power Input Specification

3.1.1 AC Inlet connector

The power supply shall incorporate an AC input connector complying with IEC 320 C-14 power inlet connector specification.

3.1.2 Input voltage and frequency specification

The power supply shall operate within all specified limits over the following input range. Harmonic distortions of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits.

The power supply shall power off, if the AC input is below 75Vac (75-85Vac delay 20 seconds power off) and shall start (auto recover) if AC input is exceed 87Vac.

Table 4 – Rated output power for each input voltage range

Parameter	Min	Rated Input	Max	Start up VAC	Power Off VAC
Low line(VAC)	90	100-127	140	87V	75-85V
High line(VAC)	180	200-240	264		
Frequency(Hz)	47	50/60	63		

Note: When Vin is 75~85Vac, 0 ~ 1 seconds 0x7C (Status Input) will display a warn, >20 seconds 0x7C (Status Input) will display warn & Fault, the power will shut down.

3.1.3 HVDC Input voltage

The power supply supports High Voltage Direct Current (HVDC) input. Allowed HVDC input range as shown in below table. The power supply shall operate within all specified limits, when HVDC input meet requirements defined in this chapter.

Table 5 – HVDC input voltage range

Parameter	Minimum input	Rated Input	Maximum input	Start up VDC	Power Off VDC
HVDC	180V	240V	310V	175V ±4V	165V ±5V

3.1.4 AC Line Fuse

The power supply shall incorporate one input fuse on the line side for input over-current protection to prevent damage to the power supply and meet product safety requirements. AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.1.5 AC line inrush

AC line inrush current shall not exceed 35A peak, for up to one-quarter of the AC cycle, after which, the input current should be no more than the specified maximum input current. The peak inrush current shall be less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

3.1.6 Power Factor and iTHD

The power supply must meet the power factor and current iTHD requirements are stated below. These requirements are within the Energy Star® Program Requirements for Computer Servers.

Table 7 – Power Factor Correction

Output power	10% load	20% load	50% load	100% load
Power factor	> 0.90	> 0.96	> 0.98	> 0.99
Input conditions	200VAC to 240VAC & 50Hz / 60Hz			

Table 8 – iTHD Requirements

Output power	> 5% & ≤ 10%	> 10% & < 20%	≥ 20%	≥ 40%	≥ 50%
Current iTHD	< 20%	< 15%	≤10%	≤8%	≤5%
Input conditions	200VAC to 240VAC & 50Hz / 60Hz				

3.1.7 AC line dropout/ Hold up

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration shall not cause tripping of control signals or protection circuits other than the SMBAlert# signal. If the AC dropout lasts longer than the holdup time the power supply should recover and meet all turn on requirements. The power supply shall meet the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration shall not cause damage to the power supply.

Table 8 –dropout time until Power output goes out of regulations

PSU	70% of Max. Load
2000W	>10mS

The +12VSB output voltage shall stay in regulation under its full load (static or dynamic) during an AC dropout duration up to 70msec whether the power supply is in ON or OFF state (PSON# asserted or de-asserted).

3.1.8 Efficiency

The redundant power supply module efficiency should meet at least Climate Saver 3 / 80Plus Platinum rating, specified in below table. The efficiency should be measured at 230VAC and with external fan power according to Climate Saver / 80Plus efficiency measurement specifications (CSCI-09-10)

Table 9 – module efficiency requirements

Efficiency Std.	20% load (12V is 32.2A, 12vsb is 0.6A)	50% load (12V is 80.5A, 12vsb is 1.5A)	100% load (12V is 161A, 12vsb is 3A)
Platinum	90%	94%	91%

3.1.9 Susceptibility Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter, which meets the criteria defined in the SSI document EPS Power Supply Specification.

Table 10 – Performance criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec. limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.1.9.1 Electrical Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024:1998 using the IEC 61000-4-2:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

3.1.9.2 Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024:1998 using the IEC 61000-4-4:1995 test standard and performance criteria B define in Annex B of CISPR 24.

3.1.9.3 Radiated Immunity

The power supply shall comply with the limits defined in EN55024:1998 using the IEC61000-4-3:1995 test standard and performance criteria A defined in Annex B of CISPR 24.

3.1.9.4 Surge Immunity

The power supply shall be tested with the system for immunity to AC Ring wave and AC Unidirectional wave, both up to 2kV(Differential mode 1K,Common mode 2K), per EN55024:1998, EN 61000-4-5:1995 and ANSI C62.45:1992.
The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.
The power supply shall comply with the limits defined in EN55024:1998 using the IEC 61000-4-5:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

3.1.9.5 AC Line Transient Specification

AC line transient conditions shall be defined as “sag” and “surge” conditions.

“Sag” conditions are also commonly referred to as “brownout”, these conditions will be defined as the AC line voltage dropping below nominal voltage conditions.

“Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.
The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 11 – AC Line SAG transient performance.

AC Line Sag (10sec interval between each sagging)				
Duration	**Sag**	**Operating AC voltage**	**Line frequency**	**Performance criteria**
0 to 1/2 AC cycle	95%	Nominal AC voltage	50/60Hz	No loss of function or performance
>1 AC cycles	>30%	Nominal AC voltage	50/60Hz	Loss of function acceptable, self-recoverable

AC Line Sag Test Condition

PSU	PSU Max. Load
2000W	70%

Table 12 – AC Line SURGE transient performance.

AC Line Surge				
Duration	**Surge**	**Operating ac voltage**	**Line frequency**	**Performance criteria**
Continuous	10%	Nominal AC voltage	50/60Hz	No loss of function or performance
0 to 1/2 AC cycle	30%	mid-point of nominal AC voltage	50/60Hz	No loss of function or performance

3.1.9.6 AC line fast transient (EFT) specification

The power supply shall meet the EN61000-4-5 directive and any additional requirements in IEC1000-4-5:1995 and the level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.
- The surge-withstand test must not produce damage to the power supply.
- The supply must meet surge-withstand test conditions under maximum and minimum DC-output load conditions.

3.1.10 Power Recovery

The power supply shall recover automatically (auto recover) after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

3.1.11 Voltage Brown Out

The power supply shall comply with the limits defined in EN55024:1998 using the IEC 61000-4-11:1995 test standard and performance criteria C defined in Annex B of CISPR 24.

In addition the power supply shall meet the following requirements:

A continuous input voltage below the nominal input range shall not damage the power supply or cause overstress to any power supply component. The power supply must be able to return to normal power up state after a brownout (Sag) condition.

3.1.12 AC Line Leakage Current

The maximum leakage current to ground for each power supply shall be 1.75mA when tested at 264VAC/63Hz.

Note: When the touch current over 3.5mA in system application, such as N+1 configuration, system side could follow IEC60950 “Equipment with touch current exceeding 3.5mA” section to get safety approval.

3.2 DC output voltages

3.2.1 Grounding

The output ground of the pins of the power supply provides the output power return path. The ground output at the PCB card edge shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 100 mΩ (Test Conditions 40A for 120sec). This path may be used to carry DC-current.

3.2.2 Output rating

The following tables defines the minimum power and current ratings. The power supply must meet both static and dynamic voltage regulation requirements for all conditions.

Table 13 –Load Requirements

<table>
<tr><td rowspan="5">PSU</td><td colspan="4">12V</td><td rowspan="2">12VSB</td></tr>
<tr><td>90~140Vac</td><td>180~200Vac</td><td>200~220Vac</td><td>220~264Vac</td></tr>
<tr><td>81.8A</td><td>130.3A(Note)</td><td>147A</td><td>163.6A</td><td rowspan="3">3A</td></tr>
<tr><td>180~210Vdc</td><td>210~240Vdc</td><td colspan="2">240~310Vdc</td></tr>
<tr><td>130.3A(Note)</td><td>147A(Note)</td><td colspan="2">163.6A</td></tr>
</table>

Note : These specification can be used by customer.

For peak loads above the Pmax.app peak load level the PSU may assert the SMBAlert# signal to shorten the duration of the peak load to < 100μsec. For peak loads up to Pmax.app peak load level the PSU must not assert SMBAert# if the peak load duration is <10msec. If the peak load last longer than 10msec the PSU may assert SMBAlert# to throttle the load within 15msec. Table 15 below are PSU requirements for Pmax peak load conditons.

Table 13-1 Peak Power Capability

Output	Max. Continuous (A)	CLST Peak 20sec duration(A)	Pmax.app Peak 10msec duration(A)	Pmax Peak 100μsec duration(A)
+12V(2000W)	163.6	Rated + 6	Rated + 30	Rated + 45
+12V(1000W)	81.8	Rated + 6	Rated + 30	Rated + 45
+12VSB	3A	>4A	NA	NA

Table 13-2 Peak Load Protection Testing Conditions

Pmax Peak Load	Peak current	System capacitance	SMBAlert# timing	Peak load duration
Rated + 540W	Rated + 45A	6 x 1500μF	>100μsec	>100μsec

3.2.3 Auxiliary Output (Standby)

The 12Vsb output shall be present when an AC input greater than $V_{recover}$ is applied.

3.2.4 No load operation

The power supply shall meet all requirements except for the transient loading requirements when operated at no load on all outputs.

3.2.5 Voltage Regulation

The power supply shall meet the Voltage regulation under all operating conditions (AC line, transient loading, output loading). These limits include the peak-peak ripple/noise. The regulation of Table 15 shall be measured at the output connector of the power supply, subject to the dynamic loading conditions in paragraph 3.2.7.

Table 15 – Output Voltage regulation

Output	Minimum	Nominal	Maximum	Unit
+12V	11.6	12.2	12.8	Vdc
+12VSB	11.6	12.2	12.8	Vdc

3.2.6 Ripple and Noise Regulation

Ripple and Noise is defined in table 16. Ripple and Noise shall be measured over a Bandwidth of 10Hz to 20MHz at the power supply output connector. A high frequency 0.1uF capacitor and 10uF tantalum capacitor can be used to terminate each output at the measurement point.

The ripple and noise specification shall be met over all load ranges and AC line voltages with 1+1 power supplies in parallel operation.To help reduce switching ripple further, an additional 2200uF low ESR electrolytic capacitor may be placed in parallel.

Table 16– Ripple and Noise Regulation

Voltage	**Ripple/Noise pk-pk**	**Remark**
+12V	200mV	With 0.1uF & 10uF
+12VSB	200mV	With 0.1uF & 10uF
Signal	**Ripple/Noise pk-pk**	**Remark**
PG	400mV	
PS_ON	400mV	
SMB_ALERT	400mV	
SMART_ON	400mV	

3.2.7 Dynamic loading(N+1)

The output voltages shall remain within limits specified for the step loading and capacitive loading specified in the table below. The load transient repetition rate shall be tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%.

The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the Peak load conditions.

Table 17 – Transient Load Requirements(High Line)

	1+0		1+1		2+1		3+1	
Output	**12V**	**12Vsb**	**12V**	**12Vsb**	**12V**	**12Vsb**	**12V**	**12Vsb**
Dynamic start up load	16A	0A	16A	0A	22A	0A	28A	0A
Δ Step Load Size	97A	1A	97A	1A	224A	1A	337A	1A
Slew Rate	0.5A/μs	0.5A/μs	0.5A/μs	0.5A/μs	0.5A/μs	0.5A/μs	0.5A/μs	0.5A/μs
Test Capacitive Load	2200uF	10μF	2200uF	10μF	4400uF	20μF	6600μF	30μF

3.2.8 Capacitive load

The power supply shall operate within specifications over the capacitive loading ranges defined below in table 18.

Table 18 – Capacitive Loading Conditions

Output	Min	Max
+12V	2000μF	50000μF
+12VSB	10μF	3100μF

3.2.9 Common Mode Noise

The Common Mode noise on any output shall not exceed 350mV pk-pk over the frequency band of 10Hz to 20MHz.
The measurement shall be made across a 100Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure).
The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

3.2.10 Close loop stability

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of: 45 degrees phase margin and -10dB-gain margin is required.
Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

3.2.11 Residual Voltage Immunity in Standby mode

The power supply should be immune to any residual voltage placed on its outputs (typically a leakage voltage through the system from standby output) up to 500mV. There shall be no additional heat generated nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on/off.

The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied.

3.2.12 Soft starting

The power supply shall contain control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load condition.

3.2.13 Hot Swap Requirements

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply shall use a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

3.2.14 Load sharing control

The +12 V output shall have active load sharing. When operating at minimum current share threshold, the output current of any 1+1 power supplies shall be within (+/-10%). For example, if power supply #1 is operating average current at 100A, then all other power supplies within the system shall be operating between 90A to 110A (+/- 10% of 100A).All current sharing functions shall be implemented internal to the power supply by making use of the SBus signal. The power distribution board(PDB), must connect the SBus signals between the power supplies together. The power supply shall be able to share with up to 1+1 supply in parallel. The failure of a power supply shall not affect the load sharing or output voltages of the other supplies still operating. The power supplies must be able to load share with 100mV of drop between different power supply's output. If the load sharing is disabled by shorting the load share bus to ground, the power supply shall continue to operate within regulation limits for loads less than or equal to the rating of one power supply.

Table 19 - Load share bus output characteristics

Item	Description	Min	Nominal	Max	Units
V_{share}; I_{out}=Max.	Voltage of load share bus at specified max output current		8		V
$\triangle V_{share}/\triangle I_{out}$	Slope of load share bus voltage with changing load		$8/I_{outmax}$		V/A

3.2.15 Parallel mode redundancy

The +12V output will have active load sharing. The output will share minimum current share threshold. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to load share in parallel and operate in a hot-swap / redundant 3+1 configurations. The 12Vsb output is not required to actively share current between power supplies (passive sharing). The 12Vsb output of the power supplies are connected together in the system so that a failure or hot swap of a redundant power supply does not cause these outputs to go out of regulation in the system. When the PSU turn on the output power can't over 2000W (N+1) before PWOK signal build. For other condition terms defined below in table 19-1.

For power extension and for redundancy, 3+1 power supplies can be connected in parallel to reach the necessary output power and/or to fulfill redundancy, phase redundancy and dual feed requirements. Refer to the below table for power calculation in parallel mode.

Table 19-1 - Load share bus output characteristics(High Line)

	1+1		2+1		3+1	
	12V	**12Vsb**	**12V**	**12Vsb**	**12V**	**12Vsb**
Maximum Load	161A	3A	322A	3A	483A	3A
Peak Load	322A	3A	483A	3A	644A	3A
Minimum current share threshold	16A	0A	48A	0A	60A	0A
Start up maximum current	161A	3A	161A	3A	161A	3A

3.3 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 10 to 70ms. All outputs must rise monotonically. Table below shows the timing requirements for the power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied.

3.3.1 Output Voltage Timing

The timing of signals and outputs are specified in below Table 20 and illustrated in Figure 2.

Table 20 - Turn on/off timing

Turn on	Description	Min	Max	Units
$T_{vout\ rise}$	Output voltage rise time for 12V	5	70	ms
	Output voltage rise time for 12Vsb	1	25	ms
$T_{sb\_on\_delay}$	Delay from AC being applied to 12Vsb being within regulation		1500	ms
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltage being within regulation		3000	ms
T_{vout_holdup}	Time all main output 12V voltages stay within regulation after loss of AC at 70% of max load.	11		ms
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK at 70% of max load.	10		ms
$T_{pson\_off\_delay}$	Delay from PSON# de-asserted to power supply turning off at 10%~100% of max load.		5	ms
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits	5	400	ms
T_{pson_pwok}	Delay from PSON# deactivate to PWOK being de-asserted.		5	ms
T_{pwok_on}	Delay from output voltage(12V) within regulation limits to PWOK asserted at turn on	100	500	ms
T_{pwok_off}	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1		ms
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal	100		ms
T_{sb_vout}	Delay from 12Vsb being in regulation to main output being in regulation at AC turn on.	50	1000	ms
T_{12Vsb_holdup}	Time the 12Vsb output voltage stays within regulation after loss of AC	70		ms

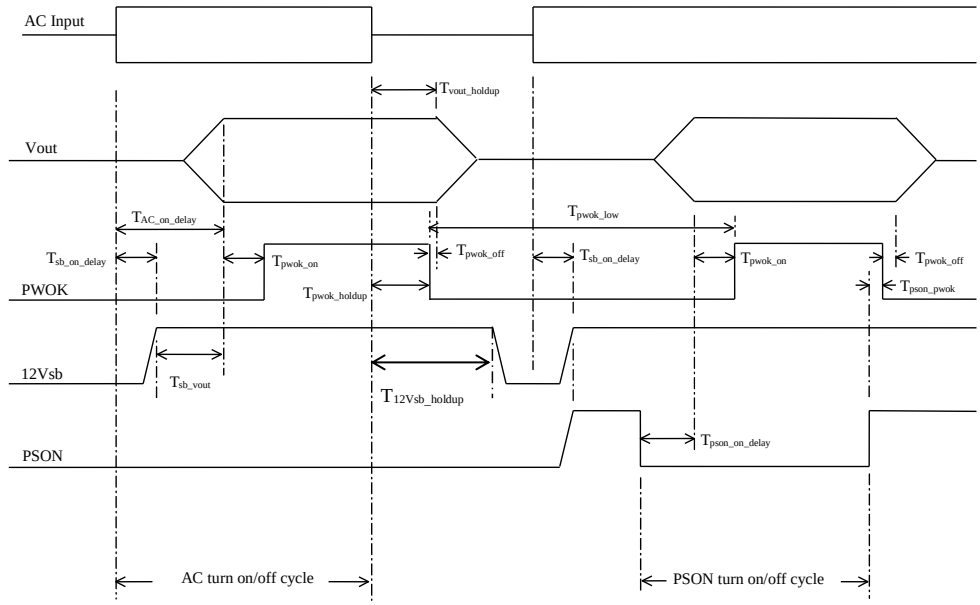


Figure 2 – Turn On/Off Timing (Power Supply Signals)

3.3.2 Overshoot

Any output overshoot at turn on shall be less than 10% of the nominal output value.

3.3.3 Undershoot

Any output shall not undershoot at turn on or off cycle under any circumstances.

3.4 Control and Indicator functions

The following section define the input and output signals from the power supply.

Signals that can be defined as low true use the following convention:

Signal# = low true.

3.4.1 PSON# Input Signal (Power supply enable)

The PSON# signal is required to remotely turn on/off the main output of the power supply.

PSON# is and active low signal that turns on the main output power rail. When this signal is not pulled low by the system or left open, the outputs (except the Standby output) turn off. PSON# is pulled to a standby voltage by a pull-up resistor internal to the power supply. See Table 21.

Table 21 – PS ON# signal characteristics

Signal Type	**Accepts an open collector/drain input from the system. Pull-up to +3.3V located in the power supply**.	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	3.46V
Source current, V_{pson} = low		4mA

3.4.2 Power OK (PG or PWOK) Output Signal

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that all outputs are within regulation limits. When any output voltage falls below regulation limits, a internal failure or when AC power has been removed for a time sufficiently long, so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit. See Table 22.

Table 22 – PWOK signal characteristics

Signal Type	**Open collector/drain output from power supply. Pull-up to +3.3V located in power supply.**	
PWOK=High	Power Good	
PWOK=Low	Power Not Good	
	MIN	MAX
Logic level low voltage, I_{sink}=4mA	0V	0.4V
Logic level high voltage, I_{source} = 200μA	2.4V	3.46V
Sink current, PWOK=low		400uA
Source current, PWOK=high		2mA

3.4.3 SMBAlert# Output Signal Pin

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, over-current warning, input under-voltage. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits. This signal is to be asserted in

parallel with LED turning solid amber or blinking amber/green. See Table 23.

The SMBAlert# signal shall be cleared and re-armed by the following methods.

- Clearing STATUS bits causing the asserted SMBAlert# signal.
- Power cycling with PSON or with input power
- Masking the event with SMBALERT_MASK
- The power supply reached a recover threshold to reset the STATUS_WARNING_bits to '0' when only STATUS_FAULT_bits is '0'.

Table 23 – SMBAlert# signal characteristics

Signal Type	**Open collector/drain output from power supply. Pull-up to +3.3V located in power supply.**	
Alert#=High	Power OK	
Alert#=Low	Power Alert to system	
	MIN	MAX
Logic level low voltage, I_{sink}=4mA	0V	0.4V
Logic level high voltage, I_{source} = 50μA	2.4V	3.46V
Sink current, Alert#=low		4mA
Source current, Alert#=high		50uA

Table 24 –Power Supply SMBAlert# Software

State	**SMBAlert# Going Low Description**		**SMBAlert# Recovery Method**
Over Current	Table 29		SMBAlert# shall be latch when the output current is back within the normal operating range.
Under Voltage	Input voltage	Input voltage dropping to 0Vac.	SMBAlert# shall be recovered when the input voltage is back within the normal operating range.
		AC input is below 75Vac (75-85Vac delay 20 seconds power off). HVDC input is below 165V.	
Over Temperature	$T_{Heatsink\_pri}$ over 105±2°C、T_{in_env} over 70±2°C		SMBAlert# shall be latch when the temperature is back to normal. It needs power cycling with AC power, PSON, or sending the PMBus CLEAR command.

Note1: When Vin is 75~85Vac, 0 ~ 5 seconds 0x7C (Status Input) will display a warn,6 seconds ~ 20seconds 0x7C (Status Input) will display warn & Fault, >20seconds the power will shut down.

Note2: MCU readings have a +/-2% tolerance for actual application.

3.4.4 A0

PSU Module Address Line 0. This signal line is provided for determining the address for the specific PSU FRU and SMBus address. The pull-up resister should be located in the system and the pull-up voltage should be limited to 3.3V. The address line should be pull low with equal to or less than 100ohm in the motherboard design.

Table 25 – A0 signal characteristics

Signal Type	**Pull-up to +3.3V located in power supply.**	
	MIN	MAX
Logic level low voltage, I_{sink}=4mA	0V	0.66V
Logic level high voltage, I_{source} = 50μA	2.64V	3.46V

3.4.5 A1

PSU Module Address Line 1. This signal line is provided for determining the address for the specific PSU FRU and SMBus address. The address line should be pull low with equal to or less than 100ohm in the motherboard design.

Table 26 – A1 signal characteristics

Signal Type	**Pull-up to +3.3V located in power supply..**	
	MIN	MAX
Logic level low voltage, I_{sink}=4mA	0V	0.66V
Logic level high voltage, I_{source} = 50μA	2.64V	3.46V

3.4.6 Present

This signal is connected to the power supply's output ground.

3.4.7 SDA and SCL

One pin is the serial clock (SCL), and the other pin is used for serial data (SDA). A 10KΩpull-up resistor pulled to internal +3.3V in the PSU.

4. Protection circuits

Protection circuits inside the power supply shall cause only the main output to shutdown (latch off). If the power supply latches off due to a protection circuit assert, an Input Power cycle OFF for 15sec or a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

Specific protection circuits shall not latch, but auto recover when the latching reason had been cleared. This protection circuits will be written in cursive writing and will have a Auto Recover in the chapter name.

The auxiliary output shall not affected by any protection circuit, unless the auxiliary output itself is affected.

4.1 Over Voltage Protection(OVP)

The power supply over voltage protection shall be locally sensed. The power supply shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels defined in Table 26 when measured at the power connectors of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power connector. +12VSB will be auto-recovered after removing OVP limit.

Table 27 - Over Voltage Protection

Output Voltage	MIN (V)	MAX (V)
+12V	13.3	14.5
+12VSB	13.3	14.5

4.2 Over Current Warning, Over Current & Over Power Protection (OCW, OCP & OPP)

The power supply shall have over current protection (OCP), over current warning (OCW), and over power protection (OPP) limits as defined in Table 28 below. These are defined to protect the PSU and to allow peak currents to power the system without the PSU shutting down. Fast OCW and Slow OCW levels are defined to assert SMBAlert# to allow the system to throttle power to protect the PSU; but also to allow peak current to the system without throttling the system.The power supply shall and shall be auto recover after the OCP/SCP had been removed.+12VSB will be auto-recovered after removing OCP limit.

Table 28 – Over Current Protection

Spec	Description	MIN	MAX	MIN	MAX
OPP / Fast OCP 1	Over power protection (asserted SMBAlert# signal & voltage foldback then hiccup mode)	Rating +45A	--	100μsec	--
Slow OCP	Slow over current protection (shutdown and hiccup mode)	Rating + 10A	Rating + 14A	20msec	100msec
Fast OCW 2	Fast over current warning (asserted SMBAlert# signal)	Rating + 30A	--	10msec	15msec
Slow OCW 3	Slow over current warning (asserted SMBAlert# signal)	Rating + 6A	Rating + 10A	15msec	20msec
OCPstby	Stby over current protection (shutdown, hiccup mode)	4.0A	--	1msec	100msec

Note: 1.MCU readings have a +/-2% tolerance for actual application.

2.Input voltage 90-120V, rating current is 81.8A

4.3 Over Temperature Protection (OTP)

The power supply shall have minimum of three thermal sensors to measure the inside environmental (T_{in_env}) and primary critical component ($T_{Heatsink\_pri}$). The thermal sensors shall be part of a protection circuit to protected against over temperature conditions caused by loss of Table 29 cooling or excessive ambient temperature. In an critical Over temperature condition, specified in below table, the PSU shall be shutdown with the exception of the auxiliary output.
The power supply shall alert the system of the OTP condition via SMBAlert# and fail LED indicator. The power supply will auto recover from this condition, when the temperature is dropping within specification again. If the OTP is caused due to a defective fan, the power supply shall latch off and not auto recover.

Table 29 – Over Temperature Protection

Condition	Warning in °C	Critical in°C	Timing for SMBAlert#/LED
T_{in_env}	62±2°C	66±2°C	1msec
$T_{Heatsink\_pri}$	--	125±2°C	1msec

Note：1. “ -- ” is Not supported

4.4 Fan Failure Protection

The power supply shall have a circuit internal to monitor the power supply internal fan. The fan failure protection shall monitor the fan speed and should assert fail LED signal in case the fan Rotation Per Minute (RPM) drop lower threshold or set PWM Δ as defined in below table.

The fan failure state shall shut down and latch off the main outputs, and shall be cleared by toggling the PSON# signal or by an AC input recycle.

Table 30 – Fan Failure Protection

Condition	FAN RPM	Timing for SMBAlert#/LED
Fault	1000	1000msec
Warning	1500	1500msec

5. Power Supply Management

5.1 Hardware Layer

The serial bus communication devices for Power Supply Management Controller (PSMC) and Field Replacement Unit (FRU) in the power supply shall be compatible with both SMBus 2.0 “high power” and I^2C Vdd based power and drive specification.

This bus shall operate at 3.3V but be tolerant to 5V pull-ups.

Two pins are allocated on the power supply. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Both pins are bi-directional and are used to form a serial bus. The device(s) in the power supply shall be located at an address(s) determined by addressing pins A0 and A1 on the power supply module. The circuits inside the power

supply shall derive their 3.3V power from the 12Vsb bus through a buffer. Device(s) shall be powered from the system side of the 12Vsb oring device. The pull-up resistors shall be on SCL or SDA inside the power supply.

5.2 Power Supply Management Controller (PSMC)

The PSMC device in the power supply shall derive its power of the 12Vsb output on the system side of the oring device and shall be grounded to return. It shall be compatible with SMBus specification 2.0 and PMBus™ Power System Management Protocol Specification Part I and Part II in Revision 2.0 or later

It shall be located at the address set by the A0 and A1 pins.

Refer to the specification posted on www.ssiforum.org and www.pmbus.org website for details on the power supply monitoring interface requirements and refer to followed section of supported features. The below table reflect the power module addresses complying with the position in the housing.

Table 31 – PSMC Addressing

PDB position and PSMC address	PM1 B0h/B1h	PM2 B2h/B3h
Pin A1/A0	0/0	0/1

5.2.1 Related Documents

- PMBus™ Power System Management Protocol Specification Part I – General Requirements, Transport And Electrical Interface ; Revision 1.2
- PMBus™ Power System Management Protocol Specification Part II – Command Language; Revision 2.0
- System Management Bus (SMBUS) Specification 2.0

5.2.2 Data Speed

The PSMC device in the power supply shall operate at the full 100kbps (100kHz) SMBus speed and avoid using clock stretching that can slow down the bus. For example, the power supply is allowed to clock stretch while parsing a command or servicing multiple interrupts or NACK.

Unsupported commands may respond with a NACK but must always set the communication error status bit in STATUS_CML.

5.2.3 Bus Errors

The PSMC shall support SMBus clock-low timeout ($T_{timeout}$). This capability requires the PSMC to abort any transaction and drop off the bus if it detects the clock being held low for >25ms, and be able to respond to new transactions within 10ms later. The total reset time from detection of the condition till restarted, ready to receive commands condition shall not exceed 35ms.

The device must recognize SMBus START and STOP conditions on ANY clock interval. The PSMC must not hang due

to ‘runt clocks’, ‘runt data’, or other out-of-spec bus timing. This is defined as signals, logic-level glitches, setup. Or hold times that are shorter than the minimums specified by the SMBus specifications. The PSMC is not required to operate normally, but must return to normal operation once ‘in spec’ clock and data timing is again received. Note if the PSMC ‘misses’ a clock from the master due to noise or other bus errors, the device must continue to accept ‘in spec’ clocks and NACK. The PSMC is supposed to re-synch with the master on the next START or STOP condition.

5.2.4 Write byte/word

The first byte of a Write Byte/Word access is the command code. The next one or two bytes, respectively, are the data to be written. In this example the master asserts the slave device address followed by the write bit. The device acknowledges and the master delivers the command code. The slave again acknowledges before the master sends the data byte or word (low byte first). The slave acknowledges each byte, and the entire transaction is finished with a STOP condition.

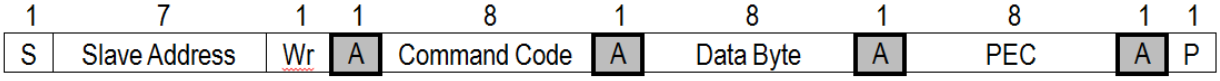


Figure 3 –Write byte protocol with PEC

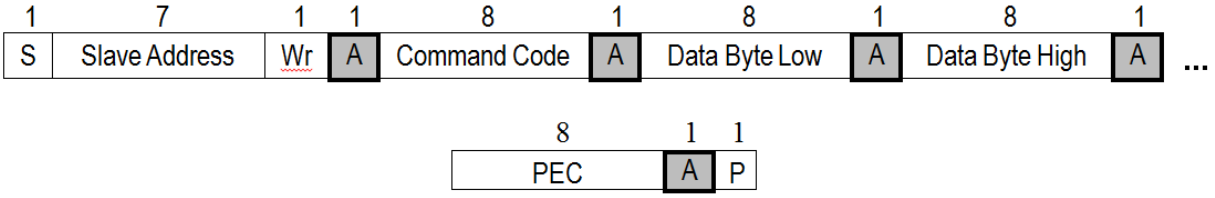


Figure 4 –Write Word Protocol with PEC

5.2.5 Read byte/word

Reading data is slightly more complicated than writing data. First the host must write a command to the slave device. Then it must follow that command with a repeated START condition to denote a read from that device’s address. The slave then returns one or two bytes of data.

Note that there is no STOP condition before the repeated START condition, and that a NACK signifies the end of the read transfer.

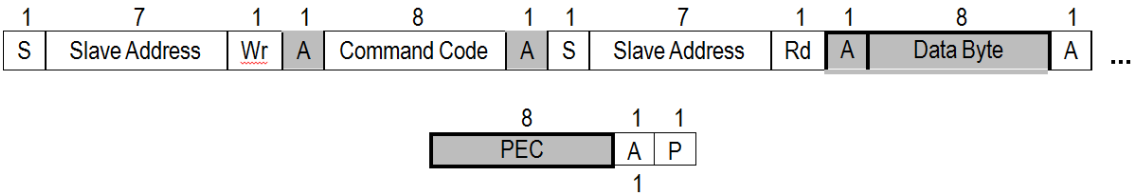


Figure 5 –Read byte protocol with PEC

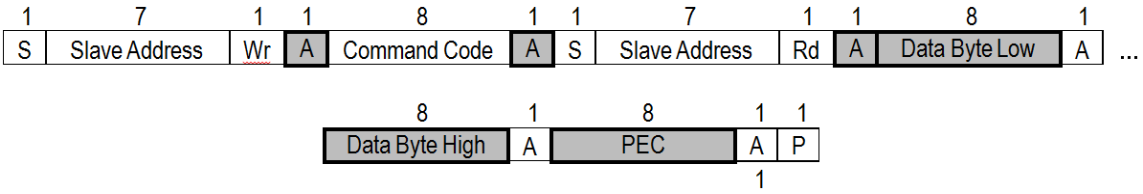


Figure 6–Read word protocol with PEC

5.2.6 Block write/read

The Block Write begins with a slave address and a write condition. After the command code the host issues a byte count which describes how many more bytes will follow in the message. If a slave has 20 bytes to send, the byte count field will have the value 20 (14h), followed by the 20 bytes of data. The byte count does not include the PEC byte. The byte count may not be 0. A Block Read or Write is allowed to transfer a maximum of 32 data bytes.

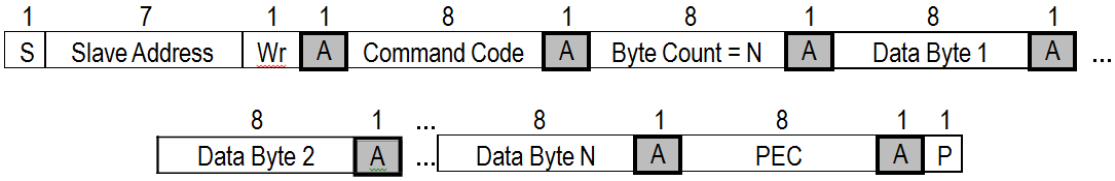


Figure 7 –Block Write with PEC

A Block Read differs from a block write in that the repeated START condition exists to satisfy the requirement for a change in the transfer direction. A NACK immediately preceding the STOP condition signifies the end of the read transfer.

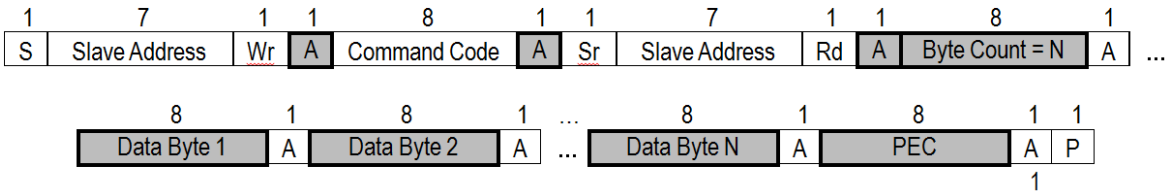


Figure 8 –Block Read with PEC

5.2.7 Sensor Accuracy

The sensor of the PSMC shall meet below accuracy requirements for sensor readings. The accuracy shall be meet at the specified environmental condition and the full range of rated input voltage. the output sensor accuracy only consider 12V output.

˙READ_VIN
˙READ_IIN
˙READ_VOUT
˙READ_IOUT
˙READ_POUT
˙READ_PIN
˙READ_EOUT

˙READ_EIN

Table 32 – Sensor Accuracy

Sensor	5% - 20% <load	20% - 40% load	40% - 100% load
Vin	±5%	±2%	±2%
Iin	±10% or ±0.08A	±3%	±2%
Pin	±5% or ±5W	±3%	±2%
Vout	±5%	±2%	±2%
Iout	± 1A	±3%	±2%
Pout	2%	±2%	±2%
Ein	±5% or ±5W	±3%	±2%
Eout	±2%	±2%	±2%

5.2.8 PSMC Sensors

Sensors shall be available to the PSMC for monitoring purpose.

All Sensors shall continue to provide real time data as long as the PSMC device is powered.

This means in standby and operation mode, while in standby the main output(s) of the power supply shall read zero Amps and Volts.

Table 33 – PSMC Sensor list

Sensor	Description
V_{input}	Input Voltage
I_{input}	Input Current
P_{input}	Input Power
V_{output_main}	Output Voltage main output
I_{output_main}	Output Current main output
P_{output_main}	Output Power main output
V_{output_aux}	Output Voltage auxiliary output
I_{output_aux}	Output Current auxiliary output
P_{output_aux}	Output Power auxiliary output
T_{comp}	Component Temperature
T_{env}	Environmental Temperature
RPM_{Fan}	Fan Speed reading
PDB_{fail}	PDB fail protection

5.3 Power Supply Field Replacement Unit (FRU)

The power supply shall support electronic access of FRU information over an I^2C bus. Four pins at the power supply connector are allocated for this. They are named SCL, SDA, A1, A0. SCL is serial clock. SDA is serial data. These two bidirectional signals from the basic communication lines over the I^2C bus. A0 and A1 are input address lines to the power supply. The backplane defines the state of these lines such that the address to the power supply is unique within the system. The resulting I^2C address shall be per table below. The Write protection pin is to ensure that data will not accidentally overwritten.

The device used for this shall be powered from a 3.3V bias voltage derived from the +12 Vsb output . No pull-up resistors shall be on SCL or SDA inside the power supply.

Table 34 - FRU Signals

	MCU Address		System addressing	
	PMBus	IPMI FRU	A1	A0
PSU - 1	B0	A0	0	0
PSU - 2	B2	A2	0	1
PSU - 3	B4	A4	1	0
PSU - 4	B6	A6	1	1

5.3.1 FRU Data

The FRU Data format shall be compliant with the IPMI ver. 1.0 (per rev. 1.1 from Sep.25th , 1999) specification. The current version of these specification is available at http://developer.intel.com/design/servers/ipmi/specs.htm.

5.3.2 FRU Device protocol

The FRU device will implement the same protocols as the commonly used memory device, including Byte Read, Sequential Read, Byte Write, and Page Read protocols.

5.3.3 FRU Data Format

The information to be contained in the FRU device is shown in the following table.

Table 35 - EEPROM Addressing

Item	Address	Byte Value (hex)	Description	Area
0	00H	01	Common Header	Format Version Number
1	01H	00	Internal Use Area	
2	02H	00	Chassis Info Area	
3	03H	00	Board Info Area	
4	04H	01	Product Info Area	
5	05H	0C	Multi Record Info Area	
6	06H	00	PAD Area	
7	07H	F2	Common Header Checksum (Total Of Bytes)	
8	08H	01	Product Area Format Version	Product Information Area
9	09H	0B	Product Area Length	
10	0AH	19	Language Code	
11	0BH	C9	**Manufacturer Name** type/length byte	
12	0CH	46	Manufacturer Name bytes	F
13	0DH	53	Manufacturer Name bytes	S
14	0EH	50	Manufacturer Name bytes	P
15	0FH	20	Manufacturer Name bytes	
16	10H	47	Manufacturer Name bytes	G
17	11H	52	Manufacturer Name bytes	R
18	12H	4F	Manufacturer Name bytes	O
19	13H	55	Manufacturer Name bytes	U
20	14H	50	Manufacturer Name bytes	P
21	15H	CC	**Product Name** type/length byte	
22	16H	46	Product Name bytes	F
23	17H	53	Product Name bytes	S
24	18H	50	Product Name bytes	P

25	19H	31	Product Name bytes	2
26	1AH	36	Product Name bytes	0
27	1BH	30	Product Name bytes	0
28	1CH	30	Product Name bytes	0
29	1DH	2D	Product Name bytes	-
30	1EH	32	Product Name bytes	2
31	1FH	30	Product Name bytes	0
32	20H	46	Product Name bytes	F
33	21H	4D	Product Name bytes	M
34	22H	CA	**Product Part/Model Number** type/length byte	
35	23H	39	Product Part Number bytes	**Need be consistent with SPEC label**
36	24H	50	Product Part Number bytes	**Need be consistent with SPEC label**
37	25H	41	Product Part Number bytes	**Need be consistent with SPEC label**
38	26H	31	Product Part Number bytes	**Need be consistent with SPEC label**
39	27H	36	Product Part Number bytes	**Need be consistent with SPEC label**
40	28H	41	Product Part Number bytes	**Need be consistent with SPEC label**
41	29H	30	Product Part Number bytes	**Need be consistent with SPEC label**
42	2AH	31	Product Part Number bytes	**Need be consistent with SPEC label**
43	2BH	30	Product Part Number bytes	**Need be consistent with SPEC label**
44	2CH	30	Product Part Number bytes	**Need be consistent with SPEC label**
45	2DH	C2	**Product Version** type/length byte	
46	2EH	31	Product Version	**Need be consistent with BOM**
47	2FH	30	Product Version	**Need be consistent with BOM**
48	30H	CC	**Product Serial Number** type/length byte	
49	31H	20	Product Serial Number bytes	**Need be consistent with SPEC label**
50	32H	53	Product Serial Number bytes	**Need be consistent with SPEC label**
51	33H	31	Product Serial Number bytes	**Need be consistent with SPEC label**
52	34H	32	Product Serial Number bytes	**Need be consistent with SPEC label**
53	35H	33	Product Serial Number bytes	**Need be consistent with SPEC label**
54	36H	34	Product Serial Number bytes	**Need be consistent with SPEC label**
55	37H	35	Product Serial Number bytes	**Need be consistent with SPEC label**
56	38H	36	Product Serial Number bytes	**Need be consistent with SPEC label**
57	39H	37	Product Serial Number bytes	**Need be consistent with SPEC label**
58	3AH	38	Product Serial Number bytes	**Need be consistent with SPEC label**
59	3BH	39	Product Serial Number bytes	**Need be consistent with SPEC label**
60	3CH	30	Product Serial Number bytes	**Need be consistent with SPEC label**
61	3DH	CA	**Asset Tag** type/length byte	**Production Date**
62	3EH	32	Asset Tag	Year
63	3FH	30	Asset Tag	Year
64	40H	31	Asset Tag	Year
65	41H	36	Asset Tag	Year
66	42H	2F	Asset Tag	/
67	43H	30	Asset Tag	Month
68	44H	34	Asset Tag	Month
69	45H	2F	Asset Tag	/
70	46H	31	Asset Tag	Day
71	47H	31	Asset Tag	Day
72	48H	D0	**FRU File ID** type/length byte	
73	49H	39	FRU File ID bytes.	**Need be consistent with SPEC label**

74	4AH	4D	FRU File ID bytes.	**Need be consistent with SPEC label**
75	4BH	2E	FRU File ID bytes.	**Need be consistent with SPEC label**
76	4CH	53	FRU File ID bytes.	**Need be consistent with SPEC label**
77	4DH	41	FRU File ID bytes.	**Need be consistent with SPEC label**
78	4EH	30	FRU File ID bytes.	**Need be consistent with SPEC label**
79	4FH	35	FRU File ID bytes.	**Need be consistent with SPEC label**
80	50H	2E	FRU File ID bytes.	**Need be consistent with SPEC label**
81	51H	30	FRU File ID bytes.	**Need be consistent with SPEC label**
82	52H	30	FRU File ID bytes.	**Need be consistent with SPEC label**
83	53H	30	FRU File ID bytes.	**Need be consistent with SPEC label**
84	54H	46	FRU File ID bytes.	**Need be consistent with SPEC label**
85	55H	2E	FRU File ID bytes.	**Need be consistent with SPEC label**
86	56H	30	FRU File ID bytes.	**Need be consistent with SPEC label**
87	57H	30	FRU File ID bytes.	**Need be consistent with SPEC label**
88	58H	31	FRU File ID bytes.	**Need be consistent with SPEC label**
89	59H	C1	no more info fields	
90	5AH	00	PAD	
91	5BH	00	PAD	
92	5CH	00	PAD	
93	5DH	00	PAD	
94	5EH	00	PAD	
95	5FH	BA	Product Info Area Checksum (Sum Of Bytes)	
96	60H	00	**Record Type ID**	**Power Supply Information**
97	61H	02	End of List/Record Format Version	
98	62H	18	Record Length	
99	63H	34	Record Checksum (zero checksum)	
100	64H	B2	Header Checksum (zero checksum)	
101	65H	40	Overall Capacity in Watts (LSB)	2000W
102	66H	06	Overall Capacity in Watts (MSB)	2000W
103	67H	FF	Peak VA	
104	68H	FF	Peak VA	
105	69H	23	Inrush current	35A
106	6AH	05	Inrush interval in ms.	5ms
107	6BH	28	Low end Input voltage range 1 (10mV ,LSB)	90V
108	6CH	23	Low end Input voltage range 1 (10mV ,MSB)	90V
109	6DH	B0	High end Input voltage range 1 (10mV ,LSB)	140V
110	6EH	36	High end Input voltage range 1 (10mV ,MSB)	140V
111	6FH	50	Low end Input voltage range 2 (10mV ,LSB)	180V
112	70H	46	Low end Input voltage range 2 (10mV ,MSB)	180V
113	71H	20	High end Input voltage range 2 (10mV ,LSB)	264V
114	72H	67	High end Input voltage range 2 (10mV ,MSB)	264V
115	73H	2F	Low end Input frequency range	47Hz
116	74H	3F	High end Input frequency range	63Hz
117	75H	0A	A/C dropout tolerance in ms(70%Load)	10mS
118	76H	1B	Binary flags	
119	77H	88	Peak Wattage(LSB)	2513W
120	78H	F6	Peak Wattage(MSB) – Hold up time in seconds	15S
121	79H	00	Combined Wattage	7:4 – Voltage 1；3:0 – Voltage 2
122	7AH	00	Combined Wattage (LSB)	

123	7BH	00	Combined Wattage (MSB)	
124	7CH	0A	Predictive fail tachometer lower threshold (RPS)	
125	7DH	01	**Record Type ID**	**12V Output Record**
126	7EH	02	End of List/Record Format Version	
127	7FH	0D	Record Length	
128	80H	21	Record Checksum (zero checksum)	
129	81H	CF	Header Checksum (zero checksum)	
130	82H	01	Output Information	
131	83H	B0	Nominal voltage (10 mV) (LSB)	12.2V
132	84H	04	Nominal voltage (10 mV) (MSB)	12.2V
133	85H	74	Maximum negative voltage (10 mV) (LSB)	11.6V
134	86H	04	Maximum negative voltage (10 mV) (MSB)	11.6V
135	87H	EC	Maximum positive voltage (10 mV) (LSB)	12.8V
136	88H	04	Maximum positive voltage (10 mV) (MSB)	12.8V
137	89H	78	Ripple and Noise (1mV) (LSB)	200mV
138	8AH	00	Ripple and Noise (1mV) (MSB)	200mV
139	8BH	32	Minimum current draw (mA)	500mA
140	8CH	00	Minimum current draw (mA)	500mA
141	8DH	E6	Maximum current draw (mA)	164A
142	8EH	32	Maximum current draw (mA)	164A
143	8FH	01	**Record Type ID**	**12Vsb Output Record**
144	90H	82	End of List/Record Format Version	
145	91H	0D	Record Length	
146	92H	27	Record Checksum (zero checksum)	
147	93H	49	Header Checksum (zero checksum)	
148	94H	82	Output Information	
149	95H	B0	Nominal voltage (10 mV) (LSB)	12.2V
150	96H	04	Nominal voltage (10 mV) (MSB)	12.2V
151	97H	74	Maximum negative voltage (10 mV) (LSB)	11.6V
152	98H	04	Maximum negative voltage (10 mV) (MSB)	11.6V
153	99H	EC	Maximum positive voltage (10 mV) (LSB)	12.8V
154	9AH	04	Maximum positive voltage (10 mV) (MSB)	12.8V
155	9BH	78	Ripple and Noise (1mV) (LSB)	200mV
156	9CH	00	Ripple and Noise (1mV) (MSB)	200mV
157	9DH	00	Minimum current draw (mA)	
158	9EH	00	Minimum current draw (mA)	
159	9FH	B8	Maximum current draw (mA)	
160	A0H	0B	Maximum current draw (mA)	
161	A1H	FF		
162	A2H	FF		
164	A3H	FF		
164	A4H	FF		
165	A5H	FF		
166	A6H	FF		
167	A7H	FF		
168	A8H	FF		
169	A9H	FF		
170	AAH	FF		
171	ABH	FF		

172	ACH	FF		
173	ADH	FF		
174	AEH	FF		
175	AFH	FF		
176	B0H	FF		
177	B1H	FF		
178	B2H	FF		
179	B3H	FF		
180	B4H	FF		
181	B5H	FF		
182	B6H	FF		
183	B7H	FF		
184	B8H	FF		
185	B9H	FF		
186	BAH	FF		
187	BBH	FF		
188	BCH	FF		
189	BDH	FF		
190	BEH	FF		
191	BFH	FF		
192	C0H	FF		
193	C1H	FF		
194	C2H	FF		
195	C3H	FF		
196	C4H	FF		
197	C5H	FF		
198	C6H	FF		
199	C7H	FF		
200	C8H	FF		
201	C9H	FF		
202	CAH	FF		
203	CBH	FF		
204	CCH	FF		
205	CDH	FF		
206	CEH	FF		
207	CFH	FF		
208	D0H	FF		
209	D1H	FF		
210	D2H	FF		
211	D3H	FF		
212	D4H	FF		
213	D5H	FF		
214	D6H	FF		
215	D7H	FF		
216	D8H	FF		
217	D9H	FF		
218	DAH	FF		
219	DBH	FF		
220	DCH	FF		

221	DDH	FF		
222	DEH	FF		
223	DFH	FF		
224	E0H	FF		
225	E1H	FF		
226	E2H	FF		
227	E3H	FF		
228	E4H	FF		
229	E5H	FF		
230	E6H	FF		
231	E7H	FF		
232	E8H	FF		
233	E9H	FF		
234	EAH	FF		
235	EBH	FF		
236	ECH	FF		
237	EDH	FF		
238	EEH	FF		
239	EFH	FF		
240	F0H	FF		
241	F1H	FF		
242	F2H	FF		
243	F3H	FF		
244	F4H	FF		
245	F5H	FF		
246	F6H	FF		
247	F7H	FF		
248	F8H	FF		
249	F9H	FF		
250	FAH	FF		
251	FBH	FF		
252	FCH	FF		
253	FDH	FF		
254	FEH	FF		
255	FFH	FF		

5.4 In-System Firmware Upload

This specification defines the common architecture for in-system power supply firmware updates. It is required that the FW in the main microcontroller on the secondary side of the power supply must be able to be updated in the system using the In-System Firmware Update feature while in the ON state (i.e. with AC power present and PSON# asserted). It is desired that any other microcontroller in the power supply also be able to be updated with this same process (example: primary side microcontroller); however, this is not a requirement at this time.

5.4.1 FW Image Mapping

The power supply firmware image shall be made up of two parts; 1)Boot loader; 2) Main program. The system shall

contain a backup of the power supply image in its BMC whenever updating the FW to the power supply.

5.4.2 Summary of Commands & Capabilities supported in Boot Loader mode

When the power supply is in FW Upload mode the following commands shall be supported.

Table 36

Code	Command	SMBus Transaction Type
19h	CAPABILITY	Read Byte w/PEC
1Ah	QUERY (used with any command)	Block Write Block Read Process Call w/ PEC
98h	PMBUS_REVISION	Read Byte w/PEC
9Ah	MFR_MODEL	Block Read
D4h	MFR_HW_COMPATIBILITY	Read Word w/PEC
D5h	MFR_FWUPLOAD_CAPABILITY	Read Byte w/PEC
D6h	MFR_FWUPLOAD_MODE	Read/Write Byte w/PEC
D7h	MFR_FWUPLOAD	Bloack Write w/ PEC (size = block size from image header)
D8h	MFR_FWUPLOAD_STATUS	Read Word w/PEC
D9h	MFR_FW_REVISION	Block Read w/PEC (3 bytes)
Basic Function	Operating Capability	
Fan control	The fan be kept at the base speed.	

6. Smart On Function

6.1 PMBus command for Smart On

6.1.1 Hardware Connection

Before enabling Smart On function, make sure pin B22 (SMART ON) on output golden finger of each PSU is connected together. The PSU shall use this to read the values of lower than 0 ~ 0.6 voltage used to determine leave smart standby mode. See Table 37 signal characteristics.

Table 37 – Smart On signal characteristics

Signal Type	**Open collector/drain output from power supply. Pull-up to +3.3V located in power supply.**	
	MIN	MAX
Logic level low voltage, I_{sink}=4mA	0V	0.66V
Logic level high voltage	N/A	N/A

6.1.2 Configuring Smart On with SMART_ON_CONFIG (D0h)

The PMBus manufacturer specific command MFR_SPECIFIC_00 is used to configure the operating state of the power supply related to Smart On. We will call the command SMART_ON_CONFIG (D0h). Below is the definition of the values used with the Read-Write Byte SMBus protocol with PEC.

SMART_ON_CONFIG (D0h)				
Value	State	Description	Enable Threshold	Disable Threshold
00h	Standard Redundancy	Turns the power supply ON into standard redundant load sharing mode.	NA	NA
01h	Smart On Active	Defines this power supply to be the one that is always ON in a cold redundancy configuration.	NA	NA
02h	Smart Standby 1	Defines the power supply that is first to turn on in a cold redundant configuration as the load increases.	40% of max	0.9 x (40% of max x 1/2) =18%
03h	Smart Standby 2	Defines the power supply that is second to turn om in a cold redundant configuration as the load increases.	62% of max	0.9 x (62% of max x 2/3) =37.2%
04h	Smart Standby 3	Defines the power supply that is third to turn on in a cold redundant configuration as the load increases.	84% of max	0.9 x (84% of max x 3/4) =56.7%
05h	Always Standby	Defines this power supply to be always in cold redundant configuration no matter what the load condition.		

Note: MCU readings have a +/-2% tolerance for actual application.

The default state of power supply is in Standard Redundancy mode. Power supply need to be re-specified a state whenever initial power on or any power supply in the system is in fault situation.

The SMART_ON_CONFIG command will reset to 00h (Standard Redundancy) when any fault or over current happened. The faults include AC loss, over hot spot temperature, over ambient temperature, +12V short internally (under voltage), +12V over voltage, fan locked, D2D controller soft-start short.

6.1.3 Power Supply Turn On Function

Powering on and off of the cold standby power supplies is only controlled by each PSU sensing output load. Once a power supply turns on after crossing the enable threshold; it lowers its threshold to the disable threshold. The system defines the ‘position’ of each power supply in the Cold Redundant operation. It will do this each time the system is powered on, a power supply fails, or a power supply is added to the system.

The system is relied upon to tell each power supply where it resides in the Cold Redundancy scheme.

When load ramps up and crosses the threshold module wake up time must be <3ms

When load ramps down and crosses the threshold module go-to-sleep time must be <5ms

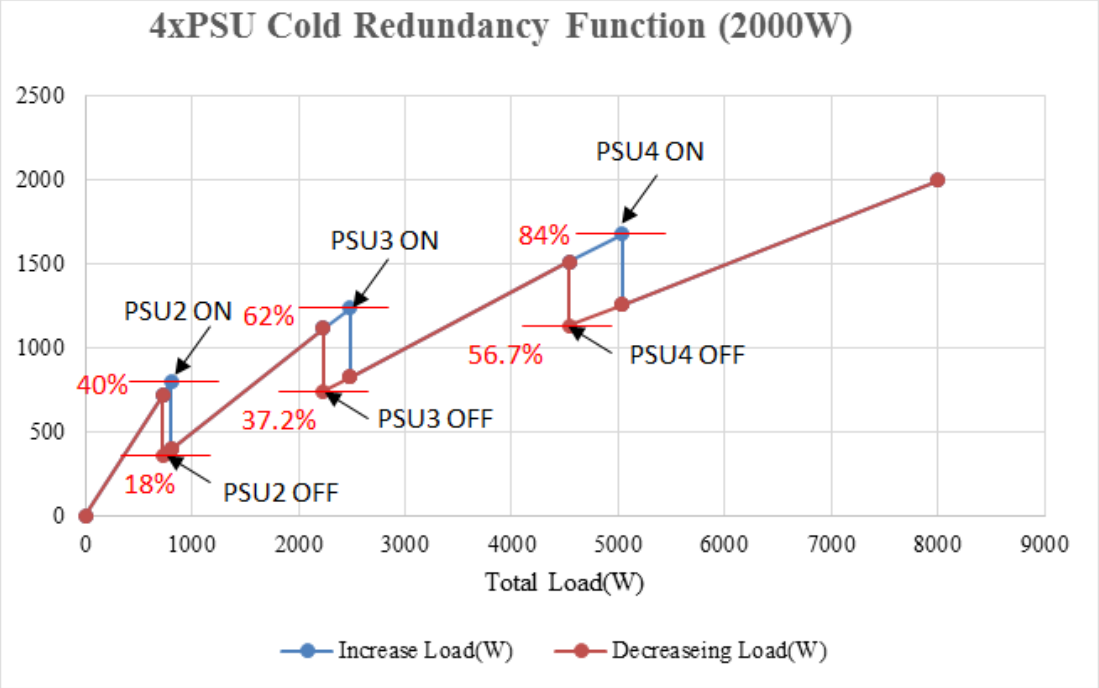


Figure 9 –4xPSU Cold Redundancy Function (2000W)

6.2 Smart Standby Power Supply Operating State

A power supply is put into Smart Standby whenever PSON# is asserted, and SMART_ON_CONFIG value is set to 02h. In the Smart Standby mode the power supply must:

1. Power ON when Smart_On bus is driven LOW

2. Keep PWOK asserted

3. No PMBus fault or warning conditions reported via STATUS commands

4. keep all fans rolling

5. LED is green blinking

6.2.1 Powering on Smart Standby supplies to maintain best efficiency

Power supplies in Smart Standby state shall monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position the system defines that power supply to be in the Smart Standby configuration; will slightly change the load share threshold that the power supply shall power on at.

6.2.2 Powering on Smart Standby supplies during a fault or over current condition

Some warnings happen or 12V output shutdown due to any fault. When an active power supply asserts, all parallel power supplies in Smart Standby mode shall power on immediately.

The trigger condition:

1. 12V OC warning/ fault happens

2. 12V OVP fault

3. 12V UVP

4. OTP warning/ fault

5. fan speed warning/ fault

6.AC loss

When an active power supply asserts, all parallel power supplies in Smart Standby mode shall power on immediately.

6.3 The Way to Enable Smart On Function

Here are the steps to put PSU into smart on mode. PSU which is assigned as smart on standby can operate in a power-off state and turn on main power if necessary.

The trigger levels above may have a +/-10% tolerance for actual application.

Step1: Make sure every PSU has AC power cord applied. Use write byte command to set command 0xD0 for each PSU to has it own role (must one PSU as active role).

The command format for Smart On function will be as following example.

B0 in smart_on_active (S B0 w D0 01 PEC P)

B2 in smart_on_standby (S B2 w D0 02 PEC P)

Step2: PSU will enter smart slave mode once the load is lower than the corresponding trigger point.

Step3: If SMART_ON signal falls to low, all PSU will turn on the main power and reset smart_config to 0x00 (standard redundancy). System needs to re-assign the roles for all PSU to enable smart on function again.

7. ENVIRONMENTAL

The power supply shall operate normally, and sustain no damage as a result of the environmental conditions listed in this chapter.

7.1 Temperature

Operating Ambient, normal mode (inlet Air): 0°C min/+55°C max at 5000m above sea level.

Operating Ambient, stand-by mode (inlet Air): -5°C min/+55°C max at 5000m above sea level.

Non-operating ambient: -40°C to +70°C (Maximum rate of change shall be 20°C/hr)

7.2 Humidity

Operating: 5%- 90% relative humidity (non-condensing)

Non-operating: 5%- 95% relative humidity (non-condensing)

Note: 95% relative humidity is achieved with a dry bulb temperature of 55°C and a wet bulb temperature of 54°C.

7.3 Altitude

A) Operation : sea level to 5000m

B) Non-Operation : sea level to 15,000m

Note: Defines the power derating when altitude above 900m.

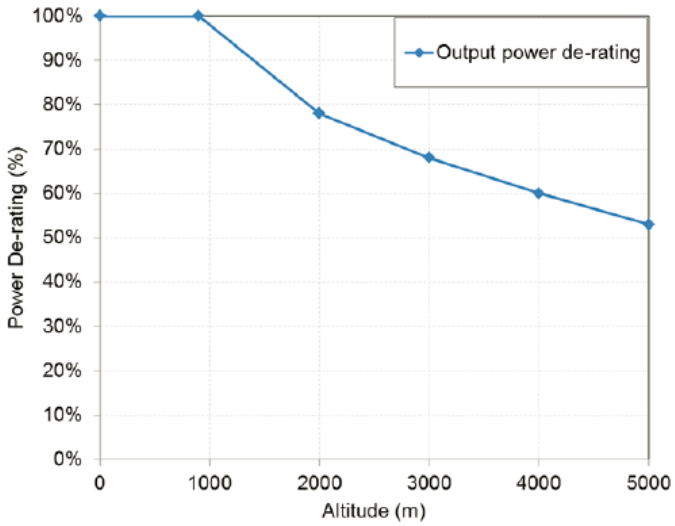


Figure 10 –power derating when altitude above 900m

7.4 Vibration

A) Operation : 0.01g²/Hz at 5 Hz sloping to 0.02g²/Hz at 20 Hz, and maintaining 0.02g²/Hz from 20 Hz to 500 Hz. The area under the PSD curve is 3.13gRMS. The duration shall be 20 minutes per axis for all three axes on all samples.

B) Non-Operation :

- **Sine sweep:** 5Hz to 500Hz @ 0.5gRMS at 0.5 octave/min; dwell 15min at each of 3 resonant points;

7.5 Mechanical Shock

A) Operation: 10G, 4.3 mSec, no malfunction
B) Non operating: 50G Trapezoidal Wave, Velocity change = 4.3m/sec. Three drops in each of six directions are applied to each of the samples.

7.6 Thermal shock (Shipping)

Non-operating: -40°C to +70°C, 50 cycles, 30°C/min. ≥ transition time ≥ 15°C/min., duration of exposure to temperature extremes for each half cycle shall be 30minutes.

7.7 Catastrophic Failure

The power supply shall be designed to fail without startling noise or excessive smoke.

7.8 EMI

The power supply shall comply with FCC part 15, CRISP 22 and EN55-22; Class A for both conducted and radiated emissions with a 3dB margin. Test shall be conducted using a shielded DC output cable to a shielded load. The load shall be adjusted to 100% load. Test will be performed at 230VAC @ 50Hz power.

The power supply shall comply with EN55024.

The power supply when installed in the system must meet the following all the immunity requirements when integrated into the end system.

7.9 Magnetic Leakage Fields

The PFC choke magnetic leakage field shall not cause any interference with a high resolution computer monitor placed next to or on top of the chassis.

7.10 Voltage Fluctuations and Flicker

The power supply shall meet the specified limits of EN61000-3-3, for voltage fluctuations and flicker for equipment ≤ 16 amps connected to low voltage distribution systems.

8. REGULATORY Requirements

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.) other than ITE application, may require further evaluation.

8.1 Product Safety Compliance

A) UL 62368-1/CSA 62368-1 Edition 2 (USA/Canada)
B) EN62368-1 Edition 2 (Europe)

C) IEC62368-1 Edition 2 (International)

D) CB Certificate & Report, IEC62368-1 Edition 2 (report to include all country national deviations)

E) CE – Low Voltage Directive 2006/95/EC (Europe)

F) GB4943-CBCA Certification (China)

8.2 Product EMC Compliance – Class A Compliance

The product is required to comply with Class A emission, as the system it is build into might be configured with the intend for commercial environment or home use. The Power supply is to have a minimum of 3dB margin to Class A Limits to support FSP's Standard margin requirements.

A) FCC / ICES-003 Emission (USA/Canada) Verification

B) CRISP 22 – Emission (International)

C) EN55032 – Emission (Europe)

D) EN55024 – Immunity (Europe)

- EN61000-4-2 Electrostatic Discharge
- EN61000-4-3 Radiated RFI Immunity
- EN61000-4-4 Electrical Fast Transients
- EN61000-4-5 Electrical Surge
- EN61000-4-6 RF Conducted
- EN61000-4-8 Power Frequency Magnetic Fields
- EN61000-4-11 Voltage Dips and Interruptions

E) EN61000-3-2 – Harmonics (Europe)

F) EN61000-3-3 – Voltage Flicker (Europe)

G) CE – EMC Directive 2004/108/EEC (Europe)

H) JEIDA (Japan)

I) AS/NZS CISPR 22 (Australia / New Zealand)

J) GB 9254 2008 (EMC) Certification (China)

K) GB 17625.1 – (Harmonics) CNCA Certification (China)

8.3 Maximum AC Leakage current to ground

1.75mA max for each power supply at 264Vac.

Note: When the touch current over 3.5mA in system application, such as N+1 configuration, system side could follow IEC60950 "Equipment with touch current exceeding 3.5mA" section to get safety approval.

8.3.1 Hi-pot

The power supply module in the system shall be test at 1800Vac, with a trigger limit of 30mA.

8.4 Electrostatic Discharge (ESD)

The power supply shall comply with the limits defined in EN 55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-2: Edition 1.2: 2001-04 test standard and performance criteria B (contact 8KV/air 15KV)defined in Annex B of CISPR 24.

8.5 Certifications / Registrations/ Declarations

A) UL Certification (US)
B) CB Certification & Report
C) TÜV Rheinland (Germany)
D) CE Declaration of Conformity (CENELEC Europe)
E) CCC / CNCA Certification (China)

8.6 Component Regulation Requirements

1. All Fans shall have the minimum certifications: UL and TÜV or VDE
2. All current limiting devices shall have UL and TÜV or VDE certifications and shall be suitable rated for the application where the device In its application complies with IEC62368.
3. All printed wiring boards shall be rated UL94V-0 and be sourced from a UL approved printing wiring board manufacturer.
4. All connectors shall be UL recognized and have a UL flame rating of UL94V-0
5. All wiring harnesses shall be sourced from a UL approved wiring harness manufacturer.
   SELV cable to be rated minimum 80V @ 120°C
6. Product safety label must be printed on UL approved label stock and printer ribbon.
   Alternatively labels can be purchased from a UL approved label manufacturer.
7. The product must be marked with the correct regulatory markings to support the certifications that are specified in this document.

8.6.1 Product Ecology Requirement

All materials, parts and subassemblies must not contain restricted materials as defined in directive 2002/95/EC, Restriction of Hazardous Substances (RoHS) 6/6.

All cords and cables shall contain <100ppm of cadmium.

All packing materials must be marked with applicable recycling logos for Europe (green dot) and Japan (Eco-marks), if sold as a retail product. All packing materials shall be recyclable.

9. Reliability and Service

9.1 Mean Time between Failures (MTBF)

The power supply shall have a minimum MTBF at continuous operation of 200,000 hours calculated at 100%, according to BELL CORE TR-322 at 25°C excluding the Fan MTBF, and at least 100,000 hours including the fan MTBF.

9.2 Serviceability

No troubleshooting by maintenance personnel is to be performed. Units shall be returned to FSP Power for any troubleshooting, unless agreed by both parties.

The power supply will lose warranty if opened other than FSP service personal or agreed by both parties.

9.3 Life Requirement

The power supply shall support 5 years calculated life for following conditions:

240VAC input

55°C inlet temperature

80% of Max.load

10. MISCELLANEOUS

10.1 Marking

The Power Supply shall carry labels defined in this section.

10.2 Outline Dimensions

The Power Supply module shall have the dimension 39/40mm x 73.5mm x185mm (HxWxL) without the card edge.

10.2.1 Power Supply Card Edge Dimension

The Power Supply Card Edge shall comply with below specification.

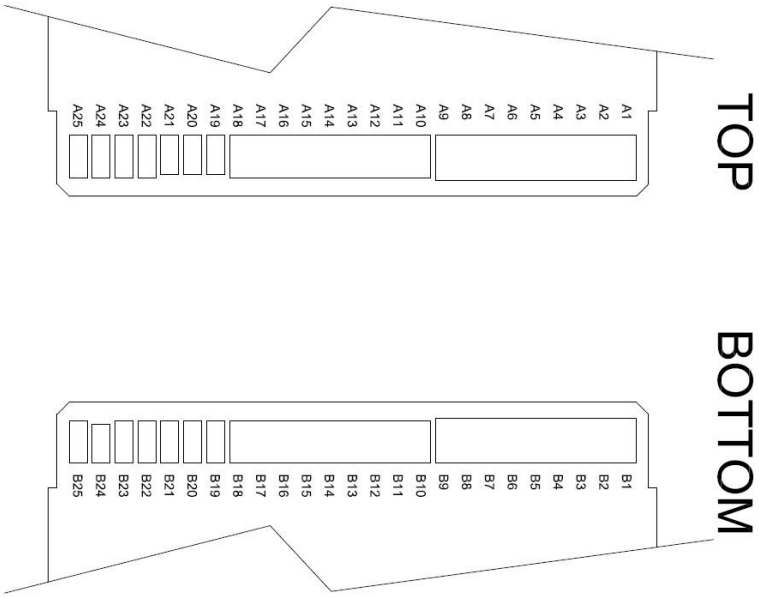


Figure 10 – Card Edge Dimension

Pin Name	Signal Name	Function
A1 ~ A9	GND	+12V return
B1 ~ B9	GND	+12V return
A10 ~ A18	Main Output	+12V
B10 ~ B18	Main Output	+12V
A19	SDA	I^2C Data signal
A20	SCL	I^2C Clock signal
A21	PSON	Power enable input
A22	SMB_Alert	SMB_Alert for failure notification
A23	Return Sense	+12V RTN Sense
A24	+12V Remote Sense	+12VS
A25	PWOK	Power OK output
B19	A0	I^2C address bit 0
B20	A1	I^2C address bit 1
B21	Standby_Output	+12VSB
B22	Smart ON	Smart ON
B23	SBus	+12V Main output Current share bus
B24	Present	GND
B25	Reserve	Reserve

10.3 Packing

The Power Supply should be packed according to the description in this chapter.

The Packing for the power supply should be recyclable and has no metal parts to hold the packing.

11. PSMC Interface

Following Chapter provide details information of the utilized PSMC Interface protocol utilized. The Interface protocol can be recognized by it's ID.

By Default the PMBus shall be utilized to achieve the best compatibility with current applications.

A customization of the PSMC Interface is possible and would accordingly reflected in a different FW ID and different specification compared to the PMBus ones.

11.1 PMBus Data Formats

The Linear Data Format is a two bytes value with:

An 11 bit, two's complement mantissa and

A 5 bit, two's complement exponent (scaling factor).

The format of the two data bytes is illustrated in Figure 11.

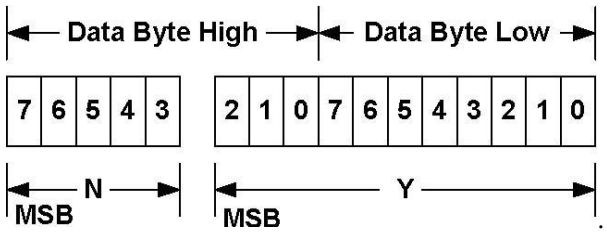


Figure 11. Linear Data Format Data Bytes

The relation between Y, N and the "real world" value is:

$X = Y \cdot 2^N$

Where, as described above:

X is the “real world” value being communicated

Y is an 11 bit, two’s complement integer; and

N is a 5 bit, two’s complement integer.

Devices that use the Linear format must accept and be able to process any value of N.

11.2 Power Sensors

The following PMBus commands shall be supported for the purpose of monitoring currents, voltages, and power. All sensors shall continue providing real time data as long as the PMBus device is powered. This means in standby mode the main output(s) of the power supply shall be zero amps and zero volts.

Table 38 – PMBus Command Summary supported

Command Code	Name	Type	Bytes	Value	Conditions
00h	PAGE	R/W	1		
01h	OPERATION	R/W	1		
02h	ON_OFF_CONFIG	R/W	1		
03h	CLEAR_FAULTS	Send Byte	0		
05h	PAGE_PLUS_WRITE	Block W			
06h	PAGE_PLUS_READ	BW-BR process call			
19h	CAPABILITY	R	1	90h	
1Ah	QUERY	BW-BR process call			
1Bh	SMBALERT_MASK	BW-BR process call	2		
20h	VOUT_MODE	R	1	17h	
30h	COEFFICIENTS	BW-BR process call	5		
3Ah	FAN_CONFIG_1_2	R/W	1	D0h	Fan1 is command in RPM
3Bh	FAN_COMMAND_1	R/W	2		
4Ah	IOUT_OC_WARN_LIMIT	R/W	2		High line / Low line
51h	OT_WARN_LIMIT	R/W	2	62℃	Warning for Ambient
78h	STATUS_BYTE	R	1		
79h	STATUS_WORD	R	2		
7Ah	STATUS_VOUT	R	1		
7Bh	STATUS_IOUT	R	1		

7Ch	STATUS_INPUT	R	1		
7Dh	STATUS_TEMPERATURE	R	1		
7Eh	STATUS_CML	R	1		
80h	INPUT_TYPE	R	1		
81h	STATUS_FANS_1_2	R	1		
86h	READ_EIN	Block R	6		
87h	READ_EOUT	Block R	6		
88h	READ_VIN	R	2		
89h	READ_IIN	R	2		
8Bh	READ_VOUT	R	2		
8Ch	READ_IOUT	R	2		
8Dh	READ_TEMPERATURE_1	R	2		Ambient
8Fh	READ_TEMPERATURE_3	R	2		Primary Hot spot
90h	READ_FAN_SPEED_1	R	2		In Fan RPM
96h	READ_POUT	R	2		
97h	READ_PIN	R	2		
98h	PMBUS_REVISION	R	1	22h	PMBus 1.2
99h	MFR_ID	Block R	9	FSP GROUP	
9Ah	MFR_MODEL	Block R	12	FSP2000-20FM	
9Bh	MFR_REVISION	Block R	2	10	
9Ch	MFR_LOCATION	Block R	5	CHINA	
9Dh	MFR_DATE	Block R	6	YYMMDD	
9Eh	MFR_SERIAL	Block R	12		
9Fh	APP_PROFILE_SUPPORT	R	1	05h	
A0h	MFR_VIN_MIN	R	2	90V / 180V	AC / DC
A1h	MFR_VIN_MAX	R	2	264V / 310V	AC / DC
A2h	MFR_IIN_MAX	R	2	12.6A / 14A	High line / Low line
A3h	MFR_PIN_MAX	R	2	2268W / 1260W	High line / Low line
A4h	MFR_VOUT_MIN	R	2	11.6V	
A5h	MFR_VOUT_MAX	R	2	12.8V	
A6h	MFR_IOUT_MAX	R	2	12V:164A / 83.5A 12VSB: 3A	High line / Low line
A7h	MFR_POUT_MAX	R	2	2000W / 1000W	High line / Low line
A8h	MFR_TAMBIENT_MAX	R	2	55℃	Max Operat Temp
A9h	MFR_TAMBIENT_MIN	R	2	0℃	Min Operat Temp
ABh	MFR_EFFICIENCY_HL	Block R	14	90%/94%/91%	At 20%/50%/100% load
C0h	MFR_MAX_TEMP_1	R	2	62℃	Warn for Ambient
C2h	MFR_MAX_TEMP_3	R	2		Warn for PFC
C3h	MFR_FAN_SPEED_MAX	R	2	30000 rpm	

C4h	MFR_FAN_SPEED_MIN	R	2	0 rpm	
D0h	SMART_ON_CONFIG	R/W	1		
D4h	MFR_HW_COMPATIBILITY	R	2		For FW boot loader
D5h	MFR_FWUPLOAD_CAPABILITY	R	1		For FW boot loader
D6h	MFR_FWUPLOAD_MODE	R/W	1		For FW boot loader
D7h	MFR_FWUPLOAD	Block W			For FW boot loader
D8h	MFR_FWUPLOAD_STATUS	R	2		For FW boot loader
D9h	MFR_FW_REVISION	Block R	3		For FW boot loader
DCh	MFR_BLACKBOX	Block R	237		
DDh	MFR_REAL_TIME_BLOCK_BOX	Block R/W	4		
DEh	MFR_SYSTEM_BLACK_BOX	Block R/W	40		
DFh	MFR_BLOCKBOX_CONFIG	R/W	1		
E0h	MFR_CLEAR_BLACKBOX	Send Byte	0		
E9h	MFR_FAN_DUTY	R	2		In Fan Duty
EAh	METER_FW_ID	Block R	16		9M.PA06.XXXX.XXX
EBh	METER_FW_DATE	Block R	8		
ECh	MFR_FW_ID	Block R	16		9M.SA05.XXXX.XXX
EDh	MFR_FW_DATE	Block R	8		
EEh	MFR_EEPROM_WRITE	Block W			
F4h	MFR_CAL_INPUT	BW-BR			
F5h	CALIBRATION OUTPUT CURRENT_1	R			
F6h	CALIBRATION OUTPUT CURRENT_2	R			
F7h	CALIBRATION OUTPUT CURRENT_3	W	1		
F8h	CALIBRATION OUTPUT VOLTAGE	W	2		

11.2.1 PAGE Command (00h)

Page member :

READ_IOUT

READ_VOUT

STATUS_IOUT

STATUS_VOUT

IOUT_OC_WARN_LIMIT

Page list :

PAGE	OUTPUT	Description
00h	12v1	Supported, Default for single 12v output
01h	12v2	--
02h	12v3	--
03h	12v4	--
04h	12v5	--
05h	12v6	--
06h-0fh	Reserved	--
10h	5v	--
11h	3.3v	--

12h-1fh	Reserved	--
20h	5vsb	--
21h	3.3vsb	--
22h	-12v	--
23h	12vsb	Supported.
24h-2fh	Reserved	--
30h	48v	--
31h	24v	--
32h-3fh	Reserved	--

Note: " -- " is Not supported

11.2.2 Operation Command (01h)

Operation Notice：

This function is only supported for module operation only without PDB.

If utilized while inserted in a PDB without function support, utilization of this function might cause Unexpected side effects.

Operation command Default Value is 0x00h.

Bits [7:6]	Bits [5:4]	Bits [3:2]	Bits [1:0]	Unit On Or Off	Margin State	Description	Supported
00	XX	XX	XX	Immediate Off (No Sequencing)	N/A	Immediate turn-off	Ok
01	XX	XX	XX	Soft Off (With Sequencing)	N/A	turn-off delay and fall time	--
10	00	XX	XX	On (turn-on)	Off	Immediate turn-on	Ok
10	01	01	XX	On	Margin Low (Ignore Fault)	Margin Low (Ignore Fault)	--
10	01	10	XX	On	Margin Low (Act On Fault)	Margin Low (Act On Fault)	--
10	10	01	XX	On	Margin High (Ignore Fault)	Margin High (Ignore Fault)	--
10	10	10	XX	On	Margin High (Act On Fault)	Margin High (Act On Fault)	--

Note: " -- " is Not supported

11.2.3 ON_OFF_CONFIG Command (02h)

Operation Notice：

This function is only supported for module operation only without PDB.

If utilized while inserted in a PDB without function support, utilization of this function might cause Unexpected side effects.

ONOFF_CONFIG command Default value is 0x15h.

Bit	Purpose	Bit Value	Meaning	Default value	Supported
7:5	Reserved	Reserved	Reserved	Reserved	Reserved
4	Sets the default to either operate any time power is present or for the on/off to be controlled by CONTROL pin and serial bus commands	0	Unit powers up any time power is present regardless of state of the CONTROL pin	1	Ok
		1	Unit does not power up until commanded by the CONTROL pin and OPERATION command (as programmed in bits [3:0]).		

3	Controls how the unit responds to commands received via the serial bus	0	Unit ignores the on/off portion of the OPERATION command from serial bus	0	Ok
		1	To start, the unit requires that that the on/off portion of the OPERATION command is instructing the unit to run. Depending on bit [2], the unit may also require the CONTROL pin to be asserted for the unit to start and energize the output.		
2	Controls how the unit responds to the CONTROL pin	0	Unit ignores the CONTROL pin (on/off controlled only the OPERATION command)	1	Ok
		1	Unit requires the CONTROL pin to be asserted to start the unit. Depending on bit [3], the OPERATION command may also be required to instruct the device to start before the output is energized.		
1	Polarity of the CONTROL pin	0	Active low (Pull pin low to start the unit)	0	--
		1	Active high (Pull high to start the unit)		
0	CONTROL pin action when commanding the unit to turn off	0	Use the programmed turn off delay (Section 16.5) and fall time (Section 16.6)	1	--
		1	Turn off the output and stop transferring energy to the output as fast as possible. The device's product literature shall specify whether or not the device sinks current to decrease the output voltage fall time.		

Note: " -- " is Not supported

11.2.4 ON_OFF_CONFIG command operation note

Setting type	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Data value	Description[1]	Supported
1	0	X	X	X	0	0x00	If AC ok, turn-on power + DLY	--
2	0	X	X	X	1	0x01	If AC ok, turn-off power	OK
3	1	0	1	0	0	0x14	HW + LO + DLY	--
4	1	0	1	0	1	0x15	HW + LO	OK
5	1	0	1	1	0	0x16	HW + HI + DLY	--
6	1	0	1	1	1	0x17	HW + HI	--
7	1	1	0	X	0	0x18	SW + DLY	--
8	1	1	0	X	1	0x19	SW	OK
9	1	1	1	0	0	0x1C	HW + LO + SW + DLY	--
10	1	1	1	0	1	0x1D	HW + LO + SW	OK
11	1	1	1	1	0	0x1E	HW + HI + SW + DLY	--
12	1	1	1	1	1	0x1F	HW + HI + SW	--

Note: " -- " is Not supported

[1] :

X = don't care

HW = turn-on/off by control pin

HI = control pin active high turn-on power

LO = control pin active low turn-on power

SW = turn-on/off by operation command

DLY = turn-off delay

11.2.5 CLEAR_FAULTS Command (03h)

Operation Notice：

Null.

Power clear faults methods

The Power have four methods can be clear PMBus faults.

Method	Description
1	PMBus clear faults command
2	PMBus operation RESET[1]
3	PS RESET[1]
4	AC RESET[1]

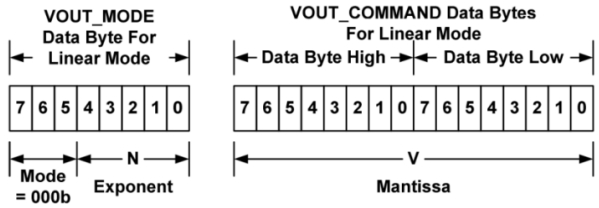
[1] : RESET mean is Turn-OFF → Turn-ON

11.2.6 VOUT_MODE Command (20h)

The data bytes for the VOUT_MODE and VOUT_COMMAND when using the Linear voltage data format are shown in Figure .

Note that the VOUT_MODE command is sent separately from output voltage related commands and only when the output voltage format changes.

VOUT_MODE is not sent every time an output voltage command is sent.



The Mode bits are set to 000b.

The Voltage, in volts, is calculated from the equation:

Voltage = $V \cdot 2^N$

Where:

Voltage is the parameter of interest in volts;

V is a 16 bit unsigned binary integer; and

N is a 5 bit two's complement binary integer.

11.2.7 SMBALERT_MASK Command (1Bh)

PMBus command	Bit location	PSU status when bit is asserted ("1")	Instances No PAGE'ing PAGE 00h = BMC PAGE 01h = ME	SMBALERT_MASK defaults for each of the three instances (No PAGE, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBAlert#

				1 = does not cause assertion of SMBAlert#
STATUS_WORD			No PAGE, 00h, 01h	
OFF	6 (lower)	OFF		NA
IOUT_OC_FAULT	4 (lower)	Refer to STATUS_IOUT		NA
TEMPERATURE	2 (lower)	Refer to STATUS_TEMPERATURE		NA
VIN_UV_FAULT	3 (lower)	Refer to STATUS_INPUT		NA
CML	1 (lower)	ON		NA
VOUT	7 (upper)	Refer to STATUS_VOUT		NA
IOUT/POUT	6 (upper)	Refer to STATUS_IOUT		NA
INPUT	5 (upper)	Refer to STATUS_INPUT		NA
FANS	2 (upper)	Refer to STATUS_FANS		NA
STATUS_VOUT			No PAGE'ing	
VOUT_OV_FAULT	7	OFF		1, NA, NA
VOUT_UV_FAULT	4	OFF		1, NA, NA
STATUS_IOUT			No PAGE'ing, 00h, 01h	
IOUT_OC_FAULT	7	OFF		1, 1, 1
IOUT_OC_WARNING	5	ON		1, 1, 0
POUT_OP_FAULT	1	OFF		1, 1, 1
POUT_OP_WARNING	0	ON		1, 1, 1
STATUS_INPUT			No PAGE'ing, 00h, 01h	
VIN_UV_WARNING	5	ON		1, 1, 1
VIN_UV_FAULT	4	OFF		1, 1, 0
Unit off for low input voltage	3	OFF		1, 1, 1
IIN_OC_WARNING	1	ON		1, 1, 1
PIN_OP_WARNING	0	ON		1, 1, 1
STATUS_TEMPERATURE			No PAGE'ing, 00h, 01h	
OT_FAULT	7	OFF		1, 1, 1
OT_WARNING	6	ON		1, 1, 0
STATUS_FANS_1_2			No PAGE'ing	
Fan_1_fault	7	OFF		1, NA, NA
Fan_1_warning	5	ON		1, NA, NA

11.2.8 STATUS_WORD Command (79h)

Byte	Bit Number	Status Bit Name	Meaning	Supported
Low	7	BUSY	A fault was declared because the device was busy and unable to respond.	--
	6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.	Ok
	5	VOUT_OV	An output overvoltage fault has occurred	Ok
	4	IOUT_OC	An output overcurrent fault has occurred	Ok
	3	VIN_UV	An input under voltage fault has occurred	Ok
	2	TEMPERATURE	A temperature fault or warning has occurred	Ok
	1	CML	A communications, memory or logic fault has occurred	Ok
	0	NONE OF THE ABOVE	A fault or warning not listed in bits [7:1] of this byte has occurred	--
High	7	VOUT	An output voltage fault or warning has occurred	Ok
	6	IOUT/POUT	An output current or output power fault or warning has occurred	Ok
	5	INPUT	An input voltage, input current, or input power fault or warning has occurred	Ok
	4	MFR_SPECIFIC	A manufacturer specific fault or warning has occurred	--

	3	POWER_GOOD#	The POWER_GOOD signal, if present, is negated	Ok
	2	FANS	A fan or airflow fault or warning has occurred	Ok
	1	OTHER	A bit in STATUS_OTHER is set	--
	0	UNKNOWN	A fault type not given in bits [15:1] of the SATUS_WORD has been detected	--

Note: " -- " is Not supported

11.2.9 STATUS_VOUT Command (7Ah)

Bit	Meaning	Supported
7	VOUT Over voltage Fault	Ok
6	VOUT Over voltage Warning	--
5	VOUT Under voltage Warning	--
4	VOUT Under voltage Fault	Ok
3	VOUT_MAX Warning (An attempt has been made to set the output voltage to value higher than allowed by the VOUT_MAX command	--
2	TON_MAX_FAULT	--
1	TOFF_MAX Warning	--
0	VOUT Tracking Error	--

Note: " -- " is Not supported

11.2.10 STATUS_IOUT Command (7Bh)

Bit	Meaning	Supported
7	IOUT Over current Fault	Ok
6	IOUT Over current And Low Voltage Shutdown Fault	--
5	IOUT Over current Warning	Ok
4	IOUT Under current Fault	--
3	Current Share Fault	--
2	Power Limiting	--
1	POUT Over power Fault	Ok
0	POUT Over power Warning	Ok

Note: " -- " is Not supported

11.2.11 STATUS_INPUT Command (7Ch)

Bit	Meaning	Supported
7	VIN Over voltage Fault	Ok
6	VIN Over voltage Warning	Ok
5	VIN Under voltage Warning	Ok
4	VIN Under voltage Fault	Ok
3	Unit Is Off For Insufficient Input Voltage	Ok
2	IIN Over current Fault	--
1	IIN Over current Warning	Ok
0	PIN Over power Warning	Ok

Note: " -- " is Not supported

11.2.12 STATUS_TEMPERATURE Command (7Dh)

Bit	Meaning	Supported
7	Over temperature Fault	Ok
6	Over temperature Warning	Ok
5	Under temperature Warning	--
4	Under temperature Fault	--
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

Note: " -- " is Not supported

11.2.13 STATUS_CML Command (7Eh)

Bit	Meaning	Supported
7	Invalid Or Unsupported Command Received	Ok
6	Invalid Or Unsupported Data Received	Ok
5	Packet Error Check Failed	--
4	Memory Fault Detected	--
3	Processor Fault Detected	--
2	Reserved	--
1	A communication fault other than the ones listed in this table has occurred	Ok
0	Other Memory Or Logic Fault has occurred.	--

Note: " -- " is Not supported

11.2.14 INPUT_TYPE Command (80h)

Bits	Value		Description	Supported
7:0	0000 0000	00h	No input	Ok
	0000 0001	01h	AC (Normal Airflow)	Ok
	0000 0010	02h	240V HVDC (Normal Airflow)	Ok
	0000 0100	04h	-48VDC (Normal Airflow)	--
	0001 0000	10h	AC (Reverse Airflow)	--
	0010 0000	20h	240V HVDC (Reverse Airflow)	--
	0100 0000	40h	-48VDC (Reverse Airflow)	--

Note: " -- " is Not supported

11.2.15 STATUS_FAN_1_2 Command (81h)

Bit	Meaning	Supported
7	Fan 1 Fault	Ok
6	Fan 2 Fault	--
5	Fan 1 Warning	Ok
4	Fan 2 Warning	--
3	Fan 1 Speed Overridden	Ok
2	Fan 2 Speed Overridden	--
1	Airflow Fault	--
0	Airflow Warning	--

Note: " -- " is Not supported

11.2.16 SMART_ON Command(D0h) (Module)

Value	State	Description
00h	Redundancy Mode	Turns the power supply ON into standard redundant load sharing mode.
01h	Active Mode	Defines this power supply is always ON in SMART ON configuration.
02h – 04h	Standby Mode	Defines the power supply that to turn off in a Smart On configuration and to turn on as the load increases.
05h	Standby Mode	Defines this power supply to be always in cold redundant configuration no matter what the load condition.

11.2.17 Bootloader Funcion(D4h, D5h, D6h, D7h, D8h, D9h)

Command	Name	Description
D4h	MFR_HW_COMPATIBILITY	Format: Read Word This is a COMPATIBILITY value used to tell if there are any changes in the FW that create an incompatibility with the FW. This value only changes when the PSU HW is changed creating an incompatibility with older versions of FW.

D5h	MFR_FWUPLOAD_CAPABILITY	Format: Read Byte Bit0: 1 = PSU support FW uploading in standby mode only
D6h	MFR_FWUPLOAD_MODE	Format: Read/Write Byte The system can use this command at any time to restart sending the FW image. Bit0: 0 = exit firmware upload mode 1 = firmware upload mode
D7h	MFR_FWUPLOAD	Format: Block Write (block = size as defined by the image header) Command used to send each block of the FW image.
D8h	MFR_FWUPLOAD_STATUS	Format: Read Word Reset: all bits get reset to '0' when the power supply enters FW upload mode. Bit0: 1 = Full image received successfully Bit1: 1 = Full image not received yet. The PSU will keep this bit asserted until the full image is received by the PSU. Bit2: 1 = Full image received but image is bad or corrupt. Power supply can power off. Bit4: 1 = FW image not supported by PSU. If the PSU receives the image header and determines that the PSU HW does not support the image being sent by the system.
D9h	MFR_FW_REVISION	Format: Block Read, 3 bytes Byte0: Minor revision; secondary Byte1: Minor revision; primary Byte2: Bit 7: 1-> Down grading of PSU FW has to be avoided. System BMC can elect to ignore this bit if needed, but recommended to follow. 0->No restriction in downgrading the PSU FW. BMC can update the PSU FW to be in sync with its known version. Bit 0-6: Major revision

11.3 Firmware control rules

11.3.1 Auto fan control rule

1. Temperature and load control Fan speed

Fan(rpm) = 4000 + [(115 – ac voltage) * 34] + [(Ambient_Temperature - 25) * 55] + [(Iout -35) * 228] +

[(Primary_Hot_Spot_Temperature - 55) * 750]

11.3.2 LED control rules

Event	Green led	Amber led
No AC power plug in.	OFF	OFF
AC ok + power turn-off.	Every 0.5sec blink once.	OFF
AC ok + power turn-on, no failure event.	ON	OFF
AC ok + power turn-on, failure event.	OFF	ON
AC ok + power turn-on, warning event.	Green and Amber led on every 0.5sec exchange of blink.	Green and Amber led on every 0.5sec exchange of blink.

11.4 Firmware Protection

1. Over Voltage

Output voltage	Warning threshold	Protect threshold
12V	--	13.8V
Input voltage	**Warning threshold**	**Protect threshold**
90Vac ~ 264Vac	305Vac	310Vac ±5V
180Vdc ~310Vdc	340Vdc	350Vdc ±5V

2. Under Voltage

Output voltage	Warning threshold	Protect threshold
12V	--	9V
Input voltage	**Warning threshold**	**Protect threshold**
90Vac ~ 264Vac	85Vac	75Vac (75~85Vac delay 20 seconds power off)
180Vdc ~ 310Vdc	--	165Vdc

Note: When Vin is 75~85Vac , 0 ~ 1 seconds 0x7C (Status Input) will display a warn, >20seconds 0x7C (Status Input) will display warn & Fault, the power will shut down.

3. Iout Over Current

Spec	Description	MIN	MAX	MIN	MAX
OPP / Fast OCP 1	Over power protection (asserted SMBAlert# signal & voltage foldback then hiccup mode)	Rating +45A	--	100μsec	--
Slow OCP	Slow over current protection (shutdown and hiccup mode)	Rating + 10A	Rating + 14A	20msec	100msec
Fast OCW 2	Fast over current warning (asserted SMBAlert# signal)	Rating + 30A	--	10msec	15msec
Slow OCW 3	Slow over current warning (asserted SMBAlert# signal)	Rating + 6A	Rating + 10A	15msec	20msec
OCPstby	Stby over current protection (shutdown, hiccup mode)	4.0A	--	1msec	100msec

Note: 1.MCU readings have a +/-2% tolerance for actual application.

2. Input voltage 90-120V, rating current is 81.8A.

4. Over Temperature

Temperature1：Power inside Environmental temperature

Temperature2：Power secondary heat sink temperature

Temperature3：Power primary heat sink temperature

	Warning threshold	Protect threshold	Re-start temp
Temperature 1	62±2°C	66±2°C	55±2°C
Temperature 2	--	--	--
Temperature 3	--	125±2°C	105±2°C

5. Fan Speed Protection

	Warning threshold	Protect threshold
Fan 1	1500rpm	1000rpm

Note: MCU readings have a +/-2% tolerance for actual application.

11.5 Black Box

This specification defines the requirements for power supplies with PMBus capability to store PMBus and other data into non-volatile memory inside the power supply. The data shall be saved to non-volatile memory upon a critical failure that caused the power supply to shutdown. The data can be accessed viha the PMBus interface by applying power to the 12Vstby pins. No AC power need to be applied to the power supply.

11.5.1 When data is saved to the Black Box?

Data is saved to the Black Box for the following fault events:

General fault

Over voltage on output

Over current on output

Loss of AC input

Input voltage fault

Fan failure

Over temperature

11.5.2 Black Box Events

There are two types of data saved in the black box; 1) System Tracking Data, 2) Power supply event data.

System tracking data is saved to the Black Box whenever the system powers ON or when a power supply is added to the system.

11.5.3 Black Box Process

System writes system tracking data to the power supply RAM at power ON

System writes the real time clock data to the PSU RAM once every ~5 minutes

Power supply tracks number of PSON and AC power cycles in EEPROM

Power supply tracks ON time in EEPROM

Power supply loads warning and fault event counter data from EEPROM into RAM

Upon a warning event; the PSU shall increment the associated counter in RAM.

Upon and fault event the PSU shall increment the associated counter in RAM

Upon a fault event that causes the PSU to shutdown all event data in the PSU's RAM is saved to event data location N in the power supply's EEPROM. This data includes the real time clock, number of AC & PSON power cycles, PSU ON time, warning event counters and fault event counters.

11.5.4 Commands

Name: MFR_BLACKBOX

Format: Read Block with PEC (238 bytes)

Code: DCh

	Item	Number of Bytes	Description
System Tracking Data	System top assembly number	10	The system will write its Intel part number for the system top assembly to the power supply when it is

			powered ON. This is 9 ASCI characters.
	System serial number	10	The system shall write the system serial number to the power supply when it is powered ON. This include the serial number and date code.
	Motherboard assembly number	10	The system will write the motherboard Intel part number for the assembly to the power supply when it is powered ON. This is 9 ASCI characters.
	Motherboard serial number	10	The system shall write the motherboard's serial number to the power supply when it is
			powered ON. This includes the serial number and date code.
	Present total PSU ON time	3	Total on time of the power supply with PSON asserted in minutes. LSB = 1 minute.
	Present number of AC power cycles	2	Total number of times the power supply powered OFF then back ON due to loss of AC power. This is only counted when the power supply's PSON# signal is asserted. This counter shall stay at FFFFh once the max is reached.
	Present number of PSON power cycles	2	Total number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting. This is only counted when AC power is present to the power supply. This counter shall stay at FFFFh once the max is reached.
Power supply event data (N)		38	Most recent occurrence of saved black box data
Time Stamp			The power supply shall track these time and power cycle counters in RAM. When the a black box event occurs the data is saved into the Black Box.
	Power supply total power on time	3	Total on time of the power supply in minutes. LSB = 1 minute.
	Real Time Clock Data from System (reserved for future use)	4	This time stamp does not need to generated by the power supply. The system rights a real time clock value periodically to the power supply using the MFR_REAL_TIME command. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT.

			Similar time formats are used in ANSI C
	Number of AC power cycles	2	Number of times the power supply powered OFF then back ON due to loss of AC power at the time of the event. This is only counted when the power supply's PSON# signal is asserted.
	Number of PSON power cycles	2	Number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting at the time of the event. This is only counted when AC power is present to the power supply.
PMBus			The power supply shall save these PMBus values into the Black Box when a black box event occurs. Fast events may be missed due to the filtering effects of the PMBus sensors.
	STATUS_WORD	2	
	STATUS_IOUT	1	
	STATUS_INPUT	1	
	STATUS_TEMPERTATURE	1	
	STATUS_FAN_1_2	1	
	READ_VIN	2	
	READ_IIN	2	
	READ_IOUT	2	
	READ_TEMPERATURE_1	2	
	READ_TEMPERATURE_2	2	
	READ_FAN_SPEED_1	2	
	READ_PIN	2	
	READ_VOUT	2	
Event Counters			The power supply shall track the total number for each of the following events. These value shall be saved to the black box when a black box event occurs. Once a value has reached 15, it shall stay at 15 and not reset.
	AC shutdown due to under voltage on input	Lower ½	The power supply shall save a count of these critical events to non-volatile memory each time they occur. The counters will increment each time the associated STATUS bit is asserted.
	Thermal shutdown	Upper ½	
	Over current or over power shutdown on output	Lower ½	
	General failure shutdown	Upper ½	
	Fan failure shutdown	Lower ½	
	Shutdown due to over voltage on output	Upper ½	
	Input voltage warning; no shutdown	Lower ½	The power supply shall save into RAM a count of these warning events. Events are count only at the

			initial assertion of the event/bit. If the event persists without clearing the bit the counter will not be incremented. When the power supply shuts down it shall save these warning event counters to non-volatile memory. The counters will increment each time the associated STATUS bit is asserted.
	Thermal warning; no shutdown	Upper ½	
	Output current power warning; no shutdown	Lower ½	
	Fan slow warning; no shutdown	Upper ½	
	Power supply event data (N-1)	38	
	Power supply event data (N-2)	38	
	Power supply event data (N-3)	38	
	Power supply event data (N-4)	38	

Name: MFR_REAL_TIME_BLACK_BOX

Format: Write/Read Block with PEC (4 bytes)

Code: DDh

The system shall use this command to periodically write the real time clock data to the power supply.

Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C.

Name: MFR_SYSTEM_BLACK_BOX

Format: Write/Read Block with PEC (40 bytes). Low byte first.

Code: DEh

The system uses this command to write the following data to the PSU.

Item	Bytes	
System top assembly number	1-10	Low bytes
System serial number	11-20	
Motherboard assembly number	21-30	
Motherboard serial number	31-40	High bytes

Name: MFR_BLACKBOX_CONFIG

Format: Read/Write Byte with PEC

Code: DFh

Bit	Value	Description
0	0 = disable black box function 1 = enable black box function	Writing a 1 enables the power supply with black box function. Writing a 0 disables the power supply black box function. The state of MFR_BLACKBOX_CONFIG shall be saved in non-volatile memory so that it is not lost during power cycling.

		Intel shall receive the power supply with the black box function enabled; bit 0 = ‘1’.
1-7	reserved	