innodisk

Total Solution For Industrial Flash Storage

iCF 1IE2

Customer: _____

Customer Part Number: _____

Innodisk Part Number: _____

Innodisk Model Name: _____

Date: _____

Innodisk Approver	Customer Approver

Features:

- PATA
- Innodisk MLC NAND
- Support iSLC technology
- iCF 1IE2
- Standard & Wide-temperature
- iPowerguard
- iDataguard
- Dynamic Thermal Management

Performance:

- Sequential Read up to 85 MB/s
- Sequential Write up to 55 MB/s

Power Requirements:

Input Voltage:	5V±5%
Max Operating Wattage:	0.60W
Idle Wattage:	0.02W

Reliability:

Capacity	TBW	DWPD
4GB	TBD	TBD
8GB	TBD	TBD
16GB	TBD	TBD
32GB	TBD	TBD
64GB	TBD	TBD
128GB	TBD	TBD

Data Retention	1 Year
Warranty	5 Years

For warranty details, please refer to:

https://www.innodisk.com/en/support_and_service/warrant

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REVISION HISTORY

Revision	Description	Date
Preliminary 0.1	First Release	Aug., 2021

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1. PRODUCT OVERVIEW

Introduction of Innodisk iCF 1IE2

The Innodisk Industrial CompactFlash® 1IE2 Memory Card (iCF 1IE2) products provide high capacity solid-state flash memory that electrically complies with the True IDE Mode that is electrically compatible with an IDE disk drive. The original CF form factor card can be used in any system that has a CF slot.

Designed to replace traditional rotating disk drives, Innodisk Industrial CompactFlash® 1IE2 Memory Cards are embedded solid-state data storage systems for mobile computing and the industrial working place. The Industrial CompactFlash® features an extremely lightweight, reliable, low-profile form factor. Industrial CompactFlash® 1IE2 (iCF 1IE2) support advanced PIO (0-6), Multiword DMA (0-4), Ultra DMA (0-6) transfer mode, multi-sector transfers, and LBA addressing.

Figure 1 Product Photo of iCF 1IE2

2. Product Feature

The Industrial ATA products provide the following system features:

- Capacity:
  4GB~128GB
- Fully compatible with CompactFlash® specification version 6.0
- Fully compatible with the IDE standard interface, ATA Standard
- Flexible 96-Bit/1KB BCH ECC engine
- Support +3.3V/+5V single power supply operation.
  * for 3.3V product requirement please contact sales for customization_3.3V power design
- Support Auto Stand-by and Sleep Mode.
- Power Consumption: 5V

Read: 0.60 W
Write: 0.59 W
Idle: 0.02 W
Peak: 2.73 W

- Support advanced PIO (0-6), Multiword DMA (0-4), Ultra DMA (0-6) transfer mode.
  *Default transfer mode: UDMA 5.
- MTBF 3,000,000 hours
- Data retention: 10 years
- R/W performance:

Capacity	Unit	4GB	8GB	16GB	32GB	64GB	128GB
Max Sequential Read	MB/s	85	85	85	85	85	85
Max Sequential Write		50	55	55	55	55	55
Max 4K Random Read	IOPS	4,000	3,800	3,800	3,800	3,800	3,800
Max 4K Random Write		1,200	1,200	1,200	1,200	1,200	1,200

Note: Performance test is based on CrystalDiskMark 6.0.2 with file size 1000MB and Queue Depth 32

- Operating temperature range:
  - Standard Grade: 0°C ~ +70°C
  - Industrial Grade: -40°C ~ +85°C
- Storage temperature range: -40°C ~ +85°C
- Read disturb management with the data refresh triggered by the Read count of each block for maximize data retention.
- Support iPowerGuard with voltage power-down detection for full power-down robustness. iPowerGuard technology is a set of preventive measures that protect the SSD in an unstable power supply environment. This comprehensive package comprises safeguards for startup and shutdown to maintain device performance and ensure data integrity.

  Notes: iPowerGuard cannot be used in PC Card Memory Mode or PC Card I/O Mode because the power on sequence will be over spec.

  If CF card is using in PC Card Memory Mode or PC Card I/O Mode, please contact sales for customization_removing iPowerGuard function.
- Support iDataGuard with an internal voltage detector functions before and after a sudden power outage to SSD. Low-power detection terminates data writing before an abnormal power-off, while table-remapping after power-on deletes corrupt data and maintains data integrity. Innodisk's iDataGuard provides effective power cycling management, preventing data stored in flash from degrading with use.

3. Product Specifications

3.1 Pin Assignment

See Table 1 for iCF 1IE2 pin assignments.

Table 1: iCF 1IE2 Pin Assignments

PC Card Memory Mode[10]			PC Card I/O Mode[10]			True IDE Mode		
Pin No.	**Name**	**I/O**	**Pin No.**	**Name**	**I/O**	**Pin No.**	**Name**	**I/O**
1	GND		1	GND		1	GND	
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	-CE1	I	7	-CE1	I	7	-CS0	I
8	A10	I	8	A10	I	8	A10[2]	I
9	-OE	I	9	-OE	I	9	-ATA SEL	I
10	A09	I	10	A09	I	10	A09[2]	I
11	A08	I	11	A08	I	11	A08[2]	I
12	A07	I	12	A07	I	12	A07[2]	I
13	VCC		13	VCC		13	VCC	
14	A06	I	14	A06	I	14	A06[2]	I
15	A05	I	15	A05	I	15	A05[2]	I
16	A04	I	16	A04	I	16	A04[2]	I
17	A03	I	17	A03	I	17	A03[2]	I
18	A02	I	18	A02	I	18	A02	I
19	A01	I	19	A01	I	19	A01	I
20	A00	I	20	A00	I	20	A00	I
21	D00	I/O	21	D00	I/O	21	D00	I/O
22	D01	I/O	22	D01	I/O	22	D01	I/O
23	D02	I/O	23	D02	I/O	23	D02	I/O
24	WP	O	24	-IOIS16	O	24	-IOCS16	O
25	-CD2	O	25	-CD2	O	25	-CD2	O
26	-CD1	O	26	-CD1	O	26	-CD1	O

27	D11[1]	I/O	27	D11[1]	I/O	27	D11[1]	I/O
28	D12[1]	I/O	28	D12[1]	I/O	28	D12[1]	I/O
29	D13[1]	I/O	29	D13[1]	I/O	29	D13[1]	I/O
30	D14[1]	I/O	30	D14[1]	I/O	30	D14[1]	I/O
31	D15[1]	I/O	31	D15[1]	I/O	31	D15[1]	I/O
32	-CE2[1]	I	32	-CE2[1]	I	32	-CS1[1]	I
33	-VS1	O	33	-VS1	O	33	-VS1	O
34	-IORD	I	34	-IORD	I	34	-IORD[7] HSTROBE[8] -HDMARDY[9]	I
35	-IOWR	I	35	-IOWR	I	35	-IOWR[7] STOP[8, 9]	I
36	-WE	I	36	-WE	I	36	-WE[3]	I
37	READY	O	37	-IREQ	O	37	INTRQ	O
38	VCC		38	VCC		38	VCC	
39	-CSEL[5]	I	39	-CSEL[5]	I	39	-CSEL	I
40	-VS2	O	40	-VS2	O	40	-VS2	O
41	RESET	I	41	RESET	I	41	-RESET	I
42	-WAIT	O	42	-WAIT	O	42	IORDY[1] -DDMARDY[8] DSTROBE[9]	O
43	-INPACK	O	43	-INPACK	O	43	DMARQ	O
44	-REG	I	44	-REG	I	44	-DMACK[6]	I
45	BVD2	O	45	-SPKR	O	45	-DASP	I/O
46	BVD1	O	46	-STSCHG	O	46	-PDIAG	I/O
47	D08[1]	I/O	47	D08[1]	I/O	47	D08[1]	I/O
48	D09[1]	I/O	48	D09[1]	I/O	48	D09[1]	I/O
49	D10[1]	I/O	49	D10[1]	I/O	49	D10[1]	I/O
50	GND		50	GND		50	GND	

Note:

1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
2) The signal should be grounded by the host.
3) The signal should be tied to VCC by the host.
4) The mode is optional for CF Cards, but required for CompactFlash® Storage Cards.
5) The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card

modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.

6) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition
7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.
8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.
9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.
10) If CF card is using in PC Card Memory Mode or PC Card I/O Mode, please contact sales for customization_removing iPowerGuard function.

3.2 Pin Description

Table 2 describes the pin descriptions for iCF 1IE2

Table 2: iCF 1IE2 Pin Description

Pin No.	Pin Name	I/O	Mode	Description
8,10,11, 12,14,15,16,17,18 19, 20	A10 – A0	I	PC Card Memory Mode	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash® Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash® Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers.
8,10,11, 12,14,1516,17,181 9, 20	A10 – A0		PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
18,19,20	A2 – A0		True IDE Mode	In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
46	BVD1	I/O	PC Card Memory Mode	This signal is asserted high, as BVD1 is not supported.
	-STSCHG		PC Card I/O Mode	This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card configuration and Status Register.
	-PDIAG		True IDE	In the True IDE Mode, this input / output is the Pass Diagnostic

			Mode	signal in the Master / Slave handshake protocol.
45	BVD2	I/O	PC Card Memory Mode	This signal is asserted high, as BVD2 is not supported.
	-SPKR		PC Card I/O Mode	This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
	-DASP		True IDE Mode	In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
26, 25	-CD1, -CD2	O	PC Card Memory Mode	These Card Detect pins are connected to ground on the CompactFlash® Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash® Storage Card or CF+ Card is fully inserted into its socket.
			PC Card I/O Mode	This signal is the same for all modes.
			True IDE Mode	This signal is the same for all modes.
7, 32	-CE1, -CE2	I	PC Card Memory Mode	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7.
	-CE1, -CE2		PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
	-CS0, -CS1		True IDE Mode	In the True IDE Mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
39	-CSEL	I	PC Card Memory Mode	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
			PC Card I/O Mode	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
			True IDE Mode	This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When

				the pin is open, this device is configured as a Slave.
2,3,4,5,6,31,30,29 ,28,27,49,48,47,23 ,22,21	D15 - D00	I/O	PC Card Memory Mode	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
			PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
			True IDE Mode	In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
1, 50	GND	-	PC Card Memory Mode	Ground.
			PC Card I/O Mode	This signal is the same for all modes.
			True IDE Mode	This signal is the same for all modes.
43	-INPACK	O	PC Card Memory Mode	This signal is not used in this mode.
	-INPACK		PC Card I/O Mode	The Input Acknowledge signal is asserted by the CompactFlash® Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash® Storage Card or CF+ Card and the CPU.
	DMARQ		True IDE Mode	This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK, i.e., the device shall wait until the host asserts -DMACK before negating DMARQ, and reasserting DMARQ if there is more data to transfer. DMARQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the

				host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.
34	-IORD	I	PC Card Memory Mode	This signal is not used in this mode.
			PC Card I/O Mode	This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash® Storage Card or CF+ Card when the card is configured to use the I/O interface.
	-IORD		True IDE Mode	In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.
	-HDMARDY			In True IDE Mode when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate -HDMARDY to pause an Ultra DMA transfer.
	HSTROBE			In True IDE Mode when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
35	-IOWR	I	PC Card Memory Mode	This signal is not used in this mode.
	-IOWR		PC Card I/O Mode	The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash® Storage Card or CF+ Card controller registers when the CompactFlash® Storage Card or CF+ Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
	-IOWR		True IDE Mode	In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.

	STOP			In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
9	-OE	I	PC Card Memory Mode	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash® Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers.
	-OE		PC Card I/O Mode	In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
	-ATA SEL		True IDE Mode	To enable True IDE Mode this input should be grounded by the host.
37	READY	O	PC Card Memory Mode	In Memory Mode, this signal is set high when the CompactFlash® Storage Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash® Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash® Storage Card or CF+ Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.
	-IREQ		PC Card I/O Mode	I/O Operation – After the CompactFlash® Storage Card or CF+ Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
	INTRQ		True IDE Mode	In True IDE Mode signal is the active high Interrupt Request to the host.
44	-REG	I	PC Card Memory Mode	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
			PC Card I/O Mode	The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.
	-DMACK		True IDE Mode	This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the -DMACK signal, including a floating condition. If DMA operation is not

				supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
41	RESET	I	PC Card Memory Mode	The CompactFlash® Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash® Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
	RESET		PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
	-RESET		True IDE Mode	In the True IDE Mode, this input pin is the active low hardware reset from the host.
13, 38	VCC	-	PC Card Memory Mode	+5 V, +3.3 V power.
			PC Card I/O Mode	This signal is the same for all modes.
			True IDE Mode	This signal is the same for all modes.
33, 40	-VS1, -VS2	O	PC Card Memory Mode	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the CompactFlash® Storage Card or CF+ Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.
			PC Card I/O Mode	This signal is the same for all modes.
			True IDE Mode	This signal is the same for all modes.
42	-WAIT	O	PC Card Memory	The -WAIT signal is driven low by the CompactFlash® Storage Card or CF+ Card to signal the host to delay completion of a

			Mode	memory or I/O cycle that is in progress.
	-WAIT		PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
	IORDY		True IDE Mode	In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.
	-DDMARDY			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer.
	DSTROBE			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
36	-WE	I	PC Card Memory Mode	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash® Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
			PC Card I/O Mode	In PC Card I/O Mode, this signal is used for writing the configuration registers.
			True IDE Mode	In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
24	WP	O	PC Card Memory Mode	Memory Mode – The CompactFlash® Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
	-IOIS16		PC Card I/O Mode	I/O Operation – When the CompactFlash® Storage Card or CF+ Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
	-IOCS16		True IDE Mode	In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

3.3 CE and FCC Compatibility

iCF 1IE2 conforms to CE and FCC requirements.

3.4 RoHS Compliance

iCF 1IE2 is fully compliant with RoHS directive.

3.5 Insertion

Compact Flash card 50pins connector: >10,000 times

3.6 Environmental Specifications

3.6.1 Temperature Ranges

Operating Temperature Range:

- Standard Grade: 0°C to +70°C
- Industrial Grade: -40°C to +85°C

Storage Temperature Range: -40°C to +85°C

3.6.2 Humidity

Relative Humidity: 10-95%, non-condensing

3.6.3 Shock and Vibration

Table 3: Shock/Vibration Test for iCF 1IE2

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2 KHz, 20 g, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms, 1500 g, 3 axes	IEC 68-2-27

3.6.4 Mean Time between Failures (MTBF)

Table 4 summarizes the MTBF prediction results for various iCF 1IE2 configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 4: iCF 1IE2 MTBF

Product	Condition	MTBF (Hours)
iCF 1IE2	Telcordia SR-332 GB, 25°C	3,000,000

3.7 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements a algorithm that can correct 96 bits per 1 KB in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

3.8 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the ***erase cycle limit*** or ***write endurance limit*** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

iCF 1IE2 uses a wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime.

3.9 NAND Flash Memory and Endurance

Innodisk CF 1IE2 uses Multi-Level Cell (MLC) NAND flash memory, which is non-volatility, high reliability and high speed memory storage.

Parameter	Value
Read Cycles	Unlimited Read Cycles
Wear-Leveling Algorithm	Support
Bad Blocks Management	Support
Error Correct Code	Support
Thermal Sensor	Support
TBW* (Total Bytes Written) Unit: TB	
4GB	TBD
8GB	TBD
16GB	TBD
32GB	TBD
64GB	TBD
128GB	TBD
*Total bytes written is based on JEDEC 218. (Solid-State Drive Requirements and Endurance Test Method) **Lifespan is calculated by device written per day.	

3.10 Mechanical dimensions

Mechanical Dimension: 42.80±0.1/36.40±0.1/3.30±0.1mm (W/T/H)

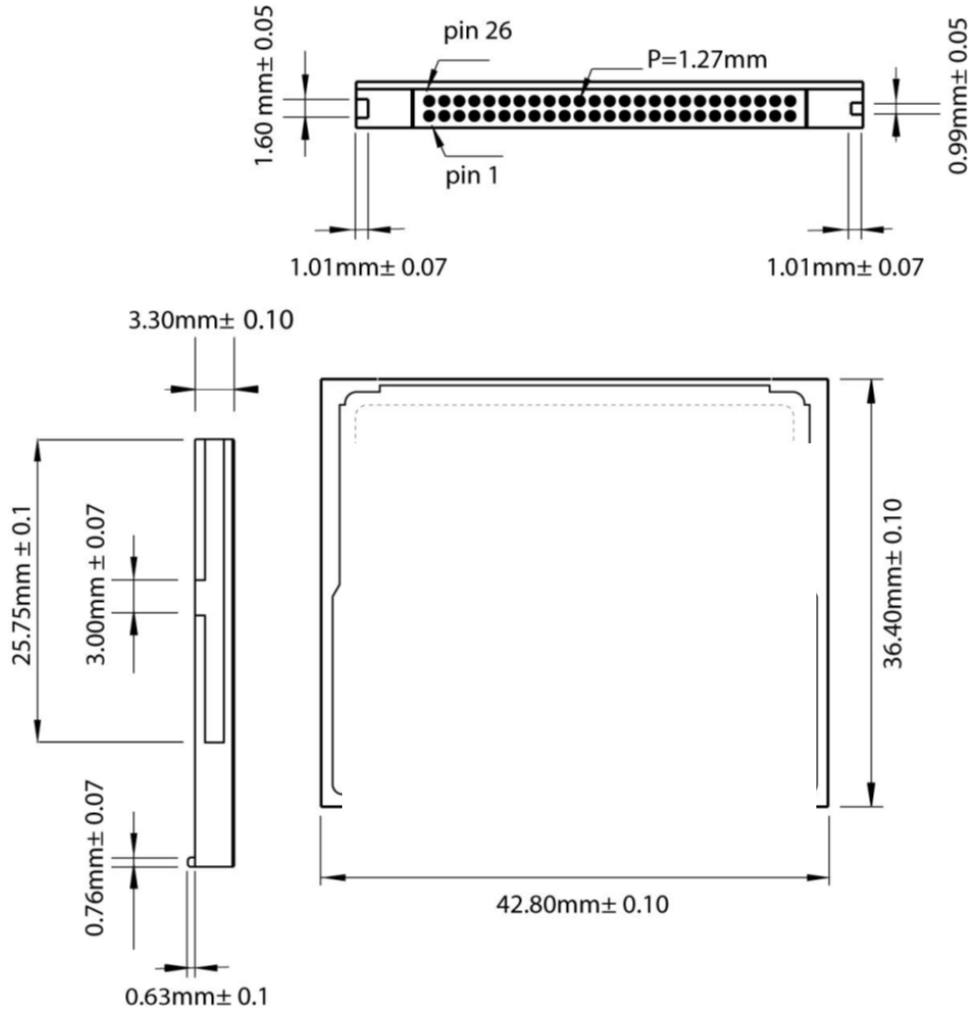

Figure 2 Mechanical Dimension of iCF 1IE2

3.11 Electrical Specifications

3.11.1 DC Characteristic

Item	Symbol	Rating	Unit
Input voltage	V_{IN}	+5 DC ± 0.5	V
		+3.3 DC ± 0.3	

* for 3.3V product requirement please contact sales for customization_3.3V power design

3.11.2 Timing Specifications

3.11.2.1 Attribute Memory Read Timing Specification

Attribute Memory access time is defined as 300ns. Detailed timing specs are shown in Table 5.

Table 5: Attribute Memory Read Timing

Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Read cycle time	tc(R)	tAVAV	250	
Address access time	ta(A)	tAVQV		250
Card enable access time	ta(CE)	tELQV		250
Output enable access time	ta(OE)	tGLQV		125
Output disable time from CE	tdis(CE)	tEHQZ		100
Output disable time from OE	tdis(OE)	tGHQZ		100
Address setup time	tsu(A)	tAVGL	30	
Output enable time from CE	ten(CE)	tELQNZ	5	
Output enable time from OE	ten(OE)	tGLQNZ	5	
Data valid from address change	tv(A)	tAXQX	0	

Note: All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -CE signal or both the -OE signal and the -WE signal shall be de-asserted between consecutive cycle operations.

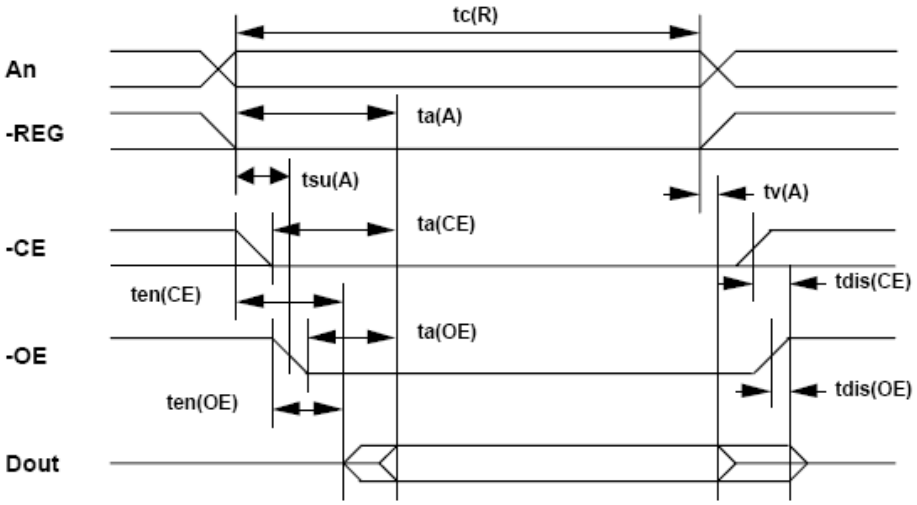

Figure 3: Attribute Memory Read Timing Diagram

3.11.2.2 Configuration Register (Attribute Memory) Write Timing Specification

The Card Configuration write access time is defined as 250ns. Defined timing specifications are shown in Table 6.

Table 6: Configuration Register (Attribute Memory) Write Timing

Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Write cycle time	tc(W)	tAVAV	80	
Write pulse width	tw(WE)	tWLWH	55	
Address setup time	tsu(A)	tAVWL	10	
Write recovery time	trec(WE)	tWMAX	30	
Data setup time for WE	tsu(D-WEH)	tDVWH	80	
Data hold time	th(D)	tWMDX	30	

Note: All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash storage card or CF+ card.

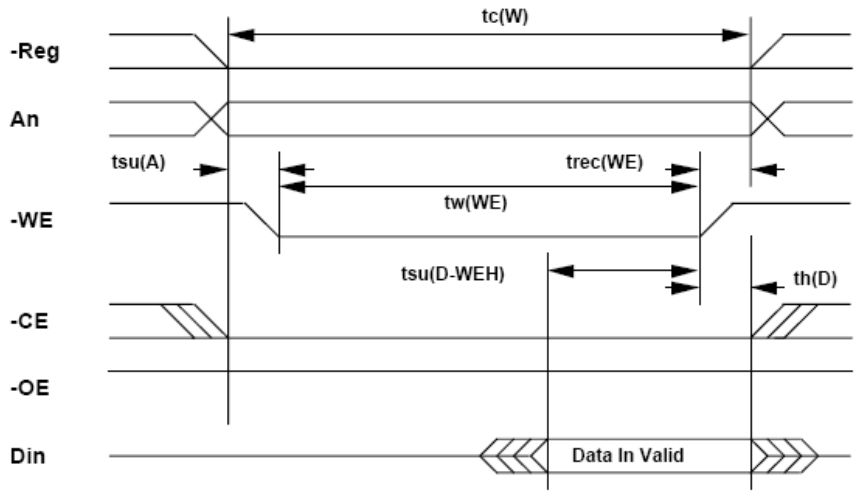

Figure 4 Configuration Register (Attribute Memory) Write Timing Diagram

3.11.2.3 Common Memory Read Timing Specification

Table 7: Common Memory Read Timing

Cycle Time Mode:			**250ns**		**120ns**		**100ns**		**80ns**	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Output enable access time	ta(OE)	tGLQV		125		60		50		40
Output disable time from OE	tdis(OE)	tGHQZ		100		60		50		40
Address setup time	tsu(A)	tAVGL	30		15		10		10	
Address hold time	th(A)	tGHAX	20		15		15		10	
CE setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE hold following OE	th(CE)	tGHEH	20		15		15		10	
Wait delay falling from OE	tv(WT-OE)	tGLWTV		35		35		35		Na
Data setup for wait release	tv(WT)	tQVWTH		0		0		0		Na

Wait width time	tw(WT)	tWTLWTH		350 (3000 for CF+)		350 (3000 for CF+)		350 (3000 for CF+)		Na

Note: 1) –WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12μs but is intentionally less in this specification.

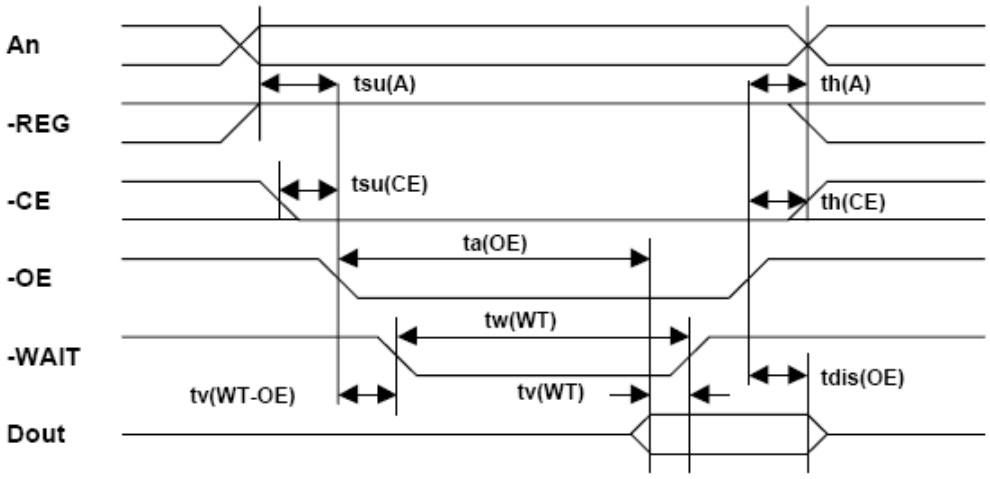

Figure 5 Common Memory Read Timing Diagram

3.11.2.4 Common Memory Write Timing Specification

Table 8: Common Memory Write Timing

Cycle Time Mode:			**250ns**		**120ns**		**100ns**		**80ns**	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before WE	tsu(D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	

CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		15	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV		35		35		35		Na
WE High from Wait Release	tv(WT)	tWTHWH	0		0		0		na	
Wait Width Time	tw(WT)	tWTLWTH		350 (3000 for CF+)		350 (3000 for CF+)		350 (3000 for CF+)		Na

Notes: 1) –WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12μs but is intentionally less in this specification.

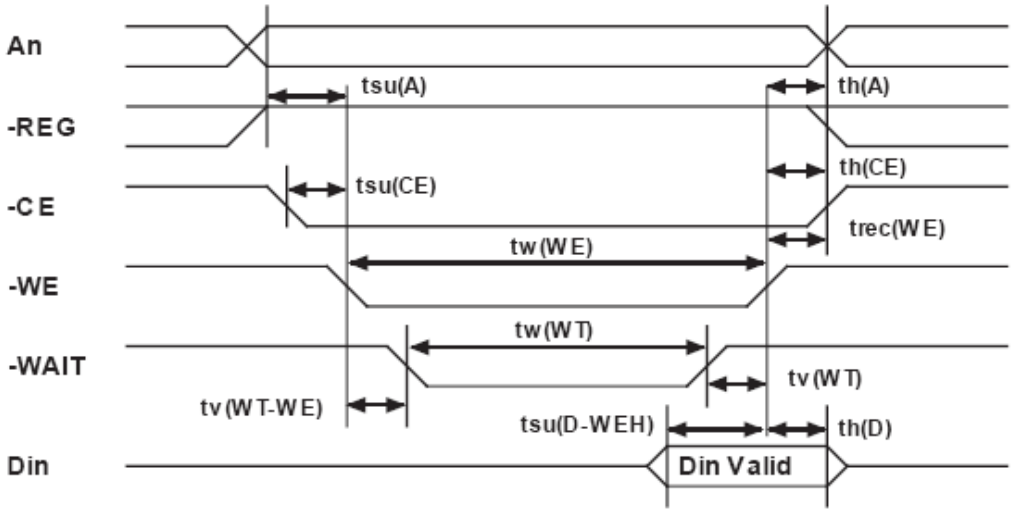

Figure 6 Common Memory Write Timing Diagram

3.11.2.5 I/O Input (Read) Timing Specification

Table 9: I/O Read Timing

Cycle Time Mode:			**250 ns**		**120 ns**		**100 ns**		**80 ns**	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Delay after IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tIGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10		10		10	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10		10		10	
REG Setup before IORD	tsuREG (IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG (IORD)	tIGHRGH	0		0		0		0	
INPACK Delay Falling from IORD3	tdfINPACK (IORD)	tIGLIAL	0	45	0	na1	0	na1	0	na1
INPACK Delay Rising from IORD3	tdrINPACK (IORD)	tIGHIAH		45		na1		na1		na1
IOIS16 Delay Falling from Address3	tdfIOIS16 (ADR)	tAVISL		35		na1		na1		na1
IOIS16 Delay Rising from Address3	tdrIOIS16 (ADR)	tAVISH		35		na1		na1		na1

Notes:1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA specification of 12μs but is intentionally less in this spec.

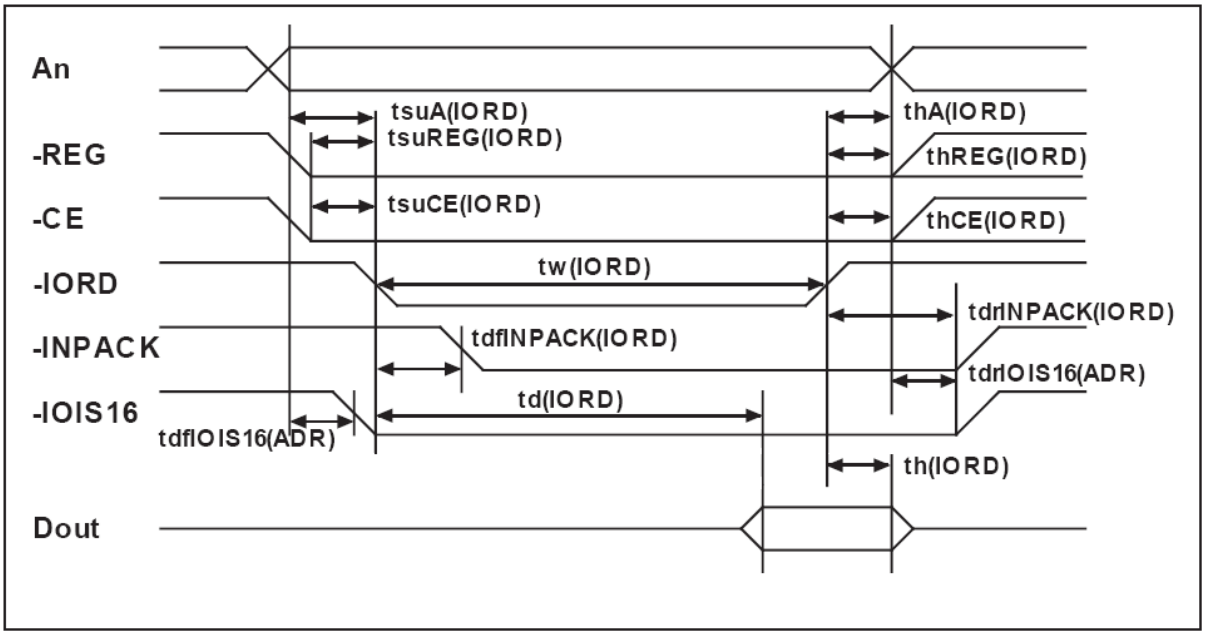

Figure 7 I/O Read Timing Diagram

3.11.2.6 Timing Specification

Table 10: I/O Write Timing

Cycle Time Mode:			**250ns**		**120ns**		**100ns**		**80ns**	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
IOWR Width Time	tw(IOWR)	tIWLIWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		25	
Address Hold following	thA(IOWR)	tIWHAX	20		20		10		10	

IOWR										
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20		20		10		10	
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35		Na1		Na1		Na1
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35		Na1		Na1		Na1

Notes: 1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA specification of 12 µs but is intentionally less in this specification.

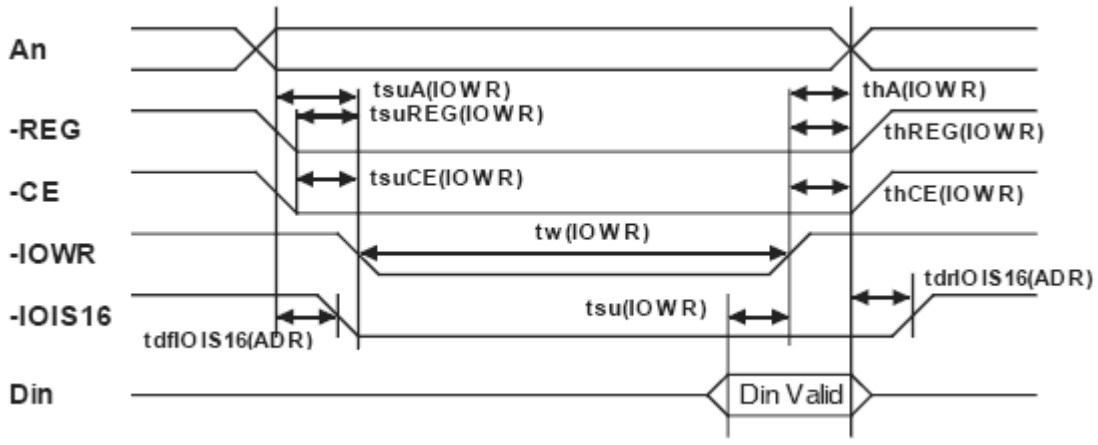

Figure 8 I/O Write Timing Diagram

3.11.2.7 True IDE PIO Mode Read/Write Timing Specification

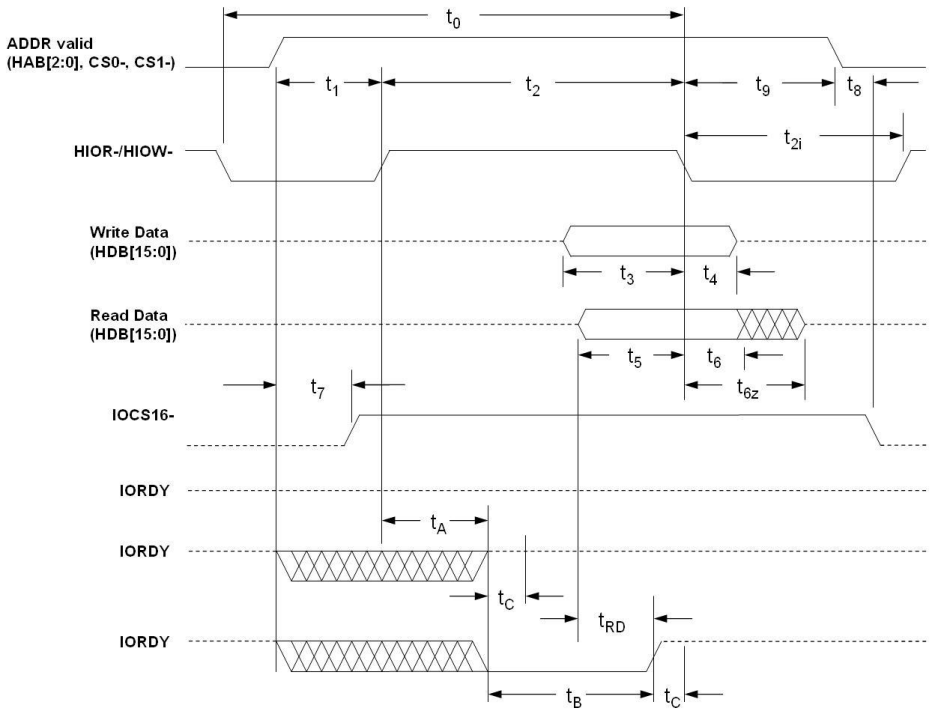

Figure 9 Read/Write Timing Diagram, PIO Mode

Table 11: Read/Write Timing Specifications, PIO Mode 0-6

PIO timing parameters		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
t_0	Cycle time (min.)	600	383	240	180	120	100	80
t_1	Address valid to HIOR-/HIOW- setup (min.)	70	50	30	30	25	15	10
t_2	HIOR-/HIOW- 16-bit (min.)	165	125	100	80	70	65	55
t_2	HIOR-/HIOW- Register 8-bit (min.)	290	290	290	80	70	65	55
t_{2i}	HIOR-/HIOW- recovery time (min.)	-	-	-	70	25	25	20
t_3	HIOW- data setup (min.)	60	45	30	30	20	20	15
t_4	HIOW- data hold (min.)	30	20	15	10	10	5	5
t_5	HIOR- data setup (min.)	50	35	20	20	20	15	10
t_6	HIOR- data hold (min.)	5	5	5	5	5	5	5

t_{6Z}	HIOR- data tri-state (max.)	30	30	30	30	30	20	20
t_7	Address valid to IOCS16-assertion (max.)	90	50	40	n/a	n/a	n/a	n/a
t_8	Address valid to IOCS16-released (max.)	60	45	30	n/a	n/a	n/a	n/a
t_9	HIOR-/HIOW- to address valid hold	20	15	10	10	10	10	10
t_{RD}	Read data valid to IORDY active (min.)	0	0	0	0	0	0	0
t_A	IORDY setup time	35	35	35	35	35	n/a	n/a
t_B	IORDY pulse width (max.)	1250	1250	1250	1250	1250	n/a	n/a
t_C	IORDY assertion to release (max.)	5	5	5	5	5	n/a	n/a

3.11.2.8 True IDE Multiword DMA Mode Read/Write Timing Specification

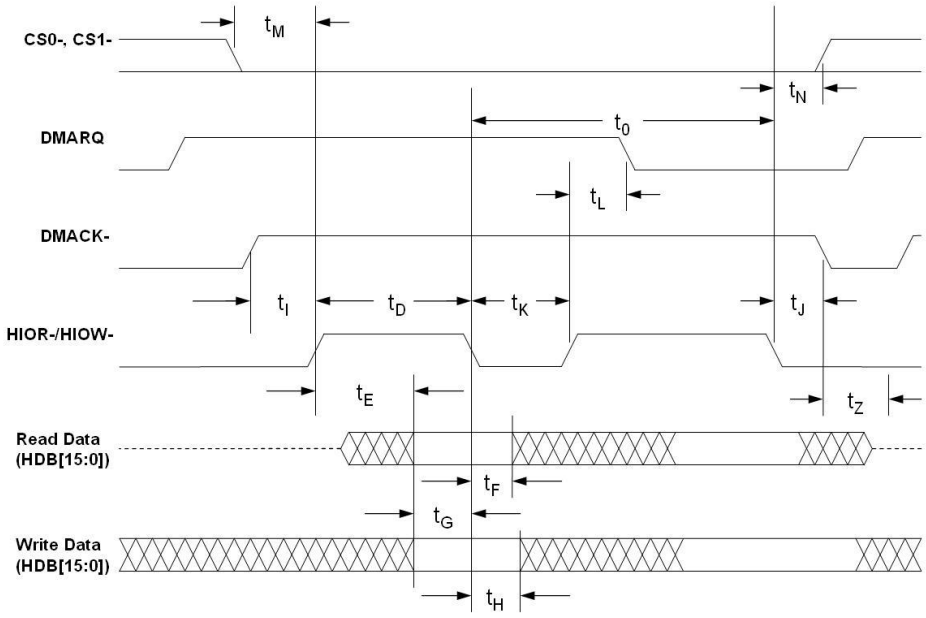

Figure 10 Read/Write Timing Diagram, Multiword DMA Mode

Table 12: Read/Write Timing Specifications, Multiword DMA Mode 0-4

Multiword DMA timing parameters		**Mode 0**	**Mode 1**	**Mode 2**	**Mode 3**	**Mode 4**
t_0	Cycle time (min.)	480	150	120	100	80
t_D	HIOR-/HIOW- assertion width (min.)	215	80	70	65	55
t_E	HIOR- data access (max.)	150	60	50	50	45
t_F	HIOR- data hold (min.)	5	5	5	5	5
t_G	HIOR-/HIOW- data setup (min.)	100	30	20	15	10
t_H	HIOW- data hold (min.)	20	15	10	5	5
t_I	DMACK to HIOR-/HIOW- setup (min.)	0	0	0	0	0
t_J	HIOR-/HIOW- to DMACK hold (min.)	20	5	5	5	5
t_{KR}	HIOR- negated width (min.)	50	50	25	25	20
t_{KW}	HIOW- negated width (min.)	215	50	25	25	20
t_{LR}	HIOR- to DMARQ delay (max.)	120	40	35	35	35
t_{LW}	HIOW- to DMARQ delay (max.)	40	40	35	35	35
t_M	CS1-, CS0- valid to HIOR-/HIOW-	50	30	25	10	5
t_N	CS1-, CS0- hold	15	10	10	10	10
t_Z	DMACK-	20	25	25	25	25

3.11.2.9 True IDE Ultra DMA Mode Read/Write Timing Specification

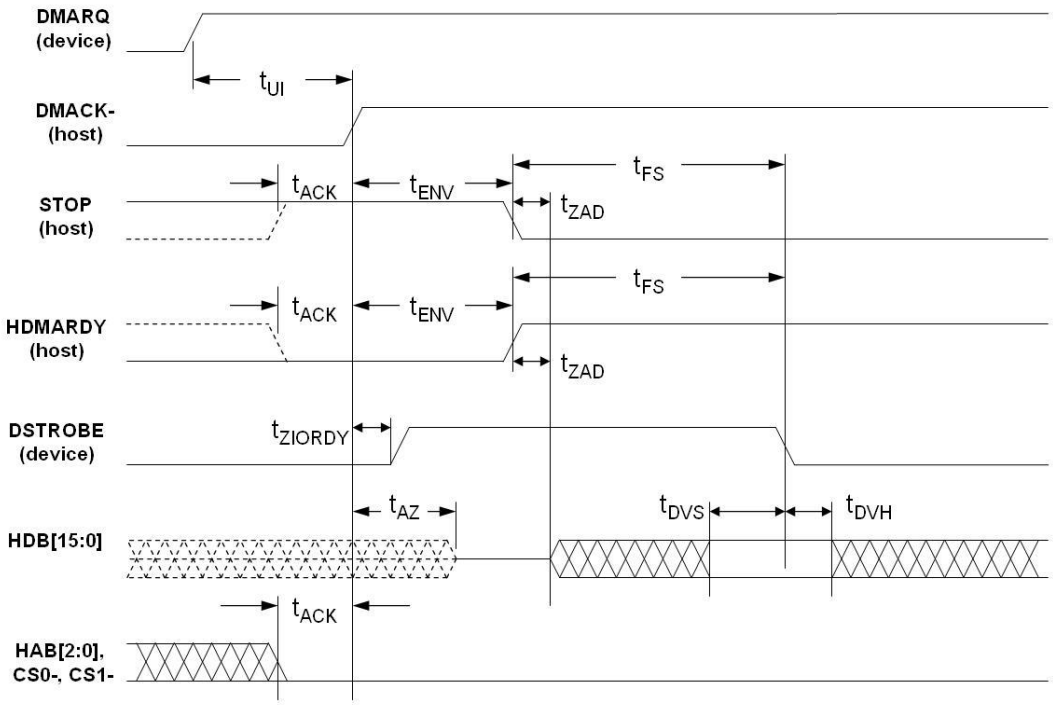

Figure 11 Ultra DMA Mode Data-in Burst Initiation Timing Diagram

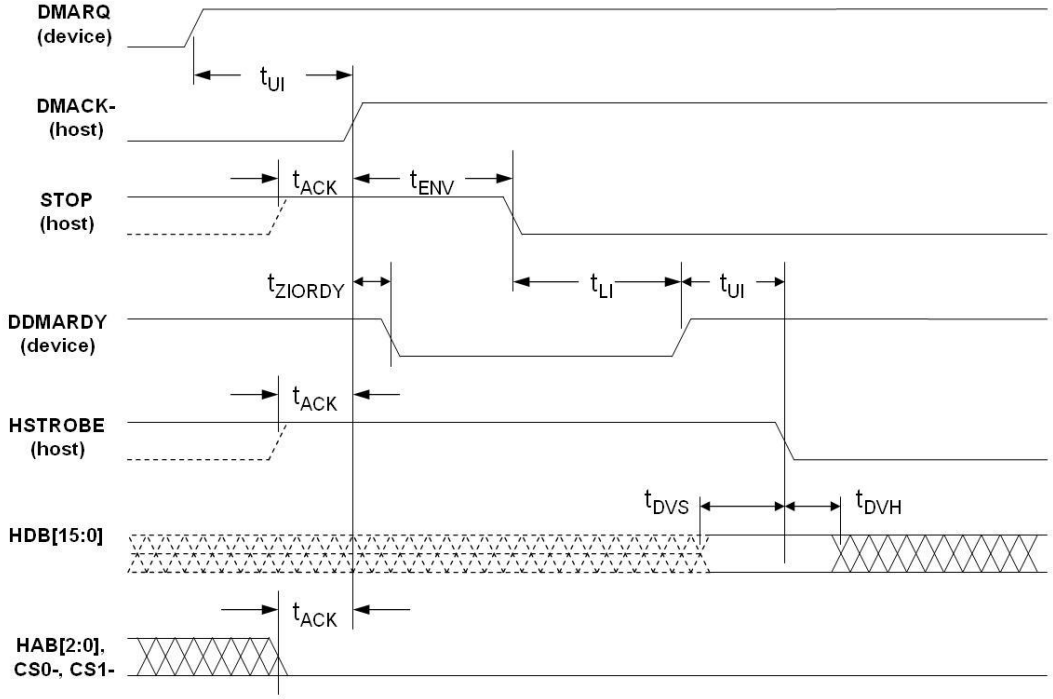

Figure 12 Ultra DMA Mode Data-out Burst Initiation Timing Diagram

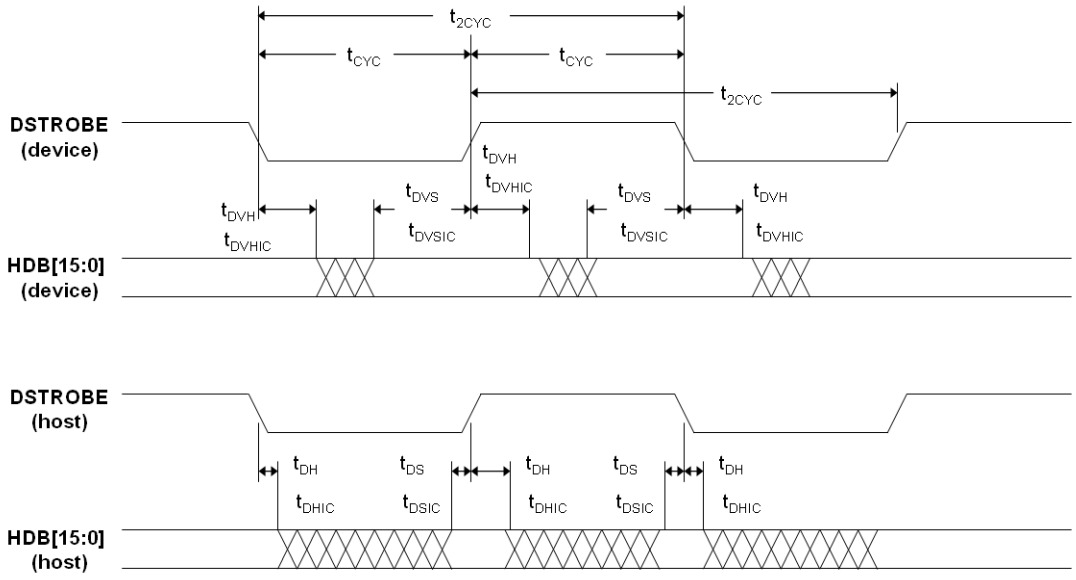

Figure 13 Sustained Ultra DMA Mode Data-in Burst Timing Diagram

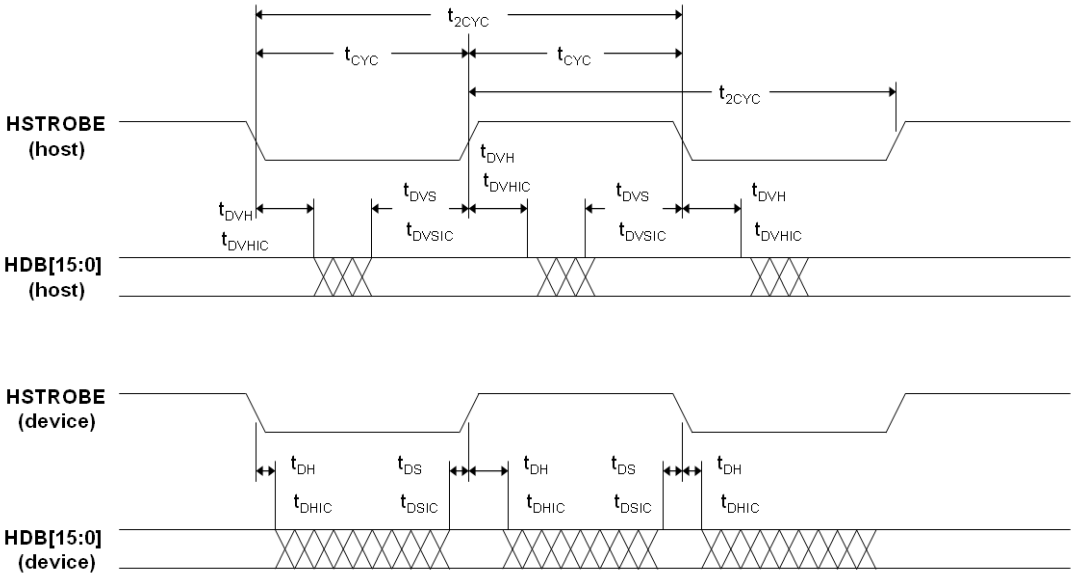

Figure 14 Sustained Ultra DMA Mode Data-out Burst Timing Diagram

Table 13: Timing Diagram, Ultra DMA Mode 0-6

Ultra DMA timing parameters		Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Mode 6	
		Min.	Max.	Min.	Max.	Min.	Min.	Max.	Min.	Max.	Max.	Max.	Min.	Max.	Max.
t_{2CYC}	Typical sustained average two cycle time	240	-	160	-	90	-	60	-	60	-	40	-	30	-

t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	112	-	73	-	39	-	25	-	25	-	16.8	-	13	-
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	230	-	153	-	86	-	57	-	57	-	38	-	29	-
t_{DS}	Data setup time (at recipient)	15	-	10	-	7	-	5	-	5	-	4	-	2.6	-
t_{DH}	Data hold time (at recipient)	5	-	5	-	5	-	5	-	5	-	4.6	-	3.5	-
t_{DVS}	Data valid setup time at sender (from data bus being valid until STROBE edge)	70	-	48	-	20	-	6.7	-	6.7	-	4.8	-	4	-
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	6.2	-	6.2	-	6.2	-	6.2	-	6.2	-	4.8	-	4	-
t_{LI}	Limited interlock time	0	150	0	150	0	100	0	100	0	100	0	75	0	60
t_{MLI}	Interlock time with minimum	20	-	20	-	20	-	20	-	20	-	20	-	20	-
t_{UI}	Unlimited interlock time	0	-	0	-	0	-	0	-	0	-	0	-	0	-
t_{AZ}	Maximum time allowed for output drivers to release (from being asserted or negated)	-	10	-	10	-	10	-	10	-	10	-	10	-	10
t_{ZAH}	Minimum delay time	20	-	20	-	20	-	20	-	20	-	20	-	20	-
t_{ZAD}	required for output	0	-	0	-	0	-	0	-	0	-	0	-	0	-

	drivers to assert or negate (from released state)														
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data out burst initiation)	20	70	20	70	20	55	20	55	20	55	20	50	20	50
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)	-	75	-	70	-	60	-	60	-	60	-	50	-	50
t_{RP}	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY-)	160	-	125	-	100	-	100	-	100	-	85	-	85	-
t_{IORDYZ}	Pull-up time before allowing IORDY to be released	-	20	-	20	-	20	-	20	-	20	-	20	-	20
t_{ZIORDY}	Minimum time device shall wait before driving IORDY	0	-	0	-	0	-	0	-	0	-	0	-	0	-
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)	20	-	20	-	20	-	20	-	20	-	20	-	20	-
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	50		50	-	50	-	50	-	50	-	50	-	50	-
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	-	230	-	200	-	130	-	120	-	120	-	90	-	80

3.12 Transfer Function

3.12.1 I/O Transfer function

The I/O transfer to or from the iCF 1IE2 can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal –IOIS16 is asserted by the iCF 1IE2. Otherwise, the –IOIS16 signal is de-asserted. When a 16 bit transfer is attempted and the –IOIS16 signal is not asserted by the iCF 1IE2, the system shall generate a pair of 8 bit references to access the word's even byte and odd byte. The iCF 1IE2 permits both 8 and 16 bit accesses to all of its I/O addresses, so –IOIS 16 is asserted for add address to which the iCF 1IE2 responds. The iCF 1IE2 may request the host to extend the length of an input cycle until data ready by asserting the –WAIT signal at the start of the cycle.

Table 14*:* PCMCIA Mode I/O Function

Function Code	**-REG**	**-CE2**	**-CE1**	**A0**	**-IORD**	**-IOWR**	**D15~D8**	**D7~D0**
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Input Access (16bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8bits)	L	L	H	X	H	L	Odd-Byte	Don't Care

3.12.2 Common Memory Transfer Function

The Common Memory transfer to or from iCF 1IE2 can be either 8 or 16 bits. The iCF 1IE2 permits both 8 and 16 bits access to all of its Common Memory addresses. The iCF 1IE2 request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the –WAIT signal at the start of the cycle.

Table 15: Common Memory Function

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15~D8	D7~D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Read Access (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Input Access (16bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Output Access (16bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8bits)	H	L	H	X	H	L	Odd-Byte	Don't Care

3.12.3 True IDE Mode I/O Transfer Function

The iCF 1IE2 can be configured in a True IDE Mode of operation. The iCF 1IE2 is configured in this mode only when –OE input signal is grounded by the host during the power off to power on cycle.

Table 16: True IDE Mode I/O Function

Function Code	-CS1	-CS0	-A0~A2	-DMACK	-IORD	-IOWR	D15~D8	D7~D0
Invalid Mode	L	L	X	X	X	X	Undefined In/Out	Undefined In/Out
	L	X	X	L	L	X	Undefined Out	Undefined Out
	L	X	X	L	X	L	Undefined In	Undefined In
	X	L	X	L	L	X	Undefined Out	Undefined Out
	X	L	X	L	X	L	Undefined In	Undefined In
Standby Mode	H	H	X	H	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	H	L	H	High Z	Data In
PIO Data Register Write	H	L	0	H	H	L	Odd-Byte In	Even-Byte In
DMA Data Register Write	H	H	X	L	H	L	Odd-Byte In	Even-Byte In
Ultra DMA Data Register Write	H	H	X	L	See Note 1		Odd-Byte In	Even-Byte In
PIO Data Register Read	H	L	0	H	L	H	Odd-Byte Out	Even-Byte Out
DMA Data Register Read	H	H	X	L	L	H	Odd-Byte Out	Even-Byte Out
Ultra DMA Data Register Read	H	H	X	L	See Note 2		Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	H	L	H	High Z	Status Out
Drive Address	L	H	7h	H	L	H	High Z	Data Out

Note1: In Ultra DMA Data Register Write mode the signals –IORD, -IOWR and IORDY are redefined and used as follows: -IORD as HSTROBE, -IOWR as STOP and IORDY as –DDMARDY. Data transfers with each edge of HSTROBE.

Note2: In Ultra DMA Data Register Read mode the signals –IORD, -IOWR and IORDY are redefined and used as follows: -IORD as –HDMARDY H, -IOWR as STOP and IORDY as DSTROBE. Data transfer with each edge of DSTROBE.

3.13 Configuration Register

3.13.1 Configuration Option Register (200h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the iCF 1IE2.

Table 17: Configuration Option Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevelREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Table 18: Information for Configuration Option Register

Name	Description
SRSET	Soft Reset: Setting this bit to one (1), waiting the minimum reset time and returning to zero(0) places the iCF 1IE2 in the reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the iCF 1IE2 in the same un-configured, Reset state as following power-up and hardware reset. This bit is PCMCIA Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.
LevelREQ	This bit is set to one (1) then Level Mode Interrupt is selected, and zero (0) then Pulse Mode is selected. Set to zero (0) by Reset.
Conf5-0	Configuration Index: Set to zero (0) by reset. It is used to select operation mode of the iCF 1IE2 as shown below

Note: Conf5 and Conf4 are reserved for CompactFlash Storage cards and shall be written as zero(0).

Table 19:iCF 1IE2 Configuration

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary
0	0	0	0	1	0	Primary I/O Mapped, 1F0h~1F7h/3F6h ~ 3F7h
0	0	0	0	1	1	Secondary I/O Mapped, 170h~177h/376h ~ 377h

3.13.2 Card Configuration and Status Register (202h in Attribute Memory)

The Card configuration and Status Register contains information about the Card's condition.

Table 20: Card Configuration and Status Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PweDwn	0	0

Table 21: Information for Card Configuration and Status Register

Name	Description
Changed	Indicates that one or both of the Pin Replacement register CReady. Or CWProt bits are set to one(1). When the changed bit is set. –STSCHG Pin 46 us held low if the SigChg bit is a One(1) and the iCF 1IE2 is configured for I/O interface.
SigChg	This bit is set and reset by the host to enable and disable a state-change "single" from the Status Register, the Changed bit controls pin 46, the Changed Status single. If no state change single is descried, this bit is set to zero(0) and pin46 (-STSCHG) single is then held high while the iCF 1IE2 is configured for I/O.
IOis8	The host sets this bit to one (1) if the iCF 1IE2 is to be configured in an 8 bit I/O Mode. The iCF 1IE2 is always configured for both 8 and 16 bit I/O, so this bit is ignored.
PwrDwn	This bit indicates whether the host requests iCF 1IE2 to be in the power saving or active mode. When the bit is one (1), the iCF 1IE2 enter a power down mode. The PwrDwn is zero (0), the host is requesting the iCF 1IE2 to enter the active mode. The PCMCIA

	READY value becomes false (busy) when this bit is changed. READY shall not become true (ready) until the power state requested has been entered. The iCF 1IE2 automatically powers down when it is idle and powers back up when it receives a command.
Int	This bit represents the internal state of the interrupt request. This value is available whether or not the I/O interface has been configured. This signal remains true until the condition that caused the interrupt request has been serviced. If interrupts are disabled by the –IEN bit in the Device Control Register, this bit is a zero (0).

3.13.3 Pin Replacement register (204h in Attribute Memory)

Table 22: Pin Replacement Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CReady	0	1	1	RReady	0
Write	0	0	CReady	0	0	0	MReady	0

Table 23: Information for Pin Replacement Register

Name	Description
CReady	This bit is set to one (1) when the bit RReady changes state. This bit can also be written by the host.
RReady	This bit is used to determine the internal state of the READY signal. This bit may be used to determine the state of the READY signal as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask(MReady) for writing the corresponding bit CReady.
MReady	This bit acts as a mask for writing corresponding bit CReady.

3.13.4 Socket and Copy Register (206h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register. This register is used for identification of the card from the other card.

Table 24: Socket and Copy Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	0	Obsolete (Drive #)	0	0	0	0

Write	0	0	0	Obsolete (Drive #)	X	X	X	X

Table 25: Information for Socket and Copy Register

Name	Description
Obsolete(Drive #)	This bit is obsolete and should be written as 0.

3.14 Software Interface

3.14.1 CF-ATA Drive Register Set Definition and Protocol

The iCF 1IE2 can be configured as a high performance I/O device through:

a) The standard PC-AT disk I/O address 1F0h-1F7h, 3F6h-3F7h (primary) or 170h-177h, 376h-377h (secondary) with IRQ14 (or other available IRQ).

b) Any system decodes 16 byte I/O block using any available IRQ.

c) Memory space

The communication to or from the card is done using the Task File register, which provide all the necessary register for control and status information related to the storage medium. The PCMCIA interface connects peripherals to the host using four register mapping methods.

Table 26: I/O Configuration

Standard Configurations			
Config Index	I/O or Memory	Address	Description
0	Memory	0h-Fh, 400h-7FFh	Memory Mapped
1	I/O	XX0h-XXFh	I/O Mapped 16 Contiguous Registers
2	I/O	1F0h-1F7h, 3F6h-3F7h	Primary I/O Mapped
3	I/O	170h-177h, 376h-377h	Secondary I/O Mapped

3.14.2 I/O Primary and Secondary Address Configurations

Table 27: Primary and Secondary I/O Decoding

-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Note

0	1F(17)h	0	0	0	0	Even RD Data	Even WR Data	1,2
0	1F(17)h	0	0	0	1	Error Register	Features	1,2
0	1F(17)h	0	0	1	0	Sector Count	Sector Count	
0	1F(17)h	0	0	1	1	Sector No.	Sector No.	
0	1F(17)h	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)h	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)h	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)h	0	1	1	1	Status	Command	
0	3F(37)h	0	1	1	0	Alt Status	Device Control	
0	3F(37)h	0	1	1	1	Drive Address	Reserved	

Note 1) Register 0 is accessed with –CE1 low and –CE2 low (and A0=Don't care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte access to the offset 0 with –CE1 low and –CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers, which lie at offset 1. When accessed twice as byte register with –CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

Note2) A byte access to register 0 with –CE1 high and –CE2 low access the error (read) or feature (write) register.

3.14.3 Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the card, the registers are accessed in the block of I/O space decoded by the system as follows:

Table 28: Contiguous I/O Decoding

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Note
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card/Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Feature	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

Note 1) Register 0 is accessed with –CE1 low and –CE2 low (and A0=Don't care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte access to the offset 0 with –CE1 low and –CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with –CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

Note 2) A byte access to register 0 with –CE1 high and –CE2 low access the error (read) or feature (write) register.

Note 3) Address lines that are not indicated are ignored by the card for accessing all the registers in this table.

3.14.4 Memory Mapped Addressing

When the card registers are accessed via memory references, the register appears in the common memory space window: 0-2K bytes as follows:

Table 29: Memory Mapped Decoding

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Note
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1,2
1	0	X	0	0	0	1	1	Error	Features	1,2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Feature	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd Rd Data	Odd WR Data	3

Note 1) Register 0 is accessed with –CE1 low and –CE2 low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte access to the offset 0 with –CE1 low and –CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with –CE1 low, the first byte

to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte accesses to register 0 with –CE1 high and –CE2 low access the error (read) or feature (write) register.

Note 2) Register at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the register is byte accessed in the order 9 then 8 the data shall be transferred odd byte then even byte. Repeated byte accessed to register 8 or 0 shall access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 shall access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to register 8 then 9 shall access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

Note 3) Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 K byte memory window to the data register is provide so that hosts can perform memory block moves to the data register when the register lies in memory space.
Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction, Some PCMCIA socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently. Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the card. A word access to address at offset 8 shall provide even data on the low-order byte of the data bus, along with odd data at offset 9 on the high-order byte of the bus.

3.14.5 True IDE Mode Addressing

When the iCF 1IE2 is configured in the True IDE mode, the I/O decoding is as follows:

Table 30: True IDE Mode I/O Decoding

-CS1	-CS0	A2	A1	A0	-DMACK	-IORD=0	-IOWR=0	Note
1	0	0	0	0	1	PIO RD Data	PIO WR Data	8 or 16 bit
1	1	X	X	X	0	DMA RD Data	DMA WR Data	16 bit
1	0	0	0	1	1	Error Register	Features	8 bit
1	0	0	1	0	1	Sector Count	Sector Count	8 bit
1	0	0	1	1	1	Sector No.	Sector No.	8 bit
1	0	1	0	0	1	Cylinder Low	Cylinder Low	8 bit
1	0	1	0	1	1	Cylinder High	Cylinder High	8 bit
1	0	1	1	0	1	Select Card/Head	Select Card/Head	8 bit
1	1	1	1	1	1	Status	Command	8 bit

0	1	1	1	0	1	Alt Status	Device Control	8 bit

3.14.6 CF-ATA Register

The following section describes the hardware registers used by the host software to issue commands to the iCF 1IE2.

Note:

In accordance with the PCMCIA specification: each of the registers below that is located at an odd offset address may be accessed in the PC Card Memory or PC Card I/O modes at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when –CE1 is high and –CE2 is low unless –IOIS16 is high (not asserted by the card) and an I/O cycle us being performed.

In True IDE Mode of operation, the size of the transfer is based solely on the register being addressed. All registers are 8 bit only except for the Data Register, which is normally 16 bits, but can be programmed to use 8 bit transfers for Non-DMA operations through the use of the Set Features command. The data register is also 8 bits during a portion of the Read Long and Write Long commands, which exist solely for historical reasons and should not be used.

3.14.6.1 Data Register

The Data Register is a 16bits register, and it is used to transfer data blocks between the card and the host. This register overlaps the Error Register. This register can be accessed in word and byte mode.

Table 31: Data Register

Data Register															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

3.14.6.2 Error Register

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

Table 32: Error Register

BBK	UNC	0	IDNF	0	ABRT	0	AMNF
D7	D6	D5	D4	D3	D2	D1	D0

3.14.6.3 Feature Register

This register provides information regarding features of the card that the host can utilize. This register is also accessed in PC Card modes on data D15-D8 during a write operation to Offset 0 with –CE2 low and –CE1 high.

Table 33: Feature Register

Feature Register							
D7	D6	D5	D4	D3	D2	D1	D0

3.14.6.4 Sector Count Register

This registers the number of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

Table 34: Sector Count Register

Sector Count Register							
D7	D6	D5	D4	D3	D2	D1	D0

3.14.6.5 Sector Number Register

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for iCF 1IE2 data access for the subsequent command.

Table 35: Sector Number Register

Sector Number Register							
D7	D6	D5	D4	D3	D2	D1	D0

3.14.6.6 Cylinder Low Register

This Register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

Table 36: Cylinder Low Register

Cylinder Low Register							
D7	D6	D5	D4	D3	D2	D1	D0

3.14.6.7 Cylinder High Register

This Register contains the high order 8 bits of the starting cylinder address or bits 23-16

of the Logical Block Address.

Table 37: Cylinder High Register

Cylinder High Register							
D7	D6	D5	D4	D3	D2	D1	D0

3.14.6.8 Device/Head Register

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing.

Table 38: Device/Head Register

1	LBA	1	DRV	HS3	HS2	HS1	HS0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: this bit is set 1.

Bit6: LBA is a flag to select either Cylinder/Head/Sector or Logical Block Address mode. When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected.

Bit5: this bit is set 1.

Bit4: DRV is the drive number. When DRV=0, drive (card) 0 is selected. When DRV=1, drive (card) 1 is selected. Setting this bit to1 is obsolete in PCMCIA modes of operation.

Bit3: When operation in the Cylinder/Head/Sector mode, this is bit 3 of the head number. It is bit 27 in the Logical Block Address mode.

Bit2: When operation in the Cylinder/Head/Sector mode, this is bit 2 of the head number. It is bit 26 in the Logical Block Address mode.

Bit1: When operation in the Cylinder/Head/Sector mode, this is bit 1 of the head number. It is bit 25 in the Logical Block Address mode.

Bit0: When operation in the Cylinder/Head/Sector mode, this is bit 0 of the head number. It is bit 24 in the Logical Block Address mode.

3.14.6.9 Status Register

These registers return the iCF 1IE2 status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not.

Table 39: Status Register

BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: the busy bit is set when the iCF 1IE2 has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit set to a 1.
Bit6: RDY indicates whether the device is capable of performing iCF 1IE2 operations. This bit is cleared at power up and remains cleared until the card is ready to accept a command.
Bit5: This bit, if set, indicates a write fault has occurred.
Bit4: This bit is set when the iCF 1IE2 is ready.
Bit3: The Data Request is set when the iCF 1IE2 requires that information be transferred either to or from the host through the Data register.
During the data transfer of DMA commands, the card shall not asserted DMARD unless either the BUST bit, the DRQ, or both are set to one.
Bit2: This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.
Bit1: This bit is always to 0.
Bit0: This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information description the error.

3.14.6.10 Device Control Register

This register is used to control the iCF 1IE2 interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY.

Table 40: Device Control Register

X	X	X	X	X	SW Rst	-IEn	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7-3: These bits are ignored.
Bit2: This bit is set to 1 in order to force the iCF 1IE2 to perform a Soft Reset operation. This does not change PCMCIA Card Configuration Register as a hardware Reset does. The Card remains in Reset until this bit is reset to '0'.
Bit1: the Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupt from the iCF 1IE2 are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset.
Bit0: This bit is ignored.

3.14.6.11 Drive Address Register

This register is provide for compatibility with the AT disk drive interface.

Table 41: Drive Address Register

X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: this bit is unknown.

Bit6: this bit is – when a write operation is in progress; otherwise, it is 1.

Bit5: this bit is the negation of bit 3 in the Drive/Head register.

Bit4: this bit is the negation of bit 2 in the Drive/Head register.

Bit3: this bit is the negation of bit 1 in the Drive/Head register.

Bit2: this bit is the negation of bit 0 in the Drive/Head register.

Bit1: this bit is 0 when drive 1 is active and selected.

Bit0: this bit is 0 when the drive 0 is active and selected.

3.15 Hardware Reset (Only for Memory Card mode and I/O Card Mode)

Table 42: Timing Diagram, Hardware Reset

	Item	Min.	Max.	Normal	Unit
t_{SU}(RESET)	Reset Setup Time	20	-	-	ms
t_{REC}(VCC)	-CE Recover Time	1	-	-	us
t_{PR}	VCC rising up time	0.1	100	-	ms
t_{PF}	VCC falling down time	3	300	-	ms
t_{W}(RESET)	Reset pulse width	10	-	-	ms
t_{H}(Hi-ZRESET)		0	-	-	
t_{S}(Hi-ZRESET)		0	-	-	

Hardware Reset Timing

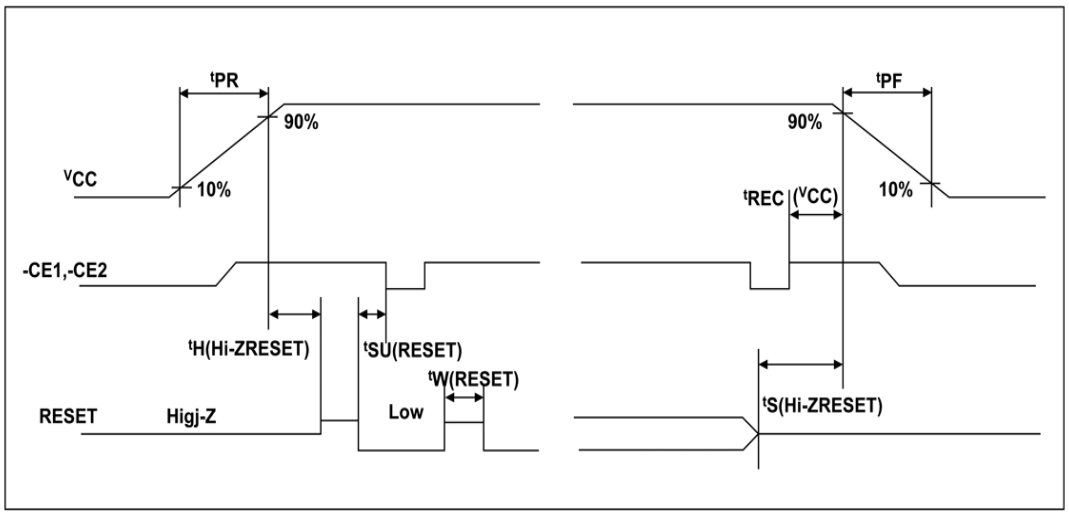

Figure 15 Timing Diagram, Hardware Reset

Note: It shows the electric character of our controller. It is irrelevant to power supply or prevention from sudden power loss protection.

3.16 Power On Reset

(1) When the VCC power reaches to 2.7V, the disk drive will be reset.

Table 43: Timing Diagram, Power On Reset

	Item	Min.	Max.	Normal	Unit	Note
t_{SU}(RESET)	-CE Setup Time	20	-	-	ms	
t_{PR}	-VCC Rising Up Time		100	-	ms	

Power on Reset Timing

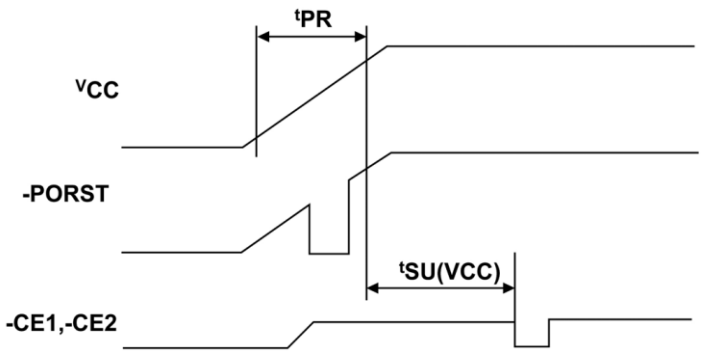

Figure 16 Timing Diagram, Power On Reset

(2) Each timing specification is shown as Table 44.

Table 44: Timing specification for each mode

Timing	Mode	mini	Max.	Note
tBSY_PORST	PC Card	5ms	500ms	
	True IDE	5ms	500ms	Slave configuration
		400ms	1 second	Master without slave device
		5ms	32 seconds	Master with slave device

3.17 Supported IDE Commands

iCF 1IE2 supports the commands listed in Table 45.

Table 45: IDE Commands

Class	Command	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	98H or E5H	-	-	-	-	D	-
1	Execute Device Diagnostic	90H	-	-	-	-	D	-
1	Erase Sector(s)	C0H	-	Y	Y	Y	Y	Y
2	Format Track	50H	-	Y	-	Y	Y	Y
1	Identify Device	ECH	-	-	-	-	D	-
1	Idle	97H or E3H	-	Y	-	-	D	-

1	Idle immediate	95H or E1H	-	-	-	-	D	-
1	Initialize Device Parameters	91H	-	Y	-	-	Y	-
1	Read Buffer	E4H	-	-	-	-	D	-
1	Read DMA	C8H	-	Y	Y	Y	Y	Y
1	Read Long Sector	22H or 23H	-	-	Y	Y	Y	Y
1	Read Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
1	Recalibrate	1XH	-	-	-	-	D	-
1	Request Sense	03H	-	-	-	-	D	-
1	Seek	7XH	-	-	Y	Y	Y	Y
1	Set Features	EFH	Y	-	-	-	D	-
1	Set Sleep Mode	99H or E6H	-	-	-	-	D	-
1	Standby	96H or E2H	-	-	-	-	D	-
1	Standby Immediate	94H or E0H	-	-	-	-	D	-
2	Write Buffer	E8H	-	-	-	-	D	-
2	Write DMA	CAH	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
2	Write Sector(s) without Erase	38H	-	Y	Y	Y	Y	Y

Defines:

FR: Feature Register

SC: Sector Count Register

SN: Sector Number Register

CY: Cylinder Registers

DH: Card/Device/Head Register

LBA: LBA Block Address Mode Supported

Y: The register contains a valid parameter for this command. For Card/Device/Head Register Y means both the CompactFlash Storage Card and head parameter are used; D – only the CompactFlash Storage Card parameter is valid and not the head parameter; C –

The register contains command specific data (see command description for use).

3.17.1 Check power mode – 98H or E5H

Register	7	6	5	4	3	2	1	0
Command(7)	98h or E5h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command checks the power mode:

If the CompactFlash Storage is in, going to, or recovering from the sleep mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt.

If the compactFlash Storage Card is in idle mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

3.17.2 Execute Device Diagnostic – 90H

Register	7	6	5	4	3	2	1	0
Command(7)	90h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command performs the internal diagnostic tests implemented by the CompactFlash Storage Card. When the diagnostic command is issued in a PCMCIA configuration mode, this command runs only on the CompactFlash Storage Card that is addressed by the Drive/Head register. This is because PCMCIA card interface does not allow for direct inter-drive communication (such as the ATA PDIAG and DASP signals). When the diagnostic command is issued in the True IDE Mode, the Drive bit is ignored and the diagnostic command is

executed by both the Master and the Slave with the Master responding with status for both devices. The Diagnostic codes are shown in Table 48. Diagnostic Codes are returned in the Error Register at the end of the command.

Table 46: Diagnostic

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controller Microprocessor Error
8Xh	Slave Error in True IDE Mode

3.17.3 Erase Sector(s) – C0H

Register	7	6	5	4	3	2	1	0
Command(7)	C0h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

3.17.4 Format Track – 50H

Register	7	6	5	4	3	2	1	0
Command(7)	50h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	X (LBA 7-0)							

Sector Count(2)	Count(LBA mode only)
Feature(1)	X

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the CompactFlash Storage Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the CompactFlash Storage Card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

3.17.5 Identify Device – ECH

Register	7	6	5	4	3	2	1	0
Command(7)	ECh							
C/D/H(6)	X	X	X	Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

The Identify Device command enables the host to receive parameter information from the CompactFlash Storage Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 49. All reserved bits or words are zero. Hosts should not depend in Obsolete words in Identify Device containing 0. Table 45 specifies each filed in the data returned by the Identify Device Command. In Table 45, X indicates a numeric nibble vale specific to the card and aaaa indicates an ASCII string specific to the particular drive.

Table 47: IDENTIFY DEVICE information

Word	Description	Value
0	General Configuration Bit 15 0=ATA device Bit 14:8 Retired Bit 7:6 Obsolete Bit 5:3 Retired Bit 2 Response incomplete Bit 1 Retired	848Ah

	Bit 0 reserved	
1	Number of logical cylinders	XXXXh
2	Specific configuration	0000h
3	Number of logical heads	0010h
4-5	Retired	0000h 0200h
6	Number of logical sectors per logical track	00XXh
7-8	Number of sectors per card	XXXXh
9	Retired	0000h
10-19	Serial number in 20 ASCII	Aaaa
20-21	Retired	0002h 0001h
22	Obsolete	0004h
23-26	Firmware revision in 8 ASCII	Aaaa
27-46	Model number in 40 ASCII	Aaaa
47	15-8: 80 7-0: 00h Reserved 01h-FFh: Maximum number of sectors that shall be transferred per DRQ data block on READ/WRITE Multiple commands	80 XXh
48	Trusted Computing feature set options 15 shall be cleared to zero 14 shall be set to one 13:1 Reserved for the Trusted Computing Group 0 0 = Trusted Computing feature set is not supported	0000h
49	Capabilities 15-14: Reserved for the IDENTIFY PACKET DEVICE command. 13: 1=Standby timer values as specified in this standard are supported 0:Standby timer values shall be managed by the device 12: Reserved for the IDENTIFY PACKET DEVICE command 11: 1=IORDY supported 0=IORDY may be disabled 10 1: IORDY may be disabled 9 1=LBA supported 8 1=DMA supported. 7-0 Retired	0F00h

50	Capabilities 15: Shell be cleared to zero 14: Shall be set to one 13:2 Reserved 1 Obsolete 0 0	0000h
51	PIO data transfer cycle timing mode	0200h
52	Obsolete	0000h
53	15 Free-fall control Sensitivity 00h: Vendor's recommended setting 7:3 Reserved 2: 1=the fields reported in word 88 are valid 1: 1=the fields reported in words (70:64) are valid 0: Obsolete	0007h
54	Number of current logical cylinders	XXXXh
55	Number of current logical heads	XXXXh
56	Number of current logical sectors per logical track	XXXXh
57-58	Current capacity in sectors	XXXXh
59	15:9 Reserved 8 0:Multiple sector setting is invalid 7:0 Current setting for number of logical sectors that shall be transferred per DRQ data block on READ/WRITE Multi commands	01XXh
60-61	Total number of user address sectors(DWord)	XXXXXXXXh
62	Obsolete	0000h
63	Multi-word DMA transfer(Not support)	0007h
64	15-8 Reserved 7-0 PIO modes supported	0003h
65	Minimum Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds In PCMCIA mode this value shall be 0h	0078h
66	Manufacturer's recommended Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds In PCMCIA mode this value shall be 0h	0078h
67	Minimum PIO transfer cycle time without flow control 15-0 Cycle time in nanoseconds	0078h
68	Minimum PIO transfer cycle time with IORDY flow control	0078h

	15-0 Cycle time in nanoseconds	
69-74	Reserved	0000h
75	No DMA QUEUED command supports	0000h
76	Serial ATA Capabilities 15:11 Reserved for Serial ATA 10 1= Supports Phy Event Counters 9 1= Supports receipt of host initiated power management Requests 8 0= No Support native Command Queuing 7:3 Reserved for future SATA signaling speed grades 2 1=Supports SATA Gen2 Signaling Speed (3.0Gb/s) 1 1=Support SATA Gen1 Signaling Speed (1.5Gb/s) 0 Shall be cleared to zero	0000h
77	Reserved for Serial ATA	0000h
78	Serial ATA features supported 15:7 Reserved for Serial ATA 6 0=Device not supports Software Settings Preservation 5 Reserved for Serial ATA 4 0= Device not supports in-order data delivery 3 0= Device not supports initiating power management 2 0= Device not supports DMA Setup auto-activation 1 0= Device not supports non-zero buffer offsets 0 Shall be cleared to zero	0000h
79	Serial ATA feature enabled 15:7 Reserved for Serial ATA 6 0=Software Settings Preservation not enabled 5 0=Reserved for Serial ATA 4 0= In-order data delivery not enabled 3 0= Device initiated power management not enabled 2 0= DMA setup auto-activation not enabled 1 0= Non-zero buffer offsets not enabled 0 Shall be cleared to zero	0000h
80-81	ATA Version support (ATA5)	0020 0000h
82	Command and feature sets supported 15 0 = Obsolete 14 0 = NOP Command not supported	7008h

	13 0 = READ BUFFER Command not supported 12 0 = WRITE BUFFER Command not supported 11 0 = Obsolete 10 0 = Host Protected Area Feature Set not supported 9 0 = DEVICE RESET Command not supported 8 0 = SERVICE Interrupt not supported 7 0 = RELEASE Interrupt not supported 6 1 = Look-ahead supported 5 1 = Write Cache supported 4 0 = indicate that the PACKET feature set is not supported 3 1 = mandatory Power Management Feature Set supported 2 0 = Obsolete 1 0 = Security Mode Feature Set not supported 0 1 = SMART Feature Set supported	
83	Command and feature sets supported 15 Shall be cleared to zero 14 Shall be set to one 13 0 = FLUSH CACHE EXT Command not supported 12 1 = mandatory FLUSH CACHE Command supported 11 0 = Device Configuration Overlay feature set not supported 10 0 = 48-Bit Address feature set not supported 9 0 = Automatic Acoustic Management feature set not supported 8 0 = SET MAX security extension not supported 7 0 = See Address Offset Reserved Area Boot, INCITS TR27:2001 6 0 = SET FEATURES subcommand not required to spin-up after power-up 5 0 = Power-Up in Standby feature set supported 4 0 = Removable Media Status Notification feature set not supported 3 0 = Advanced Power Management feature set not supported 2 0 = CFA feature set not supported 1 0 = READ/WRITE DMA QUEUED not supported	5004h

	0 1 = DOWNLOAD MICROCODE Command supported	
84	Command Set/Feature Supported Extension 15 Shall be cleared to zero 14 Shall be set to one 13-6 Reserved 5 0 = General Purpose Logging feature set not supported 4 reserved 3 0 = Media Card Pass Through Command feature set not supported 2 0 = Media Serial Number not supported 1 0 = SMART self-test not supported 0 1 = SMART Error Logging not supported	4000h
85	Command and feature sets supported or enabled 15 0 = Obsolete 14 0 = NOP Command not enabled 13 0 = READ BUFFER Command not enabled 12 0 = WRITE BUFFER Command not enabled 11 Obsolete 10 0 = Host Protected Area feature set not enabled 9 0 = DEVICE RESET Command not enabled 8 0 = SERVICE Interrupt not enabled 7 0 = RELEASE Interrupt not enabled 6 0 = Look-ahead not enabled 5 0 = Write Cache not enabled 4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported. 3 1 = Power Management Feature Set enabled 2 0 = Removable Media feature set not enabled 1 0 = Security Mode Feature Set not enabled 0 0 = SMART Feature Set not enabled	7008
86	Command set/feature enabled 15-14 0 = Reserved 13 0 = FLUSH CACHE EXT Command not supported 12 1 = FLUSH CACHE Command supported 11 0 = Device Configuration Overlay not supported 10 0 = 48-Bit Address features set not supported 9 0 = Automatic Acoustic Management feature set not	1004h

	enabled 8 0 = SET MAX security extension not enabled by SET MAX SETPASSWORD 7 0 = Reserved 6 0 = SET FEATURES subcommand required to spin-up after power-up not enabled 5 0 = Power-Up in Standby feature set not enabled 4 0 = Obsolete 3 1 = Advanced Power Management feature set enabled 2 0 = CFA feature set not supported 1 0 = READ/WRITE DMA QUEUED Command not supported 0 1 = DOWNLOAD MICROCODE Command supported	
87	Command and feature sets supported or enabled 15 Shall be cleared to zero 14 Shall be set to one 13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported 12 0 = Reserved for Technical Report, INCITS TR-37-2004 11 0 = Reserved for Technical Report, INCITS TR-37-2004 10:9 0 = Obsolete 8 0 = 64-Bit World Wide Name not supported 7 0 = WRITE DMA QUEUED FUA EXT Command not supported 6 0 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands not supported 5 0 = General Purpose Logging feature set not supported 4 0 = Obsolete 3 0 = Media Card Pass Through Command feature set not supported 2 0 = Media Serial Number is not valid 1 0 = SMART Self-Test not supported 0 0 = SMART Error-Logging not supported	4000h
88	Ultra DMA modes 15 Reserved	XX1Fh

	14 0 = Ultra DMA mode 6 is not supported 13 1= Ultra DMA mode 5 is selected 0= Ultra DMA mode 5 is not selected 12 1= Ultra DMA mode 4 is selected 0= Ultra DMA mode 4 is not selected 11 1= Ultra DMA mode 3 is selected 0= Ultra DMA mode 3 is not selected 10 1= Ultra DMA mode 2 is selected 0= Ultra DMA mode 2 is not selected 9 1= Ultra DMA mode 1 is selected 0= Ultra DMA mode 1 is not selected 8 1= Ultra DMA mode 0 is selected 0= Ultra DMA mode 0 is not selected 7 Reserved 6 0= Ultra DMA mode 6 is not supported 5 1= Ultra DMA mode 5 and below are supported 4 1= Ultra DMA mode 4 and below are supported 3 1= Ultra DMA mode 3 and below are supported 2 1= Ultra DMA mode 2 and below are supported 1 1= Ultra DMA mode 1 and below are supported 0 1= Ultra DMA mode 0 is supported	
89	Time required for Normal Erase mode SECURITY ERASE UNIT command	0000h
90	Time required for Enhanced erase mode SECURITY ERASE UNIT command	0000h
91	Current advanced power management level value	0000h
92	Master Password Identifier	0000h
93	Hardware reset result	404Fh
94	Current automatic acoustic management value 15:8 Vendor's recommended acoustic management value. 7:0 Current automatic acoustic management value.	0000h
95-126	Reserved	0000h
127	Obsolete	0000h
128	Security Status 15:9 Reserved 8 Security level 0 = high, 1 = Maximum 7:6 Reserved	XXXXh

	5 1= Enhanced security erase supported 4 1= Security count expired 3 0= Security frozen. 2 0 = Security not locked 1 0= Security not enabled 0 0= Security not supported	
129-159	Vendor specific	XXXXh
160	CFA power mode 1	A064h
161-162	Reserved	0000h
163-164	Reserved	0012 001Bh
165-175	Reserved	0000h
176-205	Current media serial number	0000h
206-254	Reserved	0000h
255	Integrity word 15:8 Check Sum 7:0 Signature	XXXXh

3.17.6 Idle -97H or E3H

Register	7	6	5	4	3	2	1	0
Command(7)	97h or E3h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Timer Count (5 msec increments)							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

3.17.7 Idle immediate - 95H or E1H

Register	7	6	5	4	3	2	1	0
Command(7)	95h or E1h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt.

3.17.8 Initialize Device Parameters - 91H

Register	7	6	5	4	3	2	1	0
Command(7)	91h							
C/D/H(6)	X	O	X	Drive	Max Head (no. of heads-1)			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Number of sectors							
Feature(1)	X							

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Device/Head registers are used by this command.

3.17.9 Read Buffer - E4H

Register	7	6	5	4	3	2	1	0
Command(7)	E4h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							

Sector Count(2)	X
Feature(1)	X

The Read Buffer command enables the host to read the current contents of the CompactFlash Storage Card's sector buffer. This command has the same protocol as the Read Sector(s) command.

3.17.10 Read DMA - C8H

Register	7	6	5	4	3	2	1	0
Command(7)	C8							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16							
Cylinder Low(4)	Cylinder Low (LBA 15-8							
Sector Number(3)	Sector Numbe(LBA 7-0							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 request 256 sectors. The transfer begins at he sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, cleat BSY. The Card asserts DMAREQ while data is available to be transferred. The Card asserts DMAREQ while data is available to be transferred. The host then reads the (512 & sector –count) bytes of data from the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts –DMACK while it is ready to transfer data by DMA and asserts –IORD once for each 16 bit word to be transferred to the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder, head, and sector number of the sector where the occurred. The amount of data transferred is indeterminate.

When a Read DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

3.17.11 Read Long Sector - 22H or 23H

Register	7	6	5	4	3	2	1	0
Command(7)	22h or 23h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	X							
Feature(1)	X							

The Read Long command performs similarly to the Read Sector(s) command except that is returns 516 bytes of data instead of 512 bytes. During a Read Long command, the CompactFlash Storage Card does not check the ECC bytes to determine if there consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

3.17.12 Read Sector(s) - 20H or 21H

Register	7	6	5	4	3	2	1	0
Command(7)	20h or 21h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count Register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has buffer, sets DRQ, cleats BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder head, and sector number of the sector 2where the error occurred. The flawed data is pending in the sector buffer.

3.17.13 Read Verify Sector(s) - 40H or 41H

Register	7	6	5	4	3	2	1	0
Command(7)	40h or 41h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash Storage Card sets BSY. When the requested sectors have been verified, the CompactFlash Storage Card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified. If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

3.17.14 Recalibrate - 1XH

Register	7	6	5	4	3	2	1	0
Command(7)	1Xh							
C/D/H(6)	1	LBA	1	Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command is effectively a NOP command to the CompactFlash Storage Card and is provided for compatibility.

3.17.15 Request Sense - 03H

Register	7	6	5	4	3	2	1	0

Command(7)	03h							
C/D/H(6)	1	LBA	1	Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command requests extended error information for the previous command. Table46 defines the valid extended error codes for the CompactFlash Storage Card Series product. The extended error code is returned to the host in the Error Register.

Table 48: Extended Error Codes

Extended Error Code	Description
01h	Self Test OK
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address
2Fh	Address Overflow
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrected ECC Error
18h	Corrected ECC Error
05h,30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error/Aborted Command
0Ch, 38h,3Bh,3Ch,3Fh	Corrupted Media Format
03h	Write/ Erase Failed
22h	Power Level 1 Disabled

3.17.16 Seek - 7XH

Register	7	6	5	4	3	2	1	0

Command(7)	7Xh				
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)
Cylinder High(5)	Cylinder High (LBA 23-16)				
Cylinder Low(4)	Cylinder Low (LBA 15-8)				
Sector Number(3)	X (LBA 7-0)				
Sector Count(2)	X				
Feature(1)	X				

This command is effectively a NOP command to the CompactFlash Storage Card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

3.17.17 Set Features – EFH

Register	7	6	5	4	3	2	1	0
Command(7)	EFh							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Config							
Feature(1)	Feature							

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the CompactFlash Storage Card shall return command aborted. Table 51: Feature Supported defines all features that are supported.

Table 49: Feature Supported

Feature	Operation
02h	Enable Write Cache.
03h	Set transfer mode based on value in Sector Counter register.
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft reset.
82h	Disable Write cache.

9Ah	Set the host current source capability. Allows tradeoff between current drawn and read/write speed.
AAh	Enable Read Look Ahead.
BBh	4 Bytes of data apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded and execution is enabled for all subsequent Read Multiple and Write Multiple commands. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write multiple disabled.

3.17.18 Set Sleep Mode - 99H or E6H

Register	7	6	5	4	3	2	1	0
Command(7)	99h or E6h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds.

3.17.19 Standby - 96H or E2H

Register	7	6	5	4	3	2	1	0
Command(7)	96h or E2h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							

Sector Number(3)	X
Sector Count(2)	X
Feature(1)	X

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, cleat BSY and return interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

3.17.20 Standby Immediate - 94H or E0H

Register	7	6	5	4	3	2	1	0
Command(7)	94h or E0h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

3.17.21 Write Buffer - E8H

Register	7	6	5	4	3	2	1	0
Command(7)	E8h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

The Write Buffer command enables the host to overwrite contents of the CompactFlash Storage Card’s sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfer 512 bytes.

3.17.22 Write DMA – CAH

Register	7	6	5	4	3	2	1	0
Command(7)	CAh							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low(LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The host then writes the (512*sector count) bytes of data to the Card using DMA. While DMAREQ is asserted by the Card, the host asserts –DMACK while it is ready to transfer data by DMA and asserts –IOWR once for each 16 bit word to be transferred from the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecovertable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The amount of data transferred is indeterminate. When a write DMA command is received by the Card and 8bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

3.17.23 Write Sector(s) - 30H or 31H

Register	7	6	5	4	3	2	1	0
Command(7)	30h or 31h							
C/D/H(6)	1	LBA	1	Drive	Head(LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector	Sector Number (LBA 7-0)							

Number(3)	
Sector Count(2)	Sector Count
Feature(1)	X

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the CompactFlash Storage Card sets BST, then sets DRQ and clears BSDY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY shall be set and DRQ shall be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It shall remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

3.18 ATA S.M.A.R.T. Functionality

The iCF 1IE2 supports the following ATA SMART commands, determined by the Feature Register value.

Value	Command
D0h	SMART Read Data
D1h	SMART Read Attribute Thresholds
D2h	SMART Enable/Disable Attribute Autosave
D5h	SMART Read Log
D6h	SMART Write Log
D8h	SMART Enable Operations
D9h	SMART Disable Operations
DAh	SMART Return Status
E0h	SMART Read Remap Data
E1h	SMART Read Wear Level Data

SMART commands with Feature Register values not mentioned in the above table are not sup- ported, and will be aborted.

3.18.1 SMART Enable Operations

COMMAND CODE B0h with a Feature Register value of D8h

PROTOCOL Non-data command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS None required

ERROR OUTPUTS Aborted if the signature in the Cylinder registers is invalid.

DESCRIPTION This command enables access to the SMART capabilities of the firmware.

The state of SMART (enabled or disabled) is preserved across power cycles.

3.18.2 SMART Disable Operations

COMMAND CODE B0h with a Feature Register value of D9h

PROTOCOL 5Ah

INPUTS

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS None required

ERROR OUTPUTS Aborted if the signature in the Cylinder registers is invalid.

DESCRIPTION This command enables access to the SMART capabilities of the firmware.

The state of SMART (enabled or disabled) is preserved across power cycles.

3.18.3 SMART Enable/Disable Attribute Autosave

COMMAND CODE B0h with a Feature Register value of D2h

PROTOCOL 5Ah

INPUTS

Register	7	6	5	4	3	2	1	0
Features	D2h							
Sector Count	00h or F1h							
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS None required

ERROR OUTPUTS Aborted if the signature in the Cylinder registers is invalid.

DESCRIPTION This command enables access to the SMART capabilities of the firmware.

The state of SMART (enabled or disabled) is preserved across power cycles.

3.18.4 SMART Read Data

COMMAND CODE B0h with a Feature Register value of D0h

PROTOCOL PIO data in.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	D2h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS None required

ERROR OUTPUTS Aborted if the signature in the Cylinder registers is invalid.

DESCRIPTION This command enables access to the SMART capabilities of the firmware.

The state of SMART (enabled or disabled) is preserved across power cycles.

Offset	Value	Description
0..1	0010h	SMART structure version
2..361		Attribute entries 1 to 30 (12 bytes each)
362	00h	Off-line data collection status (no off-line data collection)
363	00h	Self-test execution status byte (self-test completed)
364..365	0000h	Total time to complete off-line data collection
366	00h	–
367	00h	Off-line data collection capability (no off-line data collection)
368..369	0003h	SMART capabilities
370	00h	Error logging capability (no error logging)
371	00h	–
372	00h	Short self-test routine recommended polling time
373	00h	Extended self-test routine recommended polling time
374..385	00h	Reserved
386..387	0004h	SMART Hyperstone Structure Version
388..391		Firmware “Commit” counter
392..395		Firmware Wear Level Threshold
396	01h	Global Wear Leveling active
397	01h	Global Bad Block Management active
398..401		Average Flash Block Erase Count
402..405		Number of Flash Blocks involved into the Wear Leveling
406..409		Number of total ECC errors during firmware initialization
410..413		Number of correctable ECC errors during firmware initialization
414..510	00h	–
511		Data structure checksum

Spare Block Count Attribute

This attribute gives information about the amount of available spare blocks.

Offset	Value	Description
0	196	Attribute ID – Reallocation Count
1..2	0003h	Flags – Pre-fail type, attribute value is updated during normal operation
3		Attribute value. The value returned here is the percentage of remaining spare blocks summed over all flash chips, i.e. (100 * current spare blocks / initial spare blocks)
4		Attribute value (worst value)
5..7		Sum of the initial number of spare blocks for all flash chips
8..10		Sum of the current number of spare blocks for all flash chips
11	00h	Reserved

This attribute is used for the SMART Return Status command. If the attribute value field is less than the spare block threshold, the SMART Return Status command will indicate a threshold exceeded condition.

Spare Block Count Worst Channel Attribute Threshold

This attribute gives information about the amount of available spare blocks on the interleave channel that has the lowest current number of spare blocks.

Offset	Value	Description
0	213	Attribute ID – Spare Block Count Worst Channel (vendor specific)
1..2	0003h	Flags – Pre-fail type, attribute value is updated during normal operation
3		Attribute value. The value returned here is from all interleaved channels the worst percentage of remaining spare blocks i.e. (100 * current spare blocks / initial spare blocks).
4		Attribute value (worst value)

5..7		Initial number of spare blocks of the interleave channel with the lowest current number of spare blocks
8..10		Current number of spare blocks of the interleave channel with the lowest current number of spare blocks
11	00h	Reserved

This attribute is used for the SMART Return Status command. If the attribute value field is less than the spare block threshold (currently fixed at 10, may be configurable in a future firmware version), the SMART Return Status command will indicate a threshold exceeded condition.

Erase Count Attribute

This attribute gives information about the amount of flash block erases that have been per- formed.

Offset	**Value**	**Description**
0	229	Attribute ID – Erase Count Usage (vendor specific)
1..2	000Xh	Flags – Pre-fail or Advisory type, attribute value is updated during nor- mal operation
3		Attribute value. The value returned here is an estimation of the remain- ing card life, in percent, based on the number of flash block erases compared to the target number of erase cycles per block.
4		Attribute value (worst value)
5..10		Estimated total number of block erases
11	00h	Reserved

This attribute is used for the SMART Return Status command. If the attribute value field is less than the erase count threshold, the SMART Return Status command will indicate a threshold exceeded condition.

The target number of erase cycles per flash block is taken from the MaxBlockEraseCount col- umn in the Device Description file.

The attribute type (pre-fail or advisory) can be set with the -features preformat option.

Total ECC Errors Attribute

This attribute gives information about the total number of ECC errors that have occurred on flash read commands during firmware runtime. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	203	Attribute ID – Number of ECC errors
1..2	0002h	Flags — Advisory type, attribute value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5..8		Total number of ECC errors (correctable and uncorrectable)
9..10		–
11	00h	Reserved

Total Number of Reads Attribute

This attribute gives information about the total number of sectors read from flash. This can be useful for the interpretation of the number of correctable or total ECC errors. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	232	Attribute ID – Number of Reads (vendor specific)
1..2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5..10		Total number of flash read commands
11	00h	Reserved

Power On Count Attribute

Offset	Value	Description
0	12	Attribute ID – Power On Count
1..2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5..8		Number of Power On cycles
9..10		–
11	00h	Reserved

Total LBAs Written Attribute

This attribute gives the total amount of data written to the disk, in units of 32MB (65536 sec- tors). This number can be converted to Terabytes written (TBW) by dividing the raw attribute value by 2^{15}.

Offset	Value	Description
0	241	Attribute ID – Total LBAs Written (vendor specific)
1..2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5..10		Total number of LBAs written to the disk, divided by 65536
11	00h	Reserved

Total LBAs Read Attribute

This attribute gives the total amount of data read from the disk, in units of 32MB (65536 sec- tors). This number can be converted to Terabytes read by dividing the raw attribute value by 215.

Offset	Value	Description
0	242	Attribute ID – Total LBAs Read (vendor specific)
1..2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5..10		Total number of LBAs read from the disk, divided by 65536
11	00h	Reserved

Anchor Block Status Attribute

This attribute reports how many times the Anchor block of the card has been re-written, either by the Anchor block repair routine, or by a firmware update.

Offset	Value	Description
0	214	Attribute ID – Anchor Block Status (vendor specific)
1..2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5..8		Anchor Block Write Count
9..10		–
11	00h	Reserved

Trim Status Attribute

This attribute reports the amount of device content that is currently in the trimmed state (as percentage).

Offset	Value	Description
0	215	Attribute ID – Trim Status (vendor specific)
1..2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3		Attribute value
4		Attribute value (worst value)
5..10		–
11	00h	Reserved

Temperature Status Attribute

This attribute reports the current, min and max temperature if option-tempSensor is defined in dd.txt. The attribute value is set to the current temperature and the worst value is set to the maximum temperature. The temperature read out is done every 4 seconds.

Offset	Value	Description
0	194	Attribute ID – Temperature Status (vendor specific)
1..2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3		Attribute value
4		Attribute value (worst value)
5		Current temperature
6		Min. temperature
7		Max. temperature
8..10		–
11	00h	Reserved

3.18.5 SMART Read Attribute Thresholds

COMMAND CODE B0h with a Feature Register value of D1h
PROTOCOL PIO Data in.
INPUTS

Register	7	6	5	4	3	2	1	0
Features	D1h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS None required

ERROR OUTPUTS Aborted if the signature in the Cylinder registers is invalid, or if SMART is not enabled.

DESCRIPTION This command returns one sector of SMART attribute thresholds.

The data structure returned is:

Offset	Value	Description
0..1	0010h	SMART structure version
2..361		Attribute threshold entries 1 to 30 (12 bytes each)
362..379	00h	Reserved
380..510	00h	
511		Data structure checksum

Spare Block Count Attribute Threshold

Offset	Value	Description
0	196	Attribute ID – Reallocation Count
1		Spare Block Count Threshold
2..11	00h	Reserved

Spare Block Count Worst Channel Attribute Threshold

Offset	Value	Description
0	213	Attribute ID – Spare Block Count Worst Channel (vendor specific)

1		Spare Block Count Worst Channel Threshold
2..11	00h	Reserved

Erase Count Attribute Threshold

Offset	Value	Description
0	229	Attribute ID – Erase Count Usage (vendor specific)
1		Erase Count Threshold
2..11	00h	Reserved

Total ECC Errors Attribute Threshold

Offset	Value	Description
0	203	Attribute ID – Number of ECC errors
1	00h	No threshold for the Total ECC Errors Attribute
2..11	00h	Reserved

Correctable ECC Errors Attribute

Offset	Value	Description
0	204	Attribute ID – Number of corrected ECC errors
1	00h	No threshold for the Correctable ECC Errors Attribute
2..11	00h	Reserved

UDMA CRC Errors Attribute

Offset	Value	Description
0	199	Attribute ID – UDMA CRC error rate
1	00h	No threshold for the UDMA CRC Errors Attribute

2..11	00h	Reserved

Total Number of Reads Attribute

Offset	Value	Description
0	232	Attribute ID – Number of Reads (vendor specific)
1	00h	No threshold for the Total Number of Reads Attribute
2..11	00h	Reserved

Power On Count Attribute

Offset	Value	Description
0	12	Attribute ID – Power On Count
1	00h	No threshold for the Power On Count Attribute
2..11	00h	Reserved

Total LBAs Written Attribute

Offset	Value	Description
0	241	Attribute ID – Total LBAs Written (vendor specific)
1	00h	No threshold for the Total LBAs Written Attribute
2..11	00h	Reserved

Total LBAs Read Attribute

Offset	Value	Description
0	242	Attribute ID – Total LBAs Read (vendor specific)
1	00h	No threshold for the Total LBAs Read Attribute

2..11	00h	Reserved

Anchor Block Status Attribute

Offset	Value	Description
0	214	Attribute ID – Anchor Block Status (vendor specific)
1	00h	No threshold for the Anchor Block Status Attribute
2..11	00h	Reserved

Temperature Status Attribute

Offset	Value	Description
0	194	Attribute ID – Temperature Status (vendor specific)
1	00h	No threshold for the Temperature Status Attribute
2..11	00h	Reserved

3.18.6 SMART Read Log

COMMAND CODE B0h with a Feature Register value of D5h

PROTOCOL PIO data in.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	D5h							
Sector Count	Number of sectors to be read							
Sector Number	Log address							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS None required

ERROR OUTPUTS Aborted if the signature in the Cylinder registers is invalid, or if SMART is not enabled.

DESCRIPTION This command will return data of the SMART log. The following Log addresses are defined:

Address	Description
0x00	Log Directory
0x80..0x9F	Host Vendor Specific Logs
0xA0	SMART Wear Level Data
0xA1	SMART Remap Data
0xA2	Reserved

The Log Directory (at Log address 0) returns one sector that shows the number of sectors for Log addresses 1 to 255:

Offset	Value	Description
0..1	1	SMART Logging Version
10..11	1	Number of sectors in the CFA Feature Set log
256..319	16	Number of sectors in the logs at addresses 0x80..0x9F
320..321	4	Number of sectors in the log at address 0xA0
322..323	1	Number of sectors in the log at address 0xA1
324..325	1	Number of sectors in the log at address 0xA2

All other bytes in the Log Directory are zero.

The Host Vendor Specific Logs can be used by the host to store and retrieve arbitrary data.

The SMART Wear Level Data and SMART Remap Data logs return the same data that is also returned by the SMART Read Wear Level Data and SMART Read Remap Data com- mands.

3.18.7 SMART Write Log

COMMAND CODE B0h with a Feature Register value of D6h

PROTOCOL PIO data out.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	D6h							
Sector Count	Number of sectors to be written							
Sector Number	Log address							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS None required.

ERROR OUTPUTS Aborted if either the signature in the Cylinder registers, the Log address or the number of sectors is invalid, or if SMART is not enabled.

DESCRIPTION This command can be used to write data into the SMART log, see section 3.4.7 for the definition of the log addresses. Writes are allowed only to the Host Vendor Specific logs all other log addresses can only be read.

3.19 Device Parameters

iCF 1IE2 device parameters are listed in Table 50.

Table 50: Device parameters

Capacity	Cylinders	Heads	Sectors	LBA	Capacity(MB)
4GB	7,785	16	63	7847280	3831.7
8GB	15,538	16	63	15662304	7647.6
16GB	16,383	15	63	31293360	15280.0
32GB	16,383	15	63	62537328	30535.8
64GB	16,383	15	63	125059072	61064.0
128GB	16,383	15	63	250085376	122112.0

4. Innodisk Part Number Rule

CODE	1	2	3	4	5		6	7	8	9	10	11	12	13	14	15	16	17		18
	D	**H**	**C**	**F**	**C**	**-**	**0**	**8**	**G**	**Y**	**A**	**2**	**B**	**C**	**1**	**D**	**C**	**(W)**	**-**	**X**
Description	Disk	Feature Set	Form Factor			-	Capacity			controller			Flash Mode	Operation Temp.	Internal Control	CH	Flash Type	Optional Feature	-	Customized Code

Code 1st (Disk)	**Code 13th (Operation Temperature)**
D : Disk	C : Standard Grade (0 ~ +70 ℃)
	W : Industrial Grade (-40 ~ +85 ℃)
Code 2st (Feature Set)	**Code 14th (Internal Control Code)**
H: iSLC series	1~9 TSOP PCB version
Code 3nd ~ 5th (Form Factor)	**Code 15th (Channel of data transfer)**
CFC : CF card	S: Single Channel
	D: Dual Channel
Code 6th ~8th (Capacity)	**Code 16th (Flash Type)**
04G: 4GB	C: Toshiba MLC
08G: 8GB	
16G: 16GB	
32G: 32GB	**Code 17th (Optional Feature)**
64G: 64GB	W: Write Protect
128G: 128GB	
Code 9th ~ 11th (Controller)	**Code 18~th (Customized)**
YA2 : innodisk PATA controller	
Code 12th (Flash Mode)	
B: Toshiba 15nm	