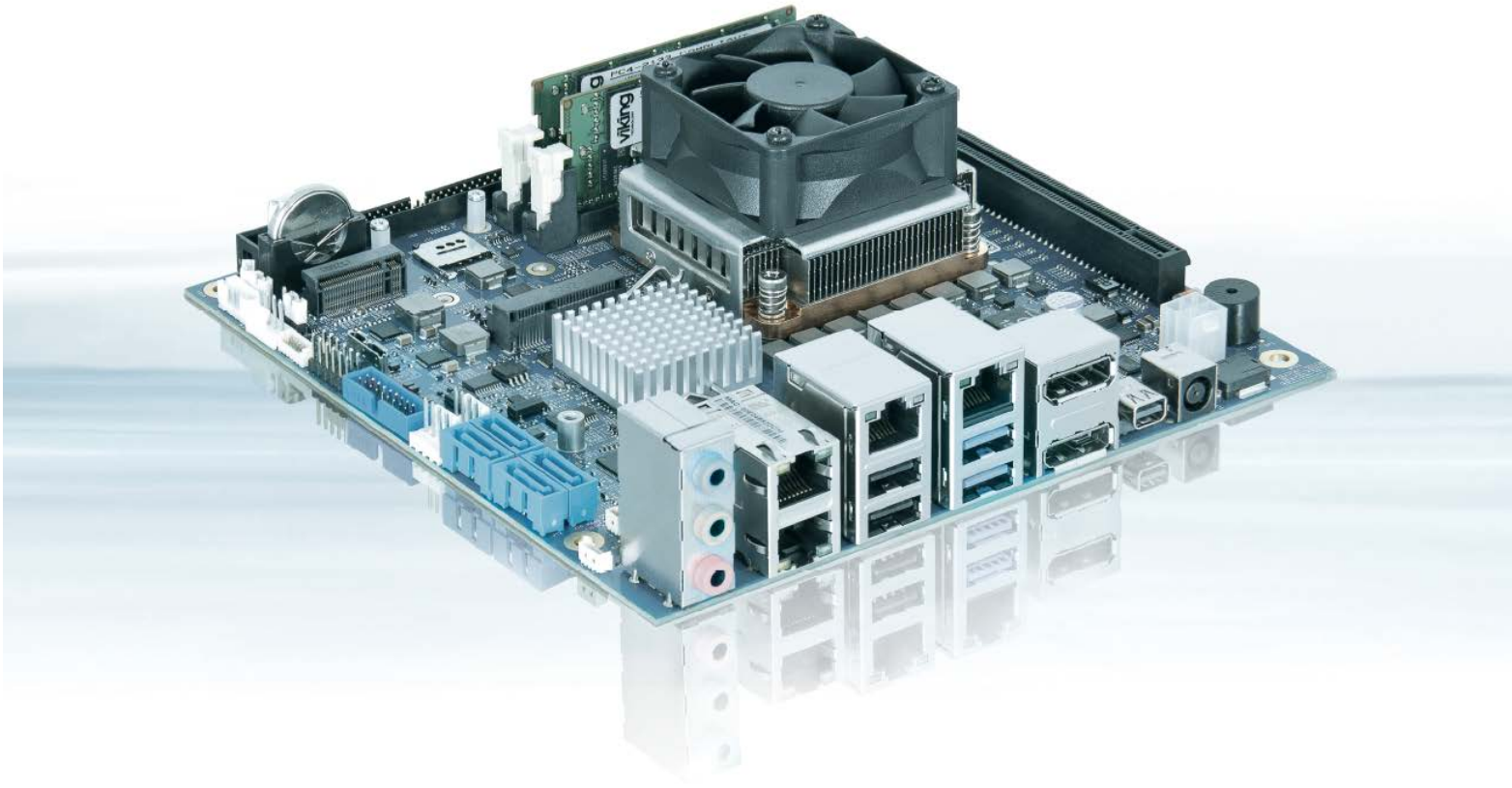
USER GUIDE



mITX-SKL-H

User Guide, Rev.1.5

Doc. ID: 1060-7483

POSSIBILITIES START HERE kontron S&T Group

MITX-SKL-H - USER GUIDE

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Kontron S&T AG

Lise-Meitner-Str. 3-5
86156 Augsburg
Germany
www.kontron.com

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Revision History

Revision	Brief Description of Changes	Date of Issue	Author
1.0	Initial Version	2017-Feb-15	CW
1.1	Added MTBF and Altitude, corrected position of J18 and J17 on Board Top Side View, corrected pin 78 and 79 for connector J4, removed On-board Connectors and Mating Connectors chapter, removed the UEFI Shell chapter and removed the following from BIOS Advanced setup chapter Thermal Configuration, Thunderbolt Support, Acoustic Management, SDIO Configuration and Switchable Graphics.	2017-May 12	CW
1.2	Added SATA Power Connector information and reinstated the On-board Connectors and Mating Connectors chapter.	2017-Sept-13	CW
1.3	Added Chapter 7.5: Caution Note.	2018-Oct-02	HJS
1.4	Chapter 4.2 Component Date, Expansion Capabilities and Chapter 8.15.1 PCI-Express x16 Connector (J4)	2020-Jan-28	CW
1.5	Added Limited Power Source Caution note and Power Supply Protection requirements	2020-Jun-17	CW

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If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

Symbols

The following signs and symbols may be used in this user guide:

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
NOTICE	NOTICE indicates a property damage message.
	Electric Shock! This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material. Please refer also to the "High-Voltage Safety Instructions" portion below in this section.
	ESD Sensitive Device! This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	HOT Surface! Do NOT touch! Allow to cool before servicing.
	Laser! This symbol inform of the risk of exposure to laser beam from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

⚠CAUTION

Handling and operation of the product is permitted only for trained personnel within a work place that is access controlled. Follow the "General Safety Instructions for IT Equipment" supplied with the product.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠CAUTION

Danger of explosion if the battery is replaced incorrectly.

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit http://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with Kontron.

Kontron follows the WEEE directive.

You are encouraged to return our products for proper disposal.

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1/ Introduction

This user guide describes the mITX-SKL-H motherboard made by Kontron AG. This board will also be denoted mITX-SKL-H within this user guide.

Use of this user guide implies a basic knowledge of PC-AT hard- and software. This user guide focuses on describing the mITX-SKL-H motherboard's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching on the power.

All configuration and setup of the CPU board is either carried out automatically or manually by the user via the BIOS setup menus.

The latest revision of this user guide, datasheet, BIOS, drivers, BSP's (Board Support Packages), mechanical drawings (2D and 3D) can be downloaded from Kontron's Web Page.

2/ Installation Procedures

2.1. Chassis Compliance

Before installing the mITX-SKL-H in the chassis, users must evaluate the chassis to ensure compliance with the requirements of the IEC60950-1 safety standard:

- The motherboard must be installed in a suitable mechanical, electrical and fire enclosure.
- The system, in its enclosure, must be evaluated for temperature and airflow considerations.
- The motherboard must be powered by a CSA or UL approved power supply that limits the maximum input current to 10 A via an external barrel-type +12 V to +24 V DC Jack, or to 16 A via an internal square ATX +12 V 4-pin connector.
- For interfaces having a power pin such as external power or fan, ensure that the connectors and wires are suitably rated. All connections from and to the product shall use Safety Extra Low Voltage (SELV) circuits only.
- Wires must have suitable ratings to withstand the maximum available power.
- The enclosure of the peripheral device fulfils IEC60950-1's fire protection requirements.

2.2. Installing the Board

NOTICE

ESD Sensitive Device

Electrostatic discharge (ESD) can damage equipment and impair electrical circuitry.

- Wear ESD-protective clothing and shoes
- Wear an ESD-preventive wrist strap attached to a good earth ground
- Check the resistance value of the wrist strap periodically (1 MΩ to 10 MΩ)
- Transport and store the board in its antistatic bag
- Handle the board at an approved ESD workstation
- Handle the board only by the edges

To get the board running follow these steps. If the board shipped from KONTRON already has components like RAM and CPU cooler mounted, then skip the relevant steps below.

NOTICE

Only connect to a power supply delivering the specified input rating and complying with the requirements of Safety Extra Low Voltage (SELV) and Limited Power Source (L.P.S.) of IEC 60950-1 and the Energy sources (ES1) of IEC 62368-1.

For more information, see Table 3: Electrical Specification

1. **Turn off the PSU (Power Supply Unit)**

NOTICE

Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected while configuring the board. Otherwise, components (RAM, LAN cards etc.) might get damaged. Make sure to use a +12 V to +24 V DC single supply only. Alternatively, use a standard ATX PSU with suitable cable kit and PS_ON# active.

2. **Insert the DDR4 1866/2133 module(s)**
   Be careful to push the memory module in the slot(s) before locking the tabs. For a list of approved DDR4 SO-DIMMs, see Chapter 4.6 System Memory or contact your Distributor or FAE.

3. **Cooler Installation**
   The mITX-SKL-H comes with a pre-installed cooler.

4. **Connecting Interfaces**
   Insert all external cables for hard disk, keyboard etc. A monitor must be connected in order to change BIOS settings.

5. **Connect and turn on PSU**
   Connect PSU to the board by the ATX+12 V- 4-pin connector or DC Jack.

6. **Power Button**
   If the board does not start by itself when switching on the ATX/DC PSU AC mains, then follow these instructions to start the board. Install the "Always On" Jumper in the "Always On" position or toggle the PWRBTN_IN# signal (available in the FRONTPNL connector), by momentary shorting pins 16 (PWRBTN_IN#) and pin 18 (GND).
   A "normally open" switch is recommended.

7. **BIOS Setup**
   Enter the BIOS setup by pressing the <DEL> key during boot up.

   Enter "Exit Menu" and Load setup Defaults.

   See Chapter 10.2 Setup Menus, for details on the BIOS setup.

CMOS jumper drains the RTC well and resets the date/time, it does not affect BIOS Settings

8. **Mounting the board in chassis**

   When fixing the motherboard in a chassis, it is recommended to use screws with integrated washer and a diameter of ≈7 mm. Do not use washers with teeth, as they can damage the PCB and cause short circuits.

NOTICE

When mounting the board in a chassis, take into consideration that the board contains components on both sides of the PCB that can easily be damaged if the board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

NOTICE

Vibration may cause damage to boards

When setting up boards within a system, steps must be taken to reduce the level of vibration within the system. It is the user's responsibility to ensure that boards can function properly in their system.

2.3. Lithium Battery Replacement

If replacing the lithium battery, follow the replacement precautions stated below.

⚠CAUTION

Danger of explosion if the lithium battery is incorrectly replaced.

- Replace only with the same or equivalent type recommended by the manufacturer
- Dispose of used batteries according to the manufacturer's instructions

3/ Product Variants

The mITX-SKL-H supports the Intel® Skylake processor family Intel® Xeon®, Core™ i7, Core™ i5, or Celeron® and is available as the following processor variants at the standard operating temperature (0°C to +60°C).

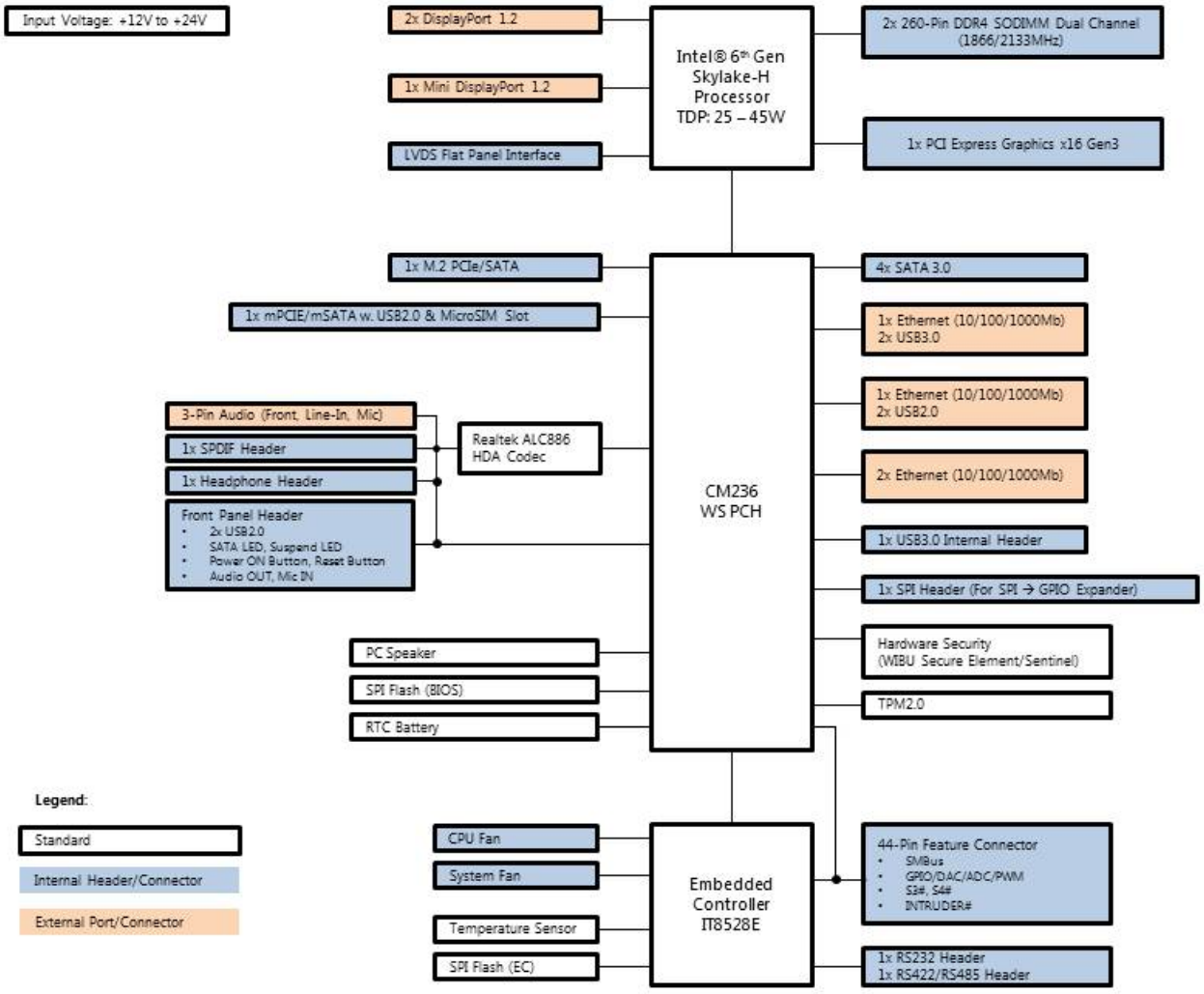
Table 1: Product Numbers Variants - Standard Operating Temperature (0°C to +60°C Operating)

Product Number	Product Name	Description
810670-4500	MITX-SKL-H CON XEON E3-1505M	Xeon ®E3-1505M 2.8 GHz 45W GT2, CM236 PCH, vPro, ECC; DP, w cooler
810671-4500	MITX-SKL-H CON i7-6820EQ	Core™ i7-6820EQ 2.8 GHz 45W GT2, CM236 PCH, non-ECC; DP, w cooler
810672-4500	MITX-SKL-H CON i5-6440EQ	Core™ i5-6440EQ 2.7 GHz 45W GT2, CM236 PCH, non-ECC; DP, w cooler
810673-4500	MITX-SKL-H CON G3900E	Celeron® G3900E, 2.4 GHz 35W GT1, CM236 PCH, non-ECC/ECC; DP, w cooler

4/ System Specifications

4.1. System Block Diagram mITX-SKL-H

Figure 1: System Block Diagram mITX-SKL-H



4.2. Component Main Data

The table below summarizes the main features of the mITX-SKL-H embedded motherboard components.

Form Factor	mITX-SKL-H – 170mm x 170 mm x 1.6 mm (PCB) Height approx. 50 mm from top of heat sink (highest point) to bottom of PCB (lowest point)
Processor	6th Generation Intel ® Skylake-H processors BGA 1440 (14 nm), CPU variants (TDP 25 W-45 W)
Memory	System memory ▶ DDR4 non-ECC/ECC SO-DIMM 1866/2133 (2 sockets) ▶ Dual channel DDR4 memory interface ▶ Support system memory up to 32 GB (2 x 16 GB)
SPI BIOS Memory /Firmware	▶ On-board 16 MB for system BIOS Winbond W25Q128FVSIG, Micron Technology N25Q128A13ESE40E or Macronix MX25L12835FM2I-10G ▶ On-board 4 MB SPI Flash for embedded controller firmware and board information SPI connector for external BIOS hard flash
Chipset	Mobile Intel ® CM236 Chipset ▶ Intel ® VT-d (Virtualisation Technology for Directed I/O) ▶ Intel ® TXT (Trusted Execution Technology) ▶ Intel ® vPRO ▶ Intel ® ME Firmware Version 11.0 ▶ Intel ® HD Audio Technology ▶ Intel ® Rapid Storage Technology ▶ Intel ® Rapid Storage Technology Enterprise ▶ SATA (Serial ATA) Gen 3 ▶ USB revision 2.0 ▶ USB revision 3.0 ▶ PCI Express revision 3.0 ▶ ACPI 6.0 compliant ▶ HD video playback
Security	▶ WIBU CodeMeter ASIC 1504-03 ▶ Safenet sentinel HL Chip (Optional) ▶ Trusted Platform Module (TPM) 2.0 support
Management	Intel ® Active Management Technology (Intel ® AMT) 9.0
Audio	High Definition Audio Realtek ALC886 HDA codec ▶ Line-in and Line-out ▶ Microphone: MIC1 and MIC2 ▶ SPDIF-Out (electrical interface only) ▶ On-board speaker (Electromagnetic Sound Generator like Hycom HY-05LF)
Video	Intel ® Generation 9 Graphics including Intel ® HD Graphics 510, Intel ® HD Graphics 530 or Intel ® HD Graphics P530 ▶ Three DP (Display Ports), comply with Display Port 1.2 specification ▶ HDMI panel support via DP to HDMI Adapter Converter ▶ DVI panel support via DP to DVI Adapter Converter ▶ VGA panel support via DP to VGA Adapter Converter ▶ LVDS panel support up to 2 channel 24-bit color (VESA and JEIDA) ▶ Triple independent pipes for Mirror or Triple independent display support ▶ Triple independent pipes for triple independent or cloned displays supported from OS. Any three displays via DP1, DP2, miniDP and LVDS can be used.
I/O Control	Via ITE IT8528E Embedded Controller via LPC Bus interface

Peripheral Interfaces	▶ Four USB 3.0 (2 x Rear I/O and 2 x optional from Internal connector) ▶ Four USB 2.0 (2x Rear I/O and 2 x Front panel connector) ▶ Optional internal USB 2.0 from mPCIe connector ▶ One Serial Port (RS232C) ▶ One Serial Port (RS422/485) ▶ Four SATA 3.0 Ports (RAID 0 / 1 / 5 / 10 support)
LAN Support	Up to four 10/100/1000 Mbit/s (RJ45) LAN with integrated magnetics and rear IO LEDs
Expansion Capabilities	▶ Slot PCIex16 (Gen 2.0 & 3.0) ▶ Support PEG Bifurcation 1 x16 (default) or 2 x8 or 1 x8 + 2 x4 through HW strapping option ▶ One mPCIe/mSATA connector with USB 2.0 port with USB SIM interface ▶ One M.2 connector supporting up to 4x PCIe lanes or a SATA interface ▶ SMBus compatible with ACCESS BUS and I2C BUS, (via Feature connector) ▶ SPI bus routed to SPI connector ▶ DDC/AUX Bus routed to DP connector (Auto detect to DDC when using passive DP to HDMI or DVI adapters) ▶ 18x GPIOs (General Purpose I/Os), (via Feature connector) ▶ DAC, ADC, PWM and TIMER (Multiplexed), (via Feature connector) ▶ WAKE UP / Interrupt Inputs (Multiplexed), (via Feature connector) ▶ 3-Wire Bus for GPIO Expansion (up to 152 GPIOs), (via Feature connector) ▶ 4-Wire SPI connector for GPIO Expansion ▶ Timer output (8-bit), (via Feature connector)
Hardware Monitor Subsystem	Smart Fan control system Supports two on-board Fan connectors: ▶ CPU Fan (on-board) ▶ System Fan (on-board) Thermal inputs: ▶ CPU Die temperature (precision +/- 3° C) ▶ System temperature (precision +/- 3° C)
Power Supply Unit	Operated by a single +12 V to +24 V DC Power Supply via either: ▶ Rear Barrel-type DC Jack DC ▶ ATX 4-pin connector **Operating at +12.6 V to +13.5 V range is not recommended.**
Battery	▶ Exchangeable 3.0 V Lithium battery for on-board Real Time Clock and CMOS RAM ▶ Manufacturer Panasonic / Part-number CR-2032L/BN, CR2032N/BN or CR-2032L/BE ▶ Approximate 6.2 years retention ▶ Current draw is less than 4.2µA when PSU is disconnected and 0 µA in S0 – S5 **⚠CAUTION** **Danger of explosion if the lithium battery is incorrectly replaced.** ▶ Replace only with the same or equivalent battery type recommended by be the manufacturer ▶ Dispose of used batteries according to the manufacturer's instruction

BIOS	Kontron AMI Aptio® V BIOS (EFI EDK2 core version) Support for ACPI 6.0 (Advanced Configuration and Power Interface) and above, Plug & Play ▶ Suspend To Ram (S3 mode) ▶ Suspend To Disk (S4 mode) ▶ "Always On" BIOS power setting ▶ RAID Support (RAID modes 0, 1, 5 and 10)
Operating System Support	Windows ▶ Windows 7 (64-bit) ▶ Windows 8.1 (64-bit) ▶ Windows 10 (64-bit) ▶ WES(Windows Embedded Standard) 7 (64-bit) Linux ▶ Linux (64-bit) ▶ Fedora-22 (64-bit) ▶ Yocto-2.1.2 (64-bit)

4.3. Environmental Conditions

The mITX-SKL-H is compliant with the following environmental conditions. It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within the allowed temperature range.

Operating Temperature	0°C to +60°C operating temperature (forced cooling)
Storage Temperature	-40°C to +70°C lower limit of storage temperature 50% to 95% relative humidity (non-condensing at 25°C to 30°C)

4.4. Standards and Certifications

The mITX-SKL-H meets the following standards and certification tests.

Electrostatic Discharge (ESD) **Radiated Emissions (EMI)**	All Peripheral interfaces intended for connection to external equipment are ESD/EMI protected. EN55022:2010 Class B - Electromagnetic compatible: Emission Standard for commercial environments EN 61000-3-2 - Electromagnetic compatibility (EMC) - Part 3-2: Limits harmonic current emission for commercial environments EN 61000-3-3 - Electromagnetic compatibility (EMC) - Part 3-3: Limits voltage changes, voltage fluctuations and flicker for commercial environments EN55024:2010 Immunity IEC / EN 61000-4-2 - Electrostatic discharge ESD IEC / EN 61000-4-3 - Radiated field IEC / EN 61000-4-4 - Electrical fast transient/burst IEC / EN 61000-4-5 - Surge IEC / EN 61000-4-6 - Immunity to conducted disturbances IEC / EN 61000-4-8 – Power frequency magnetic field IEC / EN 61000-4-11 - Voltage dips and short interruptions
Safety	IEC 60950-1 UL 60950-1 CSA C22.2 No. 60950-1
Shock (Bump)	IEC 60068-2-27 Half sign mechanical shock test (2 gn, 11 ms)
Vibration	IEC 60068-2-6 Random vibration test operating (10 Hz- 500 Hz, 1.93 grms)
Theoretical MTBF	603931 hrs @ 40°C, based on Telcordia SR-332 Issue 3
Non-Operating Altitude	Up to 2000 m
Restriction of Hazardous Substances (RoHS)	All boards in the mITX-SKL-H family are RoHS2 compliant

4.5. Supported Processors

The mITX-SKL-H supports a factory mounted BGA CPU (BGA1440) Intel® Xeon®, Core™ i7, Core™ i5, or Celeron® processor. All board versions are based on embedded CPUs.

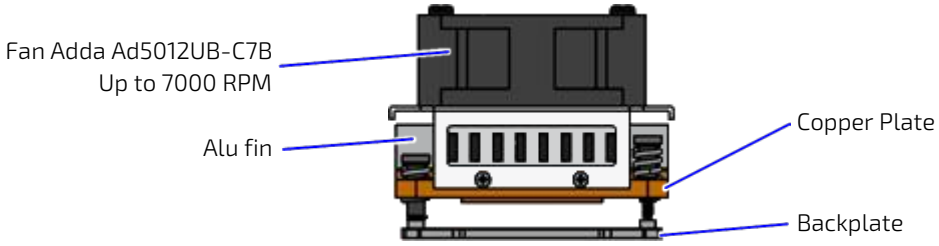
- Intel® Xeon® E3 1505M 45W GT2, CM236 WS PCH, VPro™, non-ECC/ECC
- Intel® Core™ i7 6820EQ 45W GT2, CM236 WS PCH, non-ECC
- Intel® Core™ i5-6440 EQ 45W GT2, CM236 WS PCH, non –ECC
- Intel® Celeron® G3900E 35W GT1, CM236 WS PCH, non-ECC/ECC

4.5.1. Processor Cooling

Sufficient cooling must be applied to the processor in order to remove the effects of TDP (Thermal Design Power). The level of sufficient cooling also depends on the worst-case maximum ambient operating temperature and the actual worst-case load of processor.

mITX-SKL-H is delivered with pre-installed cooler, the Kontron PN 1060-1672 "CPU Cooler mITX-SKL-H":

Figure 2: CPU Cooler mITX-SKL-H, height above PCB = 44.7 mm



4.6. System Memory

The mITX-SKL-H supports a dual channel DDR4 memory interface with one SO-DIMM socket per channel. The sockets support the following memory features:

- 2x DDR4 260-pin SO-DIMM 260 (ECC and non-ECC)
- ECC supported for Xeon and Celeron SKU only
- 2x SO-DIMM sockets, one per channel
- Maximum supported memory 32 GB
- Memory controller supports speeds of 1866/2133 MHz

If using 32-bit OS, less than 4GB is displayed in system.
(Shared Video Memory/PCI resources are subtracted).

The installed DDR4 SO-DIMM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted, or the board may not be able to boot totally.

4.6.1. Memory Operating Frequencies

In all modes, the frequency of system memory is the lowest frequency of all the memory modules placed in the system. Each memory module's frequency can be determined through the SPD registers on the memory modules.

The table below lists the resulting operating memory frequencies based on the combination of DIMMs and processor.

DIMM Type	Module Name	Memory Data Transfers (MT/s)	Resulting Memory Clock Frequency (MHz)	Theoretical Memory Bandwidth in Dual-Channel Mode (GB/s)
DDR4 1866	PC4-1866	1866	933	29.1
DDR4 2133	PC4-2133	2133	1066	33.3

Kontron offers the following memory modules:

- DDR4-2133 non-ECC SODIMM 4GB, PN 1060-2753
- DDR4-2133 non-ECC SODIMM 8GB, PN 1060-2760
- DDR4-2133 non-ECC SODIMM 16GB, PN 1060-2761
- DDR4-2133 ECC SODIMM 4GB, PN 1060-2762
- DDR4-2133 ECC SODIMM 8GB, PN 1060-2763
- DDR4-2133 ECC SODIMM 16GB, PN 1060-2764

Memory modules have, in general, a much lower longevity than embedded motherboards, and therefore the EOL of modules can be expected several times during lifetime of the motherboard. Kontron guarantees that the part numbers above will be maintained so that other similar types of qualified modules replace EOL modules.

As a minimum, it is recommended to use Kontron memory modules for prototype system(s) in order to prove the stability of the system and as a reference.

For volume production, you might request to test and qualify other types of RAM. In order to qualify RAM, it is recommend to configure 3 systems running a RAM stress test program in a heat chamber at 60 °C for a minimum of 24 hours.

4.7. On-Board Graphics Subsystem

The mITX-SKL-H supports Intel ® HD Graphics with three Display Ports (DPs). The DP interface supports the Display Port 1.2 specification.

Processor	Graphics	Base Frequency	Graphic Output	Max. Resolution	DirectX Support	OpenGL Support
Xeon® E3-1505M	Intel® HD Graphics P530	350 MHz	eDP/ DP/ HDMI/ VDI	4096 x 2304 px @ 60 Hz (eDP/DP) @ 24 Hz (HDMI 1.4)	12	4.4
i7-6820EQ	Intel® HD Graphics 530	350 MHz	eDP/ DP/ HDMI/ VDI	4096 x 2304 px @ 60 Hz (eDP/DP) @ 24 Hz (HDMI 1.4)	12	4.4
i5-6440EQ	Intel® HD Graphics 530	350 MHz	eDP/ DP/ HDMI/ VDI	4096 x 2304 px @ 60 Hz (eDP/DP) @ 24 Hz (HDMI 1.4)	12	4.4
Celeron® G3900E	Intel® HD Graphics 510	350 MHz	eDP/ DP/ HDMI/ VDI	4096 x 2304 px @ 60 Hz (eDP/DP) @ 24 Hz (HDMI 1.4)	12	4.4

Features of the Intel HD Graphics include:

- Next Generation Intel® Clear Video Technology HD Support is a collection of video playback and enhancement features that improve the end user's viewing experience
- Encode transcode HD content
- Playback of high definition content including Blu-ray Disc©
- Superior image quality with sharper, more colorful images
- Playback of Blu-ray© disc S3D content using HDMI (1.4a specification compliant with 3D)
- DirectX© Video Acceleration (DXVA) support for accelerating video processing
- Full AVC/VC1/MPEG2 HW Decode
- Advanced Scheduler 2.0, 1.0, XPDM support
- Operating Systems supported:
    - Windows© 10, 8.1
    - OSX
    - Linux© -Fedora-22 (64-bit) and Yocto-2.1.2 (64-bit)
- DirectX© 12 support
- OpenGL© 4.4 support

Up to three displays (DP1, DP2, miniDP or LVDS) can be used simultaneously to implement independent or cloned display configurations. Displays can be connected directly to any of the two display port connectors, a mini display port connector or to an LVDS convertor (via an eDP toLVDS convertor)

Table 2: Display Resolutions

Display Configuration	Maximum Display Resolution
Display Port / mini Display Port	4096 x 2304 px @ 60 Hz, 24 bpp
HDMI 1.4 (native)	4096 x 2160 px @ 24 Hz, 24 bpp
HDMI 2.0 (via LSPCon)	4096 x 2160 px @ 60 Hz, 24 bpp
DVI	1920 x 1200 px @ 60 Hz, 24 bpp
LVDS (via eDP)	1920 x 1200 px @ 60 Hz, 24 bpp

bpp – bit per pixel

The processor supports only three streaming independent and simultaneous display combinations of DP/eDP/HDMI/DVI monitors.

If four monitors are plugged in, the software policy determines which of the three interfaces will be used.

Supporting 4K display requires two DDR channels of the same size. Performance degradations exists while running 4K content for systems using single channel system memory (compared to using dual channel).

High-Bandwidth Digital Content Protection (HDCP) is the technology used to protecting high-definition content against unauthorized copying or interception between the source (computer, digital set top boxes, and so on) and the sink (panels, monitor, and TVs). The mITX-SKL-H supports HDCP 1.4 for content protection over-wired displays (HDMI, DVI, and DP). The HDCP 1.4 keys are integrated into the processor and customers are not required to physically configure or handle the keys.

4.7.1. External Graphics

External graphics is supported through one PCI Express 16-pin graphics slot allowing for bifurcation (2x8, 1x16 or 1x8 + 2x4). For more information, see Chapter 8.15.1 PCI-Express x16 Connector (J4).

4.8. Power Supply Specification

Use an appropriate power supply that meets the mITX-SKL-H's electrical specification (Table 3). Additionally, for safe operation the power supply must monitor the supply voltage and shut down if the supply is out of range. The power supply's correct input range may be either switch-selectable or auto-ranging and the power supply must automatically recover from AC power loss and be able to start up under peak loading.

The power supply connects to either the DC power jack or the on-board ATX +12 VDC 4-pin connector with a suitable cable kit and PS_ON# active.

⚠CAUTION

The board can be supplied via a power supply (AC/DC adapter) plugged into the DC power jack. Such adapters have usually no connection to protective earth. Consequently, the potential of the conductive parts on the board may drift. If a human touches such a part, this may lead to an electric shock. The board must be grounded separately, if the unit is supplied via the DC power jack.

The ATX+12V 4-pin connector must be used in according to the ATX12V PSU standard.

Table 3: Electrical Specification

Supply	Min.	Max.	Note
+12 V to +24 V[1]	11.4 V	25.2 V	Supply voltage should be ±5% for compliance with the ATX specification.
GND	0 V	0 V	Power supply GND

[1] Kontron does not recommend operating within the +12.6 VDC to +13.5 VDC range.

NOTICE

Only connect to a power supply delivering the specified input rating and complying with the requirements of Safety Extra Low Voltage (SELV) and Limited Power Source (L.P.S.) of IEC 60950-1 and the Energy sources (ES1) of IEC 62368-1.

For more information, see Table 3: Electrical Specification.

NOTICE

Ensure that the power supply manufacturer's instructions and conditions are observed.

NOTICE

Hot Plugging the power supply is not supported. Hot plugging might damage the board.

4.8.1. Power Supply Protection Requirements

Before connecting the board to an external power supply that is connected to the mains power supply ensure that protection and supply limitation requirements have been taken into consideration, to protect the board against fluctuations and interruptions in the delivered DC power supply such as Over Current Protection, Inrush Current Protection, Over Voltage Protection and Input Under Voltage Protection

The used power supply is required to contain protection circuitry such that an unintentional temporary voltage drop in the mains power supply (input under voltage) below the power supply's specified minimum, for longer than the power supply's holdup time (brownout), shuts down the power supply. The power supply must remain in this "off state" until the board's internal voltages have discharged sufficiently.

NOTICE

The power supply used must comply with the requirements of the IEC 60950-1 or IEC 62368-1 standard or better. In the case of an unintentional temporary under voltage interruption use a power supply with an adequate holdup-time (brownout) and ensure the power supply has been fully tested to at least meet the minimum immunity of AC inputs requirements, as stipulated in IEC 55024. Including power supplies marketed with a separate AC/DC power converter.

NOTICE

After a brownout condition the power supply must remain in the "off state" long enough to allow all internal voltages to discharge sufficiently. Failure to observe this required "off state" time may mean that parts of the board or peripherals work incorrectly or suffer a reduction of MTBF. The minimum "off state" time, to allow internal voltages to discharge sufficiently, is dependent on the power supply and additional electrical factors. To determine the required "off state" time, each case must be considered individually. For more information, contact Kontron Support.

4.8.2. Power Consumption

To keep the power consumption to a minimal level, the mITX-SKL-H does not implement a guaranteed minimum load. In some cases, this can lead to compatibility problems with ATX power supplies that require a minimum load to remain regulated.

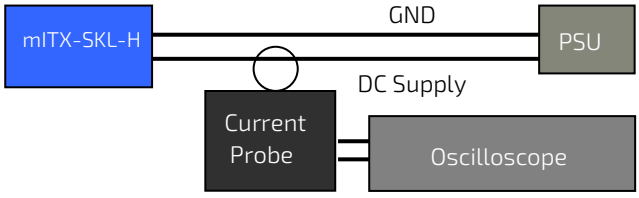
Static Power Consumption

The power consumption is measured in the low power setup and high power setup under the following software and hardware test condition.

1. Windows 10 64-bit Idle
2. Windows 10 64-bit 3DMark (Cloud Gate)
3. Windows 10 64-bit Intel® TAT, 100 % on all CPU cores and GFX
4. Windows 10 64-bit S3 (Sleep)
5. Windows 10 64-bit S5 (Shutdown)

The principle hardware test system and test equipment:

1. Teledyne LeCroy HDO4034 Oscilloscope
2. Teledyne LeCroy CP030 Current Probe
3. mITX-SKL-H Board (Core i7-6820EQ)
4. Keysight E3634A DC Power Supply (Low Power)
5. Keysight 6673A DC Power Supply (High Power



Power consumption of PSU (power loss), Monitor and SSD are not included.

mITX-SKL-H Low Power Setup:

Standard system configuration equipped with: Internal graphics, 1x SATA SSD disks, Intel® Core™ i7-6820EQ CPU, 1x SO-DIMM (4 GB module), 1x Display Port monitor, keyboard & mouse (USB), 1x 16 GB USB flash drive, +12 V CPU active cooler, 1x Ethernet connected and >90 W DC power supply.

mITX-SKL-H Low Power Setup Results:

Low Power – Windows 10 64-bit – Idle		
Supply (Actual)	Current Draw	Power Consumption
+12 V (12.01 V)	1316 mA	15.80 W
+24 V (24.06 V)	765 mA	18.41 W

Low Power – Windows 10 64-bit – 3Dmark (Cloud Gate)		
Supply (Actual)	Current Draw	Power Consumption
+12 V (11.98 V)	3428 mA	41.07 W
+24 V (24.07 V)	1736 mA	41.79 W

Low Power – Windows 10 64-bit – Intel® TAT 100% all CPU cores and GFX		
Supply (Actual)	Current Draw	Power Consumption
+12 V (11.77 V)	6528 mA	76.84 W
+24 V (24.02 V)	3034 mA	72.88 W

Low Power – Windows 10 64-bit – S3 (Sleep)		
Supply (Actual)	Current Draw	Power Consumption
+12 V (12.04 V)	182 mA	2.19 W
+24 V (24.06 V)	147 mA	3.54 W

Low Power – Windows 10 64-bit – S5 (Shutdown)		
Supply (Actual)	Current Draw	Power Consumption
+12 V (12.06 V)	155 mA	1.87 W
+24 V (24.09 V)	137 mA	3.30 W

mITX-SKL-H High Power Setup:

Standard system configuration equipped with: 1x PCIe X16 external graphics (AMD FirePro W4100), 1x M.2 PCIe SSD, 2x SATA SSD disks, 1x mPCIe Wi-Fi module, Intel® Core™ i7-6820EQ CPU, 2x SO-DIMM (16GB modules), 2x Display Port monitor, keyboard & mouse (USB), 4x 16GB USB flash drive, +12 V CPU active cooler, 1x +12 V system fan, 2x Ethernet connected and >120 W DC power supply.

mITX-SKL-H High Power Setup Results:

High Power – Windows 10 64-bit – Idle		
Supply (Actual)	Current Draw	Power Consumption
+12 V (12.02 V)	2966 mA	35.65 W
+24 V (24.01 V)	1714 mA	41.15 W

High Power – Windows 10 64-bit – 3Dmark (Cloud Gate)		
Supply (Actual)	Current Draw	Power Consumption
+12 V (12.05 V)	6963 mA	83.90 W
+24 V (24.03 V)	3744 mA	89.97 W

High Power – Windows 10 64-bit – Intel TAT 100% all CPU cores and GFX		
Supply (Actual)	Current Draw	Power Consumption
+12 V (12.00 V)	10193 mA	122.32 W
+24 V (24.00 V)	5168 mA	124.03 W

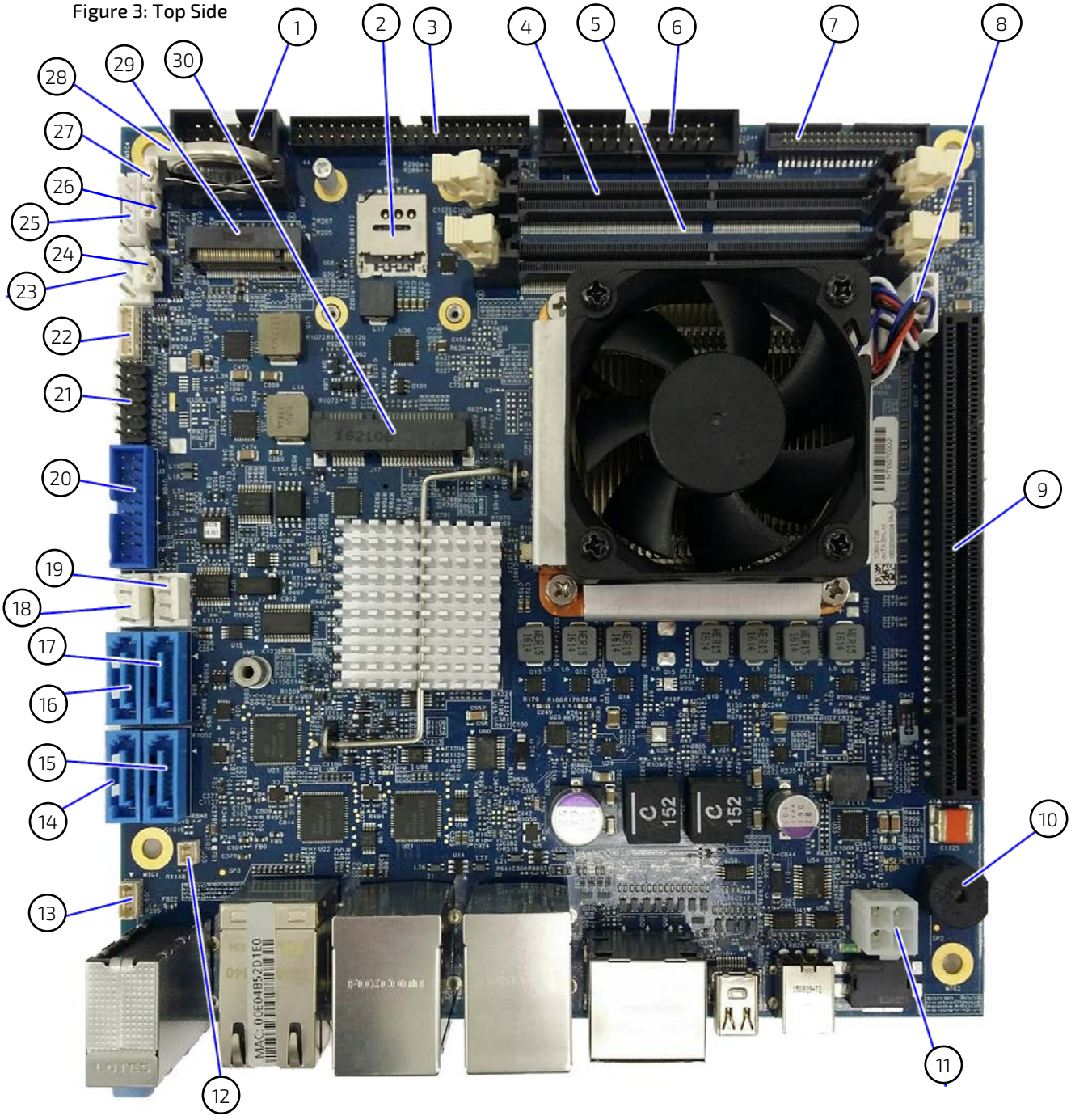
High Power – Windows 10 64-bit – S3 (Sleep)		
Supply (Actual)	Current Draw	Power Consumption
+12 V (12.02 V)	311 mA	3.74 W
+24 V (24.07 V)	209 mA	5.03 W

High Power – Windows 10 64-bit – S5 (Shutdown)		
Supply (Actual)	Current Draw	Power Consumption
+12 V (12.02 V)	260 mA	3.13 W
+24 V (24.07 V)	182 mA	4.38 W

5/ Connector Locations

5.1. Top Side

Figure 3: Top Side

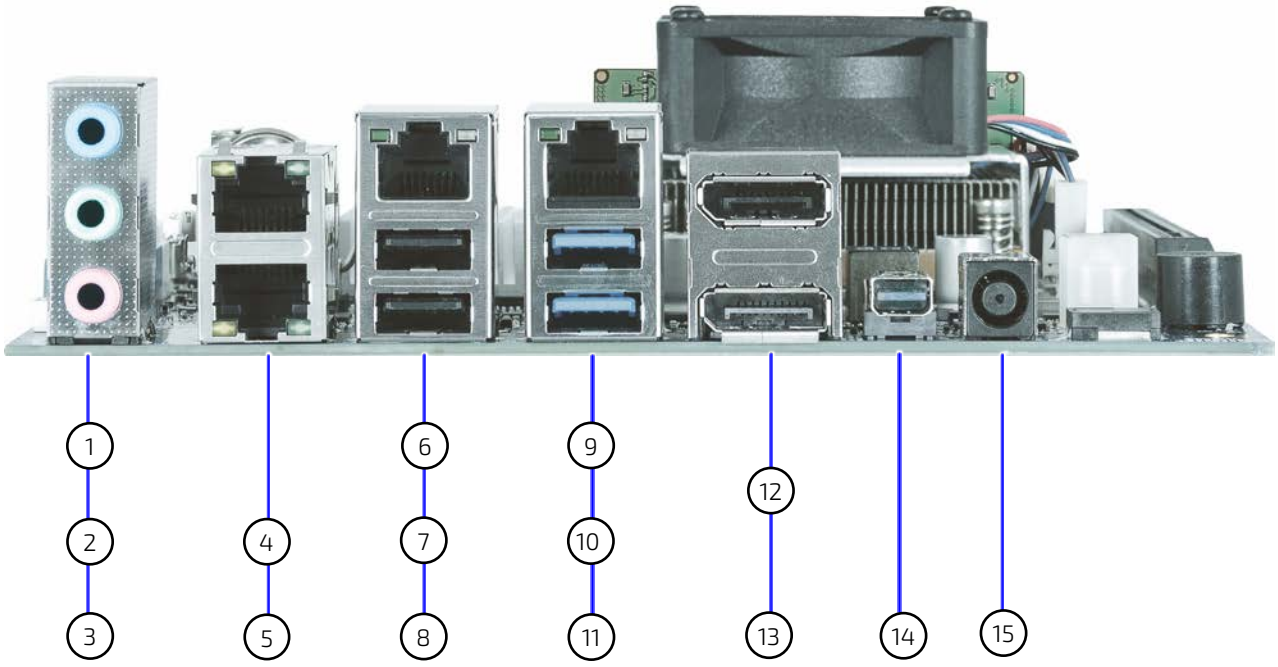


Item	Designation	Description	See Chapter
1	J22	COM Port 1 (RS232)	8.8
2	J20	MicroSIM-Card Connector	8.15.2
3	J26	Feature Connector	8.11
4	J2	DDR4 SO-DIMM Slot 2	4.6
5	J1	DDR4 SO-DIMM Slot 1	4.6

Item	Designation	Description	See Chapter
6	J27	Front Panel Connector	8.7
7	J7	LVDS Flat Panel Connector	8.10
8	J33	CPU Fan Connector	8.2
9	J4	PCIe Graphics x 16 Connector	8.15.1
10	SPK1	Speaker	
11	J31	ATX+12V 4-pin Power Connector	8.1
12	J30	SPDIF Connector	8.6
13	J29	Headphone/Speaker Connector	8.5
14	J10	SATA 1 Connector	8.3
15	J12	SATA 2 Connector	8.3
16	J13	SATA 4 Connector	8.3
17	J11	SATA 3 Connector	8.3
18	J23	SATA Power Connector 1	8.16
19	J24	SATA Power Connector 2	8.16
20	J3	Internal USB 3.0 Connector	8.4
21	J9	SPI BIOS Hardflash Connector	8.12
22	J36	SPI External Fast GPIO Connector	8.13
23	J34	System Fan Connector	8.2
24	J39	Always On Jumper	8.14.1
25	J35	COM Port 2 (RS422/485)	8.9
26	J38	Load BIOS Default Jumper	8.14.3
27	J37	Clear CMOS Jumper	8.14.2
28	J28	RTC Battery Holder	2.3
29	J18	M.2 PCIe /M.2 SATA Connector	0
30	J17	mPCIe/mSATA Connector	8.15.2

5.2. Connector Panel Side

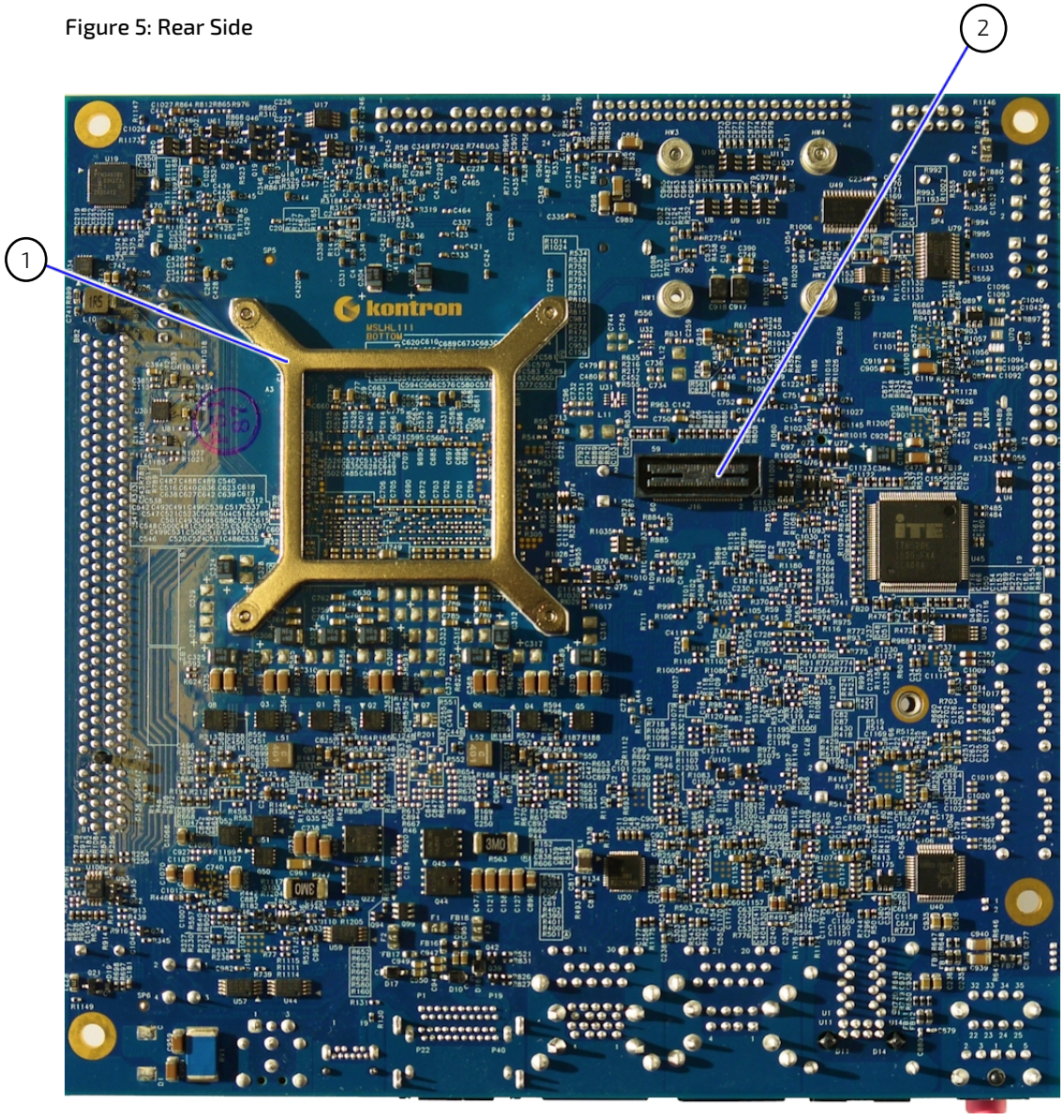
Figure 4: Connector Panel Side



Item	Designation	Description	See Chapter
1	J6-blue	Line-In 1	7.4
2	J6-green	Line-Out (Speaker)	7.4
3	J6-pink	Microphone 1	7.4
4	J8-top	Ethernet Port 3 (10/100/1000 Mb)	7.2
5	J8-bottom	Ethernet Port 4 (10/100/1000 Mb)	7.2
6	J5-(LAN)	Ethernet Port 2 (10/100/1000 Mb)	7.2
7	J5-top (USB)	USB Port 3 (USB 2.0)	0
8	J5-bottom (USB)	USB Port 4 (USB 2.0)	0
9	J21 (LAN)	Ethernet Port 1 (10/100/1000 Mb)	7.2
10	J21-top (USB)	USB Port 1 (USB 3.0/2.0)	7.3.1
11	J21-bottom (USB)	USB Port 2 (USB 3.0/2.0)	7.3.1
12	J14-top	Display Port (DP1)	7.1
13	J14-bottom	Display Port (DP2)	7.1
14	J15	Mini Display Port (DP3)	7.1.1
15	J32	DC Jack	7.5

5.3. Rear Side

Figure 5: Rear Side



Item	Designation	Description
1		Backplate CPU Cooler
2	J16	XDP Connector (NC)

6/ Connector Definitions

The following defined terms are used within this user guide to give more information concerning the pin assignment and to describe the connector's signals.

Defined Term	Description
Pin	Shows the pin numbers in the connector
Signal	The abbreviated name of the signal at the current pin. The notation "XX#" states that the signal "XX" is active low
Type	AI: Analogue Input AO: Analogue Output I: Input, TTL compatible if nothing else stated IO: Input / Output. TTL compatible if nothing else stated IOT: Bi-directional tristate IO pin IS: Schmitt-trigger input, TTL compatible IOC: Input / open-collector Output, TTL compatible IOD: Input / Output, CMOS level Schmitt-triggered (Open drain output) NC: Pin not connected O: Output, TTL compatible OC: Output, open-collector or open-drain, TTL compatible OT: Output with tri-state capability, TTL compatible LVDS: Low Voltage Differential Signal PWR: Power supply or ground reference pins
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins
Note	Special remarks concerning the signal
Designation	Type and number of item described
See Chapter	Number of the chapter within this user guide containing a detailed description

The abbreviation TBD is used for specifications that are not available yet or which are not sufficiently specified by the component vendors.

7/ I/O-Area Connectors

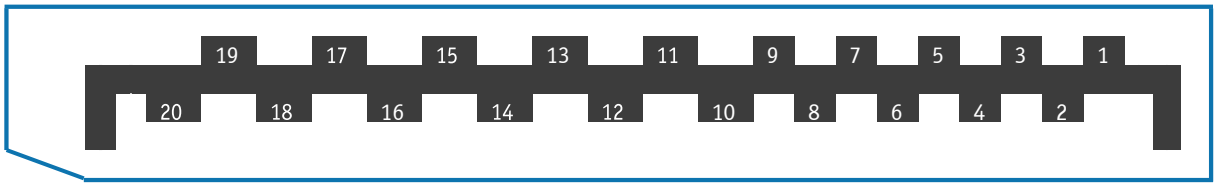
The following connectors are available on the connector panel of the mITX-SKL-H. For information regarding the connector's position on the panel, see Chapter 5.2 Connector Panel Side.

7.1. DP Connectors DP1, DP2 (J14)

The mITX-SKL-H display port (DP) connectors are based on standard DP type Foxconn 3VD11203-DPA1-4H or similar.

Figure 6: DP Connectors DP1 (Top) and DP2 (Bottom)

Top



Bottom

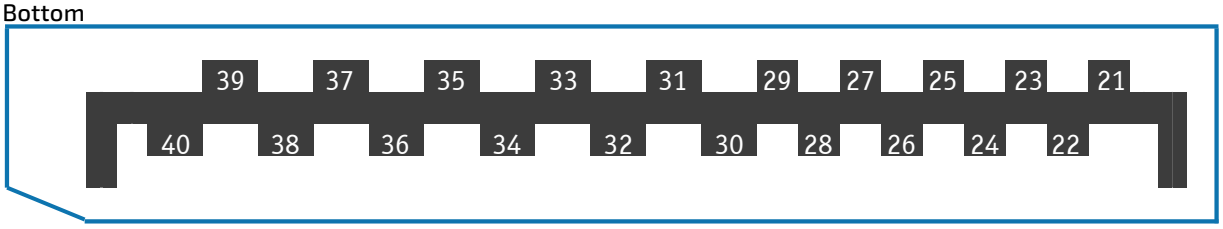


Table 4: Pin Assignment DP Connector DP1, DP2 (J14)

Pin	Signal	Description	Type	Note
1/21	Lane 0 (+)		LVDS	
2/22	GND		PWR	
3/23	Lane 0 (-)		LVDS	
4/24	Lane 1 (+)		LVDS	
5/25	GND		PWR	
6/26	Lane 1 (-)		LVDS	
7/26	Lane 2 (+)		LVDS	
8/28	GND		PWR	
9/29	Lane 2 (-)		LVDS	
10/30	Lane 3 (+)		LVDS	
11/31	GND		PWR	
12/32	Lane 3 (-)		LVDS	
13/33	Config. 1	Aux or DDC selection	I	Internally pull down (1 MΩ). Aux channel on pin-15/17 or pin-35/37 selected as default (if NC). DDC channel pin-15/17 or pin-35/37, if HDMI adapter used (3.3 V).
14/34	Config. 2	(Not used)	O	Internally connected to GND
15/35	Aux+	Aux Channel (+) or DDC Clk		AUX (+) channel used by DP DDC Clk used by HDMI

Pin	Signal	Description	Type	Note
16/36	GND		PWR	
17/37	Aux-	Aux Channel (-) or DDC Data		AUX (-) channel used by DP, DDC Data used by HDMI
18/38	Hot Plug		I	Internally pull down (100 KΩ)
19/39	Return		PWR	Same as GND
20/40	3.3 V		PWR	Fused by 1.5 A resettable PTC fuse

7.1.1. mini DP Connector DP3 (J15)

The mITX-SKL-H mini DP connector is based on the standard Mini DP type ASTRON 6990020-X04-H or similar.

Figure 7: Mini DP Connector DP3

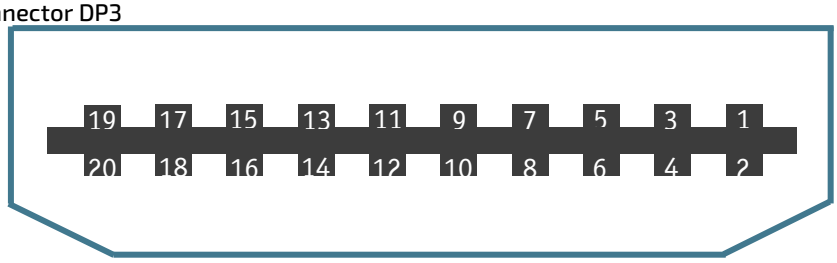


Table 5: Pin Assignment mini DP Connector DP3 (J15)

Pin	Signal	Description	Type	Note
1	Lane 0 (+)		LVDS	
2	GND		PWR	
3	Lane 0 (-)		LVDS	
4	Lane 1 (+)		LVDS	
5	GND		PWR	
6	Lane 1 (-)		LVDS	
7	Lane 2 (+)		LVDS	
8	GND		PWR	
9	Lane 2 (-)		LVDS	
10	Lane 3 (+)		LVDS	
11	GND		PWR	
12	Lane 3 (-)		LVDS	
13	Config. 1	Aux or DDC selection	I	Internally pull down (1 MΩ) Aux channel on pin 15/17 selected as default (if NC) DDC channel on pin 15/17, if HDMI adapter used (3.3V)
14	Config. 2	NC	O	Connected to GND (internally)
15	Aux+	Aux Channel (+) or DDC Clk		AUX (+) channel used by DP, DCC CLK used by HDMI
16	GND		PWR	
17	Aux-	Aux Channel (-) or DDC Data		AUX (-) channel used by DP DDC Data used by HDMI
18	Hot Plug		I	Internally pull down (100 KΩ)
19	Return		PWR	Same as GND
20	3.3 V		PWR	Fused by 1.5 A resettable PTC fuse

7.2. Ethernet Connectors (J5, J8 and J21)

The mITX-SKL-H supports up to four channels of 10/100/1000 Mbit Ethernet:

- ETH1 (J21) is based on Intel® Jacksonville i219LM Gigabit PHY with AMT 9.0 support
- ETH2 (J5), ETH3 (J8) and ETH4 (J8) are based on Intel® Pearsonville i211AT PCI Express controller

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100 MB and Category 5E, 6 or 6E with 1 Gbit LAN networks.

Ethernet connectors can be mounted as follows:

- Ethernet ETH1/ LAN1 (connector J21) is mounted together with USB Ports 1 and 2
- Ethernet ETH2/LAN2 (connector J5) is mounted together with USB Ports 4 and 3
- Ethernet ETH3 and Ethernet ETH4 (connector J8) are mounted together

All connectors support activity and link LEDs

Figure 8: Ethernet Connector with LED Flashing Communication

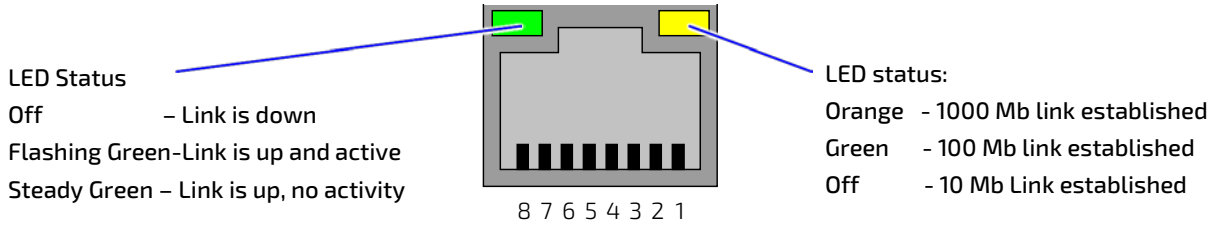


Table 6: Pin Assignment (RJ45) LAN Connectors (J5, J8, J21)

Pin	Signal	Type	Ioh / Iol	Note
1	MDI0+			
2	MDI0-			
3	MDI1+			
4	MDI2+			
5	MDI2-			
6	MDI1-			
7	MDI3+			
8	MDI3-			

'MDI' – media dependent Interface

Signal Description

Signal	Description
MDI0+ / MDI0-	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI1+ / MDI1-	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI2+ / MDI2-	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDI3+ / MDI3-	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair.In MDI crossover mode, this pair acts as the BI_DC+/- pair.

7.3. USB Connectors (I/O Area)

The mITX-SKL-H contains an xHCI (Enhanced Host Controller Interface) controller that supports six USB 2.0 ports allowing data transfers up to 480 Mb/s.

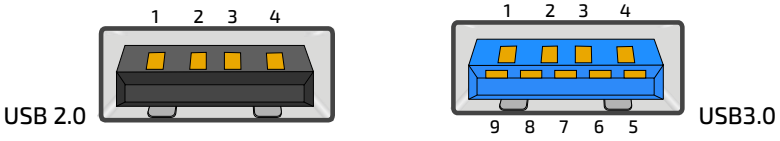
The XHCI controller supports up to four USB 3.0 ports allowing data transfers up to 5 Gb/s. Two of the USB 3.0 ports are shared with two of the USB 2.0 ports (USB1 – USB2).

Not all USB 2.0 and USB 3.0 ports are physically connected to the board.
USB 3.0 ports are backward compatible with USB 2.0.

The following USB connectors are available in the I/O area of the connector panel:

- USB 2.0/3.0 Ports 1, 2, are supplied on the combined 2 x USB and LAN connectors (J21)
- USB 2.0 Ports 3, 4 are supplied on the combined 2x USB and LAN connector (J5)

Figure 9: USB 2.0 / USB 3.0 sockets



7.3.1. USB Port 1 and USB Port 2 (J21)

USB port 1 and 2 supports USB 3.0/USB 2.0 and are located on the stacked USB/LAN connector J21.

Table 7: Pin Assignment USB Port 1 and USB Port 2 (J21)

Pin	Signal	Type	Note
Top			
18	Tx3+	IO	USB 3.0 Tx. Differential Pair (+)
17	TX3-	IO	USB 3.0 Tx. Differential Pair (-)
16	GND	PWR	
15	RX3+	IO	USB 3.0 Rx. Differential Pair (+)
14	RX3-	IO	USB 3.0 Rx. Differential Pair (-)
13	GND-	PWR	
12	D3+	IO	USB 2.0 Differential Pair (+)
11	D3-	IO	USB 2.0 Differential Pair (-)
10	VBus	PWR	+5 V Supply for USB device
Bottom			
9	Tx2+	IO	USB 3.0 Tx. Differential Pair (+)
8	TX2-	IO	USB 3.0 Tx. Differential Pair (-)
7	GND	PWR	
6	RX2+	IO	USB 3.0 Rx. Differential Pair (+)
5	RX2-	IO	USB 3.0 Rx. Differential Pair (-)
4	GND-	PWR	
3	D2+	IO	USB 2.0 Differential Pair (+)
2	D2-	IO	USB 2.0 Differential Pair (-)
1	VBus	PWR	+5 V Supply for USB device

Signal Description

Signal	Description
TXn+, TXn-, RXn+, TXn-, Dn+, Dn-	Differential pair works as serial differential receive/transmit data lines. (n= 2,3)
VBus	5 V supply for external devices. VBUS is supplied during power-down to allow wakeup on USB device activity. Protected by a 1A current limiting IC covering each of the USB port.

7.3.2. USB Port 3 and USB Port 4 (J5)

USB port 3 and USB port 4 support USB2.0 and are located on the stacked USB/LAN connector J5.

Table 8: Pin Assignment USB Port 3 and USB Port 4 (J5)

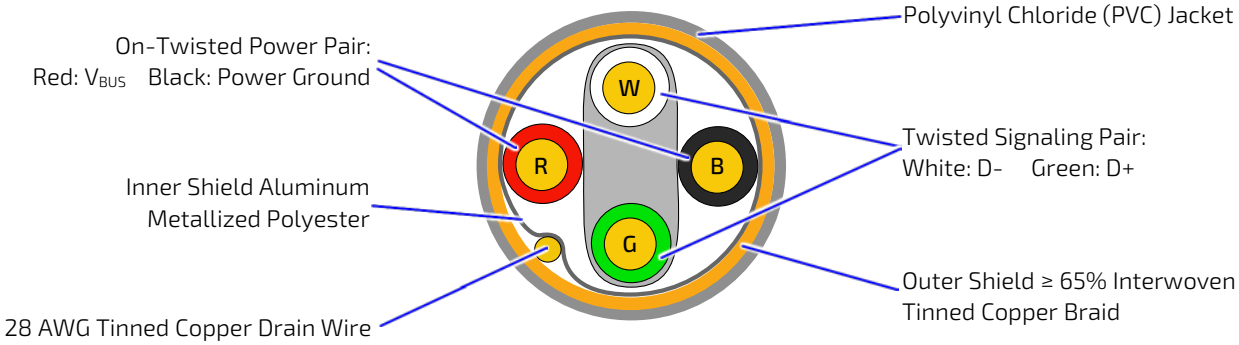
Pin	Signal	Type	Note
Top			
8	GND-	PWR	
7	D6+	IO	USB 2.0 differential pair (+)
6	D6-	IO	USB 2.0 differential pair (-)
5	VBus	PWR	
Bottom			
4	GND-	PWR	
3	D7+	IO	USB 2.0 differential pair (+)
2	D7-	IO	USB 2.0 differential pair (-)
1	VBus	PWR	

Signal Description

Signal	Description
Dn+, Dn-	Differential pair works as serial differential receive/transmit data lines. (n= 6,7)
VBus	5 V supply for external devices. VBUS is supplied during power-down to allow wakeup on USB device activity. Protected by a 1A current limiting IC covering each of the USB port.

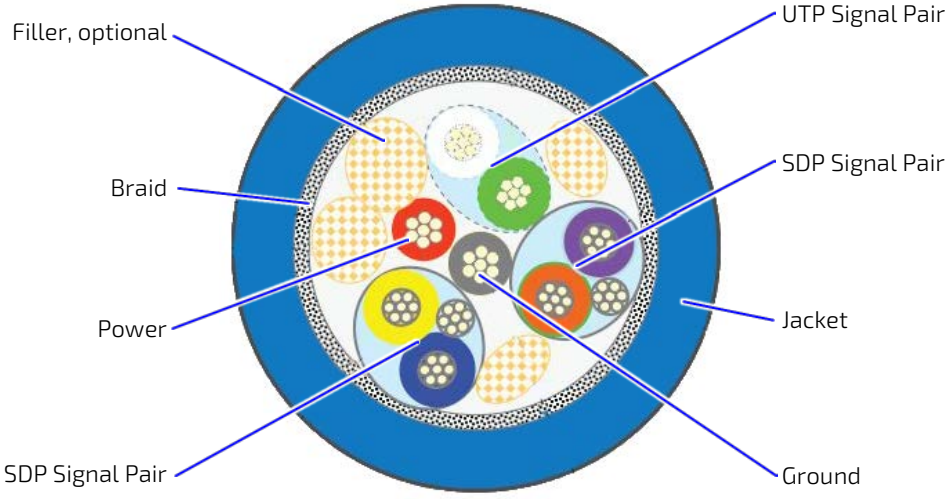
For USB2.0 cabling it is required to use only HiSpeed USB cable, specified in USB2.0 standard:

USB 2.0 High Speed Cable



For USB3.0 cabling it is required to use only HiSpeed USB cable, specified in USB3.0 standard:

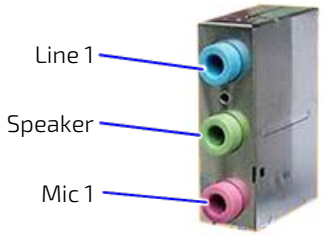
USB 3.0 High Speed Cable



7.4. Audio Jack Connector (J6)

The mITX-SKL-H provides audio output, line-in and microphone signals via a 3-pin audio Jack connector on the connector panel.

Figure 10: Audio Jack Connectors



J6

Corresponding Audio Jack

Table 9: Pin Assignment J6, Top (Line 1, Blue)

Pin Designation	Signal	Type	Note
Tip	LINE1-IN-L	IA	1.6 V_{RMS}, 47 KΩ
Ring	LINE1-IN-R	IA	1.6 V_{RMS}, 47 KΩ
Sleeve	GND	PWR	

Table 10: Pin Assignment J6, Center (Speaker, Green)

Pin Designation	Signal	Type	Note
Tip	FRONT-OUT-L	OA	For headphone, max 1.0 V_{RMS}
Ring	FRONT-OUT-R	OA	For headphone, max 1.0 V_{RMS}
Sleeve	GND	PWR	

Table 11: Pin Assignment J6, Bottom (Mic1, Pink)

Pin Designation	Signal	Type	Note
Tip	MIC1-L	IA	1.6 V_{RMS}, 47 KΩ
Ring	MIC1-R	IA	1.6 V_{RMS}, 47 KΩ
Sleeve	GND	PWR	

Signal Description

Signal	Description	Note
LINE1_IN_L	Line-in left	
LINE1_IN_R	Line-in right	
FRONT-OUT-L	Speaker out left	Shared with J29 pin connector
FRONT-OUT-R	Speaker out right	Shared with J29 pin connector
MIC1-L	Microphone in left	
MIC1-R	Microphone in right	

7.5. Power Connector DC Jack (J32)

The mITX-SKL-H is designed to be supplied from a DC jack (J32). For more information on the input tolerance of the +12 V and +24 V DC jack, see Chapter 4.8 Power Consumption.

The mITX-SKL-H can also be power by a standard 4-pin ATX+12 V supply, for more information see Chapter 8.1 Power Connector 4-Pin ATX+12 V (J31).

NOTICE

Hot plugging of the power connectors is not allowed. Hot plugging might damage the board.
When connecting to the motherboard, turn off main supply to make sure all the power lines are turned off.

Table 12: Pin Assignment DC Jack (J32)

Pin	Signal	Type	Note
1	+12 V to +24 V	PWR	
2	SIG	O	NC
3	+12 V to +24 V	PWR	
4	GND	PWR	
5	GND	PWR	
S1	Shield	PWR	SHIELD and GND are electrically connected
S2	Shield	PWR	SHIELD and GND are electrically connected
S3	Shield	PWR	SHIELD and GND are electrically connected

Signal Description

Signal	Description
Shield	SHIELD and GND are electrically connected
GND	Power Supply ground signal

⚠CAUTION

The board can be supplied via the power supply (AC/DC adapter) plugged into the DCpower jack. Such adapters have usually no connection to protective earth. Consequently, the potential of the conductive parts on the board may drift. If a human touches such a part, this may lead to an electric shock. The board must be grounded separately, if the unit is supplied via power jack.

NOTICE

Only connect to a power supply delivering the specified input rating and complying with the requirements of Safety Extra Low Voltage (SELV) and Limited Power Source (L.P.S.) of IEC 60950-1 and the Energy sources (ES1) of IEC 62368-1.
For more information, see Table 3: Electrical Specification.

8/ Internal Connectors

8.1. Power Connector 4-Pin ATX+12 V (J31)

The mITX-SKL-H is designed to be supplied from a standard 4-pin ATX+12 V supply or an DC jack

For more information see, Chapter 4.8 Power Consumption, or refer to the ATX Specification version 2.2.

NOTICE

Hot plugging of the power connectors is not allowed. Hot plugging might damage the board.

When connecting to the motherboard, turn off the main supply to make sure all the power lines are turned off.

Figure 11: 4-Pin ATX +12 V Power Connector

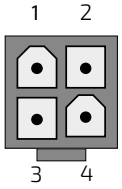


Table 13: Pin Assignment 4-Pin ATX 12 V Power Connector (J31)

Pin	Signal	Type	Note
1	GND	PWR	
2	GND	PWR	
3	+12 V to +24 V	PWR	+24 V can be supplied to 4-pin ATX 12 V connector
4	+12 V to +24 V	PWR	+24 V can be supplied to 4-pin ATX 12 V connector

Signal Description

Signal	Description
GND	Power Supply ground signal

NOTICE

Only connect to a power supply delivering the specified input rating and complying with the requirements of Safety Extra Low Voltage (SELV) and Limited Power Source (L.P.S.) of IEC 60950-1 and the Energy sources (ES1) of IEC 62368-1.

For more information, see Table 3: Electrical Specification.

8.2. Fan Connectors (J33, J34)

The system fan connector (J34) can be used to power, control and monitor a fan for chassis ventilation. The CPU fan connector (J33) is used for the connection of the fan for the CPU. The 4-pin connector is recommended for driving a 4-wire type fan, in order to implement fan speed control. 3-wire fan support is also possible, but fan speed control is not integrated.

Figure 12: Fan Connector

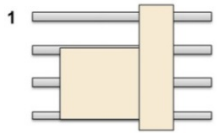


Table 14: Pin Assignment 4-Pin Fan Support Mode

Pin	Signal	Description	Type
1	GND	Ground	PWR
2	12 V	Power +12 V	PWR
3	TACHO	Tacho signal	I
4	PWM	PWM Output	O-3.3

Table 15: Pin Assignment 3-Pin Fan Support Mode

Pin	Signal	Description	Type
1	GND	Ground	PWR
2	12 V	Power +12 V	PWR
3	TACHO	Tacho signal	I
4	NC	NC	

Signal Description

Signal	Description	Type
GND	Power Supply GND signal	PWR
12 V	+12 V supply for fan. A maximum of 600 mA can be supplied from this pin.	PWR
TACHO	Tacho input signal from the fan, for rotation speed supervision RPM (Rotations Per Minute). The signal shall be generated by an open collector transistor or similar. A 4.7 Ω pull-up resistor to +12 V is on-board. The signal has to be pulsed and the on-board circuit is prepared for two pulses per rotation.	I
PWM	PWM output signal for FAN speed control	O

8.3. SATA (Serial ATA) Disk Interfaces (J10, J11, J12, J13)

The mITX-SKL-H supports an integrated SATA host controller (PCH in the CM236 chipset) that supports independent DMA operation on six ports. One device can be installed on each port for a maximum of six SATA devices via four SATA connectors, one mSATA connector and one M.2 SATA connector. A point-to-point interface (SATA cable) is used for host to device connections. All SATA ports support data transfer rates of up to 6.0 Gb/s, 3.0 Gb/s, and 1.5 Gb/s.

Before installing OS on a SATA drive make sure the drive is not a former member of a RAID system. If this is the case, some hidden data on the disk must be erased. To do this, connect two SATA drives and select RAID in BIOS. Save settings and select <Ctrl> <I> while booting to enter the RAID setup menu. Now the hidden RAID data will be erased from the selected SATA drive.

Supported SATA features:

- AHCI (Advanced Host Controller Interface) 1.3 and 1.3.1
- 2 to 4-drive RAID 0 (data striping)
- 2-drive RAID 1 (data mirroring)
- 3 to 4-drive RAID 5 (block-level striping with parity)
- 4-drive RAID 10 (data striping and mirroring)
- 2 to 4-drive matrix RAID, different parts of a single drive can be assigned to different RAID devices
- NCQ (Native Command Queuing). NCQ is for faster data access
- Swap bay support (not supported on mSATA)
- Intel® Rapid Recover Technology
- Intel® Smart Response Technology

Figure 13: SATA Connector

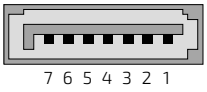


Table 16: Pin Assignment SATA1 (J10), SATA2 (J12), SATA3 (J11) and SATA4 (J13) Connectors:

Pin	Signal	Type	Ioh / Iol	Note
1	GND	PWR		
2	SATA# TX+			
3	SATA# TX-			
4	GND	PWR		
5	SATA# RX-			
6	SATA# RX+			
7	GND	PWR		

Signal Description

Signal	Description
SATA# RX+ / RX-	Host receiver differential signal pair
SATA# TX+ / TX-	Host transmitter differential signal pair
GND	Power Supply GND signal

"#" specifies 2, 3, 6 or 7 depending on SATA port.

Available Cable Kit

PN 821035 Cable SATA 500 mm

8.4. USB 3.0 Internal Connector (J3)

The following mITX-SKL-H USB ports are available on internal connectors:

- USB 3.0 Port 5 and 6 on the internal USB 3.0 connector (J3)
- USB 2.0 Port 7 and 8 are available on the internal FRONT PANEL connector (J27)

Table 17: Pin Assignment USB 3.0 Internal Connector (J3)

Pin	Signal	Type	Ioh / Iol	Note
1	V_VBUS	PWR		
2	RX5-			USB 3.0
3	RX5+			USB 3.0
4	GND	PWR		
5	TX5-			USB 3.0
6	TX5+			USB 3.0
7	GND	PWR		
8	D5-			USB 2.0
9	D5+			USB 2.0
10	NC			
11	D4+			USB 2.0
12	D4-			USB 2.0
13	GND	PWR		
14	TX4+			USB 3.0
15	TX4-			USB 3.0
16	GND	PWR		
17	RX4+			USB 3.0
18	RX4-			USB 3.0
19	V_VBUS	PWR		
20	KEY(NC)			

Signal Description

Signal	Description
V_VBUS	+5V Supply for USB Device
RX#+/-	USB 3.0 receiver differential signal pair
TX#+/-	USB 3.0 transmitter differential signal pair
D#+/-	USB 2.0 differential signal pair
GND	Power Supply GND signal

8.5. Headphone/Speaker Connector (J29)

The mITX-SKL-H headphone interface is available through the 4-pin connector (J29). This output is shared with the speaker audio jack connector (J6, green).

Figure 14: Speaker Connector

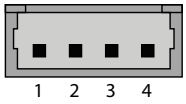


Table 18: Pin Assignment Speaker Connector (J29)

Pin	Signal	Type	Note
1	GND	PWR	
2	HPOUT-L	AO	
3	GND	PWR	
4	HPOUT-R	AO	

Signal Description

Signal	Description
HPOUT-L	Headphone output left
HPOUT-R	Headphone output right
GND	Power Supply GND signal

8.6. SPDIF-OUT Connector (J30)

The mITX-SKL-H digital audio interface (electrical SPDIF-Out) is available through the 2-pin connector (J33) and can be used to implement eight (7.1) High Definition audio channels. The audio interface is based on a high fidelity 8-channel HD audio codec that is compatible with the Intel HD Audio specification and provides:

- Stereo 24-bit resolution
- Up to 192 kHz sample rate for DACs/ADCs
- Maximum Signal-to-Noise Ratio (SNR) of 90 dB
- 16/20/24-bit S/PDIF TX outputs supporting 48 K/96 K/44.1 K/88.2 KHz sample rates

Figure 15: SPDIF-OUT Connector

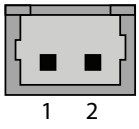


Table 19: Pin Assignment SPDIF-OUT Connector (J30)

Pin	Signal	Type	Note
1	SPDIF_OUT	O-3.3	
2	GND	PWR	

Signal Description

Signal	Description
SPDIF_OUT	Sony/Philips Digital Interface (SPDIF) audio output signal
GND	Power Supply GND signal

8.7. Front Panel Connector (FRONTPNL) (J27)

Figure 16: Front Panel Connector

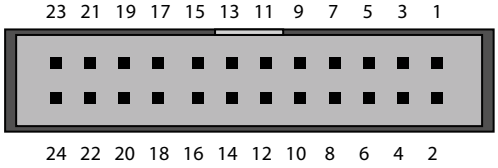


Table 20: Pin Assignment Front Panel Connector (J27)

Pin	Signal	Type	Ioh / Iol	Pull U / D	Note
1	VBUS	PWR			
2	VBUS	PWR			
3	USB2-D9-				USB 2.0
4	USB2-D10-				USB 2.0
5	USB2-D9+				USB 2.0
6	USB2-D10+				USB 2.0
7	GND	PWR			
8	GND	PWR			
9	NC	NC			
10	LINE2-L				
11	+5 V	PWR			
12	+5 V	PWR			
13	SATA_LED#	O	25 / 25 mA		
14	SUS_LED	O	7 mA		
15	GND	PWR			
16	PWRBTN_IN#	I		1.1 KΩ	
17	RSTIN#	I		4.7 KΩ	
18	GND	PWR			
19	SB3V3	PWR			
20	LINE2-R				
21	AGND	PWR			
22	AGND	PWR			
23	MIC2-L	AI			
24	MIC2-R	AI			

Signal Description

Signal	Description
VBUS	5 V supply for external devices. Standby 5 V is supplied during power down to allow wakeup on USB device activity. Protected by active power switch 1 A fuse for each USB port.
USB2_D#+/ D#-	Universal Serial Bus Differentials: Bus Data/Address/Command Bus
+5 V	Maximum load per pin is 1 A (using IDC connector) or 2 A (using crimp terminals)
SATA_LED#	SATA Activity LED (active low signal). 3.3 V output when passive open drain output
SUS_LED	Suspend Mode LED (active high signal) 3.3 V push-pull output
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX / BTX PSU and boot the board

Signal	Description
RSTIN#	Reset input. When pulled low for a minimum 16 ms, the reset process will be initiated. The reset process continues, even though the reset input is kept low.
LINE2	Line2 is second stereo line signals. (Line 2 does not have Jack detection capabilities.)
MIC2	MIC2 is second stereo microphone input. (MIC2 does not have Jack detection capabilities.)
SB3V3	Standby 3.3 V
AGND	Analogue GND for audio
GND	Power Supply GND signal

Available Cable Kit

PN 821042 Cable Front Panel Open-End, 300 mm

8.8. Serial COM1 Port (J22)

The mITX-SKL-H supports one RS232 serial port.

Figure 17: Serial COM 1

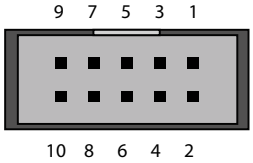


Table 21: Pin Assignment Serial COM1 Port (J22)

Pin	Signal	Type	Ioh / Iol	Pull U / D	Note
1	DCD	I			
2	DSR	I			
3	RxD	I			
4	RTS	O			
5	TxD	O			
6	CTS	I			
7	DTR	O			
8	RI	I			
9	GND	PWR			
10	5V	PWR			The COM1 5 V supply is fused with common 1.5 A resettable fuse.

Signal Description

Signal	Description
TxD	Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12 V) on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Received Data, receives data from the communications link.
DTR	Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that the modem etc. is ready to establish a communications link.
RTS	Request To Send, indicates to the modem etc. that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a ringing signal from the telephone line.
GND	Power Supply GND signal

DB9 adapter cables are available to implement standard COM ports on chassis.

Available Cable Kit (DB9 adapter cables)

PN 821017 - 100 mm or PN 821016 - 200 mm

8.9. Serial COM2 Port (J35)

The mITX-SKL-H supports one RS422/485 serial port. Full-duplex and half-duplex can be configured from the BIOS menu.

Table 22: Pin Assignment Serial COM 2 Port (J35)

Pin	Signal	Type	Ioh / Iol	Pull U / D	Note
1	RS485_TX1-	O			Data (-) in half-duplex mode
2	RS485_RX1+	I			
3	RS485_TX1+	O			Data (+) in half-duplex mode
4	RS485_RX1-	I			
5	GND	PWR			

Signal Description

Signal	Description
RS485_TX1+/-	Transmitted Data differential pair sends data to the communications link.
RS485_RX1+/-	Received Data differential pair receives data from the communications link.
GND	Power Supply GND signal

8.10. LVDS FLAT PANEL CONNECTOR (J7)

The mITX-SKL-H LVDS connector is based on a 40-pin connector type Samtec SHF-120-10-F-D.

Figure 18: LVDS Connector

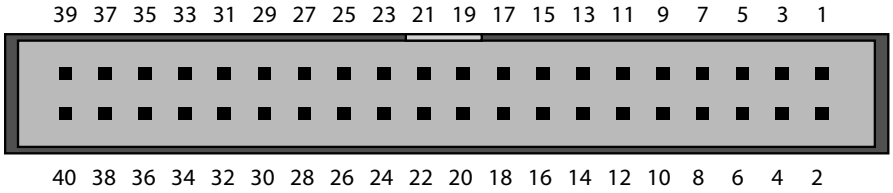


Table 23: Pin Assignment LVDS Flat Panel Connector (J7)

Pin	Signal	Type	Note
1	+12 V	PWR	Max. 0.5 A
2	+12 V	PWR	Max. 0.5 A
3	+12 V	PWR	Max. 0.5 A
4	+12 V	PWR	Max. 0.5 A
5	+12 V	PWR	Max. 0.5 A
6	GND	PWR	
7	+5 V	PWR	Max. 0.5 A
8	GND	PWR	
9	LCDVCC	PWR	Max. 0.5 A
10	LCDVCC	PWR	Max. 0.5 A
11	DDC CLK	OT	2.2 KΩ, 3.3 V
12	DDC DATA	OT	2.2 KΩ, 3.3 V
13	BKLTCTL	OT	3.3 V level
14	VDD ENABLE	OT	3.3 V level
15	BKLTEN#	OT	3.3 V level
16	GND	PWR	
17	LVDS A0-	LVDS	
18	LVDS A0+	LVDS	
19	LVDS A1-	LVDS	
20	LVDS A1+	LVDS	
21	LVDS A2-	LVDS	
22	LVDS A2+	LVDS	
23	LVDS ACLK-	LVDS	
24	LVDS ACLK+	LVDS	
25	LVDS A3-	LVDS	
26	LVDS A3+	LVDS	
27	GND	PWR	
28	GND	PWR	
29	LVDS B0-	LVDS	
30	LVDS B0+	LVDS	
31	LVDS B1-	LVDS	
32	LVDS B1+	LVDS	

Pin	Signal	Type	Note
33	LVDS B2-	LVDS	
34	LVDS B2+	LVDS	
35	LVDS BCLK-	LVDS	
36	LVDS BCLK+	LVDS	
37	LVDS B3-	LVDS	
38	LVDS B3+	LVDS	
39	GND	PWR	
40	GND	PWR	

The on-board LVDS connector supports single and dual channel, 18/24 bit SPWG panels, up to a resolution of 1600x1200 px or 1920x1080 px and with limited frame rate up to 1920x1200 px.

Signal Description

Signal	Description
LVDS A0…A3	LVDS A Channel data
LVDS ACLK	LVDS A Channel clock
LVDS B0…B3	LVDS B Channel data
LVDS BCLK	LVDS B Channel clock
BKLTCTL	Backlight control, PWM signal to implement voltage in the range 0 V-3.3 V.
BKLTEN#	Backlight enable signal (active low)
VDD ENABLE	Output display enable
LCDVCC	VCC supply to the display. 5 V or 3.3 V (1 A maximum) selected in BIOS setup menu. Power sequencing depends on LVDS panel selection.
DDC CLK	DDC Channel Clock
GND	Power Supply GND signal

Windows API will be available to operate the BKLTCTL signal. Some inverters have a limited voltage range 0 V - 2.5 V for this signal: If the voltage is > 2.5 V the inverter might latch up. Some inverters generate noise on the BKLTCTL signal, causing LVDS transmission to fail (corrupted picture on the display). By adding a 1 KΩ resistor in series with this signal, mounted at the inverter end of the cable kit, noise is limited and the picture is stable.

If the Backlight Enable is required to be active high then check the BIOS setup menus.

8.11. Feature Connector (J26)

Figure 19: Feature Connector

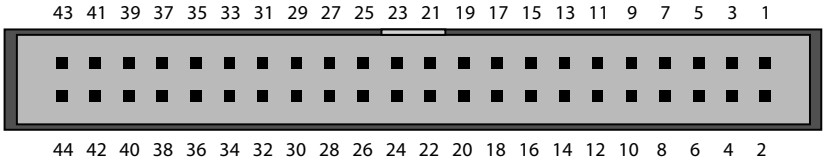


Table 24: Pin Assignment Feature Connector (J26)

Pin	Signal	Type	Ioh / Iol	Pull U / D	Note
1	INTRUDER#	I		2 MΩ / …	Pull-up to on-board Battery
2	SMBC		/4 mA	10 KΩ /…	Pull-up to +3.3 V dual (+3.3 V or SB 3.3 V)
3	S4#	O	25 mA/25 mA		
4	SMBD		/4 mA	10 KΩ /…	Pull-up to +3.3 V dual (+3.3 V or SB 3.3 V)
5	PWR_OK	O	25 mA/25 mA		
6	EXT_BAT	PWR			
7	NC				
8	NC				
9	SB3V3	PWR			
10	SB5V	PWR			
11	GPIO0	IOT			
12	GPIO1	IOT			
13	GPIO2	IOT			
14	GPIO3	IOT			
15	GPIO4	IOT			
16	GPIO5	IOT			
17	GPIO6	IOT			
18	GPIO7	IOT			
19	GND	PWR			
20	GND	PWR			
21	GPIO8	I			
22	GPIO9	I			
23	GPIO10	I			
24	GPIO11	I			
25	GPIO12	I			
26	GPIO13	IOT			
27	GPIO14	IOT			
28	GPIO15	IOT			
29	GPIO16	IOT			
30	GPIO17	IOT			
31	GND	PWR			
32	GND	PWR			
33	EGCLK	O	8 /8 mA		
34	EGCS#	O	8 /8 mA		

Pin	Signal	Type	Ioh / Iol	Pull U / D	Note
35	EGAD		8 /8 mA		
36	TMA0	O			
37	+12 V	PWR			
38	GND	PWR			
39	NC				
40	NC				
41	GND	PWR			
42	GND	PWR			
43	GND	PWR			
44	S3#	O	25 /25 mA		

Signal Description

Signal	Description
INTRUDER#	Also known as, CASE OPEN. Used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the intruder switch is not required.
SMBC	SMBus clock signal
SMBD	SMBus data signal
S3#	S3 sleep mode, active low output, optionally used to deactivate external system.
S4#	S4 sleep mode, active low output, optionally used to deactivate external system.
PWR_OK	Power OK, signal is high if no power failures are detected. (This is not the same as the P_OK signal generated by ATX PSU).
EXT_BAT	(EXTernal BATtery) option for connecting + terminal of an external primary cell battery (2.5 V - 3.47 V) (– terminal connected to GND). The external battery is protected against charging and can be used with or without the on-board battery installed.
SB3V3	Maximum load is 0.75 A (1.5 A < 1 sec.)
SB5 V	StandBy +5 V supply.
GPIO0..17	General Purpose Inputs/Output - These signals may be controlled or monitored with the use of the KT-API-V2 (Application Programming Interface).
EGCLK	Extend GPIO clock signal
EGAD	Extend GPIO address data signal
EGCS#	Extend GPIO chip select signal, active low
TMA0	Timer output
+12 V	Maximum load is 0.75 A (1.5 A < 1 sec.)
GND	Power Supply GND signal

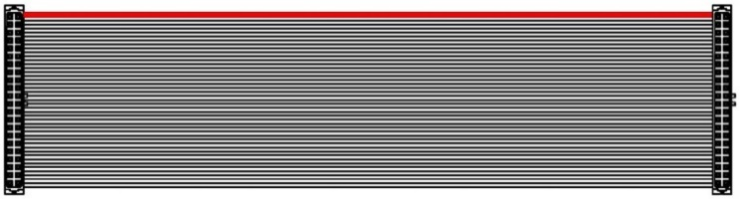
The GPIOs are controlled via the ITE IT8528E Embedded Controller. Each GPIO has 100 pF to ground, clamping diode to 3.3 V and has multiplexed functionality. Some pins can be DAC (Digital to Analogue Converter) output, PWM (Pulse Width Modulated) signal output, ADC (Analogue to Digital Converter) input, TMRI (Timer Counter Input), WUI (Wake Up Input), RI (Ring Indicator Input) or some special function.

Signal Description IT8528E Embedded Controller

Signal	IT8528E Pin Name	Type	Description
GPIO0	DAC0/GPJ0	AO/IOS	

Signal	IT8528E Pin Name	Type	Description
GPIO1	DAC1/GPJ1	AO/IOS	
GPIO2	DAC2/GPJ2	AO/IOS	
GPIO3	DAC3/GPJ3	AO/IOS	
GPIO4	PWM2/GPA2	O8/IOS	
GPIO5	PWM3/GPA3	O8/IOS	
GPIO6	PWM4/GPA4	O8/IOS	
GPIO7	PWM5/GPA5	O8/IOS	
GPIO8	ADC0/GPI0	AI/IS	
GPIO9	ADC1/GPI1	AI/IS	
GPI10	ADC2/GPI2	AI/IS	
GPI11	ADC3/GPI3	AI/IS	
GPI12	ADC4/WUI28/GPI4	AI/IS/IS	
GPI13	RI1#/WUI0/GPD0	IS/IS/IOS	
GPI14	RI2#/WUI1/GPD1	IS/IS/IOS	
GPI15	TMRI0/WUI2/GPC4	IS/IS/IOS	
GPI16	TMRI1/WUI3/GPC6	IS/IS/IOS	
GPI17	L80HLAT/BAO/WUI24/GPE0	O4/O4/IS/IOS	

Available Cable Kit:



PN 1052-5885 Cable, Feature 44pol 1 to1, 300 mm

8.12. SPI Connector (J9)

The SPI Connector is normally not used, it is for Kontron use. In case of BIOS corruption, it can be used to recover the BIOS SPI chip via an external SPI Flash IC Programmer.

Figure 20: SPI Connector 12-Pin Connector

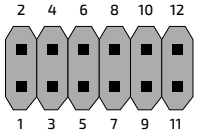


Table 25: Pin Assignment SPI Connector (J9)

Pin	Signal	Type	Ioh / Iol	Pull U / D	Note
1	CLK				
2	SB3V3	PWR			
3	CS0#	I			
4	ADDIN	IO		- / 10 KΩ	
5	V_SPI			10 KΩ /-	
6	NC				
7	MOSI	IO		10 KΩ /-	
8	ISOLATE#	IO		100 KΩ	
9	MISO	IO			
10	GND	PWR			
11	SPI_IO2_#WP	IO		1 KΩ/-	
12	SPI_IO3_#HOLD	IO		1 KΩ	

Signal Description

Signal	Description
CLK	Serial clock
V_SPI	3.3 V Standby voltage power line. Normal output power, but when the motherboard is turned off, the on-board SPI Flash can be a 3.3 V power sourced via this pin.
SB3V3	3.3 V Standby voltage power line. Normal output power, but when the motherboard is turned off, the on-board SPI Flash can be 3.3 V power sourced via this pin.
CS0#	CS0# Chip Select 0, active low
ADDIN	ADDIN input signal must be NC
MOSI	Master Output, Slave Input
ISOLATE#	The ISOLATE# input, active low, is normally NC, but must be connected to GND when programming the SPI flash. The power supply to the motherboard must be turned off when loading SPI flash.The pull up resistor is connected via diode to 5 V Standby.
MISO	Master Input, Slave Output
SPI_IO2_#WP	SPI Data I/O: A bidirectional signal used to support dual IO fast read, quad IO fast read and quad output fast read modes. The signal is not used in dual output fast read mode.
SPI_IO3_#HOLD	SPI Data I/O: A bidirectional signal used to support dual IO fast read, quad IO fast read and quad output fast read modes. The signal is not used in dual output fast read mode.
GND	Power Supply GND signal

8.13. SPI Connector for External Fast GPIO Expander (J36)

The mITX-SKL-H supports a 6-pin external SPI for external fast General Purpose Input/Output (GPIO) support. The configurable input output pins are implemented to support the mITX –SKL-H with clock, chip select and two configurable signal options (Master to Slave or Slave to Master).

Table 26: Pin Assignment SPI connector for Fast GPIO Expander (J36)

Pin	Signal	Type	Ioh / Iol	Pull U / D	Note
1	SB3V3	PWR			
2	SPI MOSI	I/O			
3	SPI MISO	I/O			
4	SPI CLK	O			
5	SPI CS#	O			
6	GND	PWR			

Signal Description

Signal	Description
SB3V3	3.3 V Standby voltage power line. Normal output power, but when the motherboard is turned off, the on-board SPI Flash connector can supply a 3.3 V power source via this pin
SPI MOSI	SPI signal (Master Out Slave In)
SPI MISO	SPI signal (Master In Slave Out)
SPI CLK	SPI signal (Clock)
SPI CS#	SPI signal (Chip Select)
GND	Power Supply ground signal

8.14. Switches and Jumpers

8.14.1. Always On Jumper Setting (J39)

The “Always On” jumper (J39) can be used to automatically power up the board.

The jumper has three pins. Pin 1-2 is the “Always On” position and not mounted is the default position. More information on setting the “Always On” Jumper (J39) can be found in the following table.

Figure 21: Always On Jumper

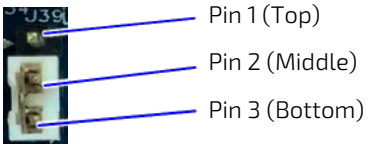


Table 27: Always On Jumper Description (J39)

J39 Position		Description
Pin 1-2	Pin 2-3	
X	-	Always On(Auto powers on the board when the external power supply is switched on)
-	X	Default position (Always On feature is disabled). It might be necessary to activate the power on button (PWRBTN_IN#) on the Front Panel connector (FRONTPNL) in order to switch on the board.
-	-	Same as the default position

“X” = Jumper set and “-“ = jumper not set

Don´t leave the jumper in position 1-2. If power is disconnected, the battery will fully deplete within a few weeks.

8.14.2. Clear CMOS Jumper (J37)

The "Clear CMOS" jumper (J37) can be used to reset the Real Time Clock (RTC) and drain the RTC well.

The jumper has one position: Pin 1-2 and not mounted (default position). More information on setting the "Clear CMOS" jumper can be found in the following table.

Table 28: Clear CMOS Jumper Description (J37)

J37 Position Pin 1-2	Description
X	Clear CMOS RTC content (Board does not boot with the jumper in this position)
-	Default position

"X" = Jumper set and "-" = jumper not set

Do not leave the jumper in position 1-2, otherwise if the power is disconnected, the battery will fully deplete within a few weeks.

8.14.3. Load BIOS Default Jumper (J38)

The "Load BIOS Default" jumper (J38) can be used to recover from incorrect BIOS settings. For example, an incorrect BIOS setting that causes the attached display not to turn on can be erased by this jumper. More information on setting the "Load BIOS Default" jumper can be found in the following table.

Table 29: Load BIOS Default Jumper Description (J38)

J38 Position Pin 1-2	Description
X	Loads default BIOS settings and erases the password (Board does not boot with the jumper in this position)
-	Default position

"X" = Jumper set and "-" = jumper not set

Do not leave the jumper in position 1-2, otherwise the board will always load the factory default on every power on and is not able to retain any user settings.

To load default BIOS settings and erase password:

1. Turn off power completely (no +12 V to +24 V supply).
2. Place the jumper to position 1-2.
3. Turn on power.
4. Motherboard beeps fast 20 times and turns off.
5. Turn off power.
6. Disconnect the jumper.
7. Turn on power, use the Power-On button (PWRBTN_IN#) if required to boot.

Motherboard might automatically reboot a few times. Wait until booting is completed.

8.15. Slot Connectors (PCIe, miniPCIe, SIM-Card and M.2)

The mITX-SKL-H supports the following slot connectors:

- 1 xPCIe x16 (16-lane) PCI Express port (J4)
- 1 x miniPCIe or mSATA, USB 2.0 (J17)
- 1x SIM-card socket (J20)
- 1x optional M.2 (J18)

8.15.1. PCI-Express x16 Connector (J4)

The mITX-SKL-H supports PCI express x 16 via slot J4 and supports PEG Bifurcation. PEG Bifurcation enables the PCI Express lanes to be divided into:

- 2x PCIe x8
- 1x PCIe x8 + 2x PCIe x4

For PEG Bifurcation a PCIe Riser Card with bifurcation and hardware modification is required.

Figure 22: Bifurcation Hardware Setup

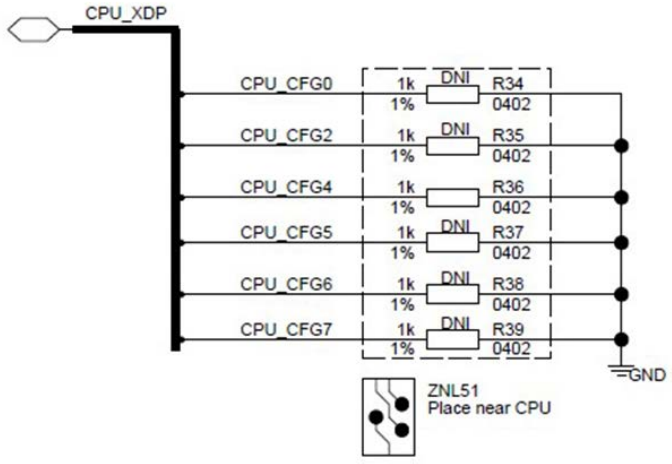


Table 30: CPU Strap Pin

Pin Name	Usage	Configuration
CFG[0]	Stall reset sequence after PCU, PLL lock until de-asserted	1 = Normal Operation; No stall (Default) 0 = Stall
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal	1 = Normal Operation (Default) 0 = Lane numbers reversed
CFG[4]	eDP enable	1 = Disabled (Default) 0 = Enabled
CFG[6:5]	PCI Express* Bifurcation	00 = 1 x8, 2 x4 PCI Express 01 = Reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express (Default)

Pin Name	Usage	Configuration
CFG[7]	PEG Training	1 = PEG Train immediately following RESET# de-assertion (Default) 0 = PEG Wait for BIOS for training
CFG[1], CFG [3] CFG[19:8]	Reserved configuration lanes	

The 16-lane (x16) PCI Express (J4) (PCIe 2.0 and PCIe 3.0) port can be used for external PCI Express cards inclusive graphics card. The maximum theoretical bandwidth using 16 lanes is 16 GB/s.

Table 31: Pin Assignment PCIe (x16) Slot Connector (J4)

	Side B Connector		Side A Connector	
Pin	Name	Description	Name	Description
1	+12V	+12 V power	NC	NC
2	+12V	+12 V power	+12V	+12 V power
3	+12V	+12 V power	+12V	+12 V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	NC	NC
6	SMBDAT	SMBus data	NC	NC
7	GND	Ground	NC	NC
8	+3V3	+3.3 V power	NC	NC
9	NC	NC	+3V3	+3.3 V power
10	SB3V3	3.3 V power	+3V3	+3.3 V power
11	WAKE#	Link Reactivation	RST#	Reset
Mechanical Key				
12	NC	NC	GND	Ground
13	GND	Ground	PCIE_x16CLK	Reference Clock Differential pair
14	PEG_TXP[0]	Transmitter Lane 0, Differential pair	PCIE_x16 CLK#	
15	PEG_TXN[0]		GND	Ground
16	GND	Ground	PEG_RXP[0]	Receiver Lane 0, Differential pair
17	CLKREQ	Clock request	PEG_RXN[0]	
18	GND	Ground	GND	Ground
19	PEG_TXP[1]	Transmitter Lane 1, Differential pair	NC	NC
20	PEG_TXN[1]		GND	Ground
21	GND	Ground	PEG_RXP[1]	Receiver Lane 1, Differential pair
22	GND	Ground	PEG_RXN[1]	
23	PEG_TXP[2]	Transmitter Lane 2, Differential pair	GND	Ground
24	PEG_TXN[2]		GND	Ground
25	GND	Ground	PEG_RXP[2]	Receiver Lane 2, Differential pair
26	GND	Ground	PEG_RXN[2]	
27	PEG_TXP[3]	Transmitter Lane 3, Differential pair	GND	Ground
28	PEG_TXN[3]		GND	Ground
29	GND	Ground	PEG_RXP[3]	Receiver Lane 3, Differential pair
30	NC	NC	PEG_RXN[3]	
31	CLKREQ	Clock request	GND	Ground

	Side B Connector		Side A Connector	
32	GND	Ground	NC	NC
33	PEG_TXP[4]	Transmitter Lane 4, Differential pair	NC	NC
34	PEG_TXN[4]		GND	Ground
35	GND	Ground	PEG_RXP[4]	Receiver Lane 4, Differential pair
36	GND	Ground	PEG_RXN[4]	
37	PEG_TXP[5]	Transmitter Lane 5, Differential pair	GND	Ground
38	PEG_TXN[5]		GND	Ground
39	GND	Ground	PEG_RXP[5]	Receiver Lane 5, Differential pair
40	GND	Ground	PEG_RXN[5]	
41	PEG_TXP[6]	Transmitter Lane 6, Differential pair	GND	Ground
42	PEG_TXN[6]		GND	Ground
43	GND	Ground	PEG_RXP[6]	Receiver Lane 6, Differential pair
44	GND	Ground	PEG_RXN[6]	
45	PEG_TXP[7]	Transmitter Lane 7, Differential pair	GND	Ground
46	PEG_TXN[7]		GND	Ground
47	GND	Ground	PEG_RXP[7]	Receiver Lane 7, Differential pair
48	CLKREQ	Clock request	PEG_RXN[7]	
49	GND	Ground	GND	Ground
50	PEG_TXP[8]	Transmitter Lane 8, Differential pair	NC	NC
51	PEG_TXN[8]		GND	Ground
52	GND	Ground	PEG_RXP[8]	Receiver Lane 8, Differential pair
53	GND	Ground	PEG_RXN[8]	
54	PEG_TXP[9]	Transmitter Lane 9, Differential pair	GND	Ground
55	PEG_TXN[9]		GND	Ground
56	GND	Ground	PEG_RXP[9]	Receiver Lane 9, Differential pair
57	GND	Ground	PEG_RXN[9]	
58	PEG_TXP[10]	Transmitter Lane 10, Differential pair	GND	Ground
59	PEG_TXN[10]		GND	Ground
60	GND	Ground	PEG_RXP[10]	Receiver Lane 10, Differential pair
61	GND	Ground	PEG_RXN[10]	
62	PEG_TXP[11]	Transmitter Lane 11, Differential pair	GND	Ground
63	PEG_TXN[11]		GND	Ground
64	GND	Ground	PEG_RXP[11]	Receiver Lane 11, Differential pair
65	GND	Ground	PEG_RXN[11]	
66	PEG_TXP[12]	Transmitter Lane 12, Differential pair	GND	Ground
67	PEG_TXN[12]		GND	Ground
68	GND	Ground	PEG_RXP[12]	Receiver Lane 12, Differential pair
69	GND	Ground	PEG_RXN[12]	
70	PEG_TXP[13]	Transmitter Lane 13, Differential pair	GND	Ground
71	PEG_TXN[13]		GND	Ground
72	GND	Ground	PEG_RXP[13]	Receiver Lane 13, Differential pair
73	GND	Ground	PEG_RXN[13]	
74	PEG_TXP[14]	Transmitter Lane 14,	GND	Ground

	Side B Connector		Side A Connector	
75	PEG_TXN[14]	Differential pair	GND	Ground
76	GND	Ground	PEG_RXP[14]	Receiver Lane 14, Differential pair
77	GND	Ground	PEG_RXN[14]	
78	PEG_TXP[15]	Transmitter Lane 15, Differential pair	GND	Ground
79	PEG_TXN[15]		GND	Ground
80	GND	Ground	PEG_RXP[15]	Receiver Lane 15, Differential pair
81	CLKREQ	Clock request	PEG_RXN[15]	
82	NC	NC	GND	Ground

CLKREQ is connected to GND on the motherboard.

8.15.2. miniPCIe, mSATA, USB2.0 (J17) and SIM-Card Support (J20)

The mITX-SKL-H supports either mPCIe or mSATA cards, and USB 2.0 via slot (J17). MicroSIM-cards are supported via slot (J20). The SIM-card socket makes it possible to use a 2G/3G-wireless modem in this mPCIe slot.

Table 32: Pin Assignment mPCIe with mSATA,/USB2.0 and SIM Card

Pin	Signal	Type	Ioh / Iol	Pull U / D	Note
1	WAKE#	O			
2	+3V3	PWR			
3	NC	NC			
4	GND	PWR			
5	NC	NC			
6	+1.5V	PWR			
7	CLKREQ#	O			10 KΩ pull-up to 3.3 V.
8	NC	PWR			
9	GND	PWR			
10	NC	NC			
11	PCIE_REFCLK5-	I			
12	NC	NC			
13	PCIE_REFCLK5+	I			
14	NC	NC			
15	GND	PWR			
16	NC	NC			
17	NC	NC			
18	GND	PWR			
19	NC	NC			
20	W_Disable#	I			10 KΩ pull-up to 3.3 V
21	GND	PWR			
22	RST#	I			

Pin	Signal	Type	Ioh / Iol	Pull U / D	Note
23	PCIE14/SATA_RX 1B-	O			
24	+3.3 V	PWR			
25	PCIE14/SATA_RX 1B+	O			
26	GND	PWR			
27	GND	PWR			
28	+1.5 V	PWR			
29	GND	PWR			
30	SMB_CLK	I			
31	PCIE14/SATA_TX 1B-	I			
32	SMB_DATA	IO			
33	PCIE14/SATA_TX 1B+	I			
34	GND	PWR			
35	GND	PWR			
36	USB_D8-	IO			
37	GND	PWR			
38	USB1_D8+	IO			
39	+3V3	PWR			
40	GND	PWR			
41	+3V3	PWR			
42	NC	NC			
43	MSATA_DET	O			10 KΩ pull-up to 3.3 V
44	NC	NC			
45	CL_CLK	I			
46	NC	NC			
47	CL_DATA	IO			
48	+1.5 V	PWR			
49	CL_RSTB	I			
50	GND	PWR			
51	W_Disable_N	NC			
52	+3V3	PWR			

8.15.3. M.2 (J18)

The mITX-SKL-H supports M.2 via one socket 3, M key, 2280 slot (J18). The M.2 specification enables four PCIe 3.0 lanes and one SATA 3.0 (6 Gb/s) to be exposed through the same slot. The M.2 option is only available for specific part numbers. The PCIe M.2 and SATA M.2 support the following BIOS depending on the class code options below:

M.2 SSD	Boot	Storage
PCIE M.2 SSD with NVME class code	Supported	Supported
PCIE M.2 SSD with AHCI class code	Not supported	Supported
SATA M.2 SSD	Supported	Supported

Table 33: Pin Assignment M.2 (J18)

Pin	Signal	Type	Note

Pin	Signal	Type	Note
1	M2_Config_3	O	
2	V_3V3_M2	PWR	
3	GND	PWR	
4	V_3V3_M2	PWR	
5	PCIE12_RX-	O	
6	NC		
7	PCIE12_RX+	O	
8	NC		
9	GND	PWR	
10	NC		
11	PCIE12_TX-	I	
12	V_3V3_M2	PWR	
13	PCIE12_TX+	I	
14	V_3V3_M2	PWR	
15	GND	PWR	
16	V_3V3_M2	PWR	
17	PCIE11_RX-	O	
18	V_3V3_M2	PWR	
19	PCIE11_RX+	O	
20	NC		
21	GND	PWR	
22	NC		
23	PCIE11_TX-	I	
24	NC		
25	PCIE11_TX+	I	
26	NC		
27	GND	PWR	
28	NC		
29	PCIE10_RX-	O	
30	NC		
31	PCIE0_RX+	O	
32	NC		
33	GND	PWR	
34	NC		
35	PCIE10_TX-	I	
36	NC		
37	PCIE10_TX+	I	
38	SSO_Deep_SLP	I	
39	GND	PWR	
40	NC		
41	PCIE9_SATA0A_RX-	O	
42	NC		
43	PCIE9_SATA0A_RX+	O	

Pin	Signal	Type	Note
44	NC		
45	GND	PWR	
46	NC		
47	PCIE9_SATA0A_TX-	I	
48	NC		
49	PCIE9_SATA0A_TX+	I	
50	PCH_PLT_RST_BUFF	I	
51	GND	PWR	
52	M2_CLKREQ	O	
53	M2_REFCLK6-	I	
54	PCH_WAKE	O	
55	M2_REFCLK6+	I	
56	NC		
57	GND	PWR	
58	NC		
59	Connector key (NC)		
60	Connector key (NC)		
61	Connector key (NC)		
62	Connector key (NC)		
63	Connector key (NC)		
64	Connector key (NC)		
65	Connector key (NC)		
66	Connector key (NC)		
67	NC		
68	SUSCLK	I	
69	M2_Config_1	O	
70	V_3V3_M2	PWR	
71	GND	PWR	
72	V_3V3_M2	PWR	
73	GND	PWR	
74	V_3V3_M2	PWR	
75	M2_Config_2	O	

8.16. SATA Power Connectors (J23, J24)

The SATA power connectors (J23) and (J24) can be used to power up SATA HDD and SSD that require input voltages of 12 V and/or 5 V.

Figure 23: SATA Power Connector

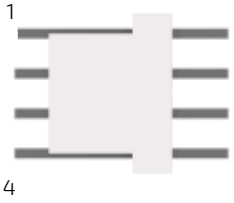


Table 34: Pin Assignment SATA Power Connectors (J23, J24)

Pin	Signal	Type	Note
1	5 V	PWR	Power +5 V
2	GND	PWR	Ground
3	GND	PWR	Ground
4	12 V	PWR	Power +12 V

Signal Description

Signal	Description
GND	Power Supply GND signal
12 V	+12 V supply for SATA HDD or SSD. A maximum of 550 mA can be supplied from this pin.
5 V	+5 V supply for SATA HDD or SSD. A maximum of 1000 mA can be supplied from this pin.

9/ On-Board Connectors & Mating Connector Types

The mating connectors/cables are connectors or cable kits that fit the on-board connector.
The Kontron cable kits marked with "*" are included in the "mITX-SKL-H Cable & Driver Kit" PN 826603.

Connector	On-Board Connectors		Mating Connectors/Cables	
	Manufact.	Type no.	Manufact.	Type no.
FANCPU, FANSYS (J33, J34)	Foxconn	HF2704E-M1	AMP	1375820-4 (4-pole)
	Molex	47053-1000	AMP	1375820-3 (3-pole)
SATA 1, 2, 3, 4 (J10, J12, J11, J13)	Lotes	ABA-SAT-010-K08	Molex	67489-8005
			Kontron	821035 (kit)
SATA Power 1,2 (J23, J24)	Molex	22-23-2041	Molex	22-01-2045
	TE Connectivity	640456-4	TE Connectivity	1375820-4
ATX +12V -4p (J31)	Molex	39-28-1043	Molex	39-01-2045
	Foxconn	HM3502E		
	Lotes	ABA-POW-003-K04		
DC Jack (J32)	Singatron	2DC1003-010111		
Headphone (J29)	Molex	53047-0410	Molex	51021-0400
LVDS (J7)	Samtec	SHF-120-01-L-D-SM-K-TR	Kontron	910000005
	Pinrex	53C-90-40GBE0	Kontron	821515 (kit) *
			Kontron	821155 (kit)
COM 1,(J22)	Foxconn	HL2205F	Molex	90635-1103
	Pinrex	510-90-10GB00	Kontron	821016 (kit)
	Cen Link	ZP91-014B1-10Y1	Kontron	821017 (kit) *
COM 2 (J35)	JST	B5B-PH-K-S(LF)(SN)(P)	JST	PHR-5
USB 2.0 (J27, FRONTPNL)	(See FRONTPNL)		Kontron	821401 (kit)
USB 3.0 (J3)	Foxconn	HLL2107-CBC2D-4H		
SPI Hardflash (J9)	Pinrex	210-92-06GB01		
SPI GPIO (J36)	Molex	53047-0610	Molex	51021-0600
SPDIF –OUT (J30)	Molex	53047-0210	Molex	51021-0200
FRONTPNL (J27)	Pinrex	510-80-24GB05	Molex	90635-1243
	Foxconn	HL2112V-P9	Kontron	821042 (kit) *
FEATURE (J26)	Pinrex	52A-90-44GB00	Don Connex	A05c-44-B-G-A-1-G
	Molex	87831-4420	Kontron	1052-5885 (kit) *

More than one connector can be listed for each type of on-board connectors even though several types with same fit, form and function are approved and could be used as alternative.

Standard connectors such as DP, miniPCIe, Audio Jack, Ethernet and USB are not included in the list.

10/ BIOS

10.1. Starting the UEFI BIOS

The mITX-SKL-H is provided with a Kontron-customized, pre-installed and configured version of AMI Aptio ® V UEFI BIOS. AMI BIOS firmware is based on the Unified Extensible Firmware Interface (UEFI 2.x) specification and the Intel® Platform Innovation Framework for EFI. This UEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the mITX-SKL-H.

The UEFI BIOS comes with a setup program that provides quick and easy access to the individual function settings for control or modification of the UEFI BIOS configuration. The setup program allows the accessing of various menus that provide functions or access to sub-menus with additional specific functions of their own.

To start the UEFI BIOS setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <DEL> key.
4. If the UEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see Chapter 10.2.4 Security Setup Menu), press <RETURN>, and proceed with step 5.
5. A setup menu will appear.

The mITX-SKL-H UEFI BIOS setup program uses a hot key-based navigation system. A hot key legend bar is located on the bottom of the setup screens.

The following table provides information concerning the usage of these hot keys.

Table 35: UEFI BIOS Navigation Hot Keys

Hotkeys	Description
<F1>	The <F1> key invokes the General Help window.
<->	The <Minus> key selects the next lower value within a field.
<+>	The <Plus> key selects the next higher value within a field.
<F2>	The <F2> key loads the previous values.
<F3>	The <F3> key loads the standard default values.
<F4>	The <F4> key saves the current settings and exit the UEFI BIOS setup.
<→> or <←>	The <Left/Right> arrows selects major setup menus on the menu bar. For example: Main, Advanced, Security, etc.
<↑> or <↓>	The <Up/Down> arrows selects fields in the current menu. For example: A setup function or a sub-screen.
<ESC>	The <ESC> key exits a major setup menu and enter the Exit setup menu. Pressing the <ESC> key in a sub-menu displays the next higher menu level.
<RETURN>	The <RETURN> key executes a command or select a submenu.

10.2. Setup Menus

The setup utility features six menus listed in the selection bar at the top of the screen:

- Main
- Advanced
- Chipset
- Security
- Boot
- Save & Exit

The left and right arrow keys selects the setup menu The currently active menu and the currently active UEFI BIOS setup item are highlighted in white. Each Setup menu provides two main frames. The left frame displays all available functions. Functions that can be configured are displayed in blue. Functions displayed in gray provide information about the status or the operational configuration. The right frame displays an item specific help window providing an explanation of the respective function.

10.2.1. Main Setup Menu

Upon entering the UEFI BIOS setup program, the main setup menu is displayed. This screen lists the main setup menu sub-screens and provides basic system information as well as functions for setting the system time and date.

Table 36: Main Setup Menu Sub-screens and Functions

Sub-screen	Description
Board Information>	Read only field Displays information about the board: Board ID, Fab ID and LAN PHY Revision
Processor Information>	Read only field Displays information about the CPU, BIOS and memory: Name, Type, Frequency, Processor ID, Stepping, Package, Number of Processors, Microcode Version, GT Info, VBIOS Version, GOP Version, Total memory and Memory Frequency
PCH Information>	Read only field Displays information about the PCH: Name, PCH SKU, Stepping, Hsio Revision, Package, TXT Capability Platform/PCH, Production Type, Dual Output Fast, Read Support, Read ID Status Clock Frequency, Write and Erase, Clock Frequency, Fast Read Status Clock Frequency, Fast Read Support, Read Clock Frequency, Number of Components, SPI Components, Density, Firmware Revision, Firmware SKU
System Language>	Selects system language
System Date>	Displays system date
System Time>	Displays system time

10.2.2. Advanced Setup Menu

The Advanced setup menu provides sub-screens and functions for advanced configurations. The following sub-screen functions are included in the menu:

- CPU Configuration
- Power & Performance
- PCH-FW Configuration Information
- RTD3 Settings
- Over Clocking Performance Menu
- Intel ICC
- Trusted Computing
- ACPI Settings
- SMART Settings
- IT8528 Super IO Configuration
- Intel ® BIOS GUARD Technology
- Serial Port Console Redirection
- Intel TXT Information
- AMI Graphic Output Protocol Policy
- PCI Subsystem Settings
- Network Stack Configuration
- CSM Configuration
- NVMe Configuration
- USB Configuration
- Hardware Health Configuration
- LAN Configuration & Show
- LVDS Configuration

NOTICE Setting items on this screen to incorrect values may cause the system to malfunction.

Table 37: Advanced Setup Menu Sub-screens and Functions

Sub-screen	Function	Second level Sub-screen/Description
CPU Configuration>	CPU Configuration>	Read only field CPU configuration parameters
	C6DRAM>	Enable/disable moving Dram contents to PRM memory when CPU is in C6 state
	SW Guard Extensions>	Enable/disable Software Guard extension (SGX)
	Select Owner EPOCH Input Type>	Select the owner EPOCH mode (No change in EPOCH owner / Change to new random owner EPOCHs /Manual user defined owner EPOCHs)
	PRMRR Size>	Display the PRMRR
	CPU FLEX Ratio Override>	Enable/disable CPU flex ratio programming override
	CPU Flex Ratio Settings>	Display the CPU Flex Ratio Settings
	Hardware Prefetcher>	Enable/disable hardware prefetcher
	Attach Cache Line Prefetcher>	Turn on/off adjacent cache lines prefetching

Sub-screen	Function	Second level Sub-screen/Description	
CPU Configuration> (continued)	Intel (VMX) Virtualization Technology>	Enable/disable Intel (VMX) to use additional hardware capabilities provided by Vanderpool Technology	
	PECI>	Enable/disable PECI	
	Active Processor Cores>	Display number of cores to enable in each processor package	
	Hyper Threading>	Enable/disable OS optimized hyper-threading technology Enable – Windows XP and Linux / Disable - other OS	
	BIST>	Enable/disable built-in self-test (BIST) on request	
	JTAG C10 Power>	Enable/disable power JTAG in C10 and deeper power states	
	AP Threads IDLE Manner>	AP threads idle manner for waiting signal to run	
	AP Threads Handoff Manner>	AP treads handoff to OS manner from end of post	
	AES>	Enable/disable Advanced Encryption Standard (AES)	
	Machine Check>	Enable/disable machine check	
	MonitorMWait>	Enable/disable MonitorMWait	
	Intel Trusted Execution Technology>	Enable/disable utilization of additional hardware capabilities provided by Intel® Trusted Execution technology Note: Changes require a full power cycle to take effect.	
	Alias Check Request DPR Memory Size (MB)>	Display alias check request DPR memory size (MB)	
	Reset AUX Content>	Reset TPM Aux content Note TXT may not be functional after Aux content is reset.	
	Flash Wear-Out Protection>	Enable/disable flash wear-out protection feature	
	Current Debug Interface Status>	Display current debug interface status	
	Debug Interface >	Enable/disable debug interface support	
	Debug Interface lock>	Enable/disable debug interface lock	
	Processor Trace Memory Allocation>	Select or disable processor trace memory region size (Range: 4 KB- 128 MB)	
	CPU SMM Enhancement>	SMM Code Access Check>	Enable/disable support for SMM code access feature
		SMM Use Delay Indication>	Enable/disable usage of SMM_DELAYED MSR for MP sync in SMI
		SMM Use Block Indication>	Enable/disable usage of SMM_BLOCKED MSR for MP sync in SMI
	FCLK Frequency for Early Power-On>	Select EFCLK frequency values (400 MHz, 800 MHz, 1 GHz)	
	Voltage Optimization>	Select voltage optimization option enable/disable/auto	

Sub-screen	Function	Second level Sub-screen/Description		
Power & Performance>	CPU – Power Management Control>	Boot Performance Mode>	Select performance state set by BIOS, starting from reset vector	
		Intel ® Speedstep™>	Enable/disable support for more than two frequency ranges	
		Race to Halt (RTH)>	Enable/disable race to halt feature Note: RTH feature dynamically increases CPU frequency to enter pkg C-state faster to reduce overall power. RTH is controlled through MSR.	
		Intel® Speed Shift™ Technology>	Enable/disable Intel®speed shift™ technology support for P-state hardware control by exposing CPPC v2 interface.	
		HDC Control>	Enable/disable HDC configuration Note: can be enable by OS if OS native support available	
		Turbo Mode>	Enable/disable processor turbo mode if EMTMM also enabled Auto-enabled unless max. turbo ratio is bigger than 16	
		View/ Configure Turbo Options>	Energy Efficient P-State>	Enable/disable energy efficient P-State feature
			Package Power Limit MSR Lock>	Enable/disable locking of package power limit
			1-Core Ratio Limit Override>	Display 1-core ratio limit override
			2-Core Ratio Limit Override>	Display 2-core ratio limit override
			3-Core Ratio Limit Override>	Display 3-core ratio limit override
			4-Core Ratio Limit Override>	Display 4-core ratio limit override
			Energy Efficient Turbo>	Enable/disable energy efficient turbo feature
		Config TDP Configuration>	Configurable TDP Boot Mode>	Configurable TDP mode as Nominal/Up/Down/Deactivate TDP selection
			Configurable TDP Lock>	Enable/disable Configurable TDP Lock
			CTDP BIOS Control>	Enable/disable CTDP control via runtime ACPI BIOS methods
			ConfigTDP Levels>	ConfigTDP turbo activation ratio, power limit 1, power limit 2
			Custom Settings Nominal ConfigTDP Nominal>	Setting for power limit 1, power limit 2, power limit 1 time window, config.TDP turbo activation ratio

Sub-screen	Function	Second level Sub-screen/Description			
Power & Performance> (continued)	CPU – Power Management Control> (continued)	Config TDP Configuration> (continued)	Custom Settings Down ConfigTDP Level 1 and 2>	Setting for power limit 1, power limit 2, power limit 1 time window, config.TDP turbo activation ratio	
		CPU VR Settings>	PSYS Slope>	Display PSYS slope in 1 /100 increments (Range: 0-200)	
			PSYS Offset>	Display PSYS slope in 1 /4 increments (Range: 0-200)	
			PSYS Pmax Power>	Display PSYS Power defined in 1/8 Watt increments (Range: 0-8192)	
			Acoustic Noise Settings>	Acoustic Noise Mitigation>	Enable/disable acoustic noise mitigation
				IA VR Domain>	Display disable fast PKG C state ramp for IA domain and slow slew rate for IA domain
				GT VR Domain>	Display disable fast PKG C state ramp for GT domain and slow slew rate for GT domain
				SA VR Domain>	Display disable fast PKG C state ramp for SA domain and slow slew rate for SA domain
			Core/IA VR Settings>	VR Configure Enable	
				AC Load Line	
				DC Load Line	
			GT-Unsliced VR Settings>	PS Current Threshold 1 / 2 / 3	
				PS3 Enable	
				PS4 Enable	
			GT Sliced VR Settings>	IMON Slope	
				IMON Offset	
				IMON Prefix	
				VR Current Limit	
				VR Voltage Limit	
				TDC Enable	
				TDC Current Limit	
				TDC Time Window	
				TDC Lock	

Sub-screen	Function	Second level Sub-screen/Description		
Power & Performance> (continued)	CPU – Power Management Control> (continued)	CPU VR Settings> (continued)	VR Mailbox Command Options>	Display VR mailbox command options 1: MPS VR command 2: PS4 Exit VR command 4: MPS VR decay command Note: Multiple commands can be selected by entering sum from values of each command.
		Platform PL1 Enable>	Enable/disable perform power limit 1 programming by activating PL1 value used by processor to limit given power	
		Platform PL2 Enable>	Enable/disable perform power limit 2 programming. If disabled, BIOS programs the default values for platform power limit 2.	
		Power Limit 4 Override>	Enable/disable power limit 4 override. If disabled, BIOS leaves default values for power limit 4	
		C-State>	Enable/disable CPU power management CPU to enter C-state when not 100 % utilized	
		Enhanced C-State>	Enable/disable C11E If all cores enter C-state, CPU switches to min. speed.	
		C-State Auto Demotion>	Configure C-state auto demotion	
		C-State Undemotion>	Configure C-state undemotion	
		Package C-State Demotion>	Enable /disable Package C-state demotion	
		Package C-state Undemotion>	Enable/disable Package C-state undemotion	
		C-State Prewake>	Enable/disable C-state prewake Disable by setting bit 30 of POWER_CTL MSR (0X1FC) to 1	
		IO MWait Redirection>	If set, maps IO read instructions sent to IO registers PMG_IO_BASE_ADDRBASE+off set to MWAIT(offset)	
		Package C-state Limit>	Select the maximum package C-state limit setting	
		C3 Latency Control (MSR 0x60A)> C6/C7 Short Latency Control (MSR 0X60B)> C6/C7 Long Latency Control (MSR 0X60C)>	Setting of time unit (Unit of measurement for IRTL value) and latency	
			Setting of time unit (Unit of measurement for IRTL value) and latency	

Sub-screen	Function	Second level Sub-screen/Description		
Power & Performance> (continued)	CPU – Power Management Control> (continued)	Thermal Monitor>	Enable/disable thermal monitoring	
		Interrupt Redirection Mode>	Select interrupt redirect mode for interrupt redirection	
		Timed Mwait>	Enable /disable timed MWAIT support	
		Custom P-State Table>	Number of P-States>	Display number of custom P-states Note: Minimum of 2 states must be present.
		Energy Performance Gain>	Enable/disable energy performance gain	
		Power Limit 3 Settings>	Power Limit 3 Override>	Enable/disable power limit 3 override If disabled, BIOS leaves the default values for power limit 3 and power limit 3 time-window.
		CPU Lock Configuration>	CFG Lock>	Enable/disable configuration of 0XE2[15] CFG lock bit
			Over Clocking Lock>	Enable/disable overclocking lock bit 20 in FLEX ratio (194) MSR
	GT- Power Management Control>	RC6 (Render Standby)>		Check to enable render standby support
		Maximum GT Frequency>		Choose between 350MHz (RPN) and 1000MHz (RP0). Value beyond the range will be clipped to min./max. supported by SKU
PCH-FW Configuration Information>	ME Firmware Version>	Display ME firmware version		
	ME FirmwareMode>	Display ME firmware mode		
	ME Firmware SKU>	Display ME firmware SKU		
	ME File System Integrity Value>	Display ME file system integrity value		
	ME Firmware Status 1>	Display ME firmware status 1		
	ME Firmware Status 2>	Display ME firmware status 2		
	NFC Support>	Display NFC support		
	ME State>	Enable/disable ME temporary disabled mode		
	Manageability Features State>	Display manageability Enable/disable manageability features supported in firmware		
	Features State>	Display features state		
	AMT BIOS Features>	Enable/disable AMT BIOS feature support If not supported the user is no longer able to access MEBx. Note: This option does not disable manageability.		
	AMT Configuration>	ASF Support>		Enable/disable alert standard format support
		USB Provisioning of AMT>		Enable/disable of AMT USB provisioning

Sub-screen	Function	Second level Sub-screen/Description		
PCH-FW Configuration Information> (continued)	AMT Configuration> (continued)	CIRA Configuration>	Active Remote Assistance Process>	Trigger CIRA boot
			CIRA Timeout>	Display CIRA timeout
		ASF Configuration>	PET Progress>	Enable/disable PET events progress to receive PET events
			Watchdog>	Enable/disable watchdog timer
			OS Timer>	Display OS timer
			BIOS Timer>	Display BIOS timer
		Secure Erase Configuration>	Secure Erase Mode>	Change secure erase module behavior
			Force Secure Erase>	Force secure erase on next boot
		OEM Flags Settings>	MEBx hotkey Pressed>	Enable/disable MEBx hotkey pressed
			MEBx Selection Screen>	Enable/disable MEBx selection screen
			Hide Unconfigure ME Confirmation Prompt>	Enable/disable hide unconfigure ME confirmation prompt
			MEBx OEM Debug Menu Enable>	Enable/disable MEBx OEM debug menu
			Unconfigure ME>	Enable/disable unconfigure ME
		MEBx Resolution Settings>	Non-UI Mode Resolution>	Resolution for non-UI text mode
			UI Mode Resolution>	Resolution for UI text mode
			Graphic Mode Resolution>	Resolution for graphics mode
	ME Unconfig 0 RTC clear>	Display ME unconfig on RTC clear		
	Comms Hub Support>	Enable/disable support for comms hub		
	JHI Support>	Enable/disable Intel® DAL host interface service (JHI)		
	Core BIOS Done Message>	Enable/disable sending core BIOS done message to ME		
	Firmware Update Configuration>	ME FW Image Re-Flash>	Enable/disable ME FW image re-flash function	
	PTT Configuration>	PTT Capability/State>	Display PTT capability/state	
		TPM Device Selection>	Select TPM device: PTT or dTPM.	
		PTP Aware OS>	Display PTP aware OS	
	ME Debug Configuration>	HECI Timeouts>	Enable/disable HECI send/receive timeouts	
		Force ME DID Init Status>	Force the DID Initialization status value	
		CPU Replaced Polling Disable>	Setting this option disables CPU replacement polling loop	
		ME DID Message>	Enable/disable ME DID message	

Sub-screen	Function	Second level Sub-screen/Description	
PCH-FW Configuration Information> (continued)	ME Debug Configuration> (continued)	HECI Retry Disable>	Setting this option disables retry mechanism for all HECI APIs
		HECI Message check Disable>	Setting this option disables message check for Bios boot path when sending
		MBP HOB Skip>	Setting this option skips MBP HOB
		HECI2 Interface Communication>	Adds and removes HECI2 Device from PCI space
		KT Device>	Enable/disable KT device
		IDER Device>	Enable/disable IDER device
		End Of Post Message>	Enable/disable End Of Post message sent to ME
		DOI3 Setting for HECI Disable>	Setting this option disables setting DOI3 bit for all HECI devices
	Note: This menu is for testing purposes. It is recommended to leave the options in their default states.		
RTD3 Settings>	RTD3 Support>	Enable/disable runtime D3 support	
	VR Staggering Delay>	Delay between subsequent VR power-on to avoid a current spike	
	VR Ramp Up Delay>	Delay between subsequent VR ramp ups if they are all turned on at the same time	
	PCIE Slot 5 Device Power-On Delay >	Delay between applying core power and deasserting PERST#	
	PCIE Slot 5 Device Power-Off Delay>	Delay after removing core power	
	Audio Delay>	Delay after applying power to HD Audio(realtek) codec device	
	I2C0 Controller>	Delay in PS0 I2C0 controller	
	Sensor Hub>	Delay after applying power to sensor hub device	
	I2C1 Controller>	Delay in PS0 I2C1 controller	
	Touchpad>	Delay after applying power to touchpad device	
	Touch Panel>	Display in PR-ON after applying power to touch panel device	
	P-State Capping>	Set _PPC and send ACPI notifications	
	USB Port 1>	USB RTD3 USB support	
	USB Port 2>		
	I2C0 Sensor Hub>	Enable/disable RTD3 support for I2C0 sensor hub	
	ZPODD>	Zero power ODD option is applicable only for WhiteTipMountain1 and AdenHills with ZPODD Feature rework	
	WWAN>	Enable/disable RTD3 support for WWAN	
	SATA Port 0>	Enable/disable setup option to control SATA port RTD3 functionality	
	SATA Port 1>		
	SATA Port 2>		
	Minicard SATA Port 3>		
	SATA Port 4>		
	PCIe Remapped CR1>	Display PCIe remapped CR1	

Sub-screen	Function	Second level Sub-screen/Description	
RTD3 Settings> (continue)	PCIe Remapped CR2>	Display PCIe remapped CR2	
	PCIe Remapped CR3>	Display PCIe remapped CR3	
	RST Raid Volumes>	Valid only with RST storage driver	
Over Clocking Performance Menu>	Over Clocking Feature>	Performance menu for processor and memory	
	WDT Enable>	Enable/disable watchdog timer Note: This option is ignored on debug BIOS	
	RSR>	Enable/disable RSR feature	
Intel ICC>	ICC/OC WatchDog Timer>	Enable/disable ICC/OC watchdog timer Note: WDT HW is always used by BIOS when clock settings are changed.	
	ICC Locks after EOP>	Display ICC locks after EOP	
	ICC Profile>	Display ICC profile	
Trusted Computing>	Security Device Support>	Enable/disable BIOS support for security devices OS will not show the security device, TCG EFI protocol and INT1A interface will not be available.	
	TPM State>	Enable/disable security device Note: Computer will reboot during restart in order to change state.	
	Pending Operation>	Schedules operation for the security device Note: Computer will reboot during restart to change state of security device.	
	Device Select>	TPM 1.2 restricts support to TPM 1.2 device, TPM 2.0 restricts support to TPM 2.0 device, Auto supports both with the default set to TPM 2.0 devices if not found.	
	Current Status Information>	Displays current status Information	
ACPI Settings>	Enable ACPI Auto Configuration>	Enable/disable BIOS ACPI auto configuration	
	Enable Hibernation>	Enable/Disable systems ability to hibernate (OS/S4 sleep state) Note: This option may not be effective with some OS(s).	
	ACPI Sleep State>	Selects highest ACPI sleep state system enters when suspend is pressed	
	Lock Legacy Resources>	Enable/disable lock of legacy resources	
	S3 Video Repost>	Enable/disable S3 video repost	
SMART Settings>	Smart Self-Test>	Enable/disable running smart self-test on all HDDs during POST	
IT8528 Super IO Configuration>	Super IO Chip>	IT8528>	
	Serial Port 1 Configuration>	Serial Port>	Enable/disable serial port (COM)
		Device Settings>	Display device settings
		Change Settings>	Select an optimal settings for super IO device
	Serial Port 2 Configuration>	Serial Port>	Enable/disable serial port (COM)
		Device Settings>	Display device settings
		Change Settings>	Select an optimal settings for super IO device

Sub-screen	Function	Second level Sub-screen/Description	
IT8528 Super IO Configuration> (continued)	Serial Port 2 Configuration> (continued)	RS422 Duplex Mode>	Set full or half duplex mode
		RTS Control>	Select receiver controlled RTS enable or permanently enable RTS
Intel ® Bios GUARD Technology>	Intel ® Bios Guard Support>	Enable/disable Intel BIOS guard support	
Serial Port Console Redirection>	Console Redirection>	Enable/disable console redirection	
	Control Redirection Settings>	Terminal Type>	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode
		Bits per second>	Select serial port transmission speed
		Data Bits>	Data bits
		Parity>	A parity bit can be sent with the data bit to detect some transmission errors
		Stop Bits>	Stops bits indicate the end of a serial data packet
		Flow Control>	Flow control can prevent data loss from buffer overflow
		VT-UTF8 Combo Key Support>	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
		Recorder Mode>	With this mode enabled only text will be sent. This is to capture terminal data
		Resolution 100x31>	Enable/disabled extended terminal resolution
		Legacy OS Redirection Resolution>	On legacy OS, the number of rows and columns supported redirection.
		Putty KeyPad>	Select function key and keypad on putty.
		Redirection After BIOS POST>	The settings specify if bootloader is selected then legacy console redirection is disable before booting to legacy OS
	COM1(Pci Bus0, Dev0, Func0)>		Read only field
	Console Redirection>		Read Only field - port is disable
	Legacy Control Redirection settings>	Legacy Serial Redirection Port>	Selects a COM port to display redirection of legacy OPROM messages
	Serial Port for Out-of-Band Management /Windows Emergency Management Services Console Redirection>	Enable/disable console redirection	

Sub-screen	Function	Second level Sub-screen/Description
Intel TXT Information>	Chipset>	Read Only field - production fused
	BiosAcm>	Read Only field - production fused
	Chipset Txt>	Read Only field - supported
	Cpu Txt>	Read Only field - supported
	Error Code>	Read Only field - none
	Class Code>	Read Only field - none
	Major Code>	Read Only field - none
	Minor Code>	Read Only field – none
AMI Graphic Output Protocol Policy>	Output Select>	Output interface
	Brightness Setting>	Read only field
	BIST Enable>	Read only field
PCI Subsystem Settings>	AMI PCI Driver Version>	Read only field - A5.01.11
	Above 4G Decoding>	Enable/disable above 4G decoding
	Hot-Plug Support>	Hot-Plug support
	Restore PCIE Registers>	Enable/disable restore PCIE registers
	Don't Reset VC-TC Mapping>	Enable/disable don't reset VC-TC mapping
Network Stack Configuration>	Network Stack>	Enable/disable UEFI network stack
CSM Configuration>	CSM Support>	Enable/disable compatibility support module support
NVMe Configuration>	NVMe controller and Device Information>	No NVMe device found
USB Configuration>	Legacy USB Support>	Enables legacy USB support
	XHCI Hand-off>	Workaround for OS(s) without XHCI hand-off support
	USB Mass Storage Driver Support>	Enable/disable USB mass storage driver support
	Port 60/64 Emulation>	Enable/disable Port 60/64 emulation
	USB transfer time-out>	Time-out value for control, bulk, and interrupt transfer
	Device reset time-out>	USB mass storage device start unit command time-out
	Device power-up delay>	Maximum time the device takes before the device reports itself to the host controller properly.
Hardware Health Configuration>	System Temp.>	Display the system temperature
	System Temp. Offset>	Adjust the offset value in C (two's complement)
	CPU Temp.>	Display CPU temperature
	System Fan Speed>	Display system fan speed

Sub-screen	Function	Second level Sub-screen/Description
Hardware Health Configuration> (continued)	System Fan Cruise Control>	Disable = full speed Thermal = does regulate fan speed according to specified temperature Speed = does regulate according to specified speed
	CPU Fan Speed>	Display CPU fan speed
	CPU Fan Cruise Control>	Disable = full speed Thermal = does regulate fan speed according to specified temperature Speed = does regulate according to specified speed
	Watchdog Function>	0 = Disable. Enter the service interval in seconds before the system will reset
	GPP_B11 GPO Setting>	This GPP_B11 is WDT related. This setting programs GPP_B11 as GPO only. It does not program WDT timer into EC
	ITE8528 Firmware Update>	This option enables auto update when version is not a match, force update or disable update EC firmware.
	PC Speaker/Beep>	Controls the default beeps during boot of the system
LAN Configuration & Show>	I211 ETH1 MacAddr & LinkStatus>	Display I211 ETH1 MacAddr & LinkStatus
	I211 ETH2 MacAddr & LinkStatus>	Display I211 ETH2 MacAddr & LinkStatus
	I211 ETH3 MacAddr & LinkStatus>	Display I211 ETH3 MacAddr & LinkStatus
	I211 ETH4 MacAddr & LinkStatus>	Display I211 ETH4 MacAddr & LinkStatus
LVDS Configuration &Show>	LVDS Flat Panel Display Support>	Enable/disable LVDS flat panel display support
	EDID ROM Emulation>	Enable/disable EDID ROM emulation to support panels with no EDID ROM
	EDID ROM Flash Page Number>	PTN3460 can store seven copies of EDID ROM on internal flash
	Panel Type>	Select the type or manufacturer's name of the display panel
	Resolution>	Select the screen resolution of the display panel
	Panel Color Depth>	Select the display panel color depth
	Panel Voltage>	Select the voltage level for powering the LVDS display panel
	Channel>	Select LVDS interface signals mode single-channel or dual-channel (Sometimes called "single-pixel" or "dual-pixel")
	Bus Swapping>	Swap LVDS interface signals: Normal – uses bus as indicated by pin name, Swapped – swaps 'odd' bus signals with 'even' bus signals
	Clock Frequency Center Spread>	Programmable center spreading of pixel clock frequency to minimize EMI
	Differential Output Swing Level>	Programmable LVDS signal swing to pre-compensate for channel attenuation or allow for power saving
	Backlight>	Enable/disable backlight
	Backlight Signal Inversion>	Enable – active high Disable – active low for display panel backlight signal
	Backlight PWM Frequency>	Set the PWM frequency the backlight
	Brightness Level>	Select the Brightness level for the backlight of the display panel

10.2.3. Chipset Setup Menu

On entering the Chipset setup menu, the screen lists two setup menu options:

- System Agent (previously Northbridge)
- PCH-IO (previously Southbridge)

10.2.3.1. System Agent Configuration

The System Agent Configuration setup menu provides sub-screens and functions for high performance data configurations. The following sub-screen functions are included in the menu:

- Memory Configuration
- Graphics Configuration
- DMI/OPI Configuration
- PEG Port Configuration
- Stop Grant configuration
- VT-d
- Chap Device (B0:D4:F0)
- Thermal Device (B0:D4:F0)
- GMM Device (B0:D4:F0)
- CRID Support
- Above 4GB MMIO BIOS Assignment
- X2APIC Opt Out
- Sky CAM Device (B0:D5:F0)

Table 38: Chipset Setup Menu- System Agent Configuration Sub-screens and Functions

Function	Second level Sub-screen / Description			
Memory Configurations>	Read only field Memory configuration (version, frequency, timings, channel /slot information, ratio reference, clock options, overclock Information)			
	Memory Thermal Configurations>	Memory Power and Thermal Throttling>	DDR PowerDown and Idle Counter>	BIOS is in control of DDR CKE mode and idle timer value
			For LPDDR Only: DDR PowerDown and Idle Counter>	For LPDDR Only: BIOS: BIOS is in control of DDR CKE mode and idle timer value
			Refresh_2X_ MODE>	0-Disabled 1-iMC enables 2xRef when warm / hot 2-iMC enables 2xRef when hot
			LPDDR Thermal Sensor>	If enabled, MC uses MR4 to read LPDDR thermal sensors
			SelfRefresh Enable>	Enable/disable (Enable=Def)
			SelfRefresh IdleTimer>	Range [64K-1;512] in DLCK800s, (512=Def)

Function	Second level Sub-screen / Description				
Memory Configurations> (continued)	Memory Thermal Configurations> (continued)	Memory Power and Thermal Throttling> (continued)	Throttler CKEMin Defeature>	On/Off	
			Throttler CKEMin Timer>	Timer value for CKEMin, Range: [255;0]	
			DRAM Power Meter>	Use User Provided Weights, Scale Factors, and Channel Power Floor Values>	Enable- user provided power weights, scale factor, and channel power floor values. Disable: BIOS set power weights, scale factor, and channel power floor
				DRAM Power Meter Setting>	Display DRAM power meter setting
			Memory Thermal Reporting>	Lock Thermal Management Registers>	Enable- locks several CPU registers related to DDR power/thermal management.
				Extern Therm Status>	Enable- uses EXTTS value
				Closed Loop Therm Manage>	Disable- Pcode ignores the EXTTS
				Open Loop Therm Manage>	Enabled: OLTM pcode algorithm will be used
				Thermal Threshold settings for CH0 and CH1 Thermal Throttle Budget settings for CH0 DIMM0 /CH0 DIMM1 and CH1 DIMM0/ Ch1 DIMM1	
			Memory RAPL>	Sets the RAPL limit register and the RAPL Pl1 and PL2, power range and time window X and Y values.	
		Memory Thermal Management>	Enable/disable memory thermal management		
	Memory Training Algorithms>	Enable/disable memory training algorithms			
	Memory Configuration>	Display memory configuration			
	MRC ULT Safe Config.>	MRC ULT Safe configure for P0			
	Maximum Memory Frequency>	Select maximum memory frequency in MHZ			

Function	Second level Sub-screen / Description	
Memory Configurations> (continued)	HOB Buffer Size>	Select HOB buffer size
	ECC Support>	Enable/disable DRR ECC support
	Max TOLUD>	Maximum TOLUD value (from 1 GB to 3.5 GB) Dynamic assignment adjusts TOLUD automatically based on the largest MMIO length of the installed graphic controller.
	SA GV>	System Agent Geyserville
	SA GV Low Frequency>	System Agent Geyserville. set frequency for low point
	Retrain On Fast Fail>	Restart MRC in cold mode if SW memory test fails during fast flow
	Command Tristate>	Command tristate support
	Enable RH Prevention>	Activity prevent row hammer
	Row Hammer Solution>	Type of method used to prevent row hammer
	RH Activation Probability>	Used to adjust MC for hardware RHP
	Exit on Failure (MRC)>	Exit on failure for MRC training steps
	MC Lock>	Enable/disable capacity to lock or not MC registers
	Probeless Trace>	HD Port, GDXC IOT/MOT or disable
	Enable Disable IED (Intel® Enhanced Debug)>	Enable/disable Intel® Enhanced Debug required 4MB SMM memory
	Ch Hash Support>	Enable/disable channel hash support Note: Only in memory interleave mode
	Ch Hash Mask>	Set the bit(s) included in the XOR function Note: Bit mask corresponds to bits [19:6]
	Ch Hash Interleaved Bit>	Select the bit used for channel interleave mode Note: Bit 7 interleaves channels at a 2 cache line granularity, (Bit 8 at 4 and Bit 9 at 8).
	VC1 Read Metering>	Enable/disable VC1 Read metering feature (RdMeter)
	VC1 RdMeter Time Window>	DisplaysVC1 read metering time window in µs over which VC1 read request counter is tracked
	VC1 Rdmeter Threshold>	Display the threshold of the counter in the time window
	Strong Weak Leaker>	Strong weak leaker value
	Memory Scrambler>	Enable/disable memory scrambler
	Force Cold Reset>	Enable/disable force cold reset or MRCcoldboot mode if coldboot is required during MRC execution Note: If ME is 5.0 MB, Force coldreset is required.

Function	Second level Sub-screen / Description	
Memory Configurations> (continued)	Channel A DIMM Control>	Enable/disable DIMMs on channel A
	Channel B DIMM Control>	Enable/disable DIMMs on channel B
	Force Single Rank>	If enabled, only Rank 0 will be used in each DIMM
	Memory Remap>	Enable/disable memory remap above 4 GB
	Time Measure>	Enable/disable printing time taken to execute MRC
	DLL Weak Lock Support>	Enable/disable DLL weak lock support
	Pwr Down Idle Timer>	The minimum value should equal the worst case Roundtrip delay + Burst_Length. 0 means AUTO: 64 for ULX/ULT, 128 for DT/Halo.
	MrcFast Boot>	Enable/disable fast path through the MRC
	Lpddr Mem WL Set>	Sets LPDDR Memory Write Latency (A – default, B- used if memory devices supports the value)
	EV Loader>	Enable/disable EV loader functionality
	EV Loader Delay>	Enable/disable EV loader 2 second delay
Graphics Configuration>	Graphics Turbo IMON Current>	Displays supported graphics turbo IMON current values (14-31)
	Skip Scanned for External GfX Card>	Enable - no scan made for external Gfx cards on PEG or PCH PCIE ports.
	External Gfx card Primary Display Configuration>	Select primary display graphics configuration
	Internal Graphics>	Keeps IGFX enabled, based on setup options
	GTT Size>	Selects GTT size
	Aperture Size>	Selects aperture size Note: Above 4 GB MMIO, the BIOS assignment is automatically enabled if selecting 2048 MB aperture. To use this feature disable CSM support.
	DVMT Pre-Allocated>	Selects DVMT 5.0 pre-allocated (fixed) graphics memory size used by internal graphics device
	DVMT Total Gfx Mem>	Selects DVMT 5.0 total graphics memory size used by internal graphics device
	Gfx Low Power Mode>	Used for SFF only
	VDD Enable>	Enables/disable VDD forcing in BIOS
	HDCP Support>	Enable/disable HDCP provisioning support
	Algorithm>	Select HDCP re-encryption flow
	PM Support>	Enable/disable PMM support
	PAVP Enable>	Enable/disable PAVP
	Cdynmax Clamping Enable>	Enable/disable cdynmax clamping

Function	Second level Sub-screen / Description			
Graphics Configuration> (continued)	Cd Clock Frequency>		Select highest Cd clock frequency supported by platform	
	IUER Button Enable>		Enable/disable IUER button functionality	
DMI/OPI Configuration>	DMI Max Link Speed>		Set DMI maximum link speed Gen1 / Gen2 / Gen3 / Auto	
	DMI Gen 3 EQ Phase 2>		Perform Gen 3 equalization phase 2	
	DMI Gen 3 EQ Phase 3 Method>		Select method for Gen3 equalization phase 3	
	DMI Vc1 Control>		Enable/disable DMI Vcm1	
	DMI Vcm Control>		Enable/disable DMI Vcm	
	Program Static Phase1 Eq>		Enable/disable programming of phase 1 presets/CTLEp	
	Gen3 Root Port Preset Value for Each Lane>		Select the lane > (lane 0 to 3)	Display value for selected lane.
	Gen3 Endpoint Preset Value for Each Lane>			
	Gen3 Endpoint Hint Value for Each Lane>			
	Gen3 RxCTLE Control>		Bundle 0>	Display Gen3 RxCTLE setting for selected bundle (0 or 1)
			Bundle 1>	
	DMI Link ASPM Control>		Enable/disable control of active state power management on SA side of the DMI link	
	DMI Extended Sync Control>		Enable/disable extended sync control	
	DMI De-Emphasis Control>		Select the DMI de-emphasis control (-6 dB, -3.5 dB)	
	DMI IOT>		Enable/disable DMI IOT	
PEG Port Configuration>	PEG 0:1:0	Enable Root Port>	Enable/disable the root port	
		Max Link Speed>	Configure PEG #:#:# maximum speed	
	PEG 0:1:1	PEG(0/1/2) Slot Power Limit Value>	Set power supply upper limit by slot. (Values: 0-255)	
	PEG 0:1:2	PEG(0/1/2) Slot Power Limit Scale>	Select scale used for the slot power limit value	
		PEG(0/1/2) Physical Slot Number>	Sets the port's physical slot number. This number must be globally unique within the chassis. (Values: 0 to 8191)	
		Peg0 Hot Plug>	PCI Express hot plug enable/disable	

Function	Second level Sub-screen / Description		
PEG Port Configuration> (continued)	PWG Port Feature Configuration>	Detect non-compliance Device>	Enable/disable non-compliance PCI express device in PEG
	Program PCIe ASPM After OpROM>	Enable/disable PCIe ASPM programming before or after OpROM Enable –progrmmed after OpROM. Disable –programmed before OPROM	
	Program Static Phase1 Eq>	Program phase1 presets/CTLEp	
	Gen3 Root Port Preset Value for Each Lane>	Select the lane > (lane 0 to 15)	Display value for selected lane.
	Gen3 End Point Preset Value for Each Lane>		
	Gen3 Endpoint Hint Value for Each Lane>		
	Gen3 RXCTLE Control>	Select (Bundle0– 7 or RXCTLE Override)	Display Gen3 RxCTLE setting for bundle
	Always Attempts SW EQ>	Always attempts SW EQ even if it has been performed once	
	Number of Presets to Test>	Select the number of presets to test Chose(7, 3, 5, 8) or (0-9) or (Auto for default value) Note: Do not change from the default unless debugging.	
	Allows PERST# GPIO Usage>	Enable/disable GPIO based resets to PEG endpoint(s) during margin search	
	SW EQ Enable VOC>	Select jitter & VOC test mode (default) or jitter only test mode	
	Jitter Dwell Time>	Displays PEG Gen3 preset search dwell time [0-65535] in µs	
	Jitter Error Target>	Displays margin search error target value [1-65535]	
	VOC Dwell Time>	Displays VOC margin search dwell time [0..65535]	
	VOC Error Target>	Display VOC margin search error target value [1-65535]	
	Generate BDAT PEG Margin Data>	Enable/disable BDAT PCIe margin tables	
	PCI Rx CEM Test Mode>	Enable/disable PEG Rx CEM loopback mode	
	PCIe Spread Spectrum Clocking>	Enable/disable spreader clocking for compliance testing	
Stop Grant Configuration>	Set automatic or manual stop grant configuration		
VT-d>	Enable/disable VT-d capabilities		
Chap Device (B0:D4:F0)>	Enable/disable SA CHAP device		
Thermal Device (B0:D4:F0)>	Enable/disable SA C thermal device		

Function	Second level Sub-screen / Description
GMM Device (B0:D4:F0)>	Enable/disable SA GMM device
CRID Support>	Enable/disable CRID control for Intel SIPP
Above 4GB MMIO BIOS Assignment>	Enable/disable above 4 GB memory mapped IO BIOS assignment Disabled automically if aperture size is set to 2048 MB.
X2APIC Opt Out>	Enable/disable X2APIC_Opt_Out bit
Sky CAM Device (B0:D5:F0)>	Enable/disable SA SKY CAM device

10.2.3.2. PCH-IO Configuration

The PCH-IO Configuration setup menu provides sub-screens for IO functions. The following subscreen functions are included in the menu:

- PCI Express Configuration
- SATA and RST Configuration
- USB Configuration
- Security Configuration
- HD Audio Configuration
- Serial IO Configuration
- ISH Configuration
- TraceHub Configuration Menu
- PCH Thermal Throttling Control
- SB Porting Configuration
- DCI Enable (HDCIEN)
- DCI Auto Detect Enable
- Debug Port Selection
- GNSS
- PCH LAN Controller
- DeepSx Power Policies
- Lan Wake From DeepSx
- Wake On LAN
- SLP_LAN# Low on DC PowerOLE_k1_off
- K1 OFF
- Wake on WLAN and BT Enable
- Disable DSX ACPRESET PullDown
- CLKRUN# Logic
- Serial IRQ Mode
- Port 61h Bit-4 Emulation
- State After G3
- Port 80h Redirection
- Enhanced Port 80 h LPC Decoding
- Compatibility Revision ID
- PCH Cross Throttling
- Disable Energy Reporting
- Enable TCO Timer
- PCIe PLL SSC
- Unlock PCH P2SB

- PMC Read Disable
- Flash Protection Range Registers (FPRR)
- SPD Write Disable
- ChipsetInit HECI Message
- Bypass ChipsetInit Sync Reset

Table 39: Chipset Setup Menu –PCH-IO Configuration Sub-screens and Functions

Function	Second level Sub-screen / Description		
PCI Express Configuration>	PCI Express Clock Gating>	Enable/disable PCI Express clock gating for each root port	
	DMI Link ASPM Control>	Enable/disable control of active state power management of DMI link	
	PCIE Port assigned to LAN>	Read only field 5	
	Port8xh Decode>	Enable/disable PCI express port 8xh decode	
	Peer Memory Write Enable>	Enable/disable peer memory write	
	Compliance Test Mode>	Enable when using compliance load board	
	PCIe-USB Glitch W/A>	Work around for bad USB device(s) connected behind PCIE/PEG port	
	PCIe Function Swap>	Disable prevents PCIO Root port function swap. If any function other than 0th is enabled, 0th becomes visible.	
	PCI Express Gen 3 Eq Lanes>	PCIE# Cm (# = 1-20)> PCIE# Cp (# = 1-20>)	Display PCIE# Cm (# = 1-20) Display PCIE# Cp (# = 1-20)
		Overrides SW EQ Settings>	Enable/disable overrides SW EQ settings
	PCIe Root Port # Links to I211 Eth2 2 – Links to I211 Eth3 3 4 6 – links to I211 Eth1 7 8 9 13 14 15 16 17 21 22 23 24	PCI Express Root Port #>	Control the PCI Express root port
		Topology>	Identify the SATA topology if it is default or ISATA or Flex or Direct Connect or M2
		ASPM>	Set the ASPM level
		L1 Substates>	PCI Express L1 substates settings
		Gen3 Eq Phase3 Method>	PCIe Gen3 equalization phase 3 method
		UPTP>	Upstream port transmitter preset
		DPTP>	Downstream port transmitter preset
		ACS>	Enable/disable access control services Extended Capability
		URR>	Enable/disable PCI Express unsupported request reporting
		FER>	Enable/disable PCI Express device fatal error reporting
		NFER>	Enable/disable PCI Express device non-fatal error reporting
		CER>	Enable/disable PCI Express device non-correctable error reporting

Function	Second level Sub-screen / Description			
PCI Express Configuration> (continued)	PCIe Root Port # Links to I211 Eth2 2 – Links to I211 Eth3 3 4 6 – links to I211 Eth1 7 8 9 13 14 15 16 17 21 22 23 24 (continued)	CTO>		Enable/disable PCI Express completion timer T0
		SEFE>		Enable/disable Root PCI Express system error on fatal error
		SECE>		Enable/disable Root PCI Express system error on correctable error
		PME SCI>		Enable/disable PCI Express PME SCI
		Hot Plug>		Enable/disable PCI Express hot plug
		Advanced Error Reporting>		Enable/disable advanced error reporting
		PCIe Speed>		Configures PCIe speed
		Transmitter Half Swing>		Enable/disable transmitter half swing
		Detect Timeout>		The number of milliseconds (ms) reference code waits for link to exit Detect state for enable ports before assuming there is no device and potentially disabling.
		Extra Bus Reserved>		Extra bus reserved (0-7) for bridges behind this root bridge
		Reserved Memory>		Reserved memory for this root bridge (1-20) MB
		Reserved I/O>		Reserved I/O (4K/ 8K/ 12K/ 16K/ 20K) range for this root bridge
		PCH PCIE# LTR>		Enable/disable PCH PCIE latency reporting
		Snoop Latency Override>		Snoop latency override for PCH PCIE
		Non Snoop Latency Override>		Non snoop latency override for PCH PCIE
		Force LTR Override>		Force LTR override for PCH PCIE
		PCIE1 LTR Lock>		PCIE LTR configuration Lock
		PCIE# CLKREQ Mapping Override>		PCIE CLKREQ override for default platform mapping
		Extra Options>	Detect Non-Compliance Device>	Detect non-compliance PCI Express device
			Prefetchable Memory>	Prefetchable memory range for this root bridge
			Reserved Memory Alignment>	Reserved memory alignement (0-31 bits)
			Prefetchable Memory Alignment>	Prefetchable memory alignement (0-31 bits)
SATA and RST Configuration>	SATA Controller>	Enable/disable SATA device		
	SATA Mode Selection>	Determines SATA controllers operation		

Function	Second level Sub-screen / Description		
SATA and RST Configuration> (continued)	SATA Test Mode>	Enable/disable test mod	
	SAT Feature Mask Configuration>	HDD Unlock>	Enable/disable HDD password unlock in OS
		LED Locate>	LED/SGPIO hardware is attached and ping to locate feature is enable on the OS
	Aggressive LPM Support>	Enable/disable PCH to aggressively enter link power state	
	SATA Controller Speed>	Displays the SATA controller speed	
	Serial ATA Port # (# = 0-7) SATA0 M.2 SATA1 mSATA SATA2 J10 SATA3 J12 SATA6 J11 SATA7 J13	SATA0 M.2:>	Unknown software preserve
		Software Preserve>	Enable/disable SATA Port
		Port #>	Designates port as hot pluggable
		Hot Plug>	Hot plug supported
		Configured as eSATA>	Enable/disable spin up device
		Spin Up Device>	Identify if SATA port is connected to solid state drive or hard disk drive
		SATA Device Type>	Identify the SATA Topology if it is default or ISATA or Flex or Direct Connect or M2
		Topology>	Enable/disable SATA Port# DevSlp
		SATA Port# DevSlp>	Enable/disable DITO configuration
		DITO Configuration>	Display DITO value
		DITO Value>	Display DM value
USB Configuration>	XHCI Disable Compliance Mode>	Option to disable compliance mode True -disables compliance mode. (Default is false)	
	xDCI Support>	Enable/disable xDCI (USB OTG device)	
	USB Port Disable Override>	Enable/disable corresponding USB port from reporting a device connection to the controller	
Security Configuration>	RTC Lock>	Enable/disable RTC lock Enable- locks bytes 38h-3Fh in lower/upper 128 byte RTC RAM bank	
	BIOS Lock>	Enable/disable PCH BIOS lock enable (BLE bit) feature	
HD Audio Configuration>	HD Audio>	Control detection of the HD-audio device Disable- HDA unconditionally disabled Enable – HDA unconditionally enabled Auto – HD enabled if present	
	Audio DSP>	Enable/disable audio DSP	
	Audio DSP Compliance Mode>	Specifies DSP enabled system compliance 1/ Non-UAA (IntelSST driver support only -CC_0400100) 2/.UAA (HD audio inbox or IntelSST driver support-CC_040380)	
	HDA-Link Codec Select>	Selects which of the following is used:	

Function	Second level Sub-screen / Description		
HD Audio Configuration> (continued)	HDA-Link Codec Select> (continued)	Platform onboard codec (single verb table installed) or External codec kit (multiple verb table installed)	
	iDisplay Audio Disconnect>	Disconnects SDI2 signal to hide/disable iDisplay audio codec	
	PME Enable>	Enable/disable power management wake of audio controller during POST	
	HD Audio Advanced Configuration>	I/O Buffer Ownership>	Selects the ownership of the I/O buffer between Intel HD audio link and I2S port (for bilingual codecs)
		I/O Buffer Voltage Select>	Selects the voltage operation mode of the I/O buffer
		HD Audio Link Frequency>	Selects HD audio link frequency (Applicable only if HDA codec supports selected frequency)
		iDisplay Link Frequency>	Selects iDisplay Link frequency (Applicable only if iDisp codec supports selected frequency)
	HD Audio DSP Features Configuration>	Read Only field (DMIC, Bluetooth and I2S)	
		WoV (Wake on Voice)>	Enable/disable DSP feature Bitmap structure: Bit 0 – WOV Bit 1 - BT Sideband Bit 2 - Codec based VAD Bit 5 - BT Intel HFP Bit 6 - BT Intel A2DP
		Bluetooth Sideband>	
		BT Intel HFP (read only field)	
		BT Intel A2DP (read only field)	
		Codec Based VAD>	
		DSP Based Speech Pre-processing Disabled>	
		Voice Activity Detection>	
		Waves>	Enable/disable 3rd party processing module support (identified by GUID) Note: WOV must first be enabled as a feature to select relevant WoV IP.
		DTS>	
		IntelSST Speech>	
		Dolby>	
		Waves Pre-process>	
		Audyssey>	
		Maximum Smart AMP>	
		Fortemedia SAMSoft>	
		Intel WoV>	
		Sound Research IP>	
		Conexant Pre-Process>	
		Conexant Smart Amp>	
		Realtek Post-Process>	
		Realtek Smart Amp>	
		Icepower IP MFX sub module>	

Function	Second level Sub-screen / Description		
HD Audio Configuration> (continued)	HD Audio DSP Features Configuration> (continued)	Icepower IP EFX sub module>	Enable/disable 3rd party processing module support (identified by GUID) Note: WOV must be enabled first as a feature, to select relevant WoV IP.
		Icepower IP SFX sub module>	
		Custom Module 'Alpha'>	
		Custom Module 'Beta'>	
		Custom Module 'Gamma'>	
Serial IO Configuration>	I2C0 Controller1>	Enables/disables Serial IO controller Following devices depend on each other: I2C0 and I2C1;2;3 UART0 and UART1, SPI0, SPI1 UART2 and I2C4, I2C5	
	I2C1 Controller2>		
	I2C2 Controller3>		
	SPI0 Controller>		
	SPI1 Controller>		
	SPI2 Controller>		
	UART0 Controller>		
	UART1 Controller>		
	UART2 Controller>		
	GPIO Controller>	Enable /disable the GPIO controller	
	Serial IO I2C0 Settings>	I2C IO Voltage Select>	Select 1.8 V or 3.3 V for the controller
		Connected Device>	Indicate what type of device is connected to this serial IO controller
	Serial IO I2C1 Settings>	I2C IO Voltage Select>	Select 1.8 V or 3.3 V for the controller
		Connected Device>	Indicate what type of device is connected to this serial IO controller
	Serial IO SPI0 Settings>	ChipSelect Polarity>	Sets initial polarity for ChipSelect signal
	Serial IO UART0 Settings>	Bluetooth Device>	Enable/disable the vendor sensor
		Wireless Charging Mode>	Set the wireless charging mode
		Hardware Flow Control>	When enabled configures additional 2 GPIO pads for use as RTS/CTS signals for UART
	Serial IO GPIO Settings>	GPIO IRQ Route>	Route all GPIO to one of the IRQ
	WITT/MITT Test Device>	Choose if WITT Device is used and with which controller	
	UART Test Device>	Choose if UART test device is used and with which controller	
	Additional Serial IO Device>	When enabled, ACPI will report additional devices connected to Serial IO	

Function	Second level Sub-screen / Description		
Serial IO Configuration> (continued)	Serial IO Timing Parameters>	Serial IO Timing Parameters>	Serial IO timing parameter (test only)
	UCSI/UCMC Device>	If enabled, ACPI reports UCSI/UCMC device	
ISH Configuration>	ISH Controller>	Enable/disable integrated sensor hub	
	PDT Unlock Message>	Enable/disable sending of PDT unlock message to ISH(checked state) After sending, the field is set back to unchecked automatically.	
	SPI>	Enable/disable SPI	
	UART0/ UART1>	Enable/disable UART0 / UART1	
	I2C0/ I2C1/ I2C2>	Enable/disable I2C0 / I2C1 / I2C2	
	GP_0 – GP_7>	Enable/disable GP_0 / 1 / 2 / 3/ 4 / 5 / 6 / 7	
TraceHub Configuration Menu>	TraceHub Enable Mode>	Select enable /disable or debugger	
	Memory Region 0 Buffer Size>	Selects size of memory region 0 or 1 buffer size	
	Memory Region 1 Buffer Size>		
PCH Thermal Throttling Control>	Thermal Throttling Level>	Determines if the Intel suggested setting is used or a manual setting	
	DMI Thermal Setting>		
	SATA Thermal Setting>		
SB Porting Configuration>	SB Porting Configuration		
DCI Enable (HDCIEN)>	Enable/disable DCI to consent to debugging over USB3 interface		
DCI Auto Detect Enable>	Enable/disable detection of a DCI connection during BIOS post time ad enables DCI		
Debug Port Selection>	Selects kernel debug port and report in ACPI DBG2 table		
GNSS>	ISH – GNSS is connected to ISH. Serial IO UART – GNSS is connected to serial IO		
PCH LAN Controller>	Enable/disable onboard NIC		
DeepSx Power Policies>	Configure DeepSX mode configuration		
Lan Wake From DeepSx>	Enable/disable wake from DeepSx by the assertion of LAN_Wake# pin		
Wake On LAN>	Enable/disable integrated LAN to wake the system		
SLP_LAN# Low on DC Power>	Enable/disable SLP_LAN# low on DC Power		
K1 OFF>	Enable/disable K1 off feature (CLKREQ)		

Function	Second level Sub-screen / Description
Wake on WLAN and BT Enable>	Enable/disable PCI express wireless LAN and Bluetooth to wake the system.
Disable DSX ACPRESET PullDown>	Disable PCH internal ACPRESENT pulldown when DeepSx or G3 exit
CLKRUN# Logic>	Enable CLKRUN# logic to stop PCI clocks
Serial IRQ Mode>	Configures serial IRQ mode
Port 61h Bit-4 Emulation>	Emulates Port 61h bit-4 toggling in SMM
State After G3>	Specifies state to go to when power is re-applied after power failure (G3 State)
Port 80h Redirection>	Controls where port 80h cycles are sent
Enhanced Port 80 h LPC Decoding>	Supports word/dword decoding of port 80h behind LPC
Compatibility Revision ID>	Enable/disable PCH compatibility revision ID feature
PCH Cross Throttling>	Enable/disable PCH cross throttling feature Note: Only ULT supports this feature.
Disable Energy Reporting>	Enables/disables PCH energy reporting feature Note: SET to disabled. This feature is only for test purposes.
Enable TCO Timer>	Enable/disable TCO timer If disabled, PCH ACPI timer is disabled and stops TCO timer.
PCIe PLL SSC>	Selects the PCIe PLL SSC percentage (Range: 0.0 % - 2.0 %) Auto keeps hardware default, no BIOS override.
Unlock PCH P2SB>	Unlock PCH P2SB SBI and configuration space by PSF
PMC Read Disable>	Enable/disable this test feature for PMC XRAM read
Flash Protection Range Registers>	Enable/disable flash protection range registers(FPRR)
SPD Write Disable>	Enable/disable the setting for SPD write disable. For security, recommendations SPD write disable bit must be set.
ChipsetInit HECI Message>	Enable/disable ChipsetInit HECI message
Bypass ChipsetInit Sync Reset>	Sets this option to skip ChipsetInit sync reset

10.2.4. Security Setup Menu

The Security setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive. The mITX-SKL-H provides no factory-set passwords.

NOTICE

If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing <RETURN>. To set a password, enter it twice and acknowledge by pressing <RETURN>.

Table 40: Security Setup Menu Functions

Function	Description	
Administrator Password>	Sets administrator password	
User Password>	Sets user password	
Secure Boot>	Attempt Secure Boot>	Secure boot activated when platform key (PK) is enrolled, System mode is user deployed, and CSM function is disabled.
	Secure Boot Mode>	Selects between standard and custom. Customer mode – secure boot variables can be configured without authentication.
	Key Management>	Enables expert users to modify secure boot policy variables without full authentication.

If only the administrator's password is set, then only access to setup is limited. The password is only entered when entering setup.

If only the user's password is set, then the password is a power on password and must be entered to boot or enter setup. Within the setup menu the user has administrator rights.

Password length requirements are maximum 20 characters and minimum 3 characters.

10.2.4.1. Remember the password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords results in being locked out of the system.

If the system cannot be booted because the User Password or the Supervisor Password are not know, contact Kontron Support for further assistance.

HDD security passwords cannot be cleared using the above method.

10.2.5. Boot Setup Menu

The boot setup menu lists the for boot device priority order, that is generated dynamically.

Table 41: Boot Setup Menu Functions

Function	Description
Setup Prompt Timeout>	Displays number of seconds that the firmware waits before initiating the original default boot selection. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State>	Selects keyboard NumLock state
Quiet Boot>	Enable/disable quiet boot option
Boot Option #1>	Sets the system boot order
Fast Boot>	Enable/disable boot with initialization of a minimal set of devices required to launch active boot option. This has no effect for BBS boot options.
New Boot Option Policy>	Controls placement of newly detected UEFI boot options

10.2.6. Save & Exit Setup Menu

The exit setup menu provides functions for handling changes made to the UEFI BIOS settings and the exiting of the setup program.

Table 42: Save and Exit Setup Menu Functions

Function	Description
Save Changes and Exit>	Exits system after saving changes
Discard Changes and Exit>	Exits system setup without saving changes
Save Changes and Reset>	Resets system after saving changes
Discard Changes and Reset>	Resets system setup without saving changes
Save Changes>	Saves changes made so far for any setup option
Discard Changes>	Discards changes made so far for any setup option
Restore Defaults>	Restores/loads default values for all setup options
Save as User Defaults>	Saves changes made so far as user defaults
Restore User Defaults>	Restores user defaults to all setup options
UEFI Built-in EFI shell>	Attempts to launch the built-in EFI Shell
Launch EFI Shell from File System Device>	Attempts to launch EFI Shell application (Shell.efi) from one of the available file system devices

List of Acronyms

The following table does not contain the complete acronyms used in signal names, signal type definitions or similar. A description of the signals is included in the I/O Connector and Internal connector chapters within this user guide.

ACPI	Advanced Configuration and Power Interface (standard that operating systems use to perform discovery and configuration of computer hardware components, to perform power management)
ADC	Analog Digital Converter
AHCI	Advanced Host Controller Interface
AMT	Active Management Technology (intel)
API	Application programming interface, a set of routine definitions, protocols, and tools for building software and applications
AT	Adcanced Technology // Anti-Theft Technology
ATA	AT Attachment, interface standard for the connection of storage devices
ATX	Advanced Technology Extended (motherboard configuration specification)
ADC	Analog Digital Converter
BIOS	Basic Input/Output System (type of firmware used to perform hardware initialization during the booting process)
BSP	Board support package (implementation of specific support code (software) for a given (device motherboard) board that conforms to a given operating system)
BTX	Balanced Technology Extended (motherboard configuration specification)
bpp	bit per pixel
CMOS	Complementary Metal Oxide Semiconductor (technology for constructing integrated circuits)
COM	Communication Equipment (Serial Bus)
CPU	Central Processing Unit
DAC	Digital Analog Converter
DDC	Display Data Channel

DDR3	Double Data Rate (SDRAM interface)
DirectX	Collection of application programming interfaces (APIs) for handling tasks
DMA	Direct Memory Access
DP	Display Port
DXVA	DirectX Video Acceleration
ECC	Error Checking and Correction
eDP	Embedded Display Port, standardized display panel interface for internal connections
EFI	Extensible Firmware Interface
EHCI	Enhanced Host Controller Interface
EMI	Electromagnetic Interference
ESD	Electrostatic discharge
GBE	Gigabyte Ethernet
GND	Ground (Earthing)
GPIO	General-purpose input/output
HBR2	High Bit Rate (Video format)
HD	High Definition Audio (Intel)
HDD	Harddisk Drive
HDMI	High-Definition Multimedia Interface
LAN	Local Area Network
LPC	Low Pin Count (Serial Bus)
LVDS	Low-voltage differential signaling
MDI	Media Dependent Interface
mITX	MiniITX (form factor for motherboards)
mPCI	Mini PCI (small form factor expansion card utilizing serial PCI Express and USB interfaces)
mPCIe	Mini PCI Express (a small form factor expansion card utilizing serial PCI Express and USB interfaces)
mSATA	Mini SATA (interface to Harddisk oder Solid State Disks)

MTBF	Mean Time Between Failures
NCQ	Native Command Queuing
OpenGL	Application programming interface (API) for rendering vector graphics
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect (local computer bus for attaching hardware devices)
PEG	PCI Express for Graphics
PCH	Platform Controller Hub
PS/2	Interface for connecting keyboards and mice
PSU	Power Supply Unit
PWM	Pulse-width modulation
px	pixel
PXE	Preboot eXecution Environment, standardized client-server environment that boots a software assembly
RAID	Redundant Array of Independent Disks
RBR	Reduced Bit Rate (Video format)
RoHS	Restriction of Hazardous Substances
RPM	Rotations Per Minute
RRT	Rapid Recover Technology (Intel)
RST	Rapid Storage Technology (Intel)
RTC	Real Time Clock
SATA	Serial ATA (bus interface)

SIM	SIM card, subscriber identification module
SMB	System Management Bus, single-ended simple two-wire bus for the purpose of lightweight communication
SNR	Signal-to-Noise Ratio
SPD	Serial Presence Detect
SPDIF	Sony/Philips Digital Interface Format, type of digital audio interconnect
SPI	Serial Peripheral Interface
TDG	Thermal Design Guideline
TDP	Thermal Design Power
TPM	Trusted Platform Module, standard for a secure cryptoprocessor
TRIM	Command in the ATA command set
TXT	Trusted Execution Technology (Intel)
UDIMM	Unregistered Dual In-line Memory Module
UEFI	Unified Extensible Firmware Interface
USB	Universal Serial Bus
VC1	Video Coding format
VGA	Video Graphics Array, video format
vPRO	Set of features built into a PC's motherboard and other hardware (Intel)
VT-d	Virtualisation Technology for Directed I/O (Intel)
WES7	Windows Embedded System 7
XHCI	Extensible Host controller Interface

About Kontron

Kontron is a global leader in Embedded Computing Technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall. For more information, please visit: **www.kontron.com**

Global

KONTRON S&T AG

Lise-Meitner-Str. 3-5
86156 Augsburg
Germany
Tel.: + 49 821 4086-0
Fax: + 49 821 4086-111
info@kontron.com