# FWA8308 Series

**Networking Appliance** 

**User's Manual** 

Version: 1.1

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# Foreword

To prevent damage to the system board, please handle it with care and follow the measures below, which are generally sufficient to protect your equipment from static electricity discharge:

When handling the board, use a grounded wrist strap designed for static discharge elimination grounded to a metal object before removing the board from the antistatic bag. Handle the board by its edges only; do not touch its components, peripheral chips, memory modules or gold contacts.

When handling processor chips or memory modules, avoid touching their pins or gold edge fingers. Return the Network Appliance system board and peripherals back into the antistatic bag when not in use or not installed in the chassis.

Some circuitry on the system board can continue to operate even though the power is switched off. Under no circumstances should the Lithium battery cell used to power the real-time clock be allowed to be shorted. The battery cell may heat up under these conditions and present a burn hazard.

# WARNING!

1. "CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED.

REPLACE ONLY WITH SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER. DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS"

- 2. This guide is for technically qualified personnel who have experience installing and configuring system boards. Disconnect the system board power supply from its power source before you connect/disconnect cables or install/remove any system board components. Failure to do this can result in personnel injury or equipment damage.
- 3. Avoid short-circuiting the lithium battery; this can cause it to superheat and cause burns if touched.
- 4. Do not operate the processor without a thermal solution. Damage to the processor can occur in seconds.
- 5. Do not block air vents at least minimum 1/2-inch clearance required.

## Chapter 1 Introduction

FWA8308 series was specifically designed for the network security & management market.

Network Security Applications:

- Firewall
- Unified Threat Management (UTM)
- Virtual Private Network (VPN)
- Proxy Server
- Caching Server

Network Management Applications:

- Load balancing
- Quality of Service
- Remote Access Service

The FWA networking appliance product line covers the spectrum from offering platforms designed for:

- SOHO
- SMB
- Enterprise

Each product is designed to address the distinctive requirements of its respective market segment from cost effective entry-level solutions to high throughput and performance-bound systems for the Enterprise level.

# Chapter 2 System Specification

Product Name	FWA8308
Form Factor	19" 1U Mainstream Networking Product
Motherboard	MB968
Processor	<ul> <li>Support for Intel® Shark Bay DT LGA1150 Haswell processors</li> <li>TDP = 35W ~ 84W (DC / QC)</li> </ul>
Chipset	Intel <sup>®</sup> Lynx Point C226 PCH Package =23 mm x 22 mm , 0.65 mm ball pitch
Supported CPUs	<ul> <li>E3-1275 v3</li> <li>E3-1225 v3</li> <li>E3-1268L v3</li> <li>i7-4770TE</li> <li>i7-4770S</li> <li>i5-4570S</li> <li>i5-4570TE</li> <li>i3-4330</li> <li>i3-4330TE</li> <li>Celeron G1820TE</li> <li>Celeron G1820</li> <li>Pentium G3320TE</li> <li>Pentium G3420</li> </ul>
Memory	<ul> <li>Four DDR3 UDIMM total for 32GB max memory (4Gb chip support)</li> <li>Support DDR3 / DDR3L at 1.5V</li> <li>Dual channel DDR3 up to 1600 MHz</li> <li>Unbuffered</li> <li>ECC or non-ECC</li> </ul>
Network	<ul> <li>Eth1: Intel® Clarkville I217LM GbE PHY, 6mm x 6mm, QFN48 with iAMT 9.0 supporting. No Bypass</li> <li>Eth2~4: Intel® Pearsonville I210-AT. No Bypass.</li> <li>Eth5~6: Intel® Pearsonville I210-AT. Support Bypass.</li> <li>Eth7~8: Intel® Pearsonville I210-AT. Support Bypass.</li> </ul>
Expansion Slot	<ul> <li>Two PCI-e x8 Golden Finger</li> <li>CF Card Socket</li> <li>Mini PCI-e Socket (m-SATA compatible)</li> </ul>
Storage	One internal 2.5" HDD (FWA8308 & FWA8308-RPSU) One internal 3.5" HDD (FWA8308-2SLOT)
Front Panel	<ul> <li>Two RJ-45 1x4 connectors for Eth1~4 &amp; 5~6</li> <li>USB 3.0 x2</li> <li>RJ-45 (for console, COM1)</li> <li>Three LEDs for Power, Bypass &amp; Status</li> <li>Factory Mode Restore Reset Switch</li> </ul>
Rear Panel	<ul> <li>PSU inlet</li> <li>1x or 2x Slot (Depend on product SKU)</li> </ul>
USB Port	<ul> <li>Two USB 3.0 + 2.0 ports at front panel</li> <li>One USB 2.0 for Mini PCI-e</li> <li>Six USB 2.0 pin headers (pitch 2.54)</li> <li>Signal Name Pin # Pin # Signal Name VCC 1 2 Ground USB1- 3 4 USB2+ USB1+ 5 6 USB2- Ground 7 8 VCC</li> </ul>

ATM	ATM 9.0
ТРМ	Nuvoton WPCT210AA0WX TPM1.2
VGA	Pin header on board
LCM	2x16 characters LCM
Watchdog Timer	256 segments, 0, 1, 2255 sec/min
Power Supply	<ul> <li>300W Single PSU (FWA8308 &amp; FWA8308-2SLOT)</li> <li>275W 1+1 redundant PSU (FWA8308-RPSU)</li> </ul>
Dimensions	44 (H) x 440 (W) x 406.5 (D) mm
Operation Temperature	0 ~ 45 °C
Storage Temperature	-20 ~ 70 °C
Operation Humidity 5% ~ 95%	
Certifications	CE, FCC, LVD
Compatible Front Expansion Cards	<ul> <li>IBP161: 4-port RJ-45 10/100/1000 Copper LAN Module Card</li> <li>IBP162: 2-port 10 GbE SFP+ LAN Module Card</li> <li>IBP163: 2+2 ports GbE Copper or SFP LAN Module Card</li> <li>IBP164: Crypto Acceleration Card</li> <li>IBP165: 4-port RJ-45 10/100/1000 Copper LAN Module Card</li> <li>IBP167: 8-port RJ-45 10/100/1000 Copper LAN Module Card</li> <li>IP331: PCI-e 1-to-1 Riser Card</li> <li>IP332: PCI-e Adapter Card (with 2.5" HDD Interface)</li> <li>IP335: PCI-e 1-to-2 Riser Card</li> </ul>

# Chapter 3 Hardware Configuration

## **Jumper Locations on MB968**



# **Jumper Settings on MB968**

### JP2: Clear CMOS Setting

JP2	Setting
123	Normal
123	Clear CMOS

#### JP3: Clear ME Setting

JP3	Setting
123	Normal
	Clear ME

### JP9: AT / ATX Mode Setting

JP9	Setting
12	ATX
	AT

### JP12: BIOS Flash Security Setting

JP12	Setting
123	Normal
123	For BIOS Update

## JP15: LED Function Selection

JP15	Setting
123	HDD Activate
123	Bypass Activate

## J17, J18: PCIE Config Setting

J18	J17	Setting
12	00 12	2 x 8 for Golden Finger PCIE1 & PCIE2
12	00 12	1x16 for Golden Finger PCIE2

#### J2: System Function Connector

J2 provides connectors for system indicators that provide light indication of the computer activities and switches to change the computer status. J2 is a 20-pin header that provides interfaces for the following functions

#### Pin 2, 4, 6, 8: Speaker

This connector provides an interface to a speaker for audio tone generation. An 8-ohm speaker is recommended.

Pin #	Signal Name
2	SPEAKER
4	NC
6	GND
8	+5V

#### Pin 1, 3, 5: Power LED

The power LED indicates the status of the main power switch.

Pin #	Signal Name
1	+5V
3	NC
5	GND

#### Pin 13, 14: ATX Power ON Switch

This 2-pin connector is an "ATX Power Supply On/Off Switch" on the system that connects to the power switch on the case. When pressed, the power switch will force the system to power on. When pressed again, it will force the system to power off.

Pin #	Signal Name
13	GND
14	Power_ON

#### Pin 17, 18: Reset Switch

The reset switch allows the user to reset the system without turning the main power switch off and then on again. Orientation is not required when making a connection to this header.

Pin #	Signal Name	
17	GND	
18	PM_SYSRST#	

#### Pins 19, 20: HDD LED

This connector connects to the hard drive activity LED on control panel. This LED will flash when the HDD is being accessed.

Pin #	Signal Name	
19	+3.3V	
20	-HDD_LED	

#### J5: VGA Connectors

SIGNAL	Pin #	Pin #	Signal Name
NAME			
VGA_R	1	2	VGA_PWR
VGA_G	3	4	GND
VGA_B	5	6	NC
NC	7	8	VGADDCDATA
GND	9	10	HSYNC
GND	11	12	VSYNC
GND	13	14	VGADDCCLK
GND	15		

#### J6, J7, J8: USB6~USB11 Ports

00	0	0	5
	ø	0	
	0	0	
2	ø		-

SIGNA L NAME	Pin #	Pin #	Signal Name
+5V	1	2	GND
D-	3	4	D+
D+	5	6	D-
GND	7	8	+5V

#### J9: Compact Flash Socket



Note: CF card supports IDE mode only.

If CF card applied, please set the SATA configuration to "IDE mode" in BIOS.

#### J10: Mini PCI- E / mSATA Socket

#### J11: SPI Debug Port

9 0 0 0 0 3 10 0 0 0 0 0 2

1	SIGNAL NAME	Pin #	Pin #	Signal Name
			2	NC
J	SPI_CS# 0	3	4	+3.3V
	SPI_SO	5	6	SPI0_HOLD#
	SPI0_WP#	7	8	SPI_CLK
	GND	9	10	SPI_SI

#### J12: Digital IO 4-IN / 4-OUT Connector

0 0 0 2	SIGN AL NAME	Pin #	Pin #	Signal Name
0	GND	1	2	+5V
<u> </u>	OUT3	3	4	OUT1
	OUT2	5	6	OUT0
	IN3	7	8	IN1
	IN2	9	10	IN0

#### J13: LPC Debug Port

0000

Signal Name	Pin #	Pin #	Signal Name
LPC_AD0	1	2	SIO_PLTRST#
LPC_AD1	3	4	LPC_FRAME#
LPC_AD2	5	6	+3.3V
LPC_AD3	7	8	Ground
LPC_CLK	9		

#### J15, J16, J20: Serial Port (COM1~COM3)

	Signal Name	Pin #	Pin #	Signal Name
00	DCD#	1	6	DSR#
005	SIN	2	7	RTS#
	SOUT	3	8	CTS#
	DTR#	4	9	RI#
	GND	5		

#### J19, J25: ATX Power Connector

#### J21, J22, J23: Power Connector, Pitch 2.54mm

	Pin #	Signal Name
	1	+5V
	2	Ground
•	3	Ground
	4	+12V

#### J24: Power Connector, Pitch 2.0mm

	Pin #	Signal Name
-	1	+5V
<del>.</del>	2	Ground
	3	Ground
	4	+12V

#### J27: mSATA Socket

0000

#### CN1, CN3: HDD Serial ATA Connector

-

#### CPU\_FAN1: CPU Fan Connector

CPU\_FAN1 is a 4-pin header for the CPU fan. The fan must be 12V (Max. 1A).



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Rotation control
	Pin # 1 2 3 4

#### FAN1, FAN2, FAN3: System Fan Connectors

FAN1, FAN2, FAN3 is a 4-pin header for system fans. The fan must be 12V (Max. 1A).

	+
 4	

Pin #	Signal Name			
1	Ground			
2	+12V			
3	Rotation detection			
4	Rotation control			

#### LED4: Status LED

A1 & C1 : Status LED

A2 & C2 : Bypass or HDD status LED A3 & C3 : Power LED

Status Bypass or HDD	SIGNAL NAME	Pin #	Pin #	Signal Name
<b></b>	SIO_GPIO33	A1	C1	SIO_GPIO32
Power	+5 V	A2	C2	JP15 Selection
ή <del>, </del> ή	+3.3 V	A3	C3	GND

#### SW1: Software reset button

I/O base :

Read IO 0x1C00 and set bit 7 to "1" (Enable GPIO function) Read IO 0x1C04 and set bit 7 to "1" (GPIO act as GPI) Read IO 0x1C0C and set check bit 7 (Control Pin)



Signal Name	Pin #	Pin #	Signal Name
GND	1	2	PCH GPIO7



# **Rear Panel Features**

# FWA8308 & FWA8308-2SLOT



# FWA8308-RPSU



# Chapter 4 Console Mode Information

FWA8308 supports output information via Console in BIOS level.

Prepare a computer as client loaded with an existing OS such as Windows XP and Windows 7. Connect client computer and FWA8308 with NULL Modem cable. Follow the steps below to configure the Windows Hyper Terminal application setting:

- 1. Execute Hyper Terminal. Issue command "hypertrm".
- 2. Customize your name for the new connection.

Connection De	scription		?	
New Co	nnection			
Enter a name ar	d choose an icon	for the conne	ction:	
Console				
Icon:				
	A 10			
		g 😒		8
<u></u>				
	ſ	ОК	Cancel	
0014			<b>C</b> 11	
noose COM p	ort on the cliei	nt computer	for the co	nnect
onnect lo				
🙈 Console				
Enter details for	he phone numbe	r that you wan	t to dial:	
Country/region:	United States (1	)	~	
	-			

3.

Phone number:

Connect using:

COM1

COM1 COM2

TCP/IP (Winsock)

V

4. Please make the port settings to Baud rate 19200, Parity None, Data bits 8, Stop bits 1

🥙 Console - HyperTerminal 📃 🗖 🔀	
File Edit View Call Transfer Help	1
Connected 0:00:02 Auto detect Auto detect SCROLL CAPS NUM Capture	

5. Power on FWA8308.

Press <**Tab**> key to enter BIOS setup screen in **Console mode**. Press <**Del**> key to enter BIOS setup screen in **VGA mode**.



Fig. 5-2 Take off six screws and open the top lead

Fig. 5-3 The base stand

# Chapter 6 Installing DDR3 Memory

Install system memory by pulling the socket's arm and pressing it into the slot gently.



Fig. 6-1 Open both arms on DIMM socket

Fig. 6-2 Install DIMM

## Notice:

1. MB968 supports two groups of dual channels memory.

One group is on the black DIMM sockets, and the other one is blue DIMM sockets.

2. The recommended height of memory module doesn't exceed 30 mm.

# Chapter 7 Installing CompactFlash Card

Insert CompactFlash card into the socket.



Fig. 7-1 Insert CompactFlash Card into the CF interface

Fig. 7-2 Completion of CompactFlash Card connection

# Chapter 8 Removing and Installing the Battery

- 1. Press the metal clip back to eject the button battery.
- 2. Replace it with a new one by pressing the battery with fingertip to restore the battery



Fig. 8-1 Eject the battery and replace with new one

Chapter 9 Installing 2.5" HDD (FWA8308 & FWA8308-RPSU)



Fig. 9- Take off two screws on bottom to remove 2.5" HDD bracket.



Fig. 9-2 Fasten the four screws to lock HDD and bracket together.



Fig. 9-3 Push HDD into connector

Fig. 9-4 Completion of HDD connection



Fig. 9-5 Fix HDD bracket with two screws

# Chapter 10 Installing Optional Dual 2.5" HDD Kit

The following is for optional Dual 2.5" HDD kit:



*Fig. 10-1* Push eight shock-absorbent pads to fasten HDD bracket.



*Fig. 10-2* Fasten the screws to lock 2.5" HDD bracket and bracket together.



Fig. 10-3 Fix HDD bracket on chassis with four screws

# Chapter 11 Installing Add-on Card





Fig. 11-1 Loosen screw on slot bracket.

Fig. 11-2 Slide in PCI-e add-on card.



Fig. 11-3 Fix the add-on card

Chapter 12 Installing Mini PCI-e Card



Fig. 12-1 Insert Mini PCI-e card.

Fig. 12-2 Push down Mini PCI-e card & fix it with two M2 screws

## Chapter 13 BIOS Information

This setup allows you to view processor configuration used in your computer system and set the system time and date.

#### **Main Settings**

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.

Main	Advanced	Chipset	Boot	Security	y Save & Exit
BIOS In	formation				Choose the system default language
System	Language		[English]		$\rightarrow \leftarrow \texttt{Select Screen}$
System	Date		[Fri 02/21/2014]		†↓ Select Item
System	Time		[10:30:55]		Enter: Select
Access	Level		Administrator		+- Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit

#### System Language

Choose the system default language.

#### System Date

Set the Date. Use Tab to switch between Data elements.

#### **System Time**

Set the Time. Use Tab to switch between Data elements.

#### **Advanced Settings**

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

			Aptio Set	up Utility	
Main	Advanced	Chipset	Boot	Security	/ Save & Exit
<ul> <li>PC</li> <li>ACC</li> <li>Wa</li> <li>CP</li> <li>SA</li> <li>This</li> <li>LAI</li> <li>Inte</li> <li>Inte</li> <li>Inte</li> <li>AM</li> <li>Acc</li> <li>US</li> <li>F8'</li> <li>Sei</li> </ul>	I Subsystem Setting PI Settings Ike up event setting U Configuration TA Configuration atdown Temperature N Bypass Configuration atd(R) Rapid Start Te el TXT(LT) Configuration sustic Management B Configuration 1866 Super IO Confi 866 H/W Monitor rial Port Console Re	e Configuration tion chnology ation nology Config Configuration iguration direction	ura		<ul> <li>→ ←Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>

#### **PCI Subsystem Settings**

	3-		Aptio Setup U	Itility	
Main	Advanced	Chipset	Boot	Securit	y Save & Exit
PCI B PCI C PCI La VGA F PERR SERR ► PC	us Driver Version ommon Settings atency Timer Palette Snoop # Generation # Generation I Express Settings		V 2.05.02 [32 PCI Bus 0 [Disabled] [Disabled] [Disabled]	Clocks]	<ul> <li>→ ←Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>

#### **PCI Latency Timer**

Value to be programmed into PCI Latency Timer Register.

#### **VGA Palette Snoop**

Enables or disables VGA Palette Registers Snooping.

#### **PERR# Generation**

Enables or disables PCI device to generate PERR#.

#### **SERR# Generation**

Enables or disables PCI device to generate SERR#.

#### **PCI Express Settings**

Change PCI Express devices settings.

#### **PCI Express Settings**

				-	
Main Ac	dvanced	Chipset	Boot	Securit	y Save & Exit
PCI Expres	s Device Regist	er Settings			
Relaxed Or	dering		[Disabled]		
Extended T	ag		[Disabled]		
No Snoop			[Enabled]		
Maximum F	Payload		[Auto]		$\rightarrow \leftarrow \texttt{Select Screen}$
Maximum F	Read Request		[Auto]		†↓ Select Item
					Enter: Select
PCI Expres	s Link Register	Settings			+- Change Field
ASPM Sup	port		[Disabled]		F1: General Help
WARNING	Enabling ASP	M may cause	some		F2: Previous Values
	PCI-E device:	s to fail			F3: Optimized Default
Extended S	Synch		[Disabled]		F4: Save ESC: Exit
Link Trainir	ig Retry		[5]		
Link Trainir	ig Timeout		100		
Unpopulate	d Links		[Keep Link ON]		
Restore PC	IE Register		[Disabled]		

Antio Setup Utility

#### **Relaxed Ordering**

Enables or disables PCI Express Device Relaxed Ordering.

#### **Extended Tag**

If ENABLED allows device to use 8-bit Tag field as a requester.

#### No Snoop

Enables or disables PCI Express Device No Snoop option.

#### **Maximum Payload**

Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

#### **Maximum Read Request**

Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

#### **ASPM Support**

Set the ASPM Level: Force LOs – Force all links to LOs State: AUTO – BIOS auto configure : DISABLE – Disables ASPM.

#### **Extended Synch**

If ENABLED allows generation of Extended Synchronization patterns.

#### Link Training Retry

Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

#### Link Training Timeout

Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 1000 uS.

#### **Unpopulated Links**

In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.

#### **ACPI Settings**

	Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Securit	y Save & Exit	
ACPI S	Settings e ACPI Auto Conf		[Disabled]		→ ←Select Screen ↑↓ Select Item	
Enable ACPI S Lock L S3 Vid	e Hibernation Sleep State egacy Resources eo Repost		[Enabled] [S1 only (CPU [Disabled] [Disabled]	Stop C]	Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit	

#### **Enable Hibernation**

Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

#### **ACPI Sleep State**

Select ACPI sleep state the system will enter, when the SUSPEND button is pressed.

#### Lock Legacy Resources

Enabled or Disabled Lock of Legacy Resources.

#### S3 Video Repost

Enable or disable S3 Video Repost.

#### Wake up event settings

Settin	igo		Aptio Setup U	tility	
Main	Advanced	Chipset	Boot	Security	Save & Exit
Wake	system with Fixed T	ime	[Disabled]		
Wake	on Ring		[Enabled]		
Wake	on PCI PME		[Enabled]		
Wake	on PCIE Wake Ever	nt	[Enabled]		$\rightarrow$ $\leftarrow$ Select Screen
					†↓ Select Item
					Enter: Select
					+- Change Field
					F1: General Help
					F2: Previous Values
					F4: Save ESC: Exit

#### Wake system with Fixed Time

Enables or Disables System wake on alarm event. When enabled, System will wake on the hr::min:: sec specified.

#### Wake on PCIE PME Wake Event

The options are Disabled and Enabled.

#### **Trusted Computing**

ating			Aptio Setup U	Itility	
Main	Advanced	Chipset	Boot	Security	Save & Exit
Config Secu	uration rity Device Sup		[Disabled]		→ ←Select Screen
Currer SUP	nt TPM Status Inform	nation F			<pre>↑ ↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit</pre>

#### Security Device Support

Enables or disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

#### **CPU Configuration**

This section shows the CPU configuration parameters.

		Aprilo Setup	otility	
Main Advanced	Chipset	Boot	Securit	y Save & Exit
CPU Configuration				
Intel(R) Xeon(R) CPU E3-1 CPU Signature Processor Family Microcode Patch FSB Speed Max CPU Speed Min CPU Speed CPU Speed Processor Cores Intel HT Technology Intel VT-x Technology Intel SMX Technology G4-bit EIST Technology CPU C3 state CPU C6 state CPU C6 state CPU C6 state CPU C7 state L1 Data Cache L1 Code Cache L2 Cache L3 Cache Hyper-threading Active Processor Cores Limit CPUID Maximum Execute Disable Bit Intel Virtualization Hardware Prefetcher Adjacent Cache Line Prefet CPU AEC	268L v3 @	2.30GHz 306c3 6 16 100 MHz 2300 MHz 2700 MHz 4 Supported		<ul> <li>→ ←Select Screen</li> <li>↑↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>

#### Hyper-threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled, only one thread per enabled core is enabled.

#### **Active Processor Cores**

Number of cores to enable in each processor package.

#### Limit CPUID Maximum

Disabled for Windows XP.

#### **Execute Disable Bit**

XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, Re33dHat Enterprise 3 Update 3.)

#### **Intel Virtualization Technology**

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

#### Hardware Prefetcher

To turn on/off the Mid level Cache (L2) streamer Prefetcher.

#### **Adjacent Cache Line Prefetch**

To turn on/off prefetching of adjacent cache lines.

SATA Devices Configuration.

			Aptio	Setup Utility	
Main	Advanced	Chipset	Boot	Security	/ Save & Exit
SATA C SATA M SATA P Softw SATA P Softw SATA P Softw SATA P Softw SATA P Softw SATA P Softw	Controller(s) Node Selection vare Preserve vort1 vare Preserve vort2 vare Preserve vort3 vare Preserve vort4 vare Preserve vort5 vare Preserve		[Enabled] [AHCI] Empty Unknown Empty Unknown Empty Unknown Empty Unknown Empty Unknown		<ul> <li>→ ← Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>
50111					

#### SATA Controller(s)

Enable / Disable Serial ATA Controller.

#### **SATA Mode Selection**

(1) IDE Mode.
 (2) AHCI Mode.

(3) RAID Mode.

#### **Thermal Configuration**

guran	Aptio Setup Utility							
Main	Advanced	Chipset	Boot	Security	Save & Exit			
► Platfor	m Thermal Configu	uration						

#### **Platform Thermal Configuration**

	U		Aptio S	etup Utility		
Main	Advanced	Chipset	Boot	Security	Save & Exit	
Platform T	hermal Configurat	ion				
Automatic Active Trip Active Trip	Thermal Rep Point 0 F Point 1		[Enabled] 100 [55 C]			
Active Trip Passive Passive	o Point 1 F e TC1 Value e TC2 Value		75 1 5			
Passive	e TSP Value		10			
PCH Ther	mal Device		[Disabled]			

#### Automatic Thermal Reporting

Configure CRT, PSV and ACO automatically based on values recommended in BWG's thermal reporting for thermal management settings. Set to Disable for manual configuration.

#### **Shutdown Temperature Configuration**

			Aptio S	etup Utility		
Main	Advanced	Chipset	Boot	Security	Save & Exit	
APCI Shi	utdown Temperatur	e	[Disabled]			

#### ACPI Shutdown Temperature

Set function Disabled or 70/75/80/85/90/95/100 °C

#### LAN Bypass Configuration

			Aptio	Setup Utility		
Main	Advanced	Chipset	Boot	Security	Save & Exit	
LAN Bypa	ass Configuration					
Bypass C	Quick Setting		[Normal]			

#### **Bypass Quick Setting**

Set LAN Bypass to Normal, Bypass, Firewall or Custom Define Mode

Normal mode: All LAN ports in NORMAL. When Watchdog monitor system hangs, software will initiates a system reboot. Bypass mode: All LAN ports in BYPASS during power-off or watchdog initiates Bypass. System will not reboot. Firewall mode: All LAN ports in BYPASS until software change it to NORMAL under OS. When watchdog monitors system hang, software will initiates a system reboot.

Custom Define mode: Customer defines watchdog reset, watchdog Bypass and power-off Bypass settings.

			Aptio Setu	ıp Utility	
Main	Advanced	Chipset	Boot	Security	Save & Exit
LAN Byp	ass Configuration				
Bypass	Quick Setting		[Custom Define]		
WDT Re	eset Signal		[Disabled]		
WDT By	pass Setting				
LAN	5 LAN6 Bypass		[Normal]		
LAN	7 LAN8 Bypass		[Normal]		
Ext L	AN1 LAN2 Bypass		[Normal]		
Ext L	AN3 LAN4 Bypass		[Normal]		
System	OFF Bypass Setting				
LAN	5 LAN6 Bypass		[Normal]		
LAN	7 LAN8 Bypass		[Normal]		
Ex	t LAN1 LAN2 Bypass		[Normal]		
Ex	t LAN3 LAN4 Bypass		[Normal]		

Note: "Ext LAN Bypass" items only appear when extended IBASE LAN module card installed.

#### AMT Configuration

		Aptio	Setup Otinity	
Main Advanced	Chipset	Boot	Security	Save & Exit
Intel AMT BIOS Hotkey Pressed MEBx Selection Screen Hide Un-Configure ME Confi Un-Configure ME Amt Wait Timer Disable ME ASF Activate Remote Assistance USB Configure PET Progress AMT CIRA Timeout Watchdog OS Timer BIOS Timer	firmation Process	[Enabled] [Disabled] [Disabled] [Disabled] [Disabled] [Enabled] [Enabled] [Enabled] [Enabled] 0 [Disabled] 0 [Disabled] 0	→ En: +- F1 F2 F3 F4	← Select Screen Select Item ter: Select Change Field : General Help : Previous Values : Optimized Default : Save ESC: Exit

#### **AMT Configuration**

Options are Enabled and Disabled.

Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

#### **Unconfigure ME**

Perform AMT/ME unconfigure without password operation.

#### **Amt Wait Timer**

Set timer to wait before sending ASF\_GET\_BOOT\_OPTIONS.

#### **Activate Remote Assistance Process**

Trigger CIRA boot.

**PET Progress** 

User can Enable/Disable PET Events progress to receive PET events or not.

#### Watchdog Timer

Enable/Disable Watchdog Timer.

#### **Acoustic Management Configuration**

			Aptio S	Setup Utility	
Main	Advanced	Chipset	Boot	Security	Save & Exit
Acoustic	Management Confi	iguration			
Automatie	c Acoustic Manage	ment	[Disabled]	-	$\rightarrow$ $\leftarrow$ Select Screen
					∱↓Select Item
				E	Inter: Select
				4	- Change Field
				E	1:General Help
				E	2: Previous Values
				E	3: Optimized Default
				F	4: Save ESC: Exit

Smart fan function Enable or Disable.

#### **USB** Configuration

			Aptio S	Setup Utility	
Main	Advanced	Chipset	Boot	Security	y Save & Exit
USB Cor	nfiguration				
USB Dev 1 K	vices: Teyboard, 1 Mouse,	2 Hubs			
Legacy L USB3.0 S XHCI Ha EHCI Ha Port 60/6	JSB Support Support nd-off nd-off 4 Emulation		[Enabled] [Enabled] [Enabled] [Disabled] [Enabled]		→ ← Select Screen ↑↓ Select Item Enter: Select +- Change Field F1: General Help
USB hard USB Trai Device re Device p	dware delays and ti nsfer time-out eset tine-out ower-up delay	me-outs:	[20 sec] [20 sec] [Auto]		F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

#### Legacy USB Support

Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

#### USB3.0 Support

Enable/Disable USB3.0 (XHCI) Controller support.

#### **XHCI Hand-off**

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

#### **EHCI Hand-off**

Enabled/Disabled. This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

#### Port 64/60 Emulation

Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.

#### **USB Transfer time-out**

The time-out value for Control, Bulk, and Interrupt transfers.

#### **Device reset tine-out**

USB mass Storage device start Unit command time-out.

#### **Device power-up delay**

Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

#### F81866 Super IO Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
Super IO F81866 S Serial Serial Power KB/MS	Configuration Super IO Chip Port 0 Configuration Port 1 Configuration Failure S Power On	Cilipset	F81866 [Always off] [None]	→ ← ↑ ↓ Ente +- F1: F2: F3: F4:	- Select Screen Select Item er: Select Change Field General Help Previous Values Optimized Default Save ESC: Exit

#### **Serial Port Configuration**

Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.

#### F81866 H/W Monitor

			Aptio S	etup Utility	
Main	Advanced	Chipset	Boot	Security	Save & Exit
PC Health	Status				
Fan1 smart Fan2 smart Fan3 smart System ten System ten FAN1 Spee FAN2 Spee FAN3 Spee VIN1 VIN2 VIN2 VIN3 VSB5V VCC3V VSB3V VBAT	t fan control t fan control f fan control nperature1 nperature2 nperature3 ed ed		[50 C] [50 C] [Disabled] +41 C +38 C +37 C 1545 RPM 1546 RPM 1546 RPM +1.776 V +5.171 V +12.408 V +5.016 V +3.392 V +3.392 V +3.264 V	<pre></pre>	<ul> <li>← Select Screen</li> <li>Select Item</li> <li>cr: Select</li> <li>Change Field</li> <li>General Help</li> <li>Previous Values</li> <li>Optimized Default</li> <li>Save ESC: Exit</li> </ul>

#### **Temperatures/Voltages**

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are readonly values as monitored by the system and show the PC health status.

#### Fan1/Fan2/Fan3 Smart Fan Control

This field enables or disables the smart fan feature. At a certain temperature, the fan starts turning. Once the temperature drops to a certain level, it stops turning again.

#### **Chipset Settings**

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

		A	ptio Setup I	Utility	
Main	Advanced	Chipset	Boot	Security	Save & Exit
► PCH ► Syst	I-IO Configuration em Agent (SA) Co	) onfiguration		- 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	<ul> <li>→ ←Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>

#### **PCH-IO Configuration**

This section allows you to configure the North Bridge Chipset.

			Aptio	Setup Utility	
Main	Advanced	Chipset	Boot	Securit	y Save & Exit
Intel PCH Intel PCH Intel PCH PCI E VUSB ( PCH / BIOS	H RC Version H SKU Name H Rev ID xpress Configurati Configuration Azalia Configurati Security Configur	tion on ation	1.6.2.0 C226 O5/C2		
PCH LAI Wake DeepSx Display L CLKRUN SB CRIE SLP_S4 Restore	N Controller on LAN Power Policies .ogic J# Logic Assertion Width AC Power Loss		[Enabled] [Enabled] [Disabled] [Enabled] [Disabled] [A-5 Seconds [Last State]	]	<ul> <li>→ ← Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>

#### **PCH LAN Controller**

Enable or disable onboard NIC.

#### Wake on LAN

Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)

#### SLP\_S4 Assertion Width

Select a minimum assertion width of the SLP\_S4# signal.

#### **Restore AC Power Loss**

Select AC power state when power is re-applied after a power failure.

#### **PCI Express Configuration**

Main	Advanced	Chipset	Boot	Securit	y Save & Exit
PCI Expr	ess Configuratior	ı			
PCI Expr	ess Clock Gating		[Enabled]		
DMI Link	ASPM Control		[Enabled]		
DMI Link	Extended Synch	Control	[Disabled]		
PCIE Ro	ot Port Function		[Disabled]		
Subtracti	ve Decode		[Disabled]		
PCIE	Port 1 is assign				
PCI E:	xpress Root Port	2			$\rightarrow$ $\leftarrow$ Select Screen
PCI E:	xpress Root Port	3			↑↓ Select Item
PCI E:	xpress Root Port	4			Enter: Select
PCI E:	xpress Root Port	5			+- Change Field
PCI E:	xpress Root Port	6			F1: General Help
PCI E:	xpress Root Port	7			F2: Previous Values
PCI E:	xpress Root Port	8			F3: Optimized Default
					F4: Save ESC: Exit

#### **PCI Express Clock Gating**

Enable or disable PCI Express Clock Gating for each root port.

#### DMI Link ASPM Control

The control of Active State Power Management on both NB side and SB side of the DMI link.

#### **PCIE Root Port Function**

Enable or disable PCI express Root Port function swapping.

#### USB Configuration

Main	Advanced	Chipset	Boot	Securit	y Save & Exit
USB Con	figuration				
USB Pree XHCI Mo BTCG	condition de		[Disabled] [Smart Auto] [Enable]		→ ← Select Screen ↑↓ Select Item Enter: Select +- Change Field
USB Port	s Per-Port Disab	le Control	[Disabled]		F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

#### **USB** Precondition

Precondition work on USB host controller and root ports for faster enumeration.

#### **xHCI Mode**

Mode of operation of xHCI controller

#### BTCG

Enable or disable trunk clock gating.

#### **USB Ports Per-Port Disable Control**

Control each of the USB ports (0~13) disabling.

#### PCH Azalia Configuration

Main Ad	vanced	Chipset	Boot	Security	y Save & Exit
PCH Azalia Co Azalia Azalia Doc Azalia PMI	nfiguration king Support E		[Auto] [Disabled] [Disabled]		<ul> <li>→ ← Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>

#### Azalia

Control Detection of the Azalia device. Disabled = Azalia will unconditionally disabled. Enabled Azalia will be unconditionally enabled. Auto = Azalia will enabled if present, disabled otherwise.

#### System Agent (SA) Configuration

(° ) ° ° <b>J</b>		Aptio	Setup Utility	
Main Advanced	Chipset	Boot	Securit	y Save & Exit
System Agent Bridge Nam	e	Haswell		
System Agent RC Version		1.6.2.0		
VT-d Capability		Supported		
VT-d		[Enabled]		
CHAP Device (B0:D7:F0)		[Disabled]		$\rightarrow$ $\leftarrow$ Select Screen
Thermal Device (B0:D4:F0	)	[Disabled]		↑↓ Select Item
Enable NB CRID		[Disabled]		Enter: Select
BDAT ACPI Table Support		[Disabled]		+- Change Field F1: General Help
<ul> <li>Graphics Configuration</li> </ul>				F2: Previous Values
DMI Configuration				F3: Optimized Default
NB PCIe Configuration				F4: Save ESC: Exit
<ul> <li>Memory Configuration</li> </ul>				
<ul> <li>Memory Thermal Config</li> </ul>	uration			
<ul> <li>GT – Power Manageme</li> </ul>	nt Control			

#### VT-d

Check to enable VT-d function on MCH.

#### Enable NB CRID

Enable or disable NB CRID WorkAround.

#### **Graphics Configuration**

.9			Aptio S	Setup Utility	
Main	Advanced	Chipset	Boot	Security	Save & Exit
Graphics IGFX VB IGfx Frec Graphics	Configuration IOS Version Juency Turbo IMON		2164 700 MHz 31		
Primary I Internal 0 GTT Size Aperture DVMT Pr DVMT To Gfx Low Graphics ► LCD 0	Display Graphics Size e-Allocated otal Gfx Mode Power Mode Performance Control		[Auto] [Auto] [2MB] [256MB] [32M] [256M] [Enabled] [Disabled]	→ Er +- F7 F3 F4	<ul> <li>← Select Screen</li> <li>↓ Select Item</li> <li>nter: Select</li> <li>− Change Field</li> <li>1: General Help</li> <li>2: Previous Values</li> <li>3: Optimized Default</li> <li>4: Save ESC: Exit</li> </ul>

#### **Primary Display**

Select which of IGFX/PEG/PCI graphics device should be primary display or select SG for switchable Gfx.

#### **Internal Graphics**

Keep IGD enabled based on the setup options.

#### **DVMT Pre-Allocated**

Select DVMT 5.0 Pre-Allocated (Fixed) graphics memory size used by the internal graphics device.

#### **DVMT Total Gfx Mem**

Select DVMT 5.0 total graphics memory size used by the internal graphics device.

#### Gfx Low Power Mode

This option is applicable for SFF only.

#### Primary IGFX Boot Display (LCD Control)

Select the Video Device that will be activated during POST. This has no effect if external graphics present. Secondary booty display selection will appear based on your selection. VGA modes will be supported only on primary display.

#### **Memory Configuration**

J			Aptio	Setup Utility	
Main Ad	lvanced	Chipset	Boot	Security	/ Save & Exit
Memory Inform	nation				
Memory Frequ Total Memory DIMM#0 DIMM#1 DIMM#2 DIMM#3 CAS Latency Minimum dela CAS to R Row Prec Active to I XMP Profile 1	uency (tCL) y time AS (tRCDmi harge (tRPn Precharge (t	n) nin) RASmin)	1600 MHz 32768 MB (D 8192 MB (DI 8192 MB (DI 8192 MB (DI 8192 MB (DI 11 11 11 28 Not Supporte	DDR3) DR3) DR3) DR3) DR3) DR3) DR3)	<ul> <li>→ ← Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>

Aptio Setup Utility

Main /	Advanced	Chipset	Boot	Securit	y Save & Exit
Boot Config Setup Pror Bootup Nu	guration npt Timeout mLock State		1 [On]		
Quiet Boot			[Disabled]		
Fast Boot			[Disabled]		$\rightarrow$ $\leftarrow$ Select Screen
Boot mode	select		[LEGACY]		↑↓ Select Item Enter: Select
FIXED BO	OT ORDER Pri	orities			+- Change Field
Boot Optio	n #1		[Hard Disk]		F1: General Help
Boot Optio	n #2		[CD/DVD]		F2: Previous Values
Boot Optio	n #3		[USB Hard [	Disk]	F3: Optimized Default
Boot Optio	n #4		[USB CD/D\	/D]	F4: Save ESC: Exit
Boot Optio	n #5		[USB Key]		
Boot Optio	n #6		[USB Floppy	/]	
Boot Optio	n #7		[Network]		
► CSM16	parameters				

#### **Setup Prompt Timeout**

Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

#### **Bootup NumLock State**

Select the keyboard NumLock state.

#### **Quiet Boot**

Enables/Disables Quiet Boot option.

#### Fast Boot

Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

#### **Boot Option Priorities**

Sets the system boot order.

#### CSM16 parameters

This section allows you to configure the boot settings.

			Aptio S	Setup Utility	
Main	Advanced	Chipset	Boot	Security	Save & Exit
CSM16 Pa	arameters				
CSM16 M	odule Version		07.70	-	→ ← Select Screen ↑↓ Select Item
GateA20 A	Active		[Upon Re	equest]	Enter: Select
Option RC	M Messages		[Force BI	OS]	+- Change Fleid Fl: Ceneral Help
INT19 Tra	p Response		[Immedia	ite] 1 1 1	F1: General help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

#### GateA20 Active

UPON REQUEST: GA20 can be disabled using BIOS services ALWAYS: do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

#### **Option ROM Messages**

Set display mode for Option ROM

#### **INT19 Trap Response**

BIOS reaction on INT19 trapping by option ROM: IMMEDIATE: execute the trap right away. POSTPONED: execute the trap during legacy boot.

#### **Security Settings**

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio	Setup	Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
Passw	ord Description				
If ONL this on for whe If ONL power or ente Admini The pa in the f Minimu Maxim	Y the Administrator ly limit access to Sr en entering Setup. Y the User's passw on password and r r Setup. In Setup ti strator rights ssword length mus ollowing range: Im length um length	's password is si etup and is only a vord is set, then t nust be entered t he User will have it be	et, then asked his is a to boot 3 3 20		<ul> <li>→ ←Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>
Admini	strator Password				
User P	assword				

#### **Administrator Password**

Set Setup Administrator Password.

#### **User Password**

Set User Password.

#### Save & Exit Settings

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	/ Save & Exit
Save (	Changes and Exit				
Discar	d Changes and Exit				
Save (	Changes and Reset				
Discar	d Changes and Rese	t			$\rightarrow \leftarrow \texttt{Select Screen}$
Save ( Save (	Options Changes				↑↓ Select Item Enter: Select +- Change Field
Discar	d Changes				F1: General Help F2: Previous Values
Restor	re Defaults				F3: Optimized Default
Save a	as User Defaults				F4: Save ESC: Exit
Restor	re User Defaults				
Boot C	Boot Override				
Launc	h EFI Shell from files	stem device			

#### Save Changes and Exit

Exit system setup after saving the changes.

#### **Discard Changes and Exit**

Exit system setup without saving any changes.

#### Save Changes and Reset

Reset the system after saving the changes.

#### **Discard Changes and Reset**

Reset system setup without saving any changes.

#### **Save Changes**

Save Changes done so far to any of the setup options.

#### **Discard Changes**

Discard Changes done so far to any of the setup options.

#### **Restore Defaults**

Restore/Load Defaults values for all the setup options.

#### Save as User Defaults

Save the changes done so far as User Defaults.

#### **Restore User Defaults**

Restore the User Defaults to all the setup options.

## Chapter 14 Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

This code and information is provided "as is" without warranty of any kind, either expressed or implied, including but not limited to the implied warranties of merchantability and/or fitness for a particular purpose.

```
//-
\parallel
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND. EITHER EXPRESSED OR IMPLIED. INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
\parallel
//--
             _____
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81866.H"
//____
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//---
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;
        char SIO;
        printf("Fintek 81866 watch dog program\n");
        SIO = Init_F81866();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81866, program abort.\n");
                return(1);
        }//if (SIO == 0)
        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return (1);
        }
        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);
        if (bTime)
                EnableWDT(bTime);
                                          }
        {
        else
        {
                DisableWDT(); }
```

}

```
//-
void EnableWDT(int interval)
{
        unsigned char bBuf;
        bBuf = Get_F81866_Reg(0x2B);
        bBuf &= (\sim 0x20);
        Set F81866 Reg(0x2B, bBuf);
                                                                         //Enable WDTO
        Set_F81866_LD(0x07);
                                                                         //switch to logic device 7
        Set_F81866_Reg(0x30, 0x01);
                                                                         //enable timer
        bBuf = Get_F81866_Reg(0xF5);
        bBuf &= (~0x0F);
        bBuf |= 0x52;
        Set_F81866_Reg(0xF5, bBuf);
                                                                         //count mode is second
        Set F81866 Reg(0xF6, interval);
                                                                 //set timer
        bBuf = Get F81866 Reg(0xFA);
        bBuf |= 0x01;
        Set F81866 Reg(0xFA, bBuf);
                                                                         //enable WDTO output
        bBuf = Get F81866 Reg(0xF5);
        bBuf |= 0x20;
        Set_F81866_Reg(0xF5, bBuf);
                                                                         //start counting
}
//-
void DisableWDT(void)
{
        unsigned char bBuf;
        Set_F81866_LD(0x07);
                                                                         //switch to logic device 7
        bBuf = Get_F81866_Reg(0xFA);
        bBuf &= \sim 0x01;
        Set F81866 Reg(0xFA, bBuf);
                                                                         //disable WDTO output
        bBuf = Get_F81866_Reg(0xF5);
        bBuf &= ~0x20;
        bBuf |= 0x40;
        Set F81866 Reg(0xF5, bBuf);
                                                                         //disable WDT
}
//--
//--
          _____
\parallel
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
\parallel
//--
                           _____
#include "F81866.H"
#include <dos.h>
//----
unsigned int F81866 BASE;
void Unlock F81866 (void);
void Lock_F81866 (void);
11-
unsigned int Init_F81866(void)
{
        unsigned int result;
        unsigned char ucDid;
        F81866 BASE = 0x4E;
        result = F81866_BASE;
```

```
ucDid = Get F81866 \text{Reg}(0x20);
       if (ucDid == 0x07)
                                                             //Fintek 81866
               goto Init_Finish; }
       F81866 BASE = 0x2E;
       result = F81866 BASE;
       ucDid = Get_F81866_Reg(0x20);
       if (ucDid == 0x07)
                                                             //Fintek 81866
               goto Init_Finish; }
       {
       F81866 BASE = 0x00;
       result = F81866_BASE;
Init Finish:
       return (result);
}
//-
void Unlock_F81866 (void)
{
       outportb(F81866 INDEX PORT, F81866 UNLOCK);
       outportb(F81866 INDEX PORT, F81866 UNLOCK);
}
11-
void Lock F81866 (void)
{
       outportb(F81866 INDEX PORT, F81866 LOCK);
}
//-----
void Set_F81866_LD( unsigned char LD)
{
       Unlock_F81866();
       outportb(F81866_INDEX_PORT, F81866_REG_LD);
       outportb(F81866_DATA_PORT, LD);
       Lock_F81866();
}
//-
void Set F81866 Reg( unsigned char REG, unsigned char DATA)
{
       Unlock F81866();
       outportb(F81866 INDEX PORT, REG);
       outportb(F81866_DATA_PORT, DATA);
       Lock F81866();
}
11.
unsigned char Get F81866 Reg(unsigned char REG)
{
       unsigned char Result;
       Unlock_F81866();
       outportb(F81866_INDEX_PORT, REG);
       Result = inportb(F81866_DATA_PORT);
       Lock_F81866();
       return Result:
}
//--
          _____
//-
      \parallel
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
11-
#ifndef __F81866_H
#define _____ F81866___H
                                              1
//-----
#define F81866 INDEX PORT
                                      (F81866 BASE)
#define F81866 DATA PORT
                                      (F81866 BASE+1)
//-----
#define F81866_REG_LD
                                      0x07
//-----
```

0x87 0xAA

//----unsigned int Init\_F81866(void); void Set\_F81866\_LD( unsigned char); void Set\_F81866\_Reg( unsigned char, unsigned char); unsigned char Get\_F81866\_Reg( unsigned char); //-----

#endif //\_\_F81866\_H

# Chapter 15 Digital I/O Sample Configuration

#### Filename : Main.cpp

// // THIS COF	F AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EIT // IMPLIED \ // PURPOSE //	HER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE VARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR E.
// #include <do< td=""><td> bs.h&gt;</td></do<>	 bs.h>
#include <co< td=""><td>nio.h&gt; dio.h&gt;</td></co<>	nio.h> dio.h>
#include <st< td=""><td>dlib.h&gt;</td></st<>	dlib.h>
#Include Fo	П000.П
#define BIT	) 0x01   0x02
#define BIT2 #define BIT3	2 0x04 3 0x08
#define BIT4	↓0x10 5 0x20
#define BIT6	5 0x40 7 0x90
#ueiiiie bii /	0,00
int main (voi	d);
void Dio5Init	ial(void);
void Dio5Se unsigned ch	tOutput(unsigned char); ar Dio5GetInput(void):
void Dio5Se	tDirection(unsigned char); ar DioSCetDirection(void);
//	
{	abar SIO
	unsigned char DIO;
	printf("Fintek 81865/81866 digital I/O test program\n");
	SIO = Init_F81865(); if (SIO == 0)
	{ printf("Can not detect Fintek 81865/81866, program abort.\n");
	return(1); }//if (SIO == 0)
	Dio5Initial();
/*	//for GPI05057
	Dio5SetDirection(0xF0); //GP5053 = input, GP5457=output printf("Current DIO direction = 0x%X\n", Dio5GetDirection());
	printf("Current DIO status = 0x%X\n", Dio5GetInput());
	printf("Set DIO output to high\n");
	Dio5SetOutput(0x0F);
	printf("Set DIO output to low\n"); Dio5SetQutput(0x00);
*/	
	//for GPI05057 Dio5SetDirection(0xF0); //GP5053 = input, GP5457=output
//	Dio5SetOutput(0x00); //clear DIO = Dio5GetInput() & 0x0F;

Dio5SetOutput(0x00); //clear DIO = Dio5GetInput() & 0x0F;if (DIO != 0x0A) { printf("The Fintek 81865 digital IO abnormal, abort.\n"); return(1); }//if (DIO != 0x0A) Dio5SetOutput(0xA0); Dio5SetOutput(0xF0); Dio5SetOutput(0xA0); //clr# is high //clk and clr# is high //clr# is high DIO = Dio5GetInput() & 0x0F; if (DIO != 0x05) { printf("The Fintek 81865 digital IO abnormal, abort.\n"); return(1); } printf("!!! Pass !!!\n"); return 0; 11void Dio5Initial(void) { unsigned char ucBuf; //switch GPIO multi-function pin for gpio 50~57 //gpio53~57 UR5\_FULL\_EN(bit1), clear UR6\_FULL\_EN(bit3) //set UR5\_FULL\_EN,should set UR\_GP\_PROG\_EN = 1 (reg26,bit0) first ucBuf = Get\_F81865\_Reg(0x26); ucBuf |= BIT0; Set\_F81865\_Reg(0x26, ucBuf); //set UR5\_FULL\_EN(bit1), clear UR6\_FULL\_EN(bit3) ucBuf = Get\_F81865\_Reg(0x2A); ucBuf &= ~BIT3;//clear bit 3, ucBuf |= BIT1;//set bit 1, Set\_F81865\_Reg(0x2a, ucBuf); //GPIO51 ~ GPIO52 //clear UR6\_ALT\_EN(bit5), IR\_ALT\_EN(bit4),set FDC\_GP\_EN(bit3) //GPI050 //set FDC\_GP\_EN(bit3), clear RTS6\_ALT\_EN(RTS6\_2\_ALT\_EN)(bit6) ucBuf = Get\_F81865\_Reg(0x2A); ucBuf &= -(BIT4+BIT5+BIT6); //clear UR6\_ALT\_EN(bit5), IR\_ALT Set\_F81865\_Reg(0x2a, ucBuf); //set FDC\_GP\_EN(bit3), should clear UR\_GP\_PROG\_EN (reg26,bit0) first ucBuf = Get\_F81865\_Reg(0x26); ucBuf = JTC0. //clear UR6\_ALT\_EN(bit5), IR\_ALT\_EN(bit4), RTS6\_ALT\_EN(RTS6\_2\_ALT\_EN)(bit6) ucBuf &= ~BIT0; Set F81865 Reg(0x26, ucBuf);//clear UR GP PROG EN = 0 (reg26,bit0) Set\_F81865\_LD(0x06); //switch to logic device 6 //enable the GP5 group ucBuf = Get\_F81865\_Reg(0x30); ucBuf |= 0x01; Set\_F81865\_Reg(0x30, ucBuf);

Set\_F81865\_Reg(0xA0, 0x00); Set\_F81865\_Reg(0xA3, 0xFF);

} // //define as input mode //push pull mode

void Dio5SetOutput(unsigned char NewData) { Set\_F81865\_LD(0x06); Set\_F81865\_Reg(0xA1, NewData); //switch to logic device 6 } 11. unsigned char Dio5GetInput(void) { unsigned char result; Set\_F81865\_LD(0x06); //switch to logic device 6 result = Get\_F81865\_Reg(0xA2); return (result); 'n void Dio5SetDirection(unsigned char NewData) { //NewData : 1 for input, 0 for output Set\_F81865\_LD(0x06); Set\_F81865\_Reg(0xA0, NewData); //switch to logic device 6 } //· unsigned char Dio5GetDirection(void) { unsigned char result: Set\_F81865\_LD(0x06); result = Get\_F81865\_Reg(0xA0); return (result); //switch to logic device 6 11 Filename : 81865.cpp 11-// // THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY // KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE // IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR // PURPOSE  $\parallel$ 11 #include "F81865.H" #include <dos.h> 11unsigned int F81865\_BASE; void Unlock\_F81865 (void); void Lock\_F81865 (void); unsigned int Init\_F81865(void) { unsigned int result; unsigned char ucDid; F81865\_BASE = 0x4E; result = F81865\_BASE; //Fintek 81865/66 } F81865\_BASE = 0x2E; result = F81865\_BASE; //Fintek 81865/66 } F81865\_BASE = 0x00; result = F81865\_BASE;

Init\_Finish:

3 11-

{

}

{

} //

{

return (result);

void Unlock F81865 (void)

outportb(F81865\_INDEX\_PORT, F81865\_UNLOCK); outportb(F81865\_INDEX\_PORT, F81865\_UNLOCK);

11. void Lock\_F81865 (void)

outportb(F81865\_INDEX\_PORT, F81865\_LOCK);

void Set\_F81865\_LD( unsigned char LD)

Unlock\_F81865(); outportb(F81865\_INDEX\_PORT, F81865\_REG\_LD); outportb(F81865\_DATA\_PORT, LD); Lock\_F81865();

} 11. void Set\_F81865\_Reg( unsigned char REG, unsigned char DATA) { Unlock\_F81865(); outportb(F81865\_INDEX\_PORT, REG); outportb(F81865\_DATA\_PORT, DATA); Lock\_F81865();

11unsigned char Get\_F81865\_Reg(unsigned char REG) { unsigned char Result; Unlock\_F81865();

#### Filename : 81865.h

} //--

//			
// // THIS CODE AN // KIND, EITHER E // IMPLIED WARF // PURPOSE. //	D INFORMATION IS PROVIDI EXPRESSED OR IMPLIED, IN ANTIES OF MERCHANTABIL	ED "AS IS" WITHOUT WARF CLUDING BUT NOT LIMITEI ITY AND/OR FITNESS FOR	RANTY OF ANY D TO THE A PARTICULAR
#ifndefF81865_ #defineF81865	<u>н</u> _н	1	
#define F818 #define F818	865_INDEX_PORT 865_DATA_PORT	(F81865_BASE) (F81865_BASE+1)	
#define F818	65_REG_LD	0x07	
#define F81865_L #define F818	NLOCK 365_LOCK	0x87	0xAA
unsigned int Init_F void Set_F81865_ void Set_F81865_ unsigned char Ge	81865(void); LD( unsigned char); Reg( unsigned char, unsigned i_F81865_Reg( unsigned char)	char); );	

//-----#endif //\_\_F81865\_H

## Chapter 16 Drivers Installation

This section describes the installation procedures for software and drivers under the Windows. The software and drivers are included with the board. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

Intel® Chipset Software Installation Utility Intel® Graphics Driver Installation LAN Drivers Installation Intel® Management Engine Interface

#### **IMPORTANT NOTE:**

After installing your Windows operating system, you must install first the Intel® Chipset Software Installation Utility before proceeding with the drivers installation.

## Intel® Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the CD that comes with the board. Click Intel and then Intel(R) 7 Series Chipset Drivers.



2. Click Intel(R) Chipset Software Installation Utility.



3. When the Welcome screen to the Intel® Chipset Device Software appears, click Next to continue.



4. Click Yes to accept the software license agreement and proceed with the installation process.



5. On the Readme File Information screen, click *Next* to continue the installation.



6. The Setup process is now complete. Click Finish to restart the computer and for changes to take effect.



## **VGA Drivers Installation**

NOTE: Before installing the *Intel(R) C216 Chipset Family Graphics Driver*, the Microsoft .NET Framework 3.5 SPI should be first installed.

To install the VGA drivers, follow the steps below.

1. Insert the CD that comes with the board. Click *Intel* and then *Intel(R)* Q7 Series Chipset Drivers.



2. Click Intel(R) C216 Chipset Family Graphics Driver.



#### 3. When the Welcome screen appears, click *Next* to continue.



4. Click **Yes** to to agree with the license agreement and continue the installation.



5. On the Readme File Information screen, click *Next* to continue the installation of the Intel® Graphics Media Accelerator Driver.



6. On Setup Progress screen, click Next to continue.



7. Setup complete. Click *Finish* to restart the computer and for changes to take effect.

## **LAN Drivers Installation**

1. Insert the CD that comes with the board. Click *Intel* and then *Intel(R)* Q7 Series Chipset Drivers.



2. Click Intel(R) PRO LAN Network Driver.



#### 3. Click Install Drivers and Software.



#### 4. When the Welcome screen appears, click Next.

HITEL Intel(R) Network Connections - InstallShield Wizard	×
Welcome to the InstallShield Wizard for Intel(R) Network Connections	(intel)
Installs drivers, Intel(R) PROSet for Windows* Device Manager, and Advanced Networking Services.	
WARNING: This program is protected by copyright law and international treaties.	
InstallShield	Cancel

### 5. Click *Next* to to agree with the license agreement.

🔡 Intel(R) Network Connections - InstallShield Wizard	x		
License Agreement Please read the following license agreement carefully.	D		
INTEL SOFTWARE LICENSE AGREEMENT			
IMPORTANT - READ BEFORE COPYING, INSTALLING OR USING.			
Do not copy, install, or use this software and any associated materials (collectively, the "Software") provided under this license agreement ("Agreement") until you have carefully read the following terms and conditions. By copying, installing, or otherwise using the Software, you agree to be bound by			
the terms of this Agreement. If you do not agree to the terms of this Agreement, do not copy, install, or use the Software.	÷		
I go not accept the terms in the license agreement     Print     I go not accept the terms in the license agreement			
InstallShield			
< <u>B</u> ack <u>N</u> ext > Cancel			

6. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.

Intel(R) Network Connections	<b>X</b>
Setup Options Select the program features you want installed.	(intel)
Install:	
Orivers     O	
Feature Description	
< <u>Back</u> Mext >	Cancel

7. The wizard is ready to begin installation. Click *Install* to begin the installation.

Intel(R) Network Connections - InstallShield Wizard	×
Ready to Install the Program The wizard is ready to begin installation.	(intel)
Click Install to begin the installation.	
If you want to review or change any of your installation settings, click Back. Cli exit the wizard.	ck Cancel to
InstallShield	Cancel

8. When InstallShield Wizard is complete, click Finish.

HINTER Intel(R) Network Connections - InstallShield Wizard	×
InstallShield Wizard Completed	(intel)
To access new features, open Device Manager, and view the properties of the network adapters.	
InstallShield	Cancel

## **Intel® Management Engine Interface**



The following application requires Microsoft .NET Framework 3.5 or later: Intel® Management Engine Components. Please install the latest version of Microsoft .NET Framework from Microsoft Download Center to run this application correctly.

Follow the steps below to install the Intel Management Engine.

1. Insert the CD that comes with the board. Click Intel and then Intel(R) AMT 8.0 Drivers.



2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click the checkbox for Install Intel® Control Center & click Next.

Intel® Installation Framework	
Intel® Management Engine Components Welcome to the Setup Program	(intel)
This setup program will install the Intel® Management Engine Components.	
It is strongly recommended that you exit all programs before continuing. Click ${\ensuremath{\mathbb N}}$	Vext to continue.
✓ Install Intel® Control Center Intel® Control Center provides a centralized starting point for Intel applicat easier to find the programs that you need.	tions making it
<back next=""></back>	<b>Cancel</b> Installation Framework

3. Click **Yes** to to agree with the license agreement.



4. When the Setup Progress screen appears, click *Next*. Then, click *Finish* when the setup progress has been successfully installed.

Intel® Installation Framework	
Intel® Management Engine Components Setup Progress	(intel)
Please wait while the following setup operations are performed:	
Creating Process: regsvr32.exe Copying File: C:\Windows\system32\drivers\IntelMEFWVer.dll Creating Process: C:\Program Files (x86)\Intel\Intel(R) Managemen Installing: Intel® Control Center Deleting File: C:\Program Files (x86)\Intel\Intel(R) Management En Copying File: C:\Program Files (x86)\Intel\Intel(R) Management En Creating Process: C:\Program Files (x86)\Intel\Intel(R) Management En Creating Process: C:\Program Files (x86)\Intel\Intel(R) Management Installing: Intel® ME FW Recovery Agent Copying File: C:\Program Files (x86)\Intel\Intel(R) Management Eng	t Engine Components\FWS gine Components\FWServic gine Components\FWServic t Engine Components\FWS t Engine Components\FWS gine Components\Firmware
Click Next to continue.	-
<	4
	Next >
	– Intel® Installation Framework
Intel® Installation Framework	
Intel® Management Engine Components Setup Is Complete	(intel)
The setup program successfully installed the following components: - Intel® Management Engine Interface - Intel® Dynamic Application Loader - Intel® Identity Protection Technology (Intel® IPT) - Serial Over LAN - Intel® Management and Security Status - Local Management Service - User Notification Service Click Finish to complete the setup process.	Finish
The setup program successfully installed the following components: - Intel® Management Engine Interface - Intel® Dynamic Application Loader - Intel® Identity Protection Technology (Intel® IPT) - Serial Over LAN - Intel® Management and Security Status - Local Management Service - User Notification Service Click Finish to complete the setup process.	- Intel® Installation Framework

Intel® USB 3.0 Drivers

1. Insert the CD that comes with the board. Click Intel and then Intel(R) C216 Series Chipset Drivers.



2. Click Intel(R) USB 3.0 Drivers.



3. When the Welcome screen to the InstallShield Wizard for Intel® USB 3.0 eXtensible Host Controller Driver, click *Next*.



4. Click **Yes** to to agree with the license agreement and continue the installation.



5. On the Readme File Information screen, click *Next* to continue the installation of the Intel® USB 3.0 eXtensible Host Controller Driver.

Intel® Installation Framework	X
Intel® USB 3.0 eXtensible Host Controller Driver	
Readme File Information	(intel)
Refer to the Readme file below to view the system requirements and installatio	n information.
***** WARNING ***** Do not run this driver's installer (Setup.exe) from a USB storage device (e. external USB hard drive or USB thumb drive). For proper installation, please copy driver files to a local hard drive folder and run from there.	
* Production Version Releases *	
* Microsoft Windows* 7 *	-
< Back Next >	Cancel
Intel® Ir	nstallation Framework

6. Setup complete. Click *Finish* to restart the computer and for changes to take effect.



# Appendix-A I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
2F8h - 2FFh	Serial Port #2(COM2)
2B0h- 2DFh	Graphics adapter Controller
360h - 36Fh	Network Ports
3F8h - 3FFh	Serial Port #1(COM1)

Appendix-B Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ8	Real Time Clock
IRQ14	Primary IDE
IRQ15	Secondary IDE

## Appendix-C FWA8308 Series Configurations

#### The following lists the available SKUs of FWA8308 for different system requirement.

# **FWA8308** 2.5" HDD x1, PCI-e add-on card rear expansion x1, front panel expansion card x1, 300W PSU

- > MB968 x1
- IP331 x1: 1-to-1 Riser Card
- > IP332 x1: PCI-e Adapter
- Single 2.5" HDD Bracket x1
- 4-pin Smart Fan x3
- > 300W Single Power Supply

#### FWA8308 Optional Items

- > IBP161, IBP162...: Expansion LAN Card
- > Dual 2.5" HDD Bracket Kit SC2FWA8308-0A1100P
- > VGA cable: C501VGA0415272000P
- > Console Cable: C501PK15108A12000P
- > Rear Rackmount Kit: 600 or 800mm



# **FWA8308-2SLOT** 3.5" HDD x1, PCI-e add-on card rear expansion x2, 300W PSU

- > MB968 x1
- > IP333 x1: 2-to-2 Riser Card
- Single 3.5" HDD Bracket x1
- 4-pin Smart Fan x3
- > 300W Single Power Supply

#### FWA8308-2SLOT Optional Items

- > Dual 2.5" HDD Bracket Kit SC2FWA8308-0A1100P
- > VGA cable: C501VGA0415272000P
- Console Cable: C501PK15108A12000P
- Rear Rackmount Kit: 600 or 800mm



# **FWA8308-RPSU** 2.5" HDD x1, PCI-e add-on card rear expansion x1, front panel expansion card x1, 275W 1+1 Redundant PSU

- > MB968 x1
- > IP331 x1: 1-to-1 Riser Card
- > IP332 x1: PCI-e Adapter
- Single 2.5" HDD Bracket x1
- 4-pin Smart Fan x3
- > 275W 1+1 Redundant Power Supply

#### FWA8308-RPSU Optional Items

- > IBP161, IBP162...: Expansion LAN Card
- > VGA cable: C501VGA0415272000P
- Console Cable: C501PK15108A12000P
- > Rear Rackmount Kit: 600 or 800mm

