# **MB968**

8-port (Haswell + C226) Networking Motherboard

# **USER'S MANUAL**

Version 1.2

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## Introduction

#### **Product Description**

The MB968 networking motherboard is based on the latest Intel<sup>®</sup> C226 chipset. The platform supports LGA1150 Haswell processors. Four DDR3 UDIMM sockets allows up to 32GB system memory.

The motherboard supports a total of eight Ethernet ports with the port 5 to port8 supporting Bypass function. It also has two fast SATA III 6Gbps ports, two USB 3.0 ports, two USB 2.0 ports and one USB 2.0 for Mini PCI-e. MB968 utilizes the dramatic increase in performance provided this Intel's latest cutting-edge technology. Measuring 355mm x 185mm, MB968 features Intel<sup>®</sup> Active Management Technology 8.0, offers eight GbE LAN ports, two fast 6Gbps SATA ports and two USB3.0 ports.

#### MB968 Features

- Supports Intel® Shark Bay DT LGA1150 Haswell processors
- Supports Intel® Lynx Point C226 PCH chipset
- Four DDR3 UDIMM for maximum 32GB total, 1600MHz, Unbuffered
- Intel CPU integrated graphics
- Intel® Clarkville I217LM GbE PHY for Eth1, No Bypass Eth2~4: Intel® Springville I210-AT, No Bypass Eth5~6: Intel® Springville I210-AT, supports Bypass Eth7~8: Intel® Springville I210-AT, supports Bypass
- Two SATA III (6.0Gb/s)
- One cableless 2.5" HDD (use IP332)
- Optional 3.5" HDD x1, 2.5" HDD x2

## Specifications

Product Name	MB968
Processor	<ul> <li>Support for Intel® Shark Bay DT LGA1150 Haswell processors</li> <li>TDP = 35W ~ 95W (DC / QC)</li> </ul>
CPU Speed	TBD
Cache Size	Up to 8MB
Chipset	Intel <sup>®</sup> Lynx Point C226 PCH Package =23 mm x 22 mm , 0.65 mm ball pitch
BIOS	AMI BIOS
Memory	<ul> <li>Four DDR3 UDIMM total for 32GB max memory (4Gb chip support)</li> <li>Support DDR3 at 1.5V</li> <li>Dual channel DDR3 up to 1600 MHz</li> <li>Unbuffered</li> <li>ECC or non-ECC</li> </ul>
Video	Intel <sup>®</sup> CPU integrated graphics     IBASE VGA4 pin header on board
Network Controller	<ul> <li>Eth1: Intel® Clarkville I217LM GbE PHY, 6mm x 6mm, QFN48 with iAMT 9.0 supporting. No Bypass</li> <li>Eth2~4: Intel® Springville I210-AT. No Bypass.</li> <li>Eth5~6: Intel® Springville I210-AT Support Bypass.</li> <li>Eth7~8: Intel® Springville I210-AT Support Bypass.</li> </ul>
SATA Ports	<ul> <li>Two SATA III (6.0Gb/s), 7-pin SATA Blue connector</li> <li>One for Front PCI-e Golden Finger #1 (to IP332)</li> <li>Two for mSATA (Mini PCI-e)</li> <li>One for CF Card</li> </ul>
Fan Connector	<ul> <li>4-pin smart fan connectors:</li> <li>Three for CPU Fan (Smart Fan reference to CPU temperature in BIOS)</li> <li>One for System Fans (Smart Fan reference to CPU temperature in BIOS))</li> </ul>
Compact Flash	Marvell 88SA8052 SATA to PATA for Compact Flash type II
Digital IO	4 in & 4 out, 2x5 pin-header
Front Panel LED	#1 LED: Power (Green = Power On, Off= No Power) #2 LED: Bypass or HDD (Jumper Select) Bypass: Green = LAN 5-6 or 7-8 Bypass, Off = LAN Normal #3 LED: Status (GPIO control, Yellow / Red)

USB Ports	<ul> <li>Two USB 3.0 + 2.0 ports at front panel</li> <li>One USB 2.0 for Mini PCI-e</li> <li>Six USB 2.0 pin headers (pitch 2.54)</li> </ul>				
Network Bypass	<ul> <li>Two segment hardware Bypass (Eth5 &amp; 6; Eth7 &amp; 8)</li> <li>Bypass mode selection in BIOS</li> </ul>				
LPC I/O	Fintek F81866AD-I (128-pin LQFP [14mm x 14 mm]) • COM1: RJ-45 Console x1 • COM2~4: RS-232 [2x5] Pin Header Onboard x3 • Hardware monitors • Fan Connector x4 • Digital IO 4in & 4 Out				
Smart Fan Control	The active temperature may be adjusted based on system thermal test result. All reference to CPU temperature.       Active     Tolerance     Default Smart Fan Enable or Disable       CPU Fan     50     +/- 5     Enable				
RTC	Intel C226 built-in RTC with on-board lithium battery & holder				
Expansion Slot (CPU PEG port)	CPU jumper sett fingers & riser ca Configuration 1 2	ing PEG port to fu ards Golden Finger Compatible Ris IP332 IP333	ollowing co #1 ser Cards	nfigi Go Co	urations for golden olden Finger #2 ompatible Riser Cards IP331 IP333
Expansion Interface	<ul> <li>Mini PCI-e Socket x1 (m-SATA compatible)</li> <li>Mini PCI-e Socket x1 (support m-SATA only)</li> </ul>				
Front Panel Buttons & Connector	<ul> <li>Two RJ-45 1x4 connectors for Eth1~4 &amp; 5~6</li> <li>USB 3.0 x2</li> <li>RJ-45 (for console, COM1)</li> <li>Three LEDs for Power, Bypass or HDD &amp; Status</li> <li>Factory Mode Restore Reset Switch</li> </ul>				
Rear I/O interface	PSU AC inlet     1x or 2x Slot (Depend on product SKU)				
Jumper / Pin Header / Switch	<ul> <li>AT or ATX mode selection jumper</li> <li>ATX mode power on / off pin header</li> <li>Power on LED pin header</li> <li>HDD active LED pin header</li> <li>System Reset pin header</li> <li>Clear CMOS</li> <li>Clear ME RTC</li> <li>Golden finger (1x16 or 2x8) switch jumper</li> </ul>				

Watchdog Timer	Yes (256 segments, 0, 1, 2255 sec/min)	
ТРМ	Nuvoton WPCT210AA0WX	
Operating Temperature	0°C ~ 45°C	
Storage Temperature	-20°C ~ 70°C	
Operational Humidity	5% ~ 95% Relative Humidity (non-condensing)	
RoHS Compliant	Yes	
Board Size	355 x 185mm, FR-4, 1.6mm thickness	
Compatible Cards	<ul> <li>IBP161: 4-port Realtek GbE LAN Card</li> <li>IBP162: 2-port Intel 10GbE Fiber LAN Card</li> <li>IBP163: 2+2 ports Intel 1350-AM2 Fiber + Copper LAN Card</li> <li>IBP164: Crypto acceleration Card</li> <li>IBP165: 4-port Intel® I210-AT GbE LAN Card</li> <li>IBP167: 8-port Intel® I350-AM4 GbE LAN Card</li> <li>IP331: PCI-e 1-to-1 Riser Card</li> <li>IP332: PCI-e Adapter Card (with 2.5" HDD Interface)</li> <li>IP333: PCI-e 2-to-2 Riser Card</li> </ul>	

### Checklist

Your MB968 package should include the items listed below.

- MB968 motherboard
- Driver DVD

### **Board Dimensions**



## **Block Diagram**



## Installations

This section provides information on how to use the jumpers and connectors on the MB968 in order to set up a workable system. The topics covered are:

Installing the CPU	
Installing the Memory	
Setting the Jumpers	
Jumper Locations on MB968	
Connectors on MB968	

### Installing the CPU

The MB968 board supports an LGA1150 Socket (shown below) for Intel Clarkdale processors.

To install the CPU, unlock first the socket by pressing the lever sideways, then lift it up to a 90-degree. Then, position the CPU above the socket such that the CPU corner aligns with the gold triangle matching the socket corner with a small triangle. Carefully insert the CPU into the socket and push down the lever to secure the CPU. Then, install the heat sink and fan.



**NOTE**: Ensure that the CPU heat sink and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.

### **Installing the Memory**

The MB968 board supports four DDR3 memory socket for a maximum total memory of 32GB in DDR3 DIMM memory type.

#### **Installing and Removing Memory Modules**

To install the DDR3 modules, locate the memory slot on the board and perform the following steps:

- 1. Hold the DDR3 module so that the key of the DDR3 module aligned with that on the memory slot.
- 2. Gently push the DDR3 module in an upright position until the clips of the slot close to hold the DDR3 module in place when the DDR3 module touches the bottom of the slot.
- 3. To remove the DDR3 module, press the clips with both hands.



### **Setting the Jumpers**

Jumpers are used on MB968 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on MB968 and their respective functions.

Jumper Locations on MB968	
Jumper Settings on MB968	
JP2: Clear CMOS Setting	
JP3: Clear ME Setting	
JP9: AT/ATX Mode Setting	
JP12: Flash Security Override Setting	
J17, J18: PCIE Config Setting	
, 6 6	

#### **Jumper Locations on MB968**





#### **Jumper Settings on MB968**

#### JP2: Clear CMOS Setting

JP2	Setting
<u> </u>	Normal
123	Clear CMOS

#### JP3: Clear ME Setting

JP3	Setting
<u>n n n</u>	Normal
123	Clear ME

#### JP9: AT / ATX Mode Setting

JP9	Setting
12	ATX
<b>D</b> 12	AT

#### JP12: BIOS Flash Security Setting

JP12	Setting
123	Normal
2 Z I	For BIOS Update

#### JP15: LED Function Selection

JP15	Setting
123	HDD Activate
123	Bypass Activate

J17, J18: PCIE Config Setting

J18	J17	Setting		
12	10	2 x 8 for Golden Finger PCIE1 & PCIE2		
00 12	00 12	1x16 for Golden Finger PCIE2		

## **Connectors on MB968**

J2: System Function Connector	19
J5: VGA Connectors	
J6, J7, J8: USB6~USB11 Ports	
J9: Compact Flash Socket	
J10: Mini PCI- E(x1) / mSATA Socket	
J11: SPI Debug Port	
J12: Digital IO 4IN/4OUT Connector	
J13: LPC Debug Port	
J19, J25: ATX Power Connector	
J21, J22, J23: External CF Power Connector	
J24: External CF Power Connector	
J27: mSATA Socket	
CN1, CN3: Serial ATA Port	
CPU_FAN1: CPU Fan Power Connector	
FAN1, FAN2, FAN3: System Fan Power Connector	
LED4: Status LED	
SW1: Software reset button	

#### J2: System Function Connector

J2 provides connectors for system indicators that provide light indication of the computer activities and switches to change the computer status. J2 is a 20-pin header that provides interfaces for the following functions



#### Pin 2, 4, 6, 8: Speaker

This connector provides an interface to a speaker for audio tone generation. An 8-ohm speaker is recommended.

Pin #	Signal Name	
2	SPEAKER	
4	NC	
6	GND	
8	+5V	

#### Pin 1, 3, 5: Power LED

The power LED indicates the status of the main power switch.

Pin #	Signal Name	
1	+5V	
3	NC	
5	GND	

#### Pin 13, 14: ATX Power ON Switch

This 2-pin connector is an "ATX Power Supply On/Off Switch" on the system that connects to the power switch on the case. When pressed, the power switch will force the system to power on. When pressed again, it will force the system to power off.

Pin #	Signal Name		
13	GND		
14	Power_ON		

#### Pin 17, 18: Reset Switch

The reset switch allows the user to reset the system without turning the main power switch off and then on again. Orientation is not required when making a connection to this header.

Pin #	Signal Name
17	GND
18	PM_SYSRST#

#### Pins 19, 20: HDD LED

This connector connects to the hard drive activity LED on control panel. This LED will flash when the HDD is being accessed.

Pin #	Signal Name
19	+3.3V
20	-HDD_LED

#### J5: VGA Connectors

5

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Signal Name	Pin #	Pin #	Signal Name
VGA_R	1	2	VGA_PWR
VGA_G	3	4	GND
VGA_B	5	6	NC
NC	7	8	VGADDCDATA
GND	9	10	HSYNC
GND	11	12	VSYNC
GND	13	14	VGADDCCLK
GND	15		

#### J6, J7, J8: USB6~USB11 Ports

	Signal Name	Pin #	Pin #	Signal Name
8 0 0	+5V	1	2	GND
0 0	D-	3	4	D+
1	D+	5	6	D-
	GND	7	8	+5V

#### **J9: Compact Flash Socket**



Note: CF card supports IDE mode only. If CF card applied, please set the SATA configuration to "IDE mode" in BIOS.

#### J10: Mini PCI- E / mSATA Socket

#### J11: SPI Debug Port

	Signal Name	Pin #	Pin #	Signal Name
			2	NC
90003	SPI_CS#0	3	4	+3.3V
10 0 0 0 0 0 2	SPI_SO	5	6	SPI0_HOLD#
	SPI0_WP#	7	8	SPI_CLK
	GND	9	10	SPI_SI

#### J12: Digital IO 4-IN / 4-OUT Connector

Signal Name	Pin #	Pin #	Signal Name
GND	1	2	+5V
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

#### J13: LPC Debug Port

8000

Signal	Pin #	Pin #	Signal
Name			Name
LPC_AD0	1	2	SIO_PLTRST#
LPC_AD1	3	4	LPC_FRAME#
LPC_AD2	5	6	+3.3V
LPC_AD3	7	8	Ground
LPC_CLK	9		

#### J15, J16, J20: Serial Port (COM1~COM3)

	Signal	Pin #	Pin #	Signal
	Name			Name
6 0 1	DCD#	1	6	DSR#
	SIN	2	7	RTS#
0 0 0	SOUT	3	8	CTS#
	DTR#	4	9	RI#
	GND	5		

#### J19, J25: ATX Power Connector

J21,	J22,	J23:	Power	Connector,	Pitch	2.54mm
------	------	------	-------	------------	-------	--------

	Pin #	Signal Name
žn_	1	+5V
0	2	Ground
•	3	Ground
4	4	+12V

#### J24: Power Connector, Pitch 2.0mm

	-	
0	1	
õ		
© ⊓	4	

Pin #	Signal Name
1	+5V
2	Ground
3	Ground
4	+12V

#### J27: mSATA Socket

#### **CN1, CN3: HDD Serial ATA Connector**

#### CPU FAN1: CPU Fan Connector

CPU\_FAN1 is a 4-pin header for the CPU fan. The fan must be 12V (Max. 1A).

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-			4

Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Rotation control

#### FAN1, FAN2, FAN3: System Fan Connectors

FAN1, FAN2, FAN3 is a 4-pin header for system fans. The fan must be 12V (Max. 1A).

	۲	۲
-		

Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Rotation control

#### LED4: Status LED

A1 & C1 : Status LED A2 & C2 : Bypass or HDD status LED A3 & C3 : Power LED

Status	Signal Name	Pin #	Pin #	Signal Name
	SIO_GPIO33	A1	C1	SIO_GPIO32
Eg Dowor	+5 V	A2	C2	JP15 Selection
Power	+3.3 V	A3	C3	GND

#### SW1: Software reset button

I/O base :

Read IO 0x1C00 and set bit 7 to "1" (Enable GPIO function) Read IO 0x1C04 and set bit 7 to "1" (GPIO act as GPI) Read IO 0x1C0C and set check bit 7 (Control Pin)

	Signal Name	Pin #	Pin #	Signal Name
	CND	1	2	PCH
1 2	GND	1	Z	GPIO7

## **Digital I/O Sample Configuration**

#### Filename : Main.cpp

```
11
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
11
//--
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81865.H"
#define BIT0 0x01
#define BIT1 0x02
#define BIT2 0x04
#define BIT3 0x08
#define BIT4 0x10
#define BIT5 0x20
#define BIT6 0x40
#define BIT7 0x80
//-----
int main (void);
void Dio5Initial(void);
void Dio5SetOutput(unsigned char);
unsigned char Dio5GetInput(void);
void Dio5SetDirection(unsigned char);
unsigned char Dio5GetDirection(void);
int main (void)
{
      char SIO;
      unsigned char DIO;
      printf("Fintek 81865/81866 digital I/O test program\n");
      SIO = Init F81865();
      if (SIO == 0)
             printf("Can not detect Fintek 81865/81866, program abort.\n");
             return(1);
       }//if (SIO == 0)
      Dio5Initial();
/*
      //for GPIO50..57
      Dio5SetDirection(0xF0);
                                 //GP50..53 = input, GP54..57=output
      printf("Current DIO direction = 0x\%X\n", Dio5GetDirection());
      printf("Current DIO status = 0x%X\n", Dio5GetInput());
      printf("Set DIO output to high\n");
       Dio5SetOutput(0x0F);
      printf("Set DIO output to low\n");
      Dio5SetOutput(0x00);
*/
      //for GPIO50 57
      Dio5SetDirection(0xF0);
                                //GP50..53 = input, GP54..57=output
      Dio5SetOutput(0x00);
                                               //clear
      DIO = Dio5GetInput() & 0x0F;
```

```
Dio5SetOutput(0x00);
                                               //clear
      DIO = Dio5GetInput() & 0x0F;
       if (DIO != 0x0A)
             printf("The Fintek 81865 digital IO abnormal, abort.\n");
             return(1);
       \frac{1}{100} = 0x0A
       Dio5SetOutput(0xA0);
                                               //clr# is high
                                               //clk and clr# is high
      Dio5SetOutput(0xF0);
       Dio5SetOutput(0xA0);
                                               //clr# is high
      DIO = Dio5GetInput() & 0x0F;
      if (DIO != 0x05)
              printf("The Fintek 81865 digital IO abnormal, abort.\n");
             return(1);
      printf("!!! Pass !!!\n");
      return 0;
void Dio5Initial(void)
{
      unsigned char ucBuf:
      //switch GPIO multi-function pin for gpio 50~57
//gpio53~57 UR5_FULL_EN(bit1), clear UR6_FULL_EN(bit3)
      //set UR5 FULL EN, should set UR GP PROG EN = 1 (reg26, bit0) first
      ucBuf = Get_F81865_Reg(0x26);
      ucBuf \models BITO;
      Set_F81865_Reg(0x26, ucBuf);
      //set UR5_FULL_EN(bit1), clear UR6_FULL_EN(bit3)
      ucBuf = Get_F81865_Reg(0x2A);
      ucBuf &= ~BIT3;//clear bit 3,
      ucBuf |= BIT1://set bit 1.
      Set_F81865_Reg(0x2a, ucBuf);
//GPIO51 ~ GPIO52
      //clear UR6_ALT_EN(bit5), IR_ALT_EN(bit4),set FDC_GP_EN(bit3)
//GPI050
//set FDC GP EN(bit3), clear RTS6 ALT EN(RTS6 2 ALT EN)(bit6)
       ucBuf = Get_F81865_Reg(0x2A);
      ucBuf &= ~(BIT4+BIT5+BIT6);
                                        //clear UR6_ALT_EN(bit5), IR_ALT_EN(bit4),
RTS6_ALT_EN(RTS6_2_ALT_EN)(bit6)
      Set_F81865_Reg(0x2a, ucBuf);
      //set FDC_GP_EN(bit3), should clear UR_GP_PROG_EN (reg26,bit0) first
      ucBuf = Get_F81865_Reg(0x26);
      ucBuf &= ~BIT0;
      Set_F81865_Reg(0x26, ucBuf);//clear UR_GP_PROG_EN = 0 (reg26,bit0)
      ucBuf = Get_F81865_Reg(0x2A);
      ucBuf \models BIT3;
                          //set FDC_GP_EN(bit3),
      Set_F81865_Reg(0x2a, ucBuf);
      Set F81865 LD(0x06);
                                                                           //switch to logic device 6
      //enable the GP5 group
      ucBuf = Get_F81865_Reg(0x30);
      ucBuf \models 0x01;
      Set_F81865_Reg(0x30, ucBuf);
       Set_F81865_Reg(0xA0, 0x00);
                                                                           //define as input mode
      Set_F81865_Reg(0xA3, 0xFF);
                                                                           //push pull mode
```

```
void Dio5SetOutput(unsigned char NewData)
                                                                             //switch to logic device 6
       Set_F81865_LD(0x06);
      Set_F81865_Reg(0xA1, NewData);
3
//-
unsigned char Dio5GetInput(void)
{
      unsigned char result;
      Set_F81865_LD(0x06);
                                                                            //switch to logic device 6
      result = Get_F81865_Reg(0xA2);
      return (result);
}
//----
void Dio5SetDirection(unsigned char NewData)
{
      //NewData: 1 for input, 0 for output
      Set_F81865_LD(0x06);
                                                                             //switch to logic device 6
      Set_F81865_Reg(0xA0, NewData);
}
//-
unsigned char Dio5GetDirection(void)
      unsigned char result;
      Set_F81865_LD(0x06);
                                                                            //switch to logic device 6
      result = Get_F81865_Reg(0xA0);
      return (result);
}
//---
```

#### Filename: 81865.cpp

// THIS CODE AND INFORMATION IS PROVIDED "AS IS" W // THIS CODE AND INFORMATION IS PROVIDED "AS IS" W // KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BL // IMPLIED WARRANTIES OF MERCHANTABILITY AND/O! // PURPOSE. // //	TTHOUT WARRANTY OF ANY JT NOT LIMITED TO THE R FITNESS FOR A PARTICULAR
//	
//	
ucDid = Get_F81865_Reg(0x20); if (ucDid == 0x07  ucDid == 0x10) { goto Init_Finish; }	//Fintek 81865/66
$F81865\_BASE = 0x2E;$ result = $F81865\_BASE;$	
$ucDid = Get_F81865_Reg(0x20);$ if (ucDid == 0x07  ucDid == 0x10) { goto Init_Finish; }	//Fintek 81865/66
F81865_BASE = 0x00; result = F81865_BASE;	

Init\_Finish:

```
return (result);
}
//-
void Unlock_F81865 (void)
      outportb(F81865_INDEX_PORT, F81865_UNLOCK);
      outportb(F81865_INDEX_PORT, F81865_UNLOCK);
}
//--
void Lock_F81865 (void)
{
      outportb(F81865_INDEX_PORT, F81865_LOCK);
//--
void Set_F81865_LD( unsigned char LD)
{
      Unlock F81865();
      outportb(F81865_INDEX_PORT, F81865_REG_LD);
      outportb(F81865_DATA_PORT, LD);
      Lock_F81865();
}
//-
void Set_F81865_Reg( unsigned char REG, unsigned char DATA)
      Unlock F81865();
      outportb(F81865_INDEX_PORT, REG);
      outportb(F81865_DATA_PORT, DATA);
      Lock_F81865();
}
//-
unsigned char Get_F81865_Reg(unsigned char REG)
{
      unsigned char Result;
      Unlock_F81865();
      outportb(F81865_INDEX_PORT, REG);
      Result = inportb(F81865_DATA_PORT);
      Lock_F81865();
      return Result:
```

#### Filename : 81865.h

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// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE // IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR // PURPOSE. // //
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR // PURPOSE. // //
// PURPOSE. // #ifndefF81865_H #defineF81865_H 1 // #define F81865_INDEX_PORT (F81865_BASE) #define F81865_DATA_PORT (F81865_BASE+1) // #define F81865_REG_LD 0x07 // #define F81865_UNLOCK 0x87 #define F81865_LOCK 0xAA //
// //
//
#IndetF81865_H       1         //
#define     F81865_INDEX_PORT     (F81865_BASE)       #define     F81865_DATA_PORT     (F81865_BASE+1)       //
/// #define         F81865_INDEX_PORT         (F81865_BASE)           #define         F81865_DATA_PORT         (F81865_BASE+1)           //
#define         F81865_DATA_PORT         (F81865_BASE+1)           //
//
#define         F81865_REG_LD         0x07           //
//
#define F81865_UNLOCK 0x87 #define F81865_LOCK 0xAA //
#define F81865_LOCK 0xAA
//
unsigned int Init_F81865(void);
void Set_F81865_LD( unsigned char);
void Set_F81865_Reg( unsigned char, unsigned char);
unsigned char Get_ro1005_keg( unsigned char);
#endif // F81865 H

## Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

#### SAMPLE CODE:

This code and information is provided "as is" without warranty of any kind, either expressed or implied, including but not limited to the implied warranties of merchantability and/or fitness for a particular purpose.

```
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND. EITHER EXPRESSED OR IMPLIED. INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//---
#include <dos.h>
#include <conio h>
#include <stdio.h>
#include <stdlib.h>
#include "F81866.H"
//----
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//___
int main (int argc, char *argv[])
{
      unsigned char bBuf;
      unsigned char bTime;
      char **endptr;
      char SIO:
      printf("Fintek 81866 watch dog program\n");
      SIO = Init F81866():
      if (SIO == 0)
       {
             printf("Can not detect Fintek 81866, program abort.\n");
             return(1):
       }//if (SIO == 0)
      if (argc != 2)
      {
             printf(" Parameter incorrect !!\n");
             return (1);
       3
      bTime = strtol (argv[1], endptr, 10);
      printf("System will reset after %d seconds\n", bTime);
      if (bTime)
             EnableWDT(bTime); }
      {
      else
             DisableWDT();
                               }
      {
```

```
return 0;
}
//-
void EnableWDT(int interval)
{
      unsigned char bBuf;
      bBuf = Get_F81866_Reg(0x2B);
      bBuf &= (~0x20);
      Set_F81866_Reg(0x2B, bBuf);
                                                                  //Enable WDTO
       Set_F81866_LD(0x07);
                                                                   //switch to logic device 7
      Set_F81866_Reg(0x30, 0x01);
                                                                  //enable timer
       bBuf = Get_F81866_Reg(0xF5);
      bBuf &= (\sim 0x0F);
      bBuf \models 0x52:
      Set_F81866_Reg(0xF5, bBuf);
                                                                   //count mode is second
      Set_F81866_Reg(0xF6, interval);
                                                            //set timer
      bBuf = Get_F81866_Reg(0xFA);
      bBuf \models 0x01;
      Set_F81866_Reg(0xFA, bBuf);
                                                                  //enable WDTO output
      bBuf = Get_F81866_Reg(0xF5);
      bBuf \models 0x20:
      Set_F81866_Reg(0xF5, bBuf);
                                                                  //start counting
//-
void DisableWDT(void)
1
      unsigned char bBuf;
      Set_F81866_LD(0x07);
                                                                  //switch to logic device 7
      bBuf = Get_F81866_Reg(0xFA);
      bBuf &= ~0x01;
      Set F81866 Reg(0xFA, bBuf);
                                                                  //disable WDTO output
      bBuf = Get_F81866_Reg(0xF5);
      bBuf &= ~0x20;
      bBuf \models 0x40;
      Set F81866 Reg(0xF5, bBuf);
                                                                  //disable WDT
}
//-
//_
11
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//___
#include "F81866.H"
#include <dos.h>
//-
unsigned int F81866 BASE:
void Unlock F81866 (void);
void Lock F81866 (void);
//---
unsigned int Init_F81866(void)
{
       unsigned int result;
      unsigned char ucDid;
      F81866_BASE = 0x4E;
      result = F81866_BASE;
```

ucDid = Get F81866 Reg(0x20); if (ucDid == 0x07)//Fintek 81866 goto Init\_Finish; { } F81866\_BASE = 0x2E; result = F81866 BASE;  $ucDid = Get_F81866_Reg(0x20);$ if (ucDid == 0x07)//Fintek 81866 goto Init\_Finish; { } F81866\_BASE = 0x00; result = F81866 BASE; Init\_Finish: return (result): } //--void Unlock\_F81866 (void) { outportb(F81866\_INDEX\_PORT, F81866\_UNLOCK); outportb(F81866\_INDEX\_PORT, F81866\_UNLOCK); } //-void Lock\_F81866 (void) { outportb(F81866\_INDEX\_PORT, F81866\_LOCK); } //----void Set\_F81866\_LD( unsigned char LD) { Unlock\_F81866(); outportb(F81866\_INDEX\_PORT, F81866\_REG\_LD); outportb(F81866\_DATA\_PORT, LD); Lock\_F81866(); } //\_\_ void Set\_F81866\_Reg( unsigned char REG, unsigned char DATA) { Unlock\_F81866(); outportb(F81866 INDEX PORT, REG); outportb(F81866\_DATA\_PORT, DATA); Lock\_F81866(); unsigned char Get F81866 Reg(unsigned char REG) { unsigned char Result; Unlock\_F81866(); outportb(F81866\_INDEX\_PORT, REG); Result = inportb(F81866\_DATA\_PORT); Lock\_F81866(); return Result; //-----// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY // KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE // IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR // PURPOSE. // //-----#ifndef \_\_F81866\_H #define \_\_F81866\_H 1 //-----#define F81866\_INDEX\_PORT #define F81866\_DATA\_PORT (F81866\_BASE) (F81866 BASE+1) //-----#define F81866\_REG\_LD 0x07 //\_\_\_\_\_

#define F81866_UNLOCK	0x87	
#define F81866_LOCK		0xAA
//		
unsigned int Init_F81866(void);		
void Set_F81866_LD( unsigned char	;);	

#endif //\_\_F81866\_H

## **BIOS Setup**

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

BIOS Introduction	32
BIOS Setup	
Advanced Settings	
Chipset Settings	
Boot Settings	
CSM parameters	54
Security Settings	55

#### **BIOS Introduction**

The BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

#### **BIOS Setup**

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

Press <DEL> / <F2> to Enter Setup

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

*Warning:* It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.

#### Main Settings

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.

Main Adv	/anced	Chipset	Boot	Security	V Save & Exit
BIOS Informa	tion				Choose the system default language
System Langu System Date System Time Access Level	uage		[English] [Fri 02/21/2014] [10:30:55] Administrator		→ ←Select Screen ↑↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default E4: Supp ESC: Brit

#### System Language

Choose the system default language.

#### System Date

Set the Date. Use Tab to switch between Data elements.

#### System Time

Set the Time. Use Tab to switch between Data elements.
## **Advanced Settings**

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Util	ity	
------------------	-----	--

Main Advanced	Chipset	Boot	Security	Save & Exit
<ul> <li>PCI Subsystem Setting</li> <li>ACPI Settings</li> <li>Wake up event setting</li> <li>CPU Configuration</li> <li>SATA Configuration</li> <li>Thermal Configuration</li> <li>Shutdown Temperaturi</li> <li>LAN Bypass Configuration</li> <li>Intel(R) Rapid Start Te</li> <li>Intel(R) Anti-Theft Tect</li> <li>AMT Configuration</li> <li>Acoustic Management</li> <li>USB Configuration</li> <li>F81866 Super IO Conf</li> <li>F81866 H/W Monitor</li> <li>Serial Port Console Re</li> </ul>	e Configuration tion chnology ation nology Configuration Configuration iguration direction	Jra		→ ← Select Screen ↑↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

## **PCI Subsystem Settings**

Aptio Setup Utility
---------------------

Main Ad	Ivanced	Chipset	Boot	Securit	y Save & Exit
PCI Bus Dri	ver Version		V 2.05.02		→ ←Select Screen ↑↓ Select Item
PCI Commo PCI Latency VGA Palette PERR# Ger SERR# Ger ► PCI Expr	on Settings / Timer e Snoop heration heration ress Settings		[32 PCI Bus Clock [Disabled] [Disabled] [Disabled]	ks]	Fiter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

#### **PCI Latency Timer**

Value to be programmed into PCI Latency Timer Register.

#### **VGA Palette Snoop**

Enables or disables VGA Palette Registers Snooping.

#### **PERR# Generation**

Enables or disables PCI device to generate PERR#.

#### SERR# Generation

Enables or disables PCI device to generate SERR#.

#### PCI Express Settings

Change PCI Express devices settings.

## **PCI Express Settings**

Aptio Setup Utility

Main Advanced	Chipset	Boot	Security	y Save & Exit
Main         Advanced           PCI Express Device Regist         Relaxed Ordering           Extended Tag         No Snoop           Maximum Payload         Maximum Read Request           PCI Express Link Register         ASPM Support           WARNING:         Enabling ASP           PCI-E device         Extended Synch           Link Training Retry         Link Training Timeout           Unpopulated Links         Restore PCIE Register	Chipset er Settings Settings M may cause s to fail	Boot [Disabled] [Enabled] [Auto] [Auto] [Disabled] some [Disabled] [5] 100 [Keep Link ON] [Disabled]	Security	y Save & Exit → ← Select Screen ↑↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

#### **Relaxed Ordering**

Enables or disables PCI Express Device Relaxed Ordering.

#### **Extended Tag**

If ENABLED allows device to use 8-bit Tag field as a requester.

#### No Snoop

Enables or disables PCI Express Device No Snoop option.

#### Maximum Payload

Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

#### Maximum Read Request

Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

#### **ASPM Support**

Set the ASPM Level: Force L0s – Force all links to L0s State: AUTO – BIOS auto configure : DISABLE – Disables ASPM.

#### **Extended Synch**

If ENABLED allows generation of Extended Synchronization patterns.

## Link Training Retry

Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

#### Link Training Timeout

Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 1000 uS.

#### **Unpopulated Links**

In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.

Antio Setun Litility

## **ACPI Settings**

Main	Advanced	Chipset	Boot	Security	y Save & Exit
ACPIS	Settings				
Enable	ACPI Auto Conf		[Disabled]		→ ←Select Screen $\uparrow \downarrow$ Select Item
Enable ACPI S Lock L S3 Vid	e Hibernation Sleep State egacy Resources leo Repost		[Enabled] [S1 only (CPL [Disabled] [Disabled]	J Stop C…]	Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

#### **Enable Hibernation**

Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

## **ACPI Sleep State**

Select ACPI sleep state the system will enter, when the SUSPEND button is pressed.

#### Lock Legacy Resources

Enabled or Disabled Lock of Legacy Resources.

#### S3 Video Repost

Enable or disable S3 Video Repost.

#### Wake up event settings

			Aprilo Setup	otinty	
Main	Advanced	Chipset	Boot	Securit	y Save & Exit
Wake	system with Fixed T	ime	[Disabled]		
Wake	on Ring		[Enabled]		
Wake	on PCI PME		[Enabled]		
Wake	on PCIE Wake Ever	nt	[Enabled]		$\rightarrow$ $\leftarrow$ Select Screen
					↑↓ Select Item
					Enter: Select
					+- Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit

#### Wake system with Fixed Time

Enables or Disables System wake on alarm event. When enabled, System will wake on the hr::min:: sec specified.

## Wake on PCIE PME Wake Event

The options are Disabled and Enabled.

## **Trusted Computing**

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	V Save & Exit
Config	juration				
Secu	rity Device Sup		[Disabled]		$\rightarrow$ $\leftarrow$ Select Screen
Curre SUP	nt TPM Status Inforn PORT TUREND OF	mation F			↑↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

## Security Device Support

Enables or disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

## **CPU Configuration**

This section shows the CPU configuration parameters.

Main Advanced	Chipset	Boot	Security	y Save & Exit
CPU Configuration				
Intel (R) Xeon (R) CPU E3-1 CPU Signature Processor Family Microcode Patch FSB Speed Max CPU Speed Or U Speed Processor Cores Intel HT Technology Intel VT-x Technology Intel VT-x Technology Intel SMX Technology 64-bit EIST Technology CPU C3 state CPU C3 state CPU C3 state CPU C4 state CPU C7 state L1 Data Cache L1 Code Cache L2 Cache L3 Cache Hyper-threading Active Processor Cores Limit CPUID Maximum Execute Disable Bit Intel Virtualization Hardware Prefetcher Adjacent Cache Line Prefet CPU AEC	268L v3 @	2.30GHz 306c3 6 16 100 MHz 2300 MHz 2700 MHz 4 Supported		<ul> <li>→ ←Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>

Aptio Setup Utility

## Hyper-threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled, only one thread per enabled core is enabled.

#### **Active Processor Cores**

Number of cores to enable in each processor package.

#### Limit CPUID Maximum

Disabled for Windows XP.

#### **Execute Disable Bit**

#### BIOS SETUP

XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, Re33dHat Enterprise 3 Update 3.)

#### Intel Virtualization Technology

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

#### Hardware Prefetcher

To turn on/off the Mid level Cache (L2) streamer Prefetcher.

#### Adjacent Cache Line Prefetch

To turn on/off prefetching of adjacent cache lines.

#### SATA Configuration

SATA Devices Configuration.

			Aprilo Setup	Othicy	
Main A	dvanced	Chipset	Boot	Security	Save & Exit
SATA Con SATA Port Softwarn SATA Port Softwarn SATA Port Softwarn SATA Port Softwarn SATA Port Softwarn SATA Port	ntroller(s) de Selection t0 e Preserve t1 e Preserve t2 e Preserve t3 e Preserve t4 e Preserve t5 e Preserve		[Enabled] [AHCI] Empty Unknown Empty Unknown Empty Unknown Empty Unknown Empty Unknown		<ul> <li>→ ← Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>

## SATA Controller(s)

Enable / Disable Serial ATA Controller.

#### SATA Mode Selection

- (1) IDE Mode.
- (2) AHCI Mode.
- (3) RAID Mode.

## **Thermal Configuration**

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit	
► Pla	tform Thermal Confi	guration				

#### Platform Thermal Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
Platfo	rm Thermal Configur	ation			
Auton Active	natic Thermal Rep e Trip Point 0 F		[Enabled] 100		
Active	e Trip Point 1		[55 C]		
Active	e Trip Point 1 F		75		
Pas	ssive TC1 Value		1		
Pas	ssive TC2 Value		5		
Pas	ssive TSP Value		10		
PCH	Thermal Device		[Disabled]		

## **Automatic Thermal Reporting**

Configure CRT, PSV and ACO automatically based on values recommended in BWG's thermal reporting for thermal management settings. Set to Disable for manual configuration.

## Shutdown Temperature Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit	
APCI	Shutdown Tempera	ture	[Disabled]			

## **ACPI Shutdown Temperature**

Set function Disabled or 70/75/80/85/90/95/100  $^\circ\!\mathrm{C}$ 

## LAN Bypass Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit	
LAN B	sypass Configuration					
Bypas	s Quick Setting		[Normal]			

#### **Bypass Quick Setting**

Set LAN Bypass to Normal, Bypass, Firewall or Custom Define Mode

Normal mode: All LAN ports in NORMAL. When Watchdog monitor system hangs, software will initiates a system reboot.

Bypass mode: All LAN ports in BYPASS during power-off or watchdog initiates Bypass. System will not reboot.

Firewall mode: All LAN ports in BYPASS until software change it to NORMAL under OS. When watchdog monitors system hang, software will initiates a system reboot.

Custom Define mode: Customer defines watchdog reset, watchdog Bypass and power-off Bypass settings.

Main	Advanced	Chipset	Boot	Security	Save & Exit
LAN E	Bypass Configuration	l			
Вураз	ss Quick Setting		[Custom Define]		
WDT WDT	Reset Signal Bypass Setting		[Disabled]		
LA	N5 LAN6 Bypass		[Normal]		
LA	N7 LAN8 Bypass		[Normal]		
Ex	t LAN1 LAN2 Bypas	5	[Normal]		
Ex	t LAN3 LAN4 Bypas	5	[Normal]		
Syste	m OFF Bypass Setti	ng			
LA	N5 LAN6 Bypass		[Normal]		
LA	N7 LAN8 Bypass		[Normal]		
Ext	LAN1 LAN2 Bypass		[Normal]		
Ext	LAN3 LAN4 Bypass		[Normal]		

Aptio Setup Utility

Note: "Ext LAN Bypass" items only appear when extended IBASE LAN module card installed.

## AMT Configuration

Aptio Setup Utility							
Main	Advanced	Chipset	Boot	Security	Save & Exit		

#### BIOS SETUP

## **AMT Configuration**

Options are Enabled and Disabled.

Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

#### **Unconfigure ME**

Perform AMT/ME unconfigure without password operation.

#### **Amt Wait Timer**

Set timer to wait before sending ASF\_GET\_BOOT\_OPTIONS.

#### Activate Remote Assistance Process

Trigger CIRA boot.

#### **PET Progress**

User can Enable/Disable PET Events progress to receive PET events or not.

#### Watchdog Timer

Enable/Disable Watchdog Timer.

## Acoustic Management Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
Acoustic Management Configuration					

## BIOS SETUP

Automatic Acoustic Management	[Disabled]	
		$\rightarrow$ $\leftarrow$ Select Screen
		↑↓ Select Item
		Enter: Select
		+- Change Field
		F1: General Help
		F2: Previous Values
		F3: Optimized Default
		F4: Save ESC: Exit

Smart fan function Enable or Disable.

## **USB Configuration**

Aptio Setup Utility Main Advanced Chipset Boot Security Save & Exit USB Configuration USB Devices: 1 Keyboard, 1 Mouse, 2 Hubs Legacy USB Support [Enabled] USB3.0 Support [Enabled] → ← Select Screen XHCI Hand-off [Enabled] ↑↓ Select Item EHCI Hand-off [Disabled] Enter: Select Port 60/64 Emulation [Enabled] +- Change Field F1: General Help USB hardware delays and time-outs: F2: Previous Values USB Transfer time-out [20 sec] F3: Optimized Default Device reset tine-out [20 sec] F4: Save ESC: Exit Device power-up delay [Auto]

## Legacy USB Support

Enables Legacy USB support.

AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

## USB3.0 Support

Enable/Disable USB3.0 (XHCI) Controller support.

#### XHCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

#### **EHCI Hand-off**

Enabled/Disabled. This is a workaround for OSes without EHCI handoff support. The EHCI ownership change should be claimed by EHCI driver.

#### Port 64/60 Emulation

Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.

#### **USB Transfer time-out**

The time-out value for Control, Bulk, and Interrupt transfers.

#### **Device reset tine-out**

USB mass Storage device start Unit command time-out.

#### Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

## F81866 Super IO Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit
Super	O Configuration				
F8186 ► Sei	66 Super IO Chip rial Port 0 Configurat	tion	F81866		→ ←Select Screen   ↓ Select Item Enter: Select
► Sei Po KB	wer Failure /MS Power On	lion	[Always off] [None]	+ F F F	Change Field '1: General Help '2: Previous Values '3: Optimized Default
				F	4: Save ESC: Exit

#### **Serial Port Configuration**

Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.

#### F81866 H/W Monitor

Antio	Setun	l Itility	

Main Advanced	Chipset	Boot	Security	y Save & Exit
PC Health Status				
Fan1 smart fan control Fan2 smart fan control Fan3 smart fan control System temperature1 System temperature2 System temperature3 FAN1 Speed FAN2 Speed FAN3 Speed VIN1 VIN2 VIN3 VSB5V VCC3V VSB5V VCC3V VSB3V VBAT		[50 C] [50 C] [Disabled] +41 C +38 C +37 C 1545 RPM 1550 RPM 1546 RPM +1.776 V +5.171 V +12.408 V +5.016 V +3.392 V +3.392 V +3.264 V		<ul> <li>→ ←Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>

#### **Temperatures/Voltages**

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

#### Fan1/Fan2/Fan3 Smart Fan Control

This field enables or disables the smart fan feature. At a certain temperature, the fan starts turning. Once the temperature drops to a certain level, it stops turning again.

## **Chipset Settings**

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

		,	ipilo octup	Stilly	
Main	Advanced	Chipset	Boot	Security	Save & Exit
► PCł ► Sys	H-IO Configuration tem Agent (SA) C	n onfiguration			<ul> <li>→ ← Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>

Aptio Setup Utility

## **PCH-IO Configuration**

This section allows you to configure the North Bridge Chipset.

Main	Advanced	Chipset	Boot	Security	/ Save & Exit
Intel Intel Intel ► P( ► U: ► P( ► B)	PCH RC Version PCH SKU Name PCH Rev ID CI Express Configu SB Configuration CH Azalia Configur. OS Security Config	ration ation juration	1.6.2.0 C226 O5/C2		
PCH W Deep Disp CLKI SB C SLP Rest	LAN Controller ake on LAN Sx Power Policies lay Logic RUN# Logic RID _S4 Assertion Widtl ore AC Power Loss	'n	[Enabled] [Enabled] [Disabled] [Enabled] [Disabled] [Jisabled] [4-5 Seconds] [Last State]		<pre>→ ← Select Screen ↑↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit</pre>

Aptio Setup Utility

#### **PCH LAN Controller**

Enable or disable onboard NIC.

#### Wake on LAN

Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)

#### SLP\_S4 Assertion Width

Select a minimum assertion width of the SLP\_S4# signal.

#### **Restore AC Power Loss**

Select AC power state when power is re-applied after a power failure.

## **PCI Express Configuration**

Main Advanced	Chipset	Boot	Security	/ Save & Exit
PCI Express Configu	uration			
PCI Express Clock (	Gating	[Enabled]		
DMI Link ASPM Cor	itrol	[Enabled]		
DMI Link Extended	Synch Control	[Disabled]		
PCIE Root Port Fun	ction	[Disabled]		
Subtractive Decode		[Disabled]		
PCIE Port 1 is as	sign			
PCI Express Roo	t Port 2			$\rightarrow \leftarrow$ Select Screen
PCI Express Roo	t Port 3			↑↓ Select Item
PCI Express Roo	t Port 4			Enter: Select
PCI Express Roo	t Port 5			+- Change Field
PCI Express Roo	t Port 6			F1: General Help
PCI Express Roo	t Port 7			F2: Previous Values
PCI Express Roo	t Port 8			F3: Optimized Default
				F4: Save ESC: Exit

## **PCI Express Clock Gating**

Enable or disable PCI Express Clock Gating for each root port.

#### **DMI Link ASPM Control**

The control of Active State Power Management on both NB side and SB side of the DMI link.

#### **PCIE Root Port Function**

Enable or disable PCI express Root Port function swapping.

## **USB** Configuration

Main	Advanced	Chipset	Boot	Security	y Save & Exit
USB	Configuration				
USB XHCI BTCC	Precondition Mode G		[Disabled] [Smart Auto] [Enable]		→ ← Select Screen ↑↓ Select Item Enter: Select +- Change Field
USB	Ports Per-Port Dis	able Control	[Disabled]		F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

## **USB** Precondition

Precondition work on USB host controller and root ports for faster enumeration.

## **xHCI Mode**

Mode of operation of xHCI controller

## BTCG

Enable or disable trunk clock gating.

## **USB Ports Per-Port Disable Control**

Control each of the USB ports (0~13) disabling.

## **PCH Azalia Configuration**

Main	Advanced	Chipset	Boot	Security	y Save & Exit
PCH Azalia A: A:	Azalia Configurat zalia Docking Sup zalia PME	oport	[Auto] [Disabled] [Disabled]		→ ← Select Screen ↑↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

## Azalia

Control Detection of the Azalia device. Disabled = Azalia will unconditionally disabled. Enabled Azalia will be unconditionally enabled. Auto = Azalia will enabled if present, disabled otherwise.

## System Agent (SA) Configuration

			Aptio Setup Ut	tility	
Main	Advanced	Chipset	Boot	Security	/ Save & Exit
Syster	m Agent Bridge N	lame	Haswell		
Syster	m Agent RC Vers	sion	1.6.2.0		
VT-d (	Capability		Supported		
VT-d			[Enabled]		
CHAP	Device (B0:D7:	=0)	[Disabled]		$\rightarrow \leftarrow \texttt{Select Screen}$
Therm	nal Device (B0:D	4:F0)	[Disabled]		↑↓ Select Item
Enable	e NB CRID		[Disabled]		Enter: Select
BDAT	ACPI Table Sup	port	[Disabled]		+- Change Field F1: General Help
<ul> <li>Graphics Configuration</li> </ul>				F2: Previous Values	
► DM	II Configuration				F3: Optimized Default
► NB	PCIe Configurat	ion			F4: Save ESC: Exit
► Me	mory Configurati	on			
	– Power Manag	ement Control			
2.01	1 offer Manag				

## VT-d

Check to enable VT-d function on MCH.

## Enable NB CRID

Enable or disable NB CRID WorkAround.

## **Graphics Configuration**

Main Advanced	Chipset	Boot	Security	/ Save & Exit
Graphics Configuration IGFX VBIOS Version IGFX Frequency Graphics Turbo IMON Primary Display Internal Graphics GTT Size Aperture Size DVMT Pre-Allocated DVMT Total Gfx Mode Gfx Low Power Mode Graphics Performance ► LCD Control		2164 700 MHz 31 [Auto] [2MB] [256MB] [32M] [256M] [Enabled] [Disabled]		<ul> <li>→ ← Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>

#### Aptio Setup Utility

#### **Primary Display**

Select which of IGFX/PEG/PCI graphics device should be primary display or select SG for switchable Gfx.

#### **Internal Graphics**

Keep IGD enabled based on the setup options.

#### **DVMT Pre-Allocated**

Select DVMT 5.0 Pre-Allocated (Fixed) graphics memory size used by the internal graphics device.

#### **DVMT Total Gfx Mem**

Select DVMT 5.0 total graphics memory size used by the internal graphics device.

#### **Gfx Low Power Mode**

This option is applicable for SFF only.

## Primary IGFX Boot Display (LCD Control)

Select the Video Device that will be activated during POST. This has no effect if external graphics present. Secondary booty display selection will appear based on your selection. VGA modes will be supported only on primary display.

## **Memory Configuration**

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	y Save & Exit
Memo	ry Information				
Memo Total I	ry Frequency /lemory		1600 MHz 32768 MB (DDR3)	)	
DIMM	#0		8192 MB (DDR3)		
DIMM	#1		8192 MB (DDR3)		$\rightarrow$ $\leftarrow$ Select Screen
DIMM	#2		8192 MB (DDR3)		↑↓ Select Item
DIMM	#3		8192 MB (DDR3)		Enter: Select
CAS L	atency (tCL)		11		+- Change Field
Minim	um delay time				F1: General Help
C	AS to RAS (tRC	Dmin)	11		F2: Previous Values
R	ow Precharge (t	RPmin)	11		F3: Optimized Default
A	ctive to Precharg	ge (tRASmin)	28		F4: Save ESC: Exit
XMP F	Profile 1		Not Supported		
XMP F	Profile 2		Not Supported		

## **Boot Settings**

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	/ Save & Exit
Boot Con Setup Pro Bootup N Quiet Boo Fast Boo Boot moo	nfiguration ompt Timeout lumLock State ot ot de select		1 [On] [Disabled] [Disabled] [LEGACY]		→ ←Select Screen ↑↓ Select Item
FIXED B Boot Opt Boot Opt Boot Opt Boot Opt Boot Opt Boot Opt Boot Opt	OOT ORDER Pri ion #1 ion #2 ion #3 ion #4 ion #5 ion #6 ion #7 6 parameters	orities	[Hard Disk] [CD/DVD] [USB Hard [USB CD/D [USB Key] [USB Flopp [Network]	Disk] VD] VJ	Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

#### Setup Prompt Timeout

Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

## **Bootup NumLock State**

Select the keyboard NumLock state.

#### Quiet Boot

Enables/Disables Quiet Boot option.

#### Fast Boot

Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

#### **Boot Option Priorities**

Sets the system boot order.

## **CSM16** parameters

This section allows you to configure the boot settings.

			Aptio Setup Oti	iity	
Main	Advanced	Chipset	Boot	Security	y Save & Exit
CSM1 CSM1 GateA Option INT19	6 Parameters 6 Module Version 20 Active ROM Messages Trap Response		07.70 [Upon Re [Force BI0 [Immediat	quest] DS] e]	<ul> <li>→ ←Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> </ul>
					F4: Save ESC: Exit

#### GateA20 Active

UPON REQUEST: GA20 can be disabled using BIOS services ALWAYS: do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

#### **Option ROM Messages**

Set display mode for Option ROM

#### **INT19 Trap Response**

BIOS reaction on INT19 trapping by option ROM: IMMEDIATE: execute the trap right away. POSTPONED: execute the trap during legacy boot.

## **Security Settings**

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
Passw	ord Description				
If ONL this on for wh If ONL power or ente Admin The pa in the f Minimu Maxim	Y the Administrato ly limit access to S an entering Setup. Y the User's password and r or password and r or Setup. In Setup t istrator rights assword length mus following range: um length um length	r's password is so etup and is only a vord is set, then t nust be entered t he User will have st be	et, then asked his is a to boot a 3 20		<ul> <li>→ ←Select Screen</li> <li>↑ ↓ Select Item</li> <li>Enter: Select</li> <li>+- Change Field</li> <li>F1: General Help</li> <li>F2: Previous Values</li> <li>F3: Optimized Default</li> <li>F4: Save ESC: Exit</li> </ul>
Admin	istrator Password				
User F	Password				

## **Administrator Password**

Set Setup Administrator Password.

## **User Password**

Set User Password.

## Save & Exit Settings

Main	Advanced	Chipset	Boot	Security	y Save & Exit
Save	Changes and Exit				
Disca	rd Changes and Exit				
Save	Changes and Reset				
Disca	rd Changes and Rese	ət			$\rightarrow \leftarrow \texttt{Select Screen}$
Save Save Disca	Options Changes rd Changes				↑↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values
Resto	re Defaults				F3: Optimized Default
Save	as User Defaults				F4: Save ESC: Exit
Resto	re User Defaults				
Boot 0	Override				
Laund	ch EFI Shell from files	ystem device			

#### Aptio Setup Utility

#### Save Changes and Exit

Exit system setup after saving the changes.

#### **Discard Changes and Exit**

Exit system setup without saving any changes.

#### Save Changes and Reset

Reset the system after saving the changes.

#### **Discard Changes and Reset**

Reset system setup without saving any changes.

#### Save Changes

Save Changes done so far to any of the setup options.

#### **Discard Changes**

Discard Changes done so far to any of the setup options.

#### **Restore Defaults**

Restore/Load Defaults values for all the setup options.

#### Save as User Defaults

Save the changes done so far as User Defaults.

#### **Restore User Defaults**

Restore the User Defaults to all the setup options.

# **Drivers Installation**

This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

Intel Chipset Software Installation Utility	56
VGA Drivers Installation.	58
LAN Drivers Installation	61
Intel® Management Engine Interface	64
Intel® USB 3.0 Drivers	66

#### **IMPORTANT NOTE:**

After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

## **Intel Chipset Software Installation Utility**

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the DVD that comes with the board. Click *Intel* and then *Intel*(*R*) 8 *Series Chipset Drivers*.



2. Click Intel(R) Chipset Software Installation Utility.



## DRIVERS INSTALLATION

3. When the Welcome screen to the Intel® Chipset Device Software appears, click *Next* to continue.

4. Click *Yes* to accept the software license agreement and proceed with the installation process.

5. On the Readme File Information screen, click *Next* to continue the installation.



6. The Setup process is now complete. Click *Finish* to restart the computer and for changes to take effect.

## **VGA Drivers Installation**

1. Insert the DVD that comes with the board. Click *Intel* and then *Intel*(*R*) 8 *Series Chipset Drivers*.



2. Click Intel(R) Core(TM) i3/i5/i7 Graphics Driver.

<b>Inside T</b>	<b>his CD</b> Version : 8.7.5D @4
Intel       Image: AMD       Image:	Intel(R) Chipset Software Installation Utility Intel(R) Core(TM) i3/i5/i7 Graphics Driver Realtek High Definition Audio Driver Intel(R) PRO LAN Network Drivers Intel(R) iAMT 8.0 Drivers Intel(R) USB 3.0 Drivers
8	Intel(R) Core(TM) 13/65/67 Graphics Driver

#### DRIVERS INSTALLATION

3. When the Welcome screen appears, click Next to continue.



4. Click *Yes* to to agree with the license agreement and continue the installation.

ntel® Installation Framework		
ntel® HD Graphics Driver		
icense Agreement		(intel)
You must accept all of the terms of the licens program. Do you accept the terms?	e agreement in order to cont	inue the setup
INTEL SOFTWARE LICENSE AGREEMENT (A)	pha / Beta, Organizational Us	e) 🔺
IMPORTANT - READ BEFORE COPYING, INS	TALLING OR USING.	
Do not use or load this software and any as: until you have carefully read the following te Software, you agree to the terms of this Ag install or use the Software.	sociated materials (collectivel erms and conditions. By loadir reement. If you do not wish t	y, the "Software") 1g or using the to so agree, do not
The Software contains pre-release "alpha" o and which Intel Corporation ("Intel") may su of the Software. Intel can provide no assur	r "beta" code, which may not bstantially modify in producin ance that it will ever produce	: be fully functional g any "final" version or make generally
	< Back Ye	es No
	L Inte	el® Tostallation Framewo

5. On the screen shown below, click *Install* to continue.

Windows Security	<b>X</b>
Would you like to install this device software?	
Name: Intel Corporation Display adapters Publisher: Intel Corporation - Software and Firmwar	
Always trust software from "Intel Corporation - Software and Firmwar".	Install Don't Install
You should only install driver software from publishers you trust. <u>safe to install?</u>	How can I decide which device software is

# 6. Setup complete. Click *Finish* to restart the computer and for changes to take effect.

Intel® Installation Framework	
Intel® HD Graphics Driver	
Setup Is Complete	(intel)
You must restart this computer for the changes to take effect computer now?	ct. Would you like to restart the
<ul> <li>Yes, I want to restart this computer now.</li> <li>No, I will restart this computer later.</li> </ul>	
Click Finish, then remove any installation media from the driv	res.
	Finish Intel® Installation Framework

## LAN Drivers Installation

1. Insert the DVD that comes with the board. Click *Intel* and then *Intel*(*R*) 8 *Series Chipset Drivers*.



2. Click Intel(R) PRO LAN Network Driver.





#### 4. When the Welcome screen appears, click Next.

Networ	k Connections			lincer
	Installs drivers, In Networking Servi	ntel(R) Network Connectio :es.	ons, and Advanced	
	WARNING: This international trea	program is protected by c ties.	opyright law and	

5. Click *Next* to to agree with the license agreement.

6. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.

Setup Options Select the program features you want installed.	(intel)
Install:	
Feature Description Drivers for all wired Intel Network Connections	

7. The wizard is ready to begin installation. Click *Install* to begin the installation.

(Intel)
inter
lick Back. Click Cancel to
tall Cancel

8. When InstallShield Wizard is complete, click *Finish*.

## Intel® Management Engine Interface

⚠

The following application requires Microsoft .NET Framework 3.5 or later: Intel® Management Engine Components. Please install the latest version of Microsoft .NET Framework from Microsoft Download Center to run this application correctly.

#### Follow the steps below to install the Intel Management Engine.

1. Insert the DVD that comes with the board. Click *Intel* and then *Intel(R) 8 Series Chipset Drivers* and then *Intel(R) AMT 9.0 Drivers*.



## DRIVERS INSTALLATION

2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click the checkbox for **Install Intel® Control Center** & click *Next*.



#### 3. Click Yes to to agree with the license agreement.

tel® Installation Framework		
ntel® Management Engine icense Agreement	Components	(intel)
You must accept all of the terms of the licer program. Do you accept the terms?	nse agreement in order to c	ontinue the setup
INTEL SOFTWARE LICENSE AGREEMENT (C IMPORTANT - READ BEFORE COPYING, IN Do not use or load this software and any a until you have carefully read the following Software, you agree to the terms of this A install or use the Software,	JEM / IAV / ISV Distribution STALLING OR USING, ssociated materials (collecti terms and conditions. By loa greement, If you do not wis	& Single User)
Please Also Note: * If you are an Original Equipment Manufar (IHV), or Independent Software Vendor (IS * If you are an End-User, then only Exhibit	turer (OEM), Independent W), this complete LICENSE A, the INTEL SOFTWARE L	Hardware Vendor AGREEMENT applies; ICENSE AGREEMENT,
	< Back	Yes No Intel® Installation Framework

4. When the Setup Progress screen appears, click *Next*. Then, click *Finish* when the setup progress has been successfully installed.

## Intel® USB 3.0 Drivers

1. Insert the DVD that comes with the board. Click *Intel* and then *Intel*(*R*) 8 *Series Chipset Drivers*.



2. Click Intel(R) USB 3.0 Drivers.



3. When the Welcome screen to the InstallShield Wizard for Intel® USB 3.0 eXtensible Host Controller Driver, click *Next*.



4. Click *Yes* to to agree with the license agreement and continue the installation.

You must accept all of the terms of the license agreement in order to continue the setup program. Do you accept the terms?	
INTEL SOFTWARE LICENSE AGREEMENT (Alpha / Beta, Organizational Use)	*
IMPORTANT - READ BEFORE COPYING, INSTALLING OR USING.	E
Do not use or load this software and any associated materials (collectively, the "Software") until you have carefully read the following terms and conditions. By loading or using the Software, you agree to the terms of this Agreement. If you do not wish to so agree, do no install or use the Software.	t
The Software contains pre-release "alpha" or "beta" code, which may not be fully functiona and which Intel Corporation ("Intel") may substantially modify in producing any "final" versi of the Software. Intel can provide no assurance that it will ever produce or make generally	l on -
<back no<="" td="" yes=""><td></td></back>	

5. On the Readme File Information screen, click *Next* to continue the installation of the Intel® USB 3.0 eXtensible Host Controller Driver.

6. Setup complete. Click *Finish* to restart the computer and for changes to take effect.



# Appendix

## A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	System Timer
060h - 064h	Keyboard Controller
070h - 07Fh	Real Time Clock
080h - 09Fh	DMA Controller #2
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #3
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
3B0h-3DFh	Graphics adapter Controller
3F8h - 3FFh	Serial Port #0 (COM1)
2F8h - 2FFh	Serial Port #1 (COM2)
3E8h - 3EFh	Serial Port #2 (COM3)
2E8h - 2EFh	Serial Port #3 (COM4)
3E8h - 3EFh	Serial Port #4 (COM5)
2E8h - 2EFh	Serial Port #5 (COM6)
360h - 36Fh	Network Ports
### **B. Interrupt Request Lines (IRQ)**

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ4	Serial Port #1
IRQ3	Serial Port #2
IRQ5	Serial Port #3
IRQ11	Serial Port #4
IRQ8	Real Time Clock
IRQ14	Primary IDE
IRQ15	Secondary IDE

### C. Register of the LAN Bypass Controller

To fulfill the varied requests on LAN Bypass controller, IBASE provide the smart LAN Bypass controller. User can define the Bypass function behavior when the system is power-on, power-off and WDT signal is asserted.

The controller is behind the SMBus controller. The I<sup>2</sup>C address is listed as below:

	I <sup>2</sup> C Address (8bit)	Remark
1 <sup>st</sup> Controller	0x68	
2 <sup>nd</sup> Controller	0x6A	Optional

#### CR 0x22 : System-On Bypass Register

Attribute : Read / Write Reset default : 0x0000

Bit	LAN Port#	Read / Write	Description	
0	Eth5, 6		Enoble / Disoble I AN Rupese	
1	Eth7, 8		function when the system is power On.	
2	Expansion LAN Card Eth1, 2	Read / Write	Read / Write	1 = Enable LAN Bypass function
3	Expansion LAN Card Eth3, 4		0 = Disable LAN Bypass function	

### CR 0x24 : System-Off Bypass Register

Attribute : Read / Write Reset default : 0x0000

Bit	LAN Port#	Read / Write	Description
0	Eth5, 6		Enable / Disable I AN Bypass
1	Eth7, 8	Read / Write	function when the system is
2	Expansion LAN Card Eth1, 2		power Off. 1 = Enable LAN Bypass function
3	Expansion LAN Card Eth3, 4		0 = Disable LAN Bypass function

## CR 0x26 : Watchdog (WDT) WDT\_IN# Signal Control Register

Attribute : Read / Write Reset default : 0x00

Bit	Read / Write	Description
0	Read / Write	<ul> <li>WDT_OUT# Generator</li> <li>The capacity use the WDT to reset the system</li> <li>1 = Generate 100ms pulse to reset signal when WDT signal is asserted.</li> <li>0 = Ignore the WDT signal.</li> </ul>
1	Read / Write	<ul> <li>WDT LAN Bypass Enable</li> <li>The capacity use the WDT to set LAN</li> <li>Bypass function</li> <li>1 = Enable LAN Bypass function when the WDT signal is asserted.</li> <li><i>CR 0x28</i> and <i>CR 0x2A</i> will be available if this bit is set to "1".</li> <li>0 = Disable WDT LAN Bypass function.</li> </ul>

APPENDIX

2 ~ 7 Reserved	2 ~ 7
----------------	-------

## CR 0x28 : Watchdog (WDT) Bypass Control Register Attribute : Read / Write

Reset default : 0x0000

Bit	LAN Port#	Read / Write	Description
0	Eth5, 6		Enable / Disable WDT Bypass function for each
1	Eth7, 8		LAN port.
2	Expansion LAN Card Eth1, 2	Read / Write	1 = Follow the setting in "WDT Bypass Register <b>CR</b> <b>0x24</b> " when the WDT
3	Expansion LAN Card Eth3, 4	write	0 = Ignore to control the bypass when the WDT is asserted.

### CR 0x2A : Watchdog (WDT) Bypass Register

Attribute : Read / Write Reset default : 0x0000

Bit	LAN Port#	Read / Write	Description
0	Eth5, 6	Read / Write	The function works when the bit in <b>CR 0x28</b> is "1". It controls LAN Bypass function should be Enabled / Disabled when the WDT
1	Eth7, 8		
2	Expansion LAN Card Eth1, 2		signal is asserted. If the bit is set to "1" in "WDT Bypass Control Register

		<b>CR 0x28</b> ", it will follow below setting:
3	Expansion LAN Card Eth3, 4	1 = Enable LAN Bypass function
		0 = Disable LAN Bypass function

# CR 0x2C : Card Plugged and Bypass Status Register Attribute : Read

Reset default : N/A

Bit	LAN Port#	Read / Write	Description
0	Eth5, 6		
1	Eth7, 8		1 = The expansion slot is populated & support
2	Expansion LAN Card Eth1, 2	Read	<ul> <li>LAN Bypass function</li> <li>0 = The expansion slot is empty or does not support</li> </ul>
3	Expansion LAN Card Eth3, 4		LAN Bypass function