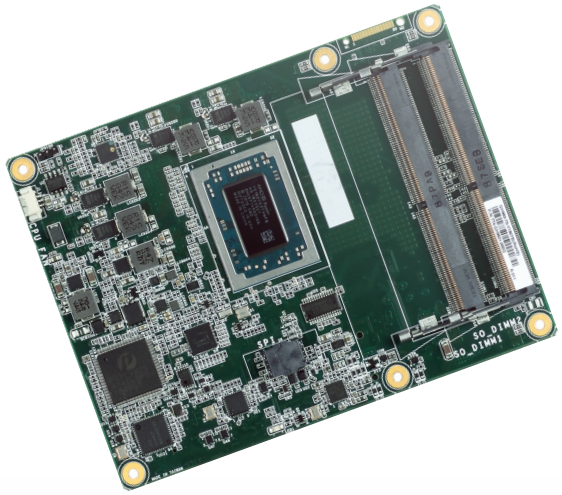
DFI



GH960

COM Express Basic Module
User's Manual

Preliminary Version

Copyright

Trademarks

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

1. The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
2. Shielded interface cables must be used in order to comply with the emission limits.

Table of Contents

About this Manual

This manual can be downloaded from the website, or acquired as an electronic file included in the optional CD/DVD. The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

Warranty

1. Warranty does not cover damages or failures that arised from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.

2. The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.

3. Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.

4. We will not be liable for any indirect, special, incidental or consequencial damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

1. To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.

2. Wear an antistatic wrist strap.

3. Do all preparation work on a static-free surface.

4. Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.

5. Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

Important:
Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

- To avoid damage to the system, use the correct AC input voltage range.

- To reduce the risk of electric shock, unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

- One GH960 board
- CPU Cooler

Optional Items

- COM332-B carrier board kit
- Heat Spreader

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

Before Using the System Board

When installing the system board in a new system, you will need at least the following internal components.

- Storage device such as hard disk drive, CD-ROM, etc.
- Power adaptor

External system peripherals may also be required for navigation and display, including at least a keyboard, a mouse and a video display monitor.

Chapter 1 - Introduction

▶ Specifications

SYSTEM	Processor	AMD® Ryzen™ Embedded Series: - V1807, Quad Core, 2MB Cache, 11 CU, 3.35GHz (3.8GHz), 35-54W - V1756, Quad Core, 2MB Cache, 8 CU, 3.25GHz (3.6GHz), 35-54W - V1605, Quad Core, 2MB Cache, 8 CU, 2.0GHz (3.6GHz), 12-25W - V1202, Dual Core, 1MB Cache, 3 CU, 2.3GHz (3.2GHz), 12-25W - R1606G, Dual Core, 1MB Cache, 3 CU, 2.6GHz (3.5GHz), 12-25W - R1505G, Dual Core, 1MB Cache, 3 CU, 2.4GHz (3.3GHz), 12-25W
	Memory	Two 260-pin SODIMM up to 32GB Dual Channel DDR4 up to 2400/3200MHz
	BIOS	Insyde SPI 64Mbit
GRAPHICS	Controller	AMD® Radeon™ Vega Graphics
	Feature	OpenGL 4.5, DirectX 12, OpenCL 2.1 HW Decode: AVC/H.264, MPEG2, VC1/WMV9, JPEG/MJPEG, HEVC/H265, VP8, VP9 HW Encode: MPEG2, AVC/H264, JPEG, HEVC/H265, VP8, VP9
	Display	1 x VGA/DDI (DDI available upon request) 1 x LVDS/eDP (eDP available upon request) 2 x DDI (HDMI/DVI/DP++) VGA: resolution up to 1920x1200 @ 60Hz LVDS: dual channel 24-bit, resolution up to 1920x1200 @ 60Hz eDP: resolution up to 3840x2160 @ 60 Hz HDMI: resolution up to 2560x1600 @ 60Hz or 4096x2160 @ 24Hz DVI: resolution up to 1920x1200 @ 60Hz DP++: resolution up to 4096x2304 @ 60Hz
	Quad Displays	VGA + LVDS + 2 DDI or eDP + 3 DDI (available upon request)
EXPANSION	Interface	1 x PCIe x8 (Gen 3) 6 x PCIe x1 or 2 x PCIe x2 or 1 x PCIe x4 1 x LPC 1 x I²C 1 x SPI 1 x SMBus 2 x UART (TX/RX)
AUDIO	Interface	HD Audio
ETHERNET	Controller	1 x Intel® I210AT PCIe (10/100/1000Mbps) (normal temp.) or 1 x Intel® I210IT PCIe (10/100/1000Mbps) (wide temp.)
I/O	USB	4 x USB 3.1 8 x USB 2.0
	SATA	2 x SATA 3.0 (up to 6Gb/s) RAID 0/1
	DIO	1 x 8-bit DIO (Default 4 inputs and 4 outputs)
WATCHDOG TIMER	Output & Interval	System Reset, Programmable via Software from 1 to 255 Seconds
SECURITY	TPM	TPM1.2/2.0 (Available Upon Request)
POWER	Type	12V, 5VSB, VCC_RTC (ATX mode) 12V, VCC_RTC (AT mode)
OS SUPPORT		Windows: Windows 10 IoT Enterprise 64-bit Linux
ENVIRONMENT	Temperature	Operating: 0 to 60°C, -40 to 85°C Storage: -40 to 85°C
	Humidity	Operating: 5 to 90% RH Storage: 5 to 90% RH
MECHANICAL	Dimensions	COM Express® Basic: 95mm (3.74") x 125mm (4.9")
	Compliance	PICMG COM Express® R3.0, Type 6

The specifications listed here may be based on editions that do not resemble your actual products. Please visit the download page at go.dfi.com/GH960 or via the QR code to the right for the latest datasheet.

▶ Features

Watchdog Timer

The Watchdog Timer function allows your application to regularly “clear” the system at the set time interval. If the system hangs or fails to function, it will reset at the set time interval so that your system will continue to operate.

DDR4

DDR4 delivers increased system bandwidth and improves performance. The advantages of DDR4 provide an extended battery life and improve the performance at a lower power than DDR3/DDR2. Instead of using memory connectors, the system features memory down with the support of ECC memory.

Graphics

The integrated Intel® HD graphics engine delivers an excellent blend of graphics performance and features to meet business needs. It provides excellent video and 3D graphics with outstanding graphics responsiveness. These enhancements deliver the performance and compatibility needed for today’s and tomorrow’s business applications. Supports VGA, LVDS, eDP and DDI display outputs.

Serial ATA

The system supports multiple SATA 3.0 (up to 6Gb/s) ports and allows for different configurations of RAID levels to meet various requirements for data redundancy and performance.

Gigabit LAN

The Intel® I210IT Gigabit LAN controller features up to 1Gbps data transmission with support for Intel® Active Management Technology. It provides remote maintenance and manageability for networked computing assets in an enterprise environment.

Wake-On-LAN

This feature allows the network to remotely wake up a Soft Power Down (Soft-Off) PC. It is supported via the onboard LAN port or via a PCI LAN card that uses the PCI PME (Power Management Event) signal. However, if your system is in the Suspend mode, you can power-on the system only through an IRQ or DMA interrupt.

USB

The system board supports the new USB 3.0. It is capable of running at a maximum transmission speed of up to 5 Gbit/s (625 MB/s) and is faster than USB 2.0 (480 Mbit/s, or 60 MB/s) and USB 1.1 (12Mb/s). USB 3.0 reduces the time required for data transmission, reduces power consumption, and is backward compatible with USB 2.0. It is a marked improvement in device transfer speeds between your computer and a wide range of simultaneously accessible external Plug and Play peripherals.

ACPI STR

The system board is designed to meet the ACPI (Advanced Configuration and Power Interface) specification. ACPI has energy saving features that enables PCs to implement Power Management and Plug-and-Play with operating systems that support OS Direct Power Management. ACPI when enabled in the Power Management Setup will allow you to use the Suspend to RAM function.
With the Suspend to RAM function enabled, you can power-off the system at once by pressing the power button or selecting “Standby” when you shut down Windows® without having to go through the sometimes tiresome process of closing files, applications and operating system. This is because the system is capable of storing all programs and data files during the entire operating session into RAM (Random Access Memory) when it powers-off. The operating session will resume exactly where you left off the next time you power-on the system.

Power Failure Recovery

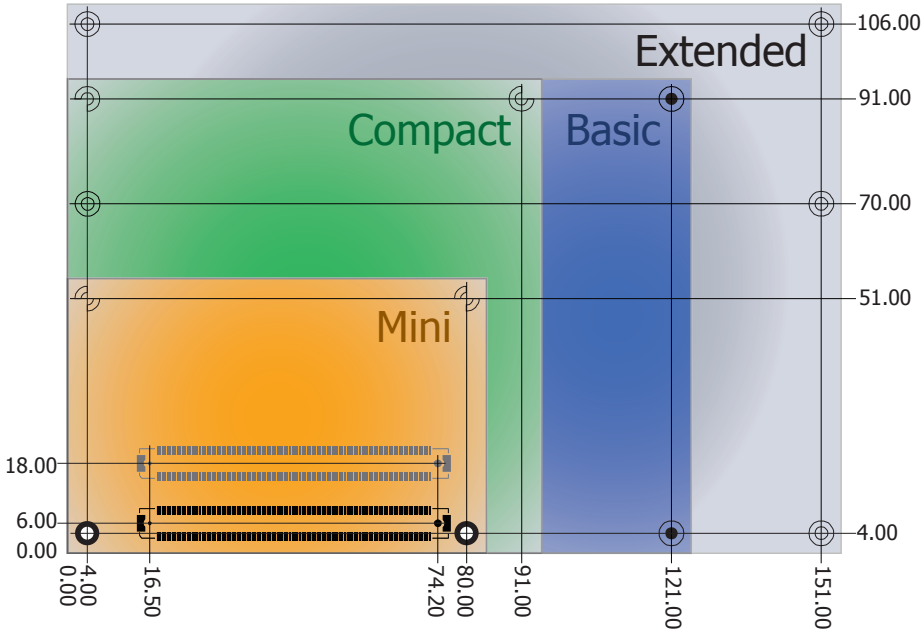
When power returns after an AC power failure, you may choose to either power-on the system manually or let the system power-on automatically.

▶ Concept

COM Express

Computer-on-module (COM) Express is a PC form factor designed with the core computing integrated on a fairly compact module. All the I/O signals and power supply are concentrated and mapped to the board-to-board connectors on the bottom side to interface with a carrier board that is typically customized to fit the application. When an upgrade or change of application is needed, the physical separation of the core computing and the I/O of COM Express cuts back the cost greatly, whereas canonical IPC designs would typically require an entire makeover. The COM Express module can be replaced when there is only need to upgrade for higher computing performance, while the carrier board can be redesigned when there is solely change in application. COM Express also comes in different form factors and signal Types cut out for different scales and aspects of the system's application. Detailed specifications of COM Express are available on the website of PCI Industrial Computer Manufacturers Group (PICMG).

- Common for all Form Factors
- Extended only
- Basic only
- Compact only
- Compact and Basic only
- Mini only



Carrier Board

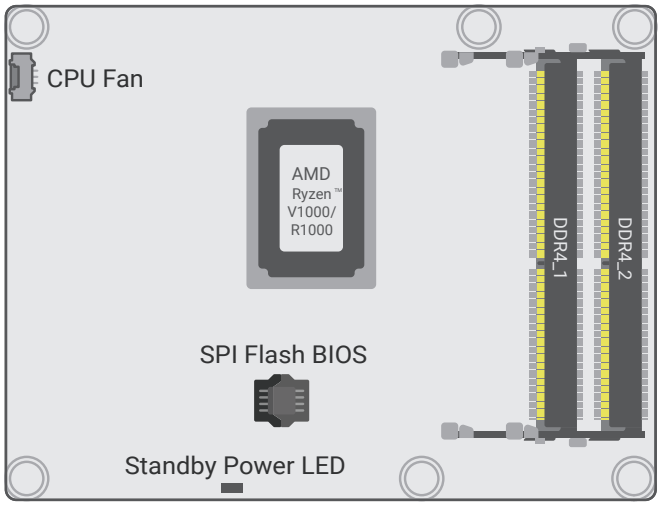
The design of a carrier board for COM Express greatly depends on the form factor and signal Type of the COM Express module. The carrier board typically handles — but not limited to — one COM Express module, and is populated with stand-offs that conform to the form factor of the module's mounting holes.

GH960 is a Type 6 COM Express (R3.0) module compatible with DFI's proprietary carrier board — COM332-B — as an optional item. If the carrier board is to be customized, the design guide for the carrier board can be attained via the Partner Zone page on our website.

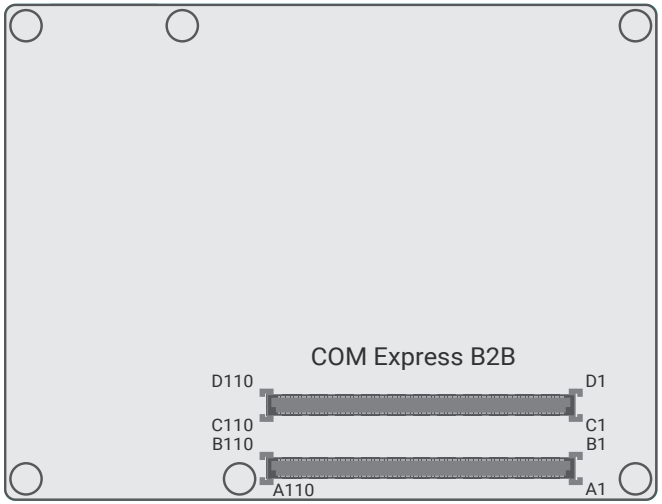
Chapter 2 - Hardware Installation

▶ Board Layout

Top View

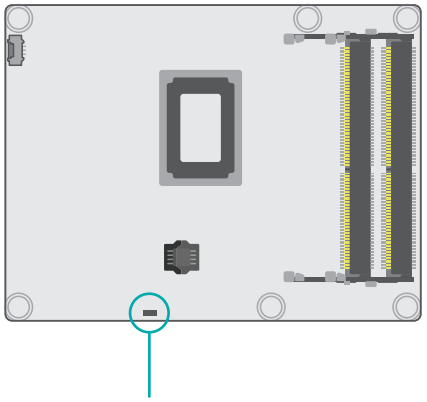


Bottom View



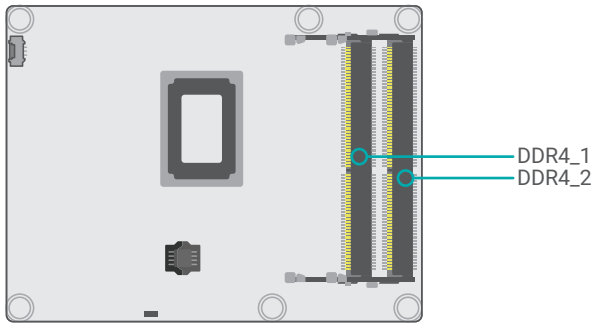
Important:
Electrostatic discharge (ESD) can damage your board, processor, disk drives, add-in boards, and other components. Perform installation procedures at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

▶ Standby Power LED



Important:
When the Standby Power LED lights red, it indicates that there is power on the system board. Power-off the PC then unplug the power cord prior to installing any devices. Failure to do so will cause severe damage to the motherboard and components.

▶ System Memory



The system board supports the following memory interface.

Single Channel (SC)
Data will be accessed in chunks of 64 bits from the memory channels.

Dual Channel (DC)
Data will be accessed in chunks of 128 bits from the memory channels. Dual channel provides better system performance because it doubles the data transfer rate.

Single Channel	DIMMs are on the same channel. DIMMs in a channel can be identical or completely different. However, we highly recommend using identical DIMMs. Not all slots need to be populated.
Dual Channel	DIMMs of the same memory configuration are on different channels.

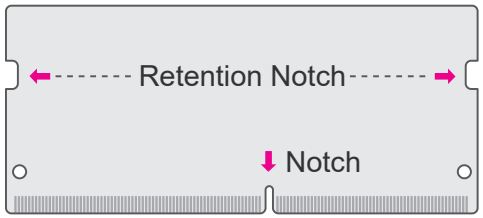
Features

- DDR4 2400/3200 MHz memory
- ECC or Non-ECC
- Dual channel memory interface

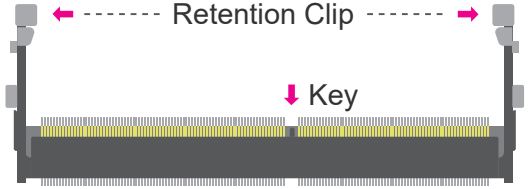
Installing the SO-DIMM Module

Before installing the memory module, please make sure that the following safety cautions are well-attended.

1. Make sure the PC and all other peripheral devices connected to it has been powered down.
2. Disconnect all power cords and cables.
3. Locate the SO-DIMM socket on the system board
4. Make sure the notch on memory card is aligned to the key on the socket.

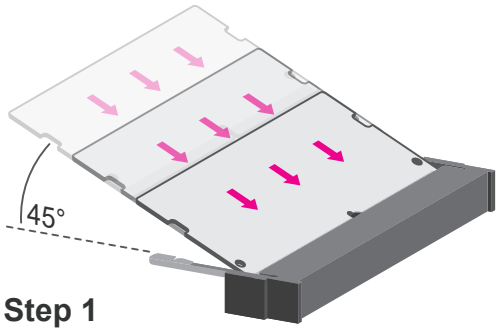


DDR4 SO-DIMM



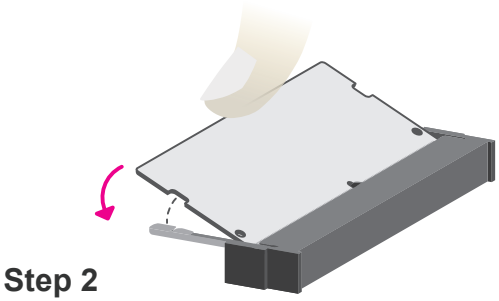
Socket Top View

Please follow the steps below to install the memory card into the socket.



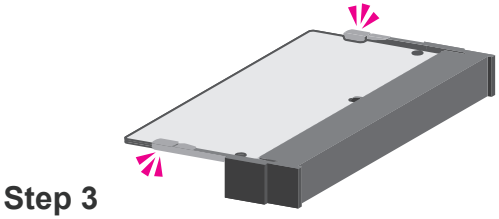
Step 1

Step 1:
Insert the memory card into the slot while making sure 1) the notch and the key are aligned, and 2) the non-connector end rises approximately 45 degrees horizontally. Press the card firmly into the socket while applying and maintaining even pressure on both ends.



Step 2

Step 2:
Press the end of the card far from the socket down while making sure the retention notch and the clip align as indicated by the dotted line in the illustration. If the retention notch and the clip do not align, please remove the card and re-insert it. Press the card all the way down.

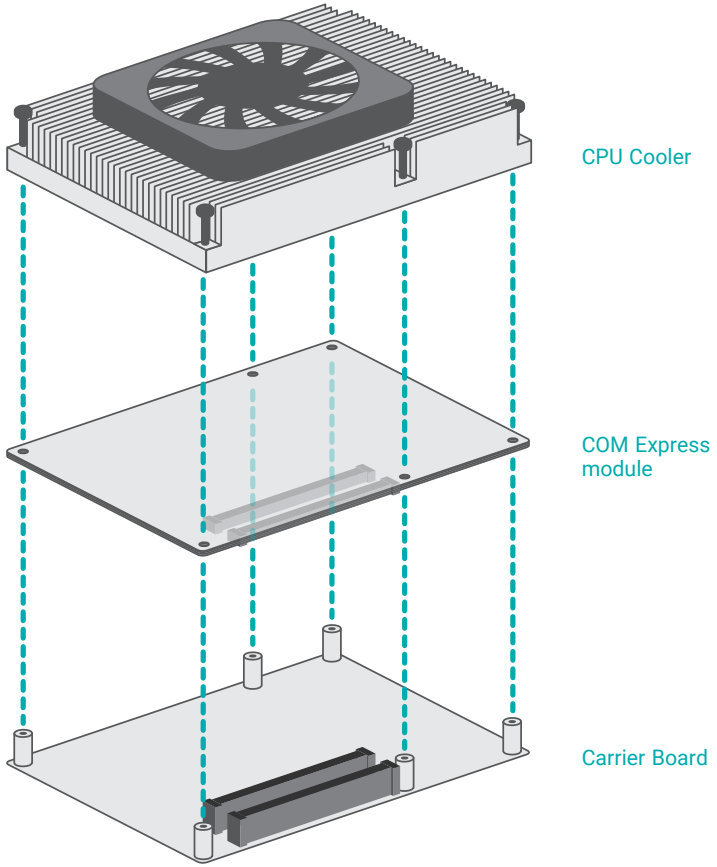


Step 3

Step 3:
The clips snap automatically and abruptly to the retention notches of the card sounding a distinctive click, and lock the card in place. Inspect that the clip sits in the notch. If not, please pull the clips outward, release and remove the card, and mount it again.

▶ Assembly

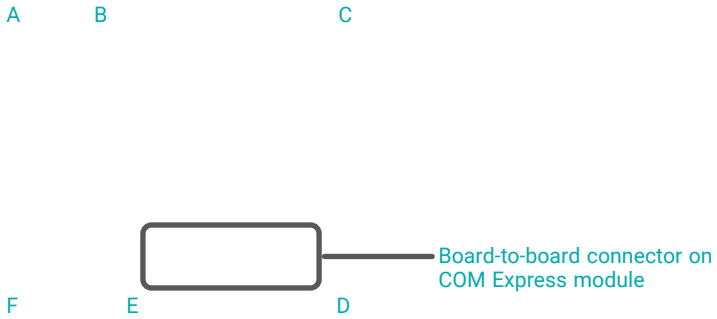
A CPU cooler is included in the standard package. The CPU cooler contains six spring screws and shall be installed after the COM Express module is securely mounted onto the carrier board. Please make sure the cooler, the module, and the carrier board are oriented correctly by inspecting whether the screws, screw holes, and stand-offs all align.

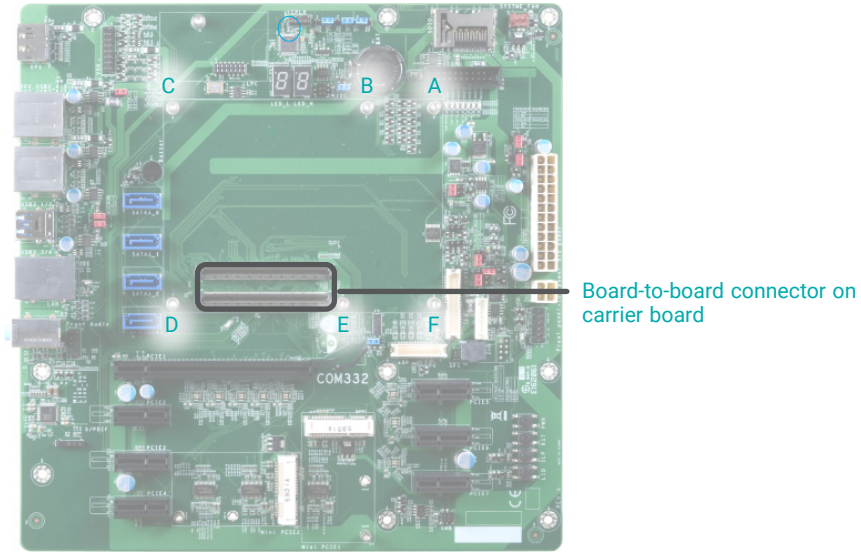


Note:
The carrier board is not included in the standard package and is typically customized.

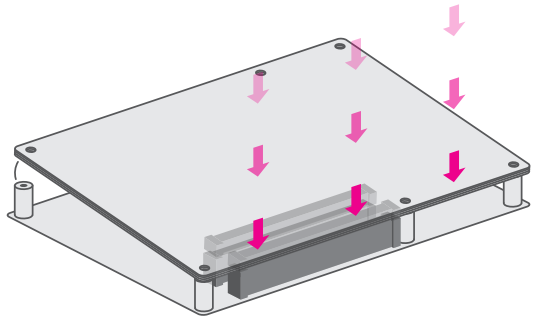
Assembly

1. Locate the COM Express board-to-board connectors on the bottom side of the module and the carrier board. Locate the mounting holes on the module and the corresponding stand-offs on the carrier board.

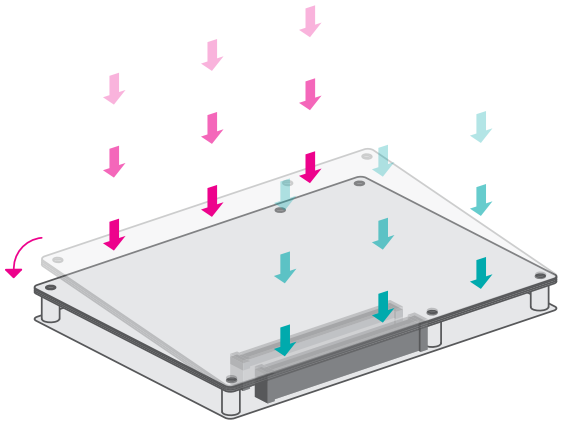




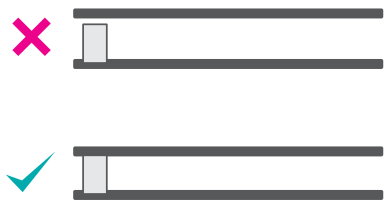
2. Place the module on the carrier board while making sure the mounting holes and connectors all align. At the long edge of the module closer to the connector, apply firm pressure onto the module and press it onto the the carrier board until the three stand-offs and the edge of the module close up. The other edge of the module away from the connector may still remain slightly aloft from the stand-offs at this moment.



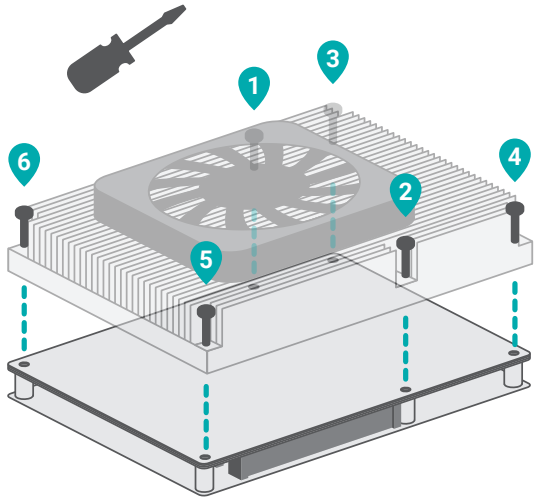
3. At the long edge away from the connector, apply firm pressure with another hand onto the module and press it onto the carrier board until the module is against the remaining three stand-offs. Please also maintain the pressure described in the previous step the whole time.



4. Inspect whether the gaps between the module and the stand-offs all close up. It is highly recommended that the module be removed and installed again following the previous steps when there is discernable gap.

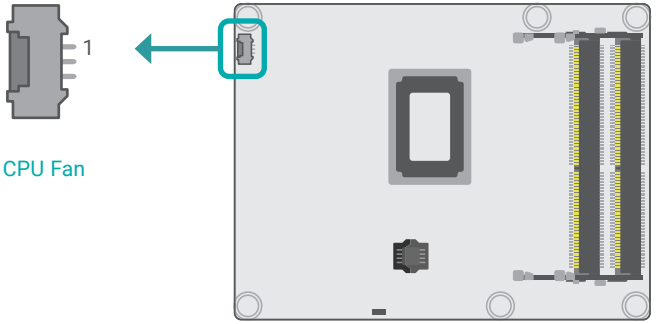


5. Place the CPU cooler, i.e. heatsink and fan, onto the module while making sure the screws on the cooler align with the screw holes on the module. The thermal interface metals underneath the cooler should also sit directly on top of the CPU and PCH chipsets on the module. Use a screw driver to fasten the screws in the order as numbered below. By following the order, the risk of damaging the component is significantly reduced.



▶ I/O Connectors

CPU Fan



■ CPU Fan

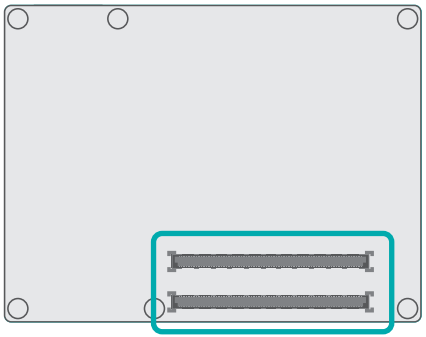
The fan connector is used to connect to cooling fans. Cooling fans provide adequate air circulation throughout the chassis and dissipate heat to prevent overheating of the system board and components.

BIOS Setting
Fan speed can be read in the Advanced menu (“SIO IT8528E” submenu) of the BIOS. Refer to chapter 3 for more information.

■ 3-pin Fan Pin Assignment

Pin	Assignment
1	Ground
2	Power
3	Sense

Board-to-board Connector



Board-to-board connector

The two board-to-board connectors are located at the bottom side of the COM Express module. Four rows (row A to row D) of pins and their signal are specified as listed below.

Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME# / ESPI_CS0#
A4	GBE0_LINK100#	B4	LPC_AD0 / ESPI_IO_0
A5	GBE0_LINK1000#	B5	LPC_AD1 /ESPI_IO_1
A6	GBE0_MDI2-	B6	LPC_AD2 / ESPI_IO_2
A7	GBE0_MDI2+	B7	LPC_AD3 / ESPI_IO_3
A8	GBE0_LINK#	B8	LPC_DRQ0# / ESPI_ALERT0#
A9	GBE0_MDI1-	B9	LPC_DRQ1# / ESPI_ALERT1#
A10	GBE0_MDI1+	B10	LPC_CLK /ESPI_CK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	GBE0_CTREF	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	SUS_STAT# /ESPI_RESET#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	SATA2_TX+	B22	SATA3_TX+
A23	SATA2_TX-	B23	SATA3_TX-
A24	SUS_S5#	B24	PWR_OK
A25	SATA2_RX+	B25	SATA3_RX+
A26	SATA2_RX-	B26	SATA3_RX-
A27	BATLOW#	B27	WDT
A28	(S)ATA_ACT#	B28	HDA_SDIN2
A29	HDA_SYNC	B29	HDA_SDIN1
A30	HDA_RST#	B30	HDA_SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	HDA_BITCLK	B32	SPKR
A33	HDA_SDOUT	B33	I2C_CK
A34	BIOS_DIS0# /ESPI_SAFS	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	ESPI_EN#
A48	RSVD	B48	USB0_HOST_PRSNT
A49	GBE0_SDP	B49	SYS_RESET#
A50	LPC_SERIRQ /ESPI_CS1#	B50	CB_RESET#
A51	GND (FIXED)	B51	GND (FIXED)
A52	PCIE_TX5+	B52	PCIE_RX5+
A53	PCIE_TX5-	B53	PCIE_RX5-
A54	GPI0	B54	GPO1
A55	PCIE_TX4+	B55	PCIE_RX4+
A56	PCIE_TX4-	B56	PCIE_RX4-
A57	GND	B57	GPO2
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	GND (FIXED)	B60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-

Pin	Row A	Pin	Row B
A70	GND (FIXED)	B70	GND (FIXED)
A71	LVDS_A0+/ eDP_TX2+	B71	LVDS_B0+
A72	LVDS_A0-/ eDP_TX2-	B72	LVDS_B0-
A73	LVDS_A1+/ eDP_TX1+	B73	LVDS_B1+
A74	LVDS_A1-/ eDP_TX1-	B74	LVDS_B1-
A75	LVDS_A2+/ eDP_TX0+	B75	LVDS_B2+
A76	LVDS_A2-/ eDP_TX0-	B76	LVDS_B2-
A77	LVDS_VDD_EN/ eDP_VDD_EN	B77	LVDS_B3+
A78	LVDS_A3+	B78	LVDS_B3-
A79	LVDS_A3-	B79	LVDS_BKLT_EN/ eDP_BKLT_EN
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+/ eDP_TX3+	B81	LVDS_B_CK+
A82	LVDS_A_CK-/ eDP_TX3-	B82	LVDS_B_CK-
A83	LVDS_I2C_CK/ eDP_AUX+	B83	LVDS_BKLT_CTRL/ eDP_BKLT_CTRL
A84	LVDS_I2C_DAT/ eDP_AUX-	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY
A86	RSVD	B86	VCC_5V_SBY
A87	eDP_HPD	B87	VCC_5V_SBY
A88	PCIE0_CLK_REF+	B88	BIOS_DIS1#
A89	PCIE0_CLK_REF-	B89	VGA_RED
A90	GND (FIXED)	B90	GND (FIXED)
A91	SPI_POWER	B91	VGA_GRN
A92	SPI_MISO	B92	VGA_BLU
A93	GPO0	B93	VGA_HSYNC
A94	SPI_CLK	B94	VGA_VSYNC
A95	SPI_MOSI	B95	VGA_I2C_CK
A96	TPM_PP	B96	VGA_I2C_DAT
A97	TYPE10#	B97	SPI_CS#
A98	SER0_TX	B98	RSVD
A99	SER0_RX	B99	RSVD
A100	GND (FIXED)	B100	GND (FIXED)
A101	SER1_TX	B101	FAN_PWNOUT
A102	SER1_RX	B102	FAN_TACHIN
A103	LID#	B103	SLEEP#
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)

Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)
C2	GND	D2	GND
C3	USB_SSRX0-	D3	USB_SSTX0-
C4	USB_SSRX0+	D4	USB_SSTX0+
C5	GND	D5	GND
C6	USB_SSRX1-	D6	USB_SSTX1-
C7	USB_SSRX1+	D7	USB_SSTX1+
C8	GND	D8	GND
C9	USB_SSRX2-	D9	USB_SSTX2-
C10	USB_SSRX2+	D10	USB_SSTX2+
C11	GND (FIXED)	D11	GND (FIXED)
C12	USB_SSRX3-	D12	USB_SSTX3-
C13	USB_SSRX3+	D13	USB_SSTX3+
C14	GND	D14	GND
C15	DDI1_PAIR6+	D15	DDI1_CTRLCLK_AUX+
C16	DDI1_PAIR6-	D16	DDI1_CTRLDATA_AUX-
C17	RSVD	D17	RSVD
C18	RSVD	D18	RSVD
C19	PCIE_RX6+	D19	PCIE_TX6+
C20	PCIE_RX6-	D20	PCIE_TX6-
C21	GND (FIXED)	D21	GND (FIXED)
C22	PCIE_RX7+	D22	PCIE_TX7+
C23	PCIE_RX7-	D23	PCIE_TX7-
C24	DDI1_HPD	D24	RSVD
C25	DDI1_PAIR4+	D25	RSVD
C26	DDI1_PAIR4-	D26	DDI1_PAIR0+
C27	RSVD	D27	DDI1_PAIR0-
C28	RSVD	D28	RSVD
C29	DDI1_PAIR5+	D29	DDI1_PAIR1+
C30	DDI1_PAIR5-	D30	DDI1_PAIR1-
C31	GND (FIXED)	D31	GND (FIXED)
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL
C35	RSVD	D35	RSVD
C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+
C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3-
C38	DDI3_DDC_AUX_SEL	D38	RSVD
C39	DDI3_PAIR0+	D39	DDI2_PAIR0+
C40	DDI3_PAIR0-	D40	DDI2_PAIR0-
C41	GND (FIXED)	D41	GND (FIXED)
C42	DDI3_PAIR1+	D42	DDI2_PAIR1+
C43	DDI3_PAIR1-	D43	DDI2_PAIR1-
C44	DDI3_HPD	D44	DDI2_HPD
C45	RSVD	D45	RSVD
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+
C47	DDI3_PAIR2-	D47	DDI2_PAIR2-
C48	RSVD	D48	RSVD

Pin	Row C	Pin	Row D
C49	DDI3_PAIR3+	D49	DDI2_PAIR3+
C50	DDI3_PAIR3-	D50	DDI2_PAIR3-
C51	GND (FIXED)	D51	GND (FIXED)
C52	PEG_RX0+	D52	PEG_TX0+
C53	PEG_RX0-	D53	PEG_TX0-
C54	TYPE0#	D54	PEG_LANE_RV#
C55	PEG_RX1+	D55	PEG_TX1+
C56	PEG_RX1-	D56	PEG_TX1-
C57	TYPE1#	D57	TYPE2#
C58	PEG_RX2+	D58	PEG_TX2+
C59	PEG_RX2-	D59	PEG_TX2-
C60	GND (FIXED)	D60	GND (FIXED)
C61	PEG_RX3+	D61	PEG_TX3+
C62	PEG_RX3-	D62	PEG_TX3-
C63	RSVD	D63	RSVD
C64	RSVD	D64	RSVD
C65	PEG_RX4+	D65	PEG_TX4+
C66	PEG_RX4-	D66	PEG_TX4-
C67	RAPID_SHUTDOWN	D67	GND
C68	PEG_RX5+	D68	PEG_TX5+
C69	PEG_RX5-	D69	PEG_TX5-
C70	GND (FIXED)	D70	GND (FIXED)
C71	PEG_RX6+	D71	PEG_TX6+
C72	PEG_RX6-	D72	PEG_TX6-
C73	GND	D73	GND
C74	PEG_RX7+	D74	PEG_TX7+
C75	PEG_RX7-	D75	PEG_TX7-
C76	GND	D76	GND
C77	RSVD	D77	RSVD
C78	PEG_RX8+	D78	PEG_TX8+
C79	PEG_RX8-	D79	PEG_TX8-
C80	GND (FIXED)	D80	GND (FIXED)
C81	PEG_RX9+	D81	PEG_TX9+
C82	PEG_RX9-	D82	PEG_TX9-
C83	RSVD	D83	RSVD
C84	GND	D84	GND
C85	PEG_RX10+	D85	PEG_TX10+
C86	PEG_RX10-	D86	PEG_TX10-
C87	GND	D87	GND
C88	PEG_RX11+	D88	PEG_TX11+
C89	PEG_RX11-	D89	PEG_TX11-
C90	GND (FIXED)	D90	GND (FIXED)
C91	PEG_RX12+	D91	PEG_TX12+
C92	PEG_RX12-	D92	PEG_TX12-
C93	GND	D93	GND
C94	PEG_RX13+	D94	PEG_TX13+
C95	PEG_RX13-	D95	PEG_TX13-
C96	GND	D96	GND
C97	RSVD	D97	RSVD
C98	PEG_RX14+	D98	PEG_TX14+
C99	PEG_RX14-	D99	PEG_TX14-
C100	GND (FIXED)	D100	GND (FIXED)
C101	PEG_RX15+	D101	PEG_TX15+
C102	PEG_RX15-	D102	PEG_TX15-
C103	GND	D103	GND
C104	VCC_12V	D104	VCC_12V
C105	VCC_12V	D105	VCC_12V
C106	VCC_12V	D106	VCC_12V
C107	VCC_12V	D107	VCC_12V
C108	VCC_12V	D108	VCC_12V
C109	VCC_12V	D109	VCC_12V
C110	GND (FIXED)	D110	GND (FIXED)

▶ Signal Descriptions

Pin Types

I Input to the Module
O Output from the Module
I/O Bi-directional input / output signal
OD Open drain output
RSVD pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

AC97/HDA Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
AC/HDA_RST#	A30	O CMOS	3.3V Suspend/3.3V	series 33Ω resistor	Reset output to CODEC, active low.	CODEC Reset.
AC/HDA_SYNC	A29	O CMOS	3.3V/3.3V	series 33Ω resistor	Sample-synchronization signal to the CODEC(s).	Serial Sample Rate Synchronization.
AC/HDA_BITCLK	A32	I/O CMOS	3.3V/3.3V	series 22Ω resistor	Serial data clock generated by the external CODEC(s).	24 MHz Serial Bit Clock for HDA CODEC.
AC/HDA_SDOUT	A33	O CMOS	3.3V/3.3V	series 33Ω resistor	Serial TDM data output to the CODEC.	Audio Serial Data Output Stream.
AC/HDA_SDIN0	B30	I/O CMOS	3.3V Suspend/3.3V		Serial TDM data inputs from up to 3 CODECs.	Audio Serial Data Input Stream from CODEC[0:2].
AC/HDA_SDIN1	B29	I/O CMOS	3.3V Suspend/3.3V			
AC/HDA_SDIN2	B28	I/O CMOS	3.3V Suspend/3.3V			

Gigabit Ethernet Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
GBE0_MDI0+	A13	I/O Analog	3.3V max Suspend		Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T / 100BASE-TX / 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	Media Dependent Interface (MDI) differential pair 0.
GBE0_MDI0-	A12	I/O Analog	3.3V max Suspend			
GBE0_MDI1+	A10	I/O Analog	3.3V max Suspend			Media Dependent Interface (MDI) differential pair 1.
GBE0_MDI1-	A9	I/O Analog	3.3V max Suspend			
GBE0_MDI2+	A7	I/O Analog	3.3V max Suspend			Media Dependent Interface (MDI) differential pair 2. Only used for 1000Mbit/sec Gigabit Ethernet mode.
GBE0_MDI2-	A6	I/O Analog	3.3V max Suspend			
GBE0_MDI3+	A3	I/O Analog	3.3V max Suspend			Media Dependent Interface (MDI) differential pair 3. Only used for 1000Mbit/sec Gigabit Ethernet mode.
GBE0_MDI3-	A2	I/O Analog	3.3V max Suspend			
GBE0_ACT#	B2	OD CMOS	3.3V Suspend/3.3V		Gigabit Ethernet Controller 0 activity indicator, active low.	Ethernet controller 0 activity indicator, active low.
GBE0_LINK#	A8	OD CMOS	3.3V Suspend/3.3V		Gigabit Ethernet Controller 0 link indicator, active low.	Ethernet controller 0 link indicator, active low.
GBE0_LINK100#	A4	OD CMOS	3.3V Suspend/3.3V		Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	Ethernet controller 0 100Mbit/sec link indicator, active low.
GBE0_LINK1000#	A5	OD CMOS	3.3V Suspend/3.3V		Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	Ethernet controller 0 1000Mbit/sec link indicator, active low.
GBE0_CTREF	A14	REF	GND min 3.3V max	NC	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap.

SATA Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
SATA0_TX+	A16	O SATA	AC coupled on Module	AC Coupling capacitor	Serial ATA or SAS Channel 0 transmit differential pair.	Serial ATA channel 0 Transmit output differential pair.
SATA0_TX-	A17	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA0_RX+	A19	I SATA	AC coupled on Module	AC Coupling capacitor	Serial ATA or SAS Channel 0 receive differential pair.	Serial ATA channel 0 Receive input differential pair.
SATA0_RX-	A20	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA1_TX+	B16	O SATA	AC coupled on Module	AC Coupling capacitor	Serial ATA or SAS Channel 1 transmit differential pair.	Serial ATA channel 1 Transmit output differential pair.
SATA1_TX-	B17	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA1_RX+	B19	I SATA	AC coupled on Module	AC Coupling capacitor	Serial ATA or SAS Channel 1 receive differential pair.	Serial ATA channel 1 Receive input differential pair.
SATA1_RX-	B20	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA2_TX+	A22	O SATA	AC coupled on Module	NA	Serial ATA or SAS Channel 2 transmit differential pair.	Serial ATA channel 2 Transmit output differential pair.
SATA2_TX-	A23	O SATA	AC coupled on Module	NA		
SATA2_RX+	A25	I SATA	AC coupled on Module	NA	Serial ATA or SAS Channel 2 receive differential pair.	Serial ATA channel 2 Receive input differential pair.
SATA2_RX-	A26	I SATA	AC coupled on Module	NA		
SATA3_TX+	B22	O SATA	AC coupled on Module	NA	Serial ATA or SAS Channel 3 transmit differential pair.	Serial ATA channel 3 Transmit output differential pair.
SATA3_TX-	B23	O SATA	AC coupled on Module	NA		
SATA3_RX+	B25	I SATA	AC coupled on Module	NA	Serial ATA or SAS Channel 3 receive differential pair.	Serial ATA channel 3 Receive input differential pair.
SATA3_RX-	B26	I SATA	AC coupled on Module	NA		
(S)ATA_ACT#	A28	I/O CMOS	3.3V / 3.3V	PU 10KW to 3.3V	ATA (parallel and serial) or SAS activity indicator, active low.	Serial ATA activity LED. Open collector output pin driven during SATA command activity.

PCI Express Lanes Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
PCIE_TX0+	A68	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Differential Transmit Pairs 0	PCIe channel 0. Transmit Output differential pair.
PCIE_TX0-	A69			AC Coupling capacitor		
PCIE_RX0+	B68	I PCIE	AC coupled off Module		PCI Express Differential Receive Pairs 0	PCIe channel 0. Receive Input differential pair.
PCIE_RX0-	B69					
PCIE_TX1+	A64	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Differential Transmit Pairs 1	PCIe channel 1. Transmit Output differential pair.
PCIE_TX1-	A65			AC Coupling capacitor		
PCIE_RX1+	B64	I PCIE	AC coupled off Module		PCI Express Differential Receive Pairs 1	PCIe channel 1. Receive Input differential pair.
PCIE_RX1-	B65					
PCIE_TX2+	A61	O PCIE	AC coupled on Module	AC Coupling capacitor (R1000 NA)	PCI Express Differential Transmit Pairs 2	PCIe channel 2. Transmit Output differential pair.
PCIE_TX2-	A62			AC Coupling capacitor (R1000 NA)		
PCIE_RX2+	B61	I PCIE	AC coupled off Module	(R1000 NA)	PCI Express Differential Receive Pairs 2	PCIe channel 2. Receive Input differential pair.
PCIE_RX2-	B62			(R1000 NA)		
PCIE_TX3+	A58	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Differential Transmit Pairs 3	PCIe channel 3. Transmit Output differential pair.
PCIE_TX3-	A59			AC Coupling capacitor		

PCIE_RX3+	B58	I PCIE	AC coupled off Module		PCI Express Differential Receive Pairs 3	PCIe channel 3. Receive Input differential pair.
PCIE_RX3-	B59					
PCIE_TX4+	A55	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Differential Transmit Pairs 4	PCIe channel 4. Transmit Output differential pair.
PCIE_TX4-	A56			AC Coupling capacitor		
PCIE_RX4+	B55	I PCIE	AC coupled off Module		PCI Express Differential Receive Pairs 4	PCIe channel 4. Receive Input differential pair.
PCIE_RX4-	B56					
PCIE_TX5+	A52	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Differential Transmit Pairs 5	PCIe channel 5. Transmit Output differential pair.
PCIE_TX5-	A53			AC Coupling capacitor		
PCIE_RX5+	B52	I PCIE	AC coupled off Module		PCI Express Differential Receive Pairs 5	PCIe channel 5. Receive Input differential pair.
PCIE_RX5-	B53					
PCIE_TX6+	D19	O PCIE	AC coupled on Module	AC Coupling capacitor (Option)	PCI Express Differential Transmit Pairs 6	PCIe channel 6. Transmit Output differential pair.
PCIE_TX6-	D20			AC Coupling capacitor (Option)		
PCIE_RX6+	C19	I PCIE	AC coupled off Module	(Option)	PCI Express Differential Receive Pairs 6	PCIe channel 6. Receive Input differential pair.
PCIE_RX6-	C20			(Option)		
PCIE_TX7+	D22	O PCIE	AC coupled on Module	NA	PCI Express Differential Transmit Pairs 7	PCIe channel 7. Transmit Output differential pair.
PCIE_TX7-	D23			NA		
PCIE_RX7+	C22	I PCIE	AC coupled off Module	NA	PCI Express Differential Receive Pairs 7	PCIe channel 7. Receive Input differential pair.
PCIE_RX7-	C23			NA		
PCIE_CLK_REF+	A88	O PCIE	PCIE		Reference clock output for all PCI Express and PCI Express Graphics lanes.	PCIe Reference Clock for all COM Express PCIe lanes, and for PEG lanes.
PCIE_CLK_REF-	A89					

PEG Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
PEG_TX0+	D52	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 0	PEG channel 0, Transmit Output differential pair.
PEG_TX0-	D53			AC Coupling capacitor		
PEG_RX0+	C52	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 0	PEG channel 0, Receive Input differential pair.
PEG_RX0-	C53					
PEG_TX1+	D55	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 1	PEG channel 1, Transmit Output differential pair.
PEG_TX1-	D56			AC Coupling capacitor		
PEG_RX1+	C55	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 1	PEG channel 1, Receive Input differential pair.
PEG_RX1-	C56					
PEG_TX2+	D58	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 2	PEG channel 2, Transmit Output differential pair.
PEG_TX2-	D59			AC Coupling capacitor		
PEG_RX2+	C58	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 2	PEG channel 2, Receive Input differential pair.
PEG_RX2-	C59					
PEG_TX3+	D61	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 3	PEG channel 3, Transmit Output differential pair.
PEG_TX3-	D62			AC Coupling capacitor		

PEG_RX3+	C61	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 3	PEG channel 3, Receive Input differential pair.
PEG_RX3-	C62					
PEG_TX4+	D65	O PCIE	AC coupled on Module	AC Coupling capacitor (R1000 NA)	PCI Express Graphics transmit differential pairs 4	PEG channel 4, Transmit Output differential pair.
PEG_TX4-	D66			AC Coupling capacitor (R1000 NA)		
PEG_RX4+	C65	I PCIE	AC coupled off Module	(R1000 NA)	PCI Express Graphics receive differential pairs 4	PEG channel 4, Receive Input differential pair.
PEG_RX4-	C66			(R1000 NA)		
PEG_TX5+	D68	O PCIE	AC coupled on Module	AC Coupling capacitor (R1000 NA)	PCI Express Graphics transmit differential pairs 5	PEG channel 5, Transmit Output differential pair.
PEG_TX5-	D69			AC Coupling capacitor (R1000 NA)		
PEG_RX5+	C68	I PCIE	AC coupled off Module	(R1000 NA)	PCI Express Graphics receive differential pairs 5	PEG channel 5, Receive Input differential pair.
PEG_RX5-	C69			(R1000 NA)		
PEG_TX6+	D71	O PCIE	AC coupled on Module	AC Coupling capacitor (R1000 NA)	PCI Express Graphics transmit differential pairs 6	PEG channel 6, Transmit Output differential pair.
PEG_TX6-	D72			AC Coupling capacitor (R1000 NA)		
PEG_RX6+	C71	I PCIE	AC coupled off Module	(R1000 NA)	PCI Express Graphics receive differential pairs 6	PEG channel 6, Receive Input differential pair.
PEG_RX6-	C72			(R1000 NA)		
PEG_TX7+	D74	O PCIE	AC coupled on Module	AC Coupling capacitor (R1000 NA)	PCI Express Graphics transmit differential pairs 7	PEG channel 7, Transmit Output differential pair.
PEG_TX7-	D75			AC Coupling capacitor (R1000 NA)		
PEG_RX7+	C74	I PCIE	AC coupled off Module	(R1000 NA)	PCI Express Graphics receive differential pairs 7	PEG channel 7, Receive Input differential pair.
PEG_RX7-	C75			(R1000 NA)		
PEG_TX8+	D78	O PCIE	AC coupled on Module	NA	PCI Express Graphics transmit differential pairs 8	PEG channel 8, Transmit Output differential pair.
PEG_TX8-	D79			NA		
PEG_RX8+	C78	I PCIE	AC coupled off Module	NA	PCI Express Graphics receive differential pairs 8	PEG channel 8, Receive Input differential pair.
PEG_RX8-	C79			NA		
PEG_TX9+	D81	O PCIE	AC coupled on Module	NA	PCI Express Graphics transmit differential pairs 9	PEG channel 9, Transmit Output differential pair.
PEG_TX9-	D82			NA		
PEG_RX9+	C81	I PCIE	AC coupled off Module	NA	PCI Express Graphics receive differential pairs 9	PEG channel 9, Receive Input differential pair.
PEG_RX9-	C82			NA		
PEG_TX10+	D85	O PCIE	AC coupled on Module	NA	PCI Express Graphics transmit differential pairs 10	PEG channel 10, Transmit Output differential pair.
PEG_TX10-	D86			NA		
PEG_RX10+	C85	I PCIE	AC coupled off Module	NA	PCI Express Graphics receive differential pairs 10	PEG channel 10, Receive Input differential pair.
PEG_RX10-	C86			NA		
PEG_TX11+	D88	O PCIE	AC coupled on Module	NA	PCI Express Graphics transmit differential pairs 11	PEG channel 11, Transmit Output differential pair.
PEG_TX11-	D89			NA		
PEG_RX11+	C88	I PCIE	AC coupled off Module	NA	PCI Express Graphics receive differential pairs 11	PEG channel 11, Receive Input differential pair.
PEG_RX11-	C89			NA		

PEG_TX12+	D91	O PCIE	AC coupled on Module	NA	PCI Express Graphics transmit differential pairs 12	PEG channel 12, Transmit Output differential pair.
PEG_TX12-	D92			NA		
PEG_RX12+	C91	I PCIE	AC coupled off Module	NA	PCI Express Graphics receive differential pairs 12	PEG channel 12, Receive Input differential pair.
PEG_RX12-	C92			NA		
PEG_TX13+	D94	O PCIE	AC coupled on Module	NA	PCI Express Graphics transmit differential pairs 13	PEG channel 13 Transmit Output differential pair.
PEG_TX13-	D95			NA		
PEG_RX13+	C94	I PCIE	AC coupled off Module	NA	PCI Express Graphics receive differential pairs 13	PEG channel 13, Receive Input differential pair.
PEG_RX13-	C95			NA		
PEG_TX14+	D98	O PCIE	AC coupled on Module	NA	PCI Express Graphics transmit differential pairs 14	PEG channel 14, Transmit Output differential pair.
PEG_TX14-	D99			NA		
PEG_RX14+	C98	I PCIE	AC coupled off Module	NA	PCI Express Graphics receive differential pairs 14	PEG channel 14, Receive Input differential pair.
PEG_RX14-	C99			NA		
PEG_TX15+	D101	O PCIE	AC coupled on Module	NA	PCI Express Graphics transmit differential pairs 15	PEG channel 15, Transmit Output differential pair.
PEG_TX15-	D102			NA		
PEG_RX15+	C101	I PCIE	AC coupled off Module	NA	PCI Express Graphics receive differential pairs 15	PEG channel 15, Receive Input differential pair.
PEG_RX15-	C102			NA		
PEG_LANE_RV#	D54	I CMOS	3.3V / 3.3V	PU 10KΩ to 3V3	PCI Express Graphics lane reversal input strap. Pull low on the Carrier board to reverse lane order.	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.

ExpressCard Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
GBE0_SDP	A49	I/O	3.3V Suspend/3.3V		Gigabit Ethernet Controller 0 Software-Definable Pin.	PCI ExpressCard0: PCI Express capable card request, active low, one per card
RSVD	A48			NC	Reserve pin	PCI ExpressCard0: reset, active low, one per card
USB0_HOST_PRSNT	B48	I CMOS	3.3V Suspend/ 3.3V	NC	Module USB client may detect the presence of a USB host on USB0	PCI ExpressCard1: PCI Express capable card request, active low, one per card
ESPI_EN#	B47	I CMOS	NA	NC	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus.	PCI ExpressCard1: reset, active low, one per card

USB Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
USB0+	A46	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 0	USB Port 0, data + or D+
USB0-	A45					USB Port 0, data - or D-
USB1+	B46	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 1	USB Port 1, data + or D+
USB1-	B45					USB Port 1, data - or D-
USB2+	A43	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 2	USB Port 2, data + or D+
USB2-	A42					USB Port 2, data - or D-
USB3+	B43	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 3	USB Port 3, data + or D+
USB3-	B42					USB Port 3, data - or D-

USB4+	A40	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 4	USB Port 4, data + or D+
USB4-	A39					USB Port 4, data - or D-
USB5+	B40	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 5	USB Port 5, data + or D+
USB5-	B39					USB Port 5, data - or D-
USB6+	A37	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 6	USB Port 6, data + or D+
USB6-	A36					USB Port 6, data - or D-
USB7+	B37	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 7. USB7 may be configured as a USB client or as a host, or both, at the Module designer's discretion. (CH960 default set as a host)	USB Port 7, data + or D+
USB7-	B36					USB Port 7, data - or D-
USB_0_1_OC#	B44	I CMOS	3.3V Suspend/3.3V	PU 10KW to 3.3V Suspend	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 0 and 1.
USB_2_3_OC#	A44	I CMOS	3.3V Suspend/3.3V	PU 10KW to 3.3V Suspend	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 2 and 3.
USB_4_5_OC#	B38	I CMOS	3.3V Suspend/3.3V	PU 10KW to 3.3V Suspend	USB over-current sense, USB channels 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 4 and 5.
USB_6_7_OC#	A38	I CMOS	3.3V Suspend/3.3V	PU 10KW to 3.3V Suspend	USB over-current sense, USB channels 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 6 and 7.
USB_SSTX0+	D4	O PCIE	AC coupled on Module	AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.	USB Port 0, SuperSpeed TX +
USB_SSTX0-	D3			AC Coupling capacitor		USB Port 0, SuperSpeed TX -
USB_SSRX0+	C4	I PCIE	AC coupled off Module		Additional receive signal differential pairs for the SuperSpeed USB data path.	USB Port 0, SuperSpeed RX +
USB_SSRX0-	C3					USB Port 0, SuperSpeed RX -
USB_SSTX1+	D7	O PCIE	AC coupled on Module	AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.	USB Port 1, SuperSpeed TX +
USB_SSTX1-	D6			AC Coupling capacitor		USB Port 1, SuperSpeed TX -
USB_SSRX1+	C7	I PCIE	AC coupled off Module		Additional receive signal differential pairs for the SuperSpeed USB data path.	USB Port 1, SuperSpeed RX +
USB_SSRX1-	C6					USB Port 1, SuperSpeed RX -
USB_SSTX2+	D10	O PCIE	AC coupled on Module	AC Coupling capacitor (USB3.1 Gen1)	Additional transmit signal differential pairs for the SuperSpeed USB data path.	USB Port 2, SuperSpeed TX +
USB_SSTX2-	D9			AC Coupling capacitor (USB3.1 Gen1)		USB Port 2, SuperSpeed TX -
USB_SSRX2+	C10	I PCIE	AC coupled off Module	(USB3.1 Gen1)	Additional receive signal differential pairs for the SuperSpeed USB data path.	USB Port 2, SuperSpeed RX +
USB_SSRX2-	C9			(USB3.1 Gen1)		USB Port 2, SuperSpeed RX -
USB_SSTX3+	D13	O PCIE	AC coupled on Module	NA	Additional transmit signal differential pairs for the SuperSpeed USB data path.	USB Port 3, SuperSpeed TX +
USB_SSTX3-	D12			NA		USB Port 3, SuperSpeed TX -
USB_SSRX3+	C13	I PCIE	AC coupled off Module	NA	Additional receive signal differential pairs for the SuperSpeed USB data path.	USB Port 3, SuperSpeed RX +
USB_SSRX3-	C12			NA		USB Port 3, SuperSpeed RX -

LVDS Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
LVDS_A0+/eDP_TX2+	A71	O LVDS	LVDS EDP: AC coupled off Module		LVDS Channel A differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board. eDP: eDP differential pairs	LVDS channel A differential signal pair 0 eDP lane 2, TX± differential signal pair
LVDS_A0-/eDP_TX2-	A72					
LVDS_A1+/eDP_TX1+	A73	O LVDS	LVDS EDP: AC coupled off Module			LVDS channel A differential signal pair 1 eDP lane 1, TX± differential signal pair
LVDS_A1-/eDP_TX1-	A74					
LVDS_A2+/eDP_TX0+	A75	O LVDS	LVDS EDP: AC coupled off Module			LVDS channel A differential signal pair 2 eDP lane 0, TX ± differential signal pair
LVDS_A2-/eDP_TX0-	A76					
LVDS_A3+	A78	O LVDS	LVDS EDP: AC coupled off Module			LVDS channel A differential signal pair 3
LVDS_A3-	A79					
LVDS_A_CK+/eDP_TX3+	A81	O LVDS	LVDS		LVDS Channel A differential clock	LVDS channel A differential clock pair eDP lane 3, TX± differential pair
LVDS_A_CK-/eDP_TX3-	A82					
LVDS_B0+	B71	O LVDS	LVDS		LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board.	LVDS channel B differential signal pair 0
LVDS_B0-	B72					
LVDS_B1+	B73	O LVDS	LVDS			LVDS channel B differential signal pair 1
LVDS_B1-	B74					
LVDS_B2+	B75	O LVDS	LVDS			LVDS channel B differential signal pair 2
LVDS_B2-	B76					
LVDS_B3+	B77	O LVDS	LVDS			LVDS channel B differential signal pair 3
LVDS_B3-	B78					
LVDS_B_CK+	B81	O LVDS	LVDS		LVDS Channel B differential clock	LVDS channel B differential clock pair
LVDS_B_CK-	B82					
LVDS_VDD_EN/eDP_VDD_EN	A77	O CMOS	3.3V / 3.3V	PD 100K	LVDS panel power enable	LVDS flat panel power enable. eDP power enable
LVDS_BKLT_EN/eDP_BKLT_EN	B79	O CMOS	3.3V / 3.3V	PD 100K	LVDS panel backlight enable	LVDS flat panel backlight enable high active signal eDP backlight enable
LVDS_BKLT_CTRL/eDP_BKLT_CTRL	B83	O CMOS	3.3V / 3.3V	PD 100K	LVDS panel backlight brightness control	LVDS flat panel backlight brightness control EDP backlight brightness control
LVDS_I2C_CK/eDP_AUX+	A83	I/O OD CMOS	3.3V / 3.3V	RSV PD 100K	I2C clock output for LVDS display use	DDC I2C clock signal used for flat panel detection and control. eDP auxiliary lane +
LVDS_I2C_DAT/eDP_AUX-	A84	I/O OD CMOS	3.3V / 3.3V	RSV PU 100K to 3V3	I2C data line for LVDS display use	DDC I2C data signal used for flat panel detection and control. eDP auxiliary lane -

RSVD/eDP_HPD	A87	I CMOS	3.3V / 3.3V	RSV series resistor to PCH EDP HPD	eDP_HPD:Detection of Hot Plug / Unplug and notification of the link layer	eDP_HPD: Detection of Hot Plug / Unplug and notification of the link layer

LPC Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
LPC_AD0 / ESPI_IO_0	B4	I/O CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V	Using as LPC function	LPC multiplexed address, command and data bus. ESPI Mode: eSPI Master Data Input / Outputs These are bi-directional input/output pins used to transfer data between master and slaves. Multiplexed with LPC_AD[0:3]	LPC multiplexed command, address and data.
LPC_AD1 /ESPI_IO_1	B5					
LPC_AD2 / ESPI_IO_2	B6					
LPC_AD3 / ESPI_IO_3	B7					
LPC_FRAME# / ESPI_CS0#	B3	O CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V	Using as LPC function	LPC frame indicates the start of an LPC cycle ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select0#. A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin.	LPC frame indicates start of a new cycle or termination of a broken cycle.
LPC_DRQ0# / ESPI_ALERT0#	B8	I CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V	PU 10K to 3.3V	LPC serial DMA request ESPI Mode: eSPI pins used by eSPI slave to request service from the eSPI master.	LPC encoded DMA/Bus master request.
LPC_DRQ1#	B9	I CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V	PU 10K to 3.3V, not support.		
LPC_SERIRQ / ESPI_CS1#	A50	I/O CMOS O CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V	PU 10K to 3.3V	LPC serial interrupt ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select# A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin.	LPC serialized IRQ.
LPC_CLK /ESPI_CK	B10	O CMOS	3.3V / 3.3V 1.8V Suspend / 1.8V	series 22Ω resistor	LPC clock output - 33MHz nominal ESPI Mode: eSPI Master Clock Output This pin provides the reference timing for all the serial input and output operations.	LPC clock output 33MHz.

SPI Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
SPI_CS#	B97	O CMOS	3.3V Suspend/3.3V		Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1	Chip select for Carrier Board SPI – may be sourced from chipset SPI0 or SPI1
SPI_MISO	A92	I CMOS	3.3V Suspend/3.3V		Data in to Module from Carrier SPI	Data in to Module from Carrier SPI
SPI_MOSI	A95	O CMOS	3.3V Suspend/3.3V		Data out from Module to Carrier SPI	Data out from Module to Carrier SPI
SPI_CLK	A94	O CMOS	3.3V Suspend/3.3V		Clock from Module to Carrier SPI	Clock from Module to Carrier SPI
SPI_POWER	A91	O	3.3V Suspend/3.3V		Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier Board.	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier.

BIOS_DIS0# / ESPI_SAFS	A34	I CMOS	NA	PU 10KΩ to 3V3 Suspend.	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to COM Express Module Base Specification Revision 2.1 for strapping options of BIOS disable signals.	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to for strapping options of BIOS disable signals.
BIOS_DIS1#	B88			PU 10KΩ to 3V3 Suspend.		Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low.

VGA Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
VGA_RED	B89	O Analog	Analog	PD 150W to GND	Red for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.	Red component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.
VGA_GRN	B91	O Analog	Analog	PD 150W to GND	Green for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.	Green component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.
VGA_BLU	B92	O Analog	Analog	PD 150W to GND	Blue for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.	Blue component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.
VGA_HSYNC	B93	O CMOS	3.3V / 3.3V		Horizontal sync output to VGA monitor	Horizontal sync output to VGA monitor.
VGA_VSYNC	B94	O CMOS	3.3V / 3.3V		Vertical sync output to VGA monitor	Vertical sync output to VGA monitor.
VGA_I2C_CK	B95	I/O OD CMOS	3.3V / 3.3V	PU 2.2KW to 3.3V	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)	DDC clock line (I2C port dedicated to identify VGA monitor capabilities).
VGA_I2C_DAT	B96	I/O OD CMOS	3.3V / 3.3V	PU 2.2KW to 3.3V	DDC data line.	DDC data line.

DDI Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
DDI1_PAIR0+	D26	O PCIE	AC coupled off Module		DDI for Display Port: DP1_LANE 0 differential pairs DDI for SDVO: SDVO1_RED± differential pair (Serial Digital Video red output) DDI for HDMI/DVI: TMDS1_DATA lanes 2 differential pairs	DP1_LANE0+ for DP / TMDS1_DATA2+ for HDMI or DVI
DDI1_PAIR0-	D27					DP1_LANE0- for DP / TMDS1_DATA2- for HDMI or DVI
DDI1_PAIR1+	D29	O PCIE	AC coupled off Module		DDI for Display Port: DP1_LANE 1 differential pairs DDI for SDVO: SDVO1_GRN± differential pair (Serial Digital Video green output) DDI for HDMI/DVI: TMDS1_DATA lanes 1 differential pairs	DP1_LANE1+ for DP / TMDS1_DATA1+ for HDMI or DVI
DDI1_PAIR1-	D30					DP1_LANE1- for DP / TMDS1_DATA1- for HDMI or DVI
DDI1_PAIR2+	D32	O PCIE	AC coupled off Module		DDI for Display Port: DP1_LANE 2 differential pairs DDI for SDVO: SDVO1_BLU± differential pair (Serial Digital Video blue output) DDI for HDMI/DVI: TMDS1_DATA lanes 0 differential pairs	DP1_LANE2+ for DP / TMDS1_DATA0+ for HDMI or DVI
DDI1_PAIR2-	D33					DP1_LANE2- for DP / TMDS1_DATA0- for HDMI or DVI
DDI1_PAIR3+	D36	O PCIE	AC coupled off Module		DDI for Display Port: DP1_LANE 3 differential pairs DDI for SDVO: SDVO1_CK± differential pair (Serial Digital Video clock output) DDI for HDMI/DVI: TMDS1_CLK differential pairs	DP1_LANE3+ for DP / TMDS1_CLK+
DDI1_PAIR3-	D37					DP1_LANE3- for DP / TMDS1_CLK-
DDI1_PAIR4+	C25	I PCIE	AC coupled off Module	NA,no spport	DDI for SDVO: SDVO1_INT± differential pair (Serial Digital Video B interrupt input differential pair)	NA
DDI1_PAIR4-	C26			NA,no spport		NA
DDI1_PAIR5+	C29	I PCIE	AC coupled off Module	NA,no spport	DDI for SDVO: SDVO1_TVCLKIN± differential pair (Serial Digital Video TVOUT synchronization clock input differential pair.)	NA
DDI1_PAIR5-	C30			NA,no spport		NA
DDI1_PAIR6+	C15	I PCIE	AC coupled off Module	NA,no spport	DDI for SDVO: SDVO1_FLDSTALL± differential pair (Serial Digital Video Field Stall input differential pair.)	NA
DDI1_PAIR6-	C16			NA,no spport		NA

DDI1_CTRLCLK_AUX+	D15	I/O PCIE	AC coupled on Module	PD 100K to GND	DDI for Display Port: DP1_AUX+ Differetial pairs (DP AUX+ function if DDI1_DDC_AUX_SEL is no connect) Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	DP1_AUX+ for DP
		I/O OD CMOS	3.3V / 3.3V	NA	DDI for SDVO: SDVO1_CTRLCLK (SDVO I2C clock line - to set up SDVO peripherals.) DDI for HDMI/DVI: HDMI1_CTRLCLK (HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high)	HDMI1_CTRLCLK for HDMI or DVI
DDI1_CTRLCLK_AUX-	D16	I/O PCIE	AC coupled on Module	PU 100K to 3.3V	DDI for Display Port: DP1_AUX- Differetial pairs (DP AUX- function if DDI1_DDC_AUX_SEL is no connect) Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	DP1_AUX- for DP
		I/O OD CMOS	3.3V / 3.3V	NA	DDI for SDVO: SDVO1_CTRLDATA (SDVO I2C data line - to set up SDVO peripherals.) DDI for HDMI/DVI: HDMI1_CTRLDATA (HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high)	HDMI1_CTRLDATA for HDMI or DVI
DDI1_HPD	C24	I CMOS	3.3V / 3.3V	PD 100K to GND	DDI for Display Port: DP1_HPD (DP Hot-Plug Detect) DDI for HDMI/DVI: HDMI1_HPD (HDMI Hot-Plug Detect)	DP1_HPD for DP / HDMI1_HPD for HDMI or DVI
DDI1_DDC_AUX_SEL	D34	I CMOS	3.3V / 3.3V	PD 1M to GND	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	Selects the function of DP1 AUX±(Low) or HDMI1 DDC CLK/DATA(High) The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode. When HDMI/DVI is directly done on the Carrier Board, this pin shall be pulled to 3.3V with a 100k Ohm resistor to configure the AUX pairs as DDC channels.
DDI2_PAIR0+	D39	O PCIE	AC coupled off Module		DDI for Display Port: DP2_LANE 0 differential pairs DDI for HDMI/DVI: TMDS2_DATA lanes 2 differential pairs	DP2_LANE0+ for DP / TMDS2_DATA2+ for HDMI or DVI
DDI2_PAIR0-	D40					DP2_LANE0- for DP / TMDS2_DATA2- for HDMI or DVI
DDI2_PAIR1+	D42	O PCIE	AC coupled off Module		DDI for Display Port: DP2_LANE 1 differential pairs DDI for HDMI/DVI: TMDS2_DATA lanes 1 differential pairs	DP2_LANE1+ for DP / TMDS2_DATA1+ for HDMI or DVI
DDI2_PAIR1-	D43					DP2_LANE1- for DP / TMDS2_DATA1- for HDMI or DVI
DDI2_PAIR2+	D46	O PCIE	AC coupled off Module		DDI for Display Port: DP2_LANE 2 differential pairs DDI for HDMI/DVI: TMDS2_DATA lanes 0 differential pairs	DP2_LANE2+ for DP / TMDS2_DATA0+ for HDMI or DVI
DDI2_PAIR2-	D47					DP2_LANE2- for DP / TMDS2_DATA0- for HDMI or DVI
DDI2_PAIR3+	D49	O PCIE	AC coupled off Module		DDI for Display Port: DP2_LANE 3 differential pairs DDI for HDMI/DVI: TMDS2_CLK differential pairs	DP2_LANE3+ for DP / TMDS2_CLK+
DDI2_PAIR3-	D50					DP2_LANE3- for DP / TMDS2_CLK-
DDI2_CTRLCLK_AUX+	C32	I/O PCIE	AC coupled on Module	PD 100K to GND	DDI for Display Port: DP2_AUX+ Differetial pairs (DP AUX+ function if DDI2_DDC_AUX_SEL is no connect) Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	DP2_AUX+ for DP
		I/O OD CMOS	3.3V / 3.3V	NA	DDI for HDMI/DVI: HDMI2_CTRLCLK (HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high)	HDMI2_CTRLCLK for HDMI or DVI
DDI2_CTRLCLK_AUX-	C33	I/O PCIE	AC coupled on Module	PU 100K to 3.3V	DDI for Display Port: DP2_AUX- Differetial pairs (DP AUX- function if DDI2_DDC_AUX_SEL is no connect) Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	DP2_AUX- for DP
		I/O OD CMOS	3.3V / 3.3V	NA	DDI for HDMI/DVI: HDMI2_CTRLDATA (HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high)	HDMI2_CTRLDATA for HDMI or DVI
DDI2_HPD	D44	I CMOS	3.3V / 3.3V	PD 100K to GND	DDI for Display Port: DP2_HPD (DP Hot-Plug Detect) DDI for HDMI/DVI: HDMI2_HPD (HDMI Hot-Plug Detect)	DP2_HPD for DP / HDMI1_HPD for HDMI or DVI

DDI2_DDC_AUX_SEL	C34	I CMOS	3.3V / 3.3V	PD 1M to GND	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	Selects the function of DP2 AUX±(Low) or HDMI2 DDC CLK/ DATA(High) The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode. When HDMI/DVI is directly done on the Carrier Board, this pin shall be pulled to 3.3V with a 100k Ohm resistor to configure the AUX pairs as DDC channels.
DDI3_PAIR0+	C39	O PCIE	AC coupled off Module	(Optional)	DDI for Display Port: DP3_LANE 0 differential pairs DDI for HDMI/DVI: TMDS3_DATA lanes 2 differential pairs	DP3_LANE0+ for DP / TMDS3_DATA2+ for HDMI or DVI
DDI3_PAIR0-	C40			(Optional)		DP3_LANE0- for DP / TMDS3_DATA2- for HDMI or DVI
DDI3_PAIR1+	C42	O PCIE	AC coupled off Module	(Optional)	DDI for Display Port: DP3_LANE 1 differential pairs DDI for HDMI/DVI: TMDS3_DATA lanes 1 differential pairs	DP3_LANE1+ for DP / TMDS3_DATA1+ for HDMI or DVI
DDI3_PAIR1-	C43			(Optional)		DP3_LANE1- for DP / TMDS3_DATA1- for HDMI or DVI
DDI3_PAIR2+	C46	O PCIE	AC coupled off Module	(Optional)	DDI for Display Port: DP3_LANE 2 differential pairs DDI for HDMI/DVI: TMDS3_DATA lanes 0 differential pairs	DP3_LANE2+ for DP / TMDS3_DATA0+ for HDMI or DVI
DDI3_PAIR2-	C47			(Optional)		DP3_LANE2- for DP / TMDS3_DATA0- for HDMI or DVI
DDI3_PAIR3+	C49	O PCIE	AC coupled off Module	(Optional)	DDI for Display Port: DP3_LANE 3 differential pairs DDI for HDMI/DVI: TMDS3_CLK differential pairs	DP3_LANE3+ for DP / TMDS3_CLK+
DDI3_PAIR3-	C50			(Optional)		DP3_LANE3- for DP / TMDS3_CLK-
DDI3_CTRLCLK_AUX+	C36	I/O PCIE	AC coupled on Module	PD 100K to GND (Optional)	DDI for Display Port: DP3_AUX+ Differetial pairs (DP AUX+ function if DDI3_DDC_AUX_SEL is no connect) Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	DP3_AUX+ for DP
		I/O OD CMOS	3.3V / 3.3V	NA	DDI for HDMI/DVI: HDMI3_CTRLCLK (HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high)	HDMI3_CTRLCLK for HDMI or DVI
DDI3_CTRLCLK_AUX-	C37	I/O PCIE	AC coupled on Module	PU 100K to 3.3V (Optional)	DDI for Display Port: DP3_AUX- Differetial pairs (DP AUX- function if DDI3_DDC_AUX_SEL is no connect)	DP3_AUX- for DP
		I/O OD CMOS	3.3V / 3.3V	NA	DDI for HDMI/DVI: HDMI3_CTRLDATA (HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high)	HDMI3_CTRLDATA for HDMI or DVI
DDI3_HPD	C44	I CMOS	3.3V / 3.3V	PD 100K to GND (Optional)	DDI for Display Port: DP3_HPD (DP Hot-Plug Detect) DDI for HDMI/DVI: HDMI3_HPD (HDMI Hot-Plug Detect)	DP3_HPD for DP / HDMI1_HPD for HDMI or DVI
DDI3_DDC_AUX_SEL	C38	I CMOS	3.3V / 3.3V	PD 1MΩ to GND (Optional)	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	Selects the function of DP3 AUX±(Low) or HDMI3 DDC CLK/ DATA(High) The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode. When HDMI/DVI is directly done on the Carrier Board, this pin shall be pulled to 3.3V with a 100k Ohm resistor to configure the AUX pairs as DDC channels.

Serial Interface Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
SER0_TX	A98	O CMOS	5V/12V		General purpose serial port 0 transmitter	Transmit Line for Serial Port 0 ; PD 4.7KΩ
SER0_RX	A99	I CMOS	5V/12V	PU 10KΩ to 3.3V	General purpose serial port 0 receiver	Receive Line for Serial Port 0
SER1_TX	A101	O CMOS	5V/12V		General purpose serial port 1 transmitter	Transmit Line for Serial Port 1 ; PD 4.7KΩ
SER1_RX	A102	I CMOS	5V/12V	PU 10KΩ to 3.3V	General purpose serial port 1 receiver	Receive Line for Serial Port 1

I2C Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description

I2C_CK	B33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3.3V Suspend	General purpose I2C port clock output	General Purpose I2C Clock output
I2C_DAT	B34	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3.3V Suspend	General purpose I2C port data I/O line	General Purpose I2C data I/O line.

Miscellaneous Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
SPKR	B32	O CMOS	3.3V / 3.3V		Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.	Output used to control an external FET or a logic gate to drive an external PC speaker.
WDT	B27	O CMOS	3.3V / 3.3V	PD 10KΩ to GND.	Output indicating that a watchdog time-out event has occurred.	Output indicating that a watchdog time-out event has occurred.
FAN_PWMOUT	B101	O CMOS	3.3V / 12V		Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.
FAN_TACHIN	B102	I OD CMOS	3.3V / 12V		Fan tachometer input for a fan with a two pulse output.	Fan tachometer input for a fan with a two pulse output.
TPM_PP	A96	I CMOS	3.3V / 3.3V	RSV PD 4.7KΩ to GND.	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. Thissignal is used to indicate Physical Presence to the TPM.

Power and System Management Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
PWRBTN#	B12	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.	Power button low active signal used to wake up the system from S5 state (soft off). This signal is triggered on the falling edge.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.
CB_RESET#	B50	O CMOS	3.3V Suspend/3.3V	PD 100KΩ to GND	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software.	Reset output signal from Module to Carrier Board. This signal may be driven low by the Module to reset external components located on the Carrier Board.
PWR_OK	B24	I CMOS	3.3V / 3.3V	PU 10KΩ to 3.3V and PD 20K to GND	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.	Power OK status signal generated by the ATX power supply to notify the Module that the DC operating voltages are within the ranges required for proper operation.
SUS_STAT#	B18	O CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3V3	Indicates imminent suspend operation; used to notify LPC devices.	Suspend status signal to indicate that the system will be entering a low power state soon. It can be used by other peripherals on the Carrier Board as an indication that they should go into power-down mode.
SUS_S3#	A15	O CMOS	3.3V Suspend/3.3V	PD 10KΩ to GND	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.	S3 Sleep control signal indicating that the system resides in S3 state (Suspend to RAM).
SUS_S4#	A18	O CMOS	3.3V Suspend/3.3V	PD 10KΩ to GND	Indicates system is in Suspend to Disk state. Active low output.	S4 Sleep control signal indicating that the system resides in S4 state (Suspend to Disk).

SUS_S5#	A24	O CMOS	3.3V Suspend/3.3V	PD 10KΩ to GND	Indicates system is in Soft Off state.	S5 Sleep Control signal indicating that the system resides in S5 State (Soft Off).
WAKE0#	B66	I CMOS	3.3V Suspend/3.3V	PU 10K to 3.3V Suspend	PCI Express wake up signal.	PCI Express wake-up event signal.
WAKE1#	B67	I CMOS	3.3V Suspend/3.3V	PU 10K to 3.3V Suspend	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.	General purpose wake-up signal.
BATLOW#	A27	I CMOS	3.3V Suspend/ 3.3V	PU 10KΩ to 3.3V Suspend	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low. It also can be used to signal some other external power management event.
LID#	A103	I OD CMOS	3.3V Suspend/12V	PU 47KΩ to 3.3V Suspend	LID switch. Low active signal used by the ACPI operating system for a LID switch.	LID switch. Low active signal used by the ACPI operating system for a LID switch.
SLEEP#	B103	I OD CMOS	3.3V Suspend/12V	PU 47KΩ to 3.3V Suspend	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.
RAPID_ SHUTDOWN	C67	I CMOS	5.0V Suspend/ 5.0V	PD 100KΩ to GND	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs.	NA

Thermal Protection Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
THRM#	B35	I CMOS	3.3V / 3.3V	PU 10KΩ to 3.3V	Input from off-Module temp sensor indicating an over-temp situation.	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.
THRMTRIP#	A35	O CMOS	3.3V / 3.3V	PU 1KΩ to 3.3V	Active low output indicating that the CPU has entered thermal shutdown.	Thermal Trip indicates an overheating condition of the processor. If 'THRMTRIP#' goes active the system immediately transitions to the S5 State (Soft Off).

SMBUS Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
SMB_CK	B13	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	System Management Bus bidirectional clock line.	System Management Bus bidirectional clock line
SMB_DAT	B14	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	System Management Bus bidirectional data line.	System Management bidirectional data line.
SMB_ALERT#	B15	I CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	System Management Bus Alert

GPIO Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
GPO0	A93	O CMOS	3.3V / 3.3V	RSV PU 47K to 3V3/ 3.3V Suspend	General purpose output pins. Upon a hardware reset, these outputs should be low.	General Purpose Outputs for system specific usage.
GPO1	B54					
GPO2	B57					
GPO3	B63					

GPI0	A54	I CMOS	3.3V / 3.3V	PU 100KΩ to 3.3V	General purpose input pins. Pulled high internally on the Module.	General Purpose Input for system specific usage. The signals are pulled up by the Module.
GPI1	A63					
GPI2	A67					
GPI3	A85					

Power and GND Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
VCC_12V	A104~A109 B104~B109 C104~C109 D104~D109	Power			Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	
VCC_5V_SBY	B84~B87	Power			Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	
VCC_RTC	A47	Power			Real-time clock circuit-power input. Nominally +3.0V.	
GND	Pin Type = Power. Pin#: A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110, C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41,D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110				Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	

Module type Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	GH960 PU/PD	Module Base Specification R3.0 Description	COM Express Carrier Design Guide R2.0 Description
TYPE0#	C54	PDS		N.C.	TYPE2# TYPE1# TYPE0# X X X pin out Type 1 NC NC NC pin out Type 2 NC NC GND pin out Type 3 (no IDE) NC GND NC pin out Type 4 (no PCI) NC GND GND pin out Type 5 (no IDE, no PCI) GND NC NC pin out Type 6 (no IDE, no PCI)	The Type pins indicate the COM Express pin-out type of the Module. To indicate the Module's pin-out type, the pins are either not connected or strapped to ground on the Module. The Carrier Board has to implement additional logic, which prevents the system to switch power on, if a Module with an incompatible pin-out type is detected.
TYPE1#	C57	PDS		N.C.		
TYPE2#	D57	PDS		PD 0Ω to GND		
TYPE10#	A97	PDS		N.C.	Dual use pin. Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier that a Rev 1.0/2.0 Module is installed TYPE10# NC Pin-out R2.0 PD Pin-out Type 10 pull down to ground with 47K resistor 12V Pin-out R1.0 This pin is reclaimed from the VCC_12V pool. In R1.0 Modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no connect for types 1-6. A Carrier can detect a R1.0 Module by the presence of 12V on this pin. R2.0 Module types 1-6 will no connect this pin. Type 10 Modules shall pull this pin to ground through a 47K resistor.	Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier Board, that a Rev 1.0/2.0 Module is installed. TYPE10# NC Pin-out R2.0 PD Pin-out Type 10 pull down to ground with 47k 12V Pin-out R1.0

Chapter 3 - BIOS Settings

▶ Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.
It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

Note:
The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration
Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility
The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.
The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message “Press DEL to run setup” will appear on the screen. If the message disappears before you respond, restart the system or press the “Reset” button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

Legends

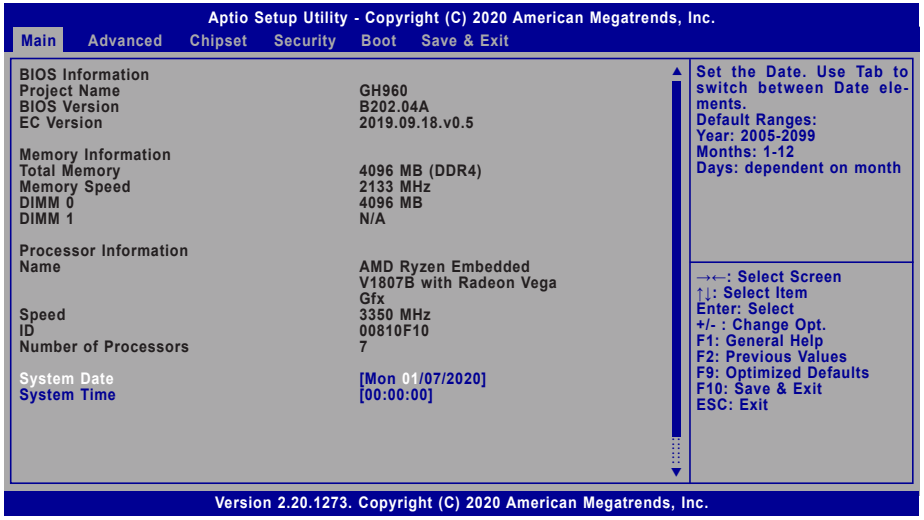
Keys	Function
Right / Left arrow	Move the highlight left or right to select a menu
Up / Down arrow	Move the highlight up or down between submenus or fields
<Enter>	Enter the highlighted submenu
+ (plus key)/F6	Scroll forward through the values or options of the highlighted field
- (minus key)/F5	Scroll backward through the values or options of the highlighted field
<F1>	Display general help
<F2>	Display previous values
<F9>	Optimized defaults
<F10>	Save and Exit
<Esc>	Return to previous menu

Scroll Bar
When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu
When “▶” appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

▶ Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility. Basic hardware information is displayed.



System Date

The date format is <month>, <date>, <year>. Press "Tab" to switch to the next field and press "-" or "+" to modify the value.

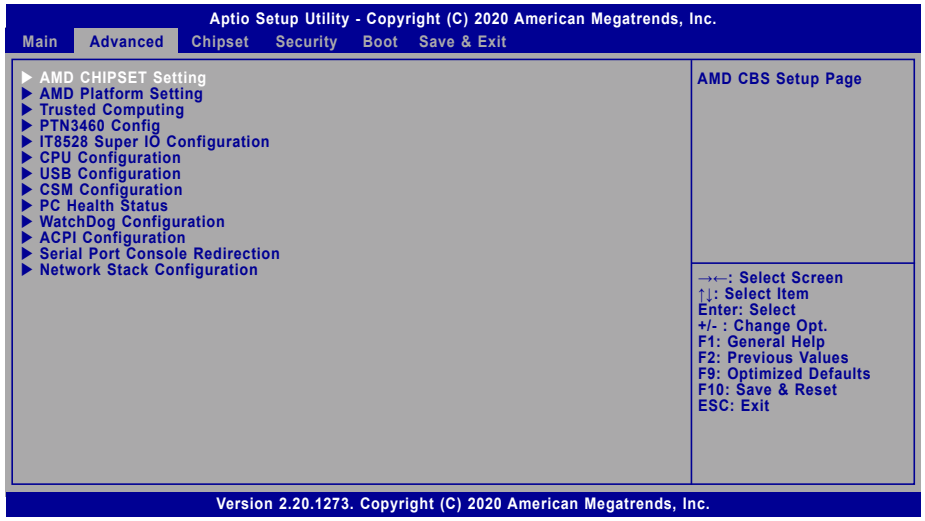
System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

▶ Advanced

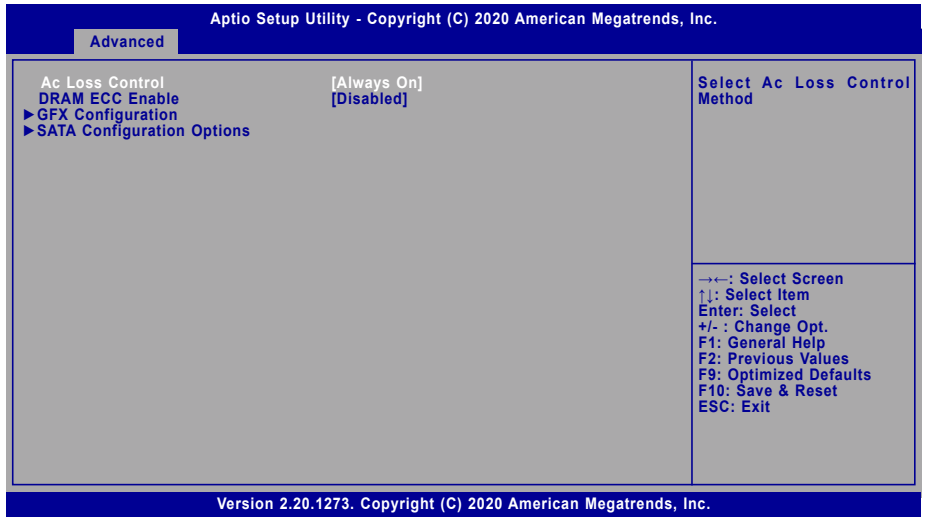
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Important:
Setting incorrect field values may cause the system to malfunction.



▶ Advanced

AMD CHIPSET Setting



Ac Loss Control

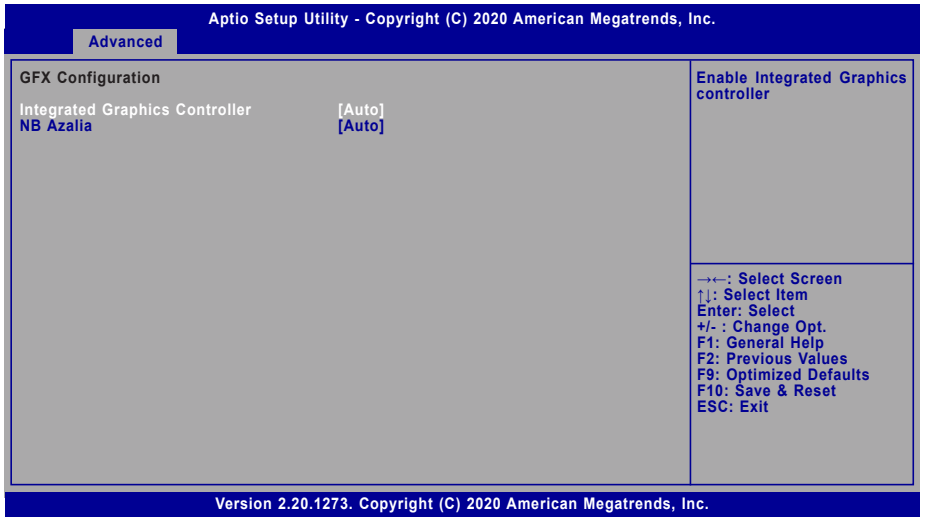
Select among Always On, Always Off, and Last State. This field is used to specify what state the system is set to return to when power is re-applied after AC power failure or loss (G3 state).

Always On	The system automatically powers on after power failure.
Always Off	The system enters soft-off state after power failure. Power-on signal input is required to power up the system.
Last State	The system returns to the last state right before power failure.

DRAM ECC Enable

Enable or disable (Error-correcting code) ECC function of the memory.

► GFX Configuration



Integrated Graphics Controller

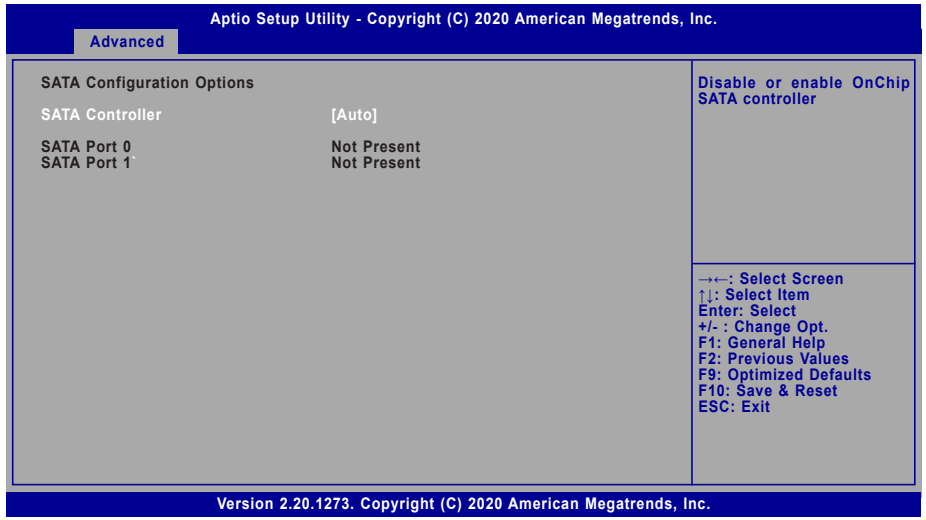
Enable or disable the integrated graphics controller, or select Auto for auto-detection.

NB Azalia

Enable or disable the integrated HD Audio controller, or select Auto for auto-detection.

▶ Advanced ▶ AMD CHIPSET Setting

▶ SATA Configuration Options



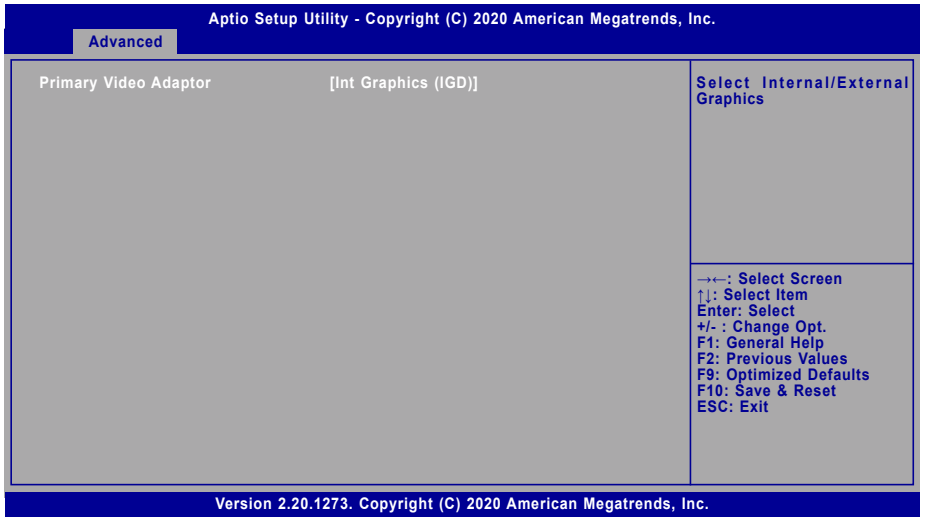
SATA Controller

Enable or disable the SATA controller, or select Auto for auto-detection.

The information of the SATA devices installed on the system is shown.

▶ Advanced

AMD Platform Setting

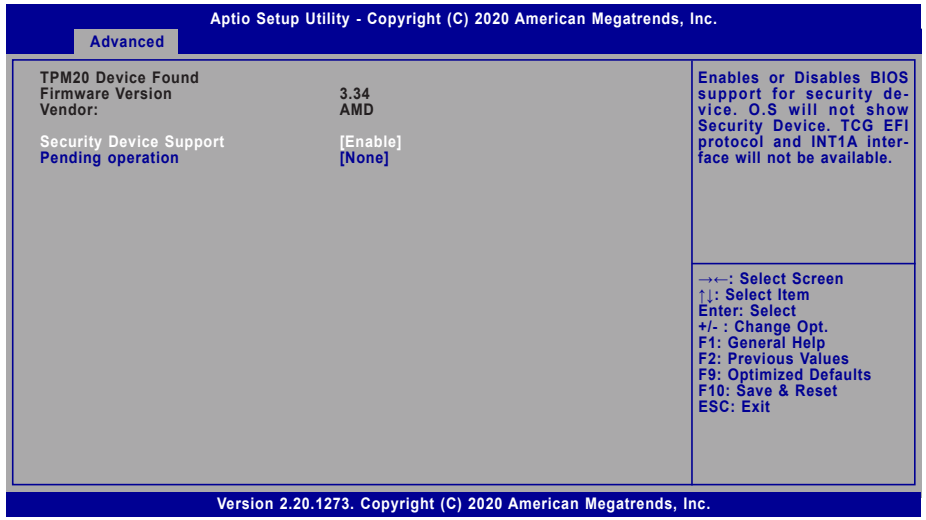


Primary Video Adaptor

Select which graphics controller will be the primary video adaptor — Int Graphics (IGD) or Ext Graphics (PEG).

▶ Advanced

Trusted Computing



Security Device Support

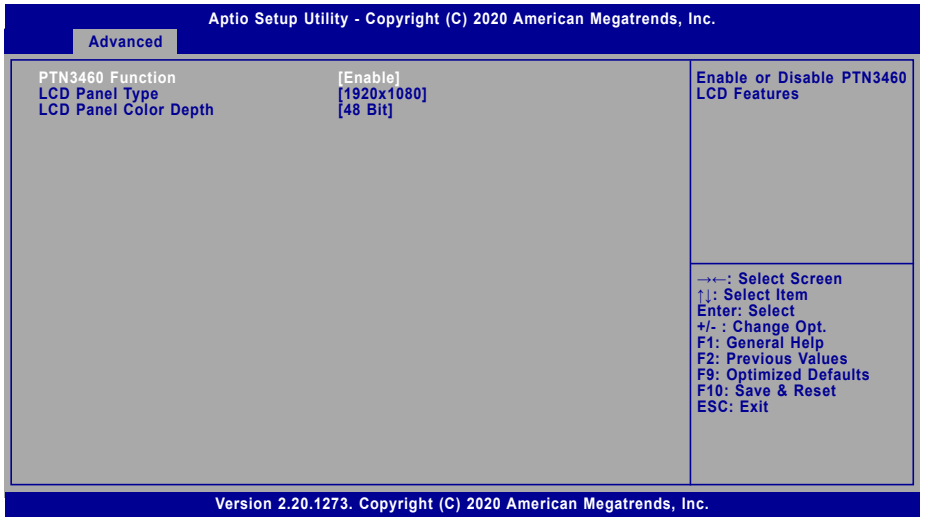
This field is used to enable or disable BIOS support for the security device such as an TPM 2.0 to achieve hardware-level security via cryptographic keys.

Pending operation

To clear the existing TPM encryption, select "TPM Clear" and restart the system. This field is not available when "Security Device Support" is disabled.

▶ Advanced

PTN3460 Config



PTN3460 Function

Enable or Disable PTN3460 LCD Features. When this field is disabled, the following fields will remain hidden.

LCD Panel Type

Select the resolution of the LCD Panel — 800X480, 800X600, 1024X768, 1366X768, 1280X1024, 1920X1080, or 1920X1200.

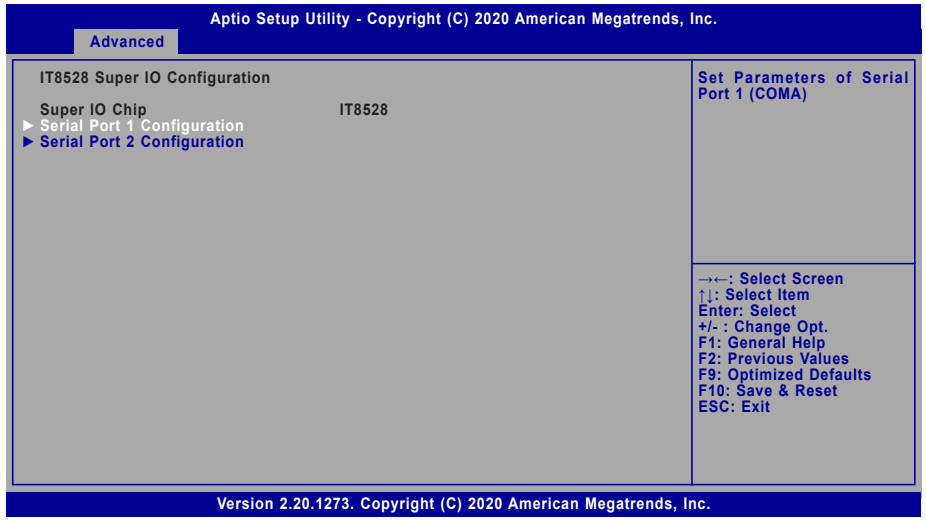
LCD Panel Color Depth

Select the color depth of the LCD Panel — 18 Bit, 24 Bit, 36 Bit, 48 Bit.

Note:
The configuration must match the specifications of your LCD Panel in order for the LCD Panel to display properly.

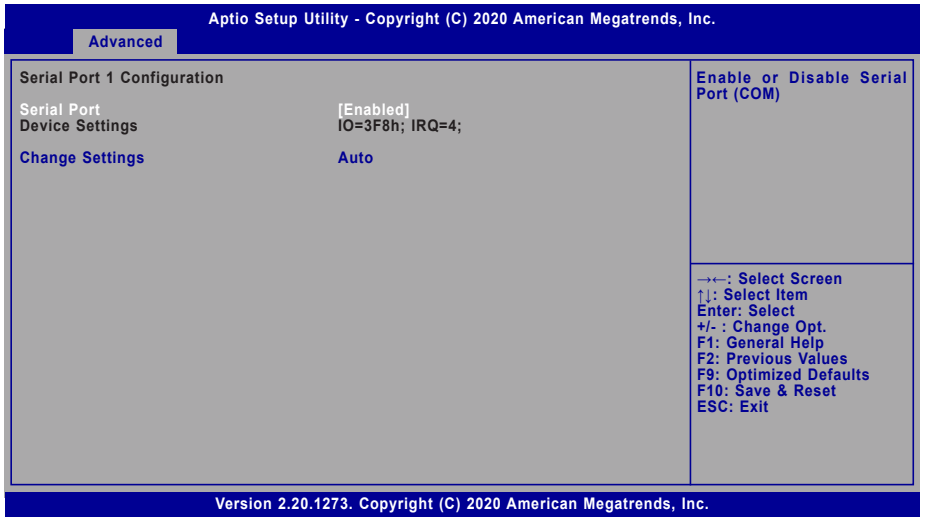
▶ Advanced

IT8528 Super IO Configuration



The Super IO Chip information is displayed. Select a submenu for more settings.

▶ Serial Port 1/2 Configuration



Serial Port

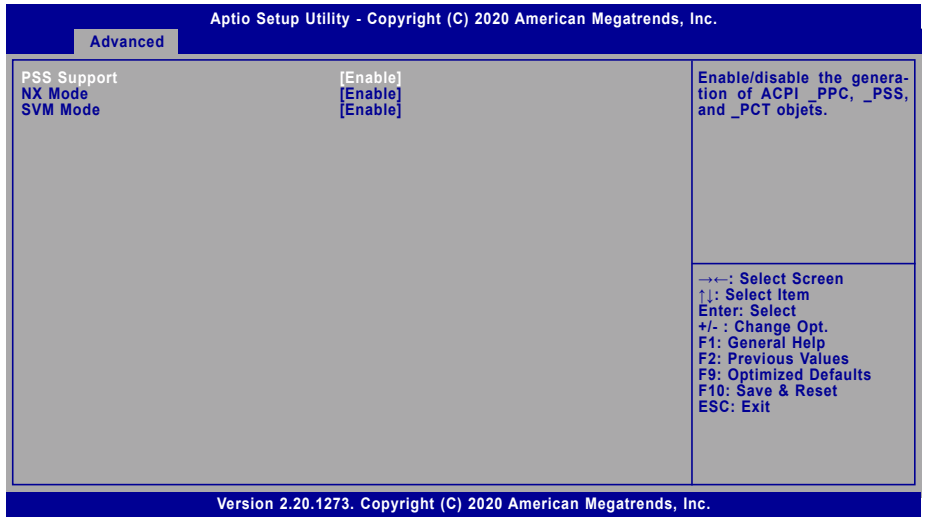
Enable or disable the current serial COM port.

Change Settings

Select an I/O Address and IRQ for the current serial Port, or select Auto to assign automatically.

▶ Advanced

CPU Configuration



PSS Support

Enable or disable the power, performance, and speed related ACPI functions of the CPU.

NX Mode

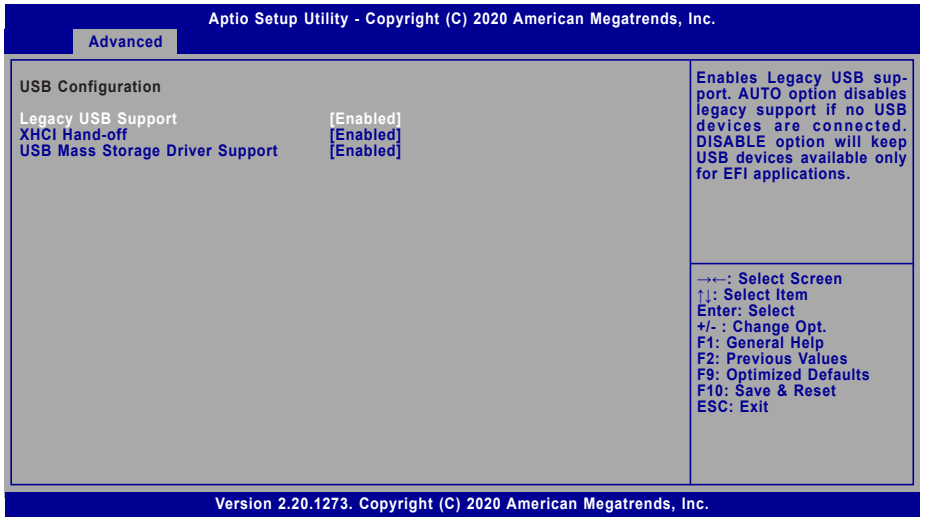
Enable or disable the protection function that keeps no-execute codes from being executed by the CPU.

SVM Mode

Enable or disable Secure Virtual Machine (SVM) for CPU virtualization.

▶ Advanced

USB Configuration



Legacy USB Support

Enabled	Enable Legacy USB support.
Disabled	Keep USB devices available only for EFI applications.
Auto	Disable Legacy support if no USB devices are connected.

XHCI Hand-off

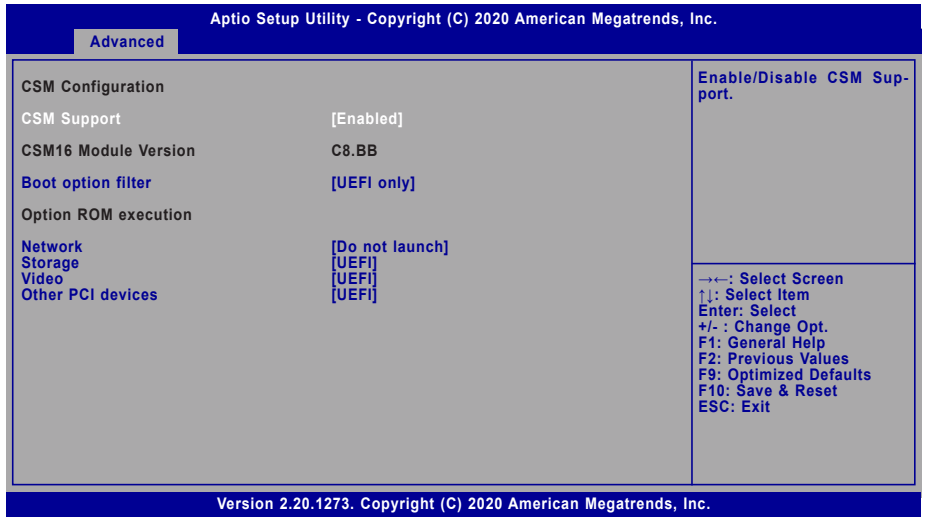
Enable or disable XHCI Hand-off.

USB Mass Storage Driver Support

Enable or disable USB Mass Storage Driver Support.

▶ Advanced

CSM Configuration



CSM Support

This section is used to enable or disable CSM Support. The following fields are only available when "CSM Support" is enabled.

Boot option filter

This field controls Legacy/UEFI ROMs priority — UEFI and Legacy, Legacy only, UEFI only.

Network

This field controls the execution of UEFI and Legacy Network OpROM.

Storage

This field controls the execution of UEFI and Legacy Storage OpROM.

Video

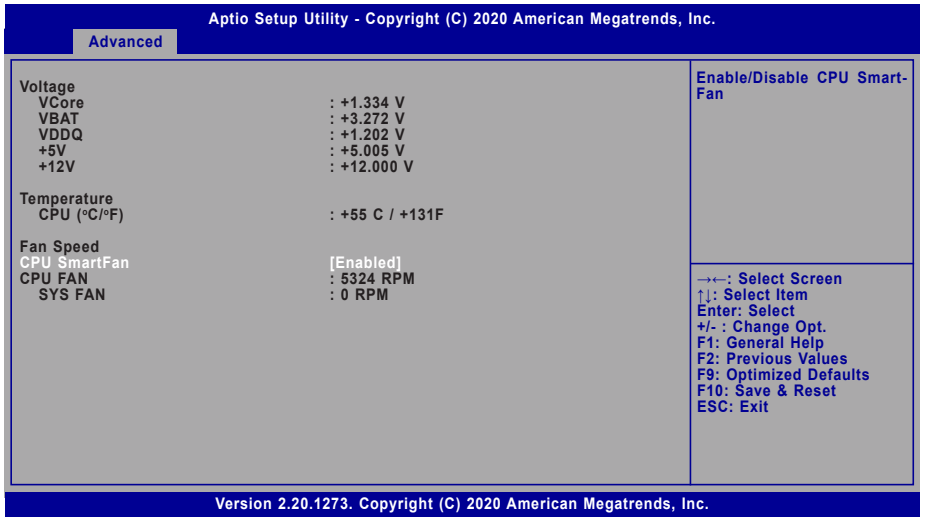
This field controls the execution of UEFI and Legacy Video OpROM.

Other PCI devices

This field determines OpROM execution policy for devices other than Network, Storage or Video.

▶ Advanced

PC Health Status



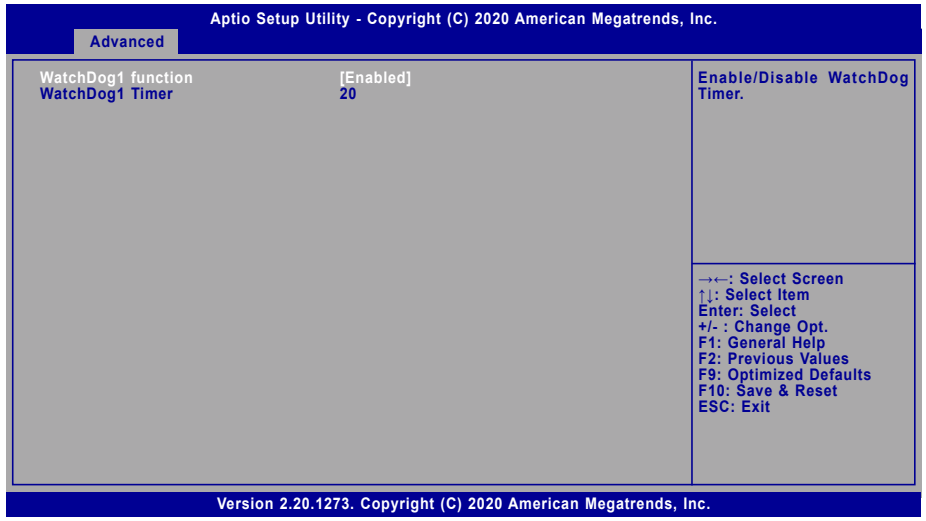
This section displays the system's health information, i.e. voltage readings, CPU and system temperatures, and fan speed readings.

CPU SmartFan

Enable or disable CPU Smart Fan. Once enabled, the fan speed will be moderated according to the current CPU temperature.

▶ Advanced

WatchDog Configuration



WatchDog1 function

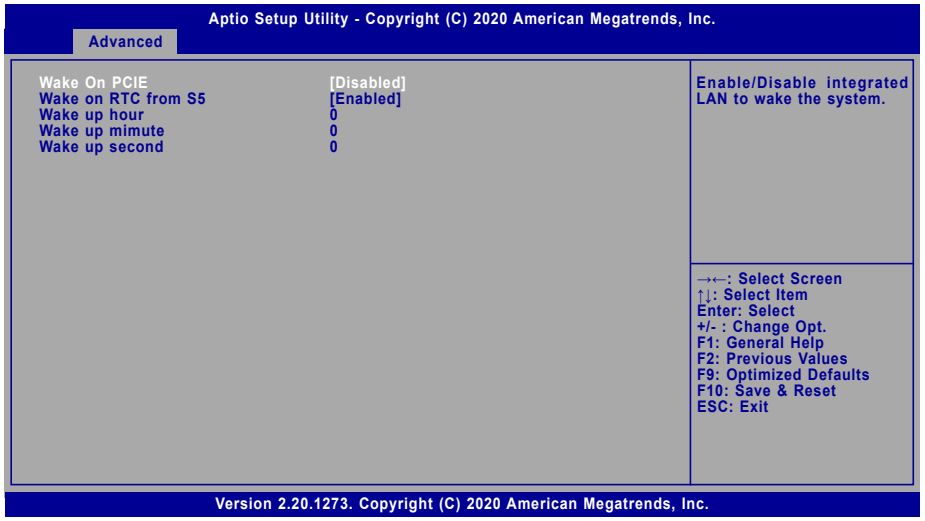
Enable or disable WatchDog function. Once it is enabled, please configure the following field.

SuperIO WatchDog Timer

Set the WatchDog Timer timeout value, ranging from 1 to 255 (second).

▶ Advanced

ACPI Configuration



Wake On PCIE

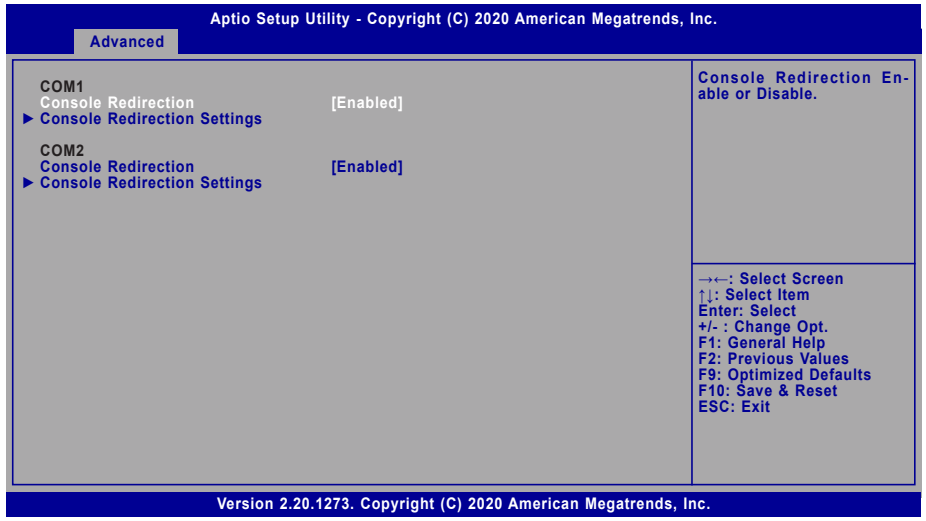
Enable or disable Wake-on-LAN function for the integrated LAN to wake up the system.

Wake on RTC from S5

When Enabled, the system will automatically power up at a designated time every day. Once it's switched to [Enabled], please set up the time of day — hour, minute, and second — for the system to wake up.

▶ Advanced

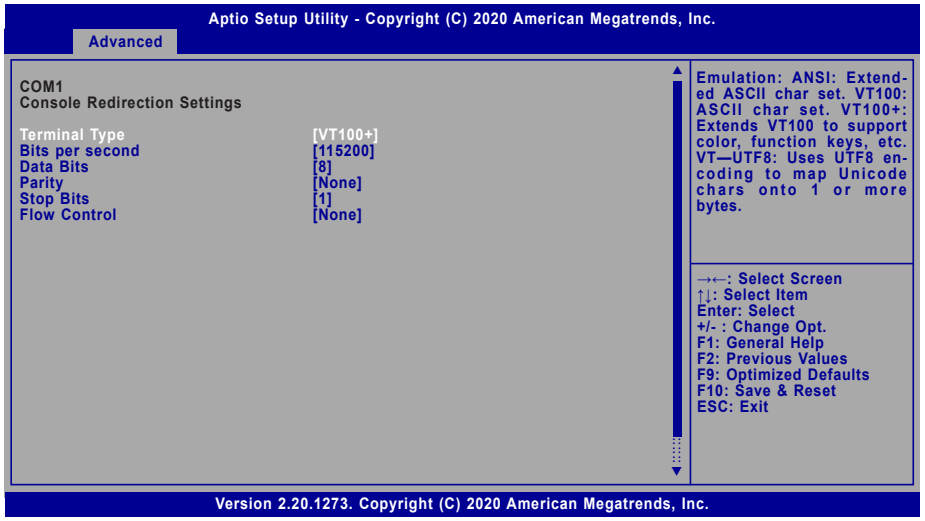
Serial Port Console Redirection



Console Redirection

By enabling Console Redirection of a COM port, the sub-menu of console redirection settings will become available for configuration as detailed in the following.

▶ Console Redirection Settings



Configure the serial settings of the current COM port.

Terminal Type

Select terminal type: VT100, VT100+, VT-UTF8 or ANSI.

Bits per second

Select serial port transmission speed: 9600, 19200, 38400, 57600 or 115200.

Data Bits

Select data bits: 7 bits or 8 bits.

Parity

Select parity bits: None, Even, Odd, Mark or Space.

Stop Bits

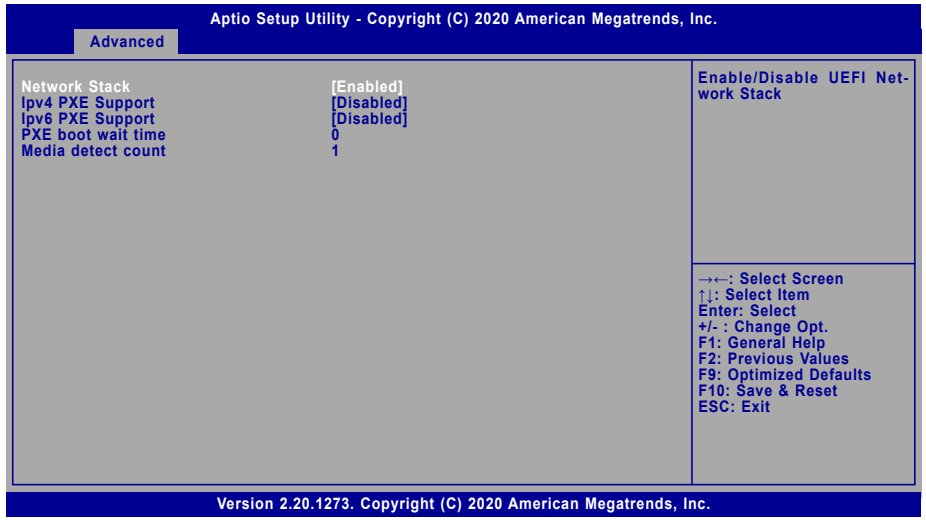
Select stop bits: 1 bit or 2 bits.

Flow Control

Select flow control type: None or Hardware RTS/CTS.

▶ Advanced

Network Stack Configuration



Network Stack

Enable or disable UEFI network stack. The following fields will appear when this field is enabled.

Ipv4 PXE Support

Enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

Ipv6 PXE Support

Enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

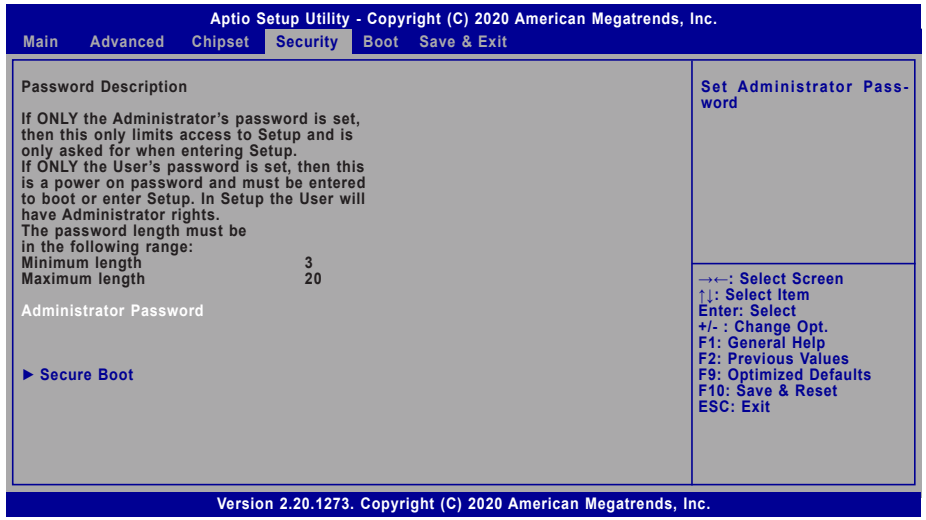
PXE boot wait time

Set the wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

Media detect count

Set the number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

▶ Security

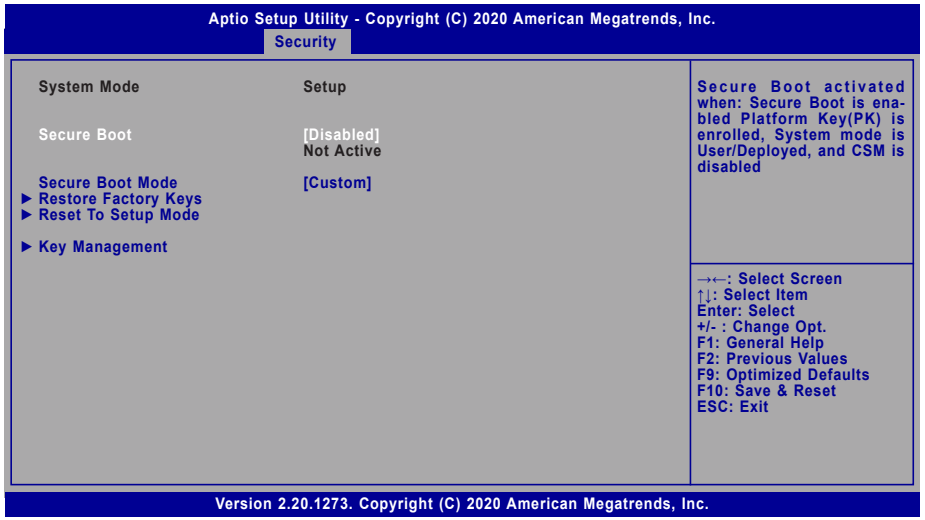


Administrator Password

Set the administrator password. To clear the password, input nothing and press enter when a new password is asked. Administrator Password will be required when entering the BIOS.

▶ Security

Secure Boot



Secure Boot

The Secure Boot store a database of certificates in the firmware and only allows the OSes with authorized signatures to boot on the system. To activate Secure Boot, please make sure that “Secure Boot” is “[Enabled]”, Platform Key (PK) is enrolled, “System Mode” is “User”, and CSM is disabled. After enabling/disabling Secure Boot, please save the configuration and restart the system. When configured and activated correctly, the Secure Boot status will be “Active”.

Secure Boot Mode

Select the secure boot mode — Standard or Custom. When set to Custom, the following fields will be configurable for the user to manually modify the key database.

Restore Factory Keys

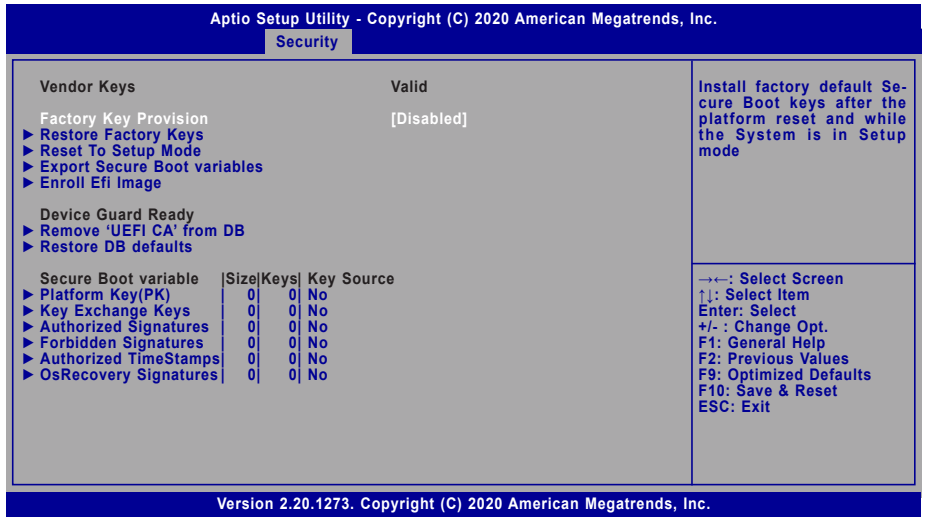
Force system to User Mode. Load OEM-defined factory defaults of keys and databases onto the Secure Boot. Press Enter and a prompt will show up for you to confirm.

Reset To Setup Mode

Clear the database from the NVRAM, including all the keys and signatures installed in the Key Management menu. Press Enter and a prompt will show up for you to confirm.

▶ Security ▶ Secure Boot

▶ Key Management



Factory Key Provision

Enable or disable the provision factory default keys on next re-start. This will only take place when the "System Mode" in the previous menu is in "Setup", which can be achieved by moveing the cursor to the "Reset To Setup Mode" and press Enter.

Restore Factory Keys

Force system to User Mode. Configure NVRAM to contain OEM-defined factory default Secure Boot keys.

Reset To Setup Mode

Clear the database from the NVRAM, including all the keys and signatures installed in the Key Management menu. Press Enter and a prompt will show up for you to confirm.

Export Secure Boot variables

Export the Secure Boot settings (i.e. all keys and signatures) as files to the root directory of a file system device. Press Enter and select a storage device listed in the pop-up menu. The saved files will be named automatically according to the type of key/signature as listed below.

- "PK" for Platform Keys
- "KEK" for Key Exchange Keys
- "db" for Authorized Signatures
- "dbx" for Forbidden Signatures

Enroll Efi Image

Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db). Press Enter and select a storage device listed in the pop-up menu, select a directory, and then select the EFI Image document.

Remove 'UEFI CA' from DB

Remove Microsoft UEFI CA from the Authorized Signature database. For systems that support Device Guard, Microsoft UEFI CA must NOT be included in the Authorized Signature database.

Restore DB defaults

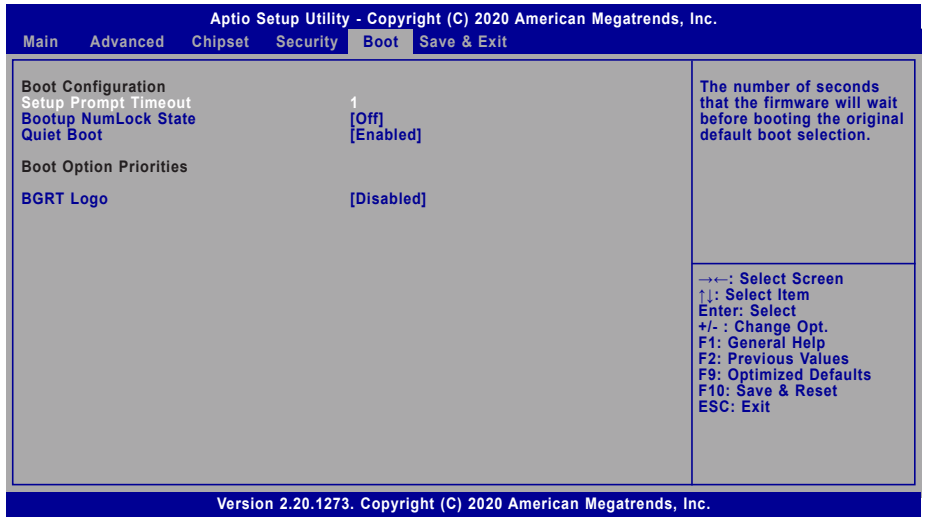
Press Enter to restore the database variable to factory defaults.

Manually configure the following keys and signatures. Move the cursor to the field and press Enter, and then a pop-up menu will show up.

Platform Key(PK), Key Exchange Keys, Authorized Signatures, Forbidden Signatures, Authorized TimeStamps, OsRecovery Signatures

Details	List the information of enrolled keys and signatures
Export	Save the key or signature as a file to the root directory of a file system. The saved files will be named automatically according to the type of key/signature as previously listed in the "Export Secure Boot Variables".
Update	Load factory default database
Append	Enroll keys and signatures from a file system
Delete	Delet keys and signatures

▶ Boot



Setup Prompt Timeout

Set the number of seconds to wait for the setup activation key. 65535 (0xFFFF) denotes indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state: On or Off.

Quiet Boot

This section is used to enable or disable quiet boot option.

Boot Option Priorities

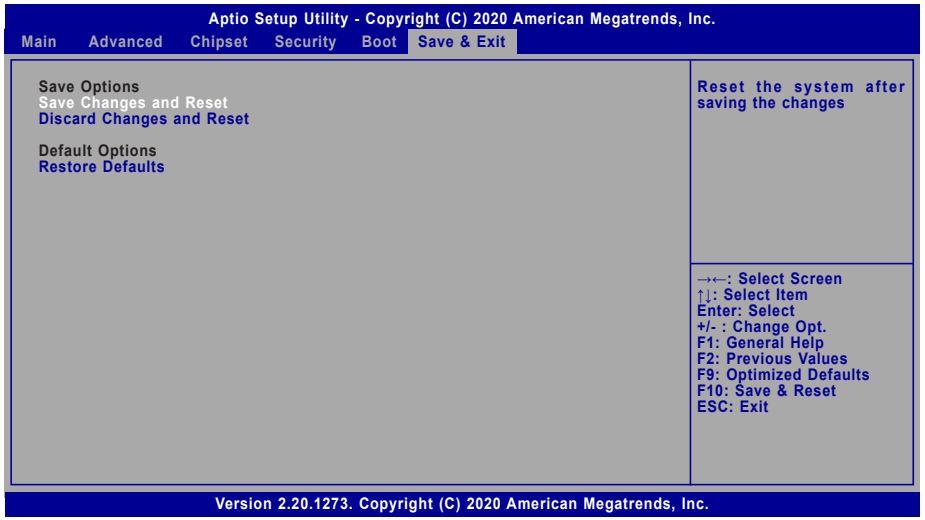
Rearrange the system boot order of available boot devices. Please enable the devices that you wish to set as boot devices in the "Advanced > CSM Configuration" submenu.

BGRT Logo

It is used to enable or disable the support of display logo with ACPI BGRT table.

Note:
If “Boot option filter” of “CSM Configuration” is set to “UEFI and Legacy” or “UEFI only”, and “Quiet Boot” is set to enabled, “BGRT Logo” will show up for configuration. Refer to the Advanced > CSM Configuration submenu for more information.

▶ Save & Exit



Save Changes and Reset

To save the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system after saving all changes made.

Discard Changes and Reset

To discard the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system setup without saving any changes.

Restore Defaults

To restore and load the optimized default values, select this field and then press <Enter>. A dialog box will appear. Select Yes to restore the default values of all the setup options.

▶ Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files and specific instructions about how to update BIOS with the flash utility. For updating AMI BIOS in UEFI mode, you may refer to the how-to video at https://www.dfi.com/Knowledge/Video/5.

▶ Notice: BIOS SPI ROM

1. The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.

2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.

3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

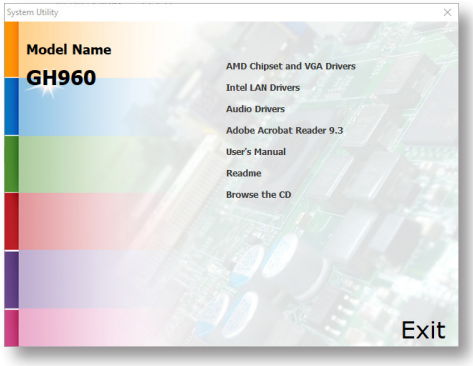
Note:
a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.
b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not.

Chapter 4 - Supported Software

Install drivers, utilities and software applications that are required to facilitate and enhance the performance of the system board. You may acquire the software from your sales representatives, from a DVD included in the shipment, or from the website download page at https://www.dfi.com/DownloadCenter.

▶ Auto-run Menu

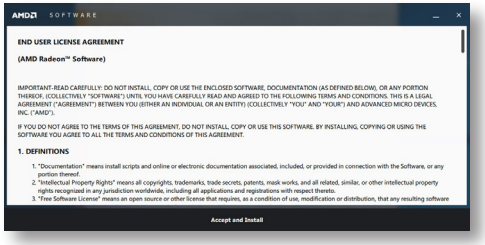
After inserting your DVD-ROM into your optical drive or executing your DVD image, the System Utility auto-run menu may pop up. Click on the utility or driver that is to be installed on the system. Please refer to the following sections that correspond to your selection for more information.



Note:
This step can be ignored if the applications are standalone files.

▶ AMD Chipset and VGA Drivers

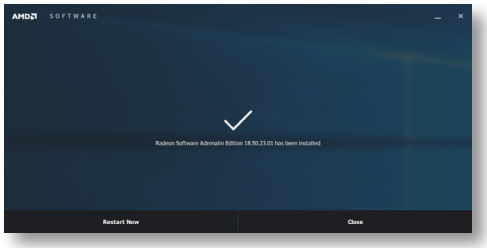
1. Read the license agreement then click “Accept and Install”.



2. The step displays the installing status in the progress.

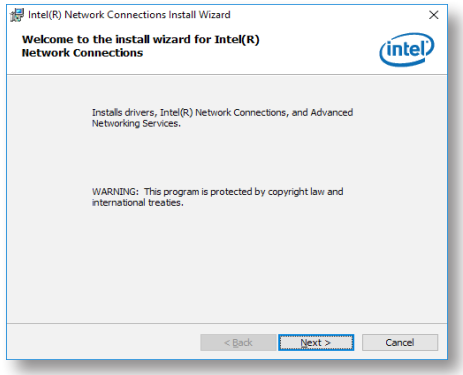
3. After completing installation, click “Restart Now” to exit setup.

   Restarting the system will allow the new software installation to take effect.

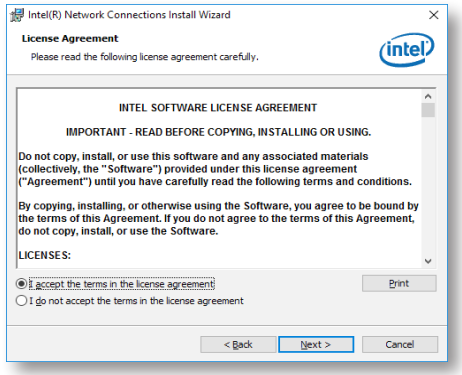


▶ Intel LAN Driver

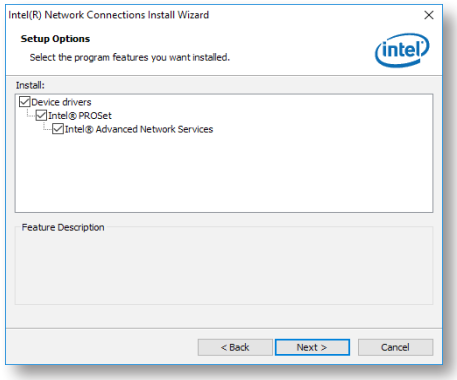
1. Setup is ready to install the driver. Click “Next”.



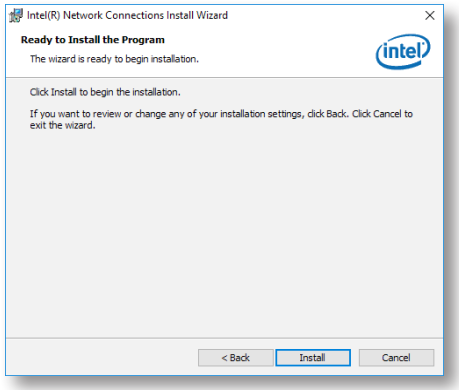
2. Click “I accept the terms in the license agreement” then click “Next”.



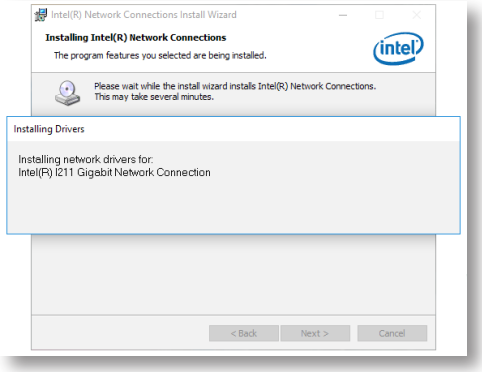
3. Select the program features you want installed then click “Next”.



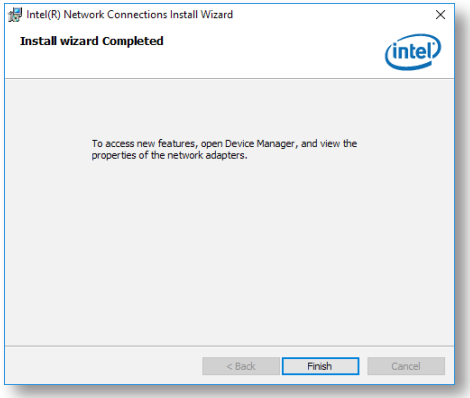
4. Click “Install” to begin the installation.



5. The step displays the installing status in the progress.

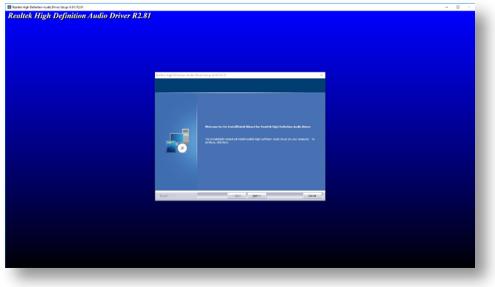


6. After completing installation, click “Finish”.



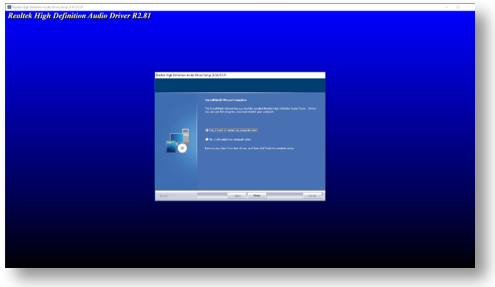
▶ Audio Drivers

1. Setup is ready to install the driver. Click “Next”.



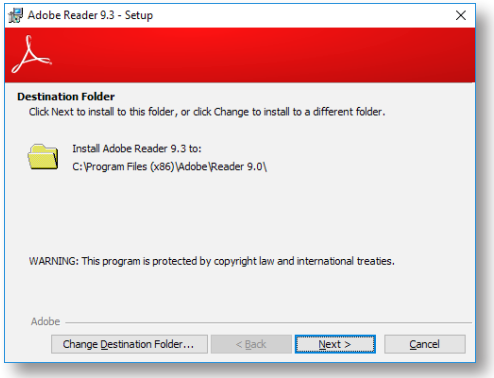
2. Click “Yes, I want to restart my computer now” then click “Finish”.

   Restarting the system will allow the new software installation to take effect.

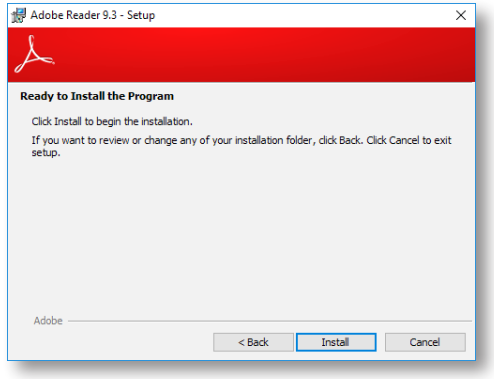


▶ Adobe Acrobat Reader 9.3

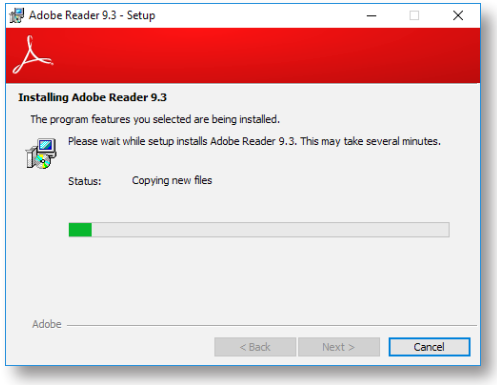
1. Click “Next” to install or click “Change Destination Folder” to select another folder.



2. Click “Install” to begin installation.



3. Setup is now installing the driver.



4. Click “Finish” to exit installation.