Approval Sheet

Customer	
Product Number	**M4DI-4GSSIC0K-F**
Module speed	**PC4-2666**
Pin	**260 pin**
Cl-tRCD-tRP	**19-19-19**
Operation temperature	**0℃~85℃**
Date	**29th Nov 2018**

The Total Solution For
Industrial Flash Storage

Rev 1.0

1. Features

Key Parameter

Industry Nomenclature	**Speed Grade**	**Data Rate MT/s**			**CL**	**tRCD**	**tRP**
		CL=15	**CL=17**	**CL=19**			
PC4-2666	**I**	2133	2400	2666	19	19	19

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- JEDEC Standard 260-pin Small Outline Dual In-Line Memory Module
- Intend for PC4-2666 applications
- Inputs and Outputs are SSTL-12 compatible
- VDD=VDDQ= 1.2 Volt (1.14V~1.26V)
- VPP=2.5 Volt (2.375V~2.75V)
- VDDSPD=2.2-3.6V
- Low-Power auto self-refresh (LPASR)
- SDRAMs have 16 internal banks for concurrent operation (4 Bank Group of 4 banks each)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals.
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Gold Plating Thickness 30µ”
- Fly-By topology
- Terminated control, command and address bus
- Programmable /CAS Latency: 10,11,12,13,14,15,16,17,18,19,20
- On-die VREFDQ generation and Calibration
- Temperature Sensor with SPD EEPROM
- Support ECC Function
- RoHS and Halogen free *(Section 13)*

2. Environmental Requirements

DDR4 ECC SODIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +55	°C	3
HOPR	Operating Humidity (relative)	10 to 90	°C%	
TSTG	Storage Temperature	-50 to +100	°C	1
HSTG	Storage Humidity (without condensation)	5 to 95	%	1
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. 2. Up to 9850 ft. 3. The component maximum case temperature (TCASE) shall not exceed the value specified in the DDR4 DRAM component specification. JESD79-4 *Follow JEDEC spec.*				

3. SDRAM Parameters by device density

RTT_Nom Setting	Parameter		4Gb	Units
tREFI	Average periodic refresh interval	0°C≦**TCASE**≦**85**°C	7.8	µs
		85°C<**TCASE**≦**95**°C	3.9	µs

4. Ordering Information

DDR4 VLP ECC SODIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M4DI-4GSSIC0K-F	4GB	PC4-2666	512Mx72	9	1	Y

5. Pin Configurations (Front side/Back side)

DDR4 ECC SODIMM

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VSS	2	VSS	67	DQ29	68	VSS	133	A1	134	EVENT_n, NF	199	DM5_n/DBI5_n	200	DQS5_t
3	DQ5	4	DQ4	69	VSS	70	DQ24	135	VDD	136	VDD	201	VSS	202	VSS
5	VSS	6	VSS	71	DQ25	72	VSS	137	CK0_t	138	CK1_t/NF	203	DQ46	204	DQ47
7	DQ1	8	DQ0	73	VSS	74	DQS3_c	139	CK0_c	140	CK1_c/NF	205	VSS	206	VSS
9	VSS	10	VSS	75	DM3_n/DBI3_n	76	DQS3_t	141	VDD	142	VDD	207	DQ42	208	DQ43
11	DQS0_c	12	DM0_n/DBI0_n	77	VSS	78	VSS	143	PARITY	144	A0	209	VSS	210	VSS
13	DQS0_t	14	VSS	79	DQ30	80	DQ31	145	BA1	146	A10/AP	211	DQ52	212	DQ53
15	VSS	16	DQ6	81	VSS	82	VSS	147	VDD	148	VDD	213	VSS	214	VSS
17	DQ7	18	VSS	83	DQ26	84	DQ27	149	CS0_n	150	BA0	215	DQ49	216	DQ48
19	VSS	20	DQ2	85	VSS	86	VSS	151	WE_n/A14	152	RAS_n/A16	217	VSS	218	VSS
21	DQ3	22	VSS	87	CB5/NC	88	CB4/NC	153	VDD	154	VDD	219	DQS6_c	220	DM6_n/DBI6_n
23	VSS	24	DQ12	89	VSS	90	VSS	155	ODT0	156	CAS_n/A15	221	DQS6_t	222	VSS
25	DQ13	26	VSS	91	CB1/NC	92	CB0/NC	157	CS1_n	158	A13	223	VSS	224	DQ54
27	VSS	28	DQ8	93	VSS	94	VSS	159	VDD	160	VDD	225	DQ55	226	VSS
29	DQ9	30	VSS	95	DQS8_c	96	DM8_n/DBI8_n/NC	161	ODT1	162	C0/CS2_n/NC	227	VSS	228	DQ50
31	VSS	32	DQS1_c	97	DQS8_t	98	VSS	163	VDD	164	VREFCA	229	DQ51	230	VSS
33	DM1_n/DBI1_n	34	DQS1_t	99	VSS	100	CB6/NC	165	C1, CS3_n, NC	166	SA2	231	VSS	232	DQ60
35	VSS	36	VSS	101	CB2/NC	102	VSS	167	VSS	168	VSS	233	DQ61	234	VSS
37	DQ15	38	DQ14	103	VSS	104	CB7/NC	169	DQ37	170	DQ36	235	VSS	236	DQ57
39	VSS	40	VSS	105	CB3/NC	106	VSS	171	VSS	172	VSS	237	DQ56	238	VSS
41	DQ10	42	DQ11	107	VSS	108	RESET_n	173	DQ33	174	DQ32	239	VSS	240	DQS7_c
43	VSS	44	VSS	109	CKE0	110	CKE1	175	VSS	176	VSS	241	DM7_n/DBI7_n	242	DQS7_t
45	DQ21	46	DQ20	111	VDD	112	VDD	177	DQS4_c	178	DM4_n/DBI4_n	243	VSS	244	VSS
47	VSS	48	VSS	113	BG1	114	ACT_n	179	DQS4_t	180	VSS	245	DQ62	246	DQ63
49	DQ17	50	DQ16	115	BG0	116	ALERT_n	181	VSS	182	DQ39	247	VSS	248	VSS
51	VSS	52	VSS	117	VDD	118	VDD	183	DQ38	184	VSS	249	DQ58	250	DQ59
53	DQS2_c	54	DM2_n/DBI2_n	119	A12	120	A11	185	VSS	186	DQ35	251	VSS	252	VSS
55	DQS2_t	56	VSS	121	A9	122	A7	187	DQ34	188	VSS	253	SCL	254	SDA
57	VSS	58	DQ22	123	VDD	124	VDD	189	VSS	190	DQ45	255	VDDSPD	256	SA0
59	DQ23	60	VSS	125	A8	126	A5	191	DQ44	192	VSS	257	VPP	258	VTT
61	VSS	62	DQ18	127	A6	128	A4	193	VSS	194	DQ41	259	VPP	260	SA1
63	DQ19	64	VSS	129	VDD	130	VDD	195	DQ40	196	VSS				
65	VSS	66	DQ28	131	A3	132	A2	197	VSS	198	DQS5_c				

Note:
1. NC = No Connect, RFU = Reserved for Future Use
2. Address A17 is only valid for 16 Gb x4 based SDRAMs.
3. RAS_n is a multiplexed function with A16.
4. CAS_n is a multiplexed function with A15.
5. WE_n is a multiplexed function with A14.

6. Architecture

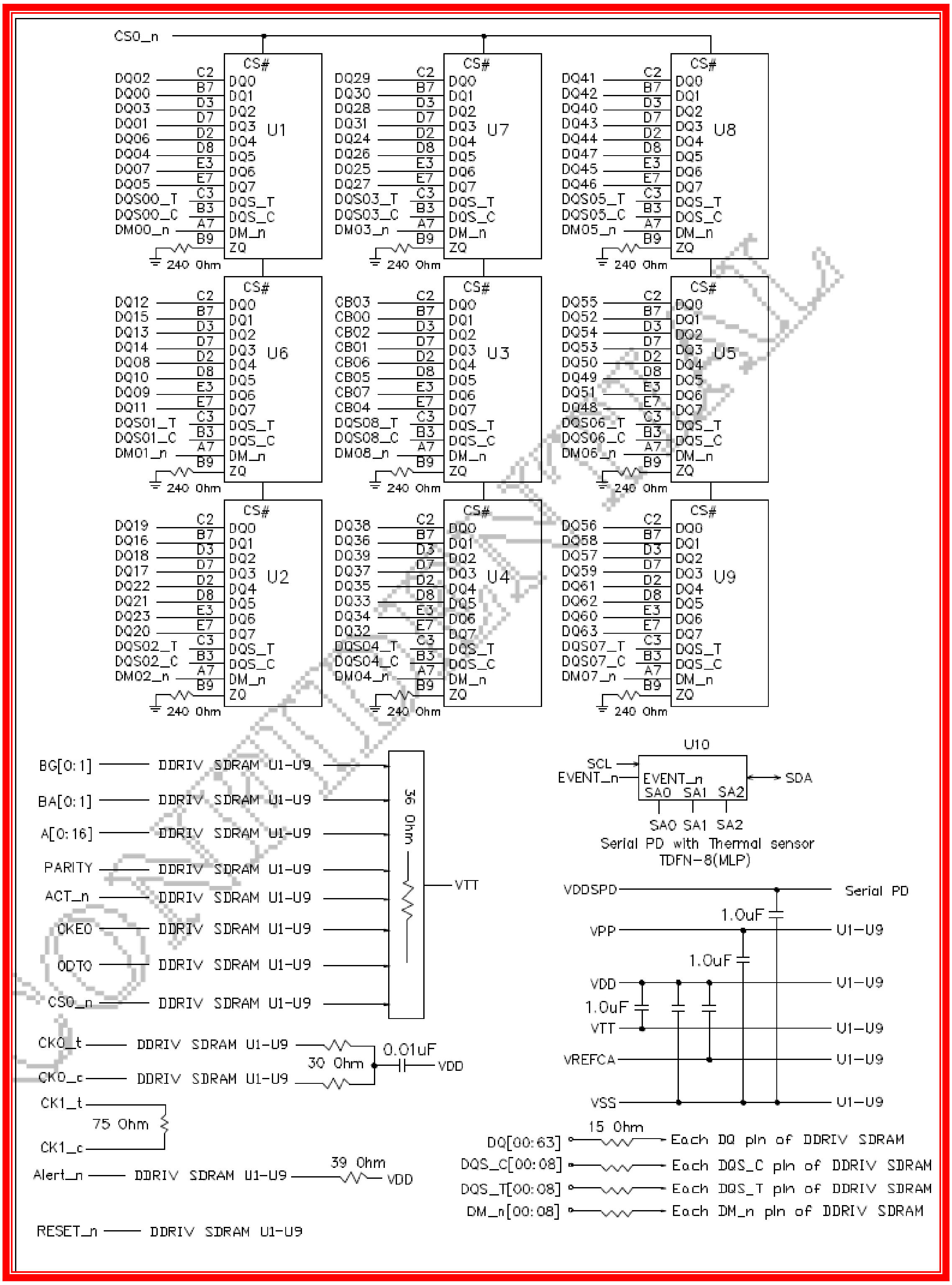
Pin Definition

Pin Name	Description	Pin Name	Description
A0–A16	SDRAM address bus	SCL	I^2C serial bus clock for SPD/TS
BA0, BA1	SDRAM bank select	SDA	I^2C serial bus data line for SPD/TS
BG0, BG1	SDRAM bank group select	SA0–SA2	I^2C slave address select for SPD/TS
RAS_n[1]	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n[2]	SDRAM column address strobe	VDD	SDRAM I/O & core power supply
WE_n[3]	SDRAM write enable	VPP	SDRAM activating power supply
CS0_n, CS1_n CS2_n, CS3_n	Rank Select Lines	C0, C1	Chip ID lines for 3DS components
CKE0, CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD/TS positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0–CB7	DIMM ECC check bits (for x72 module)		
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set SDRAMs to a Known State
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	EVENT_n	SPD signals a thermal event has occurred.
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)	VTT	Termination supply for the Address, Command and Control bus
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	NC	No connection
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

Note 1 RAS_n is a multiplexed function with A16.
Note 2 CAS_n is a multiplexed function with A15.
Note 3 WE_n is a multiplexed function with A14.

7. Function Block Diagram:

- (4GB, 1 Rank 512Mx8 DDR4 SDRAMs)



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

8. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.3 to +1.5	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.3 to +1.5	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.3 to +1.5	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.

For measurement conditions, please refer to the JEDEC document JESD51-2.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under

all operating conditions.

3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 ℃ case temperature. Full specifications are supported in this range, but the following additional

conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

9. Operating Condition

Symbol	Parameter	Min	Nom	Max	Units	Notes
VDD	Supply Voltage	1.14	1.2	1.26	V	1
VPP	DRAM activating power supply	2.375	2.5	2.75	V	2
VREFCA(DC)	Input reference voltage command/ address bus	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	3
VTT	Termination Voltage	0.49 × VDD	0.5 × VDD	0.51 × VDD	V	4

Note:

1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
4. VTT termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.

10. Operating, Standby, and Refresh Currents

- 4GB ECC SODIMM (1 Rank 512Mx8 DDR4 SDRAMs)

Symbol	Proposed Conditions	Value		Units
		IDD Max.	IPP Max.	
IDD0	Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n:stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2;ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	TBD	TBD	mA
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0	TBD	TBD	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stableat 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	TBD	TBD	mA
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1	TBD	TBD	mA
IDD2N	Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banksclosed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	TBD	TBD	mA
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N	TBD	TBD	mA

IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern	TBD	TBD	mA
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled3	TBD	TBD	mA
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled3	TBD	TBD	mA
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled3	TBD	TBD	mA
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled3	TBD	TBD	mA
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	TBD	TBD	mA
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	TBD	TBD	mA
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern	TBD	TBD	mA

IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N	TBD	TBD	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	TBD	TBD	mA
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	TBD	TBD	mA
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R	TBD	TBD	mA
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled3, Other conditions: see IDD4R	TBD	TBD	mA
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	TBD	TBD	mA
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W	TBD	TBD	mA
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions: see IDD4W	TBD	TBD	mA

IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled3, Other conditions: see IDD4W	TBD	TBD	mA
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled3, Other conditions: see IDD4W	TBD	TBD	mA
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	TBD	TBD	mA
IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B	TBD	TBD	mA
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B	TBD	TBD	mA
IDD6N	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	TBD	TBD	mA
IDD6E	Self-Refresh Current: Extended Temperature Range) TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	TBD	TBD	mA

IDD6R	Self-Refresh Current: Reduced Temperature Range TCASE: 0 - 45 °C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: see Table 34 on p age 37; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	TBD	TBD	mA
IDD6A	Auto Self-Refresh Current TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: see Table 34 on p age 37; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	TBD	TBD	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	TBD	TBD	mA
IDD8	Maximum Power Down Current TBD	TBD	TBD	mA

11. Timing Parameters

Clock Timing

Parameter	Symbol	MIN	MAX	Units
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	ns
Average Clock Period	tCK(avg)	0.750	<0.833	ns
Average high pulse width	tCH(avg)	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_ to t	tCK(avg)max + tJIT(per)max_tot	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.45	-	tCK(avg)
Clock Period Jitter- total	JIT(per)_tot	-38	38	ps
Clock Period Jitter- deterministic	JIT(per)_dj	-19	19	ps
Clock Period Jitter during DLL lock-ing period	tJIT(per, lck)	-30	30	ps
Cycle to Cycle Period Jitter	tJIT(cc)_to-tal	75		ps
Cycle to Cycle Period Jitter deter-ministic	tJIT(cc)_dj	38		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	60		ps
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	ps
Cumulative error across 2 cycles	tERR(2per)	-55	55	ps
Cumulative error across 3 cycles	tERR(3per)	-66	66	ps
Cumulative error across 4 cycles	tERR(4per)	-73	73	ps
Cumulative error across 5 cycles	tERR(5per)	-78	78	ps
Cumulative error across 6	tERR(6per)	-83	83	ps

cycles				
Cumulative error across 7 cycles	tERR(7per)	-87	87	ps
Cumulative error across 8 cycles	tERR(8per)	-91	91	ps
Cumulative error across 9 cycles	tERR(9per)	-94	94	ps
Cumulative error across 10 cycles	tERR(10per)	-96	96	ps
Cumulative error across 11 cycles	tERR(11per)	-99	99	ps
Cumulative error across 12 cycles	tERR(12per)	-101	101	ps
Cumulative error across 13 cycles	tERR(13per)	-103	103	ps
Cumulative error across 14 cycles	tERR(14per)	-104	104	ps
Cumulative error across 15 cycles	tERR(15per)	-106	106	ps
Cumulative error across 16 cycles	tERR(16per)	-108	108	ps
Cumulative error across 17 cycles	tERR(17per)	-110	110	ps
Cumulative error across 18 cycles	tERR(18per)	-112	112	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)		ps
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	TBD	-	ps
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	TBD	-	ps
Command and Address hold time to CK_t, CK_c referenced	tIH(base)	TBD	-	ps

to Vih(dc) / Vil(dc) levels				
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	TBD	-	ps
Control and Address Input pulse width for each input	tIPW	385	-	ps
Command and Address Timing				
Parameter	Symbol	MIN	MAX	Units
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 5 ns)	-	nCK
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S(1/ 2K)	Max(4nCK,3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,4.9ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/ 2K)	Max(4nCK,4.9ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,21ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,12ns)	-	ns

Delay from start of internal write transaction to internal read com-mand for different bank group	tWTR_S	max(2nCK,2.5ns)	-	
Delay from start of internal write transaction to internal read com-mand for same bank group	tWTR_L	max(4nCK,7.5ns)	-	
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (5nCK,3.75ns)	-	ns
delay from start of internal write transaction to internal read com-mand for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max (5nCK,3.75ns)	-	ns
delay from start of internal write transaction to internal read com-mand for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+max (5nCK,3.75ns)	-	ns
DLL locking time	tDLLK	854	-	nCK
Mode Register Set command cycle time	tMRD	8	-	nCK
Mode Register Set command up-date delay	tMOD	max(24nCK,15ns)	-	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
Multi Purpose Register Write Re-covery Time	tWR_MPR	tMOD (min) + AL + PL	-	-
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))		nCK
DQ0 or DQL0 driven to 0 set-up time to first DQS rising	tPDA_S	0.5	-	UI

edge				
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	UI
CS_n to Command Address Latency				
CS_n to Command Address Laten-cy	tCAL	5	-	nCK
DRAM Data Timing				
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.18	tCK(avg) /2
DQ output hold time from DQS_t,DQS_c	tQH	0.74	-	tCK(avg) /2
Data Valid Window per device: tQH - tDQSQ for a device	tDVWd	TBD	-	UI
Data Valid Window per device, per pin: tQH - tDQSQ each device's out-put	tDVWp	0.72	-	UI
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-310	170	Ps
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	170	ps
Data Strobe Timing				
DQS_t, DQS_c differential READ Preamble	tRPRE	0.9		tCK
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	TBD	tCK
DQS_t,DQS_c differential output high time	tQSH	0.4	-	tCK
DQS_t,DQS_c differential output low time	tQSL	0.4	-	tCK
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	tCK
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	TBD	tCK
DQS_t and DQS_c low-impedance time	tLZ(DQS)	-310	170	ps

(Referenced from RL-1)				
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	170	ps
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	tCK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	tCK
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	tCK
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	tCK
DQS_t, DQS_c rising edge output timing locatino from rising	tDQSCK (DLL On)	-170	170	ps
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)		270	ps
MPSM Timing				
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)		
Exit MPSM to commands not requiring a locked DLL	tXMP	txs(imin)		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)		
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	
Calibration Timing				

Power-up and RESET calibration time	tZQinit	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	nCK
Normal operation Short calibration time	tZQCS	128	-	nCK
Reset/Self Refresh Timing				
Exit Reset from CKE HIGH to a valid command	command tXPR	max (5nCK,tRFC(min)+ 10ns)	-	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT(min)	tRFC4(min)+ 10ns	-	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	
Exit Self Refresh to commands re-quiring a locked DLL	tXSDLL	tDLLK(min)	-	
Minimum CKE low width for Self re-fresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	
Minimum CKE low width for Self re-fresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power- Down Entry (PDE)	tCKSRE	max(5nCK,10 ns)	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power- Down when CA Parity is enabled	tCKS-RE_PAR	max (5nCK,10ns) +PL	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or	tCKSRX	max(5nCK,10 ns)	-	

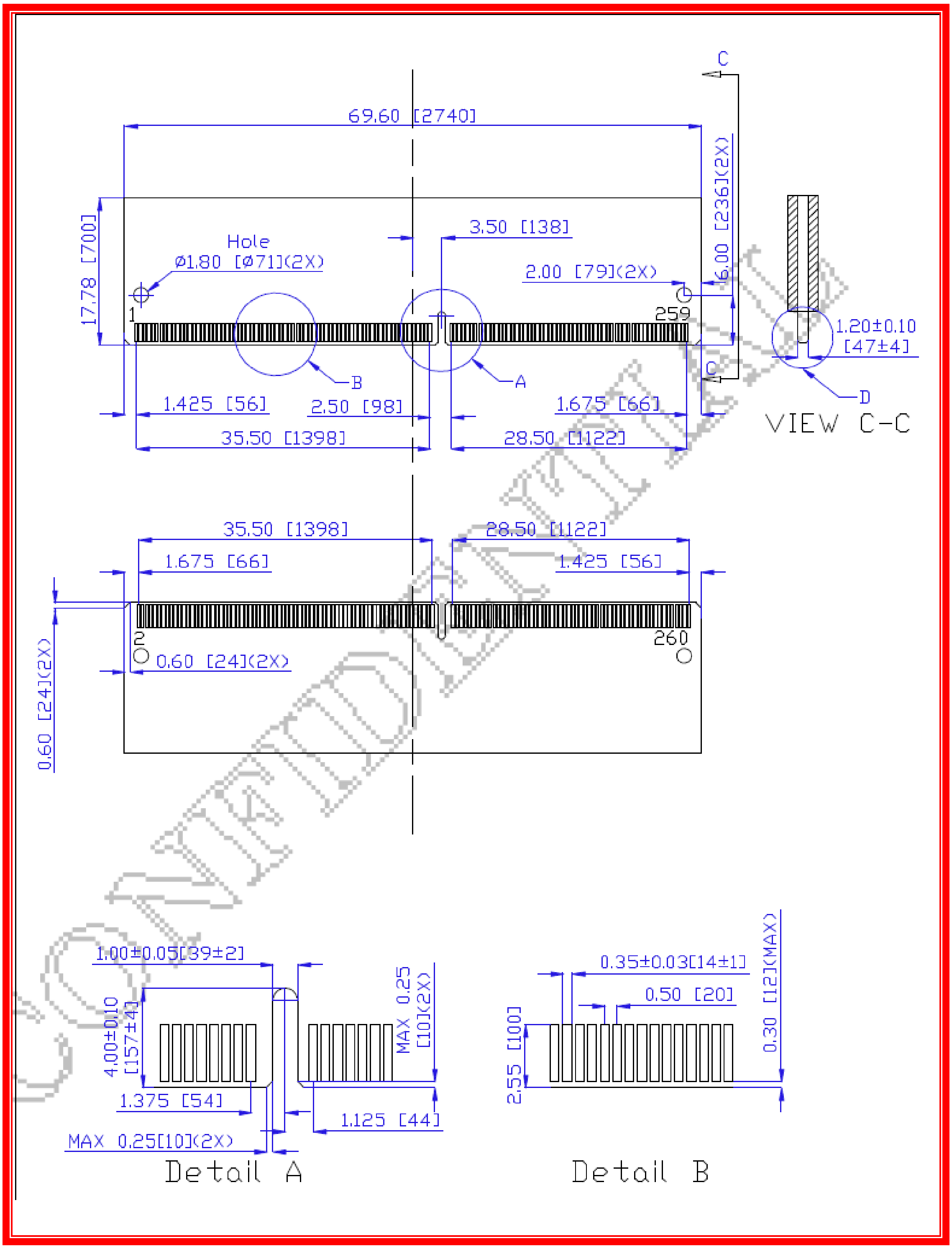
Reset Exit				
Power Down Timing				
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	(4nCK,6ns)	-	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	
Command pass disable delay	tCPDED	4	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	2	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	2	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	
PDA Timing				
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)		
Mode Register Set command	tMOD_PDA	tMOD		

up-date delay in PDA mode				
ODT Timing				
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	ns
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
Write Leveling Timing				
First DQS_t/DQS_n rising edge af-ter write leveling mode is pro-grammed	tWLMRD	40	-	nCK
DQS_t/DQS_n delay after write lev-eling mode is programmed	tWLDQSEN	25	-	nCK
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	tCK(avg)
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	tCK(avg)
Write leveling output delay	tWLO	0	9.5	ns
Write leveling output error	tWLOE		2	ns
CA Parity Timing				
Commands not guaranteed to be executed during this time	tPAR_UN-KNOWN	-	PL	
Delay from errant command to ALERT_n assertion	tPAR_ALER T_ON	-	PL+6ns	
Pulse width of ALERT_n signal when asserted	tPAR_ALER T_PW	80	160	nCK
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALER T_RSP	-	71	nCK

Parity Latency	PL	5		nCK
CRC Error Reporting				
CRC error to ALERT_n latency	tCRC_ALER T	3	13	ns
CRC ALERT_n pulse width	CRC_ALER T_PW	6	10	nCK
tREFI				
tRFC1 (min)	2Gb	160	-	ns
	4Gb	260	-	ns
	8Gb	350	-	ns
	16Gb	TBD	-	ns
tRFC2 (min)	2Gb	110	-	ns
	4Gb	160	-	ns
	8Gb	260	-	ns
	16Gb	TBD	-	ns
tRFC3 (min)	2Gb	90	-	ns
	4Gb	110	-	ns
	8Gb	160	-	ns
	16Gb	TBD	-	ns

12. PACKAGE DIMENSION

- (4GB, 1 Rank 512Mx8 DDR4 base VLP ECC SODIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified

13. RoHS Declaration

innodisk

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宜鼎國際股份有限公司

Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟2011/65/EU 及（EU） 2015/863 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
鉛（Pb）	< 1000 ppm
汞（Hg）	< 1000 ppm
鎘（Cd）	< 100 ppm
六價鉻（Cr 6+）	< 1000 ppm
多溴聯苯（PBBs）	< 1000 ppm
多溴二苯醚（PBDEs）	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯（DEHP）	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯（BBP）	< 1000 ppm
鄰苯二甲酸二丁酯（DBP）	< 1000 ppm
鄰苯二甲酸二異丁酯（DIBP）	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2017 / 01 / 18

Revision Log

Rev	Date	Modification
0.1	29th Nov 2018	Preliminary Edition
1.0	29th Nov 2018	Official Released