



BW968
COM Express Compact Module
User's Manual

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COM Express Specification Reference

PICMG[®] COM Express Module[™] Base Specification.

http://www.picmg.org/

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

- The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
- 2. Shielded interface cables must be used in order to comply with the emission limits.

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About this Manual

This manual can be downloaded from the website, or acquired as an electronic file included in the optional CD/DVD. The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

Warranty

- Warranty does not cover damages or failures that arised from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.
- 2. The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.
- Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.
- 4. We will not be liable for any indirect, special, incidental or consequencial damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

- To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.
- 2. Wear an antistatic wrist strap.
- 3. Do all preparation work on a static-free surface.
- Hold the device only by its edges. Be careful not to touch any of the components, contacts
 or connections.
- Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.



Important:

Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

To avoid damage to the system:

Use the correct AC input voltage range.

To reduce the risk of electric shock:

Unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

- One BW968 board
- One Heat sink (Height: TBD)

Optional Items

- · COM332-B carrier board kit
- Heat spreader

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

Before Using the System Board

Before using the system board, prepare basic system components.

If you are installing the system board in a new system, you will need at least the following internal components.

- Memory module
- Storage devices such as hard disk drive, DVD-ROM, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

Chapter 1 - Introduction

Specifications

System	Processor	Intel® Pentium®/Celeron® Processor N3000 Family, BGA 1170 (*) Intel® Atom™ Processor x5-E8000, Quad Core, 2M Cache, 1.04GHz, 5W Intel® Pentium® Processor N3710, Quad Core, 2M Cache, 1.6GHz (2.56GHz), 6W Intel® Celeron® Processor N3160, Quad Core, 2M Cache, 1.6GHz (2.24GHz), 6W Intel® Celeron® Processor N3060, Dual Core, 2M Cache, 1.6GHz (2.48GHz), 6W Intel® Celeron® Processor N3010, Dual Core, 2M Cache, 1.04GHz (2.24GHz), 4W
	Memory	Two 204-pin SODIMM up to 8GB Dual Channel DDR3L 1600MHz
	BIOS	Insyde SPI 64Mbit
Graphics	Controller	Intel® HD Graphics
	Feature	OpenGL 4.2, Direct X 11.1, OpenCL 1.2, OGL ES 3.0 HW Decode: H.264, MPEG2, VC1, VP8, H.265, MPEG4 HW Encode: H.264, MPEG2, MPEG4
	Display	1 x VGA/DDI (DDI available upon request) 1 x LVDS/eDP (eDP available upon request) 1 x DDI VGA: resolution up to 1920x1200 @ 60Hz LVDS: dual channel 24-bit, resolution up to 1920x1200 @ 60Hz eDP: resolution up to 2560x1440 @ 60Hz HDMI: resolution up to 3840x2160 @ 30Hz or 2560x1600 @ 60Hz DP: resolution up to 3840x2160 @ 30Hz or 2560x1600 @ 60Hz
	Triple Displays	VGA + LVDS + DDI DDI + eDP + DDI (available upon request)
Expansion	Interface	3 x PCIe x1 (Gen 2) 1 x LPC 1 x I ² C 1 x SMBus 2 x Serial (TX/RX)
Audio	Interface	HD Audio
Ethernet	Controller	1 x Intel [®] I211AT PCIe (10/100/1000Mbps)
I/O	USB	4 x USB 3.0 8 x USB 2.0
	SATA	2 x SATA 3.0 (up to 6Gb/s)
	DIO	1 x 8-bit DIO

WatchDog Timer	Output & Interval	System Reset, Programmable via Software from 1 to 255 Seconds
Security	TPM	Available Upon Request
Power	Туре	12V, 5VSB, VCC_RTC (ATX mode) 12V, VCC_RTC (AT mode)
	Consumption	Typical: N3710: 12V @ 0.28A (3.41Watt) Max.: N3710: 12V @ 0.61A (7.35Watt)
OS Support		Windows 8.1 64-bit Windows 7 (/WES7) 32/64-bit Windows 10 IoT Enterprise 64-bit Debian 8 (with VESA graphic driver) CentOS 7 (with VESA graphic driver) Ubuntu 15.10 (Intel graphic driver available)
Environment	Temperature	Operating: 0 to 60°C Storage: -40 to 85°C
	Humidity	Operating: 10 to 90% RH Storage: 10 to 90% RH
	MTBF	746,818 hrs @ 25°C; 402,691 hrs @ 45°C; 241,711 hrs @ 60°C Calculation Model: Telcordia Issue 2, Method Case 3 Environment: GB, GC – Ground Benign, Controlled
Mechanical	Dimensions	COM Express® Compact 95mm (3.74") x 95mm (3.74")
	Compliance	PICMG COM Express® R2.1, Type 6

^{*}When PXE function is used with the UEFI boot type, the client screen might display partial screen if the PXE server employs a graphical user interface (GUI)-based management interface. This problem is due to resolution compatibility between the server and the client.

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Features

Watchdog Timer

The Watchdog Timer function allows your application to regularly "clear" the system at the set time interval. If the system hangs or fails to function, it will reset at the set time interval so that your system will continue to operate.

• DDR3L

DDR3L is a higher performance DDR3 SDRAM interface providing less voltage and higher speed successor. DDR3L supporting 1600MHz delivers increased system bandwidth and improved performance to provide its higher bandwidth and its increase in performance at a lower power.

Graphics

The integrated Intel® HD graphics engine delivers an excellent blend of graphics performance and features to meet business needs. It provides excellent video and 3D graphics with outstanding graphics responsiveness. These enhancements deliver the performance and compatibility needed for today's and tomorrow's business applications. Supports 1 x VGA/DDI, 1 x LVDS/eDP and 1 DDI interfaces for triple display outputs.

Serial ATA

Serial ATA is a storage interface that is compliant with SATA 1.0a specification. With speed of up to 6Gb/s (SATA 3.0), it improves hard drive performance faster than the standard parallel ATA whose data transfer rate is 100MB/s. The bandwidth of the SATA 3.0 will be limited by carrier board design.

Gigabit LAN

The Intel® I211AT Gigabit Ethernet controller supports up to 1Gbps data transmission.

• USB

The system board supports the new USB 3.0. It is capable of running at a maximum transmission speed of up to 5 Gbit/s (625 MB/s) and is faster than USB 2.0 (480 Mbit/s, or 60 MB/s) and USB 1.1 (12Mb/s). USB 3.0 reduces the time required for data transmission, reduces power consumption, and is backward compatible with USB 2.0. It is a marked improvement in device transfer speeds between your computer and a wide range of simultaneously accessible external Plug and Play peripherals.

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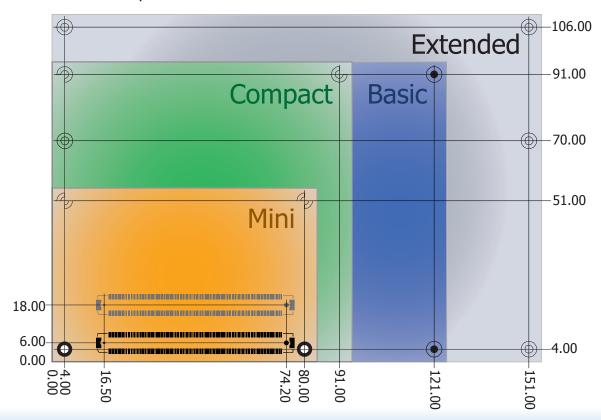
Chapter 2 - Concept

COM Express Module Standards

The figure below shows the dimensions of the different types of COM Express modules.

BW968 is a COM Express Compact module. The dimension is 95mm x 95mm.

- O Common for all Form Factors
- Extended only
- Basic only
- **Compact** only
- [♠] Compact and Basic only



Chapter 2 Concept www.dfi.com

Specification Comparison Table

The table below shows the COM Express standard specifications and the corresponding specifications supported on the BW968 module.

		COM Express Module Base	DFI BW968
Connector	Feature	Specification Type 6	Type 6
Connector	reacure	(No IDE or PCI, add DDI+ USB3)	
		Min / Max	
A-B		System I/O	
A-B	PCI Express Lanes 0 - 5	1/6	3
A-B	LVDS Channel A	0 / 1	0 / 1 (Option : eDP or LVDS)
A-B	LVDS Channel B	0 / 1	1
A-B	eDP on LVDS CH A pins	0 / 1	1 / 0 (Option : eDP or LVDS)
A-B	VGA Port	0 / 1	0/1 (Option : DDI2 or VGA)
A-B	TV-Out	NA	NA
A-B	DDI 0	NA	NA
A-B ⁵	Serial Ports 1 - 2	0 / 2	2
A-B	CAN interface on SER1	0 / 1	0
A-B	SATA / SAS Ports	1 / 4	2
A-B	AC'97 / HDA Digital Interface	0 / 1	1
A-B	USB 2.0 Ports	4 / 8	8
A-B	USB Client	0 / 1	0
A-B	USB 3.0 Ports	NA	NA
A-B	LAN Port 0	1 / 1	1
A-B	Express Card Support	1 / 2	2
A-B	LPC Bus	1 / 1	1
A-B	SPI	1 / 2	1
A-B		System Manageme	ent
A-B ⁶	SDIO (muxed on GPIO)	0 / 1	0
A-B	General Purpose I/O	8 / 8	8
A-B	SMBus	1 / 1	1
A-B	I2C	1/1	1
A-B	Watchdog Timer	0 / 1	1
A-B	Speaker Out	1 / 1	1
A-B	External BIOS ROM Support	0 / 2	1
A-B	Reset Functions	1/1	1

- 5 Indicates 12V-tolerant features on former VCC_12V signals.
- 6 Cells in the connected columns spanning rows provide a rough approximation of features sharing connector pins.

Connector	Feature	COM Express Module Base Specification Type 6 (No IDE or PCI, add DDI+ USB3) Min / Max	DFI BW968 Type 6	
A-B		Power Manageme	nt	
A-B	Thermal Protection	0 / 1	1	
A-B	Battery Low Alarm	0 / 1	1	
A-B	Suspend/Wake Signals	0 / 3	1	
A-B	Power Button Support	1 / 1	1	
A-B	Power Good	1 / 1	1	
A-B	VCC_5V_SBY Contacts	4 / 4	4	
A-B ⁵	Sleep Input	0 / 1	1	
A-B ⁵	Lid Input	0 / 1	1	
A-B ⁵	Fan Control Signals	0 / 2	2	
A-B	Trusted Platform Modules	0 / 1	1	
A-B		Power		
A-B	VCC_12V Contacts	12 / 12	12	

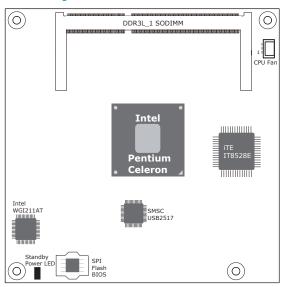
Module Pin-out - Required and Optional Features C-D Connector. PICMG® COM.0 Revision 2.1

Connector	Feature	COM Express Module Base Specification Type 6 (No IDE or PCI, add DDI+ USB3) Min / Max	DFI BW968 Type 6
C-D		System I/O	
	PCI Express Lanes 16 - 31	0 / 16	0
	PCI Express Graphics (PEG)	0 / 1	0
C-D ⁶	Muxed SDVO Channels 1 - 2	NA	NA
	PCI Express Lanes 6 - 15	0 / 2	0
	PCI Bus - 32 Bit	NA	NA
	PATA Port	NA	NA
	LAN Ports 1 - 2	NA	NA
	DDIs 1 - 3	0/3	1/2 (Option : DDI2 or VGA)
C-D ⁶	USB 3.0 Ports	0 / 4	2
C-D		Power	
C-D	VCC_12V Contacts	12 / 12	12

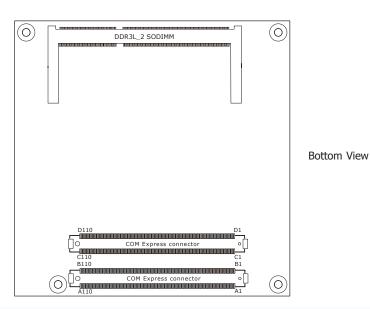
Chapter 2 Concept www.dfi.com

Chapter 3 - Hardware Installation

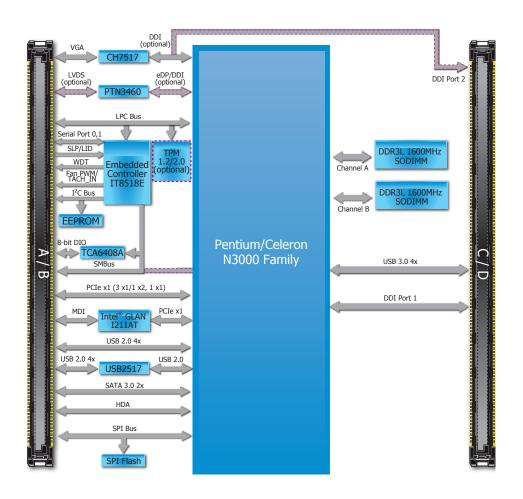
Board Layout



Top View



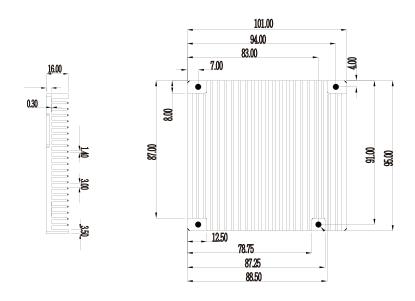
Block Diagram

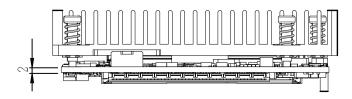


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Mechanical Diagram

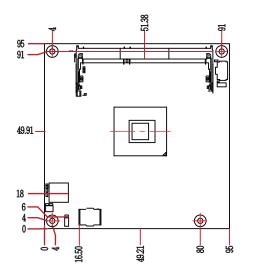
BW968 Module with Heat Sink



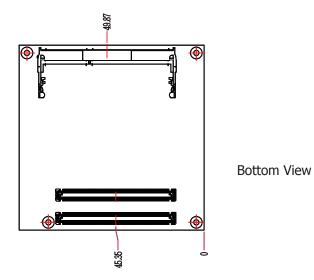


Side View of the Module with Heat Sink

BW968 Module



Top View



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Important:

Electrostatic discharge (ESD) can damage your board, processor, disk drives, add-in boards, and other components. Perform installation procedures at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

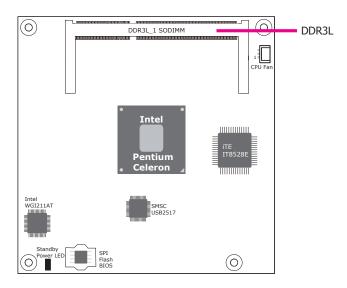
System Memory

The system board is equipped with 2GB/4GB/8GB DDR3L system memory onboard supporting 1600MHz, dual channel memory interface.

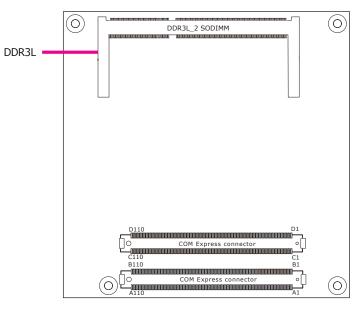


Important:

When the Standby Power LED is red, it indicates that there is power on the board. Power-off the PC then unplug the power cord prior to installing any devices. Failure to do so will cause severe damage to the board and components.



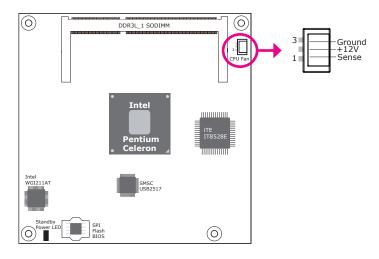
Top View



Bottom View

Connectors

CPU Fan Connector



Connect the CPU fan's cable connector to the CPU fan connector on the board. The cooling fan will provide adequate airflow throughout the chassis to prevent overheating the CPU and board components.

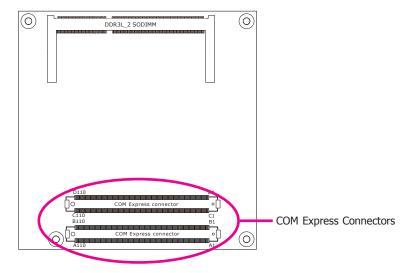
BIOS Setting

"Module Board H/W Monitor" submenu in the Advanced menu of the BIOS will display the current speed of the cooling fan. Refer to chapter 4 of the manual for more information.

COM Express Connectors

The COM Express connectors are used to interface the BW968 COM Express board to a carrier board. Connect the COM Express connectors (located on the solder side of the board) to the COM Express connectors on the carrier board.

Refer to the "Installing onto a Carrier Board" section for more information.



Refer to the following pages for the pin functions of these connectors.

COM Express Connectors

Row A		Row B		Row A		Row B		
A1	GND (FIXED)	B1	GND (FIXED)	A56	NA	B56	NA	
A2	GBE0 MDI3-	B2	GBE0 ACT#	A57	GND	B57	GPO2	
A3	GBE0 MDI3+	B3	LPC FRAME#	A58	NA	B58	NA	
A4	GBE0 LINK100#	B4	LPC AD0	A59	NA	B59	NA	
A5	GBE0 LINK1000#	B5	LPC AD1	A60	GND (FIXED)	B60	GND (FIXED)	
A6	GBE0 MDI2-	B6	LPC AD2	A61	PCIE TX2+	B61	PCIE RX2+	
A7	GBE0 MDI2+	B7	LPC_AD3	A62	PCIE TX2-	B62	PCIE RX2-	
A8	GBE0 LINK#	B8	NA	A63	GPI1	B63	GP03	
A9	GBE0 MDI1-	B9	NA	A64	PCIE TX1+	B64	PCIE RX1+	
A10	GBE0 MDI1+	B10	LPC CLK	A65	PCIE TX1-	B65	PCIE RX1-	
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#	
A12	GBE0 MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#(LAN_WAKE-)	
A13	GBE0_MDI0+	B13	SMB CK	A68	PCIE TX0+	B68	PCIE RX0+	
A14	NA	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-	
A15	SUS S3#	B15	SMB_ALERT#	A70	GND(FIXED)	B70	GND (FIXED)	
	_	_			` '		, ,	
A16	SATA0_TX+	B16	SATA1_TX+	A71	LVDS_A0+	B71	LVDS_B0+	
A17	SATA0_TX-	B17	SATA1_TX-	A72	LVDS_A0-	B72	LVDS_B0-	
A18	SUS_S4#	B18	SUS_STAT#	A73	LVDS_A1+	B73	LVDS_B1+	
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-	B74	LVDS_B1-	
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	LVDS_B2+	
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	LVDS_B2-	
A22	NA	B22	NA	A77	LVDS_VDD_EN	B77	LVDS_B3+	
A23	NA	B23	NA	A78	LVDS_A3+	B78	LVDS_B3-	
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN	
A25	NA	B25	NA	A80	GND (FIXED)	B80	GND (FIXED)	
A26	NA	B26	NA	A81	LVDS_A_CK+	B81	LVDS_B_CK+	
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	LVDS_B_CK-	
A28	(S)ATA_ACT#	B28	NA	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL	
A29	AC/HDA_SYNC	B29	AC/HDA _SDIN1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY	
A30	AC/HDA _RST#	B30	AC/HDA _SDIN0	A85	GPI3	B85	VCC_5V_SBY	
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY	
A32	AC/HDA _BITCLK	B32	SPKR	A87	eDP_HPD	B87	VCC_5V_SBY	
A33	AC/HDA _SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	BIOS_DIS1#	
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED	
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)	
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN	
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU	
A38	USB 6 7 OC#	B38	USB 4 5 OC#	A93	GPO0	B93	VGA HSYNC	
A39	USB4-	B39	USB5-	A94	SPI CLK	B94	VGA VSYNC	
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK	
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM PP	B96	VGA_I2C_DAT	
A42	USB2-	B42	USB3-	A97	NA .	B97	SPI_CS#	
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	RSVD	
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0 RX	B99	RSVD	
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)	
A46	USB0+	B46	USB1+	A101	SER1 TX	B101	FAN PWMOUT	
A47	VCC_RTC	B47	EXCD1 PERST#	A102	SER1_RX	B102	FAN TACHIN	
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	LID#	B103	SLEEP#	
A49	EXCD0_FERS1#	B49	SYS_RESET#	A104	VCC_12V	B103	VCC 12V	
A50	LPC_SERIRQ	B50	CB_RESET#	A104	VCC_12V	B104	VCC_12V	
A51	GND (FIXED)	B51	GND (FIXED)	A105	VCC_12V	B105	VCC_12V VCC 12V	
A52	NA	B52	NA	A100	VCC_12V VCC_12V	B100	VCC_12V	
_	NA NA	_	NA NA	_				
A53		B53		A108	VCC_12V	B108	VCC_12V	
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V	
A55	NA	B55	NA	A110	GND (FIXED)	B110	GND (FIXED)	

Row C		Row D		Row C		Row D	
C1	GND (FIXED)	D1	GND (FIXED)	C56	NA	D56	NA
C2	GND	D2	GND	C57	NA	D57	NA
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	NA	D58	NA
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	NA	D59	NA
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	NA	D61	NA
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	NA	D62	NA
C8	GND	D8	GND	C63	RSVD	D63	RSVD
C9	USB_SSRX2-	D9	USB_SSTX2-	C64	RSVD	D64	RSVD
C10	USB_SSRX2+	D10	USB_SSTX2+	C65	NA	D65	NA
C11	GND (FIXED)	D11	GND (FIXED)	C66	NA	D66	NA
C12	USB_SSRX3-	D12	USB_SSTX3-	C67	RSVD	D67	GND
C13	USB_SSRX3+	D13	USB_SSTX3+	C68	NA	D68	NA
C14	GND	D14	GND	C69	NA	D69	NA
C15	NA	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	NA	D16	DDI1_CTRLDATA_AUX-	C71	NA	D71	NA
C17	RSVD	D17	RSVD	C72	NA	D72	NA
C18	RSVD	D18	RSVD	C73	GND	D73	GND
C19	NA	D19	NA	C74	NA	D74	NA
C20	NA	D20	NA	C75	NA	D75	NA
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	NA	D22	NA	C77	RSVD	D77	RSVD
C23	NA	D23	NA	C78	NA	D78	NA
C24	DDI1_HPD	D24	RSVD	C79	NA	D79	NA
C25	NA	D25	RSVD	C80	GND (FIXED)	D80	GND (FIXED)
C26	NA	D26	DDI1_PAIR0+	C81	NA	D81	NA
C27	RSVD	D27	DDI1_PAIR0-	C82	NA	D82	NA
C28	RSVD	D28	RSVD	C83	RSVD	D83	RSVD
C29	NA	D29	DDI1_PAIR1+	C84	GND	D84	GND
C30	NA	D30	DDI1_PAIR1-	C85	NA	D85	NA
C31	GND (FIXED)	D31	GND (FIXED)	C86	NA	D86	NA
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+	C87	GND	D87	GND
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-	C88	NA	D88	NA
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	NA	D89	NA
C35	RSVD	D35	RSVD	C90	GND (FIXED)	D90	GND (FIXED)
C36	NA	D36	DDI1_PAIR3+	C91	NA	D91	NA
C37	NA	D37	DDI1_PAIR3-	C92	NA	D92	NA
C38	NA	D38	RSVD	C93	GND	D93	GND
C39	NA	D39	DDI2_PAIR0+	C94	NA	D94	NA
C40	NA	D40	DDI2_PAIR0-	C95	NA	D95	NA
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	NA	D42	DDI2_PAIR1+	C97	RSVD	D97	RSVD
C43	NA	D43	DDI2_PAIR1-	C98	NA	D98	NA
C44	NA	D44	DDI2_HPD	C99	NA	D99	NA
C45	RSVD	D45	RSVD	C100	GND (FIXED)	D100	GND (FIXED)
C46	NA	D46	DDI2_PAIR2+	C101	NA	D101	NA
C47	NA	D47	DDI2_PAIR2-	C102	NA	D102	NA
C48	RSVD	D48	RSVD	C103	GND	D103	GND
C49	NA	D49	DDI2_PAIR3+	C104	VCC_12V	D104	VCC_12V
C50	NA	D50	DDI2_PAIR3-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	NA	D52	NA	C107	VCC_12V	D107	VCC_12V
C53	NA	D53	NA	C108	VCC_12V	D108	VCC_12V
C54	NA	D54	NA	C109	VCC_12V	D109	VCC_12V
C55	NA	D55	NA	C110	GND (FIXED)	D110	GND (FIXED)

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COM Express Connectors Signals and Descriptions

Pin Types
I Input to the Module
O Output from the Module
I/O Bi-directional input / output signal
OD Open drain output

AC97/HDA Signals a	AC97/HDA Signals and Descriptions								
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968	Carrier Board	Description			
AC/HAD_RST#	A30	O CMOS	3.3V Suspend/3.3V		Connect to CODEC pin 11 RESET#	Reset output to CODEC, active low.			
AC/HDA_SYNC	A29	O CMOS	3.3V/3.3V		Connect to CODEC pin 10 SYNC	Sample-synchronization signal to the CODEC(s).			
AC/HDA_BITCLK	A32	I/O CMOS	3.3V/3.3V		Connect to CODEC pin 6 BIT_CLK	Serial data clock generated by the external CODEC(s).			
AC/HDA_SDOUT	A33	O CMOS	3.3V/3.3V		Connect to CODEC pin 5 SDATA_OUT	Serial TDM data output to the CODEC.			
AC/HDA_SDIN2	B28	I/O CMOS	3.3V Suspend/3.3V	NA					
AC/HDA_SDIN1	B29	I/O CMOS	3.3V Suspend/3.3V			Serial TDM data inputs from up to 2 CODECs.			
AC/HDA_SDIN0	B30	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODEC0 pin 8 SDATA_IN				

Gigabit Ethernet Si	Graphit Ethernet Signals and Descriptions									
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968	Carrier Board	Description				
GBEO_MDI0+	A13	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI0+/-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following:				
GBE0_MDI0-	A12	I/O Analog	3.3V max Suspend							
GBE0_MDI1+	A10	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI1+/-					
GBE0_MDI1-	A9	I/O Analog	3.3V max Suspend							
GBE0_MDI2+	A7	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI2+/-					
GBE0 MDI2-	A6	I/O Analog	3.3V max Suspend							
GBE0 MDI3+	A3	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI3+/-					
GBE0_MDI3-	A2	I/O Analog	3.3V max Suspend							
GBE0_ACT#	B2	OD CMOS	3.3V Suspend/3.3V		Connect to LED and recommend current limit resistor 150 Ω to 3.3VSB	Gigabit Ethernet Controller 0 activity indicator, active low.				
GBE0_LINK#	A8	OD CMOS	3.3V Suspend/3.3V		NC NC	Gigabit Ethernet Controller 0 link indicator, active low.				
GBE0_LINK100#	A4	OD CMOS	3.3V Suspend/3.3V			Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.				
GBE0_LINK100#	A4	OD CMOS	3.3V Suspend/3.3V		Connect to LED and recommend current limit resistor 150 Ω to 3.3VSB	Circles Falson of Controller 0 1000 Meit / one light indicator action law				
GBE0_LINK1000#	A5	OD CMOS	3.3V Suspend/3.3V		Connect to LED and recommend current limit resistor 150 Ω to 3.3VSB	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.				

SATA Signals and De	escriptions					
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968	Carrier Board	Description
SATA0_TX+	A16	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA0 Conn TX pin	Serial ATA or SAS Channel 0 transmit differential pair.
SATA0_TX-	A17	O SATA	AC coupled on Module	AC Coupling capacitor	CONNECT TO SATAO CONTIT TA PIN	Settal ATA 01 SAS Chainlei o Cansinic unicientali pair.
SATA0_RX+	A19	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA0 Conn RX pin	Serial ATA or SAS Channel 0 receive differential pair.
SATA0_RX-	A20	I SATA	AC coupled on Module	AC Coupling capacitor	connect to SATAO conn KX pin	Serial ATA OF SAS Charmer of receive differential pair.
SATA1_TX+	B16	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA1 Conn TX pin	Serial ATA or SAS Channel 1 transmit differential pair.
SATA1_TX-	B17	O SATA	AC coupled on Module	AC Coupling capacitor	ediffect to SATA2 confit TX pin	Schal ATA 61 575 channel I danshir dinectical pair.
SATA1_RX+	B19	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA1 Conn RX pin	Serial ATA or SAS Channel 1 receive differential pair.
SATA1_RX-	B20	I SATA	AC coupled on Module	AC Coupling capacitor	CONNECT TO SMALE CONNECT ON PIN	Serial ATA 01 SAS Chailler I Teceive differential pair.
SATA2_TX+	A22	O SATA	AC coupled on Module	NA	Connect to SATA2 Conn TX pin	Serial ATA or SAS Channel 2 transmit differential pair.
SATA2_TX-	A23	O SATA	AC coupled on Module	NA	connect to SATAZ CONN TA pin	Schar ATA of SAS charmed 2 dansmic americana pair.
SATA2_RX+	A25	I SATA	AC coupled on Module	NA	Connect to SATA2 Conn RX pin	Serial ATA or SAS Channel 2 receive differential pair.
SATA2_RX-	A26	I SATA	AC coupled on Module	NA	connect to SATA2 conn for pin	Schal ATA G. SAS channel 2 receive direction pair.
SATA3_TX+	B22	O SATA	AC coupled on Module	NA		Serial ATA or SAS Channel 3 transmit differential pair.
SATA3_TX-	B23	O SATA	AC coupled on Module	NA		Schal ATA 61 545 channel 5 danshir direction pair.
SATA3_RX+	B25	I SATA	AC coupled on Module	NA		Serial ATA or SAS Channel 3 receive differential pair.
SATA3_RX-	B26	I SATA	AC coupled on Module	NA		·
ATA_ACT#	A28	I/O CMOS	3.3V / 3.3V	PU 10K to 3.3V	Connect to LED and recommend current limit resistor 220Ω to 3.3V	ATA (parallel and serial) or SAS activity indicator, active low.

Chapter 3

PCI Express Lanes Si	anals and Descri	ptions							
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968	Carrier Board	Description			
PCIE_TX0+	A68	O PCIE	AC coupled on Module	AC Coupling capacitor	ng capacitor Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 0			
PCIE_TX0-	A69	UPCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI express differential Transmit Pairs 0			
PCIE_RX0+	B68	I PCIE	AC coupled off Module		Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 0			
PCIE_RX0-	B69	I FCIL	AC coupled on Flodule		Slot - Connect to PCIE Conn pin	FCI Express Differential Receive Fails 0			
PCIE_TX1+	A64	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 1			
PCIE_TX1-	A65	OFCIL	Ac coupled on Module	AC Coupling capacitor		ret Express billerential Transmit rails 1			
PCIE_RX1+	B64	I PCIE	AC coupled off Module		Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 1			
PCIE_RX1-	B65	I FCIL	AC coupled on Flodule		Slot - Connect to PCIE Conn pin	FCI Express Differential Receive Fails 1			
PCIE_TX2+	A61	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 2			
PCIE_TX2-	A62	OFCIL	Ac coupled on Module	AC Coupling capacitor		ret Express billerential Transmit rails 2			
PCIE_RX2+	B61	I PCIE	AC coupled off Module		Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 2			
PCIE_RX2-	B62	TTOL	Ac coupied on Floduic		Slot - Connect to PCIE Conn pin	r of Express bireferration receive runs 2			
PCIE_TX3+	A58	O PCIE	AC coupled on Module	NA	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 3			
PCIE_TX3-	A59	OTCIL	Ac coupied on Floduic	NA		. Cr. Express Surferenda Transmit. and S			
PCIE_RX3+	B58	I PCIE	AC coupled off Module	NA	Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 3			
PCIE_RX3-	B59	I I CIL	Ac coupied on Floudic	NA	Slot - Connect to PCIE Conn pin				
PCIE_TX4+	A55	O PCIE	AC coupled on Module	NA	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 4			
PCIE_TX4-	A56	OTCIL	Ac coupied on Floduic	NA		. a Express sure creation realisment and r			
PCIE_RX4+	B55	I PCIE	AC coupled off Module	NA	Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 4			
PCIE_RX4-	B56	I I CIL	Ac coupied on Floudic	NA	Slot - Connect to PCIE Conn pin	. or Express sure creating receive rains .			
PCIE_TX5+	A52	O PCIE	AC coupled on Module	NA	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 5			
PCIE_TX5-	A53	OTCIL	Ac coupied on Floudic	NA		r de Express principalism ransmit rans 5			
PCIE_RX5+	B52	I PCIE	AC coupled off Module	NA	Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 5			
PCIE_RX5-	B53	I T OIL	ne coupied on module	NA	Slot - Connect to PCIE Conn pin	- of Express sincernal recent runs s			
PCIE_TX6+	D19	O PCIF	AC coupled on Module	NA	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 6			
PCIE_TX6-	D20	OTCIL	Ac coupied on Floudic	NA		rea Express billerential Transmit rais 0			
PCIE_RX6+	C19	I PCIE	AC coupled off Module	NA	Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 6			
PCIE_RX6-	C20	I T OIL	ne coupied on module	NA	Slot - Connect to PCIE Conn pin	- OZ ENPLOS SINCECITAL NECESTO I UNIO O			
PCIE_TX7+	D22	O PCIE	AC coupled on Module	NA	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 7			
PCIE_TX7-	D23	0.012	no coupled on Floudic	NA		- de Express surcicidad i reasona i ano /			
PCIE_RX7+	C22	I PCIE	AC coupled off Module	NA	Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 7			
PCIE_RX7-	C23		on module	NA	Slot - Connect to PCIE Conn pin	r of Express birterental receive runs /			
PCIE0_CK_REF+	A88	O PCIE	PCIE		Connect to PCIE device, PCIe CLK Buffer or slot	Reference clock output for all PCI Express and PCI Express Graphics			
PCIE0_CK_REF-	A89	O PCIE	ruc		Connect to FCIE device, PCIE CLR Duffer Of Siot	lanes.			

Chapter 3

PEG Signals and Des	scriptions					
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968	Carrier Board	Description
PEG_TX0+ PEG_TX0-	D52 D53	O PCIE	AC coupled on Module	NA NA		PCI Express Graphics transmit differential pairs 0
PEG_TXU- PEG_RX0+	C52			NA NA		
PEG_RX0-	C53	I PCIE	AC coupled off Module	NA NA		PCI Express Graphics receive differential pairs 0
PEG_TX1+	D55	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 1
PEG_TX1-	D56 C55			NA NA		
PEG_RX1+ PEG_RX1-	C56	I PCIE	AC coupled off Module	NA NA		PCI Express Graphics receive differential pairs 1
PEG_TX2+	D58	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 2
PEG_TX2-	D59	O PCIE	AC coupled on Module	NA		PCI Express Graphics dansinic differential pairs 2
PEG_RX2+ PEG_RX2-	C58 C59	I PCIE	AC coupled off Module	NA NA		PCI Express Graphics receive differential pairs 2
PEG_TX3+	D61			NA NA		
PEG_TX3-	D62	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 3
PEG_RX3+	C61	I PCIE	AC coupled off Module	NA NA		PCI Express Graphics receive differential pairs 3
PEG_RX3- PEG_TX4+	C62 D65			NA NA		
PEG_TX4-	D66	O PCIE	AC coupled on Module	NA NA		PCI Express Graphics transmit differential pairs 4
PEG_RX4+	C65	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 4
PEG_RX4-	C66 D68	TTGE	Ac coupled on Floudic	NA NA		Tel Express Graphics receive uniterential pairs 1
PEG_TX5+ PEG_TX5-	D68 D69	O PCIE	AC coupled on Module	NA NA		PCI Express Graphics transmit differential pairs 5
PEG_RX5+	C68	I PCIE	AC	NA NA		DCT Comment Complete annual of differential points C
PEG_RX5-	C69	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 5
PEG_TX6+ PEG_TX6-	D71 D72	O PCIE	AC coupled on Module	NA NA		PCI Express Graphics transmit differential pairs 6
PEG_RX6+	C71			NA NA		
PEG_RX6-	C72	I PCIE	AC coupled off Module	NA NA		PCI Express Graphics receive differential pairs 6
PEG_TX7+	D74	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 7
PEG_TX7- PEG_RX7+	D75 C74			NA NA		
PEG_RX7+	C75	I PCIE	AC coupled off Module	NA NA		PCI Express Graphics receive differential pairs 7
PEG_TX8+	D78	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 8
PEG_TX8-	D79	OTGE	Ac coupled on Floudic	NA		1 C2 EXPLOSS Graphics d'ansimic differential pairs 0
PEG_RX8+ PEG_RX8-	C78 C79	I PCIE	AC coupled off Module	NA NA		PCI Express Graphics receive differential pairs 8
PEG_TX9+	D81	O PCIE	AC coupled on Module	NA NA		DCI Frances Consider to a series to the series of
PEG_TX9-	D82	U PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 9
PEG_RX9+	C81 C82	I PCIE	AC coupled off Module	NA NA		PCI Express Graphics receive differential pairs 9
PEG_RX9- PEG_TX10+	D85			NA NA		
PEG_TX10-	D86	O PCIE	AC coupled on Module	NA NA		PCI Express Graphics transmit differential pairs 10
PEG_RX10+	C85	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 10
PEG_RX10- PEG_TX11+	C86 D88		ne coupled on riodale	NA NA		Tat Express Graphics receive uniterated pairs 25
PEG_TX11+	D89	O PCIE	AC coupled on Module	NA NA		PCI Express Graphics transmit differential pairs 11
PEG_RX11+	C88	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 11
PEG_RX11-	C89	1 FCIL	Ac coupled on module	NA NA		1 of Express Graphics receive differential pails 11
PEG_TX12+ PEG_TX12-	D91 D92	O PCIE	AC coupled on Module	NA NA		PCI Express Graphics transmit differential pairs 12
PEG_RX12+	C91	I DCIE	AC	NA NA		DCI Forman Complian manifest differential pains 12
PEG_RX12-	C92	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 12
PEG_TX13+	D94 D95	O PCIE	AC coupled on Module	NA NA		PCI Express Graphics transmit differential pairs 13
PEG_TX13- PEG_RX13+	C94			NA NA		
PEG_RX13-	C95	I PCIE	AC coupled off Module	NA NA		PCI Express Graphics receive differential pairs 13
PEG_TX14+	D98	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 14
PEG_TX14- PEG_RX14+	D99 C98		pbdaic	NA NA		P P
PEG_RX14+ PEG_RX14-	C98	I PCIE	AC coupled off Module	NA NA	+	PCI Express Graphics receive differential pairs 14
PEG_TX15+	D101	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 15
PEG_TX15-	D102	UPGE	Ac coupled on module	NA		ret Express Graphics danstill differential pails 15
PEG_RX15+ PEG_RX15-	C101 C102	I PCIE	AC coupled off Module	NA NA		PCI Express Graphics receive differential pairs 15
						PCI Express Graphics lane reversal input strap. Pull low on the Carrier
PEG_LANE_RV#	D54	I CMOS	3.3V / 3.3V	PU 10K to 3.3V		board to reverse lane order.

ExpressCard Signals and Descriptions									
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968	Carrier Board	Description			
EXCD0_CPPE#	A49					PCI ExpressCard: PCI Express capable card request, active low, one per			
EXCD1_CPPE#	B48	I CMOS	3.3V /3.3V			card			
EXCD0_PERST#	A48	O CMOS	3.3V /3.3V			PCI ExpressCard: reset, active low, one per card			
EXCD1_PERST#	B47	O CMOS	3.34 /3.34			PCI ExpressCard. Teset, active low, one per card			

DDI Signals and Description	ne						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968	Carrier Board	Description	
DDI1 PAIR0+/SDVO1 RED+	D26			247300	Connect AC Coupling Capacitors 0.1uF to Device		
DDI1 PAIRO-/SDVO1 RED-	D27	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 0 differential pairs/Serial Digital Video B red output differential pair	
DI1_PAIR1+/SDVO1_GRN+	D29				Connect AC Coupling Capacitors 0.1uF to Device		
DI1_PAIR1+/SDVO1_GRN-	D30	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 1 differential pairs/Serial Digital Video B green output differential pair	
DI1 PAIR2+/SDVO1_GRV	D32				Connect AC Coupling Capacitors 0.1uF to Device		
	D33	O PCIE	AC coupled off Module			DDI 1 Pair 2 differential pairs/Serial Digital Video B blue output differential pair	
DI1_PAIR2-/SDVO1_BLU- DI1_PAIR3+/SDVO1_CK+	D36				Connect AC Coupling Capacitors 0.1uF to Device		
		O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 3 differential pairs/Serial Digital Video B clock output differential pair.	
DI1_PAIR3-/SDVO1_CK-	D37	1 1			Connect AC Coupling Capacitors 0.1uF to Device		
DI1_PAIR4+/SDVO1_INT+	C25	I PCIE	AC coupled off Module	NA		Serial Digital Video B interrupt input differential pair.	
DI1_PAIR4-/SDVO1_INT-	C26	11.012	ne coupled on Housie	NA		Serial Signal Video S Interrupt input american pair.	
DI1_PAIR5+/SDVO1_TVCLKIN+	C29	I PCIE	AC coupled off Module	NA		Serial Digital Video TVOUT synchronization clock input differential pair.	
DI1_PAIR5-/SDVO1_TVCLKIN-	C30	I FCIL	Ac coupled on Floudie	NA		Serial Digital video 1 voor Synchronization dock input differential pair.	
DI1_PAIR6+/SDVO1_FLDSTALL+	C15	I PCIE	AC	NA		Cariel Disited Mides Field Chall insuch differential anim	
DI1_PAIR6-/SDVO1_FLDSTALL-	C16	I PCIE	AC coupled off Module	NA		Serial Digital Video Field Stall input differential pair.	
				PD 100K to GND			
		I/O PCIE	AC coupled on Module	(S/W IC between Rpu/PCH)	Connect to DP AUX+	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect	
DI1_CTRLCLK_AUX+/SDVO1_CTRLCLK	DIE						
DII_CTRECER_AUX+/3DVOI_CTRECER	. 1013	I/O OD CMOS	3.3V / 3.3V	PU 4.7K to 3.3V, PD 100K to GND (S/W IC between Rpu/Rpd	Connect to HDMI/DVI I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	
				resistor)			
		I/O PCIE	AC coupled on Module	PU 100K to 3.3V	Connect to DP AUX-	DP AUX- function if DDI1_DDC_AUX_SEL is no connect	
		I/O FCIE	ac coupled on module	(S/W IC between Rpu/PCH)	CONNECT TO DE MOX-	or Mon-Iditation in Doll-Doc-Mon-See is 110 contract	
DI1_CTRLCLK_AUX-/SDVO1_CTRLDATA	A D16			PU 4.7K to 3.3V/PU 100K to 3.3V			
		I/O OD CMOS	3.3V / 3.3V	(S/W IC between 4.7K/100K	Connect to HDMI/DVI I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	
		1/0 00 01103	3.34 / 3.3V	resistor)	Connect to Horizott Ize CINEDATA		
	1			,			
DI1_HPD	C24	I CMOS	3.3V / 3.3V	PD 100K to GND	PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect	
	-						
						Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX	
DIA DDC AUY CEL	D24	T CMOC	2 21/ / 2 21/	DD 1M: CND	DIT 100K F- 3 3/ 5-* DDC(HDM1/D/4)	DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm	
DI1_DDC_AUX_SEL	D34	I CMOS	3.3V / 3.3V	PD 1M to GND	PU 100K to 3.3V for DDC(HDMI/DVI)	resistor to configure the DDI[n]_AUX pair as the DDC channel.	
						Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort	
						SSI(II_DDS_AON_SEE STORING OF CONTINUES OF DISTRIBUTED	
DI2_PAIR0+	D39	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 0 differential pairs	
DI2_PAIRO-	D40	OPCIE	AC Coupled on Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pail 0 differential pails	
DI2_PAIR1+	D42	o pers			Connect AC Coupling Capacitors 0.1uF to Device	207.2 2 1.4 100 11.1 1	
DI2_PAIR1-	D43	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 1 differential pairs	
DI2 PAIR2+	D46				Connect AC Coupling Capacitors 0.1uF to Device		
DI2 PAIR2-	D47	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 2 differential pairs	
DI2_PAIR3+	D49	+	+		Connect AC Coupling Capacitors 0.1uF to Device		
DI2_PAIR3-	D50	O PCIE	AC coupled off Module			DDI 2 Pair 3 differential pairs	
NIT LUIVI-	טכט	_		DD 100K to CND	Connect AC Coupling Capacitors 0.1uF to Device		
		I/O PCIE	AC coupled on Module	PD 100K to GND	Connect to DP AUX+	DP AUX+ function if DDI2_DDC_AUX_SEL is no connect	
			,	(S/W IC between Rpu/PCH)			
DI2_CTRLCLK_AUX+	C32			PU 2.2K to 3.3V, PD 100K to GND			
		I/O OD CMOS	3.3V / 3.3V	(S/W IC between Rpu/Rpd	Connect to HDMI/DVI I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high	
				resistor)	· ·	= = = = = = = = = = = = = = = = = = = =	
	+		+	PU 100K to 3.3V			
		I/O PCIE	AC coupled on Module	(S/W IC between Rpu/PCH)	Connect to DP AUX-	DP AUX- function if DDI2_DDC_AUX_SEL is no connect	
DIS CTRICIK ALIV	C22		1	(3/ W 1C between Kpu/PCn)	Connect to HDMI/DW T2C CTRI DATA		
DI2_CTRLCLK_AUX-	C33	1/0 00 01/05	2 21/ / 2 21/	PU 2.2K to 3.3V/PU 100K to 3.3V		LIDMI/DVI 12C CTDI DATA & DDI2 DDC ALW CEL : " II II : I	
		I/O OD CMOS	3.3V / 3.3V	(S/W IC between 4.7K/100K	Connect to HDMI/DVI I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high	
				resistor)			
DI2_HPD	D44	I CMOS	3.3V / 3.3V	PD 100K to GND	PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect	
						Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX	
						DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm	
DI2_DDC_AUX_SEL	C34	I CMOS	3.3V / 3.3V	PD 1M to GND	PU 100K to 3.3V for DDC(HDMI/DVI)	resistor to configure the DDI[n] AUX pair as the DDC channel.	
						resistor to confingere the DDI(n)_AOA pair as the DDC chainner.	
						Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort	
DI3_PAIR0+	C39	O DCIE	AC	NA		DDI 3 Driv 0 differential arise	
DI3 PAIRO-	C40	O PCIE	AC coupled off Module	NA NA		DDI 3 Pair 0 differential pairs	
DI3 PAIR1+	C42			NA NA			
DI3_PAIR1-	C43	O PCIE	AC coupled off Module	NA NA		DDI 3 Pair 1 differential pairs	
DI3_PAIR1- DI3_PAIR2+	C43		1	NA NA			
		O PCIE	AC coupled off Module	NA NA		DDI 3 Pair 2 differential pairs	
DI3_PAIR2-	C47		 			*	
DI3_PAIR3+	C49	O PCIE	AC coupled off Module	NA		DDI 3 Pair 3 differential pairs	
DI3_PAIR3-	C50		,	NA		·	
		I/O PCIE	AC coupled on Module	NA		DP AUX+ function if DDI3_DDC_AUX_SEL is no connect	
		-70 1 CIL	, to coupled on Houtile	11/3		S. ASA. GREAT II DEED_DDG_NOA_SEE IS NO CONNECT	
DI3_CTRLCLK_AUX+	C36			·			
		I/O OD CMOS	3.3V / 3.3V	NA		HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high	
			1 '				
		_					
		I/O PCIE	AC coupled on Module	NA		DP AUX- function if DDI3_DDC_AUX_SEL is no connect	
DI3_CTRLCLK_AUX-	C37						
_		I/O OD CMOS	3.3V / 3.3V	NA		HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high	
		*					
DI3_HPD	C44	I CMOS	3.3V / 3.3V	NA		DDI Hot-Plug Detect	
·				· · · · · · · · · · · · · · · · · · ·		Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX	
	1		1			DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm	
DI3_DDC_AUX_SEL	C38	I CMOS	3.3V / 3.3V	NA			
DI3_DDC_AUX_SEL	C38	I CMOS	3.3V / 3.3V	NA		resistor to configure the DDI[n]_AUX pair as the DDC channel. [Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort	

Chapter 3

USB0+ A USB0- A USB1- E USB1- E USB2- A USB2- A USB2- A USB2- A USB2- A USB2- A USB2- B E USB2- B USB3- B E	15				
USB0+ A USB0- A USB1- E USB1- E USB2- A USB2- A USB2- A USB2- A USB2- A USB2- A USB2- B E USB2- B USB3- B E	Pin# Module Pi	Type Pwr Rail /Tolerance	BW968	Carrier Board	Description
USB1+ E USB1- E USB2+ A USB2- A USB3+ E	A 4C		BW300	Connect 90 \(\Omega \) @100MHz Common Choke in series and ESD suppressors to GND to USB	
USB1-	A45 I/O USB	3.3V Suspend/3.3V		connector	USB differential pairs 0
USB2+	B46 I/O USB	3.3V Suspend/3.3V		Connect 90 @100MHz Common Choke in series and ESD suppressors to GND to USB	USB differential pairs 1
USB2- USB3+	845	3.5 v Sasperia, 3.5 v		connector	oob american pano 1
USB3+	A43 I/O USB	3.3V Suspend/3.3V		Connect 90 \text{\Omega} \text{\Omega} 100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 2
	BN3			Connect 90 \Q @100MHz Common Choke in series and ESD suppressors to GND to USB	
	B42 I/O USB	3.3V Suspend/3.3V		connector	USB differential pairs 3
	A40 I/O USB	3.3V Suspend/3.3V		Connect 90 \(\Omega \) @100MHz Common Choke in series and ESD suppressors to GND to USB	USB differential pairs 4
	A39	3.5 v Sasperia, 3.5 v		connector	oob american pano 1
	B40 I/O USB	3.3V Suspend/3.3V		Connect 90 @ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 5
	A 2.7			Connect 90 \(\Omega \) @100MHz Common Choke in series and ESD suppressors to GND to USB	
	A36 I/O USB	3.3V Suspend/3.3V		connector	USB differential pairs 6
	B37 I/O USB	3.3V Suspend/3.3V		Connect 90 \(\Omega \) @100MHz Common Choke in series and ESD suppressors to GND to USB	USB differential pairs 7
	B36 I/O 035 B44 I CMOS	3.3V Suspend/3.3V	PU 10k to 3V3SB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_2_3_OC#	A44 I CMOS	3.3V Suspend/3.3V	PU 10k to 3V3SB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_4_5_OC#	B38 I CMOS	3.3V Suspend/3.3V	PU 10k to 3V3SB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
	A38 I CMOS	3.3V Suspend/3.3V	PU 10k to 3V3SB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_SSTX0-	D4 O PCIE	AC coupled on Module	AC Coupling capacitor AC Coupling capacitor	Connect 90 \(\Omega \) @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
	C3 I PCIE	AC coupled off Modul		Connect 90 \Omega \@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
	D7 D6 O PCIE	AC coupled on Module	AC Coupling capacitor AC Coupling capacitor	Connect 90 @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSRX1+	C7 C6 I PCIE	AC coupled off Modul		Connect 90 \@100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSTX2+	D10 D9 O PCIE	AC coupled on Module	AC Coupling capacitor AC Coupling capacitor	Connect 90 Q @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSRX2+	C10 I PCIE	AC coupled off Modul	ne coupling capacitor	Connect 90 ♀ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
	D13		AC Coupling capacitor	Connect 90 \(\Omega \) @100MHz Common Choke in series and ESD suppressors to GND to USB	
	D12 O PCIE	AC coupled on Module	AC Coupling capacitor	connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
	C13 I PCIE	AC coupled off Modul	, ,	Connect 90 \(\Omega \) @100MHz Common Choke in series and ESD suppressors to GND to USB	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX3-	C12	Ac coupied on Floudi		connector	Padadonal receive signal differential pairs for the superspeed 655 data path.
LVDC Cianala and Description					
LVDS Signals and Description	Pin# Module Pi	Type Pwr Rail /Tolerance	BW968	Carrier Board	Description
	A71	,,		Connect to LVDS connector	LVDS Channel A differential pairs
LVU3_AU+	A72 O LVDS	LVDS			Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/ LVDS_A_CK+/-,
	A73	11/06		Connect to LVDS connector	—LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer
LVDS_A0-		LVDS			on-board
LVDS_A0-	A74				
LVDS_A0-	Δ75			Connect to LVDS connector	
LVDS_A0-		LVDS		Connect to LVDS connector	
LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A2- LVDS_A2- LVDS_A2-	A75 O LVDS A76			Connect to LVDS connector Connect to LVDS connector	
LVDS_A0- # LVDS_A1+ # LVDS_A1- # LVDS_A2+ LVDS_A2- LVDS_A2- LVDS_A3+ # A	A75 O LVDS A76 O LVDS	LVDS LVDS			
LVDS_A0- LVDS_A1+ LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3- LVDS_A3- LVDS_ACK+ LVDS_ACK+	A75 O LVDS A76 O LVDS A78 O LVDS A79 O LVDS	LVDS			Wee Ground A ##www.intent
LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3- LVDS_A3- LVDS_A CK+ LVDS_A CK- LVDS_	A75 O LVDS A76 O LVDS A78 O LVDS A79 O LVDS A81 O LVDS			Connect to LVDS connector Connect to LVDS connector	LVDS Channel A differential clock
LVDS_A0- LVDS_A1+ LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3- LVDS_A A- LVDS_A CK+ LVDS_A CK- LVDS_B0+ E	A75 O LVDS A76 O LVDS A78 O LVDS A79 O LVDS A81 O LVDS B71 O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential clock
LVDS_A0- LVDS_A1+ LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3- LVDS_A3- LVDS_A CK+ LVDS_A CK- LVDS_B0+ LVDS_B0- E	A75 O LVDS A76 O LVDS A78 O LVDS A79 O LVDS A81 O LVDS B71 O LVDS B72 O LVDS	LVDS LVDS LVDS		Connect to LVDS connector Connect to LVDS connector Connect to LVDS connector	LVDS Channel B differential pairs
LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3- LVDS_A3- LVDS_A CK+ LVDS_B0+ LVDS_B0- LVDS_B0- LVDS_B0- LVDS_B0- LVDS_B1+ LVDS_B1+ LVDS_A0- LVDS_B1+ L	A75 O LVDS A76 O LVDS A78 O LVDS A79 O LVDS A81 O LVDS B71 O LVDS	LVDS LVDS		Connect to LVDS connector Connect to LVDS connector	_LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/ LVDS_A_CK+/-,
LVDS_A0- LVDS_A1+ LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3- LVDS_A3- LVDS_A CK+ LVDS_B0+ LVDS_B0+ LVDS_B1- LVDS_B1- LVDS_B1- LVDS_B1- LVDS_B2+ LVDS_B2+ LVDS_B2+ LVDS_B2+ LVDS_B2+ LVDS_B2+ LVDS_B2+ LVDS_B1+ LVDS_B2+ L	A75 O LVDS A76 O LVDS A78 O LVDS A79 O LVDS A81 O LVDS B71 O LVDS B72 O LVDS B73 O LVDS B74 O LVDS B75 O LVDS	LVDS LVDS LVDS LVDS		Connect to LVDS connector Connect to LVDS connector Connect to LVDS connector	- LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/ LVDS_A_CK+/-, - LVDS_B_CK+/-) shall have 1000 terminations across the pairs at the destination. These
LVDS_A0- LVDS_A1+ LVDS_A1+ LVDS_A1+ LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3- LVDS_A3- LVDS_A CK+ LVDS_A CK- LVDS_B0- LVDS_B0- LVDS_B1- LVDS_B1- LVDS_B2- LVDS_B2- LVDS_B2- LVDS_B2- LVDS_B2- LVDS_B2- LVDS_B2- LVDS_B1- LVDS_B2-	A75 O LVDS A76 O LVDS A78 O LVDS A79 O LVDS A81 O LVDS B71 O LVDS B72 O LVDS B73 O LVDS B73 O LVDS B75 O LVDS B75 O LVDS	LVDS LVDS LVDS		Connect to LVDS connector	_LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/ LVDS_A_CK+/-,
LVDS_A0- LVDS_A1+ LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2+ LVDS_A3+ LVDS_A3- LVDS_A3- LVDS_A3- LVDS_B0+ LVDS_B0+ LVDS_B0+ LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2+ LVDS_B2- LVDS_B2- LVDS_B2- LVDS_B3+ E	A75 A76 O LVDS A78 O LVDS A79 O LVDS A81 A82 O LVDS B71 B72 B73 O LVDS B73 O LVDS B74 B75 B75 O LVDS B76 B77 O LVDS	LVDS LVDS LVDS LVDS		Connect to LVDS connector Connect to LVDS connector Connect to LVDS connector Connect to LVDS connector	LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-, LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 10Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer
LVDS_A0- LVDS_A1+ LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3- LVDS_A3- LVDS_A CK+ LVDS_B0- LVDS_B0- LVDS_B1- LVDS_B1- LVDS_B2- LVDS_B2- LVDS_B3- L	A75 A76 O LVDS A78 O LVDS A79 O LVDS A81 A82 O LVDS B71 B72 B73 O LVDS B73 O LVDS B74 B75 B76 O LVDS B77 B78 B78 B78 B79 B78 B79 B78 B79 B79 B78 B79	LVDS LVDS LVDS LVDS LVDS LVDS LVDS		Connect to LVDS connector	LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/ LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board
LVDS_A0- LVDS_A1+ LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3- LVDS_A3- LVDS_A CK+ LVDS_A CK- LVDS_B0- LVDS_B0- LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3+ LVDS_B3-	A75 A76 O LVDS A78 O LVDS A79 A81 A82 O LVDS B71 B72 O LVDS B73 B74 B75 B75 O LVDS B76 B77 O LVDS B78 B78 B78 B79 O LVDS	LVDS LVDS LVDS LVDS LVDS LVDS		Connect to LVDS connector	LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-, LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 10Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer
LVDS_A0- LVDS_A1+ LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3- LVDS_A- LVDS_A- LVDS_A- LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1+ LVDS_B2+ LVDS_B2- LVDS_B2- LVDS_B3+ LVDS_B3+ LVDS_B3+ LVDS_B3- LVDS_B1- LVDS_B1- LVDS_B1- LVDS_B2- LVDS_B3- LVDS_B3- LVDS_B3- LVDS_B1- LVDS_B3- LVDS_B1- LVDS_B1- LVDS_B3- LVDS_B1- LVDS_B3- LVDS_B1- LVDS_B	A75 A76 O LVDS A78 O LVDS A79 O LVDS A81 A82 O LVDS B71 B72 B73 O LVDS B73 O LVDS B74 B75 B76 O LVDS B77 B78 B78 B78 B79 B78 B79 B78 B79 B79 B78 B79	LVDS LVDS LVDS LVDS LVDS LVDS LVDS LVDS		Connect to LVDS connector	- LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/ LVDS_A_CK+/-, - LVDS_B_CK+/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer - on-board LVDS Channel B differential clock
LVDS_A0- LVDS_A1+ LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2+ LVDS_A3- LVDS_A3- LVDS_A3- LVDS_ACK+ LVDS_A CK+ LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2- LVDS_B3- LVDS_B3- LVDS_B3- LVDS_B3- LVDS_B1- LVDS_B1- LVDS_B1- LVDS_B2- LVDS_B3- LVDS_B3- LVDS_B3- LVDS_BCK+ LVDS_B CK+ LVDS_B LVB- LVB- LVDS_B LVB- L	A75 A76 A78 O LVDS A79 A81 A82 O LVDS B71 B72 B73 B73 B74 B75 B76 B76 B77 B78 B78 B81 B81 O LVDS B81 B81 O LVDS B81 B81 O LVDS B81 B82 O LVDS B81 B82 O LVDS B81 B82 O LVDS B77 O CMOS B79 O CMOS	LVDS LVDS LVDS LVDS LVDS LVDS LVDS LVDS LVDS 3.3V / 3.3V / 3.3V / 3.3V		Connect to LVDS connector	LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/ LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board LVDS Channel B differential clock LVDS panel power enable LVDS panel backlight enable
LVDS_A0- LVDS_A1+ LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3- LVDS_A3- LVDS_A0- LVDS_A0- LVDS_B0- LVDS_B0- LVDS_B1- LVD	A75 O LVDS A78 O LVDS A79 O LVDS A79 O LVDS A81 O LVDS B71 O LVDS B73 O LVDS B73 O LVDS B75 O LVDS B76 O LVDS B77 O LVDS B77 O LVDS B78 O LVDS B81 O LVDS B81 O LVDS B82 O LVDS B82 O LVDS B83 O CMOS B79 O CMOS B83 O CMOS	LVDS LVDS LVDS LVDS LVDS LVDS LVDS LVDS LVDS 3.3V / 3.3V / 3.3V / 3.3V / 3.3V / 3.3V		Connect to LVDS connector Connect to enable control of LVDS panel power circuit Connect to enable control of LVDS panel backlight power circuit. Connect to brightness control of LVDS panel backlight power circuit.	LVDS Channel B differential pairs Ther LVDS fat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-, LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 1000 terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board LVDS Channel B differential clock LVDS panel backlight onable LVDS panel backlight brightness control
LVDS_A0- LVDS_A1- LVDS_A1+ LVDS_A1- LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3- LVDS_A_CK- LVDS_A_CK- LVDS_B0- LVDS_B0- LVDS_B1- LVDS_B1- LVDS_B2- LVDS_B3+ LVDS_B3- LVDS_B3- LVDS_B3- LVDS_B3- LVDS_B1- LVDS_B1- LVDS_B1- LVDS_B1- LVDS_B1- LVDS_B2- LVDS_B3- LVDS_B3- LVDS_B3- LVDS_B3- LVDS_B3- LVDS_B3- LVDS_B3- LVDS_B1- LVDS_BCK- LVDS_BCC- LVDS_BCK- LVDS_BCC- LVDS_BCK- LVDS_BC	A75 A76 A78 O LVDS A79 A81 A82 O LVDS B71 B72 B73 B73 B74 B75 B76 B76 B77 B78 B78 B81 B81 O LVDS B81 B81 O LVDS B81 B81 O LVDS B81 B82 O LVDS B81 B82 O LVDS B81 B82 O LVDS B77 O CMOS B79 O CMOS	LVDS LVDS LVDS LVDS LVDS LVDS LVDS LVDS LVDS 3.3V / 3.3V 3.3V / 3.3V 3.3V / 3.3V S.3V / 3.3V	PU 4.7K to 3.3V PU 4.7K to 3.3V	Connect to LVDS connector	LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/ LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board LVDS Channel B differential clock LVDS panel power enable LVDS panel backlight enable

Chapter 3

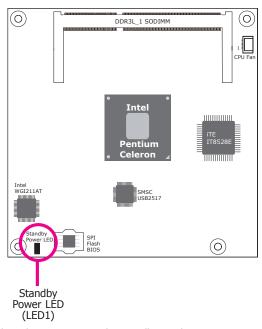
PC Signals and Descri													
nal	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968	Carrier Board	Description							
_AD0	B4												
_AD1	B5	I/O CMOS	3.3V / 3.3V			LPC multiples	ed address	command and	data bus				
C_AD2	B6	2,0 0,105	5.5 7 5.5 7		Connect to LPC device	El e malapies	ica adai coo,	communa and	data bas				
C_AD3	B7												
C_FRAME#	B3	O CMOS	3.3V / 3.3V			LPC frame in	dicates the s	tart of an LPC	cycle				
C_DRQ0#	B8	I CMOS	3.3V / 3.3V	NC	NC	LPC serial DN	1A request						
C_DRQ1#	B9		· ·	NC	NC								
C_SERIRQ	A50	I/O CMOS	3.3V / 3.3V	PU 1K to 3.3V	Connect to LPC device	LPC serial int							
C_CLK	B10	O CMOS	3.3V / 3.3V			LPC clock out	:put - 24MH:	nominal					
I Signals and Descrip						L							
al	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968	Carrier Board	Description	C . D	LCDT			CDTO CDT		
CS#	B97 A92	O CMOS I CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V		Connect to Carrier Board SPI Device CS# pin	Chip select for Data in to Mo	or Carrier Bo	ard SPI - may	be sourced t	rom chipset	SPIO or SPI		
_MISO					Connect a series resistor 33 Ω to Carrier Board SPI Device SO pin								
_MOSI CLK	A95 A94	O CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V		Connect a series resistor 33 Ω to Carrier Board SPI Device SI pin	Data out from Clock from M							
CLK	A94	O CMOS	3.3V Suspena/3.3V		Connect a series resistor 33 Ω to Carrier Board SPI Device SCK pin	Clock from M	odule to Cal	rier SPI					
						Power supply	for Carrier	Board SPI - so	urced from N	1odule – no	minally		
POWER	A91	0	3 3V Suspend/3 3V					ovide a minim					
_POWER	A91	U	3.3V Suspend/3.3V					n 100mA of Si					
						shall only be	used to pov	er SPI devices	on the Carri	er			
			+			Selection stra	ins to deterr	nine the BIOS	hoot device				
								oat these or p		nleace refe	er to		
								e Specification				RIOS disable	ciona
S_DIS0#	A34			PU 10K to 3.3V		CON Express	rioddic bas	c opecineution	RCVISION 2.3	тог эппирр	ing options o	DIOS disabil	. sigilu
						BIOS	BIOS	Chipset	Chipset	Carrier	SPI	Bios	Ref
						DIS1#	BIOS DIS0#	Chipset SPI CS1#	Chipset SPI CS0#	SPI CS#	Descriptor	Entry	Line
						5.0	5.00,	Destination	Destination	0.1_00#	Docompto.		
												0.01010011	_
		I CMOS	NA			1	1	Module	Module	High	Module	SPI0/SPI1	0
		I CMOS	NA			1	0	Module	Module	High	Module	Carrier FWH	1
							١ ،	Wodule	Wodule	riigii	Wodule	Camer I WII	'
						0	1	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2
DS_DIS1#	B88			PU 10K to 3.3V									_
						0	0	Carrier	Module	SPI1	Module	SPI0/SPI1	3
								(Default)	(Default)	(Default)	(Default)	(Default)	
A Signals and Descri	intions												
al	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968	Carrier Board	Description							
RED	B89	O Analog	Analog	PD 150 to GND	PD 150R,connect to VGA connector with EMI filter & ESD protect compon		tor Analog	outnut					
N_RED	B91	O Analog	Analog	PD 150 to GND	PD 150R, connect to VGA connector with EMI filter & ESD protect components of the connect connect components of the connect								
L_GKN L BLU	B92	O Analog O Analog		PD 150 to GND	PD 150R, connect to VGA connector with EMI filter & ESD protect compon PD 150R, connect to VGA connector with EMI filter & ESD protect compon								
L_BLU HSYNC	B92 B93	O Analog O CMOS	Analog 3.3V / 3.3V	AN 120 (0 RMD	Connect to VGA connector with a3.3V Buffer IC to isolate PCH & Display I								
A_VSYNC	B94	O CMOS	3.3V / 3.3V	DI 12 2K 1 2 2::	Connect to VGA connector with a 33V Buffer IC to isolate PCH & Display I				1:6 1/6:	.,	1.191		
A_I2C_CK	B95	I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V	Connect to VGA connector with a 3.3V to 5V Level shift circuit.			dedicated to id	entify VGA n	nonitor capa	abilities)		
_I2C_DAT	B96	I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V	Connect to VGA connector with a 3.3V to 5V Level shift circuit.	DDC data line	2.						
rial Interface Signals													
ial	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968	Carrier Board	Description							
0 TX	A98	O CMOS	5V / 12V		PD 4.7K to GND			rt 0 transmitte					
	7.50	0 0103	5., 12.		15 11/10 010			ecting Logic	Level Signa	ls on Pins	Reclaimed	from VCC	L2V)
0 RX	A99	I CMOS	5V / 12V	PU 10K to 3.3V		General purp							
		1 0.100	,	. 0 10.1 20 5.5 V				ecting Logic		ils on Pins	Reclaimed	from VCC_:	L2V)
R1_TX	A101	O CMOS	5V / 12V		PD 4.7K to GND			rt 1 transmitte					
	,,101	0 0.100	,					ecting Logic	Level Signa	als on Pins	Reclaimed	from VCC_:	L2V)
	1	1											
R1_RX	A102	I CMOS	5V / 12V	PU 10K to 3.3V		General purp		ecting Logic					

Miscellaneous Sign	als and Descriptio	ns					
gnal	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968		Carrier Board	Description
PKR	B32	O CMOS	3.3V / 3.3V	PU 10K to 3.3V			Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.
VDT	B27	O CMOS	3.3V / 3.3V	PD 100K to GND			Output indicating that a watchdog time-out event has occurred.
AN_PWNOUT	B101	O OD CMOS	3.3V / 3.3V				Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM. (Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)
AN_TACHIN	B102	I OD CMOS	3.3V / 3.3V	PU 47K to 3V3			Fan tachometer input for a fan with a two pulse output. (Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)
ГРМ_РР	A96	I CMOS	3.3V / 3.3V				Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.
Power and System	Management Sign	ale and Description	one				
ignal	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968		Carrier Board	Description
PWRBTN#	B12	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC	PU 4.7K to 3V3_SB		A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3SB	NC PU 4.7K to 3V3_SB		Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.
CB_RESET#	B50	O CMOS	3.3V Suspend/3.3V				Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software.
PWR_OK	B24	I CMOS	3.3V / 3.3V	PU 10K to 3V3			Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.
SUS_STAT#	B18	O CMOS	3.3V Suspend/3.3V	PU 1K to 3V3SB			Indicates imminent suspend operation; used to notify LPC devices.
SUS_S3#	A15	O CMOS	3.3V Suspend/3.3V	PD 100K to GND			Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.
SUS_S4#	A18	O CMOS	3.3V Suspend/3.3V	PD 100K to GND			Indicates system is in Suspend to Disk state. Active low output.
SUS_S5#	A24	O CMOS	3.3V Suspend/3.3V	PD 100K to GND			Indicates system is in Soft Off state.
WAKE0#	B66	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3SB			PCI Express wake up signal.
WAKE1#	B67	I CMOS	3.3V Suspend/3.3V	NA			General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.
BATLOW#	A27	I CMOS	3.3V Suspend/ 3.3V	PU 10K to 3V3SB			Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.
LID#	A103	I OD CMOS	3.3V Suspend/12V	PU 47K to 3V3_DU_EC			LID switch. Low active signal used by the ACPI operating system for a LID switch. (Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)
SLEEP#	B103	I OD CMOS	3.3V Suspend/12V	PU 4.7K to 3V3_DU			Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again. (Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)
THRM#	B35	I CMOS	3.3V / 3.3V	PU 1K to 3V3			Input from off-Module temp sensor indicating an over-temp situation.
THRMTRIP#	A35	O CMOS	3.3V / 3.3V	PU 1K to 3.3V			Active low output indicating that the CPU has entered thermal shutdown.
SMB_CK	B13	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC			System Management Bus bidirectional clock line.
SMB_DAT	B14	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC			System Management Bus bidirectional data line. System Management Bus Alert – active low input can be used to
SMB_ALERT#	B15	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC			generate an SMI# (System Management Interrupt) or to wake the system.
GPIO Signals and D							
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	BW968		Carrier Board	Description
GPO0	A93						Constant assessment as in a
GPO1 GPO2	B54 B57	O CMOS	3.3V / 3.3V				General purpose output pins. Upon a hardware reset, these outputs should be low.
GPO3	B63						open a manana coocy areas supula silvata de totti
GPI0	A54			PU 47K to 3.3V			
GPI1	A63	I CMOS	3.3V / 3.3V	PU 47K to 3.3V			General purpose input pins.
GPI2	A67	1 01105	5.54 / 5.54	PU 47K to 3.3V			Pulled high internally on the Module.
GPI3	A85			PU 47K to 3.3V	1		

Chapter 3

Power and GND Signals and Descriptions									
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance BW968	Carrier Board	Description				
VCC_12V	A104~A109 B104~B109 C104~C109 D104~D109	Power			Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.				
VCC_5V_SBY	B84~B87	Power			Standby power input: +5.0V nominal. If VCCS_SBY is used, all available VCC_SV_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.				
VCC_RTC	A47	Power			Real-time clock circuit-power input. Nominally +3.0V.				
GND	A1, A11, A21, A31 A41, A51, A57, A6 A66, A70, A80, A9 A100, A110, B1, B11, B21, B31, B4 B51, B60, B70, B8 B90, B100, B110, C1, C2, C5, C8, C1 C4, C21, C31, C4 C51, C60, C70, C7 C76, C80, C84, C8 C90, C93, C96, C100, C103, C110 D1, D2, D5, D8, D11, D14, D21, D31, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	0, 0, 1, 0, 11, 11, 3, 7, Power			Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.				

Standby Power LED



This LED will light when the system is in the standby mode.

Cooling Options

Heat Sink with Cooling Fan

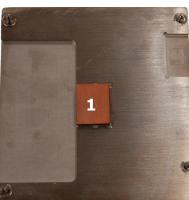


Note:

The system board used in the following illustrations may not resemble the actual board. These illustrations are for reference only.



Top View of the Heat Sink



Bottom View of the Heat Sink

 \bullet "1" denotes the location of the thermal pad/paste designed to contact the corresponding components that are on BW968.



Important:

Remove the plastic covering from the thermal pads prior to mounting the heat sink onto BW968.

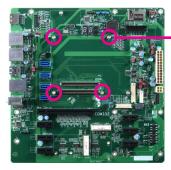
Installing BW968 onto a Carrier Board

4

Important:

The carrier board (COM332-B) used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install BW968 onto the carrier board of your choice.

Install the module and heatsink onto the carrier board. The photo below shows the location of the mounting holes on the carrier board.



Mounting standoffs

2. Grasp BW968 by its edges and position it on top of the carrier board with the mounting holes of BW968 aligning with the standoffs on the carrier board. This will also align the COM Express connectors of the two boards to each other.



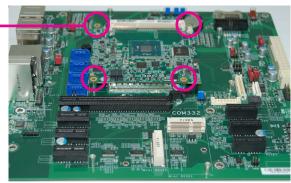
COM Express connectors on BW968



COM Express connectors on the carrier board

3. Press BW968 down firmly to seat it in the COM Express connectors of the carrier board.



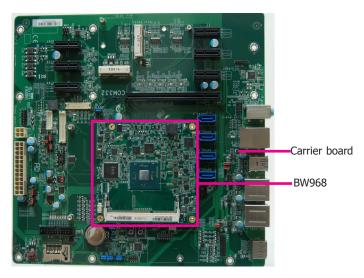




Note:

The above illustration shows the pressing points of the module onto the carrier board. Be careful when pressing the module to avoid damages to the connectors.

4. Verify that BW968 is firmly seated in the COM Express connectors of the carrier board.



5. Install a heat sink onto the BW968 with the carrier board. The photo below shows the heatsink installed on BW968.



Installing the COM Express Debug Card

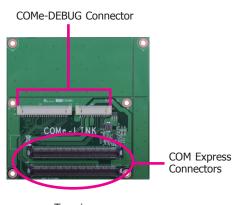


Note:

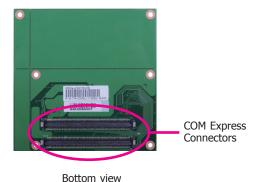
The system board used in the following illustrations may not resemble the actual board. These illustrations are for reference only.

 COMe-LINK1 is the COM Express debug card designed for COM Express Compact modules to debug and display signals and codes of COM Express modules.

COMe-LINK1

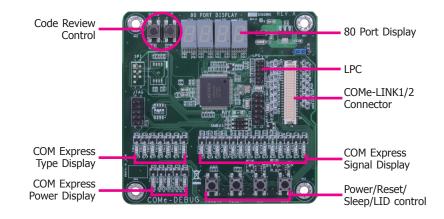


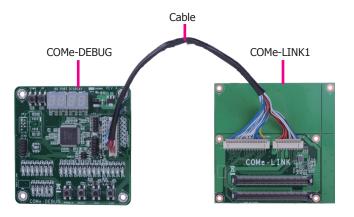
Top view



2. Connect the COMe-DEBUG card to COMe-LINK1 via a cable.

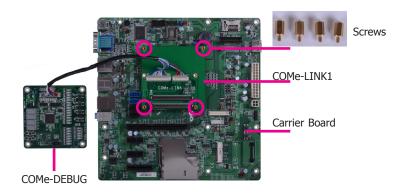
COMe-DEBUG



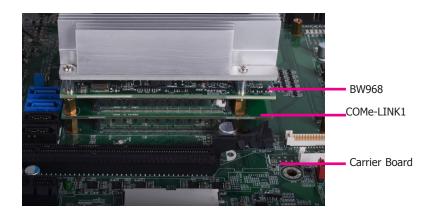


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4. Use the provided screws to fix the COMe-LINK1 debug card onto the carrier board.



5. Then use the instructions from the previous section to install BW968 and heatsink on the top of the COMe-LINK1 debug card.



Side View of the Module, Debug Card and Carrier Board

Chapter 4 - BIOS Setup

Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.

It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.



Note:

The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.

The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message "Press DEL to run setup" will appear on the screen. If the message disappears before you respond, restart the system or press the "Reset" button. You may also restart the system by pressing the <Ctrl> <Alt> and keys simultaneously.

Legends

KEYs	Function
F1	Help
<esc></esc>	Exit
Up and Down Arrows	Select Item
Right and Left Arrows	Select Item
<f5>/<f6></f6></f5>	Change Values
<enter></enter>	Select ▶ Submenu
<f9></f9>	Setup Defaults
<f10></f10>	Save and Exit

Scroll Bar

When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

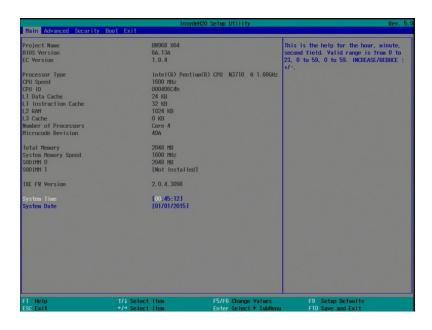
Submenu

When "▶" appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

Insyde BIOS Setup Utility

Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Date

The date format is <month>, <date>, <year>. Day displays a day, from Sunday to Saturday. Month displays the month, from January to December. Date displays the date, from 1 to 31. Year displays the year, from 1980 to 2099.

System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

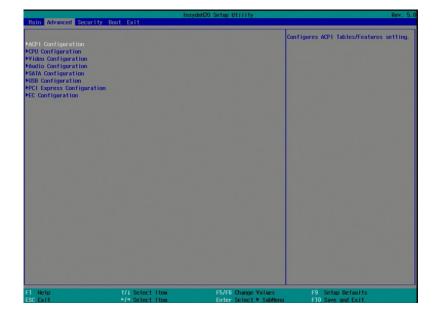
Advanced

The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.



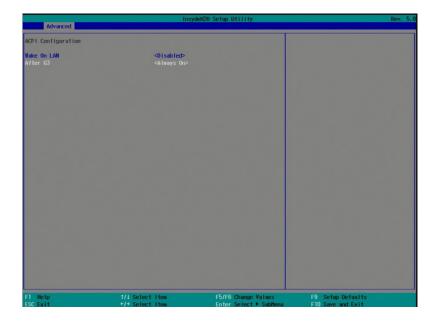
Important:

Setting incorrect field values may cause the system to malfunction.



ACPI Settings

This section allows you to configure the ACPI settings.



Wake on LAN

Set this field to enable to wake up the system via the onboard LAN or via a LAN card that supports the remote wake up function.

After G3

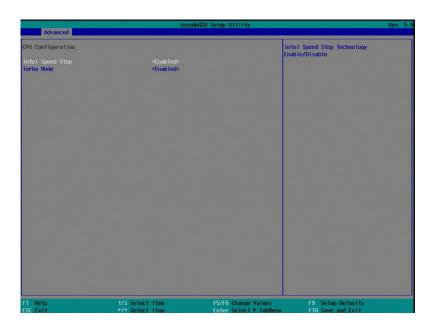
This field is to specify what state to go when power is re-applied after a power failure (G3 state).

Always On Power on the system when power is re-applied after AC power loss.

Always Off The system will be off when power is re-applied after AC power loss.

CPU Configuration

This section allows you to configure the CPU.



Intel Speed Step

Enable/Disable Intel Speed Step Technology.

Turbo Mode

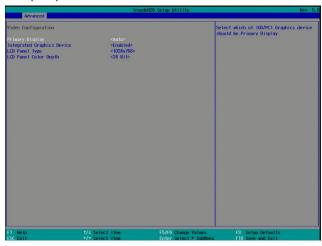
This field is used to enable or disable processor turbo mode.

Video Configuration

This section allows you to configure the video settings.

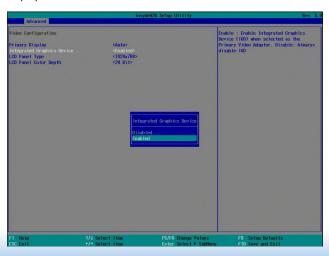
Primary Display

Select the primary display: Auto, integrated graphics display (IGD) or PCIe graphics card (PCIe).



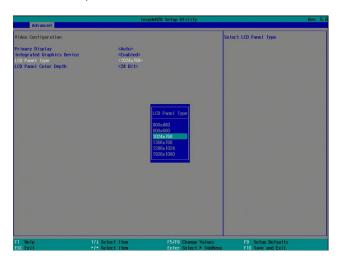
Integrated Graphics Device

Enable or disable Integrated Graphics Device when IGD is selected as the primary display.



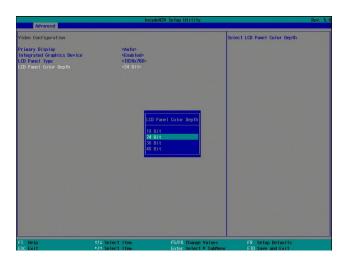
LCD Panel Type

Select the LCD panel resolution.



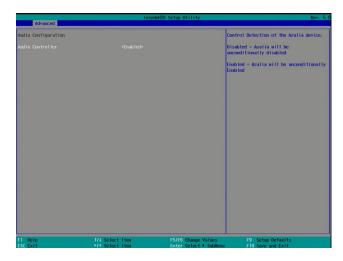
LCD Panel Color Depth

Select the LCD panel color depth: 18 bit, 24 bit, 36 bit or 48 bit.



Audio Configuration

This section allows you to configure the audio settings.



Audio Controller

Control the detection of the Azalia device.

Disabled

Azalia will be unconditionally disabled.

Enabled

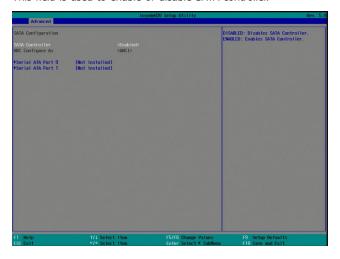
Azalia will be unconditionally enabled.

SATA Configuration

This section lets you select the SATA controller and the type of hard disk drive installed on the system.

SATA Controller

This field is used to enable or disable SATA controller.

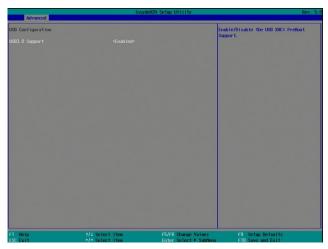


Serial ATA Port 0 and 1

This field is used to enable or disable the serial ATA port.

USB Configuration

This section allows you to configure the parameters of the USB device.



USB3.0 Support

Enabled

Enable the USB XHCI PreBoot Support.

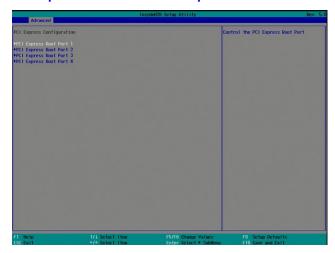
Disabled

Disable the USB XHCI PreBoot Support.

PCI Express Configuration

This section configures settings relevant to PCI Express root ports.

PCI Express Root Port 1 to PCI Express Root Port 4



PCI Express Root Port 1 to 4

This field is used to enable or disable the PCI Express Root Port.



PCIe Speed

Select the speed of the PCI Express Root Port: Gen1 or Gen2.

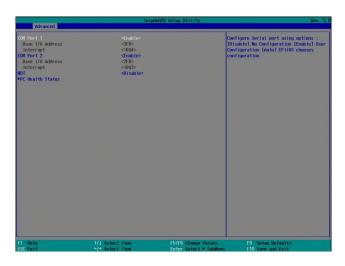
EC Configuration

This section allows you to configure the Embedded Controller (EC) settings.

COM Port 1 to COM Port 2

Configure the settings for each COM port.

Disable Disable this COM port. **Enable** Enable this COM port.



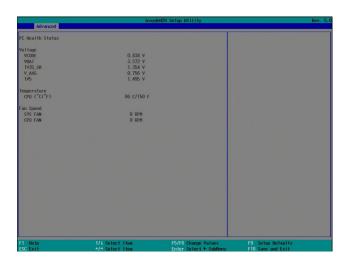
WDT

Enable or disable the watchdog function. A counter will appear if you select to enable WDT. Input any value between 1 to 255 seconds.



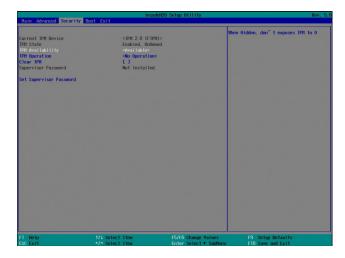
PC Health Status

This field only displays the PC health information.



Security

This section allows you to configure the Trusted Platform Module (TPM) on the system.



TPM Availability

Select to show or hide TPM configuration options.

TPM Operation

Select "Enable" to enable storage and endorsement hierarchy and "disable" to disable storage and endorsement hierarchy. Select "No Operation" to make no changes.

Clear TPM

Remove all TPM context associated with a specific owner.

Set Supervisor Password

Set the supervisor's password and the length of the password must be greater than one character. $\,$

Boot

This section shows the available boot options and allows you to configure them for the system.



OS Selection

This field is used to select the operating system.

Numlock

Select the power-on state for Numlock.

Boot Type

Select the boot type. The options are Dual Boot Type, Legacy Boot Type, and UEFI Boot Type.

Network Stack

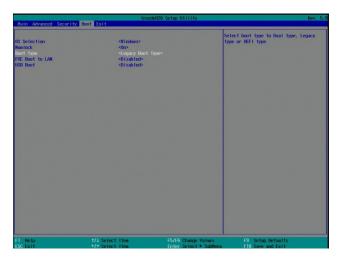
Enable or disable UEFI network stack. It supports the operation of these functions or software: Windows 8 BitLocker Network Unlock, UEFI IPv4/IPv6 PXE and legacy PXE Option ROM.

USB Boot

Enable or disable the booting to USB boot devices.

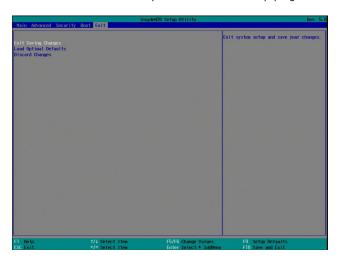
PXE Boot to LAN

If "Legacy Boot Type" is selected for Boot Type, the "PXE Boot to LAN" option will be shown. This field is used to enable or disable booting the device through the Ethernet adaptor supporting PXE (Preboot Execution Environment).



Exit

This section shows the exit options of the BIOS setup program.



Exit Saving Changes

Select this field and then press <Enter> to exit the system setup and save your changes.

Load Optimal Defaults

Select this field and then press <Enter> to load optimal defaults.

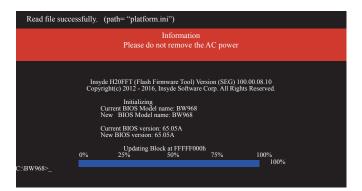
Discard Changes

Select this field and then press <Enter> to exit the system setup without saving your changes.

Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files and specific instructions about how to update BIOS with the flash utility.

When you download the given BIOS file, you may find a BIOS flash utility attached with the BIOS file. This is the utility for performing BIOS updating procedure. For your convenience, we will also provide you with an auto-execution file in the BIOS file downloaded. This auto-execution file will bring you directly to the flash utility menu soon after system boots up and finishes running the boot files in your boot disk.



Notice: BIOS SPI ROM

- The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.
- 2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.
- 3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

心

Note:

- a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.
- b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not

Chapter 4 BIOS Setup www.dfi.com

Chapter 5 - Supported Software

Install drivers, utilities and software applications that are required to facilitate and enhance the performance of the system board. You may acquire the software from your sales representatives, from an optional DVD included in the shipment, or from the website download page at https://www.dfi.com/DownloadCenter.

Auto Run Page (For Windows 10)



Auto Run Page (For Windows 8.1)





Auto Run Page (For Windows 7)







Note:

This step can be ignored if the applications are standalone files.

Intel Chipset Software Installation Utility

The Intel Chipset Software Installation Utility is used for updating Windows INF files so that the Intel chipset can be recognized and configured properly in the system.

To install the utility, click "Intel Chipset Software Installation Utility" on the main menu.

1. Setup is now ready to install the utility. Click Next.



2. Read the license agreement then click Yes.



3. Go through the readme document for system requirements and installation tips then click Next.



4. After completing installation, click Finish to exit setup.



Intel Graphics Drivers

To install the driver, click "Intel Graphics Drivers" on the main menu.

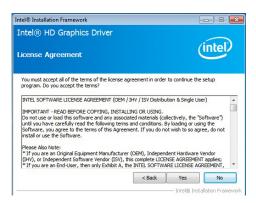
 Setup is now ready to install the graphics driver. Click "Next".



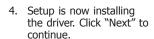
By default, the "Automatically run WinSAT and enable the Windows Aero desktop theme" is enabled. With this enabled, after installing the graphics driver and the system rebooted, the screen will turn blank for 1 to 2 minutes (while WinSAT is running) before the Windows 7/ Windows 8.1/ Windows 10 desktop appears. The "blank screen" period is the time Windows is testing the graphics performance.

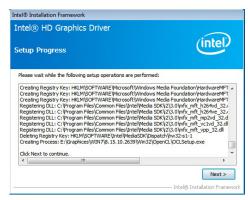
We recommend that you skip this process by disabling this function then click "Next".

2. Read the license agreement then click "Yes".



3. Go through the readme document for system requirements and installation tips then click "Next".





Refer to the Readme file below to view the system requirements and installation information.

(1)These operating systems supported for embedded designs and usage

- 0 X

(intel

< Back Next > Cancel

Intel® Installation Frame

Intel® Installation Framework

Intel® HD Graphics Driver

Readme File Information

Production Version Releases

February 8, 2012

Microsoft Windows* 7 Microsoft Windows* Embedded Standard 7(1)

 Click "Yes, I want to restart this computer now" then click "Finish".

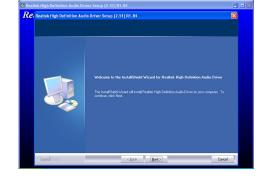
Restarting the system will allow the new software installation to take effect.



Audio Drivers

To install the driver, click "Audio Drivers" on the main menu.

- 1. Setup is now ready to install the audio driver. Click Next.
- 2. Follow the remainder of the steps on the screen; clicking "Next" each time you finish a step.



3. Click "Yes, I want to restart my computer now" then click Finish.

Restarting the system will allow the new software installation to take effect.



Intel LAN Drivers

To install the driver, click "Intel LAN Drivers" on the main menu.

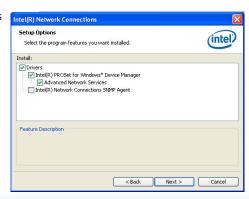
1. Setup is ready to install the driver. Click Next.



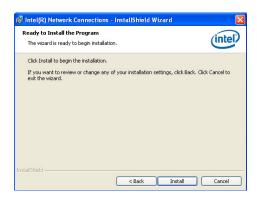
Click "I accept the terms in the license agreement" then click "Next".



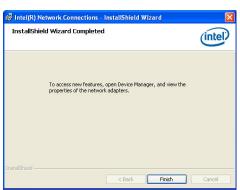
3. Select the program featuers you want installed then click Next.



4. Click Install to begin the installation.



5. After completing installation, click Finish.



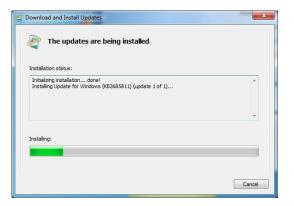
Kernel Mode Driver (For Windows 7 only)

To install the driver, click "Kernel Mode Driver Framework" on the main menu.

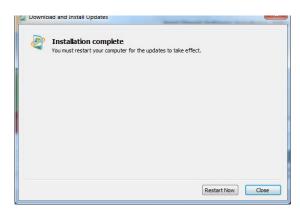
1. Click "Yes" to install the update.



2. The update is installed now.



3. Click "Restart Now" to restart your computer when the installation is complete.



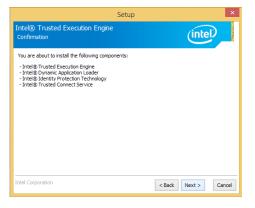
Intel Trusted Execution Engine Driver

To install the driver, click "Intel Trusted Execution Engine Driver" on the main menu.

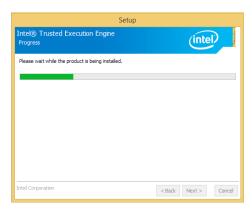
 Tick "I accept the terms in the License Agreement" and then click "Next."



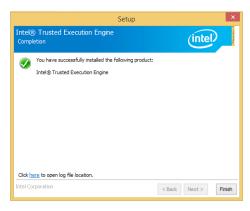
2. The step shows the components which will be installed. Then, Click Next.



3. The step displays the installing status in the progress.



4. Click "Finish" when the installation is complete.



HW Utility

HW Utility provides information about the board, Watchdog,and DIO. To access the utility, click "HW Utility" on the main menu.



Note:

If you are using Windows 7 or later versions, you need to access the operating system as an administrator to be able to install the utility.

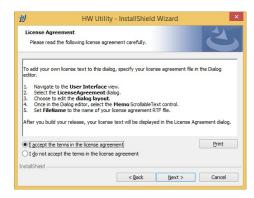
Setup is ready to install the driver



2. Click "Next" to continue.



 Read the license agreement then click "I accept the terms in the license agreement". Click "Next".



4. The wizard is ready to begin installation. Click "Install".



5. Please wait while the program features are being installed.



The HW Utility icon will appear on the desktop. Double-click the icon to open the utility.



Information

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Note:

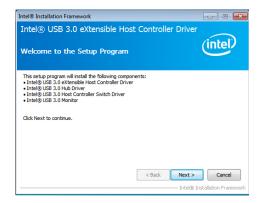
Note: The screenshot displayed above is for illustrative purpose only, and may not resemble the actual screen.

The BW968 HW Utility features the following tabs: Information, HW Health, HW Healthset, Watchdog, DIO and Backlight. Click on the tabs to access information about the board.

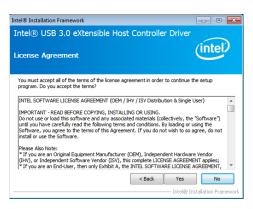
Intel USB 3.0 Drivers (For Windows 7 and Windows 8.1)

To install the driver, click "Intel USB 3.0 Driver" on the main menu.

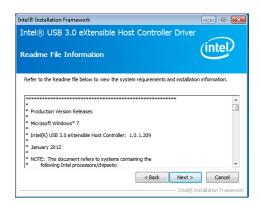
1. Setup is ready to install the driver. Click Next.



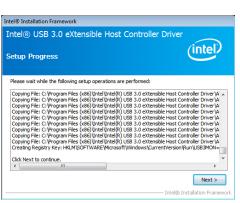
2. Read the license agreement then click Yes.



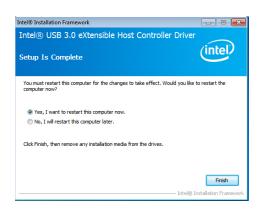
Go through the readme document for more installation tips then click Next.



 Setup is currently installing the driver. After installation has completed, click Next.



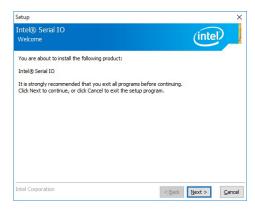
5. After completing installation, click Finish.



IO Driver

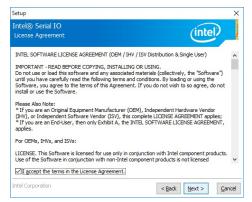
To install the driver, click "Intel Serial IO Driver" on the main menu

1. Setup is ready to install the driver. Click Next.

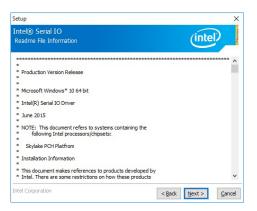


2. Read the license agreement carefully.

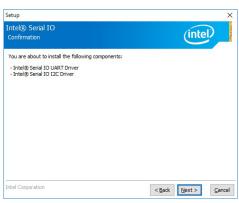
Click "I accept the terms in the License Agreement" then click Next.



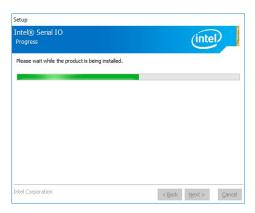
3. Read the file information then click Next.



4. Setup is ready to install the driver. Click Next.



5. Setup is now installing the driver.



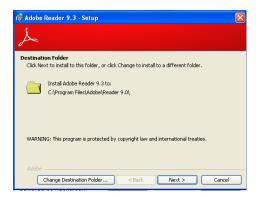
6. Click Finish.



Adobe Acrobat Reader 9.3

To install the reader, click "Adobe Acrobat Reader 9.3" on the main menu.

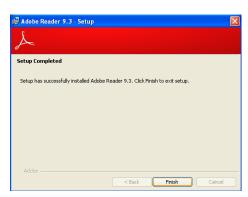
Click Next to install or click
 Change Destination Folder to
 select another folder.



2. Click Install to begin installation.



3. Click Finish to exit installation.



Appendix A - Troubleshooting

Troubleshooting Checklist

This chapter of the manual is designed to help you with problems that you may encounter with your personal computer. To efficiently troubleshoot your system, treat each problem individually. This is to ensure an accurate diagnosis of the problem in case a problem has multiple causes.

Some of the most common things to check when you encounter problems while using your system are listed below.

- 1. The power switch of each peripheral device is turned on.
- 2. All cables and power cords are tightly connected.
- 3. The electrical outlet to which your peripheral devices are connected is working. Test the outlet by plugging in a lamp or other electrical device.
- 4. The monitor is turned on.
- 5. The display's brightness and contrast controls are adjusted properly.
- 6. All add-in boards in the expansion slots are seated securely.
- 7. Any add-in board you have installed is designed for your system and is set up correctly.

Monitor/Display

If the display screen remains dark after the system is turned on:

- 1. Make sure that the monitor's power switch is on.
- 2. Check that one end of the monitor's power cord is properly attached to the monitor and the other end is plugged into a working AC outlet. If necessary, try another outlet.
- 3. Check that the video input cable is properly attached to the monitor and the system's display adapter.
- 4. Adjust the brightness of the display by turning the monitor's brightness control knob.

The picture seems to be constantly moving.

- 1. The monitor has lost its vertical sync. Adjust the monitor's vertical sync.
- 2. Move away any objects, such as another monitor or fan, that may be creating a magnetic field around the display.
- 3. Make sure your video card's output frequencies are supported by this monitor.

The screen seems to be constantly wavering.

1. If the monitor is close to another monitor, the adjacent monitor may need to be turned off. Fluorescent lights adjacent to the monitor may also cause screen wavering.

Power Supply

When the computer is turned on, nothing happens.

- 1. Check that one end of the AC power cord is plugged into a live outlet and the other end properly plugged into the back of the system.
- 2. Make sure that the voltage selection switch on the back panel is set for the correct type of voltage you are using.
- 3. The power cord may have a "short" or "open". Inspect the cord and install a new one if necessary.

Appendix A Troubleshooting www.dfi.com

Hard Drive

Hard disk failure.

- 1. Make sure the correct drive type for the hard disk drive has been entered in the BIOS.
- 2. If the system is configured with two hard drives, make sure the bootable (first) hard drive is configured as Master and the second hard drive is configured as Slave. The master hard drive must have an active/bootable partition.

Excessively long formatting period.

If your hard drive takes an excessively long period of time to format, it is likely a cable connection problem. However, if your hard drive has a large capacity, it will take a longer time to format.

Serial Port

The serial device (modem, printer) doesn't output anything or is outputting garbled

characters.

- 1. Make sure that the serial device's power is turned on and that the device is on-line.
- 2. Verify that the device is plugged into the correct serial port on the rear of the computer.
- 3. Verify that the attached serial device works by attaching it to a serial port that is working and configured correctly. If the serial device does not work, either the cable or the serial device has a problem. If the serial device works, the problem may be due to the onboard I/O or the address setting.
- 4. Make sure the COM settings and I/O address are configured correctly.

Keyboard

Nothing happens when a key on the keyboard was pressed.

- 1. Make sure the keyboard is properly connected.
- 2. Make sure there are no objects resting on the keyboard and that no keys are pressed during the booting process.

System Board

- 1. Make sure the add-in card is seated securely in the expansion slot. If the add-in card is loose, power off the system, re-install the card and power up the system.
- 2. Check the jumper settings to ensure that the jumpers are properly set.
- 3. Verify that all memory modules are seated securely into the memory sockets.
- 4. Make sure the memory modules are in the correct locations.
- 5. If the board fails to function, place the board on a flat surface and seat all socketed components. Gently press each component into the socket.
- 6. If you made changes to the BIOS settings, re-enter setup and load the BIOS defaults.

Appendix A Troubleshooting www.dfi.com

Appendix B - Insyde BIOS Standard Status POST Code

SEC Phase 8-Bit POST Code Values

Functionality Name	POST Code Value	Description
SEC_SYSTEM_POWER_ON	01	CPU power on and switch to Protected mode
SEC_AFTER_MICROCODE_PATCH	03	Setup Cache as RAM
SEC_ACCESS_CSR	04	PCIE MMIO Base Address initial
SEC_GENERIC_MSRINIT	05	CPU Generic MSR initialization
SEC_CPU_SPEEDCFG	06	Setup CPU speed
SEC_SETUP_CAR_OK	07	Cache as RAM test
SEC_FORCE_MAX_RATIO	08	Tune CPU frequency ratio to maximum level
SEC_GO_TO_SECSTARTUP	09	Setup BIOS ROM cache
SEC_GO_TO_PEICORE	0A	Enter Boot Firmware Volume

PEI Phase 8-Bit POST Code Values

Functionality Name	POST Code Value	Description
PEI_SIO_INIT	70	Super I/O initialization
PEI_CPU_REG_INIT	71	CPU Early Initialization
PEI_CPU_AP_INIT	72	Multi-processor Early initialization
PEI_CPU_HT_RESET	73	HyperTransport initialization
PEI_PCIE_MMIO_INIT	74	PCIE MMIO BAR Initialization
PEI_NB_REG_INIT	75	North Bridge Early Initialization
PEI_SB_REG_INIT	76	South Bridge Early Initialization
PEI_PCIE_TRAINING	77	PCIE Training
PEI_TPM_INIT	78	TPM Initialization
PEI_MEMORY_INSTALL	80	Simple Memory test
PEI_TXTPEI	81	TXT function early initialization
PEI_MEMORY_CALLBACK	83	Set cache for physical memory

DXE Phase 8-Bit POST Code Values

Functionality Name	Post Code Values	Description
DXE_SB_SPI_INIT	41	South bridge SPI initialization
DXE_VARIABLE_RECLAIM	61	Variable store garbage collection and reclaim operation
DXE_FLASH_PART_NONSUPPORT	62	Flash part not supported.

BDS Phase 8-Bit POST Code Values

Functionality Name	POST Code Value	Description
BDS_ENTER_BDS	10	Enter BDS entry
BDS_INSTALL_HOTKEY	11	Install Hotkey service
BDS_ASF_INIT	12	ASF Initialization
BDS_PCI_ENUMERATION_START	13	PCI enumeration
BDS_BEFORE_PCIIO_INSTALL	14	PCI resource assign complete
BDS_PCI_ENUMERATION_END	15	PCI enumeration complete
BDS_CONNECT_CONSOLE_IN	16	Keyboard Controller, Keyboard and Mouse initializatio
BDS_CONNECT_CONSOLE_OUT	17	Video device initialization
BDS_CONNECT_STD_ERR	18	Error report device initialization
BDS_CONNECT_USB_HC	19	USB host controller initialization
BDS_CONNECT_USB_BUS	1A	USB BUS driver initialization
BDS_CONNECT_USB_DEVICE	1B	USB device driver initialization
BDS_NO_CONSOLE_ACTION	1C	Console device initialization fail
BDS_ENUMERATE_ALL_BOOT_OPTIO	27	Get boot device information
BDS_ENTER_SETUP	29	Enter Setup Menu
BDS_ENTER_BOOT_MANAGER	2A	Enter Boot manager
BDS_READY_TO_BOOT_EVENT	2E	Last Chipset initialization before boot to OS
BDS_GO_LEGACY_BOOT	2F	Start to boot Legacy OS
BDS_GO_UEFI_BOOT	30	Start to boot UEFI OS
BDS_LEGACY16_PREPARE_TO_BOOT	31	Prepare to Boot to Legacy OS
BDS_EXIT_BOOT_SERVICES	32	Send END of POST Message to ME via HECI

PostBDS Phase 8-Bit POST Code Values

Functionality Name	POST Code Value	Description
POST_BDS_NO_BOOT_DEVICE	F9	No Boot Device
POST_BDS_JUMP_BOOT_SECTOR	FE	Try to Boot with INT 19

ACPI 8-Bit POST Code Values

Functionality Name	POST Code Value	Description
ASL_ENTER_S1	51	Prepare to enter S1
ASL ENTER S3	53	Prepare to enter S3
ASL_ENTER_S4	54	Prepare to enter S4
ASL_ENTER_S5	55	Prepare to enter S5
ASL_WAKEUP_S1	E1	System wakeup from S1
ASL_WAKEUP_S3	E3	System wakeup from S3
ASL_WAKEUP_S4	E4	System wakeup from S4
ASL_WAKEUP_S5	E5	System wakeup from S5

SMM 8-Bit POST Code Values

Functionality Name	POST Code Value	Description
SMM_ACPI_ENABLE_END	A7	ACPI enable function complete
SMM_S1_SLEEP_CALLBACK	A1	Enter S1
SMM_S3_SLEEP_CALLBACK	A3	Enter S3
SMM_S4_SLEEP_CALLBACK	A4	Enter S4
SMM_S5_SLEEP_CALLBACK	A5	Enter S5