IB905

Intel® Sandy Bridge / PCH

3.5-inch Embedded Board

USER'S MANUAL

Version 1.1

Acknowledgments

Table of Contents

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Introduction

Product Description

The IB905 3.5-inch embedded board is based on the latest Intel® QM67 chipset. The platform supports 2nd generation Intel® Core processor family with rPGA988B packing and features an integrated dual-channel DDR3 memory controller as well as a graphics core.

The latest Intel® processors provide advanced performance in both computing and graphics quality. This meets the requirement of customers in the gaming, POS, digital signage and server market segment.

The Intel® QM67 is made with 32 nanometer technology that supports Intel's first processor architecture to unite the CPU and the graphics core on the transistor level. The IB905 3.5-inch embedded board utilizes the dramatic increase in performance provided by this Intel's latest cutting-edge technology. Measuring 102mm x 148mm, IB905 offers fast 6Gbps SATA support (2 ports), USB3.0 (2 ports) and interfaces for , DVI-I, LVDS displays. IB905 features Intel Active Management Technology 7.0.

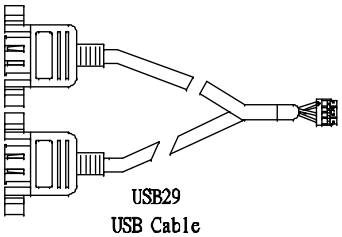
IB905 FEATURES:

- Supports Intel® 2nd Generation Core i7/i5/i3 QC/DC mobile processors
- One DDR3 SoDIMM, 1066/1333MHz, Max. 4GB memory
- Dual Intel® PCI-Express Gigabit LAN
- Integrated Graphics for DVI-I/LVDS displays
- 2x SATA 3.0, 6x USB 2.0, USB 3.0 (2 ports), 2x COM, Watchdog timer
- 1x Mini PCI-E
- Digital I/O, LPC/Smart battery interface

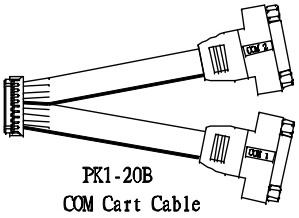
Checklist

Your IB905 package should include the items listed below.

- The IB905 3.5-inch embedded board
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- SATA-12 ;PK1-20B ;PW87 cable
- Optional SATA-5;Audio-18;USB29;HSIB905

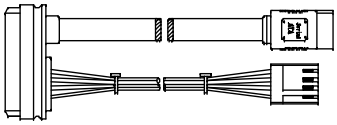


USB29
USB Cable



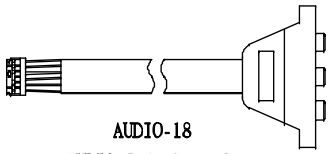
PK1-20B
COM Cart Cable

SATA-5
SATA Cable

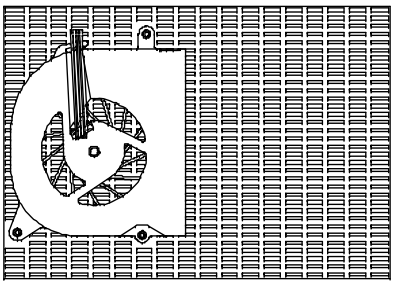


SATA 12
SATA & POWER Cable

PW87
DC-in Power Cable



AUDIO-18
AUDIO 5.1 channel



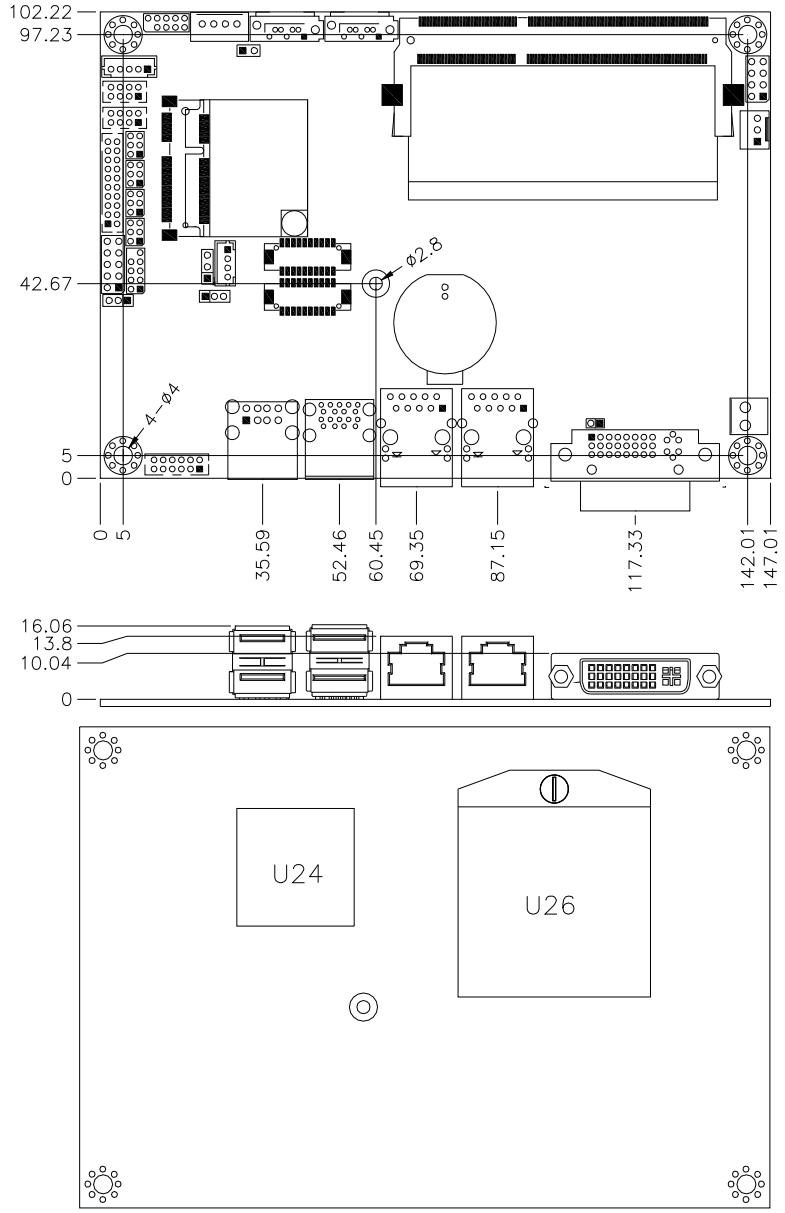
HSIB905-PGA(+FAN)
Heat Sink

IB905 Specifications

Form Factor	3.5" Disk Size
CPU Type	- Intel® 2nd generation Core™ i7/i5/i3/Celeron QC/DC mobile processor - rPGA package, 37.5 x 37.5 mm - TDP: QC = 45W~ 55W/ DC = 35W
CPU Speed	Up to 2.7GHz
Cache	Up to 8MB
CPU Socket	rPGA988B(Socket G2) @ solder side
Chipset	Intel® QM67 PCH @ solder side 25 x 27 mm package size , TDP=3.9W
BIOS	AMI BIOS, support ACPI Function
Memory	Intel® 2nd generation Core™ i7/i5 QC/DC mobile processor integrated memory controller DDRIII 1066/1333/1600 MHz SO-DIMM x **1** (w/o ECC, 1.5V), Max. 8GB
VGA	Intel® 2nd Gen. Core™ i7/i5/i3 mobile processor integrated Gfx DVI-I x 1 (thru Level shifter ASM1442) [Thru Digital Port B]
LVDS	24-bit dual channels LVDS interface w/DF13 socket x2
LAN	1. Intel® 82579V GbE PHY as 1st LAN 2. Intel® 82583V PCIe GbE as 2nd LAN
USB (Universal Serial Bus)	1. Intel® QM67 PCH integrated USB 2.0 host controller, **6** ports : 2-port in the rear panel + 4-ports via pin header 2. USB 3.0 host controller [ASM1042], support **2** ports in the rear panel [Does not support DOS boot function]
Serial ATA Ports	Intel® QM67 PCH built-in SATA controller, supports 2 x SATA 3.0 (6Gbps)
Audio	Intel® QM67 PCH built-in High Definition Audio controller + Realtek ALC662, support 5.1-channel
LPC I/O	**Winbond W83627DHG** COM1 (RS232 only) COM2 (RS232/422/485) with pin-18 with power @500 mA (jumper selectable for 5V or 12V) via DF11 2x10 pin connector Hardware Monitor: 2x Thermal inputs 2x Voltage monitoring 1x fan speed DC control
Digital IO	4 in & 4 out
IAMT(7.0)	**N/A**
Expansion Slots	Mini PCI-e socket x **1**, Half-sized type, reserved one mounting hole only; [USB device support]
Edge Connector	DVI-I x1 RJ45 x2 for LAN 1&2 USB 3.0 stack connector x 1 for USB1 ~2 [Blue color] USB 2.0 stack connector x 1 for USB3 ~4

On Board Header/Connector	2 ports x SATA **III** [Blue color] 2x4 pins header x 2 for 4 USB 2.0 ports[DF11] DF13-20 socket connector x 2 for 24-bit dual channel LVDS 2x6 pins box header x1 for Audio [DF11] 2x10 pins box header x 1 for COM1~2 [DF11] 2x5 pins headers x 1 for LPC **Digital IO** Mini PCI-e(1x) connector x **1** [Half-sized] 5 pins box header x 1 for smart battery 4 pins box header x 1 for backlight/brightness control 4 pins power connector x **1** for SATA HDD 2 pins power connector x 1 for 12V DC-in [180 degree vertical type]
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec/min)
Power Connector	+12V DC-in only
RoHS	Yes
Board Size	102mm x 147mm
Others	

Board Dimensions

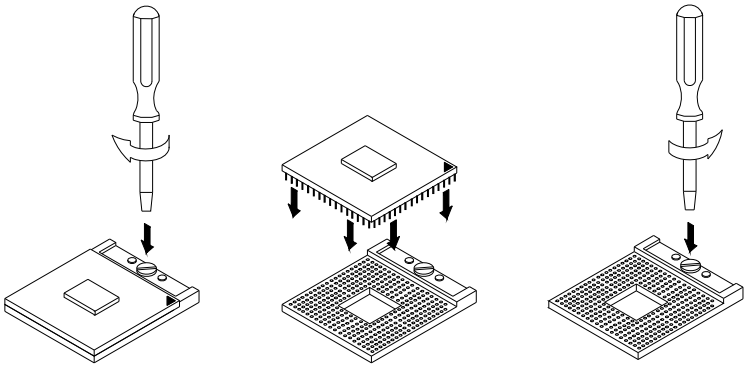


Installations

This section provides information on how to use the jumpers and connectors on the IB905 in order to set up a workable system. The topics covered are:

Installing the CPU

The IB905 board supports rPGA988B socket for Intel® Sandy Bridge Dual Core mobile processors.
The processor socket comes with a screw to secure the processor. As shown in the left picture below, loosen the screw first before inserting the processor. Place the processor into the socket by making sure the notch on the corner of the CPU corresponds with the notch on the inside of the socket. Once the processor has slide into the socket, fasten the screw. Refer to the figures below.



***NOTE**: Ensure that the CPU heat sink and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.*

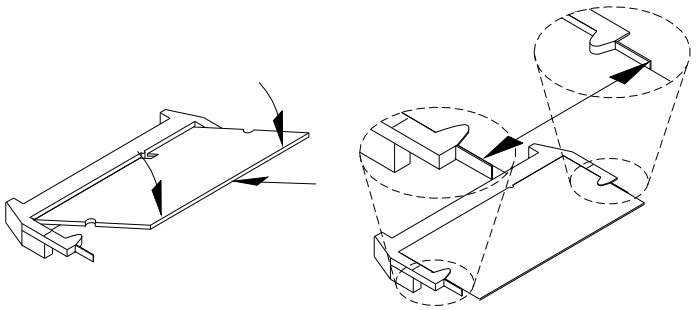
Installing the Memory

The IB905 board supports one DDR3 memory socket for a maximum total memory of 4GB in DDR3 SO-DIMM memory type.

Installing and Removing Memory Modules

To install the DDR3 modules, locate the memory slot on the board and perform the following steps:

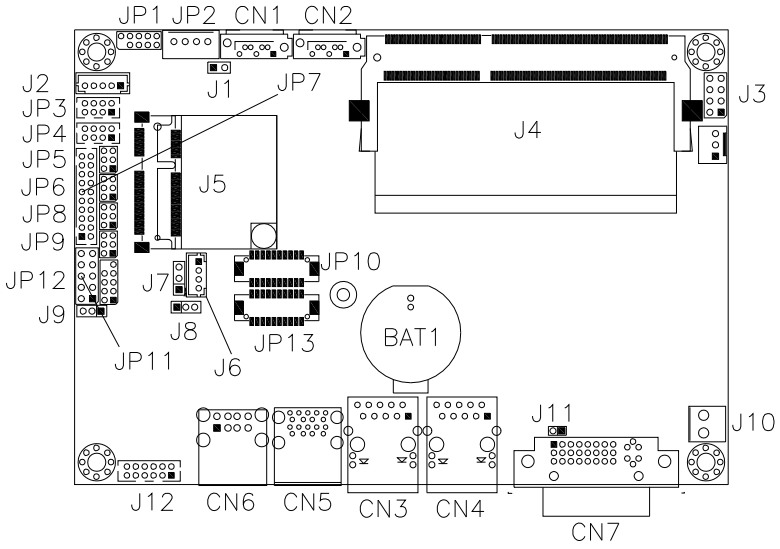
1. Hold the DDR3 module so that the key of the DDR3 module aligns with that on the memory slot. Insert the module into the socket at a slight angle (approximately 30 degrees). Note that the socket and module are both keyed, which means that the module can be installed only in one direction.
2. To seat the memory module into the socket, apply firm and even pressure to each end of the module until you feel it slip down into the socket.
3. With the module properly seated in the socket, rotate the module downward. Continue pressing downward until the clips at each end lock into position.
4. To remove the DDR3 module, press the clips with both hands.



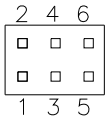
Setting the Jumpers

Jumpers are used on IB905 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on IB905 and their respective functions.

Jumper Locations on IB905

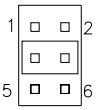


JP5, JP6, JP8: RS232/RS422/RS485 (COM2) Selection



COM2 Function	RS-232	RS-422	RS-485
Jumper Setting (pin closed)	JP5: 3-5&4-6 JP8: 1-2 JP6: 3-5 & 4-6	JP5: 1-3&2-4 JP8: 3-4 JP6: 1-3 & 2-4	JP5: 1-3&2-4 JP8: 5-6 JP6: 1-3 & 2-4

JP9: COM2 RS232 RI/+5V/+12V Power Setting

JP9	Setting	Function
	Pin 1-2 Short/Closed	+5V
	Pin 3-4 Short/Closed	RI
	Pin 5-6 Short/Closed	+12V

J7: LCD Panel Power Selection

J7	LCD Panel Power
	3.3V
	5V

J1: Flash Descriptor Security Override (Factory use only)

J1	Flash Descriptor Security Override
Open	Disabled (Default)
Close	Enabled

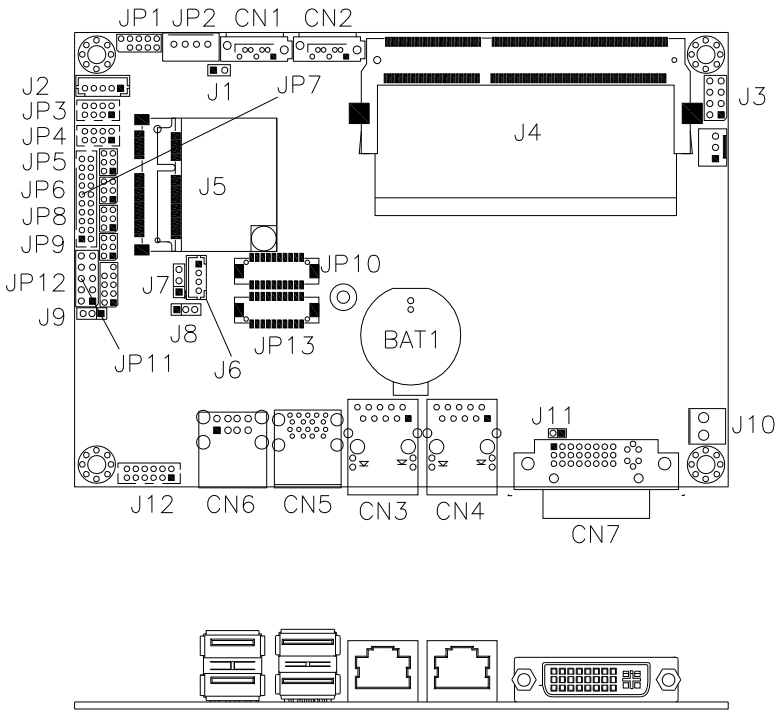
J8: ATX or AT Power Selection

J8	Setting	Function
	Pin 1-2 Short/Closed	ATX Mode
	Pin 2-3 Short/Closed	AT Mode

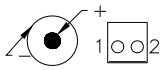
J9: Clear CMOS Contents

J9	Setting	Function
	Pin 1-2 Short/Closed	Normal
	Pin 2-3 Short/Closed	Clear CMOS

Connectors on IB905

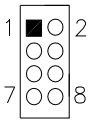

JP1
JP2
CN1
CN2
J2
JP3
JP4
JP5
JP6
JP8
JP9
JP12
J9
J1
JP7
J5
J4
J3
JP10
J7
J8
JP13
BAT1
JP11
J6
J11
J10
J12
CN6
CN5
CN3
CN4
CN7

J10: DC-IN 12V Power Connector



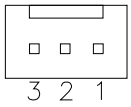
Pin #	Signal Name
1	DC in (12V only)
2	Ground

J3: Front Panel Connector



Signal Name	Pin #	Pin #	Signal Name
Power BTN	1	2	Power BTN
HDD LED+	3	4	HDD LED-
Reset BTN	5	6	Reset BTN
Power LED+	7	8	Power LED-

SYS_FAN1:DC-system Fan Power Connector

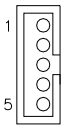


Pin #	Signal Name
1	Ground
2	+12V
3	NC

JP2: HDD Power Connector

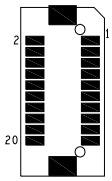
Pin #	Signal Name
1	+5V
2	Ground
3	Ground
4	+12V

J2: Smart Battery Interface Connector



Pin #	Signal Name
1	RST
2	EXTSMI
3	Ground
4	DATA
5	CLK

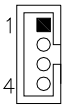
J10, J13: LVDS1, LVDS2 Connectors (1st/2nd channel)



Signal Name	Pin #	Pin #	Signal Name
TX0-	2	1	TX0+
Ground	4	3	Ground
TX1-	6	5	TX1+
*5V/3.3V	8	7	Ground
TX3-	10	9	TX3+
TX2-	12	11	TX2+
Ground	14	13	Ground
TXC-	16	15	TXC+
*5V/3.3V	18	17	ENABKL
+12V	20	19	+12V

** Remarks: These connectors support 24-bit.J10 is 1st channel. J13 is 2nd channel. J7 can be used to set 1-2 3.3V or 2-3 5V.*

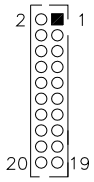
J6: LCD Backlight Connector (DC type)



Pin #	Signal Name
1	+12V
2	Backlight Enable
3	*Backlight Adj (DC type)
4	Ground

** LCD backlight brightness can be adjusted by the OS or in the BIOS setup. In the BIOS setup, both backlight enable/disable and backlight brightness can be configured. Also, the backlight voltage can be set to 3.3V or 5V.*

JP7: COM1, COM2 Serial Port (DF11 Connector)

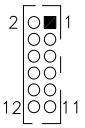


Signal Name	Pin #	Pin #	Signal Name
DSR1 Data set ready	2	1	DCD1 Data carrier detect
RTS1 Request to send	4	3	RXD1 Receive data
CTS1 Clear to send	6	5	TXD1 Transmit data
RI1 Ringing indicator	8	7	DTR1 Data terminal ready
Not used	10	9	Ground
DSR2	12	11	DCD2
RTS2	14	13	RXD2
CTS2	16	15	TXD2
RI2	18	17	DTR2
Not used	20	19	Ground

COM2 is jumper selectable for RS-232, RS-422 and RS-485.

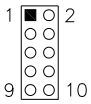
Pin #	Signal Name		
	RS-232	**R2-422**	**RS-485**
11	DCD	TX-	DATA-
13	RX	TX+	DATA+
15	TX	RX+	NC
17	DTR	RX-	NC
19	Ground	Ground	Ground
12	DSR	NC	NC
14	RTS	NC	NC
16	CTS	NC	NC
18	RI	NC	NC
20	NC	NC	NC

J12: Audio Connector (DF11 Connector)



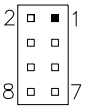
Signal Name	Pin #	Pin #	Signal Name
LINEOUT_R	2	1	LINEOUT_L
Ground	4	3	JD_FRONT
LINEIN_R	6	5	LINEIN
Ground	8	7	JD_LINEIN
MIC-In	10	9	MIC_L
Ground	12	11	JD_MIC1

JP11: Digital I/O

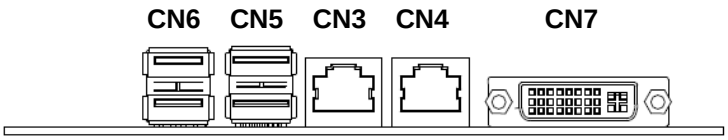


Signal Name	Pin	Pin	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

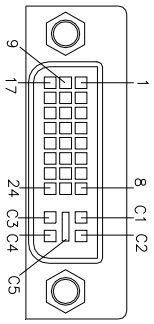
JP3, JP4: USB3~USB6 Connector(DF11 Connector)



Signal Name	Pin	Pin	Signal Name
Ground	2	1	Vcc
D4+	4	3	D3-
D4-	6	5	D3+
Vcc	8	7	Ground



CN7: DVI-I Connector



Signal Name	Pin #	Pin #	Signal Name
DATA 2-	1	16	HOT POWER
DATA 2+	2	17	DATA 0-
Shield 2/4	3	18	DATA 0+
DATA 4-	4	19	SHIELD 0/5
DATA 4+	5	20	DATA 5-
DDC CLOCK	6	21	DATA 5+
DDC DATA	7	22	SHIELD CLK
Anlog-Vsync	8	23	CLOCK -
DATA 1-	9	24	CLOCK +
DATA 1+	10	C1	Anlog-Red
SHIELD 1/3	11	C2	Anlog-Green
DATA 3-	12	C3	Anlog-Blue
DATA 3+	13	C4	Anlog-Hync
DDC POWER	14	C5	A GROUND2
A GROUND 1	15	C6	A GROUND3

CN5: USB3.0 Connector

CN6: USB2.0 Connector

CN4: Gigabit LAN (Intel 82579LM)

CN3: Gigabit LAN (Intel 82583V)

J5: Mini-PCIE Connector

CN1, CN2: SATA Connectors

JP12: LPC Debug Connector (Factory use only)

JP1: SPI Flash Connector (Factory use only)

BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

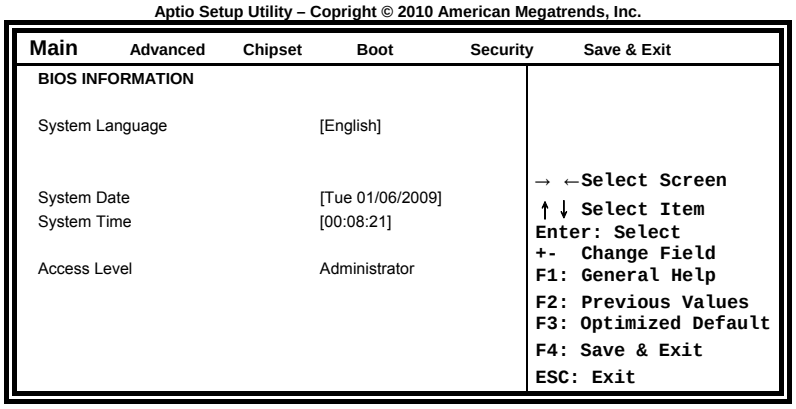
```
Press  <DEL> or <F2> to  Enter  Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Main BIOS Setup

This setup allows you to record some basic hardware configurations in your computer system and set the system clock.



***Note**: If the system cannot boot after making and saving system changes with Setup, the AMI BIOS supports an override to the CMOS settings that resets your system to its default.*

***Warning:** It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.*

System Language

Choose the system default language.

System Date

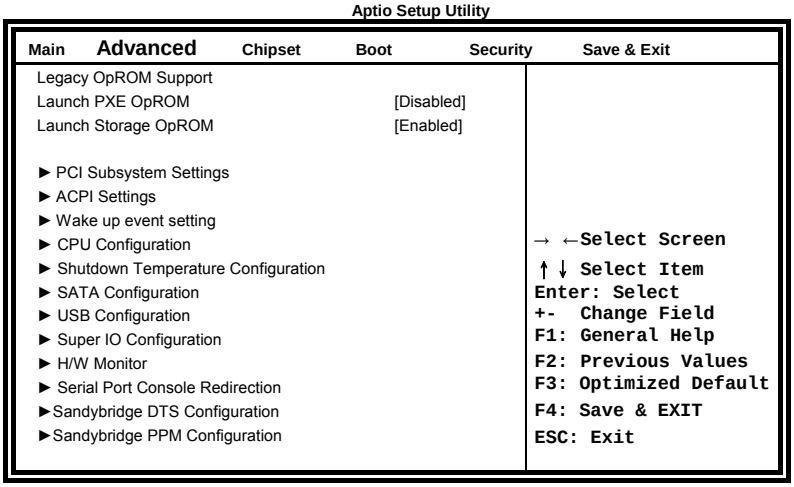
Set the Date. Use Tab to switch between Data elements.

System Time

Set the Time. Use Tab to switch between Data elements.

Advanced Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



Launch PXE OpROM

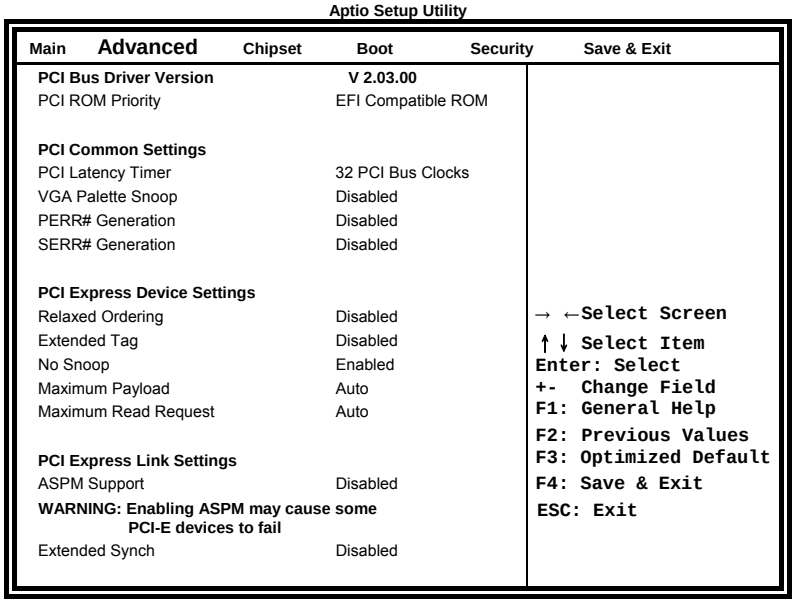
Enable or Disable Boot Option for Legacy Network Devices.

Launch Storage OpROM

Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM.

PCI Subsystem Settings

This section allows you to configure the PCI, PCI-X and PCI Express settings.



PCI ROM Priority

In case of multiple Option ROMs (Legacy and EFI Compatible), specifies what PCI Option ROM to launch.

PCI Latency Timer

Value to be programmed into PCI Latency Timer Register.

VGA Palette Snoop

Enables or Disables VGA Palette Registers Snooping.

PERR# Generation

Enables or Disables PCI Device to Generate PERR#.

SERR# Generation

Enables or Disables PCI Device to Generate SERR#.

Relaxed Ordering

Enables or Disables PCI Express Device Relaxed Ordering.

Extended Tag
If ENABLED allows Device to use 8-bit Tag field as a requester.

No Snoop
Enables or Disables PCI Express Device No Snoop option.

Maximum Payload
Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

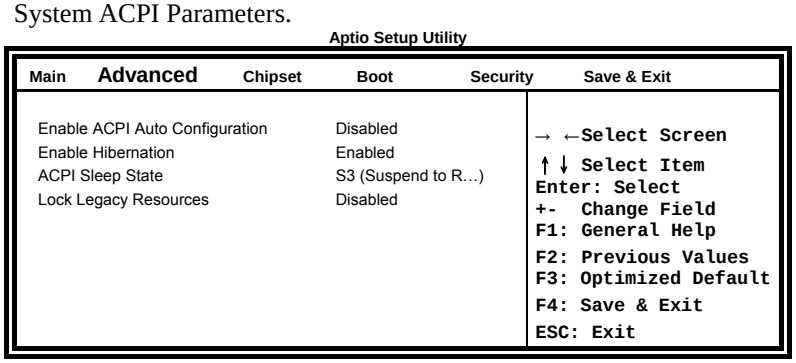
Maximum Read Request
Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

ASPM Support
Set the ASPM Level: Force L0- Force all links to L0 Stage:
AUTO – BIOS auto configure:
DISABLE- Disables ASPM.

Extended Synch
If ENABLED allows generation of Extended Synchronization patterns.

ACPI Settings

System ACPI Parameters.



Enable ACPI Auto Configuration

Enables or Disables BIOS ACPI Auto Configuration.

Enable Hibernation

Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State

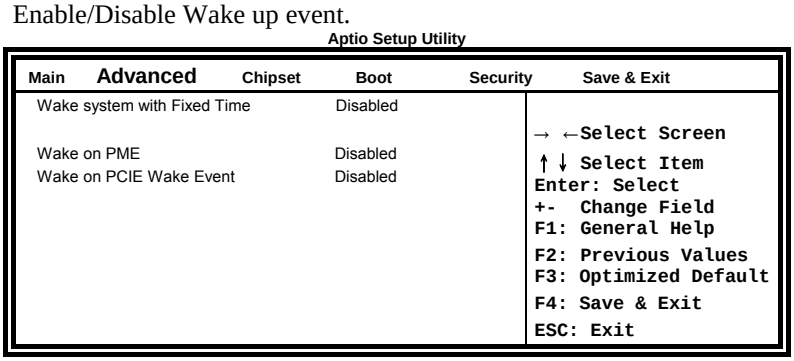
Select the highest ACPI sleep state the system will enter, when the SUSPEND button is pressed.

Lock Legacy Resources

Enables or Disables System Lock of Legacy Resources.

Wake up event settings

Enable/Disable Wake up event.



Wake system with Fixed Time

Enables or Disables System wake on alarm event. When enabled, System will wake on the hr::min:: sec specified.

Wake on Ring

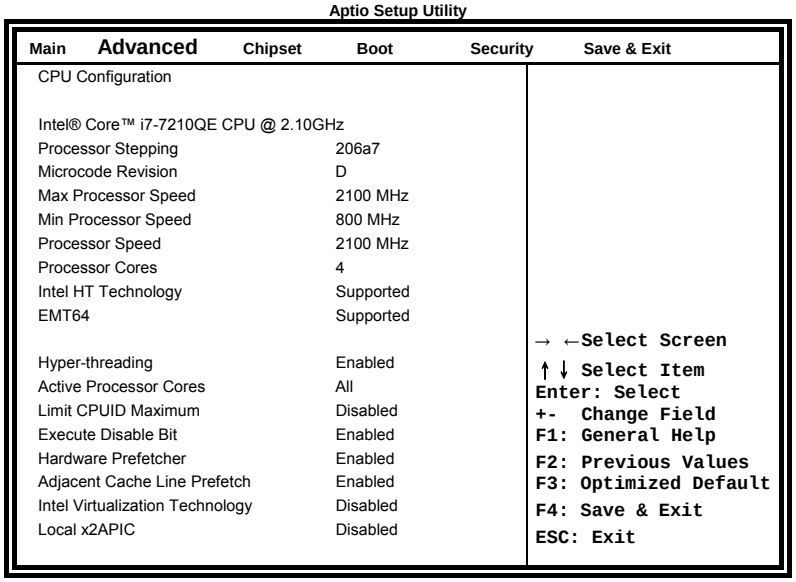
The options are Disabled and Enabled.

Wake on PCIE Wake Event

The options are Disabled and Enabled.

CPU Configuration

This section shows the CPU configuration parameters.



Hyper-threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled, only one thread per enabled core is enabled.

Active Processor Cores

Number of cores to enable in each processor package.

Limit CPUID Maximum

Disabled for Windows XP.

Execute Disable Bit

XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3.)

Hardware Prefetcher

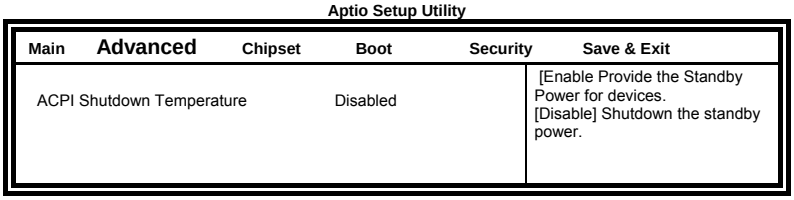
To turn on/off the MLC streamer prefetcher.

Adjacent Cache Line Prefetch
To turn on/off prefetching of adjacent cache lines.

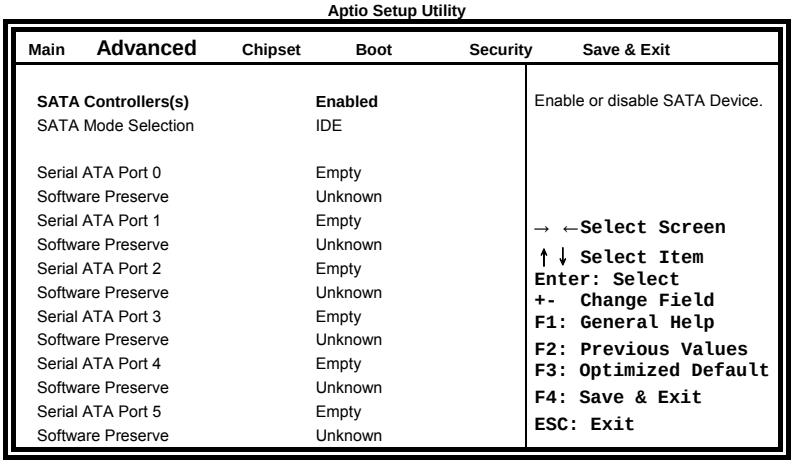
Intel Virtualization Technology
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology

Local x2APIC
Enable Local x2APIC. Some OSes do not support this.

Shutdown Temperature Configuration
The default setting is Disabled.



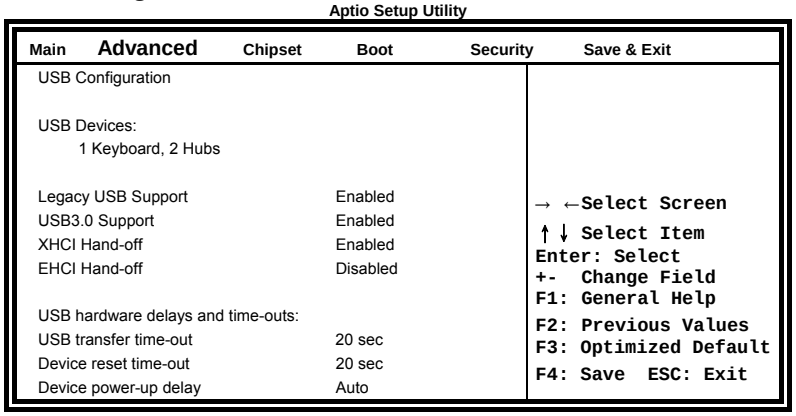
SATA Configuration
SATA Device Options Settings



SATA Mode
Determines how SATA controllers(s) operate. The options are IDE, AHCI and RAID.

USB Configuration

USB Configuration Parameters.



Legacy USB Support

Enables Legacy USB support.
AUTO option disables legacy support if no USB devices are connected.
DISABLE option will keep USB devices available only for EFI applications.

USB3.0 Support

Enable/Disable USB3.0 (XHCI) Controller support.

XHCI Hand-off
This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

EHCI Hand-off
This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

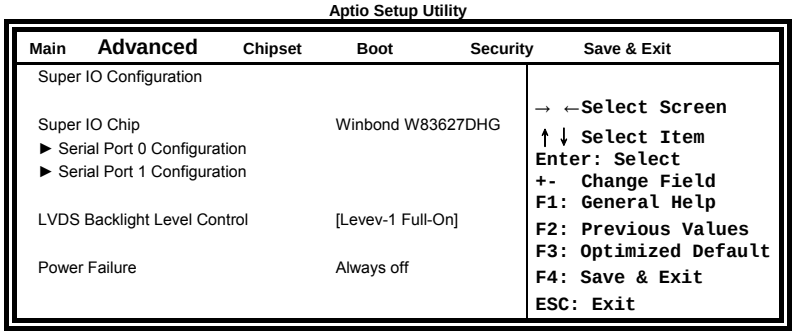
USB transfer time-out
The time-out value for Control, Bulk, and Interrupt transfers.

Device reset time-out
USB mass storage device Start Unit command time-out.

Device power-up delay
Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a hub port the delay is taken from Hub Descriptor.

Super IO Configuration

System Super IO Chip Parameters.



Serial Port Configuration

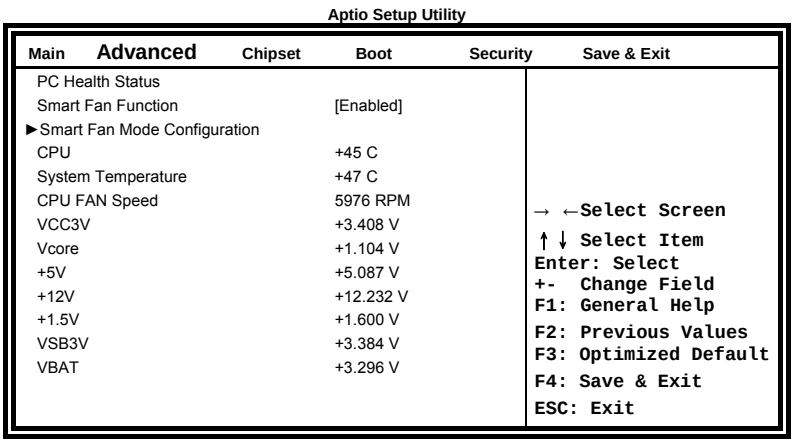
Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.

Power Failure

Options are:
Keep last state
Always on
Always off (default)

H/W Monitor

Monitor hardware status.



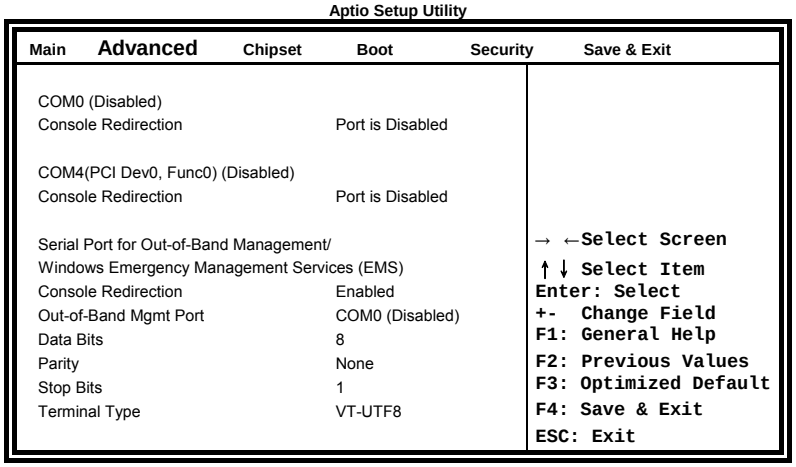
Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

Smart Fan Mode Configuration

This field enables (55C/60C/65C/70C) or disables the smart fan feature. At a certain temperature, the fan starts turning. Once the temperature drops to a certain level, it stops turning again.

Serial Port Console Redirection



Console Redirection

Console Redirection Enable/Disable.

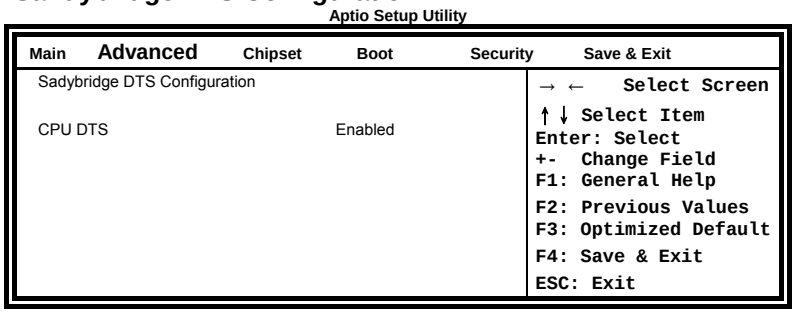
Out-of-Band Mgmt Port

Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.

Terminal Type

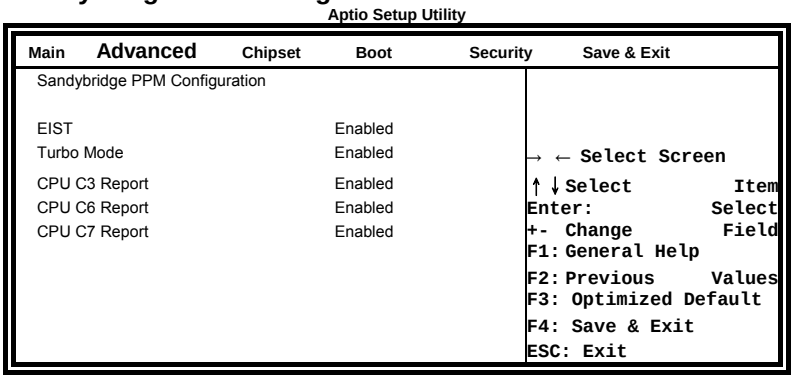
VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100.

Sandybridge DTS Configuration



CPU DTS
Disabled: ACPI thermal management uses EC reported temperature values.
Enabled: ACPI thermal management uses DTS SMM mechanism to obtain CPU temperature values.
Out of Spec: ACPI Thermal Management uses EC reported temperature values and TS SMM is used to handle Out of Spec.

Sandybridge PPM Configuration



EIST
Enable/Disable Intel SpeedStep.

Turbo Mode
Turbo Mode.

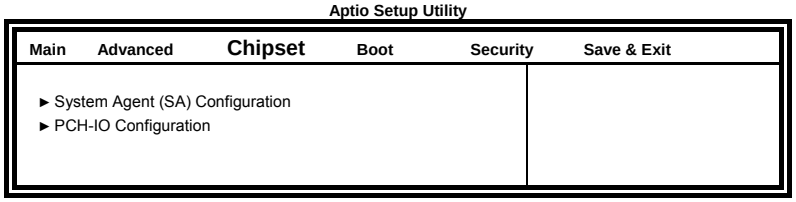
CPU C3 Report
Enable/Disable CPU C3 (ACPI C2) report to OS.

CPU C6 Report
Enable/Disable CPU C6 (ACPI C3) report to OS.

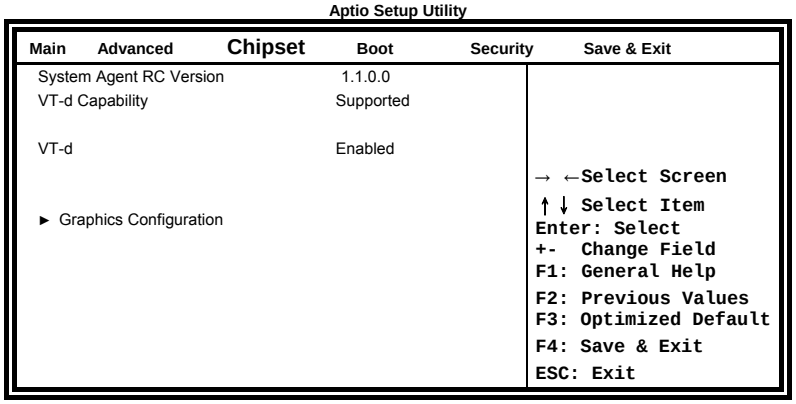
CPU C7 Report
Enable/Disable CPU C7 (ACPI C3) report to OS.

Chipset Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



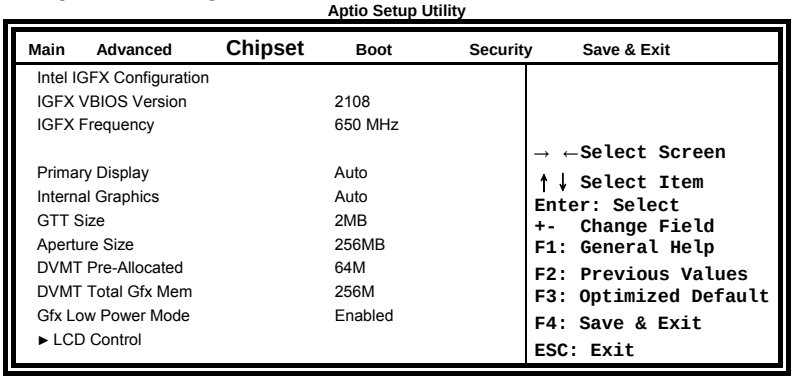
System Agent (SA) Configuration



VT-d

Check to enable VT-d function on MCH.

Graphics Configuration



Primary Display
Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.

Internal Graphics
Keep IGD enabled based on the setup options.

GTT Size
Select the GTT Size: 1MB, 2MB.

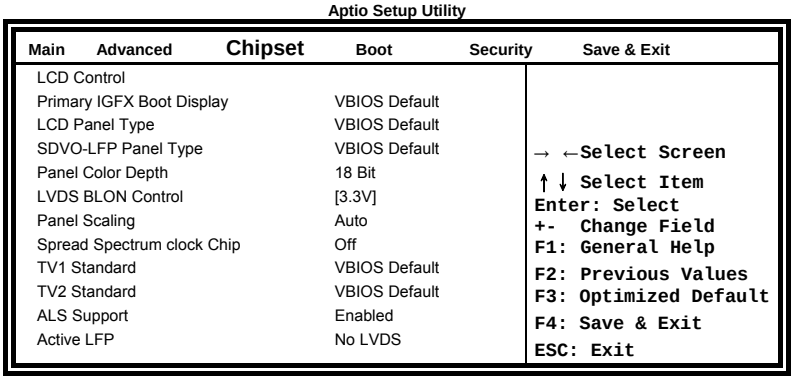
Aperture Size
Select the Aperture Size: 128MB, 256MB, 512MB.

DVMT Pre-Allocated
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device: 0M~512M.

DVMT Total Gfx Mem
Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device: 128M, 256M, MAX.

Gfx Low Power Mode
This option is applicable for SFF only.

LCD Control



Primary IGFX Boot Display

Select the Video Device that will be activated during PoST. This has no effect if external graphics present.
Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.

Active LFP

Select the Active LFP Configuration.
No LVDS: VBIOS does not enable LVDS.
Int-LVDS: VBIOS enables LVDS driver by Integrated encoder.
SDVO LVDS: VBIOS enables LVDS driver by SDVO encoder.
eDP Port-A: LFP Driven by Int-DisplayPort encoder from Port-A.

Panel Color Depth

Select the LFP Panel Color Depth: 18 Bit, 24 Bit.

LVDS BLON Control

Select the LFP Panel Inverted voltage: 3.3V, 5V.

LCD Panel Type

Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item: 640x480 LVDS ~ 2048x1536 LVDS.

SDVO-LFP Panel Type

Select SDVO panel used by Internal Graphics Device by selecting the appropriate setup item: VBIOS Default, 1024x768 ~ 1600x1200.

Panel Scaling
Select the LCD panel scaling option used by the Internal Graphics Device: Auto, Off, Force Scaling.

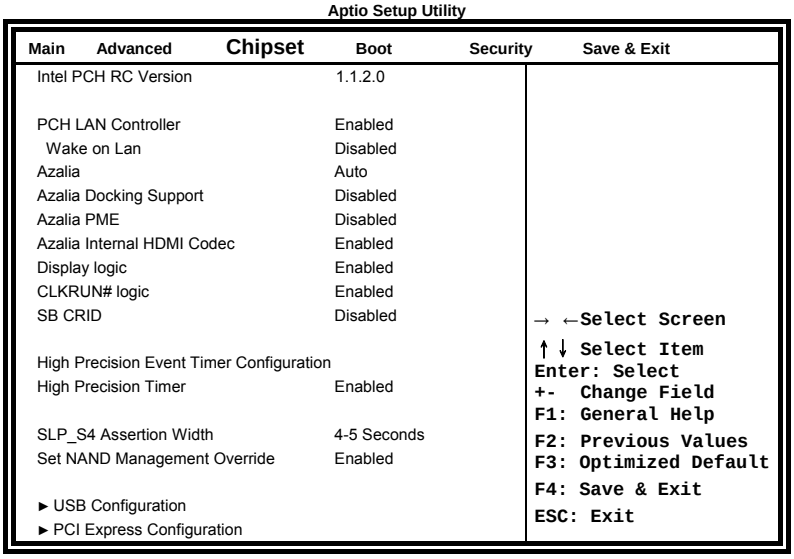
Spread Spectrum clock Chip
Hardware: Spread is controlled by chip;
Software: Spread is controlled by BIOS.

TV1 Standard
Select the ability to configure a TV Format.

TV2 Standard
Select the ability to configure a TV Minor Format.

ALS Support
Valid only for ACPI.
Legacy = ALS Support though the IGD INT 10 function.
ACI = ALS support through an ACPI ALS driver.

PCH-IO Configuration



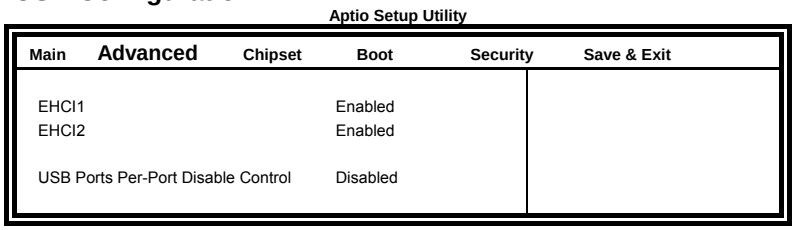
Azalia

Control Detection of the Azalia device.
Disabled = Azalia will be unconditionally disabled.
Enabled = Azalia will be unconditionally enabled. Auto = Azalia will be enabled if present, disabled otherwise.

Set NAND Management Override

Option to Override NAND Management to allow driver or 3rd parties software to configure the NAND module after POST.

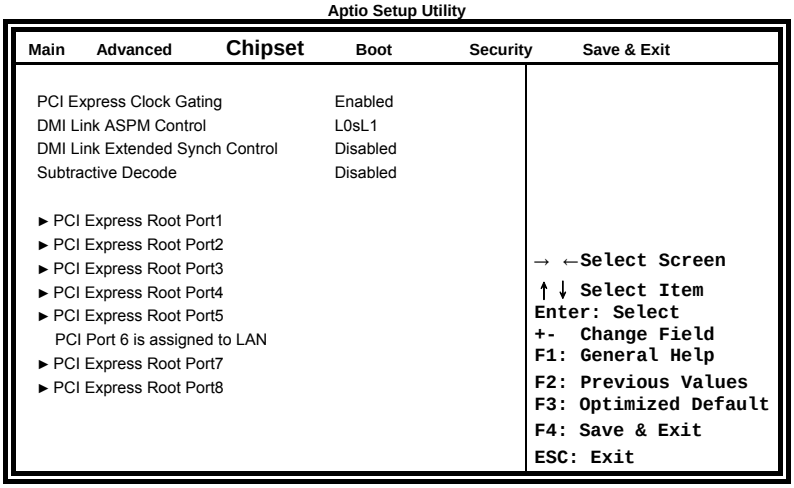
USB Configuration



EHCI1

Control the USB EHCI (USB2.0) functions.
One EHCI controller must always be enabled.

PCI Express Configuration



DMI Clink ASPM Control

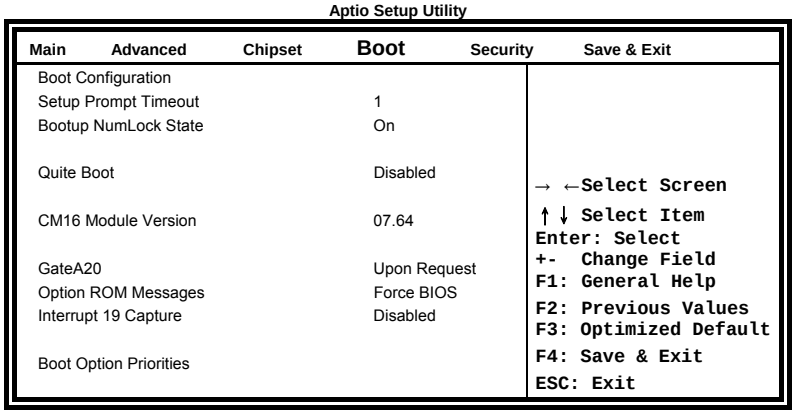
The control of Active State Power Management on both NB side and SB side of the DMI Link.

DMI Link Extended Synch Control

The control of Extended Synch on SB side of the DMI Link.

Boot Settings

This section allows you to configure the boot settings according to your preference.



Setup Prompt Timeout

Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

GateA20 Active

UPON REQUEST – GA20 can be disabled using BiOS services.
ALWAYS – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

Option ROM Messages

Set display mode for Option ROM. Options are Force BIOS and Keep Current.

Interrupt 19 Capture

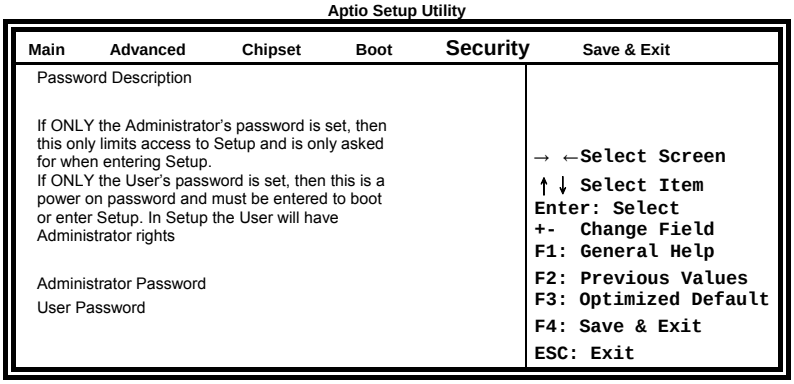
Enable: Allows Option ROMs to trap Int 19.

Boot Option Priorities

Sets the system boot order.

Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



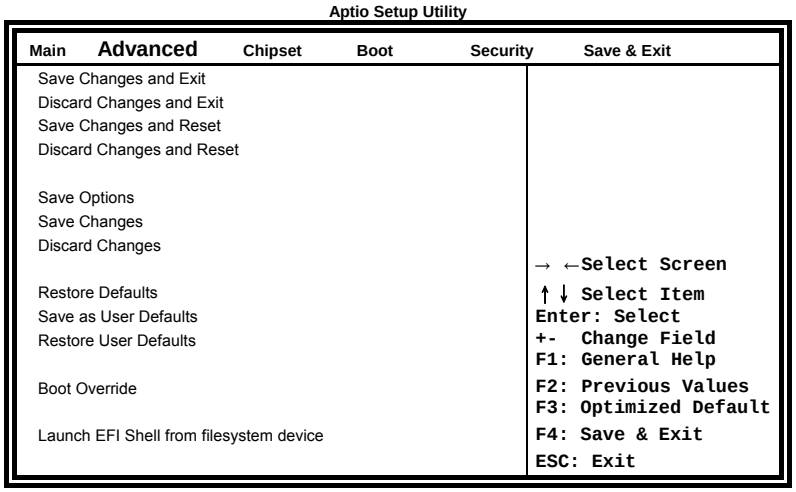
Administrator Password

Set Setup Administrator Password.

User Password

Set User Password.

Save & Exit Settings



Save Changes and Exit
Exit system setup after saving the changes.

Discard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save Changes done so far to any of the setup options.

Discard Changes
Discard Changes done so far to any of the setup options.

Restore Defaults
Restore/Load Defaults values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

Boot Override
Pressing ENTER causes the system to enter the OS.

Launch EFI Shell from filesystem device
Attempts to Launch EFI Shell application (Shellx64.efi) from one of the available filesystem devices.

Drivers Installation

This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

IMPORTANT NOTE:
After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

Intel Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) QM67/Q67 Chipset Drivers***.

2. Click ***Intel(R) Chipset Software Installation Utility.***

3. When the Welcome screen to the Intel® Chipset Device Software appears, click ***Next*** to continue.

4. Click ***Yes*** to accept the software license agreement and proceed with the installation process.

5. On the Readme File Information screen, click ***Next*** to continue the installation.

6. The Setup process is now complete. Click ***Finish*** to restart the computer and for changes to take effect.

VGA Drivers Installation

NOTE: Before installing the *Intel(R) QM67 Chipset Family Graphics Driver,* the Microsoft .NET Framework 3.5 SPI should be first installed.

To install the VGA drivers, follow the steps below.
1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) QM67/Q67 Chipset Drivers***.

2. Click ***Intel(R) QM67 Chipset Family Graphics Driver.***

3. When the Welcome screen appears, click ***Next*** to continue.

4. Click ***Yes*** to to agree with the license agreement and continue the installation.

5. On the Readme File Information screen, click ***Next*** to continue the installation of the Intel® Graphics Media Accelerator Driver.

6. On Setup Progress screen, click ***Next*** to continue.

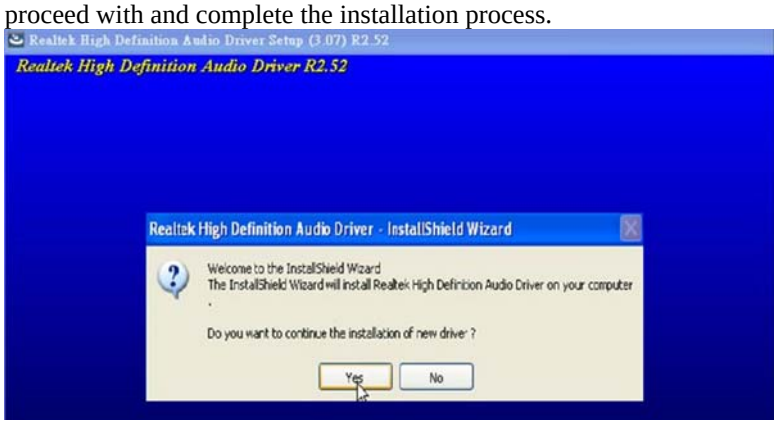
7. Setup complete. Click ***Finish*** to restart the computer and for changes to take effect.

Realtek HD Audio Driver Installation

Follow the steps below to install the Realtek HD Audio Drivers.
1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) QM67/Q67 Chipset Drivers***.

2. Click ***Realtek High Definition Audio Driver.***

3. On the Welcome to the InstallShield Wizard screen, click ***Yes*** to proceed with and complete the installation process.



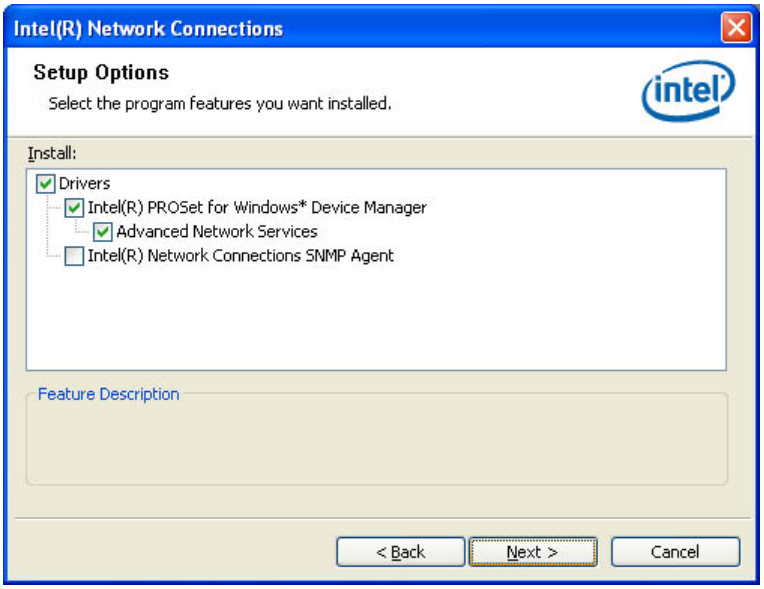
LAN Drivers Installation

1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) QM67/Q67 Chipset Drivers***.

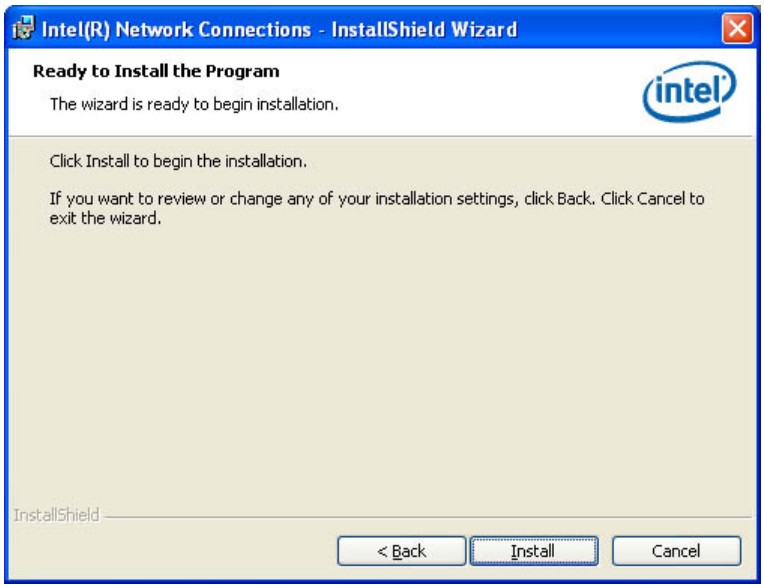
2. Click ***Intel(R) PRO LAN Network Driver.***

3. When the Welcome screen appears, click ***Next***. On the next screen, click ***Yes*** to to agree with the license agreement.

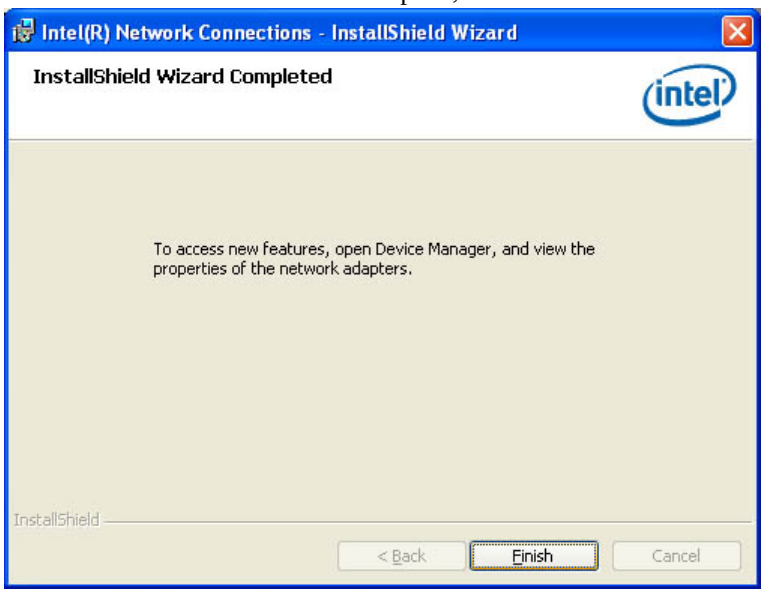
4. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.



5. The wizard is ready to begin installation. Click ***Install*** to begin the installation.



6. When InstallShield Wizard is complete, click ***Finish***.



ASMedia USB 3.0 Drivers

1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) QM67/Q67 Chipset Drivers***.

2. Click ***Intel(R) PRO LAN Network Driver.***

2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click ***Next***.

3. When InstallShield Wizard is complete, click ***Finish***.

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Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 064h	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
E000-E01F	Network Connection
F060-F07F	Network Connection
F080-F0D7	SATA Storage Controller
2F8h - 2FFh	Serial Port #2(COM2)
3B0h- 3BBh	Graphics adapter Controller
3F8h - 3FFh	Serial Port #1(COM1)
3D0h - 3DFh	CGA adapter

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Reserved
IRQ6	Reserved
IRQ7	Reserved
IRQ8	Real Time Clock
IRQ9	Reserved
IRQ10	Serial Port #3
IRQ11	Serial Port #4
IRQ12	PS/2 Mouse
IRQ13	80287
IRQ14	Primary IDE
IRQ15	Secondary IDE
IRQ19	SATA Storage

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//=====================================================================
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=====================================================================
#include <stdio.h>
#include <stdlib.h>
#include "W627DHG.H"
//=====================================================================
int main (int argc, char *argv[]);
void copyright(void);
void EnableWDT(int);
void DisableWDT(void);
//=====================================================================
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        copyright();

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return 1;
        }

        if (Init_W627DHG() == 0)
        {
                printf(" Winbond 83627HF is not detected, program abort.\n");
                return 1;
        }
        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        EnableWDT(bTime);

        return 0;
}
//=====================================================================
```

```
void copyright(void)
{
        printf("\n======== Winbond 83627DHG Watch Timer Tester (AUTO DETECT) ========\n"\
                        "       Usage : W627E_WD reset_time\n"\
                        "       Ex : W627E_WD 3  => reset system after 3 second\n"\
                        "            W627E_WD 0  => disable watch dog timer\n");
}
//============================================================================
void EnableWDT(int interval)
{
        unsigned char bBuf;

        bBuf = Get_W627DHG_Reg( 0x2D);
        bBuf &= (!0x01);
        Set_W627DHG_Reg( 0x2D, bBuf);                   //Enable WDTO

        Set_W627DHG_LD( 0x08);                          //switch to logic device 8
        Set_W627DHG_Reg( 0x30, 0x01);                   //enable timer

        bBuf = Get_W627DHG_Reg( 0xF5);
        bBuf &= (!0x08);
        Set_W627DHG_Reg( 0xF5, bBuf);                   //count mode is second

        Set_W627DHG_Reg( 0xF6, interval);               //set timer
}
//============================================================================
void DisableWDT(void)
{
        Set_W627DHG_LD(0x08);                           //switch to logic device 8
        Set_W627DHG_Reg(0xF6, 0x00);                    //clear watchdog timer
        Set_W627DHG_Reg(0x30, 0x00);                    //watchdog disabled
}
//============================================================================
```

```
//===========================================================================
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//===========================================================================
#include "W627DHG.H"
#include <dos.h>
//===========================================================================
unsigned int W627DHG_BASE;
void Unlock_W627DHG (void);
void Lock_W627DHG (void);
//===========================================================================
unsigned int Init_W627DHG(void)
{
	unsigned int result;
	unsigned char ucDid;

	W627DHG_BASE = 0x2E;
	result = W627DHG_BASE;

	ucDid = Get_W627DHG_Reg(0x20);
	if (ucDid == 0x88)
	{	goto Init_Finish;	}

	W627DHG_BASE = 0x4E;
	result = W627DHG_BASE;
	ucDid = Get_W627DHG_Reg(0x20);
	if (ucDid == 0x88)
	{	goto Init_Finish;	}

	W627DHG_BASE = 0x00;
	result = W627DHG_BASE;

Init_Finish:
	return (result);
}
//===========================================================================
void Unlock_W627DHG (void)
{
	outportb(W627DHG_INDEX_PORT, W627DHG_UNLOCK);
	outportb(W627DHG_INDEX_PORT, W627DHG_UNLOCK);
}
//===========================================================================
void Lock_W627DHG (void)
{
	outportb(W627DHG_INDEX_PORT, W627DHG_LOCK);
}
//===========================================================================
void Set_W627DHG_LD( unsigned char LD)
{
	Unlock_W627DHG();
	outportb(W627DHG_INDEX_PORT, W627DHG_REG_LD);
	outportb(W627DHG_DATA_PORT, LD);
	Lock_W627DHG();
}
```

```
//=============================================================================
void Set_W627DHG_Reg( unsigned char REG, unsigned char DATA)
{
        Unlock_W627DHG();
        outportb(W627DHG_INDEX_PORT, REG);
        outportb(W627DHG_DATA_PORT, DATA);
        Lock_W627DHG();
}
//=============================================================================
unsigned char Get_W627DHG_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_W627DHG();
        outportb(W627DHG_INDEX_PORT, REG);
        Result = inportb(W627DHG_DATA_PORT);
        Lock_W627DHG();
        return Result;
}
//=============================================================================




//=============================================================================
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//
//=============================================================================
#ifndef __W627DHG_H
#define __W627DHG_H                     1
//=============================================================================
#define         W627DHG_INDEX_PORT          (W627DHG_BASE)
#define         W627DHG_DATA_PORT           (W627DHG_BASE+1)
//=============================================================================
#define         W627DHG_REG_LD              0x07
//=============================================================================
#define W627DHG_UNLOCK                      0x87
#define         W627DHG_LOCK                0xAA
//=============================================================================
unsigned int Init_W627DHG(void);
void Set_W627DHG_LD( unsigned char);
void Set_W627DHG_Reg( unsigned char, unsigned char);
unsigned char Get_W627DHG_Reg( unsigned char);
//=============================================================================
#endif  //__W627DHG_H
```