

Approval Sheet

Customer	
Product Number	M4M0-8GS15CSJ
Module speed	PC4-2400
Pin	288 pin
Cl-tRCD-tRP	17-17-17
Operating Temp	0°C ~85°C
Date	8 th September 2017

Rev 1.1

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
		CL=13	CL=15	CL=17			
PC4-2400	S	1866	2133	2400	14.16	14.16	46.16

- JEDEC Standard 288-pin Mini Registered Dual In-Line Memory Module
- Intend for PC4-2400 applications
- Inputs and Outputs are SSTL-12 compatible
- VDD=VDDQ= 1.2 Volt (1.14V~1.26V)
- VPP=2.5 Volt (2.375V~2.75V)
- VDDSPD=2.2-3.6V
- Low-Power auto self-refresh (LPASR)
- SDRAMs have 16 internal banks for concurrent operation (4 Bank Group of 4 banks each)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals.
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Golden Connector :30u"
- Fly-By topology
- Terminated control, command and address bus
- Programmable /CAS Latency: 10,11,12,13,14,15,16,17,18
- Operation temperature – (0°C~85°C)
- On-die VREFDQ generation and Calibration
- On-Board EEPROM
- RoHS and Halogen free (Section 13)
- Temperature Sensor with SPD EEPROM

2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	See Note	°C	1
TSTG	Storage Temperature	-50 to +100	°C	
HOPR	Operating Humidity (relative)	10 to 90	%	
HSTG	Storage Humidity (without condensation)	5 to 95	%	
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2
1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR4 DRAM component specification. 2. Up to 9850 ft.				

3. SDRAM Parameters by device density

RTT_Nom Setting	Parameter		8Gb	Units
tREFI	Average periodic refresh interval	$0^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85^{\circ}\text{C}$	7.8	μs
		$85^{\circ}\text{C} < T_{\text{CASE}} \leq 95^{\circ}\text{C}$	3.9	μs

4. Ordering Information

DDR4 VLP Mini-RDIMM w/ ECC						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M4M0-8GS15CSJ	8GB	PC4-2400	1Gx72	9	1	Y

5. Pin Configurations (Front side/Back side)

DDR4 1Gx8 base Mini-RDIMM w/ ECC

Front	Pins	Back	Front	Pins	Back	Front	Pins	Back			
NC	1	145	VREPCA	ALERT_n	60	204	RESET_n	DQ32	96	240	DQ36
NC	2	146	SAVE_n, NC	CKE0	61	205	RFU	VSS	97	241	VSS
RFU	3	147	RFU	VDD	62	206	VDD	DQ33	98	242	DQ37
VSS	4	148	VSS	ACT_n	63	207	CKE1, NC	VSS	99	243	VSS
DQ0	5	149	DQ4	BG0	64	208	BG1	DQS4_c	100	244	DQS13_t %
VSS	6	150	VSS	VDD	65	209	VDD	DQS4_t	101	245	DQS13_c *
DQ1	7	151	DQ5	A12/BC_n	66	210	A11	VSS	102	246	VSS
VSS	8	152	VSS	A9	67	211	A7	DQ34	103	247	DQ38
DQS0_c	9	153	DQS9_t %	VDD	68	212	VDD	VSS	104	248	VSS
DQS0_t	10	154	DQS9_c *	A8	69	213	A5	DQ35	105	249	DQ39
VSS	11	155	VSS	A6	70	214	A4	VSS	106	250	VSS
DQ2	12	156	DQ6	VDD	71	215	VDD	DQ40	107	251	DQ44
VSS	13	157	VSS	A3	72	216	A2	VSS	108	252	VSS
DQ3	14	158	DQ7	A1	73	217	RFU	DQ41	109	253	DQ45
VSS	15	159	VSS	VDD	74	218	VDD	VSS	110	254	VSS
DQ8	16	160	DQ12	CK0_t	75	219	CK1_t	DQS5_c	111	255	DQS14_t %
VSS	17	161	VSS	CK0_c	76	220	CK1_c	DQS5_t	112	256	DQS14_c *
DQ9	18	162	DQ13	VDD	77	221	VDD	VSS	113	257	VSS
VSS	19	163	VSS	RFU	78	222	RFU	DQ42	114	258	DQ46
DQS1_c	20	164	DQS10_t %	VTT	79	223	VTT	VSS	115	259	VSS
DQS1_t	21	165	DQS10_c *	Key				DQ43	116	260	DQ47
VSS	22	166	VSS	EVENT_n	80	224	PARITY	VSS	117	261	VSS
DQ10	23	167	DQ14	VDD	81	225	VDD	DQ48	118	262	DQ52
VSS	24	168	VSS	A0	82	226	BA1	VSS	119	263	VSS
DQ11	25	169	DQ15	BA0	83	227	A10/AP	DQ49	120	264	DQ53
VSS	26	170	VSS	VDD	84	228	VDD	VSS	121	265	VSS
DQ16	27	171	DQ20	RAS_n/A16	85	229	A14 WE_n	DQS6_c	122	266	DQS15_t %
VSS	28	172	VSS	CS0_n	86	230	A15 CAS_n	DQS6_t	123	267	DQS15_c *
DQ17	29	173	DQ21	VDD	87	231	VDD	VSS	124	268	VSS
VSS	30	174	VSS	ODT0	88	232	A13	DQ50	125	269	DQ54
DQS2_c	31	175	DQS11_t %	CS1_n, NC	89	233	A17, NC	VSS	126	270	VSS
DQS2_t	32	176	DQS11_c *	VDD	90	234	VDD	DQ51	127	271	DQ55
VSS	33	177	VSS	ODT1, NC	91	235	C1, CS3_n, NC	VSS	128	272	VSS
DQ18	34	178	DQ22	C0, CS2_n, NC	92	236	NC, C2	DQ56	129	273	DQ60
VSS	35	179	VSS	VDD	93	237	VDD	VSS	130	274	VSS
DQ19	36	180	DQ23	RFU	94	238	RFU	DQ57	131	275	DQ61
VSS	37	181	VSS	VSS	95	239	VSS	VSS	132	276	VSS
DQ24	38	182	DQ28					DQS7_c	133	277	DQS16_t %
VSS	39	183	VSS					DQS7_t	134	278	DQS16_c *
DQ25	40	184	DQ29					VSS	135	279	VSS
VSS	41	185	VSS					DQ58	136	280	DQ62
DQS3_c	42	186	DQS12_t %					VSS	137	281	VSS
DQS3_t	43	187	DQS12_c *					DQ59	138	282	DQ63
VSS	44	188	VSS					VSS	139	283	VSS
DQ26	45	189	DQ30					SA0	140	284	SA1
VSS	46	190	VSS					VDDSPD	141	285	SA2
DQ27	47	191	DQ31					SDA	142	286	SCL
VSS	48	192	VSS					VPP	143	287	VPP
CB0, NC	49	193	CB4, NC					VPP	144	288	VPP
VSS	50	194	VSS								
CB1, NC	51	195	CB5, NC								
VSS	52	196	VSS								
DQS8_c	53	197	DQS17_t %								
DQS8_t	54	198	DQS17_c *								
VSS	55	199	VSS								
CB2, NC	56	200	CB6, NC								
VSS	57	201	VSS								
CB3, NC	58	202	CB7, NC								
VSS	59	203	VSS								

CS pin will based on Chip and Module configuration, normal CS2 and CS3 will be NC

% These signals include TDQS_t, BDI_n and DM_n refer to below
Pin153=TDQS9_t/DM0_n, /DBI0_n; Pin164=TDQS10_t/DM1, /DBI1; Pin175=TDQS11_t/D
Pin197=TDQS17_t/DM8, /DBI8; Pin244=TDQS13_t, /DM4, /DBI4; Pin255=TDQS14_t, /DM5,
Pin277=TDQS16_t, /DM7, /DBI7

* These signals include TDQS_c and NC refer to below
Pin154, 165, 176, 187, 198, 245, 256, 267, 278-NC

CS pin will based on Chip and Module configuration, normal CS2 and CS3 will be NC

% These signals include TDQS_t, BDI_n and DM_n refer to below

Pin153=TDQS9_t/DM0_n, /DBI0_n; Pin164=TDQS10_t/DM1, /DBI1; Pin175=TDQS11_t/DM2, /DBI2; Pin186=TDQS12_t/DM3, /DBI3
Pin197=TDQS17_t/DM8, /DBI8; Pin244=TDQS13_t/DM4, /DBI4; Pin255=TDQS14_t/DM5, /DBI5; Pin266=TDQS15_t/DM6, /DBI6
Pin277=TDQS16_t/DM7, /DBI7

* These signals include TDQS_c and NC refer to below

Pin154, 165, 176, 187, 198, 245, 256, 267, 278=NC

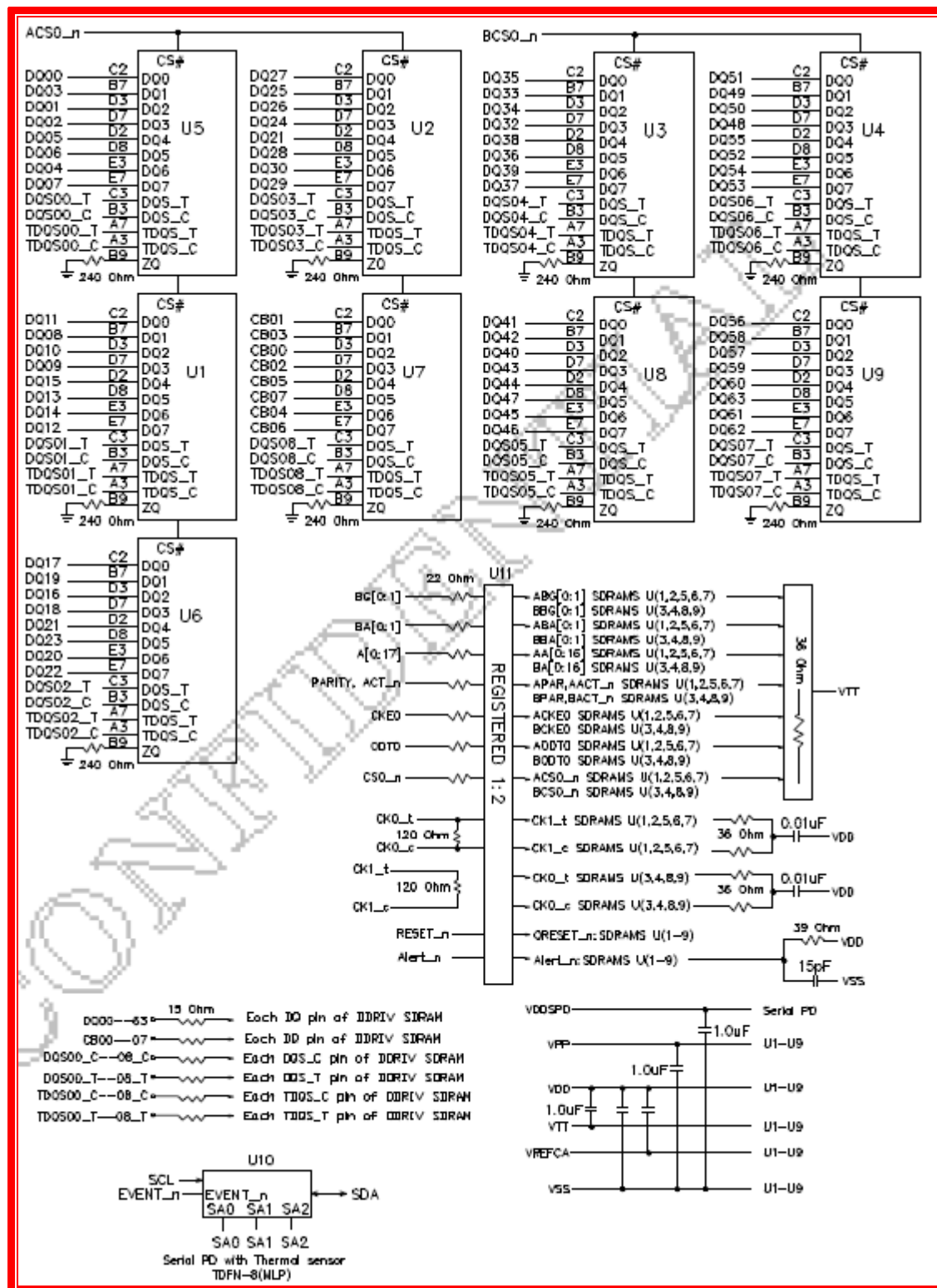
6. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0-A17	Register address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I2C serial bus data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0-SA2	I2C slave address select for SPD/TS and register
RAS_n	Register row address strobe input	PAR	Register parity input
CAS_n	Register column address strobe input	VDD	SDRAM core power supply
WE_n	Register write enable input	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input activate input	ALERT_n	Register ALERT_n output
DQ0-DQ63	DIMM memory data bus	RESET_n	Set Register and SDRAMs to a Known State
CB0-CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t-DQS17_t	Data buffer data strobes (positive)	VTT	SDRAM I/O termination supply
DQS0_c-DQS17_c	Data buffer data strobes (negative)	RFU	Reserved for future use
CK0_t, CK1_t	Register clock input (positive)		
CK0_c, CK1_c	Register clock input (negative)		

7. Function Block Diagram:

- (8GB, 1 Rank 1Gx8 DDR4 SDRAMs)



8. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.3 to +1.5	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.3 to +1.5	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.3 to +1.5	V	4,6

Note:

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM.

For measurement conditions, please refer to the JEDEC document JESD51-2.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.

3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stressing only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

9. Module Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.3 to +1.5	V	
V_{DD}	Voltage on VDD supply relative to Vss	-0.3 to +1.5	V	1
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.3 to +1.5	V	1
V_{PP}	Voltage on VPP supply relative to Vss	-0.3 to +3.0	V	2
Note: 1. VDDQ tracks with VDD; VDDQ and VDD are tied together. 2. VPP must be greater than or equal to VDD at all times.				

10. Operating Condition

Symbol	Parameter	Min	Nom	Max	Units	Notes
V _{DD}	Supply Voltage	1.14	1.2	1.26	V	1
V _{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
V _{REFCA(DC)}	Input reference voltage command/ address bus	0.49 x V _{DD}	0.5 x V _{DD}	0.51 x V _{DD}	V	3
I _{VTT}	Termination reference voltage (DC) – command/address bus	-750	-	750	mA	
V _{TT}	Termination Voltage	0.49 × V _{DD}	0.5 × V _{DD}	0.51 × V _{DD}	V	4
I _I	Input leakage current; any input excluding ZQ; 0V < V _{IN} < 1.1V	-2.0	-	2.0	μA	5
I _{I/O}	DQ leakage; 0V < V _{in} < V _{DD}	-4.0	-	4.0	μA	5
I _{ozpd}	Output leakage current; V _{OUT} = V _{DD} ; DQ is disabled	-	-	5.0	μA	
I _{ozpu}	Output leakage current; V _{OUT} =V _{SS} ; DQ and ODT are disabled; ODT is disabled with ODT input HIGH	-		5.0	μA	
I _{VREFCA}	VREFCA leakage; VREFCA = V _{DD} /2 (after DRAM is initialized)	-2.0	-	2.0	μA	

Note:

- V_{DDQ} tracks with V_{DD}; V_{DDQ} and V_{DD} are tied together.
- V_{PP} must be greater than or equal to V_{DD} at all times.
- V_{REFCA} must not be greater than 0.6 x V_{DD}. When V_{DD} is less than 500mV, V_{REF} may be less than or equal to 300mV.
- V_{TT} termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.
- Multiply by the number of DRAM die on the module.
- Tied to ground. Not connected to edge connector.

11. Operating, Standby, and Refresh Currents

- 8GB Mini-RDIMM w/ ECC (1 Rank 1Gx8 DDR4 SDRAMs)

Symbol	Proposed Conditions	Value		Units
		IDD Max.	IPP Max.	
IDD0	Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	279	36	mA
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0	306	36	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	405	36	mA
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1	432	36	mA
IDD2N	Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	207	27	mA
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N	234	27	mA

IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern	234	27	mA
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled3	153	27	mA
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled3	207	27	mA
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled3	189	27	mA
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled3	216	27	mA
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	144	27	mA
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	189	27	mA
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	324	27	mA

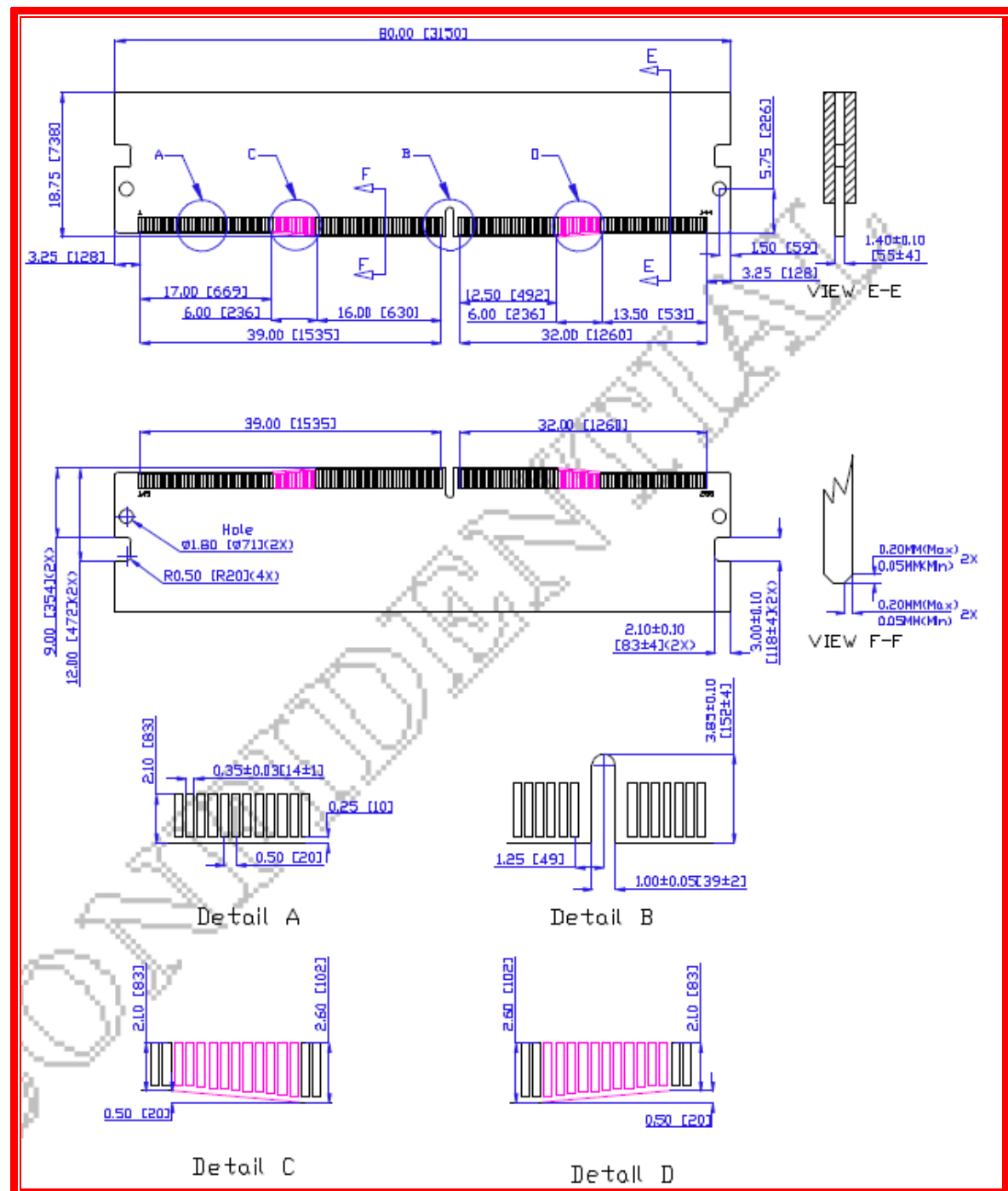
IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N	342	27	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	198	27	mA
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	963	27	mA
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R	999	27	mA
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled3, Other conditions: see IDD4R	981	27	mA
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	801	27	mA
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W	846	27	mA
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions: see IDD4W	810	27	mA

IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled ³ , Other conditions: see IDD4W	747	27	mA
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled ³ , Other conditions: see IDD4W	891	27	mA
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1791	162	mA
IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B	1251	135	mA
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B	1053	126	mA
IDD6N	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MIDLEVEL	207	36	mA
IDD6E	Self-Refresh Current: Extended Temperature Range) TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL	306	45	mA

IDD6R	Self-Refresh Current: Reduced Temperature Range TCASE: 0 - 45 °C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: see Table 34 on p age 37; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	144	45	mA
IDD6A	Auto Self-Refresh Current TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: see Table 34 on p age 37; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	198	45	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1287	76.5	mA
IDD8	Maximum Power Down Current TBD	99	27	mA

12. PACKAGE DIMENSION

- (8GB, 1Rank 1Gx8 DDR4 base Mini-RDIMM w/ ECC)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ± 0.15 (6), unless otherwise specified

13. RoHS Declaration



宜鼎國際股份有限公司
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RoHS 自我宣告書 (RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 關於 RoHS 之規範要求。
Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。
Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
鉛 (Pb)	< 1000 ppm
汞 (Hg)	< 1000 ppm
鎘 (Cd)	< 100 ppm
六價鉻 (Cr 6+)	< 1000 ppm
多溴聯苯 (PBBs)	< 1000 ppm
多溴二苯醚 (PBDEs)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱: Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人: Randy Chien 簡川騰

Company Representative Title 公司代表人職稱: Chairman 董事長

Date 日期: 2016 / 08 / 04




Revision Log

Rev	Date	Modification
0.1	13 rd March 2017	Preliminary Edition
1.0	13 rd March 2017	Official Released
1.1	8 th September 2017	Modified typo