Approval Sheet

Customer	
Product Number	**M3S0-2GSVF4QE**
Module speed	**PC3-14900**
Pin	**204 pin**
Cl-tRCD-tRP	**13-13-13**
DRAM Operating Temp	**-40℃~85℃**
Date	**11st October 2016**

The Total Solution For Industrial Flash Storage

Rev 1.0

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)
		CL=9	CL=11	CL=13			
PC3-14900	T	1333	1600	1866	13.125	13.125	13.125

- JEDEC Standard 204-pin Dual In-Line Memory Module
- Intend for PC3-14900 applications
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.35 Volt (-0.067/+0.1V) or 1.5 Volt (-0.075/+0.075V)
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8μs ($T_C \leq +85°C$)
- 15/10/1 Addressing (row/column/rank)-2GB
- SDRAM operating temperature range $-40°C \leq T_{CASE} \leq +85°C$
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 5,6,7,8,9,10,11,13
  - Burst Length: switch on-the-fly: BL=8 or BC 4
- RoHS Compliant *(Section 13)*

2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	-40 to +85	°C	1
T_{STG}	Storage Temperature	-50 to +100	°C	
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR3 DRAM component specification.
2. Up to 9850 ft.

3. DRAM Parameters by device density

RTT_Nom Setting	Parameter		4Gb	Units
tRFC	REF command ACT or REF command time		260	ns
tREFI	Average periodic refresh interval	-40°C≦T_{CASE}≦**85**°C	7.8	µs
		85°C<T_{CASE}≦**95**°C	3.9	µs

4. Ordering Information

DDR3L W/T Sorting SODIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M3S0-2GSVF4QE	2GB	PC3-14900	256Mx64	4	1	N

5. Pin Configurations (Front side/Back side)

X64 SODIMM

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREFDQ	2	Vss	69	DQ27	70	DQ31	137	DQS4	138	Vss
3	Vss	4	DQ4	71	Vss	72	Vss	139	Vss	140	DQ38
5	DQ0	6	DQ5	73	CKE0	74	CKE1	141	DQ34	142	DQ39
7	DQ1	8	Vss	75	VDD	76	VDD	143	DQ35	144	Vss
9	Vss	10	/DQS0	77	NC	78	A15 ***	145	Vss	146	DQ44
11	DM0	12	DQS0	79	BA2	80	A14 ***	147	DQ40	148	DQ45
13	Vss	14	Vss	81	VDD	82	VDD	149	DQ41	150	Vss
15	DQ2	16	DQ6	83	A12, /BC	84	A11	151	Vss	152	/DQS5
17	DQ3	18	DQ7	85	A9	86	A7	153	DM5	154	DQS5
19	Vss	20	Vss	87	VDD	88	VDD	155	Vss	156	Vss
21	DQ8	22	DQ12	89	A8	90	A6	157	DQ42	158	DQ46
23	DQ9	24	DQ13	91	A5	92	A4	159	DQ43	160	DQ47
25	Vss	26	Vss	93	VDD	94	VDD	161	Vss	162	Vss
27	/DQS1	28	DM1	95	A3	96	A2	163	DQ48	164	DQ52
29	DQS1	30	/Reset	97	A1	98	A0	165	DQ49	166	DQ53
31	Vss	32	Vss	99	VDD	100	VDD	167	Vss	168	Vss
33	DQ10	34	DQ14	101	CK0	102	CK1	169	/DQS6	170	DM6
35	DQ11	36	DQ15	103	/CK0	104	/CK1	171	DQS6	172	Vss
37	Vss	38	Vss	105	VDD	106	VDD	173	Vss	174	DQ54
39	DQ16	40	DQ20	107	A10, /AP	108	BA1	175	DQ50	176	DQ55
41	DQ17	42	DQ21	109	BA0	110	/RAS	177	DQ51	178	Vss
43	Vss	44	Vss	111	VDD	112	VDD	179	Vss	180	DQ60
45	/DQS2	46	DM2	113	/WE	114	/S0	181	DQ56	182	DQ61
47	DQS2	48	Vss	115	/CAS	116	ODT0	183	DQ57	184	Vss
49	Vss	50	DQ22	117	VDD	118	VDD	185	Vss	186	/DQS7
51	DQ18	52	DQ23	119	A13 ***	120	ODT1	187	DM7	188	DQS7
53	DQ19	54	Vss	121	/S1	122	NC *	189	Vss	190	Vss
55	Vss	56	DQ28	123	VDD	124	VDD	191	DQ58	192	DQ62
57	DQ24	58	DQ29	125	TEST/NC	126	VREFCA	193	DQ59	194	DQ63
59	DQ25	60	Vss	127	Vss	128	Vss	195	Vss	196	Vss
61	Vss	62	/DQS3	129	DQ32	130	DQ36	197	SA0	198	/EVENT
63	DM3	64	DQS3	131	DQ33	132	DQ37	199	VDDSPD	200	SDA
65	Vss	66	Vss	133	Vss	134	Vss	201	SA1	202	SCL
67	DQ26	68	DQ30	135	/DQS4	136	DM4	203	Vtt	204	Vtt

* NC = No Connect
** TEST (PIN# 125) reserve for bus probing, is NC on normal modules.
*** Pin might conneceted to NC ball od DRAMs (depanding on density); alternatively may connect to termination resistor

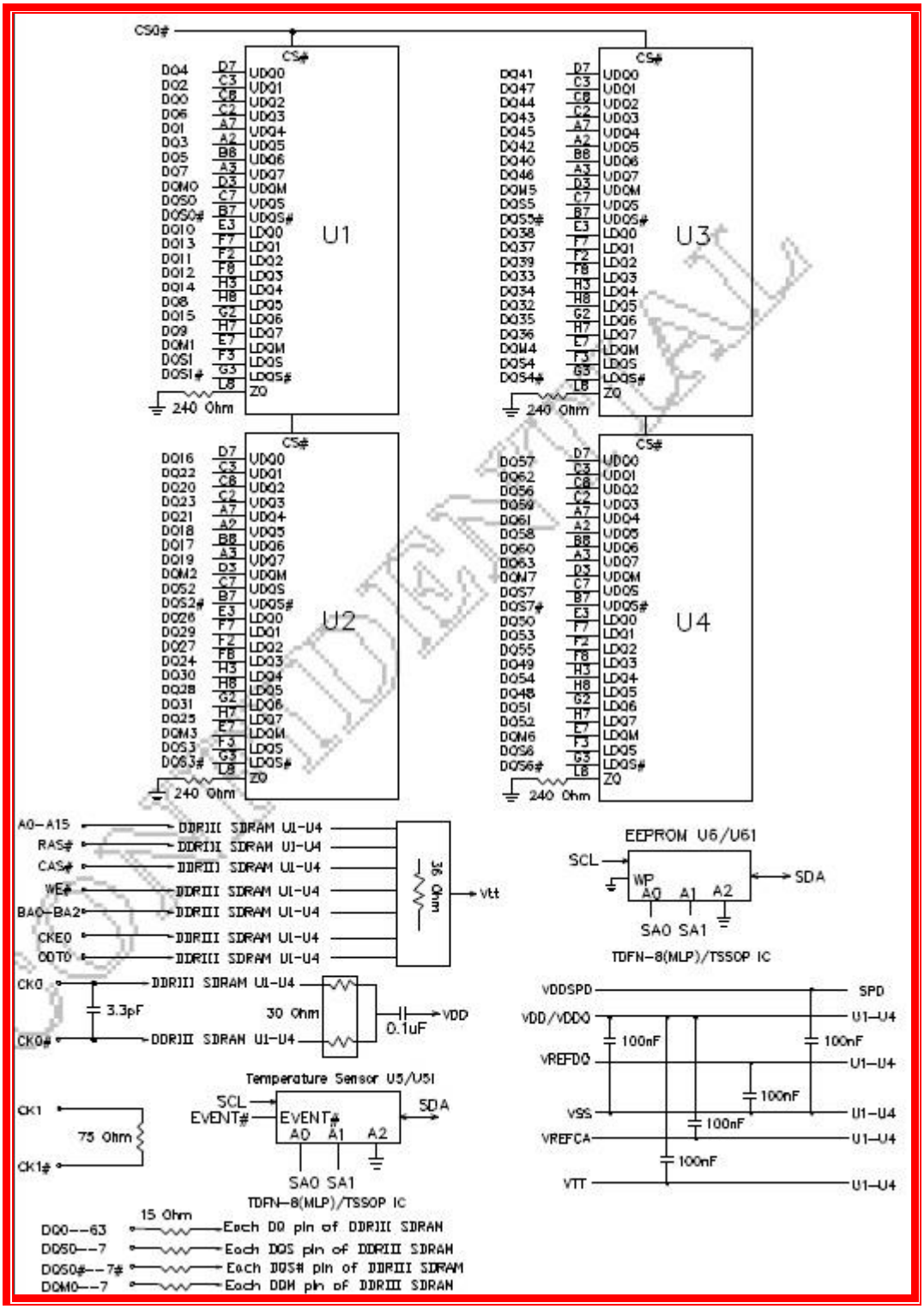
6. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
/RAS	SDRAM row address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
/CAS	SDRAM column address strobe	V_{DD}	Power Supply
/WE	SDRAM write enable	V_{DDID}	V_{DD} Identification Flag
/S0 - /S1	DIMM Rank Select Lines	V_{DDQ}	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	V_{REFDQ}	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	V_{REFCA}	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	V_{SS}	Ground
DQS0 – DQS8 /DQS0-/DQS8	SDRAM data strobes	V_{DDSPD}	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	/Reset	Reset enable
CK0 – CK1 /CK0 - /CK1	Differential SDRAM Clocks	/Event	Reserved for optional temperature-sensing hardware
RSVD	Reserved for future use.	V_{TT}	SDRAM I/O termination supply.

7. Function Block Diagram:

- (2GB, 1 Rank, 256Mx16 DDR3L SDRAMs)



8. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	-40 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.4 to +1.80	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.4 to +1.80	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.4 to +1.80	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.
For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under
all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 ℃ case temperature. Full specifications are supported in this range, but the following additional
conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.
4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

9. DRAM AC & DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
Recommended DC Operating Conditions - DDR3L (1.35V) operation						
V_{DD}	Supply Voltage	1.283	1.35	1.45	V	1,2
VDDSPD	Supply Voltage	3	3.3	3.6	V	
V_{DDQ}	Supply Voltage	1.283	1.35	1.45	V	1,2
Recommended DC Operating Conditions - DDR3 (1.5V) operation						
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
VDDSPD	Supply Voltage	3	3.3	3.6	V	
V_{DDQ}	Supply Voltage	1.425	1.5	1.575	V	1,2
Single Ended AC/DC Input Levels						
$V_{IH\ (DC)}$ DDR3L	DC Input High (Logic1) Voltage	VREF + 90	-	V_{DD}	V	3
$V_{IH\ (DC)}$ DDR3	DC Input High (Logic1) Voltage	VREF + 100		V_{DD}	V	3
$V_{IL\ (DC)}$ DDR3L	DC Input Low (Logic 0) Voltage	V_{SS}	-	V_{REF} - 90	V	3
$V_{IL\ (DC)}$ DDR3	DC Input Low (Logic 0) Voltage	V_{SS}		V_{REF} - 100	V	3
$V_{IH\ (AC)}$ DDR3L	AC Input High (Logic1) Voltage	V_{REF}+ 135	-	-	V	3
$V_{IH\ (AC)}$ DDR3	AC Input High (Logic1) Voltage	V_{REF}+ 150			V	3
$V_{IL\ (AC)}$ DDR3L	AC Input Low (Logic 0) Voltage	-	-	V_{REF} - 135	V	3
$V_{IL\ (AC)}$ DDR3	AC Input Low (Logic 0) Voltage			V_{REF} - 150	V	3
$V_{REFDQ\ (DC)}$	Reference Voltage for DQ, DM inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
$V_{REFCA\ (DC)}$	Reference Voltage for ADD,CMD inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
Single Ended AC/DC Output Levels						
$V_{OH\ (DC)}$	DC output high measurement level (for IV curve linearity)	-	0.8 x VDDQ	-	V	
$V_{OM\ (DC)}$	DC output mid measurement level (for IV curve linearity)	-	0.5 x VDDQ	-	V	
$V_{OL\ (DC)}$	DC output low measurement level (for IV curve linearity)	-	0.2 x VDDQ	-	V	

$V_{OH\ (AC)}$	AC output high measurement level (for output SR)	-	VTT + 0.1 x VDDQ	-	V	6
$V_{OL\ (AC)}$	AC output low measurement level (for output SR)		VTT - 0.1 x VDDQ	-	V	6

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Differential AC/DC Input Levels						
$V_{IHdiff\ DDR3L}$	Differential Input high	+0.18	-	Note 9	V	7
$V_{IHdiff\ DDR3}$	Differential Input high	+0.2		Note 9	V	7
$V_{ILdiff\ DDR3L}$	Differential Input logic Low	Note 9	-	-0.18	V	7
$V_{ILdiff\ DDR3}$	Differential Input logic Low	Note 9	-	-0.2	V	7
$V_{IHdiff(ac)\ DDR3L}$	Differential Input high ac	2* ($V_{IH\ (AC)}$- V_{REF})	-	Note 9	V	8
$V_{IHdiff(ac)\ DDR3}$	Differential Input high ac	2* ($V_{IH\ (AC)}$- V_{REF})	-	Note 9	V	8
$V_{ILdiff(ac)\ DDR3L}$	Differential Input logic Low ac	Note 9	-	2* (V_{REF}- $V_{IL\ (AC)}$)	V	8
$V_{ILdiff(ac)\ DDR3}$	Differential Input logic Low ac	Note 9	-	2* (V_{REF}- $V_{IL\ (AC)}$)	V	8
Differential AC and DC Output Levels						
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	-	+ 0.2 x VDDQ	-	V	10
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	-	- 0.2 x VDDQ	-	V	10

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
4. Recommended DC Operating Conditions - DDR3 (1.5V) operation : The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV); Recommended DC Operating Conditions - DDR3L (1.35V) operation: The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 13.5 mV)
5. For reference: approx. VDD/2.
6. The swing of ± 0.1 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2
7. Used to define a differential signal slew-rate.
8. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
9. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot.
10. The swing of ± 0.2 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

10. Operating, Standby, and Refresh Currents

- 2GB SODIMM (1 Rank, 256Mx16 DDR3L SDRAMs)

Symbol	Parameter/Condition		PC3-14900	Unit
I DD0	One bank; Active - Precharge		152	mA
I DD1	One bank; Active - Read - Precharge		220	mA
I DD2N	Precharge Standby Current		72	mA
IDD2NT	Precharge Standby ODT Current		88	mA
I DD2P	Precharge Power Down Current	Fast Mode	52	mA
	Precharge Power Down Current	Slow Mode	52	mA
I DD2Q	Pecharge Quiet Standby Current		72	mA
I DD3N	Active Standby Current		120	mA
I DD3P	Active Power-Down Current		76	mA
I DD4R	Operating Current Burst Read		480	mA
I DD4W	Operating Current Burst Write		440	mA
I DD5B	Burst Refresh Current		840	mA
I DD6	Self-Refresh Current: Normal Temperature Range		56	mA
I DD7	Operating Bank Interleave Read Current		780	mA
I DD8	RESET Low Current		52	mA

11. Timing Parameters

Symbol	Parameter	PC3-14900		Unit
		Min.	Max.	
Clock Timing				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.071	<1.25	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-60	60	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-50	50	Ps
JIT (CC)	Cycle to Cycle Period Jitter	120		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	100		Ps
TJIT (duty)		-	-	Ps
TERR (2per)	Cumulative error across 2 cycle	-88	88	Ps
TERR (3per)	Cumulative error across 3 cycle	-105	105	Ps
TERR (4per)	Cumulative error across 4 cycle	-117	117	Ps
TERR (5per)	Cumulative error across 5 cycle	-126	126	Ps
TERR (6per)	Cumulative error across 6 cycle	-133	133	Ps
TERR (7per)	Cumulative error across 7 cycle	-139	139	Ps
TERR (8per)	Cumulative error across 3 cycle	-145	145	Ps
TERR (9per)	Cumulative error across 4 cycle	-150	150	Ps
TERR (10per)	Cumulative error across 5 cycle	-154	154	Ps

TERR (11per)	Cumulative error across 6 cycle	-158	158	Ps
TERR (12per)	Cumulative error across 7 cycle	-161	161	Ps
TERR (nper)	Cumulative error across 13~50 cycle	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		Ps
Data Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDQSQ	DQS, DQS# to DQ skew, per group, per access	-	85	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-390	195	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	195	Ps
tDS(base) AC135	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	68	-	Ps
tDH(base) DC 100	Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	-	-	Ps
Data Strobe Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tRPRE	DQS,DQS# differential READ Preamble	0.9		tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)
tQSH	DQS, DQS# differential output high time	0.4		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.4		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)
tDQSCK	DQS, DQS# rising edge output access time from rising CK, CK#	-195	195	Ps

tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-390	195	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	195	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.27	0.27	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.18	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.18	-	tCK(avg)
Command and Address Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to Internal read command	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			
tRC	Refer to Section 1 Feature			
tCCD		4	-	nCK

tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup(tRP / tCK(avg))		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	34	9 tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4nCK, 5ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4nCK, 6ns)	-	
tFAW	Four activate window for 1KB page size	27	-	ns
tFAW	Four activate window for 2KB page size	35	-	ns
tIS (base) AC135	Command and Address setup time to CK, CK#, referenced to Vih(ac) / Vil(ac) levels.	65		ns
tIH(base) DC100	Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	100		ps
tIS(base) AC125	Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	150		ps
Calibration Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tZQinit	Power-up and RESET calibration time	Max. (512nCK, 640ns)	-	nCK
tZQoper	Normal operation Full calibration time	Max. (256nCK, 320ns)	-	nCK
tZQCS	Normal operation Short calibration time	Max. (64nCK, 80ns)	-	nCK
Reset Timing				

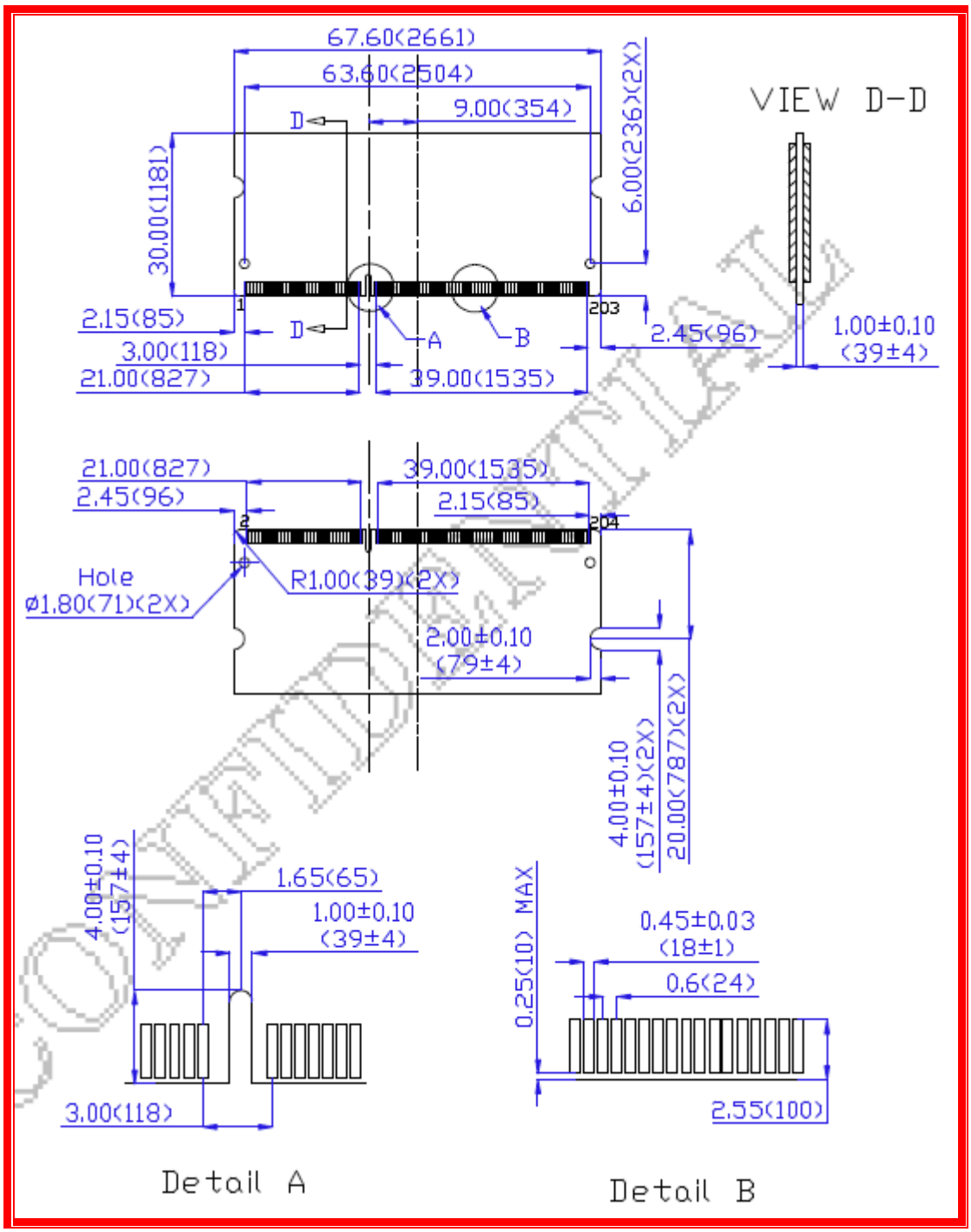
Symbol	Parameter	Min.	Max.	Unit
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK,tRFC(min) +10ns)	-	
Self Refresh Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXS	Exit Self Refresh to commands not requiring a locked DLL	Max(5nCK), tRFC(min) +10ns)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE9min) +1nCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5nCK,10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5nCK,10ns)	-	
Power Down Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24ns)	-	
tCKE	CKE minimum pulse width	max(3nCK,5ns)	-	
tCPDED	Command pass disable delay	2	-	nCK

tPD	Power Down Entry to Exit Timing	tCK(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	nCK
ODT Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK
tAONPD	Asynchronous RTT turn-on delay (Powe-Down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns

tAON	RTT-turn-on	-195	195	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	tCK(avg)
Write Leveling Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	nCK
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	-	nCK
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	140	-	ps
tWLH	Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	140	-	ps
tWLO	Write leveling output delay	0	7.5	ns
tWLOE	Write leveling output error	0	2	ns

12. PACKAGE DIMENSION

- (2GB, 1 Rank, 256Mx16 DDR3L base SODIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

13. RoHS Declaration

innodisk

宜鼎國際股份有限公司

Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書 (RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
鉛 (Pb)	< 1000 ppm
汞 (Hg)	< 1000 ppm
鎘 (Cd)	< 100 ppm
六價鉻 (Cr 6+)	< 1000 ppm
多溴聯苯 (PBBs)	< 1000 ppm
多溴二苯醚 (PBDEs)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2016 / 08 / 04

Rev 1.0

October 2016

Revision Log

Rev	Date	Modification
0.1	11st October 2016	Preliminary Edition
1.0	11st October 2016	Official released.