Approval Sheet

Customer	
Product Number	**M3S0-4GSSC4N9**
Module speed	**PC3-10600**
Pin	**204 pin**
Cl-tRCD-tRP	**9-9-9**
SDRAM Operating Temp	**-40℃~85℃**
Date	**16th February 2016**

Approval by Customer

P/N:

Signature:

Date:

Sales:

Sr. Technical Manager: John Hsieh

Rev 1.0

The Total Solution For
Industrial Flash Storage

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)
		CL=7	CL=9	CL=11			
PC3-10600	**N**	1066	1333	1333	13.5	13.5	13.5

- JEDEC Standard 204-pin Dual In-Line Memory Module
- Intend for PC3-10600 applications
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.35 Volt (1.28V~1.45V) & 1.5V (1.425V~1.575V)
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8µs (Tc ≤ +85°C)
- 16/10/1 Addressing (row/column/rank)-4GB
- SDRAM operating temperature range -40°C ≤ Tc ≤ +85°C
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 9
  - Burst Length: switch on-the-fly: BL=8 or BC 4
- RoHS Compliant *(Section 12)*

2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	-40 to +85	°C	1
TSTG	Storage Temperature	-50 to +100	°C	
HOPR	Operating Humidity (relative)	10 to 90	%	
HSTG	Storage Humidity (without condensation)	5 to 95	%	
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2
1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification. 2. Up to 9850 ft.				

3. DRAM Parameters by device density

RTT_Nom Setting	Parameter		4Gb	Units
tRFC	REF command ACT or REF command time		260	ns
tREFI	Average periodic refresh interval	0°C≦**TCASE≦85**°C	7.8	μs
		85°C≦**TCASE≦95**°C	3.9	μs

4. Ordering Information

DDR3L W/T Sorting SODIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M3S0-4GSSC4N9	4GB	PC3-10600	512Mx64	8	1	N

5. Pin Configurations (Front side/Back side)

X64 SODIMM

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREFDQ	2	Vss	69	DQ27	70	DQ31	137	DQS4	138	Vss
3	Vss	4	DQ4	71	Vss	72	Vss	139	Vss	140	DQ38
5	DQ0	6	DQ5	73	CKE0	74	CKE1	141	DQ34	142	DQ39
7	DQ1	8	Vss	75	VDD	76	VDD	143	DQ35	144	Vss
9	Vss	10	/DQS0	77	NC	78	A15 ***	145	Vss	146	DQ44
11	DM0	12	DQS0	79	BA2	80	A14 ***	147	DQ40	148	DQ45
13	Vss	14	Vss	81	VDD	82	VDD	149	DQ41	150	Vss
15	DQ2	16	DQ6	83	A12, /BC	84	A11	151	Vss	152	/DQS5
17	DQ3	18	DQ7	85	A9	86	A7	153	DM5	154	DQS5
19	Vss	20	Vss	87	VDD	88	VDD	155	Vss	156	Vss
21	DQ8	22	DQ12	89	A8	90	A6	157	DQ42	158	DQ46
23	DQ9	24	DQ13	91	A5	92	A4	159	DQ43	160	DQ47
25	Vss	26	Vss	93	VDD	94	VDD	161	Vss	162	Vss
27	/DQS1	28	DM1	95	A3	96	A2	163	DQ48	164	DQ52
29	DQS1	30	/Reset	97	A1	98	A0	165	DQ49	166	DQ53
31	Vss	32	Vss	99	VDD	100	VDD	167	Vss	168	Vss
33	DQ10	34	DQ14	101	CK0	102	CK1	169	/DQS6	170	DM6
35	DQ11	36	DQ15	103	/CK0	104	/CK1	171	DQS6	172	Vss
37	Vss	38	Vss	105	VDD	106	VDD	173	Vss	174	DQ54
39	DQ16	40	DQ20	107	A10, /AP	108	BA1	175	DQ50	176	DQ55
41	DQ17	42	DQ21	109	BA0	110	/RAS	177	DQ51	178	Vss
43	Vss	44	Vss	111	VDD	112	VDD	179	Vss	180	DQ60
45	/DQS2	46	DM2	113	/WE	114	/S0	181	DQ56	182	DQ61
47	DQS2	48	Vss	115	/CAS	116	ODT0	183	DQ57	184	Vss
49	Vss	50	DQ22	117	VDD	118	VDD	185	Vss	186	/DQS7
51	DQ18	52	DQ23	119	A13 ***	120	ODT1	187	DM7	188	DQS7
53	DQ19	54	Vss	121	/S1	122	NC *	189	Vss	190	Vss
55	Vss	56	DQ28	123	VDD	124	VDD	191	DQ58	192	DQ62
57	DQ24	58	DQ29	125	TEST/NC	126	VREFCA	193	DQ59	194	DQ63
59	DQ25	60	Vss	127	Vss	128	Vss	195	Vss	196	Vss
61	Vss	62	/DQS3	129	DQ32	130	DQ36	197	SA0	198	/EVENT
63	DM3	64	DQS3	131	DQ33	132	DQ37	199	VDDSPD	200	SDA
65	Vss	66	Vss	133	Vss	134	Vss	201	SA1	202	SCL
67	DQ26	68	DQ30	135	/DQS4	136	DM4	203	Vtt	204	Vtt

* NC = No Connect

** TEST (PIN# 125) reserve for bus probing, is NC on normal modules.

*** Pin might conneceted to NC ball od DRAMs (depanding on density); alternatively may connect to termination resistor

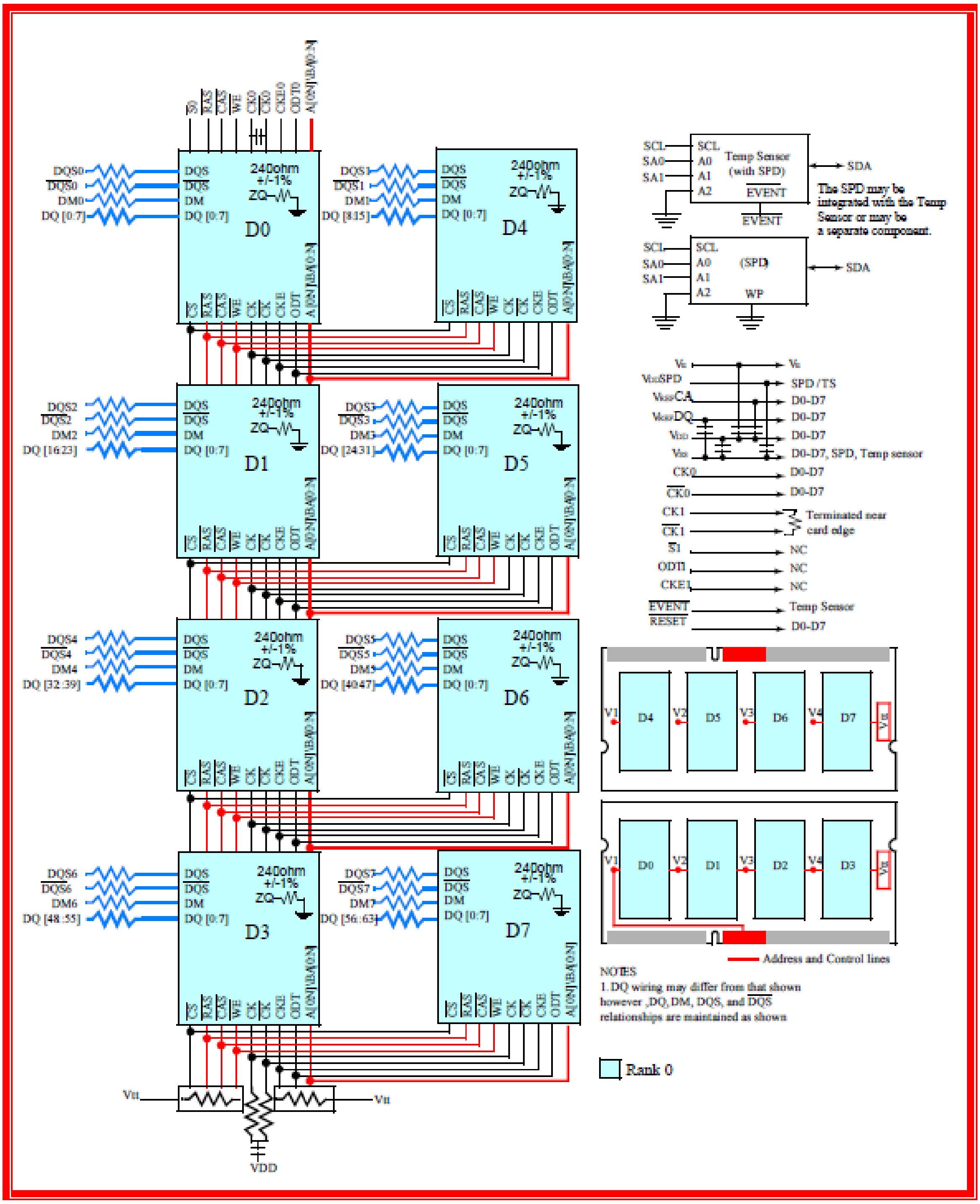
6. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
/RAS	SDRAM row address strobe	SA0 – SA1	Serial Presence Detect Address Inputs
/CAS	SDRAM column address strobe	VDD	Power Supply
/WE	SDRAM write enable	VDDID	VDD Identification Flag
/S0 - /S1	DIMM Rank Select Lines	VDDQ	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	VREFDQ	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	VREFCA	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	VSS	Ground
DQS0 – DQS8 /DQS0-/DQS8	SDRAM data strobes	VDDSPD	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	/Reset	Reset enable
CK0 – CK1 /CK0 - /CK1	Differential SDRAM Clocks	Event#	Reserved for optional temperature-sensing hardware
RSVD	Reserved for future use.	VTT	SDRAM I/O termination supply.

7. Function Block Diagram:

- (4GB, 1 Rank, 512Mx8 DDR3L SDRAMs)



The SPD may be integrated with the Temp Sensor or may be a separate component.

NOTES
1. DQ wiring may differ from that shown however ,DQ, DM, DQS, and DQS relationships are maintained as shown

8. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	-40 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.4 to +1.975	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.4 to +1.975	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.4 to +1.975	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.

For measurement conditions, please refer to the JEDEC document JESD51-2.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.

3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 ℃ case temperature. Full specifications are supported in this range, but the following additional conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

9. DRAM AC & DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
VDD	Supply Voltage	1.283	1.35	1.45	V	1,2
VDDQ	Supply Voltage	1.283	1.35	1.45	V	1,2
Single Ended AC/DC Input Levels						
VIH (DC)	DC Input High (Logic1) Voltage	VREF + 0.1	-	VDD	V	3
VIL (DC)	DC Input Low (Logic 0) Voltage	VSS	-	VREF - 0.1	V	3
VIH (AC)	AC Input High (Logic1) Voltage	VREF+ 0.175	-	-	V	3
VIL (AC)	AC Input Low (Logic 0) Voltage	-	-	VREF - 0.175	V	3
VREFDQ (DC)	Reference Voltage for DQ, DM inputs	0.49VDDQ	0.5VDDQ	0.51VDDQ	V	4,5
VREFCA (DC)	Reference Voltage for ADD,CMD inputs	0.49VDDQ	0.5VDDQ	0.51VDDQ	V	4,5
Single Ended AC/DC output Levels						
VOH (DC)	DC output high measurement level (for IV curve linearity)	-	0.8 x VDDQ	-	V	
VOM (DC)	DC output mid measurement level (for IV curve linearity)	-	0.5 x VDDQ	-	V	
VOL (DC)	DC output low measurement level (for IV curve linearity)	-	0.2 x VDDQ	-	V	
VOH (AC)	AC output high measurement level (for output SR)	-	VTT + 0.1 x VDDQ	-	V	6
VOL (AC)	AC output low measurement level (for output SR)		VTT - 0.1 x VDDQ	-	V	6

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Differential AC/DC Input Levels						
VIHdiff	Differential Input high	+0.2	-	Note 9	V	7
VILdiff	Differential Input logic Low	Note 9	-	-0.2	V	7
VIHdiff(ac)	Differential Input high ac	2* **(VIH (AC)-VREF)**	-	Note 9	V	8
VILdiff(ac)	Differential Input logic Low ac	Note 9	-	2* **(VREF-VIL (AC))**	V	8
Differential AC and DC Output Levels						
VOHdiff(AC)	AC differential output high measurement level (for output SR)	-	+ 0.2 x VDDQ	-	V	10
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-	- 0.2 x VDDQ	-	V	10

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
4. The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
5. For reference: approx. VDD/2 +/- 15 mV.
6. The swing of ± 0.1 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT = VDDQ/2
7. Used to define a differential signal slew-rate.
8. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
9. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot.
10. The swing of ± 0.2 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT = VDDQ/2 at each of the differential outputs.

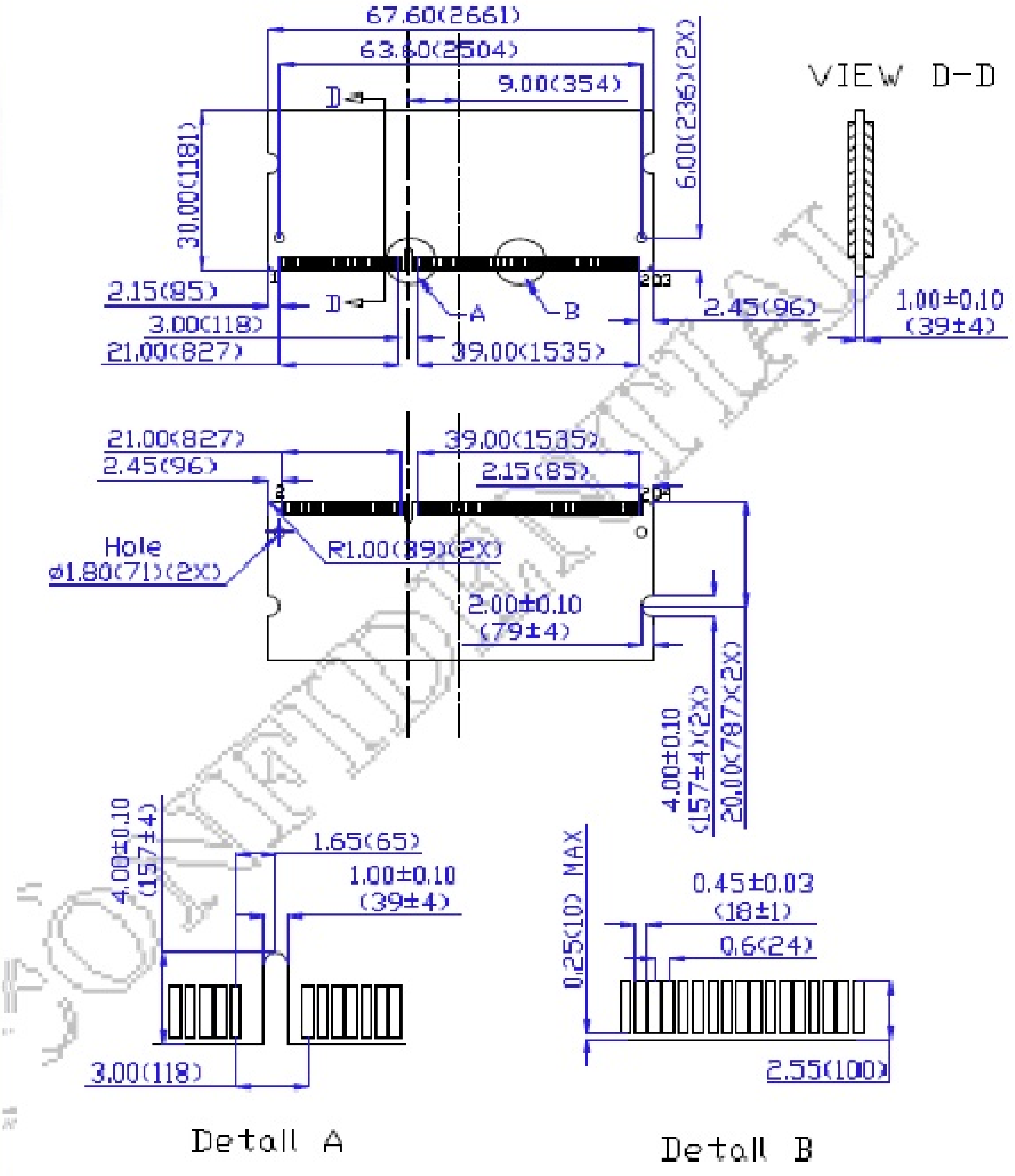
10. Operating, Standby, and Refresh Currents

- 4GB SODIMM (1 Rank, 512Mx8 DDR3L SDRAMs T_{CASE} = 0 °C ~ 70 °C)

Symbol	Parameter/Condition		PC3-10600	Unit
I DD0	One bank; Active - Precharge		232	mA
I DD1	One bank; Active - Read - Precharge		320	mA
I DD2N	Precharge Standby Current		104	mA
I DD2NT	Precharge Standby ODT Current		120	mA
I DD2P	Precharge Power Down Current	Fast Mode	88	mA
	Precharge Power Down Current	Slow Mode	88	mA
I DD2Q	Pecharge Quiet Standby Current		96	mA
I DD3N	Active Standby Current		184	mA
I DD3P	Active Power-Down Current		88	mA
I DD4R	Operating Current Burst Read		568	mA
I DD4W	Operating Current Burst Write		568	mA
I DD5B	Burst Refresh Current		1600	mA
I DD6	Self-Refresh Current: Normal Temperature Range		120	mA
I DD7	Operating Bank Interleave Read Current		1040	mA
I DD8	RESET Low Current		120	mA

11. PACKAGE DIMENSION

- (4GB, 1 Rank, 512Mx8 DDR3L base SODIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

12. RoHS Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟2011/65/EU 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	**Limited of RoHS ppm（mg/kg）**
Cd	＜ 100 ppm
Pb	＜ 1000 ppm
Hg	＜ 1000 ppm
Chromium VI（Cr+6）	＜ 1000 ppm
Polybromodiphenyl ether（PBDE）	＜ 1000 ppm
Polybrominated Biphenyls（PBB）	＜ 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Richard Lee 李鐘亮

Company Representative Title 公司代表人職稱： CEO 執行長

Date 日期： 2014 / 07 / 29

(Company Stamp/公司大小章)

Rev 1.0

Revision Log

Rev	Date	Modification
0.1	16th February 2016	Preliminary Edition
1.0	16th February 2016	Official released.