OFP-151-PC
OFP-2100-PC
OFP-2101-PC
Open Frame Panel PC

User's Manual

Version 1.0
(January 2021)

iBASE

Compliance

CE

This product may cause radio interference in which case users may be required to take adequate measures.

FC

This product has been tested and found to comply with the limits for a Class B device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with manufacturer's instructions, may cause harmful interference to radio communications.

Operation is subject to the following two conditions:

- This product may not cause harmful interference
- This product must accept any interference received including interference that may cause undesired operation.

However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception which can be determined by turning the equipment off and on, you may correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
- Consult the distributor or an experienced radio/TV technician for help.

WEEE

This product must not be disposed of as normal household waste, in accordance with the EU directive of for waste electrical and electronic equipment (WEEE - 2012/19/EU). Instead, it should be disposed of by returning it to a municipal recycling collection point. Check local regulations for disposal of electronic products.

iBASE

Green IBASE

This product complies with the current RoHS restrictions that prohibit the use of the following substances in concentrations exceeding 0.1% by weight (1000 ppm) except for cadmium, limited to 0.01% by weight (100 ppm).

- Lead (Pb)
- Mercury (Hg)
- Cadmium (Cd)
- Hexavalent chromium (Cr6+)
- Polybrominated biphenyls (PBB)
- Polybrominated diphenyl ether (PBDE)

Important Safety Information

Carefully read the precautions before using the device.

Environmental conditions:

- Put the device horizontally on a stable and solid surface during installation in case the device may fall, causing serious damage.
- Leave plenty of space around the device for ventilation.
- Use this product in environments with ambient temperatures between 0˚C and 40˚C.
- DO NOT LEAVE THIS DEVICE IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY BE BELOW -20° C OR ABOVE 60° C. To prevent from damages, the device must be used in a controlled environment.
- Keep the device away from humidity to avoid fog or condensation from accumulating on the inner surface of the panel.

Care for your IBASE products:

- Before cleaning the device, turn it off and unplug all cables in case a small amount of electrical current may still flow.
- Use neutral cleaning agents or diluted alcohol to clean the device chassis with a cloth. Then wipe the chassis with a dry cloth.
- Use a computer vacuum cleaner to remove dust to prevent the air vent or slots from getting clogged.

WARNING

Attention during use:

- Do not use this product near water.
- Do not spill water or any other liquids on your device.
- Do not place heavy objects on the top of the device.
- Operate this device from the type of power indicated on the marking label. If you are not sure of the type of power available, consult your distributor or local power company.
- Ensure to use the correct power supply voltage.
- Do not walk on the power cord or allow anything to rest on it.
- If you use an extension cord, make sure that the total ampere rating of the product plugged into the extension cord does not exceed its limits.

Avoid Disassembly

Disassembly, modification, or any attempt at repair could generate hazards and cause damage to the device, even bodily injury or property damage, and will void any warranty on the product.

CAUTION

Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Warranty Policy

- **IBASE standard products:**

  24-month (2-year) warranty from the date of shipment. If the date of shipment cannot be ascertained, the product serial numbers can be used to determine the approximate shipping date.

- **3rd-party parts:**

  12-month (1-year) warranty from delivery for the 3rd-party parts that are not manufactured by IBASE, such as CPU, CPU cooler, memory, storage devices, power adapter, panel and touch screen.

* Products, however, that fail due to misuse, accident, improper installation or unauthorized repair shall be treated as out of warranty and customers shall be billed for repair and shipping charges.

iBASE

Technical Support & Services

1. Visit the IBASE website at www.ibase.com.tw to find the latest information about the product.
2. If you need any assistance from your distributor or sales representative concerning problems that you may have encountered, please prepare the following information:

   - Product model name
   - Product serial number
   - Detailed description of the problem
   - Error messages in text or in screenshots if there is any
   - The arrangement of the peripherals
   - Software used (such as OS and application software, including the version numbers)

3. For repair service, please download the RMA form from http://www.ibase.com.tw/english/Supports/RMAService/.
   Fill out the form and contact your distributor or sales representative.

Table of Contents

Chapter 1
General Information

The information provided in this chapter includes:

- Features
- Packing List
- Specifications
- Dimensions

1.1 Introduction to OFP Series

The OFP-151-PC, IPC-2100-PC and IPC-2101-PC are open-frame fanless panel PCs that come with optional colored frame, flat bezel design and easily accessible storage space. They are upgradeable and ideal for industrial automation and factory automation applications. These devices are powered by Intel® Pentium® QC N4200 (OFP-151-PC / OFP-2100-PC); and Intel® Core i7 7600U, Intel® Core i5 7300U and Intel® Core i3 7100U processors (OFP-2101-PC).

(Photo of OFP-151-PC)

1.2 Features

- Fanless, modular flat bezel open frame design
- Easily accessible storage space
- IP65-rated front bezel, 4GB DDR memory, 64GB (default)
- 4x USB 3.0, 2x GbE
- Supports Windows 10, 64-bit; Linux Kernel 4+
- Optional colored frame and power adaptor

1.3 Packing List

Your product package should include the items listed below. If any of the items below is missing, contact the distributor or the dealer from whom you have purchased the product.

- OFP-151-PC / OFP-2100-PC / OFP-2101-PC x 1

1.4 Specifications

Product Name	OFP-151-PC	OFP-2100-PC	OFP-2101-PC
Display & Touch Screen			
Display Size	15” TFT-LCD	21” TFT-LCD	
Max. Resolution	1024 x 768	1920 x 1080	
Luminance (cd/m^2)	420	250	
Contrast	1:600	1:1000	
Max. Color	16.2M	16.7M	
View Angle (H°/V°)	160/160	178/178	
Backlight Lifetime (hrs)	30,000		
Touch Type	Projected Capacitive		
Touch Interface	USB		
Light Transmission (%)	89		
Point of Touch	10		
I/O Interface			
USB 3.0	4		
USB 2.0	0		
RS-232/422/485 (BIOS Selectable)	1 (RJ50)		1 (DSUB9)
RS-232	Optional		
LAN	2x GbE		
Additional Graphics	1x HDMI, 1x DP		
Audio	None		
Digital I/O	Optional		
Power Connector	1x 3-pin terminal block		
Power Button	1x 2-pin terminal block for remote		
Mechanical			
Dimensions (mm)	375.2 x 289.6 x 60.9	543 x 334 x 88.2	
Net Weight (kg)	5	7.6	7.7

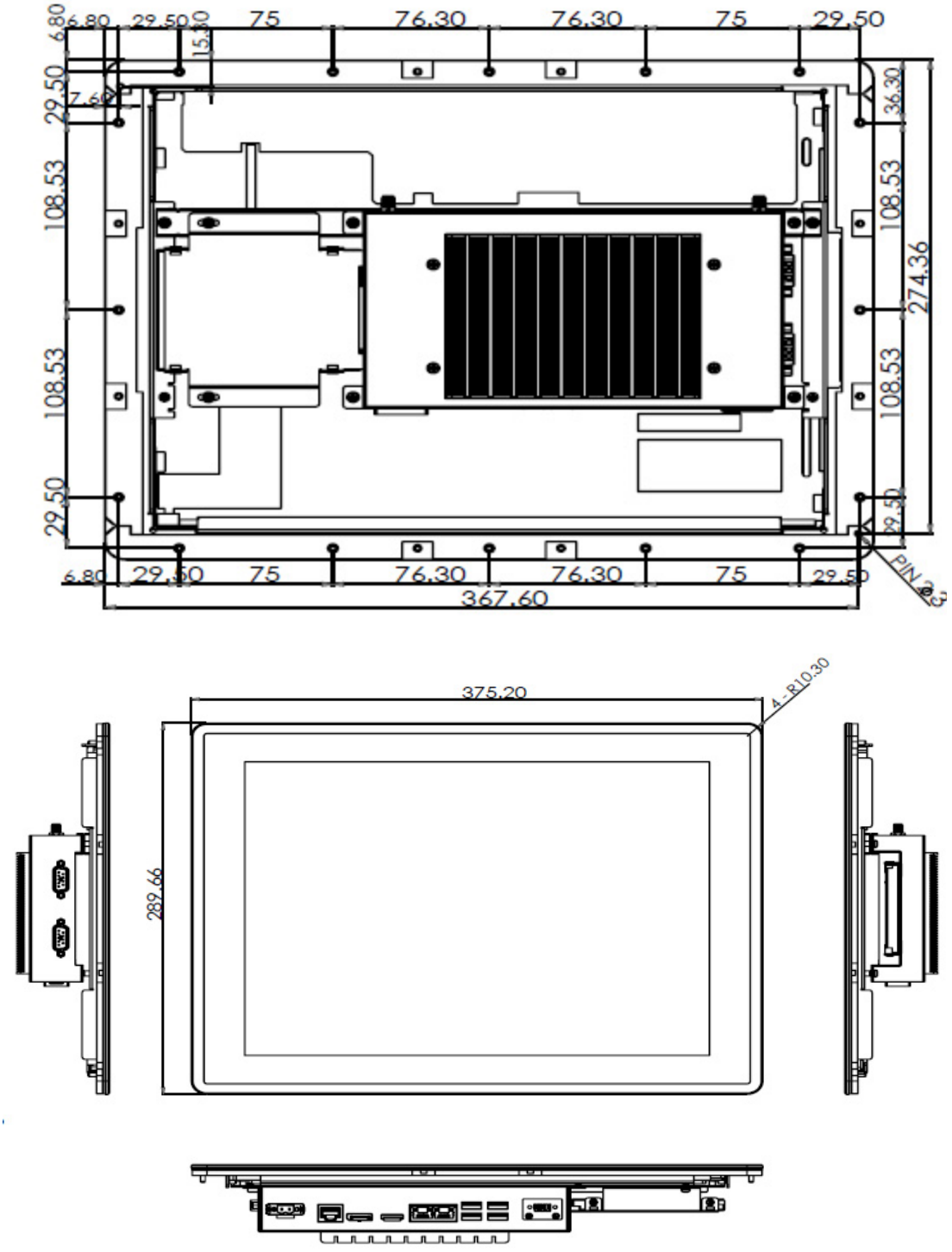
System			
Product Name	**OFP-151-PC**	**OFP-2100-PC**	**OFP-2101-PC**
Processor	Intel® Pentium® QC N4200	Intel I® Pentium® QC N4200	Intel® Core i7 7600U Intel® Core i5 7300U Intel® Core i3 7100U
Memory	Max. 8GB, default 4GB	Max. 8GB, default 4GB	Max. 32GB, default 4GB
Thermal Design	Fanless		
Membrane Control	N/A		
Built-in Speaker/Mic	N/A		
Expansion			
Internal Expansion Bus	1x mPCIe half size mSATA; 1x M.2 B-key	1x mPCIe half size mSATA; 1x M.2 B-key	1x mPCIe full f size mSATA; 1x M.2 B-key
Expansion Slot	None		
Wireless	Optional		
Storage Space			
HDD	1 x 2.5” SATA HDD, default 64G SSD		
Removable	N/A		
Power			
Power Input Range	9V~36V DC		9V~24V DC
Construction			
Chassis Material	SGCC		
Color (Front /Back)	Raw SGCC		
IP Rating	Front side with IP65		
Mounting	Open frame design		
Environment			
Operating Temperature	0°C ~ 50°C		
Storage Temperature	-20 ~ 70 °C		
Storage Humidity	10 ~ 90% (non-condensing) at 40 °C		
Certification	CE, FCC Class B		
Supported O.S.	Windows 10, 64-bit; Linux Kernel 4+		

All specifications are subject to change without prior notice.

1.5 Dimensions

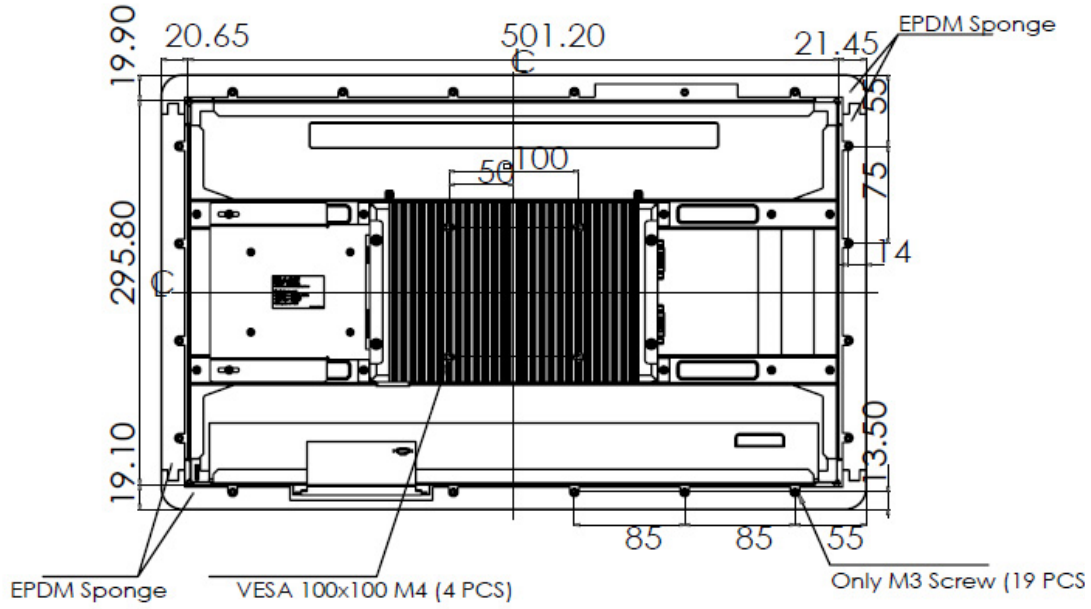
Unit: mm
Dimensions: 375.2 x 289.6 x 60.9

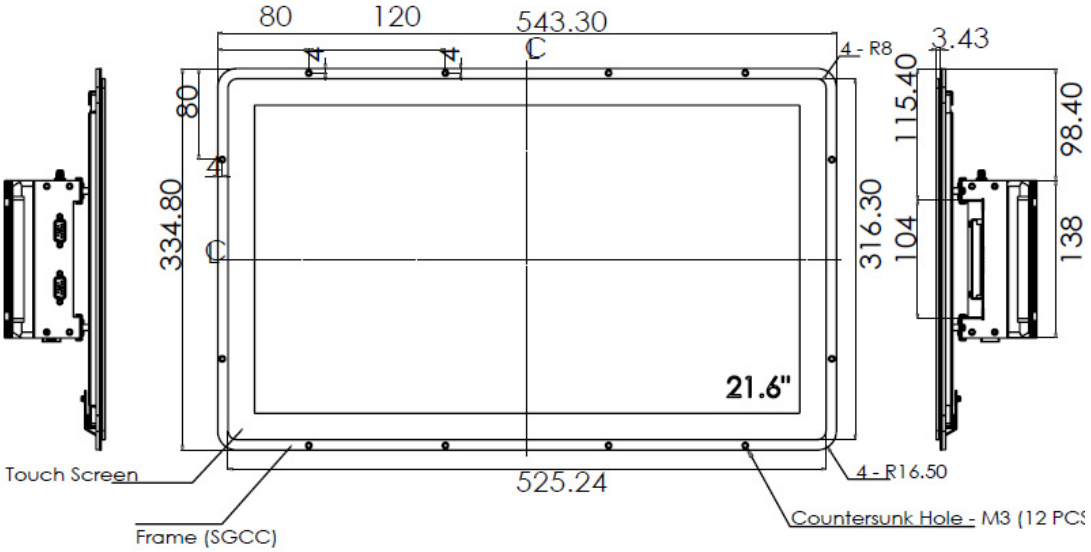
OFP-151-PC

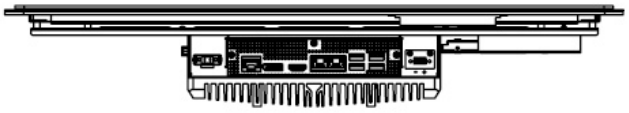


OFP-2100-PC

Unit: mm
Dimensions: 543 x 334 x 88.2

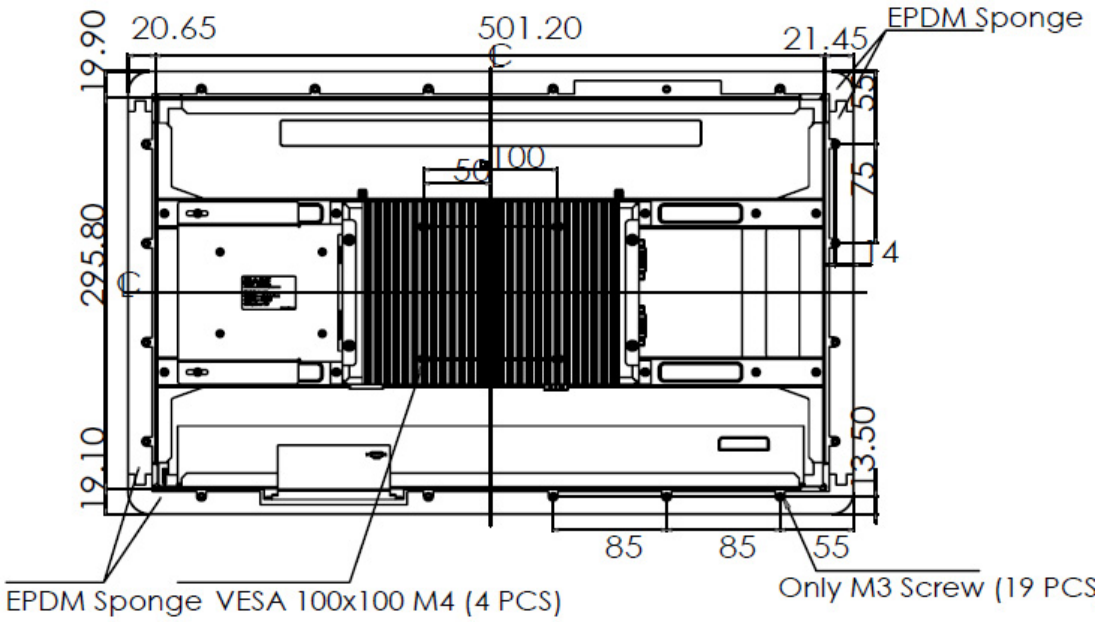


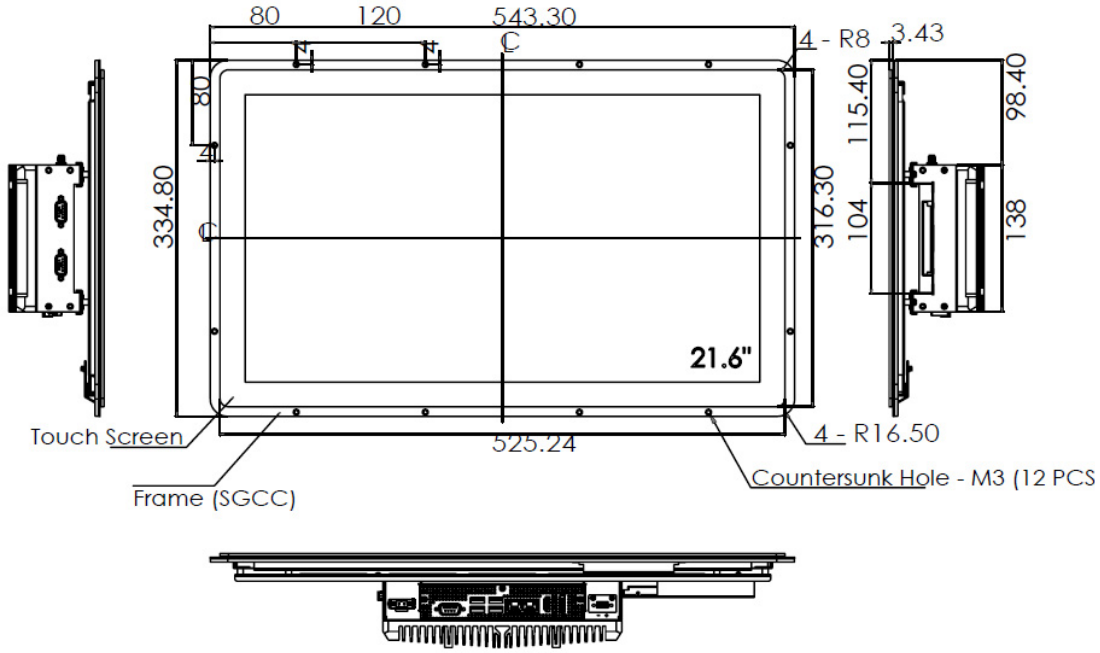




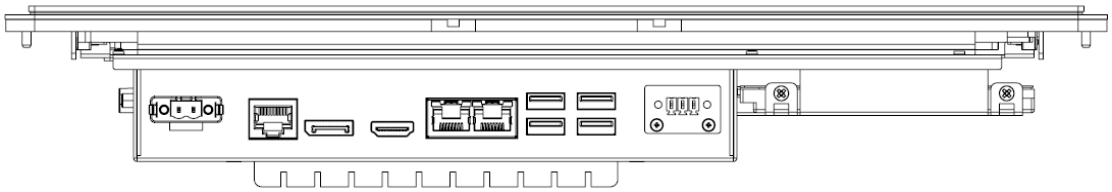
OFP-2101-PC

Unit: mm
Dimensions: 543 x 334 x 88.2

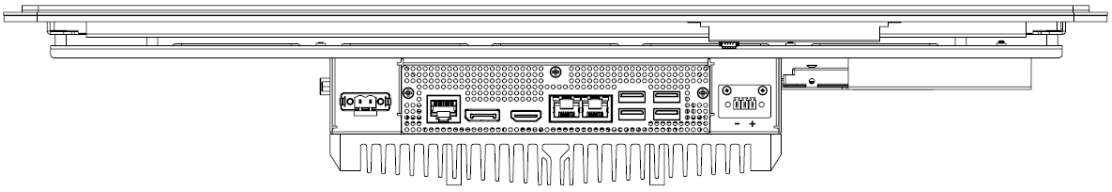




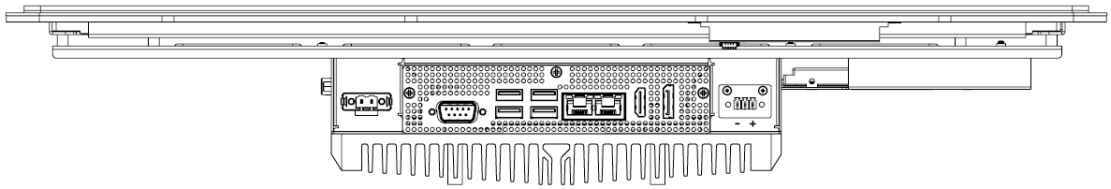
1.6 I/O Side View of the OFP Series



OFP-151-PC



OFP-2100-PC

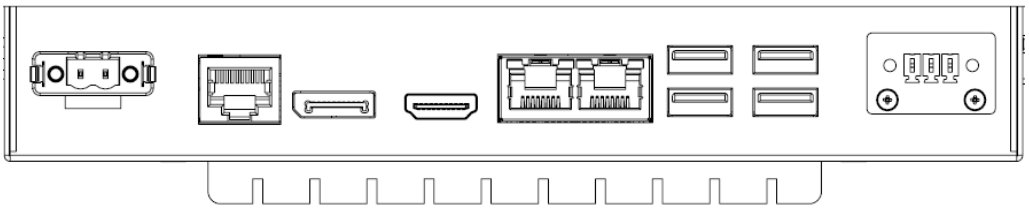


OFP-2101-PC

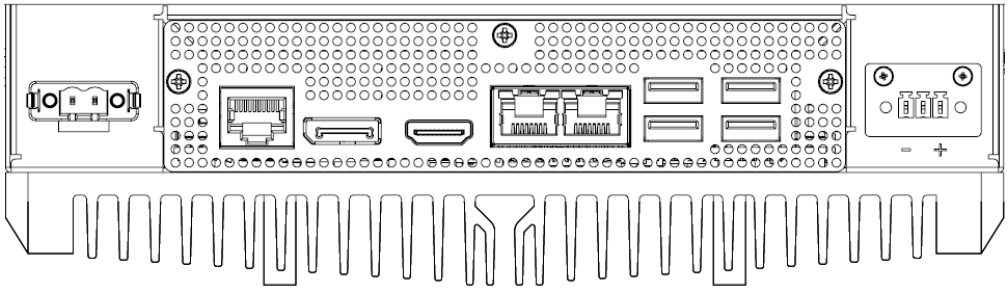
NOTE:
As shown in the above pictures, both the OFP-151-PC and OFP-2100-PC open frame panel PCs have the same I/O connectors in conjunction with the 3-pin terminal block for power input and a 2-pin terminal block for power button located on the same side. Both models use the IB811F-420 embedded board.

On the other hand, the OFP-2101-PC open frame panel PC uses the IB917 embedded board.

Both the OFP-2100-PC and OFP-2101-PC are using the same heat sink and SATA drive installation method.

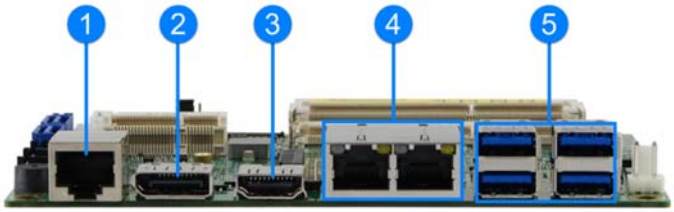


I/O View OFP-151-PC

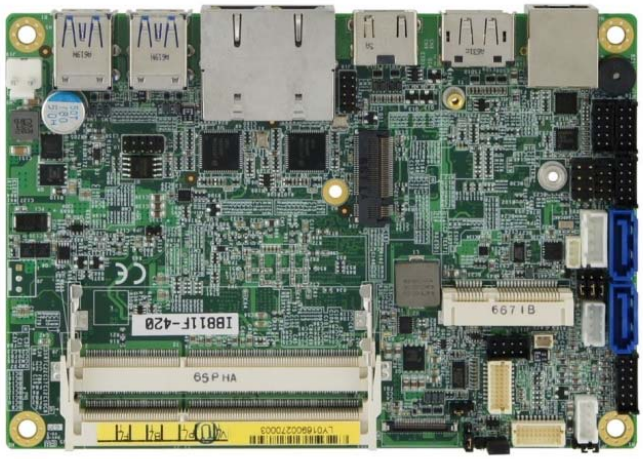


I/O View of OFP-2100-PC

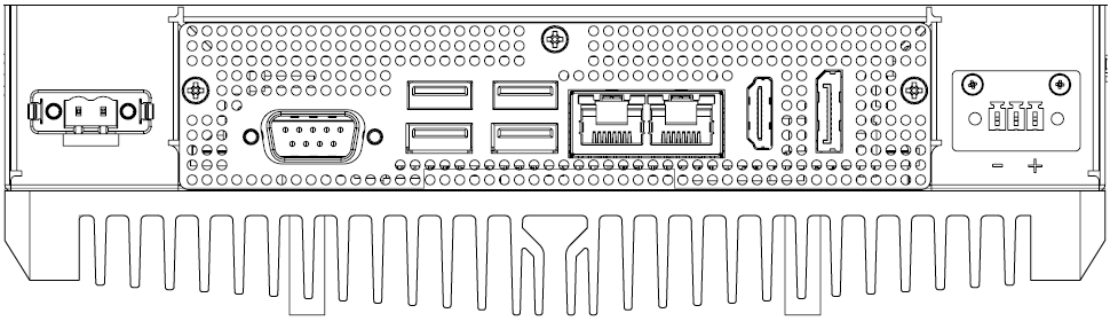
Below shows the edge connectors on the IB811F-420 board that is used by the OFP-151-PC and OFP-2100-PC open frame panel PCs



No.	Name	No.	Name
1	COM1 (RJ50) Port	4	LAN Port
2	DisplayPort	5	USB 3.0 Port
3	HDMI Port		

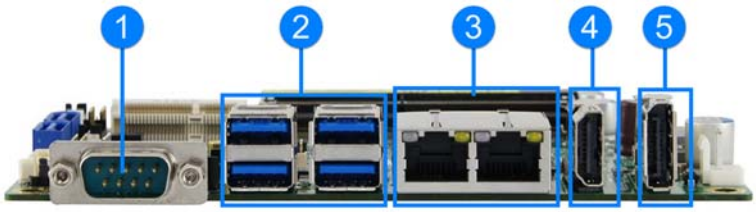


IB811F-420

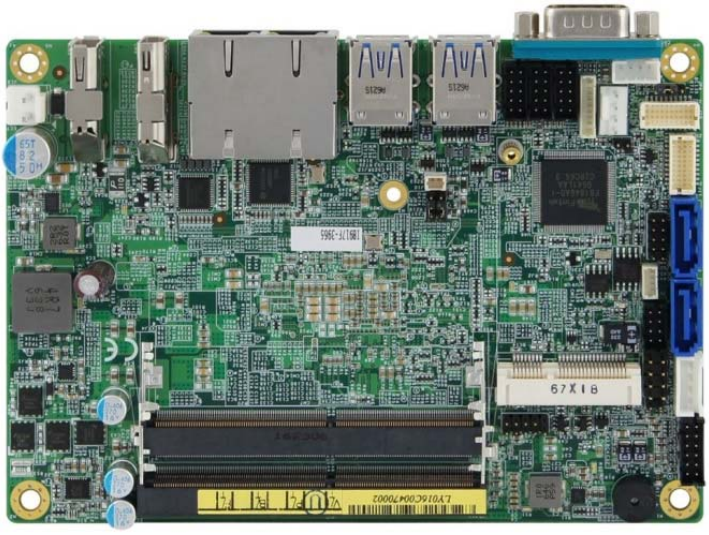


I/O View of OFP-2101-PC

Below shows the edge connectors on the IB917 board that is used by the OFP-2101-PC open frame panel PC



No.	Name	No.	Name
1	COM1 RS-232/422/485	4	HDMI Port
2	USB 3.0 Ports	5	DisplayPort
3	LAN Port		



IB917

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Chapter 2
Hardware Configuration

The information provided in this chapter includes:

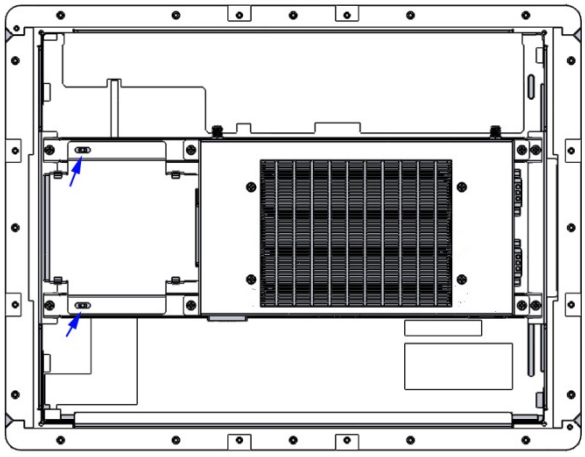
- Installations
- Jumpers and Connectors

2.1 Installations

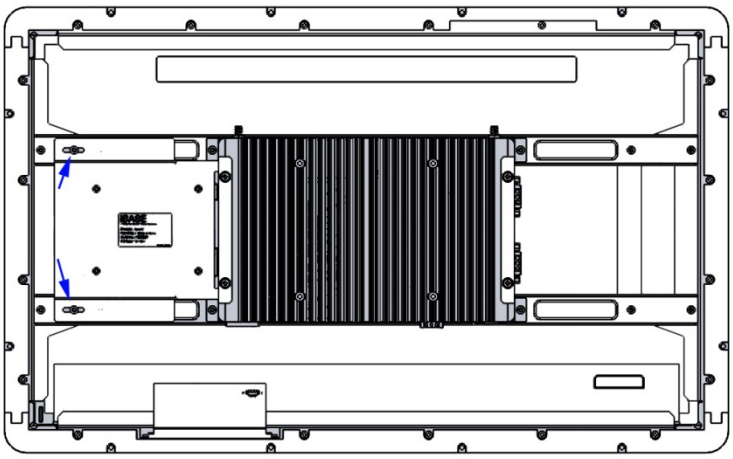
Avoid device disassembly: Disassembly, modification, or any attempt at repair could generate hazards and cause damage to the device, injury, or property damage, and will void any warranty. If you need to make any changes to the device, be sure to unplug the power cord and have qualified engineers or technicians do it.

2.1.1 SSD / HDD Replacement

1. To remove the HDD tray, remove the two screws locking the tray as indicated by the two arrows and push the tray away from the embedded system towards the edge of the panel.

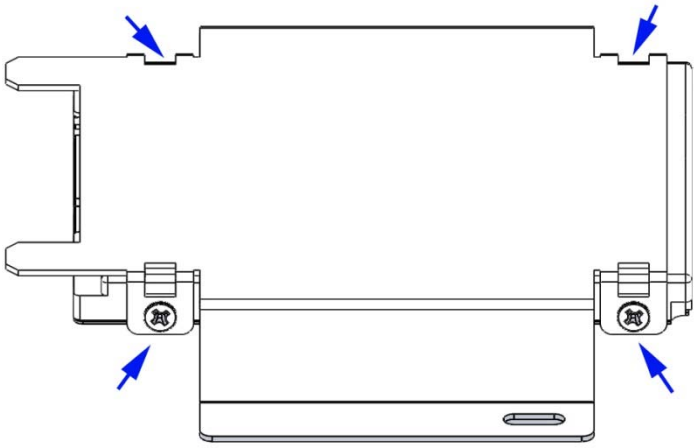


OFP-151-PC

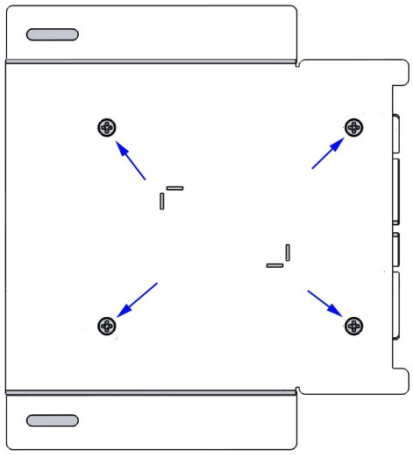


OFP-2101-PC

2. To remove HDD from the HDD tray, remove the 4 screws that are securing the HDD to the tray.



HDD Tray of OFP-151-PC

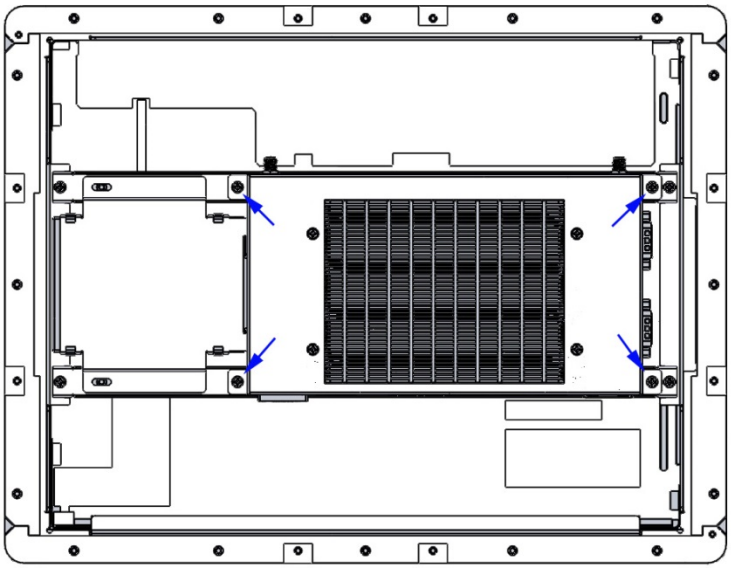


HDD Tray of OFP-2101-PC

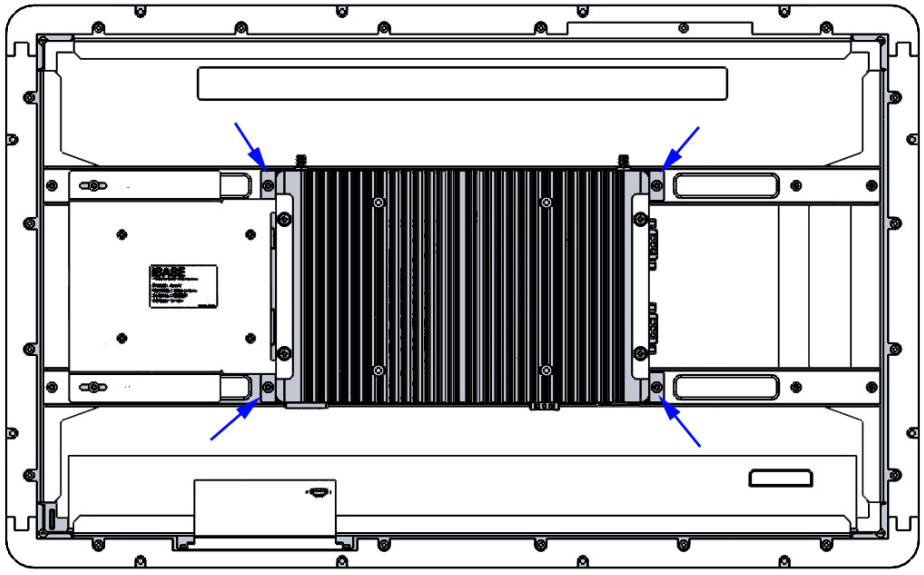
2.1.2 Memory Replacement

To replace or install memory modules, perform the following steps.

3. Remove the 4 screws that are securing the embedded PC to the panel PC, as shown by the arrows below.



OFP-151-PC

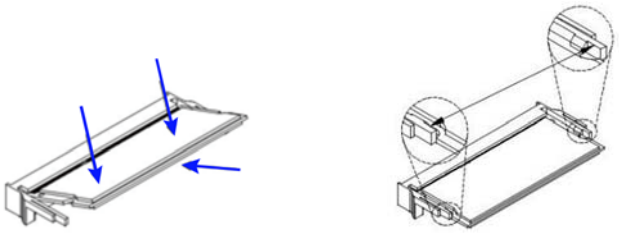


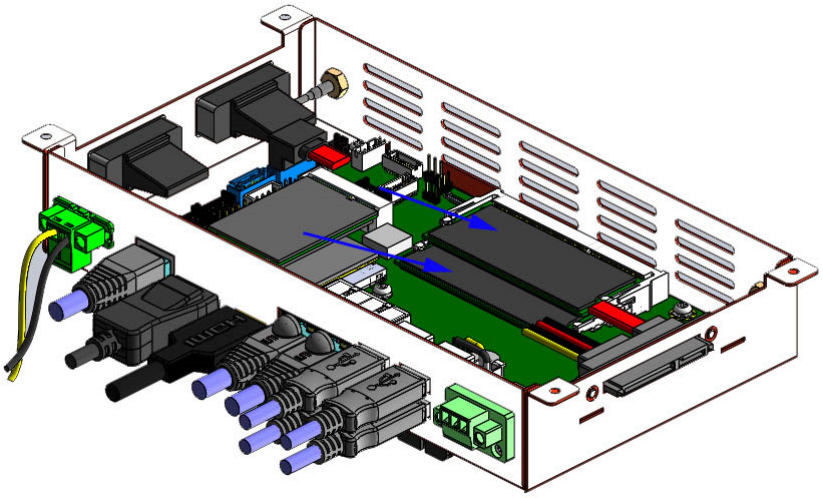
OFP-2101-PC

NOTE:

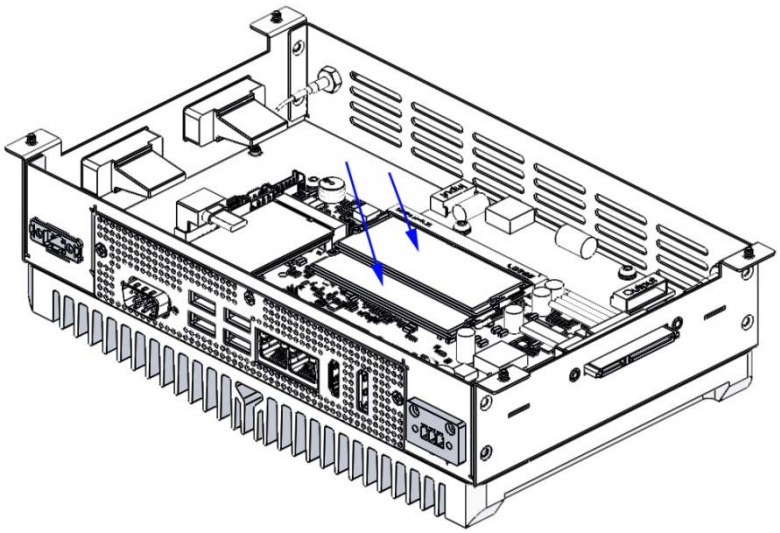
1. The OFP series panel PCs has a default 4GB memory on board. While the OFP-151-PC and OFP-2100-PC support up to 8GB memory, OFP-2101-PC can accommodate up to 32GB.

4. Locate the memory slot and align the key of the memory module with that on the memory slot. Insert the module slantwise and gently push the module straight down until the clips of the slot close to hold the module in place when the module touches the bottom of the slot.
5. Remove the memory modules by using your fingers to press down on the two-side clips that hold each module in place.





OFP-151-PC / OFP-2100-PC

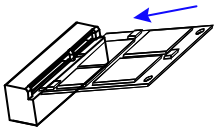


OFP-2101-PC

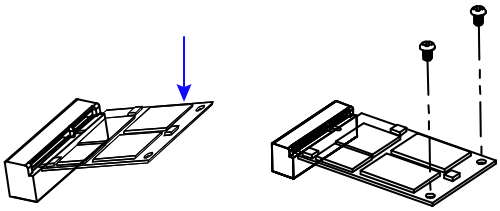
2.1.3 Mini-PCIe Installation

To replace or install a mini-PCIe card, perform the following steps after removing the rear cover.

1. Locate the mini-PCIe slot, align the key of the card to the interface, and insert the card slantwise.



2. Push the card down and fix it with the supplied flat head screw.

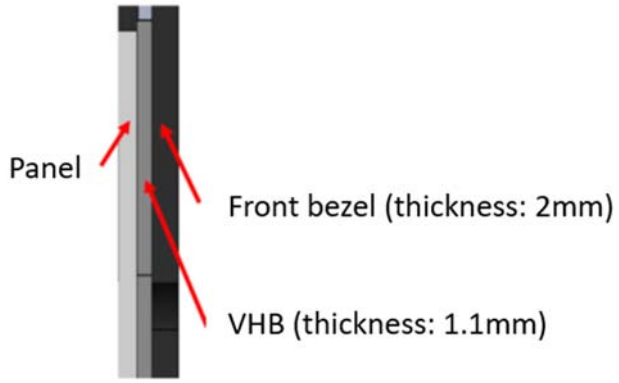


2.1.4 Front bezel design suggestion

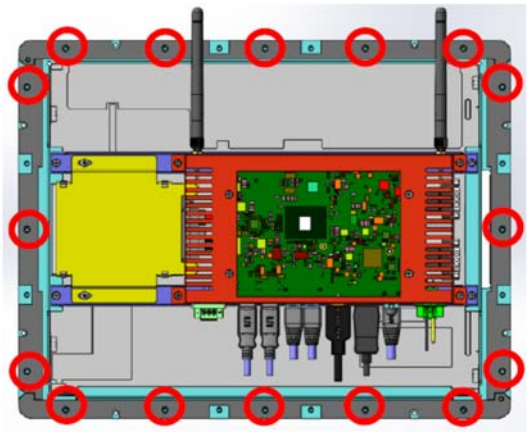
To design or install front bezel, please refer the following two suggestions.

2.1.4.1 One-way fixed design

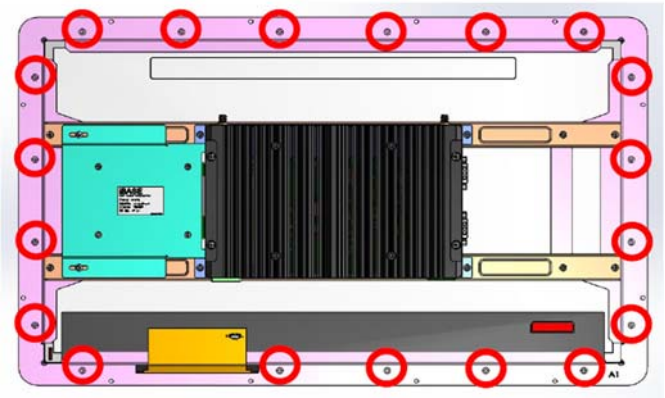
1. The recommended thickness of front bezel and double sided tape is as follows.



2. Fixed OFP system and front bezel from rear side to front side using M3 screws.



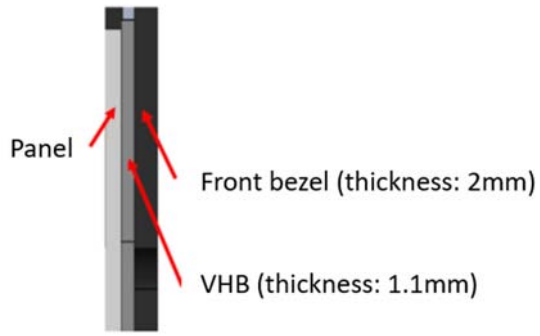
OFP-151-PC (M3 Screw *16PCS)



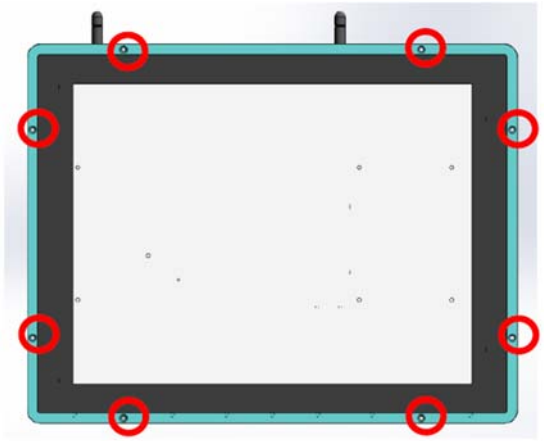
OFP-2100/2101-PC (M3 Screw *19PCS)

2.1.4.2 Two-way fixed design

1. The recommended thickness of front bezel and double sided tape is as follows.



2. Fixed OFP system and front bezel from rear side to front side or front side to rear side using M3 screws.



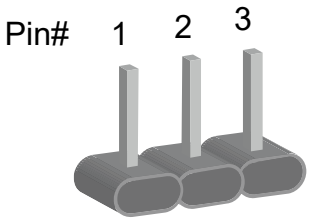
OFP-151-PC (M3 Screw *8PCS)

OFP-2100/2101-PC (M3 Screw *12PCS)

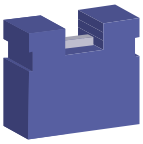
2.2 Setting the Jumpers

Configure the jumpers with the settings required to be able to use the features needed for your application. Contact your supplier if you have doubts about the best configuration for your use.

Jumpers are short-length conductors consisting of several metal pins with a non-conductive base mounted on the circuit board. Jumper caps are used to have the functions and features enabled or disabled. If a jumper has 3 pins, you can connect either PIN1 to PIN2 or PIN2 to PIN3 by shorting with the jumper cap.

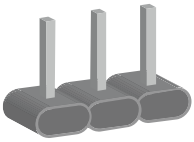
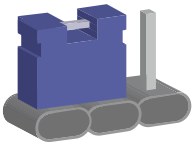
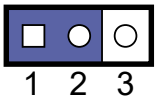
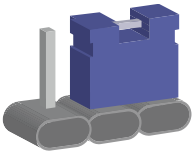
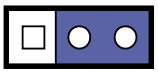


A 3-pin jumper



A jumper cap

Refer to the illustration below to set the jumpers.

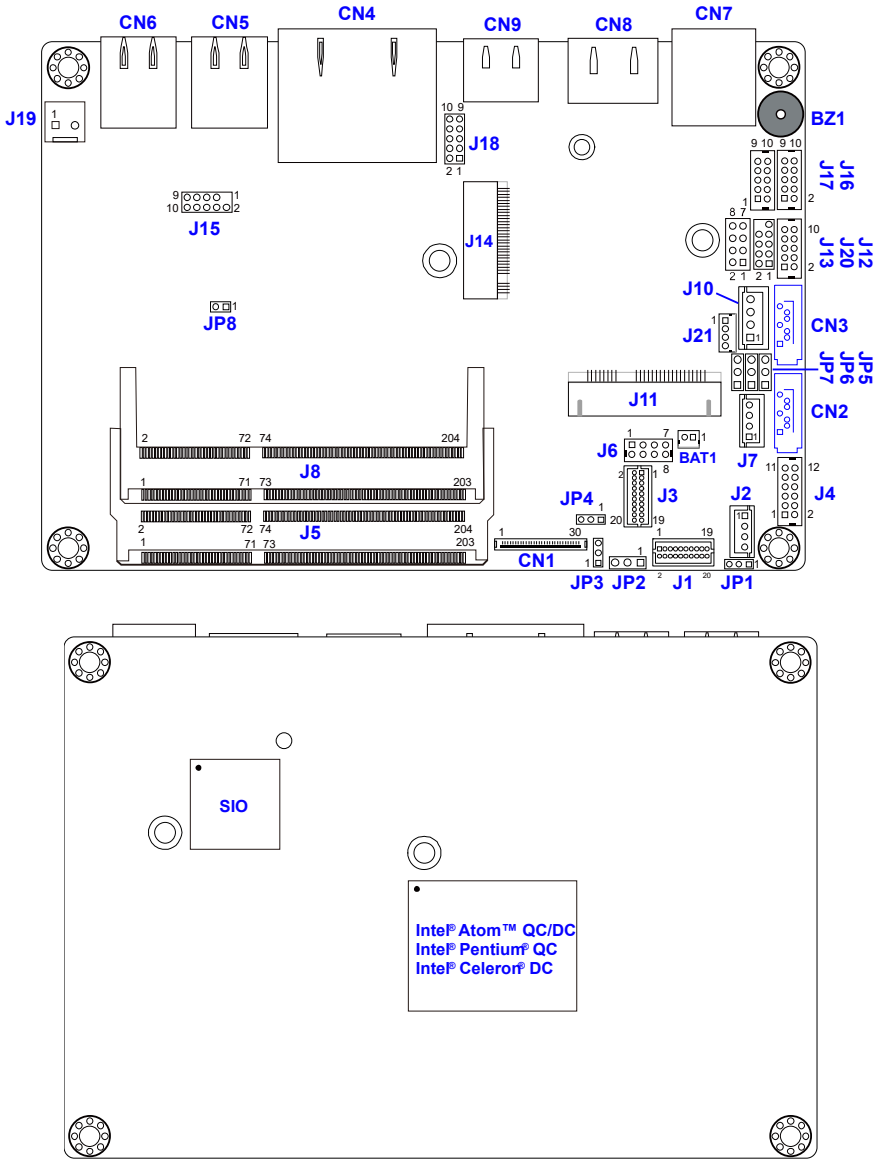
Pin closed	Oblique view	Illustration
Open		
1-2		
2-3		

When two pins of a jumper are encased in a jumper cap, this jumper is **closed**, i.e. turned **On**.

When a jumper cap is removed from two jumper pins, this jumper is **open**, i.e. turned **Off**.

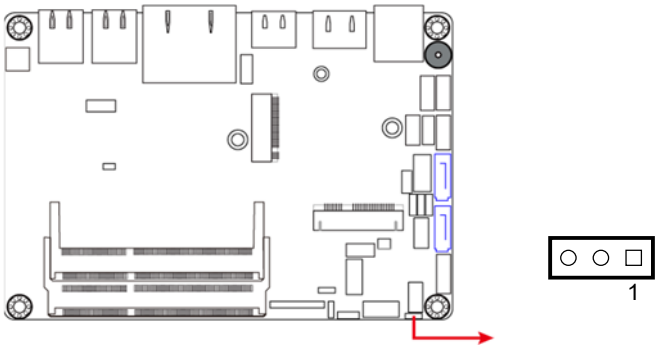
2.3 Jumper & Connector Locations (IB811F)

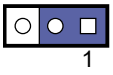
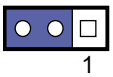
Motherboard: IB811F



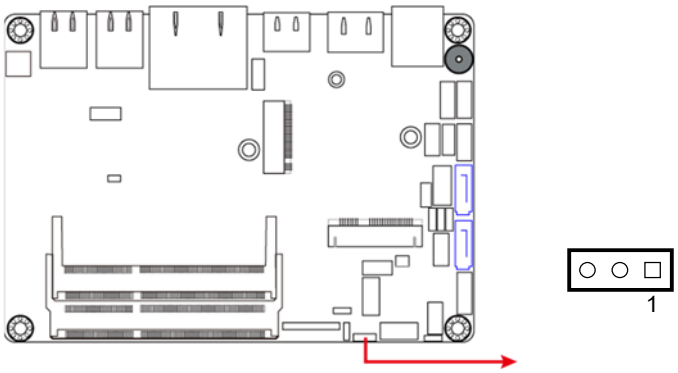
Board diagram of IB811F

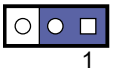
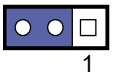
2.3.1 LVDS Panel Brightness Selection (JP1)



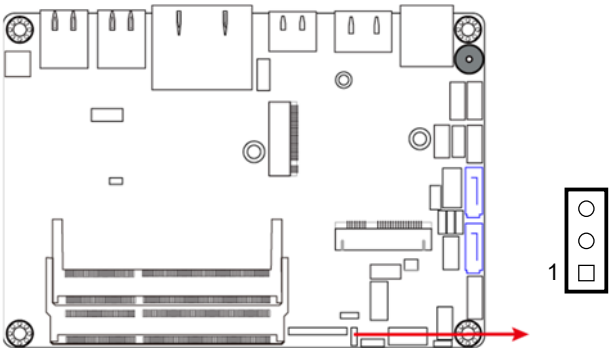
Function	Pin closed	Illustration
3.3V (default)	1-2	
5V	2-3	

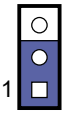
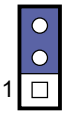
2.3.2 LVDS Panel Power Selection (JP2)



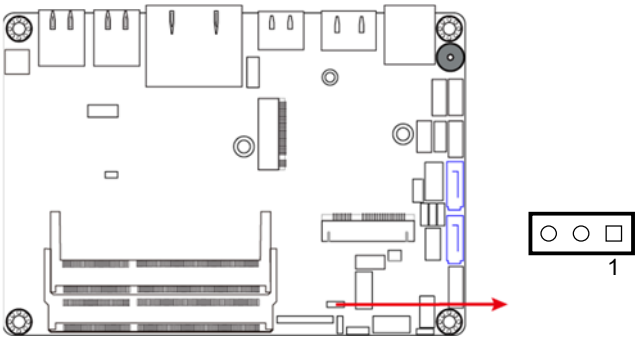
Function	Pin closed	Illustration
3.3V (default)	1-2	
5V	2-3	

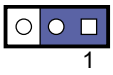
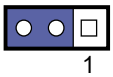
2.3.3 eDP Panel Power Selection (JP3)



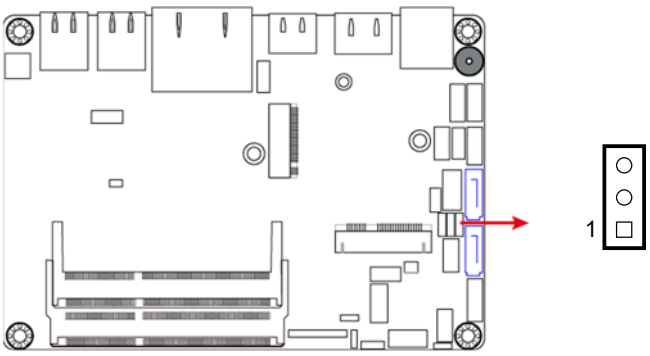
Function	Pin closed	Illustration
3.3V (default)	1-2	
5V	2-3	

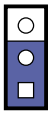
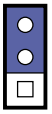
2.3.4 eDP / LVDS Panel Selection (JP4)



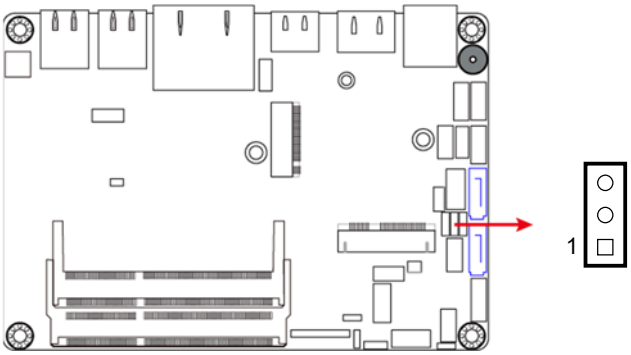
Function	Pin closed	Illustration
eDP	1-2	
LVDS (default)	2-3	

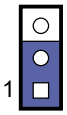
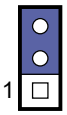
2.3.5 ATX / AT Power Selection (JP5)



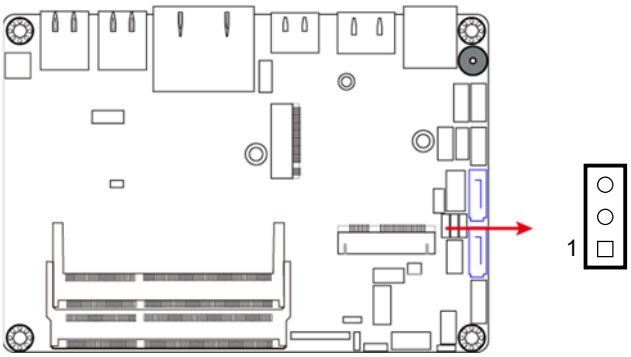
Function	Pin closed	Illustration
ATX (default)	1-2	
AT	2-3	

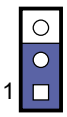
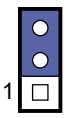
2.3.6 CMOS Data Clearance (JP6)



Function	Pin closed	Illustration
Normal (default)	1-2	
Clear CMOS	2-3	

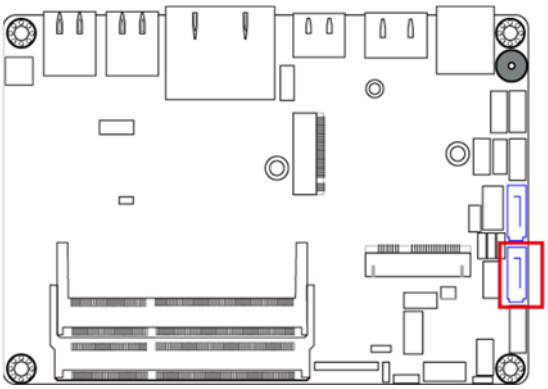
2.3.7 ME Register Clearance (JP7)



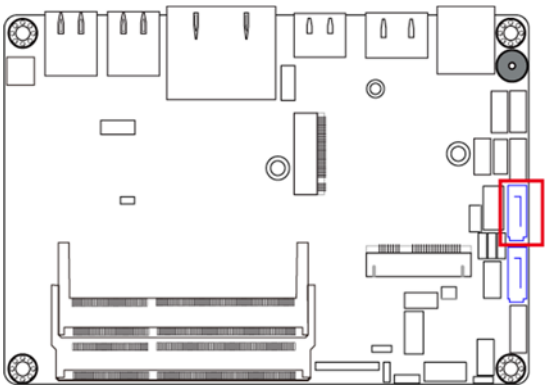
Function	Pin closed	Illustration
Normal (default)	1-2	
Clear ME	2-3	

2.3.8 SATA III Connector (CN2, CN3)

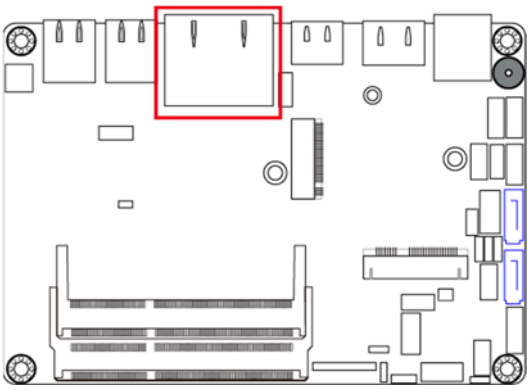
CN2: shared with M.2 B-key



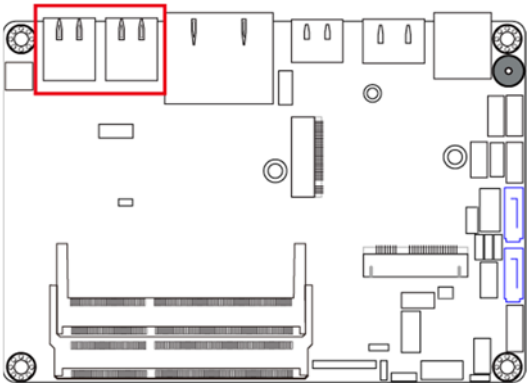
CN3: shared with mSATA



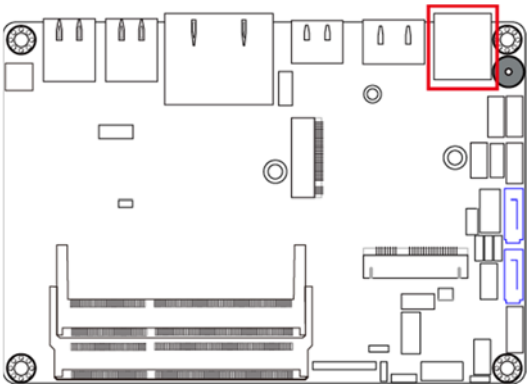
2.3.9 LAN Ports (CN4)



2.3.10 USB 3.0 Ports (CN5, CN6)



2.3.11 Console COM1 (RJ50) RS-232/422/485 Port (CN7)

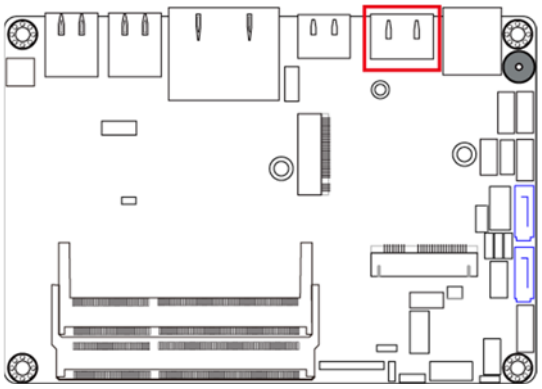


COM1 port is jumper-less and configurable in BIOS.

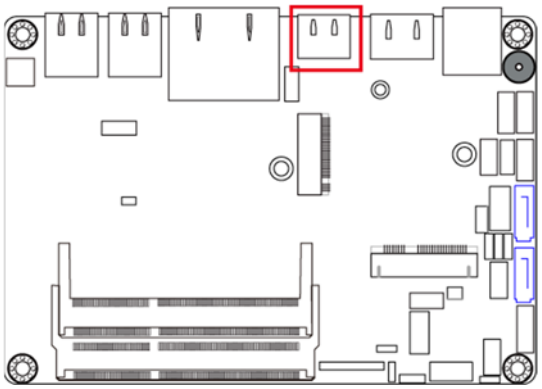
Pin	Assignment	Pin	Assignment
1	DSR, Data set ready	6	DCD, Data carrier detect
2	Ground	7	DTR, Data terminal ready
3	Ground	8	CTS, Clear to send
4	TX, Transmit	9	RTS, Request to send
5	RX, Receive	10	RI, Ring Indicator

Pin	Assignment		
	RS-232	RS-422	RS-485
1	DSR	NC	NC
2	Ground	Ground	Ground
3	Ground	Ground	Ground
4	TX	RX+	NC
5	RX	TX+	Data+
6	DCD	TX-	Data-
7	DTR	RX-	NC
8	CTS	NC	NC
9	RTS	NC	NC
10	RI	NC	NC

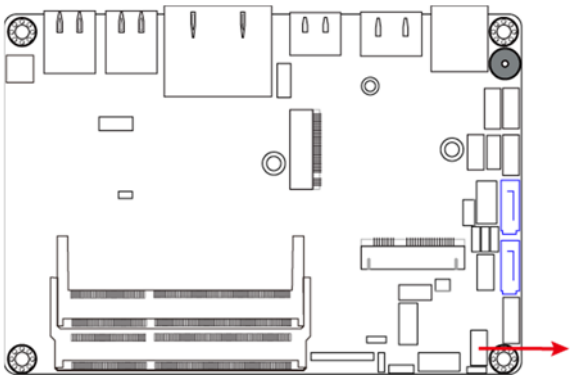
2.3.12 DisplayPort (CN8)

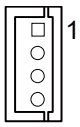


2.3.13 HDMI Port (CN9)



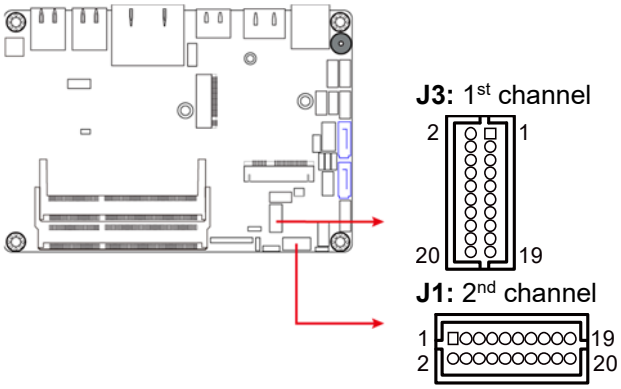
2.3.14 LCD Backlight Connector (J2)





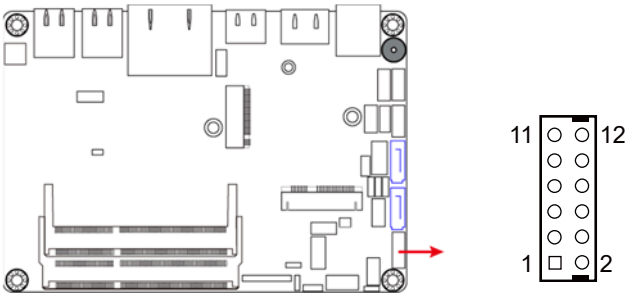
Pin	Assignment	Pin	Assignment
1	+12V	3	Brightness Control
2	Backlight Enable	4	Ground

2.3.15 LVDS Connector (J1, J3)



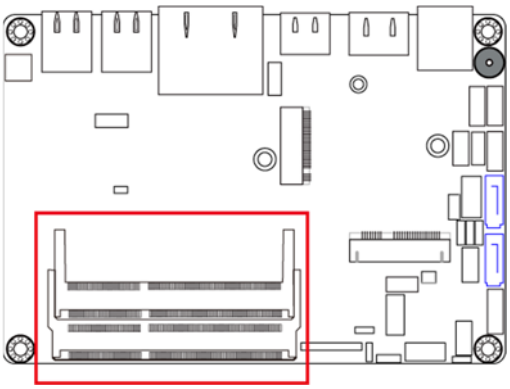
Pin	Assignment	Pin	Assignment
1	TX0P	2	TX0N
3	Ground	4	Ground
5	TX1P	6	TX1N
7	Ground	8	Ground
9	TX2P	10	TX2N
11	Ground	12	Ground
13	CLKP	14	CLKN
15	Ground	16	Ground
17	TX3P	18	TX3N
19	VDD	20	VDD

2.3.16 Audio Connector (J4)

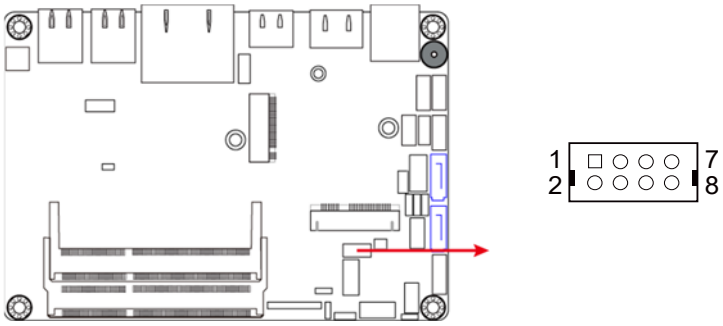


Pin	Assignment	Pin	Assignment
1	Lineout_L	2	Lineout_R
3	JD_FRONT	4	Ground
5	LINEIN_L	6	Linein_R
7	JD_LINEIN	8	Ground
9	MIC_L	10	MIC-R
11	JD_MIC1	12	Ground

2.3.17 DDR3L SO-DIMM Slot (J5, J8)

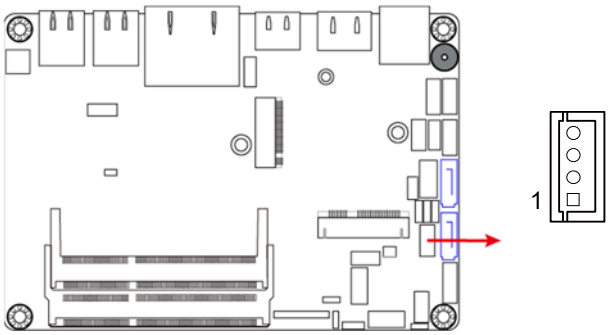


2.3.18 USB 2.0 Connector (J6)



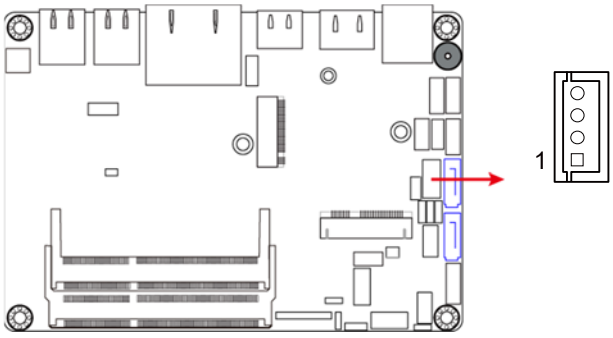
Pin	Assignment	Pin	Assignment
1	VCC	2	Ground
3	D0-	4	D1+
5	D0+	6	D1-
7	Ground	8	VCC

2.3.19 Amplifier Connector (J7)



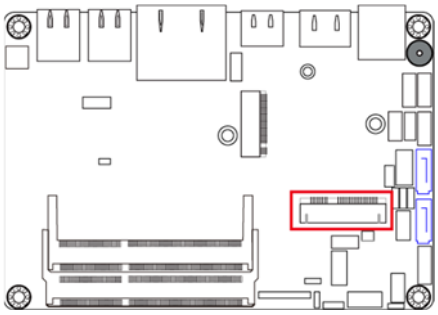
Pin	Assignment	Pin	Assignment
1	OUTL+	3	OUTR-
2	OUTL-	4	OUTR+

2.3.20 SATA HDD Power Connector (J10)

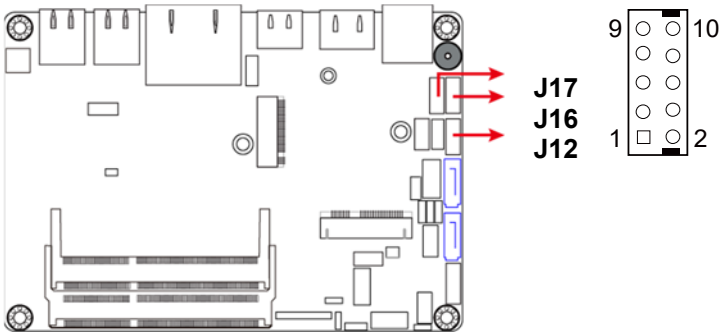


Pin	Assignment	Pin	Assignment
1	+5V	3	Ground
2	Ground	4	+12V

2.3.21 Mini PCIe / mSATA Slot (J11)



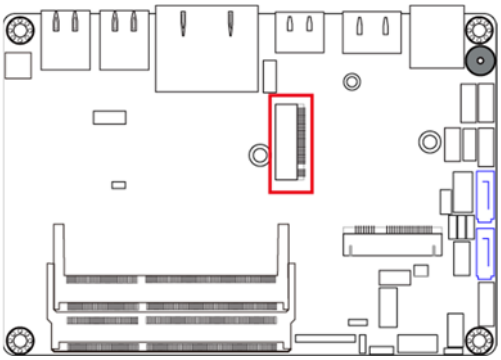
2.3.22 COM2 / COM3 / COM4 RS-232 Port (J16, J17, J12)



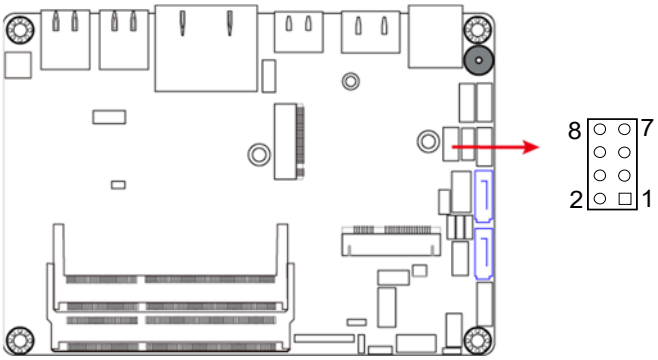
Pin	Assignment	Pin	Assignment
1	DCD, Data carrier detect	2	RXD, Receive data
3	TXD, Transmit data	4	DTR, Data terminal ready
5	Ground	6	DSR, Data set ready

7	RTS, Request to send	8	CTS, Clear to send
9	RI, Ring indicator	10	Not Used

2.3.23 M.2 (B key) 3042 Slot (J14)



2.3.24 Front Panel Connector (J13)

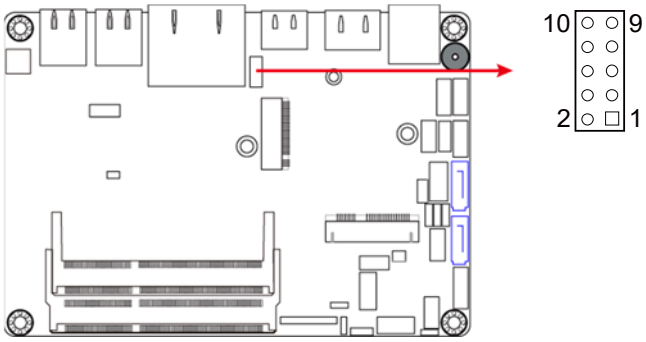


Pin	Assignment	Pin	Assignment
1	Ground	2	PWR_BTN
3	3.3V	4	HDD Active
5	Ground	6	Reset
7	+5V	8	Ground

J13 is utilized for system indicators to provide light indication of the computer activities and switches to change the computer status. It provides interfaces for the following functions.

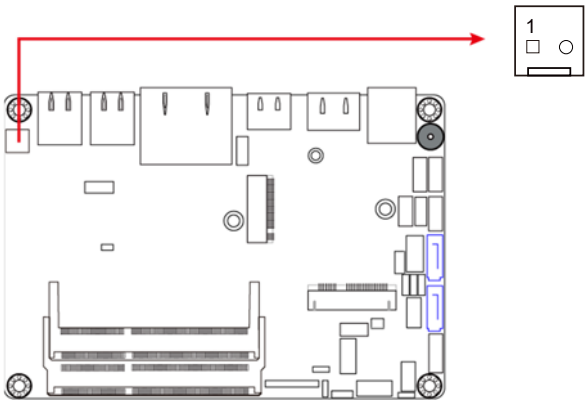
- **ATX Power ON Switch (Pins 1 and 2)**
- **Hard Disk Drive LED Connector (Pins 3 and 4)**
- **Reset Switch (Pins 5 and 6)**
- **Power LED: Pins 7 and 8**

2.3.25 Digital I/O Connector (J18)



Pin	Assignment	Pin	Assignment
1	Ground	2	VCC
3	OUT3	4	OUT1
5	OUT2	6	OUT0
7	IN3	8	IN1
9	IN2	10	IN0

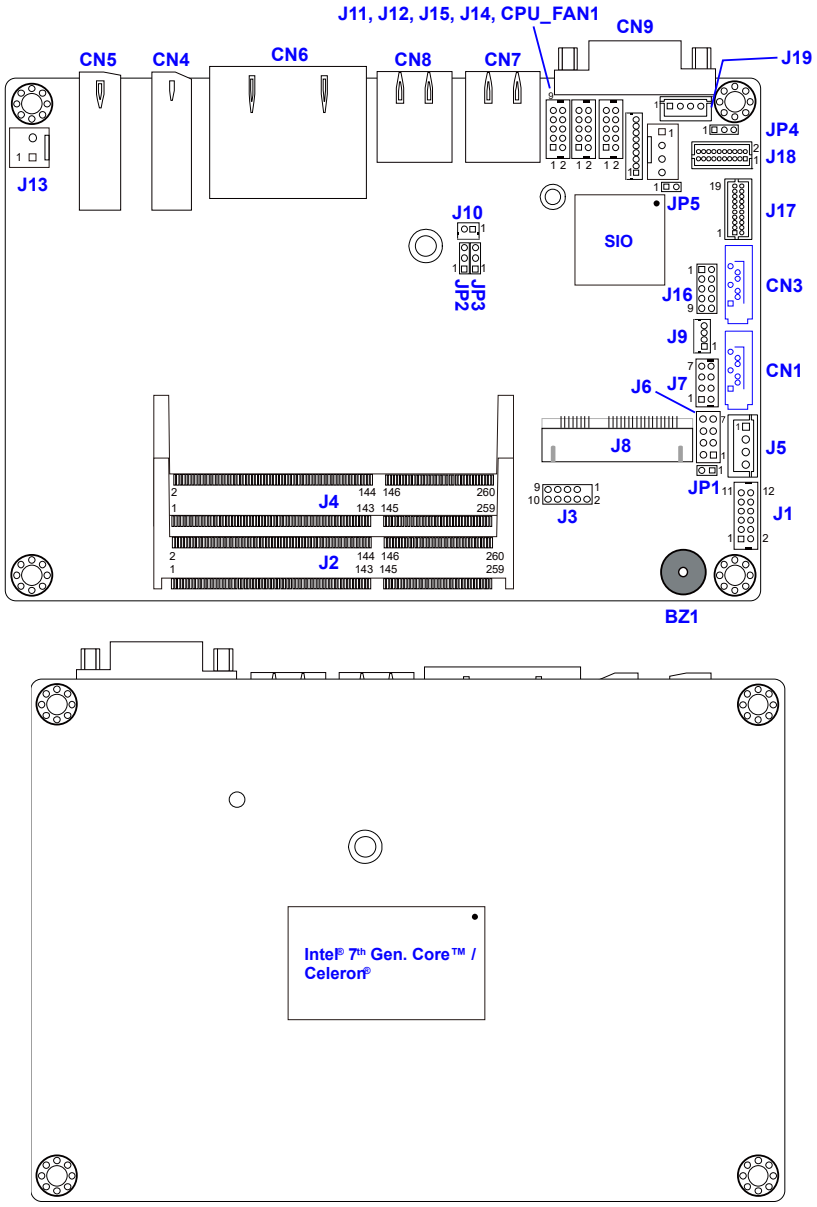
2.3.26 DC Power Input Connector (J19)



Pin	Assignment
1	+9V ~ +36V
2	Ground

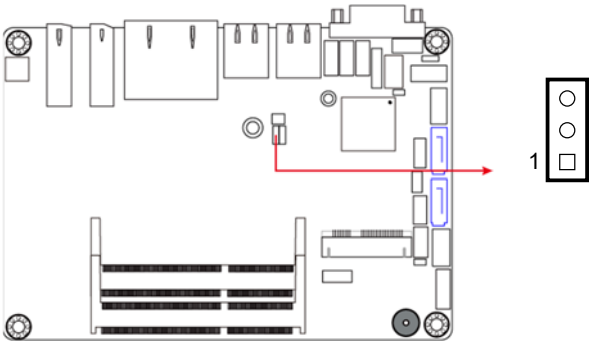
2.4 Jumper & Connector Locations (IB917)

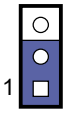
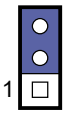
Motherboard: IB917



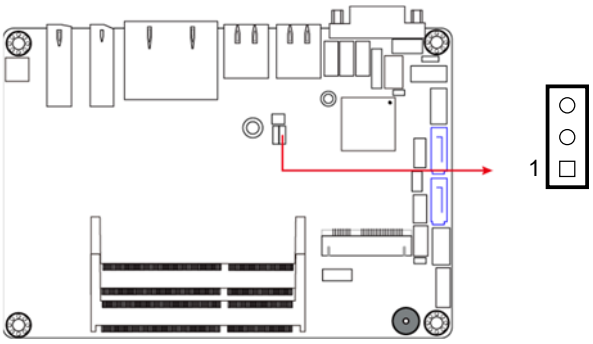
Board diagram of IB917

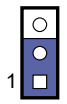
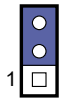
2.4.1 CMOS Data Clearance (JP2)



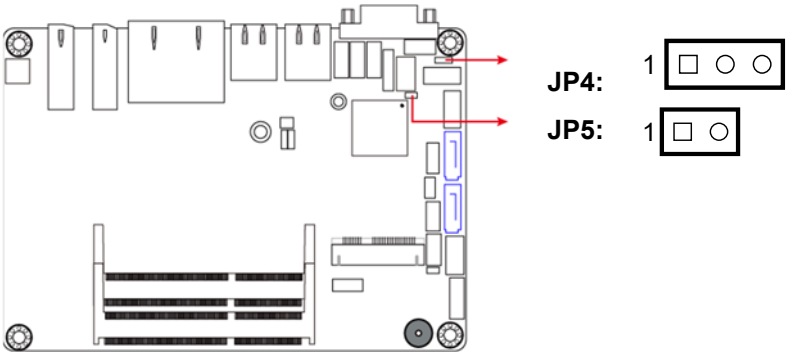
Function	Pin closed	Illustration
Normal (default)	1-2	
Clear CMOS	2-3	

2.4.2 ME Register Clearance (JP3)



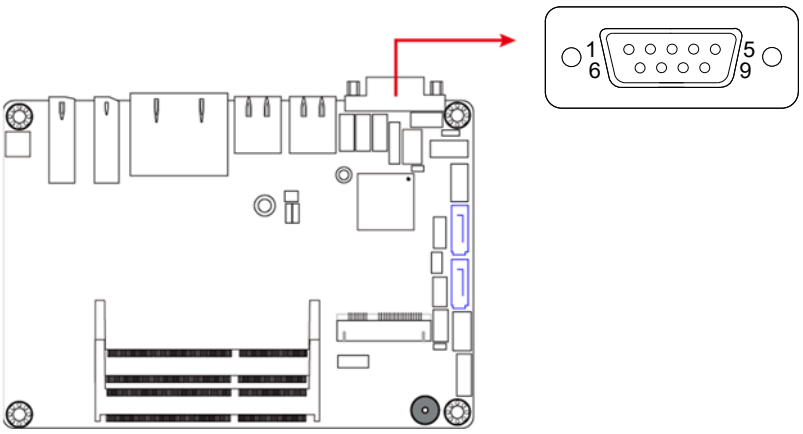
Function	Pin closed	Illustration
Normal (default)	1-2	
Clear ME	2-3	

2.4.3 LVDS Panel Power / Brightness Selections (JP4 / JP5)



Jumper	Function	Pin closed	Illustration
JP4	3.3V (default)	1-2	1
	5V	2-3	1
JP5	3.3V (default)	Open	1
	5V	Close	1

2.4.4 COM1 RS-232/422/485 Port (CN9)

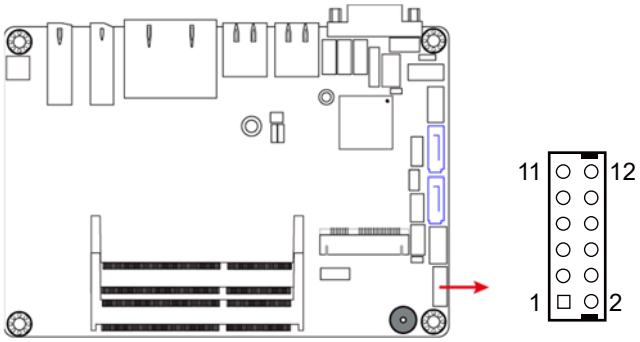


COM1 port is jumper-less and configurable in BIOS.

Pin	Assignment	Pin	Assignment
1	DCD, Data carrier detect	6	DSR, Data set ready
2	RXD, Receive data	7	RTS, Request to send
3	TXD, Transmit data	8	CTS, Clear to send
4	DTR, Data terminal ready	9	RI, Ring indicator
5	Ground		

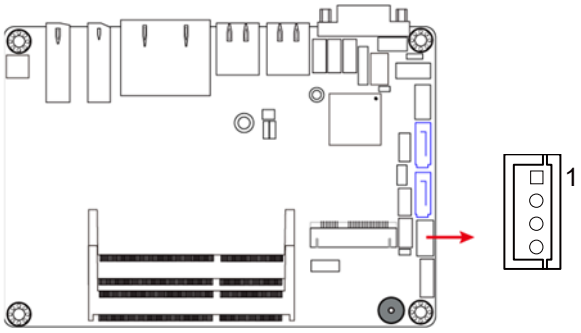
Pin	Assignment		
	RS-232	RS-422	RS-485
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

2.4.5 Audio Connector (J1)



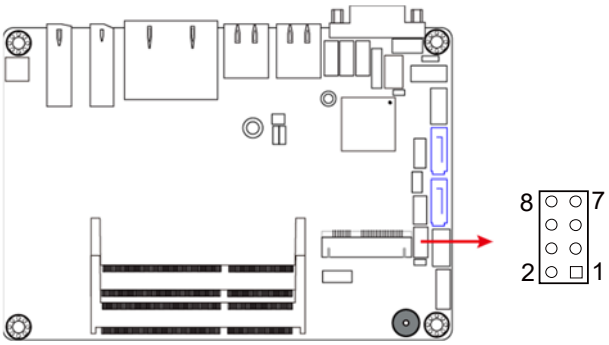
Pin	Assignment	Pin	Assignment
1	Lineout_L	2	Lineout_R
3	JD_FRONT	4	Ground
5	LINEIN_L	6	Linein_R
7	JD_LINEIN	8	Ground
9	MIC_L	10	MIC-R
11	JD_MIC1	12	Ground

2.4.6 SATA HDD Power Connector (J5)



Pin	Assignment	Pin	Assignment
1	+5V	3	Ground
2	Ground	4	+12V

2.4.7 Front Panel Connector (J6)

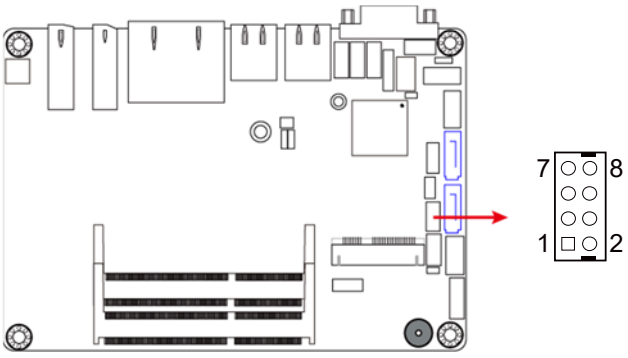


Pin	Assignment	Pin	Assignment
1	Ground	2	PWR_BTN
3	3.3V	4	HDD Active
5	Ground	6	Reset
7	+5V	8	Ground

J6 is utilized for system indicators to provide light indication of the computer activities and switches to change the computer status. It provides interfaces for the following functions.

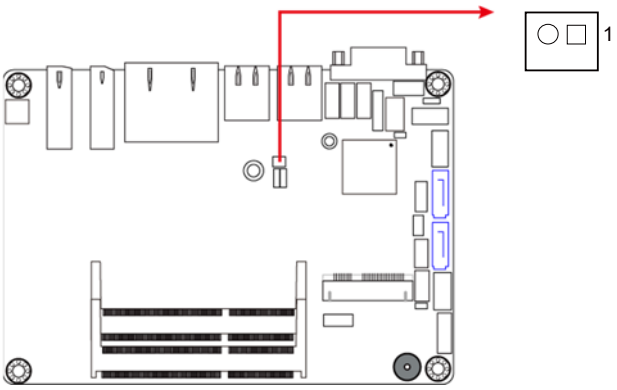
- **ATX Power ON Switch (Pins 1 and 2)**
  The 2 pins makes an “ATX Power Supply On/Off Switch” for the system that connects to the power switch on the case. When pressed, the power switch will force the system to power on. When pressed again, it will power off the system.
- **Hard Disk Drive LED Connector (Pins 3 and 4)**
  This connector connects to the hard drive activity LED on control panel. This LED will flash when the HDD is being accessed.
- **Reset Switch (Pins 5 and 6)**
  The reset switch allows you to reset the system without turning the main power switch off and then on again. Orientation is not required when making a connection to this header.
- **Power LED: Pins 7 and 8**
  This connector connects to the system power LED on control panel. This LED will light when the system turns on.

2.4.8 USB 2.0 Connector (J7)



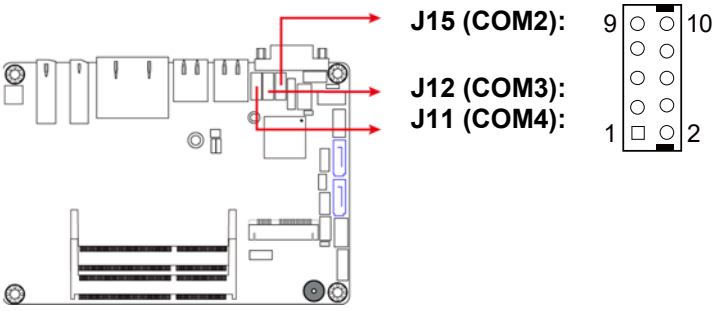
Pin	Assignment	Pin	Assignment
1	VCC	2	Ground
3	D0-	4	D1+
5	D0+	6	D1-
7	Ground	8	VCC

2.4.9 Battery Connector (J10)



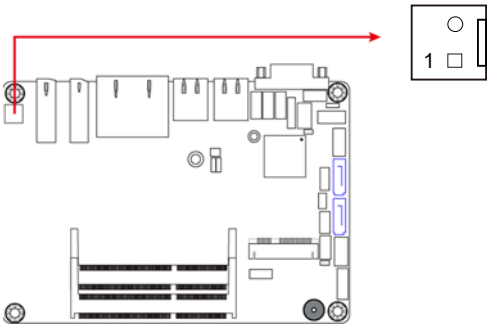
Pin	Assignment
1	Battery+
2	Ground

2.4.10 COM2, COM3, COM4 RS-232 Ports (J15, J12, J11)



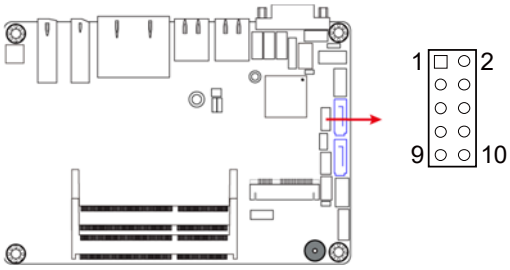
Pin	Assignment	Pin	Assignment
1	DCD, Data carrier detect	2	RXD, Receive data
3	TXD, Transmit data	4	DTR, Data terminal ready
5	Ground	6	DSR, Data set ready
7	RTS, Request to send	8	CTS, Clear to send
9	RI, Ring indicator	10	Not Used

2.4.11 DC Power Input Connector (J13)



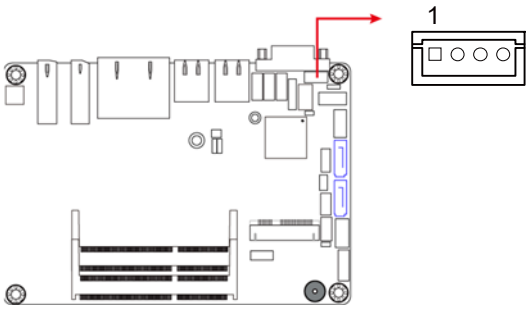
Pin	Assignment
1	+9V ~ +24V
2	Ground

2.4.12 Digital I/O Connector (J16)



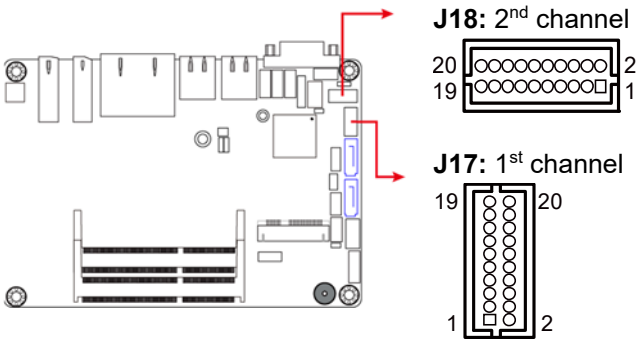
Pin	Assignment	Pin	Assignment
1	Ground	2	VCC
3	OUT3	4	OUT1
5	OUT2	6	OUT0
7	IN3	8	IN1
9	IN2	10	IN0

2.4.13 LCD Backlight Connector (J19)



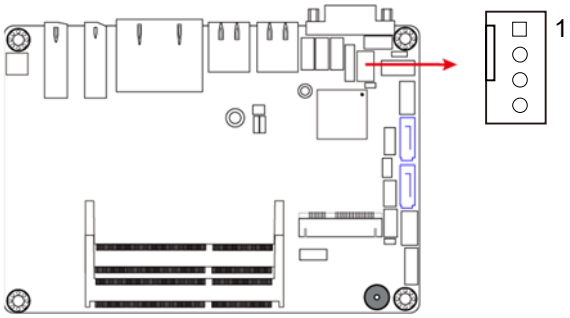
Pin	Assignment	Pin	Assignment
1	+12V	3	Brightness Control
2	Backlight Enable	4	Ground

2.4.14 LVDS Connector (J17, J18)



Pin	Assignment	Pin	Assignment
1	TX0P	2	TX0N
3	Ground	4	Ground
5	TX1P	6	TX1N
7	Ground	8	Ground
9	TX2P	10	TX2N
11	Ground	12	Ground
13	CLKP	14	CLKN
15	Ground	16	Ground
17	TX3P	18	TX3N
19	Power	20	Power

2.4.15 CPU Fan Connector (CPU_FAN1)



Pin	Assignment	Pin	Assignment
1	Ground	3	CPU Fan In
2	12V	4	CPU Fan Out

Chapter 3
Driver Installations

The driver installation information in this chapter is for the IB811F and IB917 boards.

3.1 Intel® Chipset Software Installation Utility (IB811F)

The Intel® Chipset drivers should be installed first before the software drivers to install INF files for Plug & Play function for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the disk enclosed in the package. Click **Intel** on the left pane and then **Intel(R) Apollolake Chipset Drivers** on the right pane.
2. Click **Intel(R) Chipset Software Installation Utility**.

3. When the *Welcome* screen to the Intel® Chipset Device Software appears, click **Next** to continue.
4. Click **Yes** to accept the software license agreement and proceed with the installation process.
5. On the *Readme File Information* screen, click **Install** for installation.
6. The driver has been completely installed. You are suggested to restart the computer for changes to take effect.

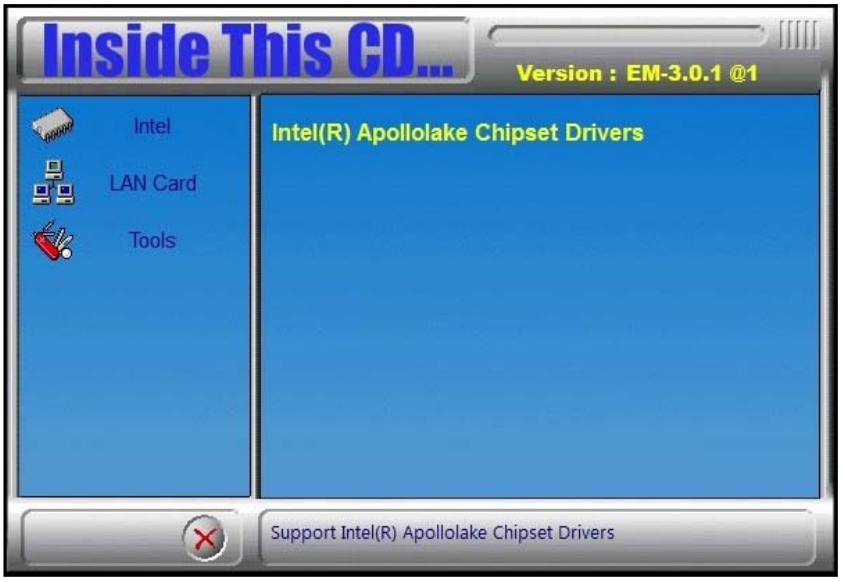
3.2 VGA Driver Installation (IB811F)

1. Click **Intel** on the left pane and then **Intel(R) Apollolake Chipset Drivers** on the right pane.
2. Click **Intel(R) Apollolake Graphics Driver**.

3. When the *Welcome* screen appears, click **Next** to continue.
4. Click **Yes** to accept the license agreement and click **Next** until the installation starts.
5. The driver has been completely installed. You are suggested to restart the computer for changes to take effect.

3.3 HD Audio Driver Installation (IB811F)

1. Click **Intel** on the left pane and then **Intel(R) Apollolake Chipset Drivers** on the right pane.



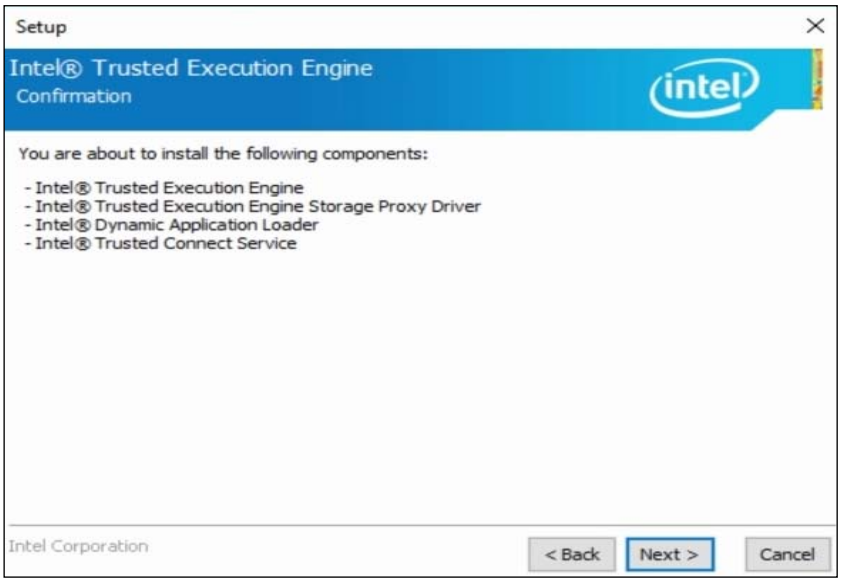
2. Click **Realtek High Definition Audio Driver**.

3. On the *Welcome* screen of the InstallShield Wizard, click **Next** for installation.
4. Click **Next** until the installation starts.
5. The driver has been completely installed. You are suggested to restart the computer for changes to take effect.

3.4 Intel® Trusted Execution Engine Drivers (IB811F)

1. Click **Intel** on the left pane and then **Intel(R) Apollolake Chipset Drivers** on the right pane.
2. Click **Intel(R) TXE Drivers**.

3. When the *Welcome* screen appears, click **Next**.
4. Accept the license agreement and click **Next**.
5. Click **Next** for installation.



6. As the driver has been sccessfully installed, you are suggested to restart the computer for changes to take effect.

3.5 Intel® Serial IO Drivers (IB811F)

1. Click **Intel** on the left pane and then **Intel(R) Apollolake Chipset Drivers** on the right pane.
2. Click **Intel(R) Serial IO Drivers**.

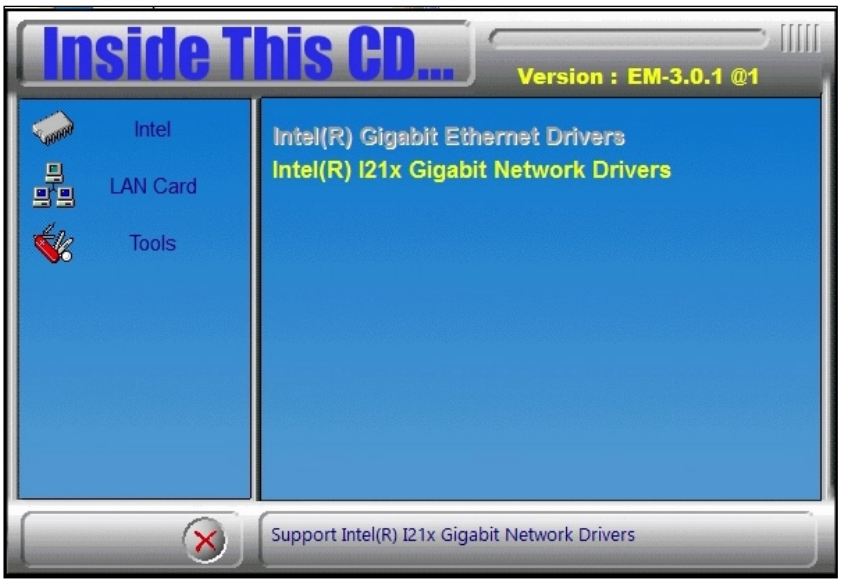
3. When the *Welcome* screen to the InstallShield Wizard appears, click **Next**.

4. Accept the license agreement and click **Next**.
5. After reading the *Readme File Information*, click **Next** for installation.
6. As the driver has been sccessfully installed, you are suggested to restart the computer for changes to take effect.

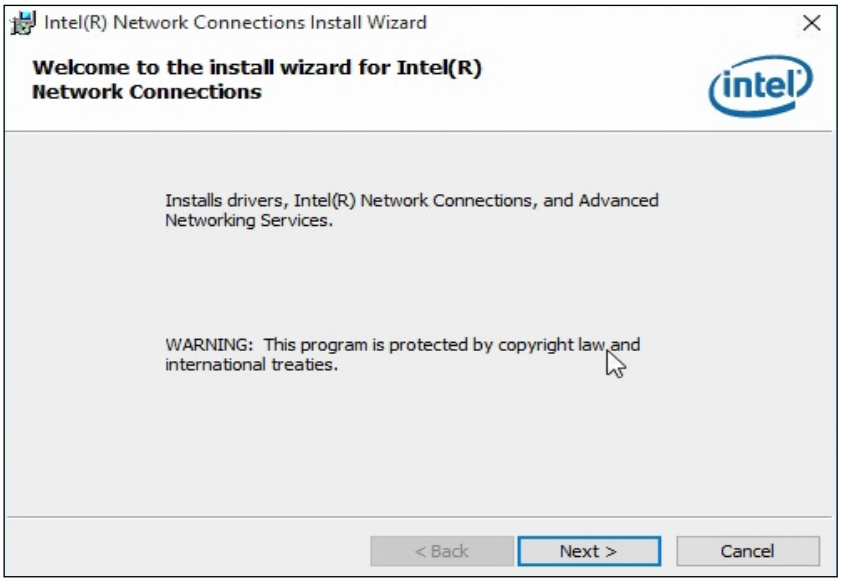
3.6 LAN Driver Installation (IB811F)

1. Click **LAN Card** on the left pane and then **Intel LAN Controller Drivers** on the right pane.

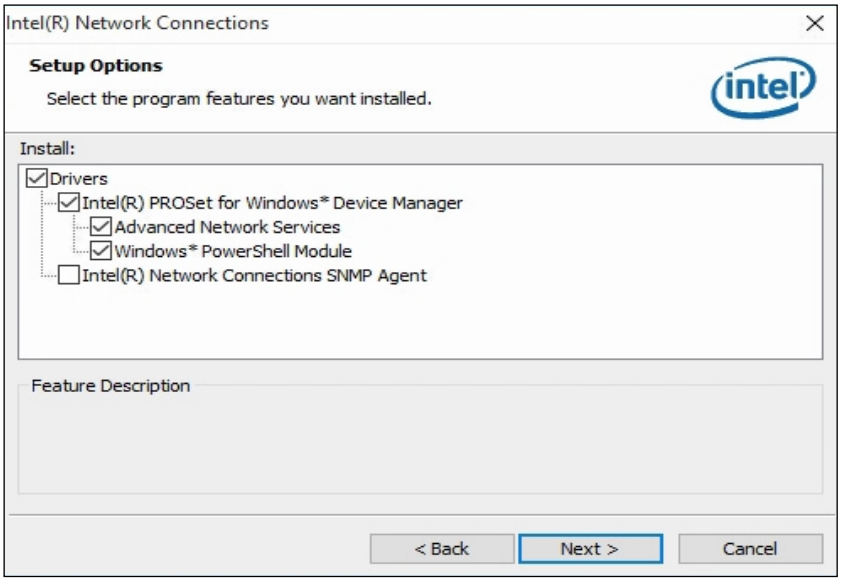
2. Click **Intel(R) I21x Gigabit Network Drivers.**.



3. When the *Welcome* screen appears, click **Next**.



4. Accept the license agreement and click **Next**.
5. On the *Setup Options* screen, click the checkbox to select the desired driver(s) for installation. Then click **Next** to continue.



6. The wizard is ready for installation. Click **Install**.
7. As the installation is complete, you are suggested to restart the computer for changes to take effect.

3.7 Intel® Chipset Software Installation Utility (IB917)

The Intel® Chipset drivers should be installed first before the software drivers to install INF files for Plug & Play function for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the disk enclosed in the package. Click **Intel** on the left pane and then **Intel(R) Kabylake-U Chipset Drivers** on the right pane.

2. Click **Intel(R) Chipset Software Installation Utility**.

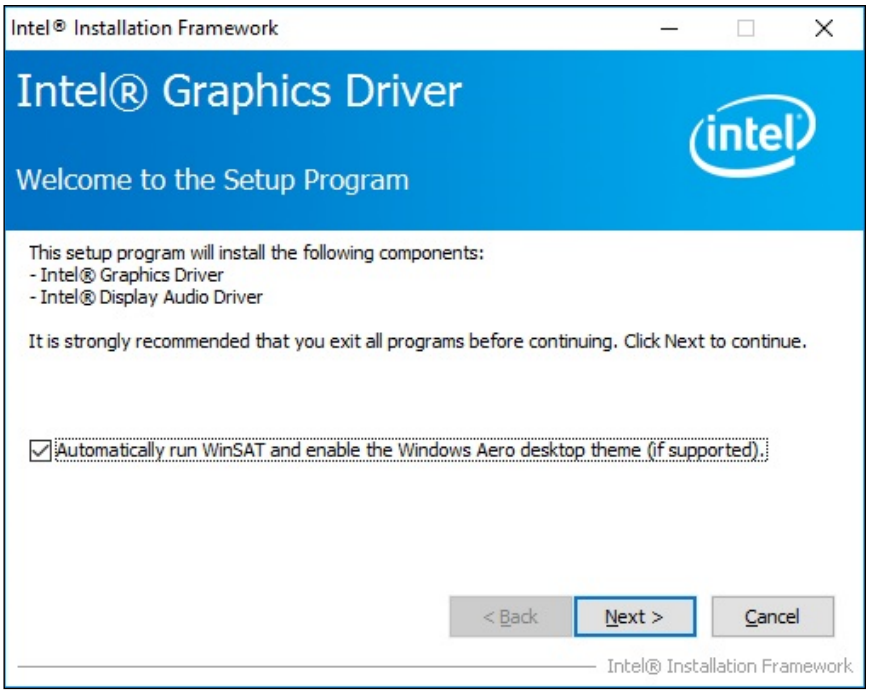
3. When the *Welcome* screen to the Intel® Chipset Device Software appears, click **Next** to continue.
4. Accept the software license agreement and proceed with the installation process.
5. On the *Readme File Information* screen, click **Install** for installation.
6. After the installation, restart the computer for changes to take effect.

3.8 VGA Driver Installation (IB917)

1. Insert the disk enclosed in the package. Click **Intel** on the left pane and then **Intel(R) Kabylake-U Chipset Drivers** on the right pane.

2. Click **Intel(R) HD Graphics Driver**.

3. When the *Welcome* screen appears, click **Next** to continue.



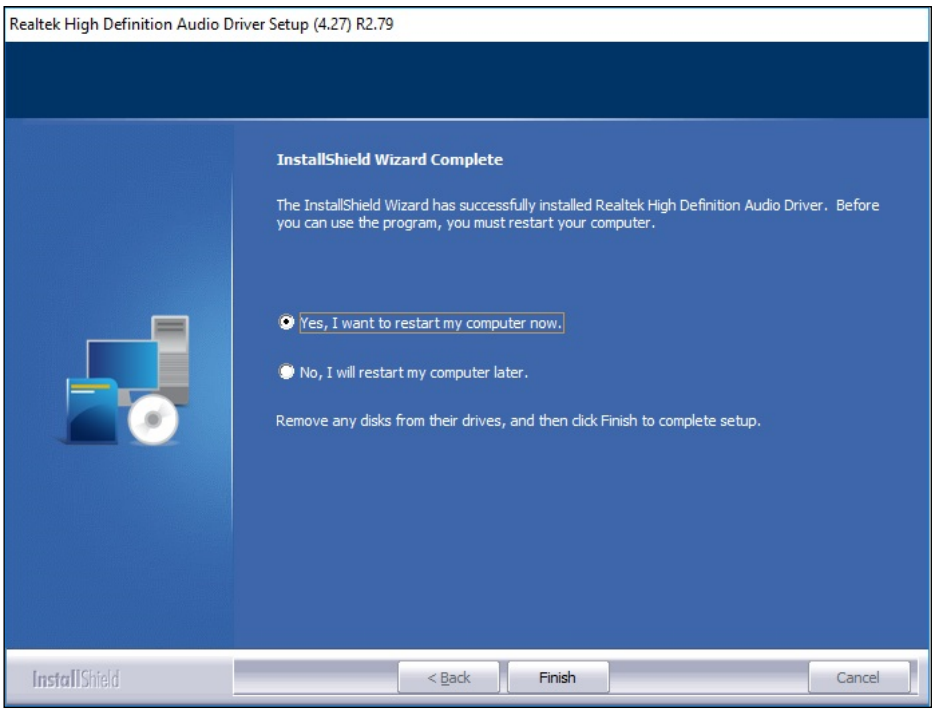
4. Click **Yes** to accept the license agreement and click **Next** until the installation starts.
5. On the *Readme File Information* screen, click **Next** until the installation starts.
6. After the installation, restart the computer for changes to take effect.

3.9 HD Audio Driver Installation (IB917)

1. Insert the disk enclosed in the package. Click **Intel** on the left pane and then **Intel(R) Kabylake-U Chipset Drivers** on the right pane.

2. Click **Realtek High Definition Audio Driver**.

3. On the *Welcome* screen of the InstallShield Wizard, click **Next**.



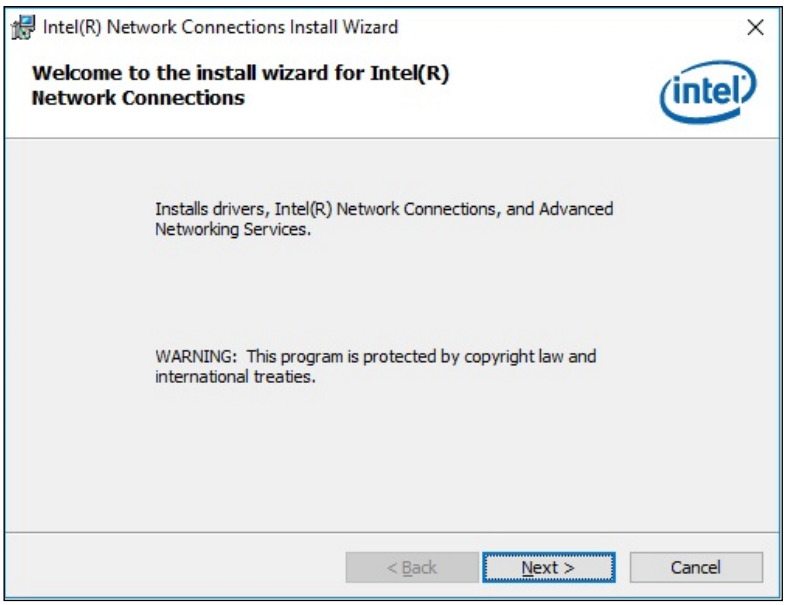
4. Click **Next** until the installation starts.
5. After the installation, restart the computer for changes to take effect.

3.10 LAN Driver Installation (IB917)

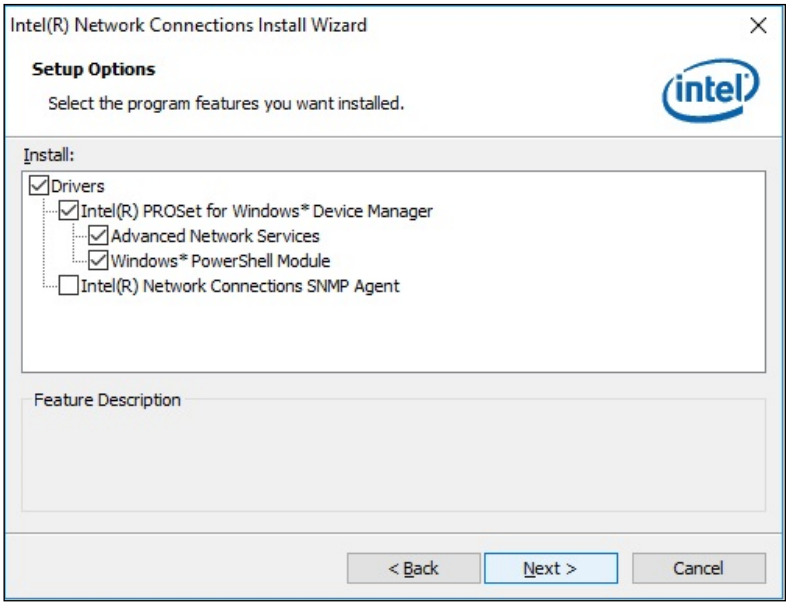
1. Insert the disk enclosed in the package. Click **Intel** on the left pane and then **Intel(R) Kabylake-U Chipset Drivers** on the right pane.

2. Click **Intel(R) PRO LAN Network Drivers**..

3. When the *Welcome* screen appears, click **Next**.



4. Accept the license agreement and click **Next**.
5. On the *Setup Options* screen, click the checkbox to select the desired driver(s) for installation. Then click **Next** to continue.



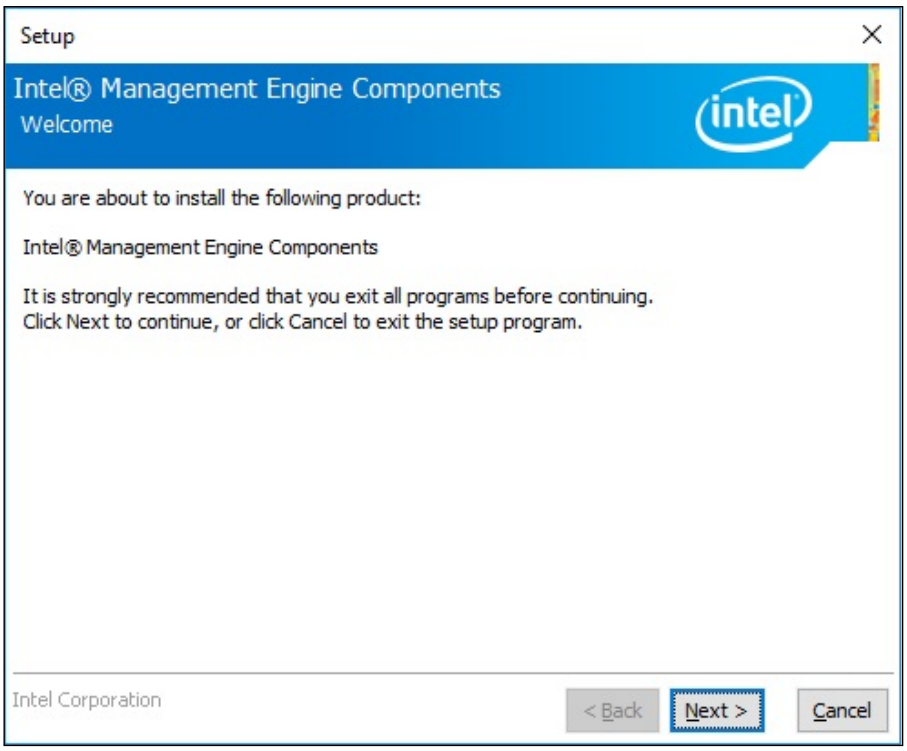
6. The wizard is ready for installation. Click **Install**.
7. After the installation, restart the computer for changes to take effect.

3.11 Intel® Management Engine Drivers Installation (IB917)

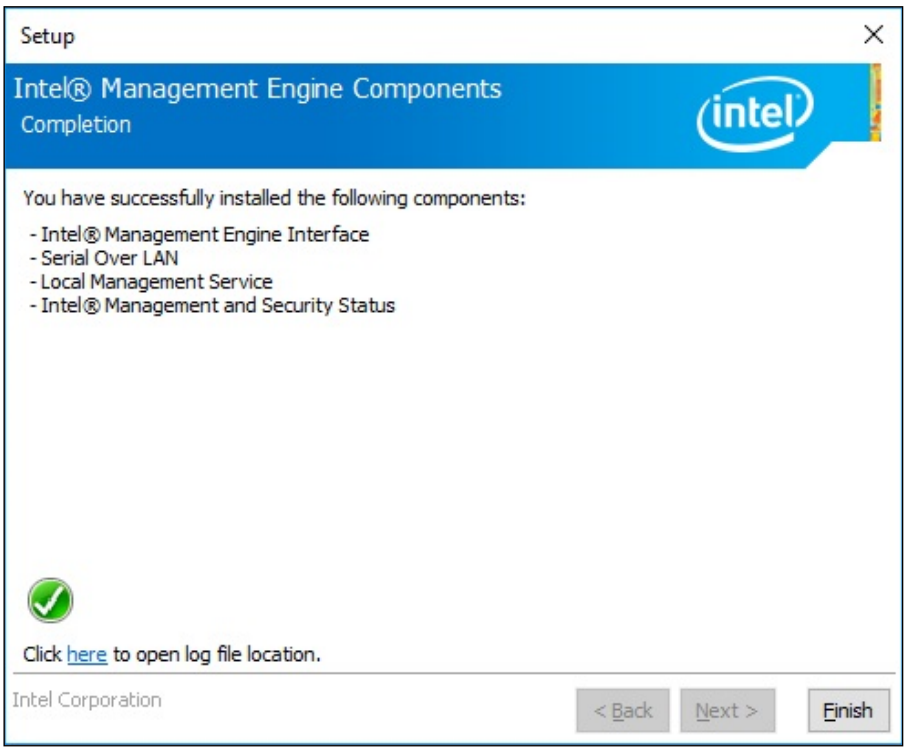
1. Insert the disk enclosed in the package. Click **Intel** on the left pane and then **Intel(R) Kabylake-U Chipset Drivers** on the right pane.

2. Click **Intel(R) ME 11.x Drivers**.

3. When the *Welcome* screen appears, click **Next**.



4. Accept the license agreement and click **Next** until the installation starts.
5. After the installation, restart the computer for changes to take effect.



Chapter 4
BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the IB811F and IB917 boards installed in the OFP-151-PC system.

4.1 Introduction

The BIOS (Basic Input/Output System) installed in the ROM of your computer system supports Intel® processors. The BIOS provides critical low-level support for standard devices such as disk drives, serial ports and parallel ports. It also provides password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

4.2 BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Press the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup.

If you still need to enter Setup, restart the system by pressing the ”Reset” button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again.

The following message will appear on the screen:

```
Press <DEL> to Enter Setup
```

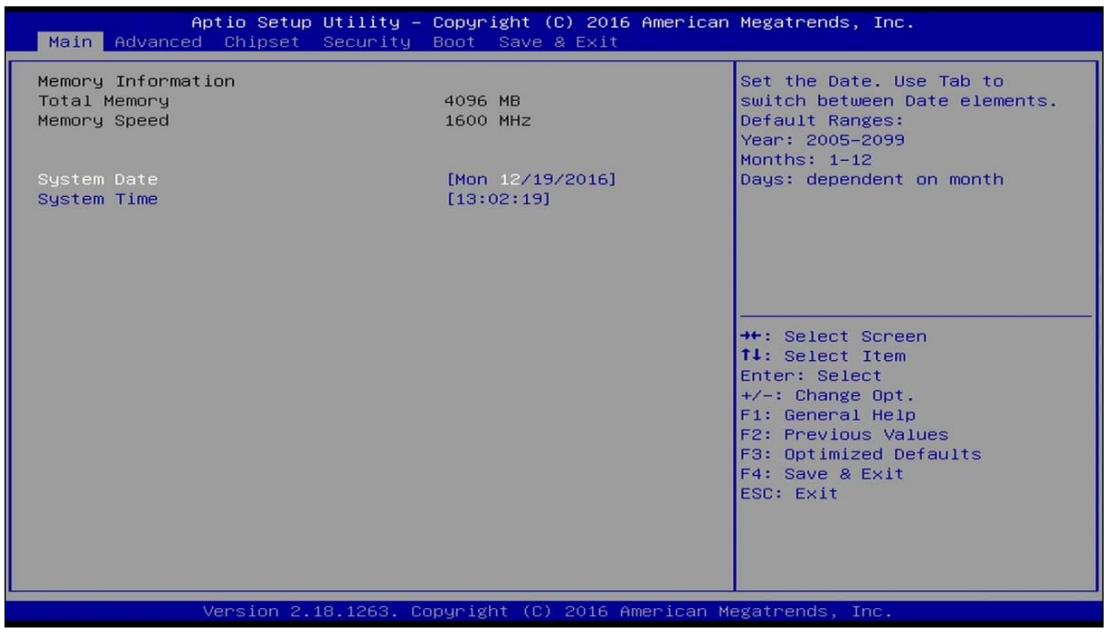
In general, press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help, and <Esc> to quit.

When you enter the BIOS Setup utility, the *Main Menu* screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: It is strongly recommended that you avoid making any changes to the chipset defaults.

These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could make the system unstable and crash in some cases.

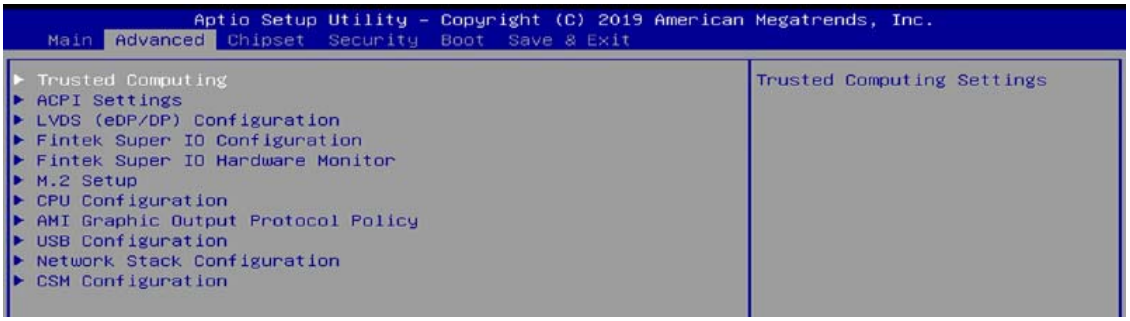
4.3 Main Settings (IB818F)



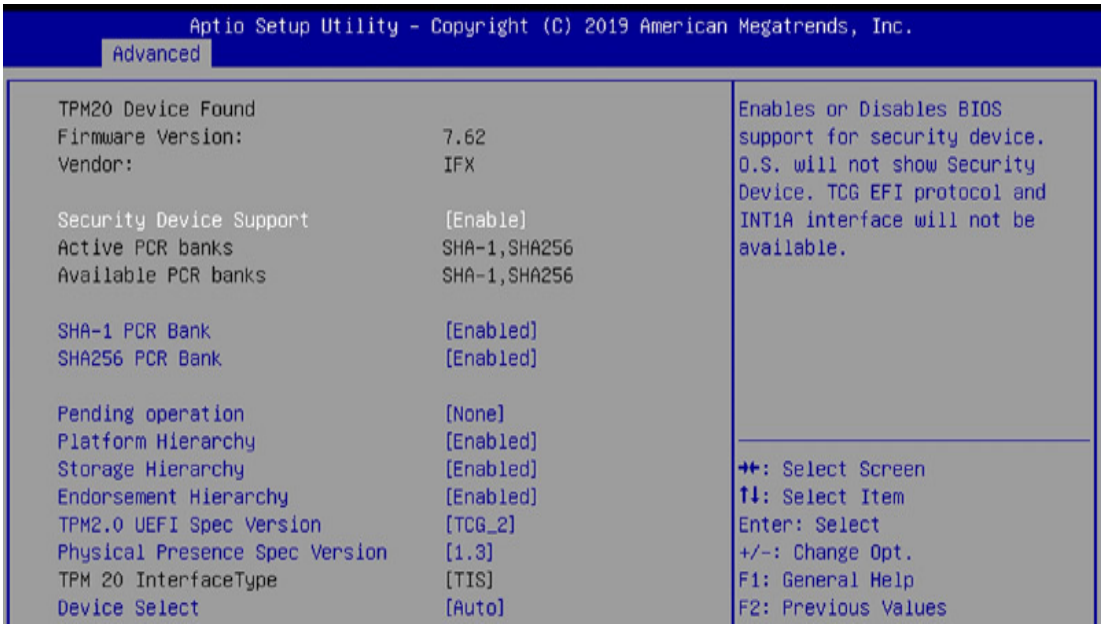
BIOS Setting	Description
System Date	Sets the date. Use the <Tab> key to switch between the data elements.
System Time	Set the time. Use the <Tab> key to switch between the data elements.

4.4 Advanced Settings (IB818F)

This section allows you to configure, improve your system and allows you to set up some system features according to your preference.

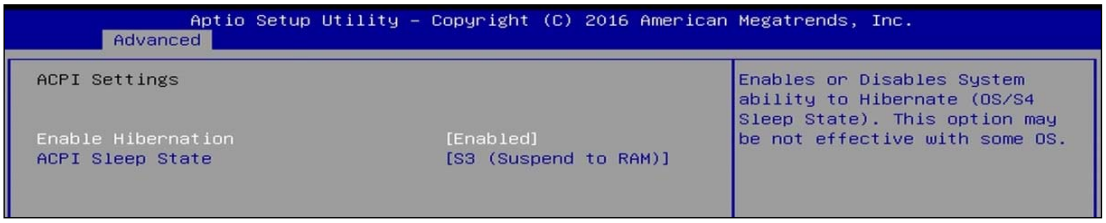


4.4.1 Trusted Computing



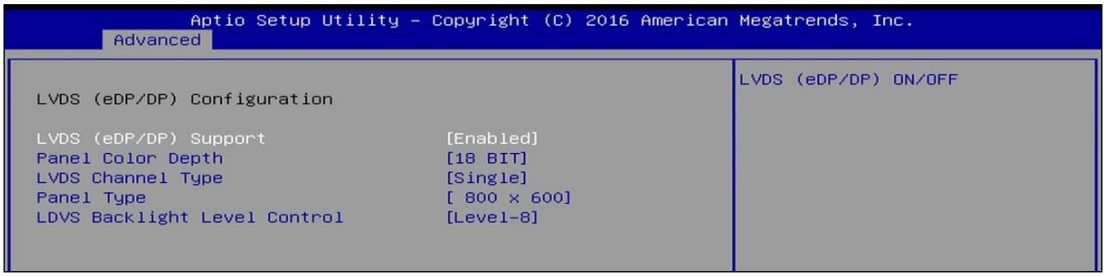
BIOS Setting	Description
Security Device Support	Enables / Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
SHA-1 PCR Bank	Enable or Disable SHA1 PCR Bank
SHA256 PCR Bank	Enable or Disable SHA256 PCR Bank
SHA-1 PCR Bank	Enable or Disable SHA1 PCR Bank
Pending operation	Schedule an operation for the security device. NOTE: Your computer will reboot dring restart in order to change state of security device. Options: None, TPM Clear
Platform Hierarchy	Enable or Disable Platform Hierarchy
Storage Hierarchy	Enable or Disable Storage Hierarchy
Endorsement Hierarchy	Enable or Disable Endorsement Hierarchy
TPM2.0 UEFI Spec Version	Select the TCG2 Spec Version Support TCG_1_2: the Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later
Physical Presence Spec Version	Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.
Device Select	TPM 1.2 will restrict support to TPM 1.2 devices. TPM 2.0 will restrict support to TPM 2.0 devices. Auto will support both with the default sat to TPM 2.0 devices if not found. TPM 1.2 devices will be enumerated.

4.4.2 ACPI Computing



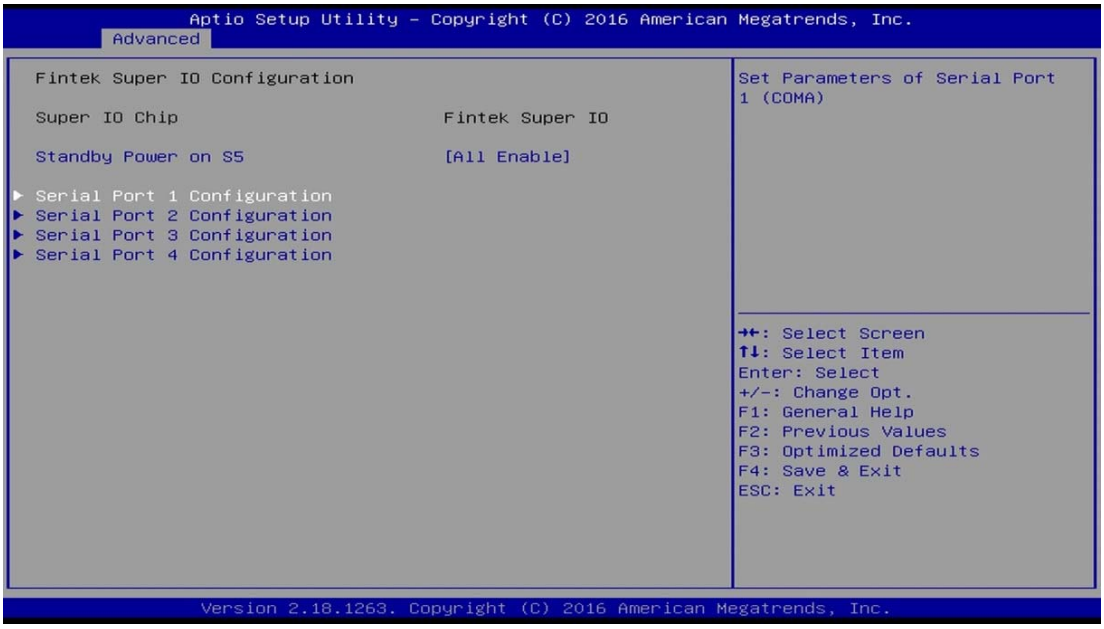
BIOS Setting	Description
Enable Hibernation	Enables / Disables the system ability to hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Selects an ACPI sleep state (Suspend Disabled or S3) where the system will enter when the Suspend button is pressed.

4.4.3 LVDS (eDP/DP) Configuration

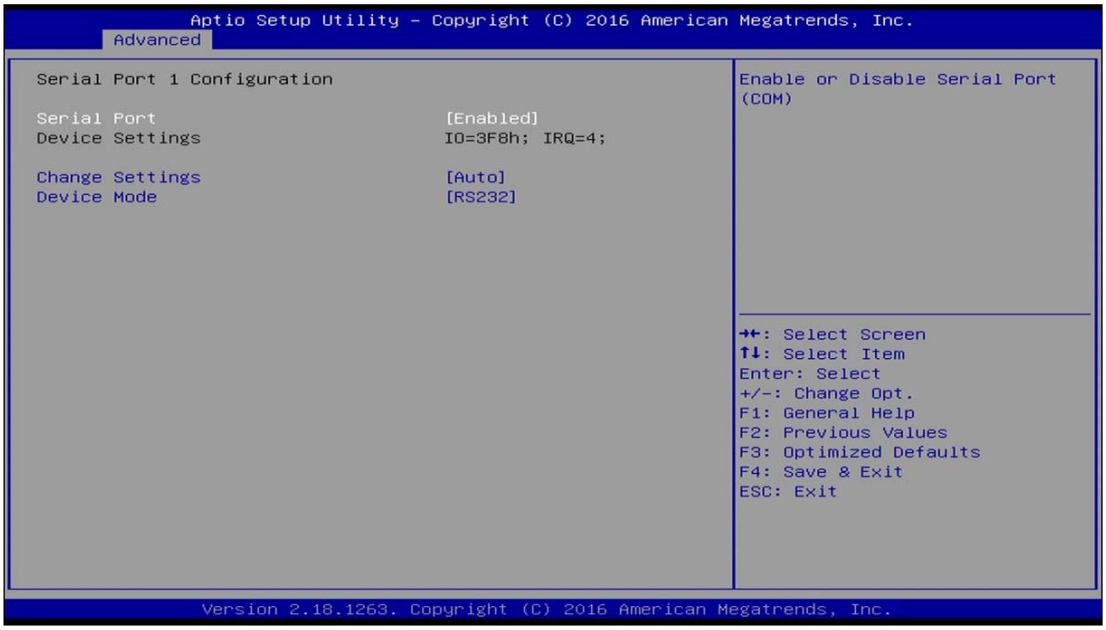


BIOS Setting	Description
LVDS (eDP/DP) Support	Enables / Disables LVDS (eDP/DP)
Panel Color Depth	Selects a panel color depth as 18 or 24 (VESA or JEIDA) bit.
LVDS Channel Type	Sets the LVDS channel type as single or dual channel.
Panel Type	Selects a resolution that fits your panel. Options: 800 x 600 / 1024 x 768 / 1280 x 1024 / 1366 x 768 / 1440 x 900 / 1600 x 900 / 1920 x 1080
LVDS Backlight Level Control	Selects from Level 1 to Level 8 for the LVDS backlight.

4.4.4 Fintek Super IO Configuration

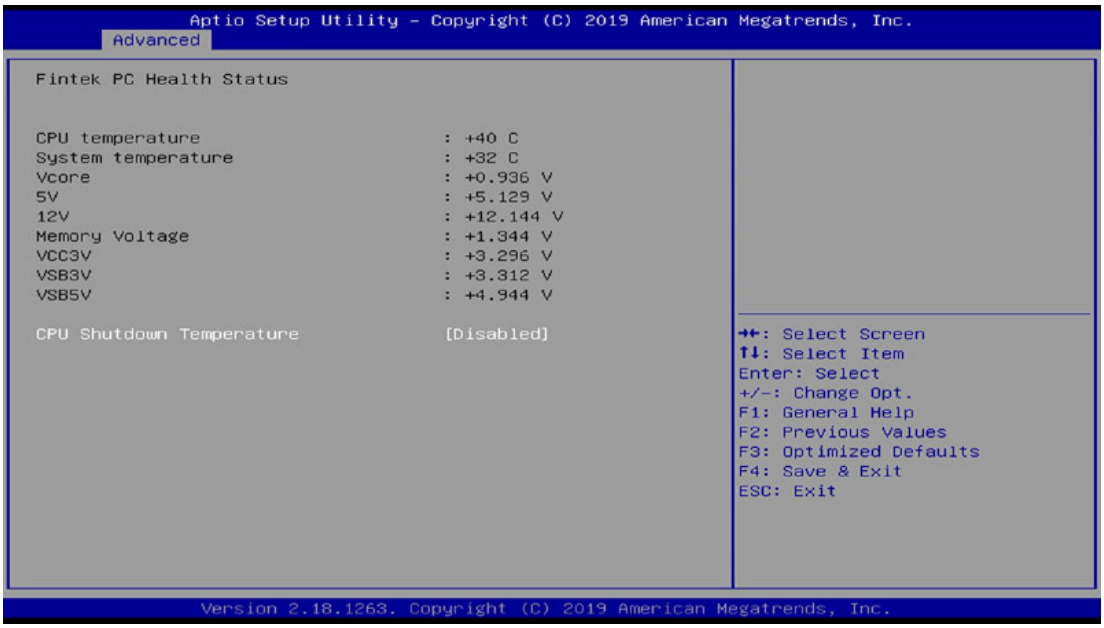


BIOS Setting	Description
Standby Power on S5	Enables / Disables to provide the standby power for devices. Options: All Enable / Enable Ethernet for WOL / All Disable
Serial Ports Configuration	Sets parameters of serial ports. Enables / Disables the serial port and select an optimal setting for the Super IO device.



BIOS Setting	Description
Serial Port	Enables / Disables the serial port.
Change Settings	Selects an optimal settings for Super IO device. Options: • Auto • IO = 3F8h; IRQ = 4 • IO = 3F8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2F8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 3E8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2E8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12
Device Mode	Changes the serial port mode to: • RS232 • RS485 TX Low Active • RS485 with Termination TX Low Active • RS422 • RS422 with Termination

4.4.5 Fintek Super IO Hardware Monitor

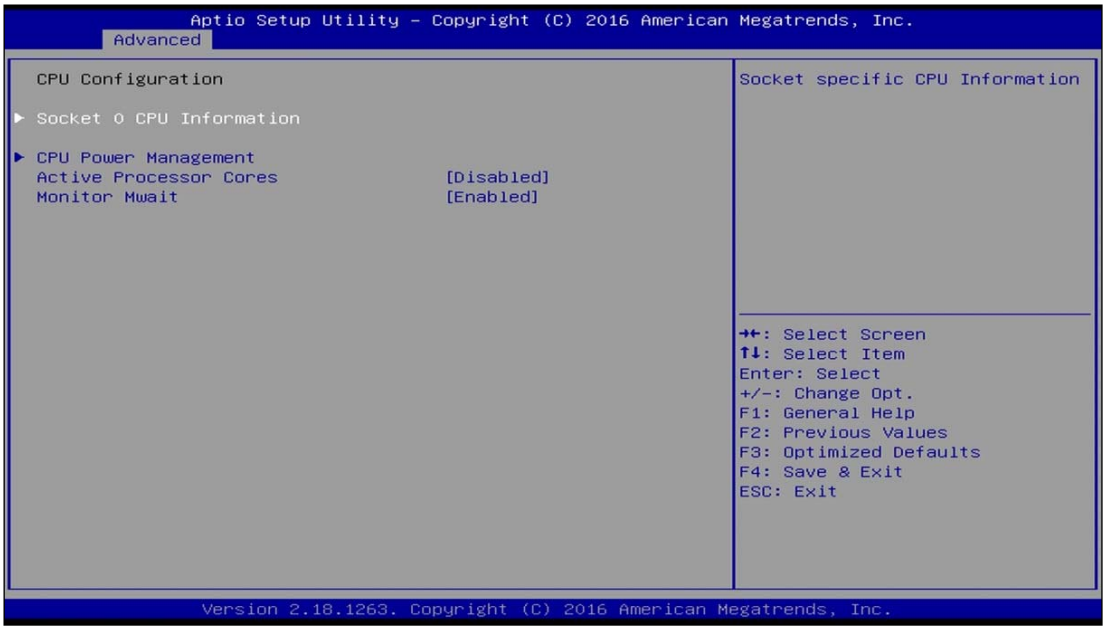


BIOS Setting	Description
Temperatures / Voltages	These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.
CPU Shutdown Temperature	Sets a threshold of temperature to shut down if CPU goes overheated. Options: Disabled / 70 °C / 75 °C / 80 °C / 85 °C / 90 °C / 95 °C

4.4.6 M.2 Setup

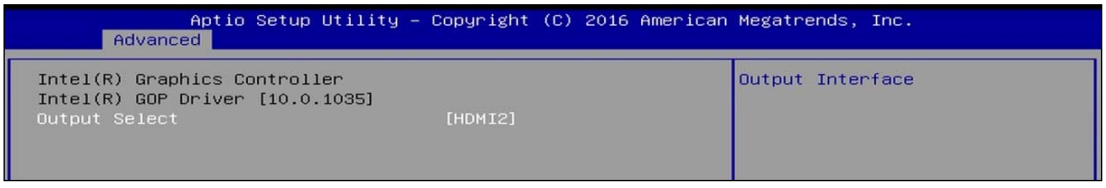
BIOS Setting	Description
M.2 Select	Selects the M.2 interface as SATA or PCIe.

4.4.7 CPU Configuration



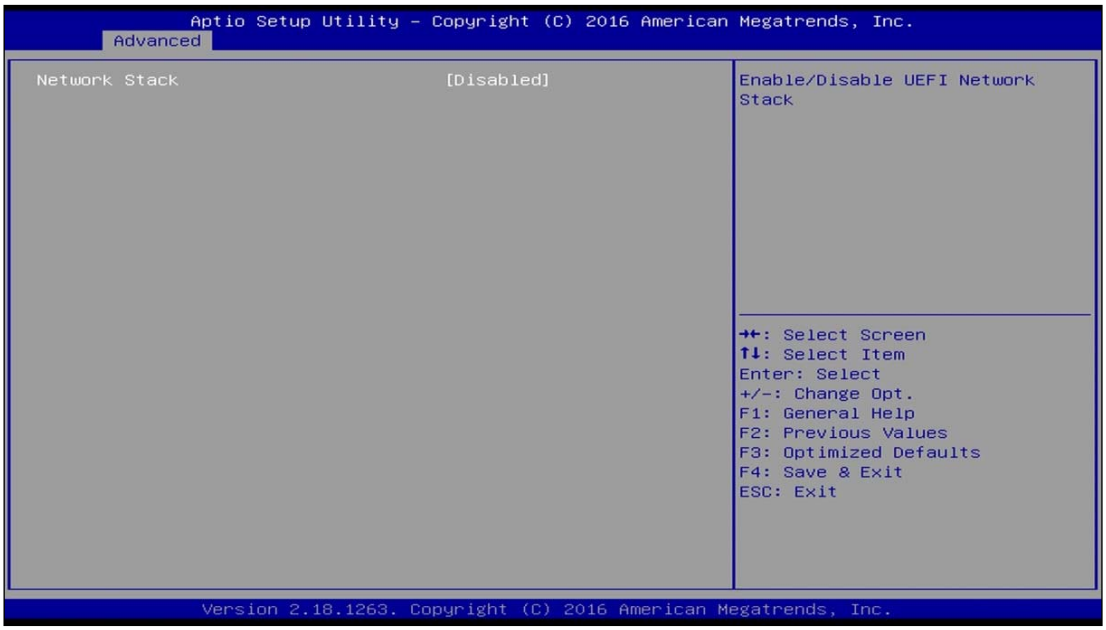
BIOS Setting	Description
Socket 0 CPU Information	Displays the socket specific CPU information.
CPU Power Management	Allows you to enable / disable Turbo Mode.
Active Processor Cores	Enables / Disables the cores in the processor package.
Monitor Mwait	Enables / Disables Monitor Mwait.

4.4.8 AMI Graphic Output Protocol Policy



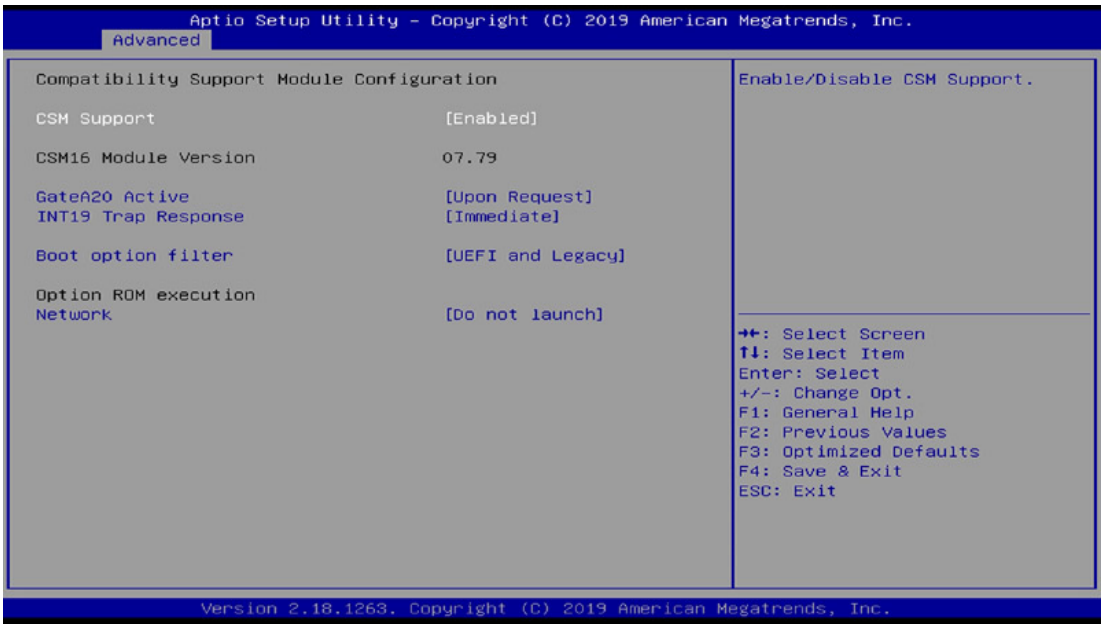
BIOS Setting	Description
Output Select	Outputs through HDMI interface.

4.4.9 Network Stack Configuration



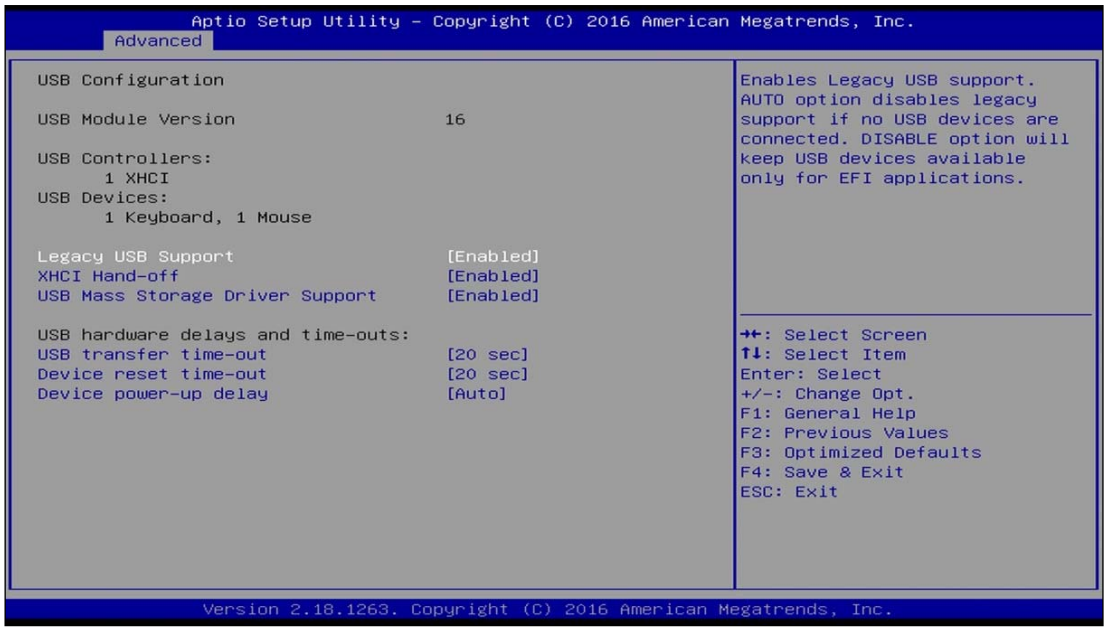
BIOS Setting	Description
Network Stack	Enables / Disables UEFI Network Stack.
IPv4 PXE Support	Enables / Disables IPv4 PXE Boot Support. If disabled, Ipv4 PXE boot option will not be created.
IPv4 HTTP Support	Enables / Disables IPv4 HTTP Boot Support. If disabled, Ipv4 HTTP boot option will not be created.
IPv6 PXE Support	Enables / Disables IPv6 PXE Boot Support. If disabled, Ipv4 PXE boot option will not be created.
IPv6 HTTP Support	Enables / Disables IPv6 HTTP Boot Support. If disabled, Ipv4 HTTP boot option will not be created.
PXE boot wait time	Assigns a period of time to press ESC key to abort the PXE boot.
Media detect count	Assigns a number of times to check the presence of media.

4.4.10 CSM Configuration



BIOS Setting	Description
CSM Support	Enables / Disables CSM support.
GateA20 Active	• **Upon Request** disables GA20 when using BIOS services. • **Always** cannot disable GA20, but is useful when any RT code is executed above 1 MB.
INT19 Trap Response	Sets how BIOS reacts on INT19 trap by Option ROM. • **Immediate** executes the trap right away. • **Postponed** executes the trap during legacy boot.
Boot option filter	Controls the priority of Legacy and UEFI ROMs.
Option ROM execution - Network	Controls the execution of UEFI and Legacy PXE Option ROM. Options: Do not launch/UEFI/ Legacy.

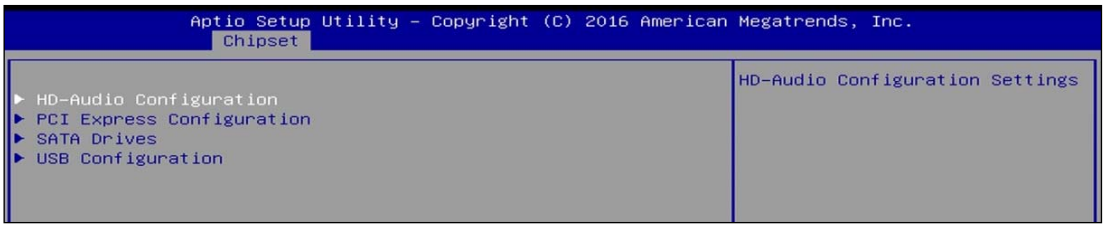
4.4.11 USB Configuration



BIOS Setting	Description
Legacy USB Support	• **Enabled** enables Legacy USB support. • **Auto** disables legacy support if there is no USB device connected. • **Disabled** keeps USB devices available only for EFI applications.
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Enables / Disables the support for USB mass storage driver.
USB Transfer time-out	The time-out value (1 / 5 10 / 20 secs) for Control, Bulk, and Interrupt transfers.
Device reset time-out	Gives seconds (10 / 20 / 30 / 40 secs) to delay execution of Start Unit command to USB mass storage device.
Device power-up delay	The maximum time the device will take before it properly reports itself to the Host Controller. **Auto** uses default value for a Root port it is 100ms. But for a Hub port, the delay is taken from Hub descriptor.

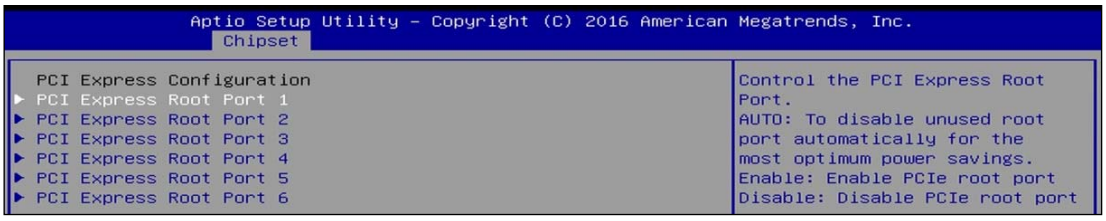
4.5 Chipset Settings (IB818F)

4.5.1 South Cluster Configuration

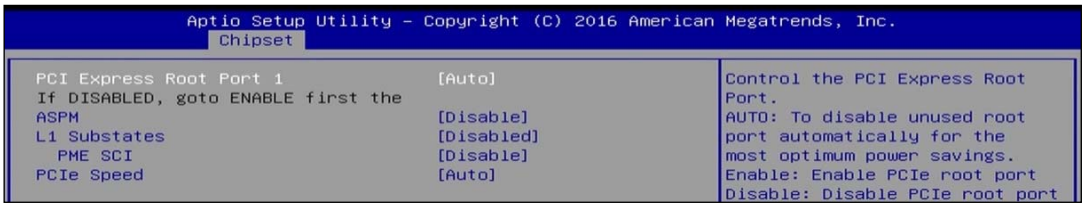


4.5.1.1 HD Audio Configuration

4.5.1.2 PCI Express Configuration



BIOS Setting	Description
PCI Express Root Port 1 ~ 6	Accesses the control of the PCI Express Root Port.

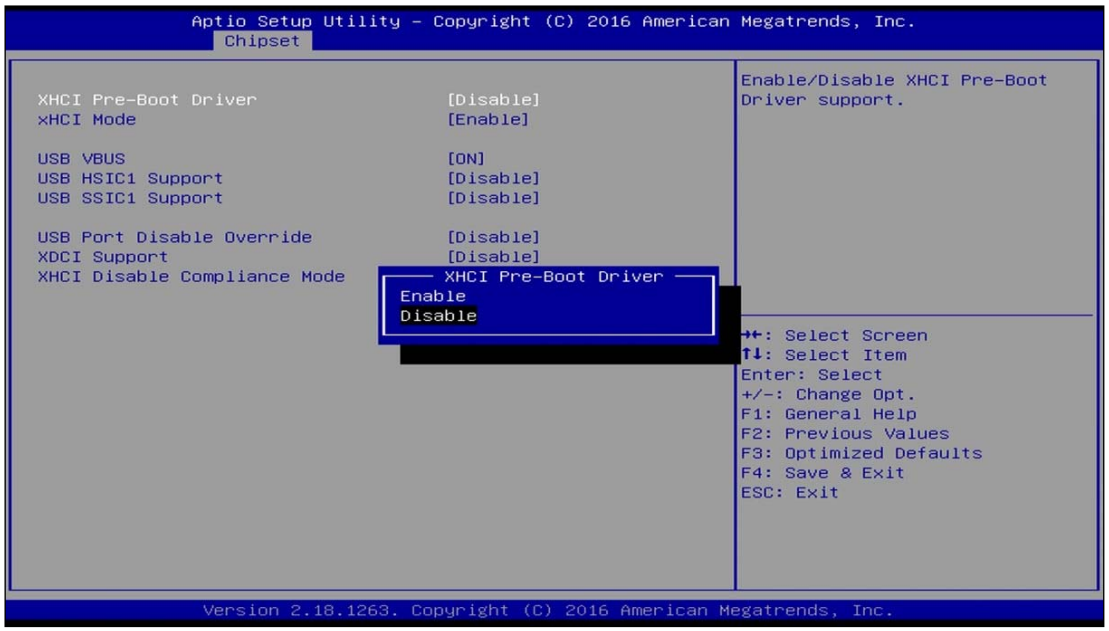


BIOS Setting	Description
PCI Express Root Port	Enables/ Disables the PCIe root port. **Auto:** To disable unused root port automatically for the most optimum power savings.
ASPM	Sets the PCIe active state power management. Options: Disable / L0s / L1 / L0SL1 / Auto
L1 Substates	Sets PCIe L1 substates. Options: Disables / L1.1 / L1.2 / L1.1 & L1.2
PME SCI	Enables / Disables PME SCI.
PCIe Speed	Configures the PCIe speed.

4.5.1.3 SATA Drivers

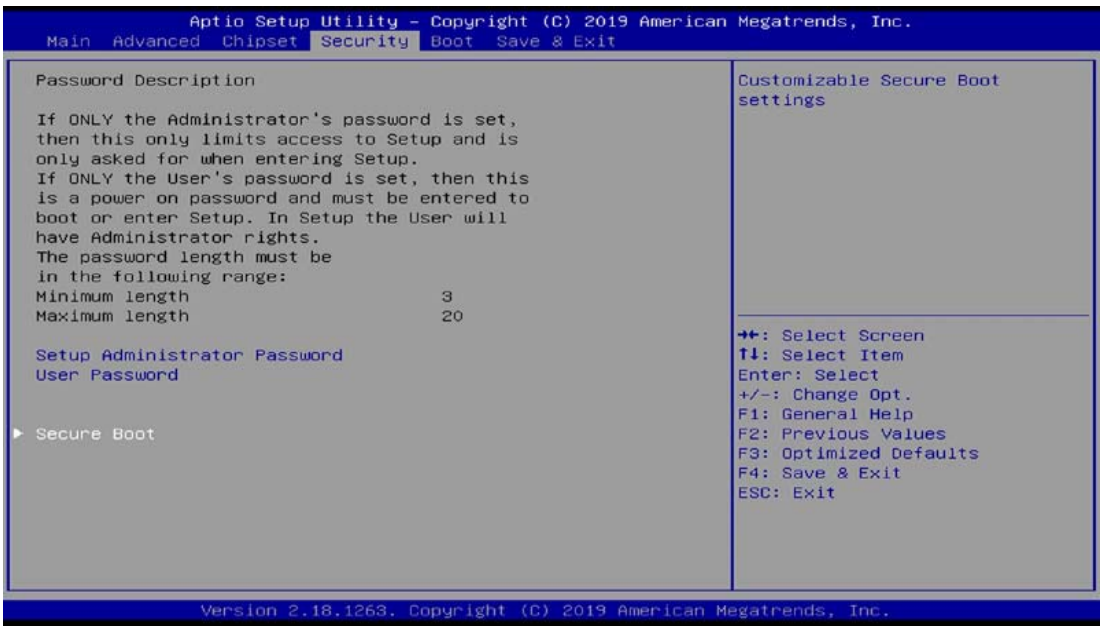
BIOS Setting	Description
Chipset SATA	Enables / Disables the Chipset SATA Controller. The Chipset SATA Controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port).
SATA Mode Selection	Determines how SATA controller(s) operate.

4.5.1.4 USB Configuration



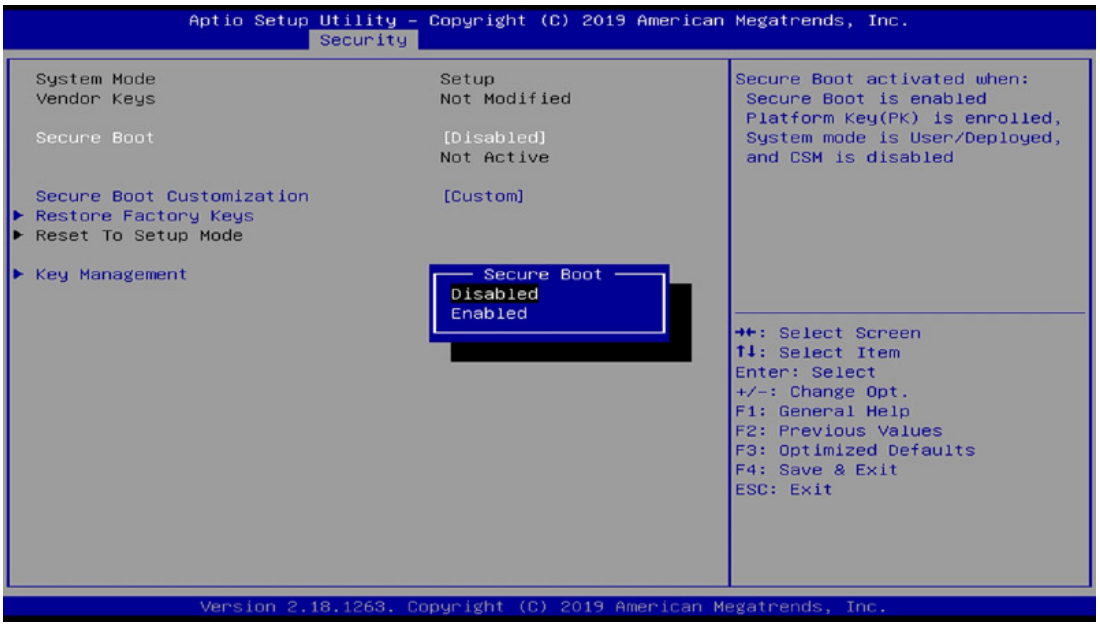
BIOS Setting	Description
XHCI Pre-Boot Driver	Enables / Disables the support for XHCI Pre-Boot Driver.
XHCI Mode	Enables / Disables XHCI mode. If disabled, XHCI controller would be disabled, and none of the USB devices are detectable or usable when systen is booted up in OS. Do NOT disable it unless for debug purpose.
USB VBUS	VBUS should be ON in HOST mode. It should be OFF in OTG device mode.
USB HSIC1 Support	Enables / Disables USB HSIC1.
USB SSIC1 Support	Enables / Disables USB SSIC1.
USB Port Disable Override	Selectively enables / disables the corresponding USB port from reporting a device connection to the controller.
XDCI Support	Enables / Disables XDCI.
XHCI Disable Compliance Mode	**FALSE** makes the XHCI Link Compliance Mode not disabled. **TRUE** disables the XHCI Link Compliance Mode.

4.6 Security Settings (IB818F)



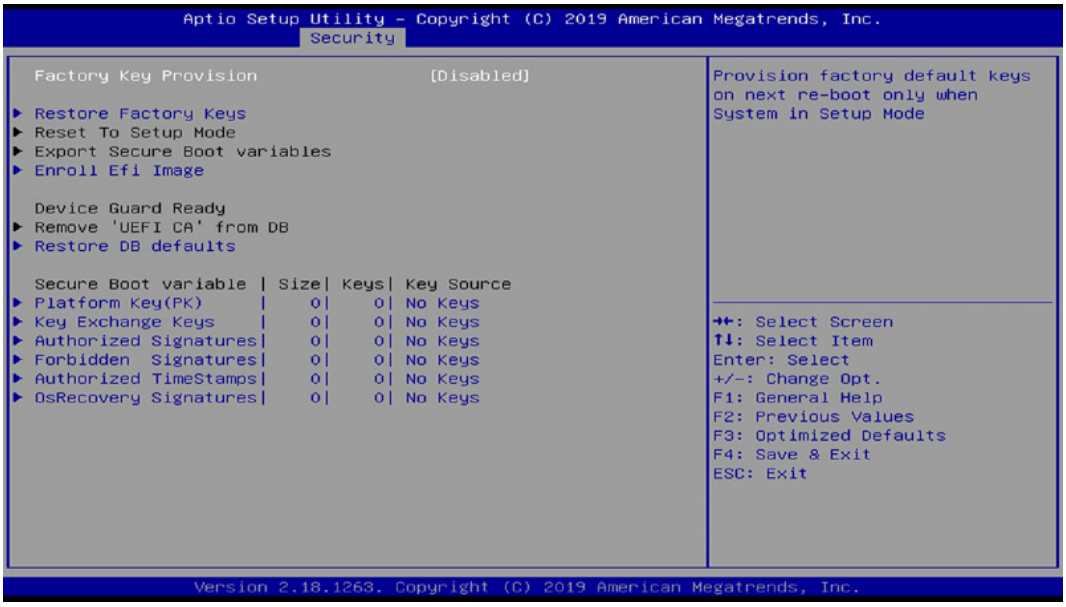
BIOS Setting	Description
Setup Administrator Password	Sets an administrator password for the setup utility.
User Password	Sets a user password.
Secure Boot	Customizable Secure Boot

4.6.1 Secure Boot



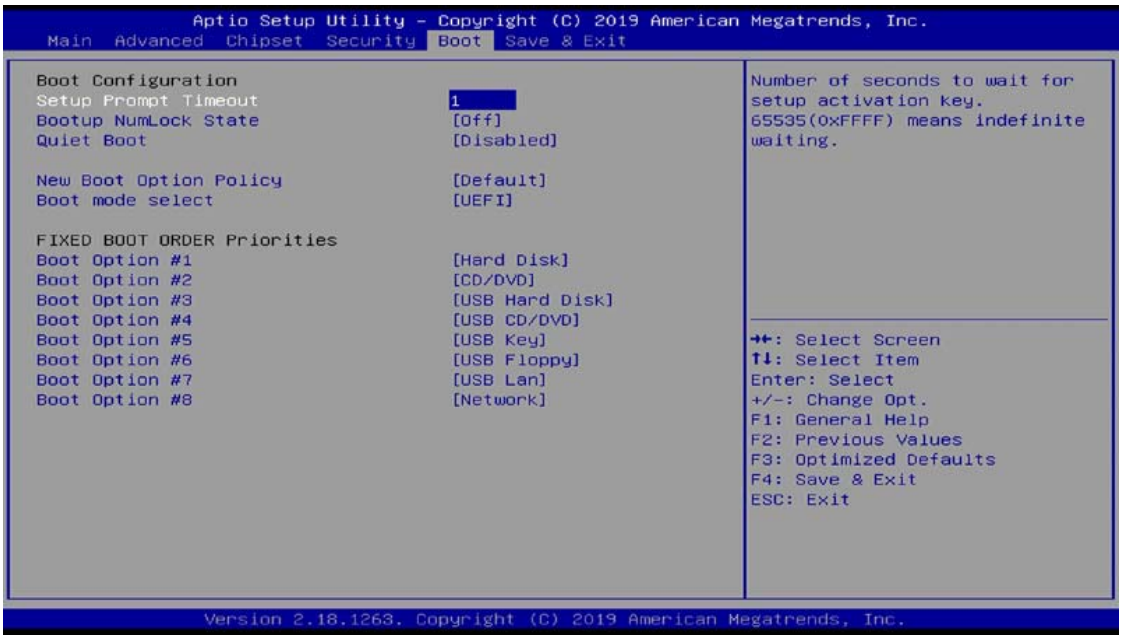
BIOS Setting	Description
Secure Boot	Secure activated when: secure boot is enable, Platform Key(PK) is enrolled, system mode is User/Deployed, and CSM is disabled.
Secure Boot Customization	Secure Boot Mode – Custom & Standard, Set UEFI Secure Boot Mode to STANDARD mode or CUSTOM mode, this change takes effect after save. And after reset, the mode will return to STANDARD mode.
Restore Factory Keys	Force System to User Mode. Configure NVRAM to contain OEM-defined factory default Secure Boot keys.
Key Management	Enables expert users to modify Secure Boot Policy variables without full authentication

4.6.2 Key Management



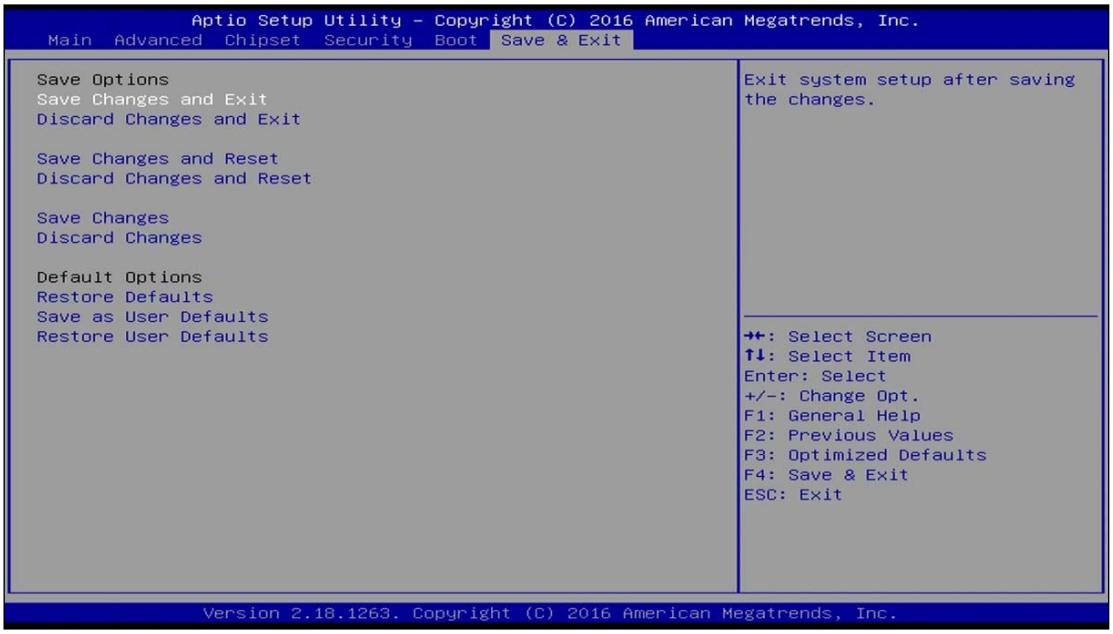
BIOS Setting	Description
Factory Key Provision	Provision factory default keys on next re-boot only when System in Setup Mode. Options available: Enabled/Disabled. Default setting is Disabled.
Restore Factory Keys	Force System to User Mode. Configure NVRAM to contain OEM-defined factory default Secure Boot keys.
Enroll Efi Image	Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authoried Signature database (db)
Restore DB defaults Efi Image	Restore DB variable to factory defaults
Platform Key (PK)	Displays the current status of the Platform Key (PK). Options available: Update
Key Exchange Keys	Displays the current status of the Key Exchange Key Database (KEK). Options available: Update/Append.
Authorized Signatures	Displays the current status of the Authorized Signature Database. Options available: Update /Append.
Forbidden Signatures	Displays the current status of the Forbidden Signature Database. Options available: Update /Append.
Authorized TimeStamps	Displays the current status of the Authorized TimeStamps Database. Options available: Update /Append.
OsRecovery Signatures	Displays the current status of the OsRecovery Signature Database. Options available: Update /Append.

4.7 Boot Settings (IB818F)



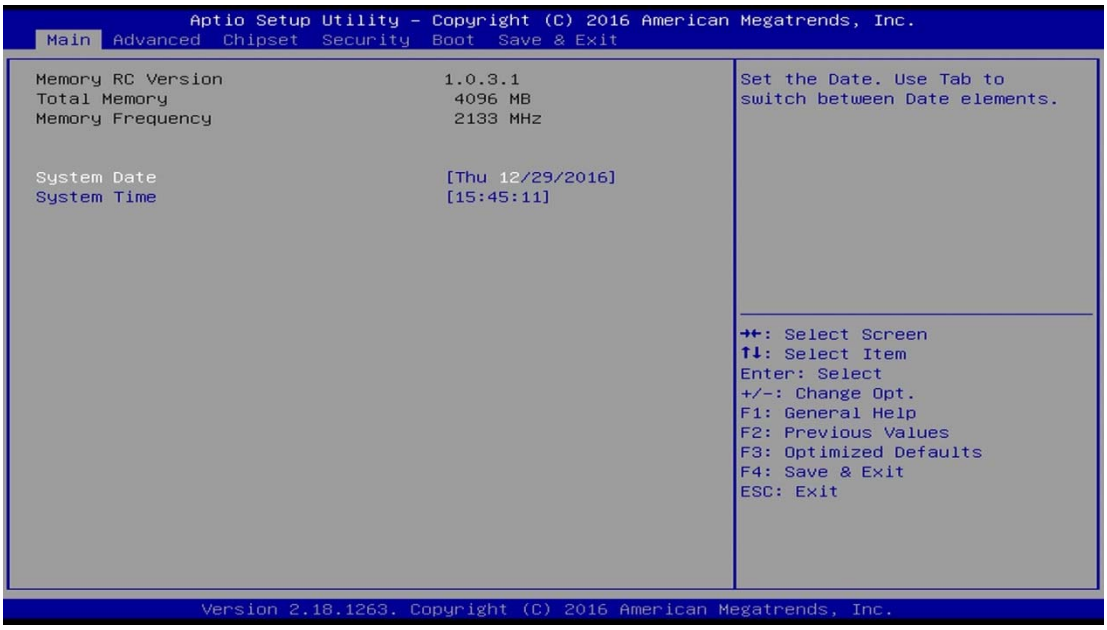
BIOS Setting	Description
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	Selects the keyboard NumLock state.
Quiet Boot	Enables / Disables Quiet Boot option.
New Boot Option Policy	Controls the placement of newly detected UEFI boot options. Options: Default, Place First, Place Last
Boot mode select	Selects a Boot mode, Legacy / UEFI / Dual.
Fixed Boot Order Priorities	Sets the system boot order priorities for hard disk, CD/DVD, USB hard disk, USB CD/DVD, USB Key, USB Floppy, USB Lan, Network.

4.8 Save & Exit Settings (IB818F)



BIOS Setting	Description
Save Changes and Exit	Exits system setup after saving the changes.
Discard Changes and Exit	Exits system setup without saving any changes.
Save Changes and Reset	Resets the system after saving the changes.
Discard Changes and Reset	Resets system setup without saving any changes.
Save Changes	Saves changes done so far to any of the setup options.
Discard Changes	Discards changes done so far to any of the setup options.
Restore Defaults	Restores / Loads defaults values for all the setup options.
Save as User Defaults	Saves the changes done so far as User Defaults.
Restore User Defaults	Restores the user defaults to all the setup options.

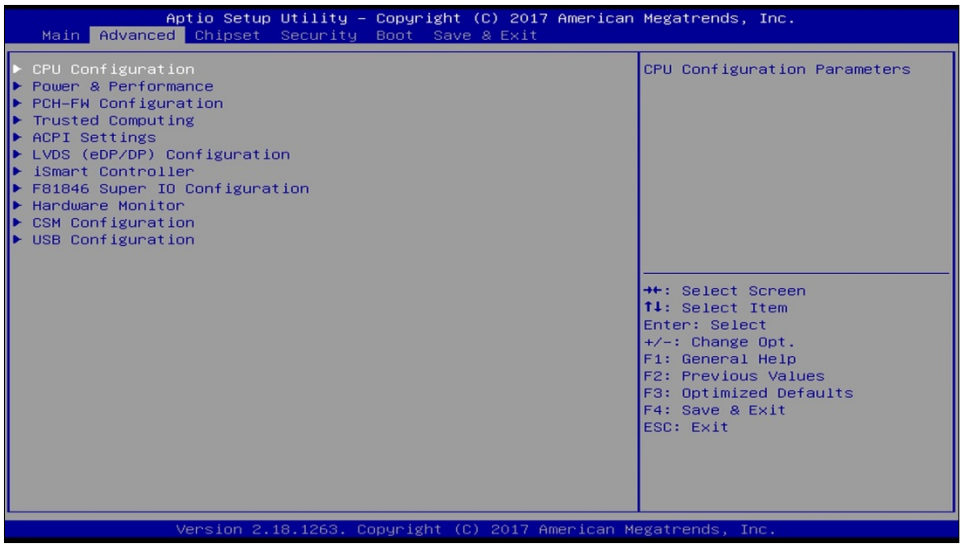
4.9 Main Settings (IB917)



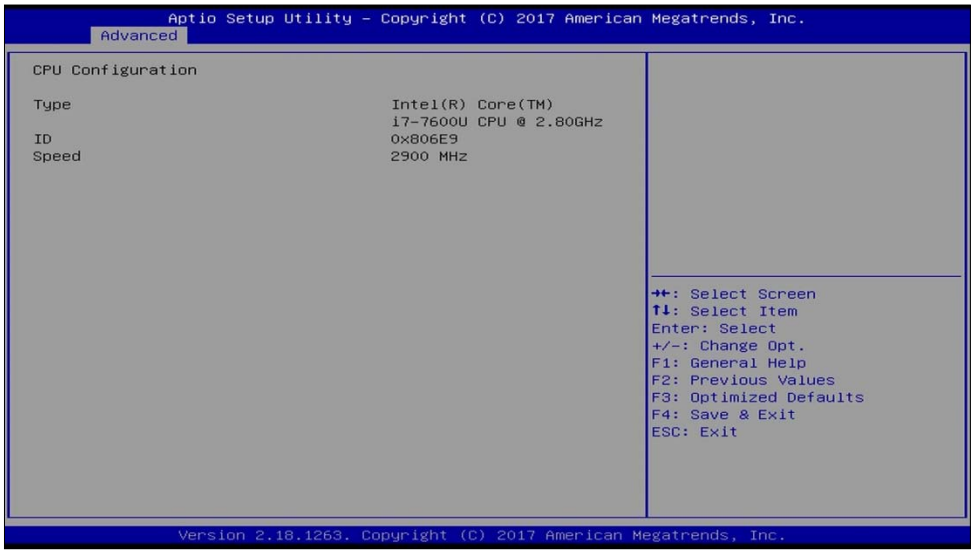
BIOS Setting	Description
System Date	Sets the date. Use the <Tab> key to switch between the data elements.
System Time	Set the time. Use the <Tab> key to switch between the data elements.

4.10 Advanced Settings (IB917)

This section allows you to configure, improve your system and allows you to set up some system features according to your preference.



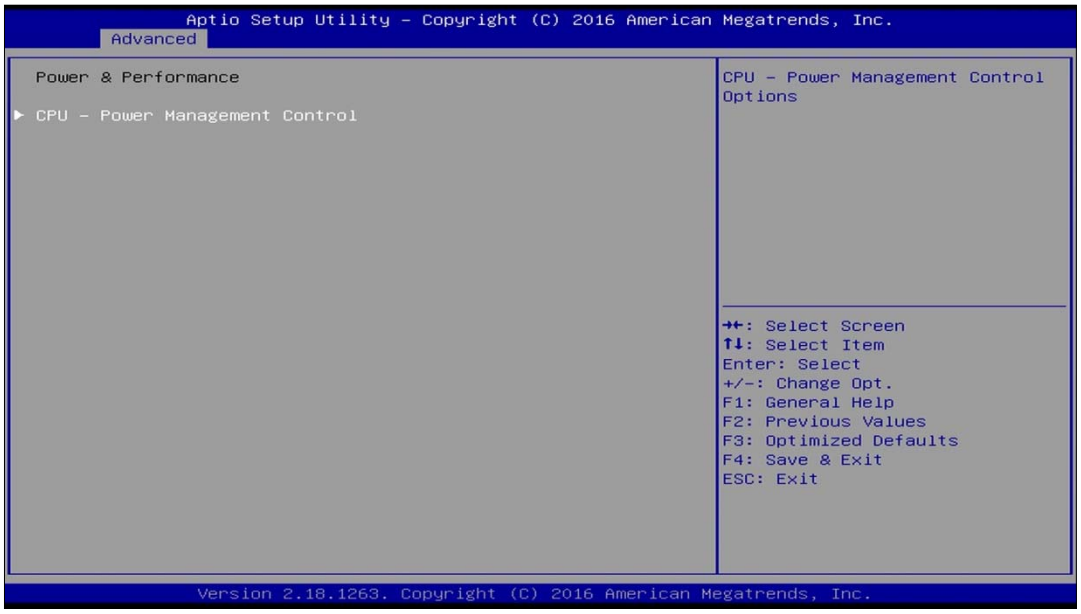
4.10.1 CPU Configuration

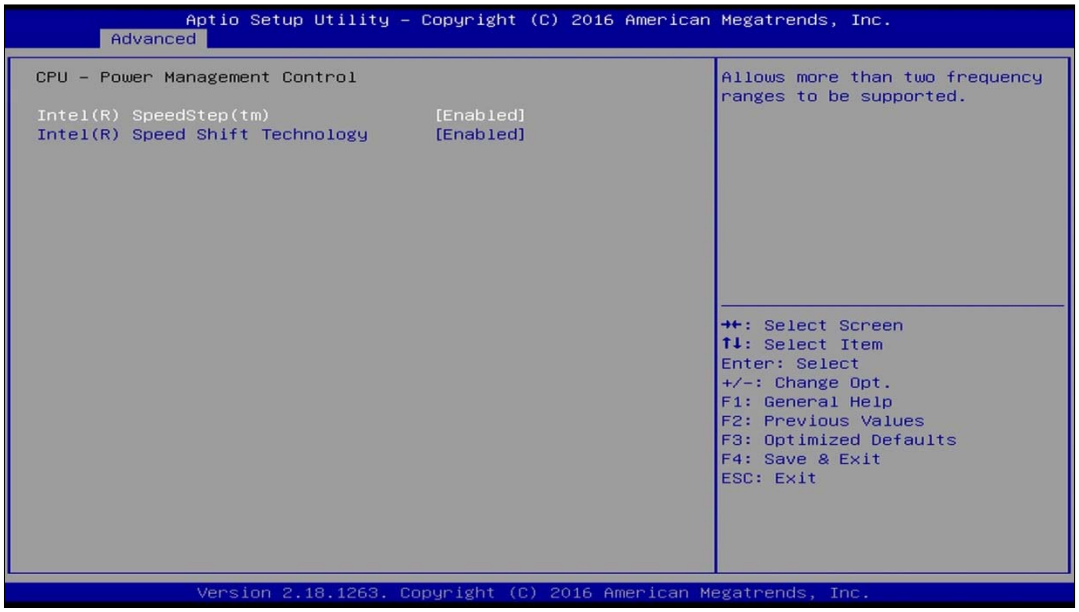


Displays the type, ID and speed of the CPU.

Note: The CPU information displayed varies upon your actual CPU type.

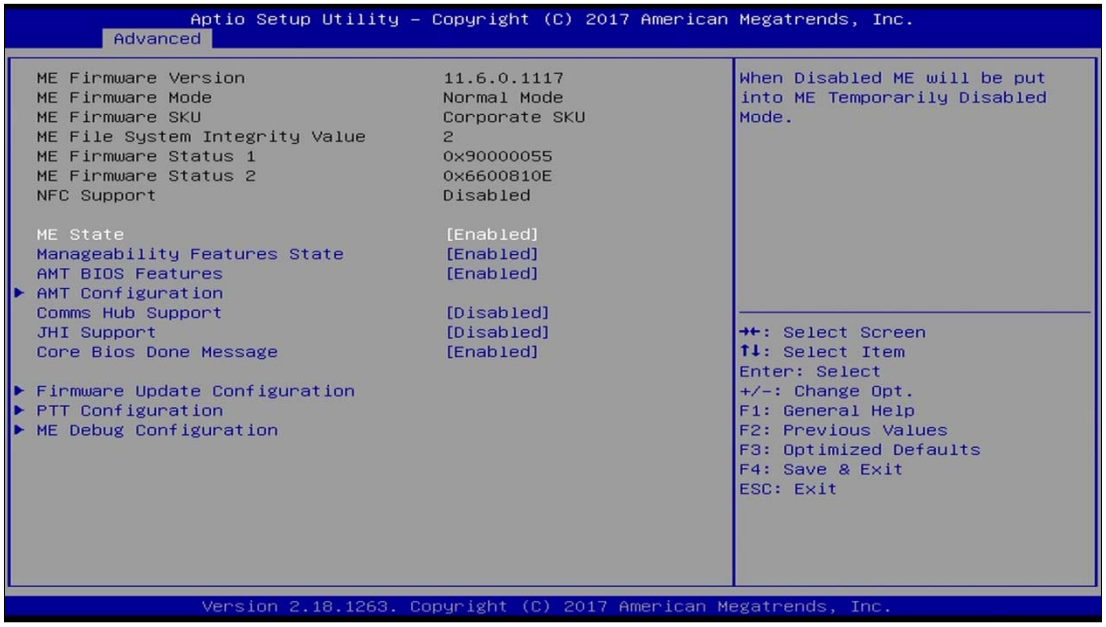
4.10.2 Power & Performance





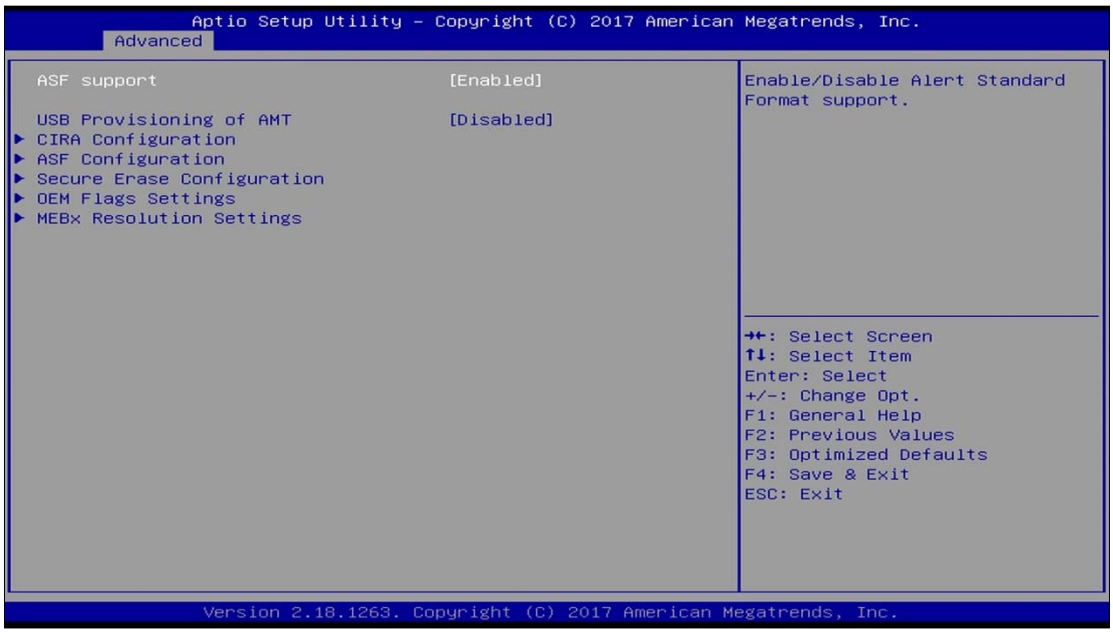
BIOS Setting	Description
Intel(R) SpeedStep(tm)	Allows more than two frequency ranges to be supported.
Intel(R) Speed Shift Technology	Enables / Disables Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.

4.10.3 PCH-FW Configuration



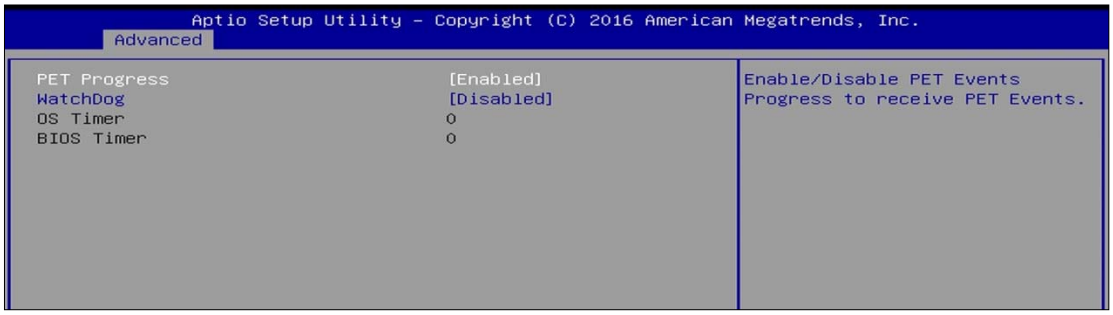
BIOS Setting	Description
ME State	When disabled ME will be put into ME Temporarily Disabled Mode.
Manageability Features State	Enables / Disables Intel(R) manageability features in FW. To disable support platform must be in an unprovisioned state first.
AMT BIOS Features	When disabled AMT BIOS features are no longer supported and user is no longer able to access MEBx Setup. **Note:** This option does not disable manageability features in FW.
AMT Configuration	Configures Intel(R) Active Management Technology Parameters.
Comms Hub Support	Enables / Disables support for Comms Hub.
JHI Support	Enables / Disables Intel(R) DAL Host Interface Service (JHI).
Core BIOS Done Message	Enables / Disables Core BIOS done message sent to ME.
Firmware Update Configuration	Configures Management Engine Technology parameters.
PTT Configuration	Configures PTT capability or state.
ME Debug Configuration	Configures ME debug options. **Note:** This menu is provided for testing puropses. It is recommended to leave the options in their default states.

4.10.3.1 AMT Configuration



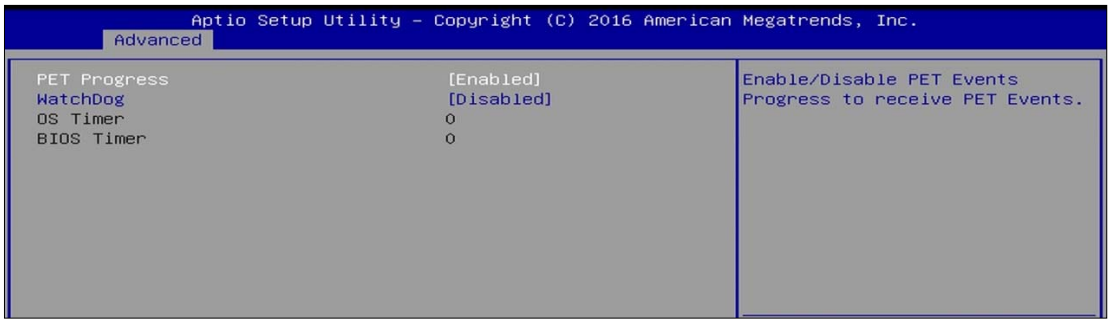
BIOS Setting	Description
ASF Support	Enables / Disables Alert Standard Format support.
USB Provisioning of AMT	Enables / Disables of AMT USB provisioning.
CIRA Configuration	Configures remote assistance process parameters.
ASF Configuration	Configures Alert Standard Format parameters.
Secure Erase Configutation	Secures erase configuration menu.
OEM Flags Settings	Configures OEM Flags.
MEBx Resolution Settings	Shows resolution settings for MEBx display modes.

CIRA Configuration



BIOS Setting	Description
Activate Remote Assistance Process	Trigger CIRA boot. **Note:** Network Access must be activated first from MEBx Setup.

ASF Configuration

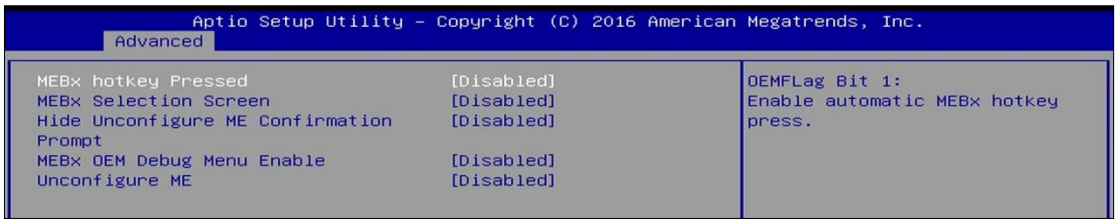


BIOS Setting	Description
PET Progress	Enables / Disables PET events progress to receive PET events.
WatchDog	Enables / Disables the watchdog timer.

Secure Erase Configuration:

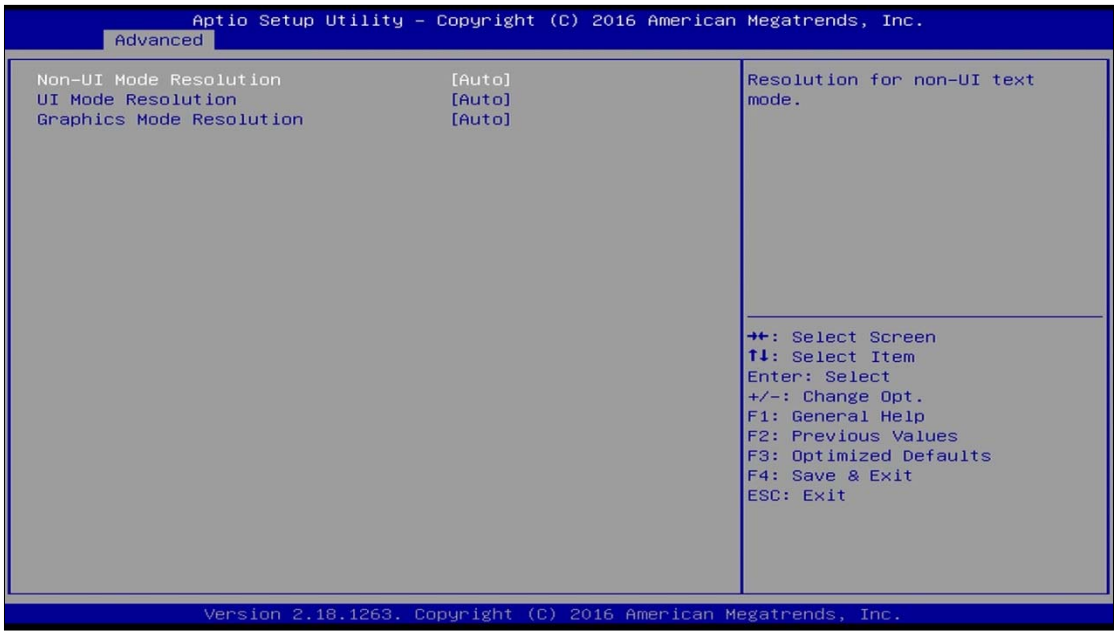
BIOS Setting	Description
Secure Erase Mode	Changes Secure Erase module behavior. • **Simulated** performs SE flow without erasing SSD. • **Real** erases SSD.
Force Secure Erase	Force Secure Erase on next boot.

OEM Flags Settings:



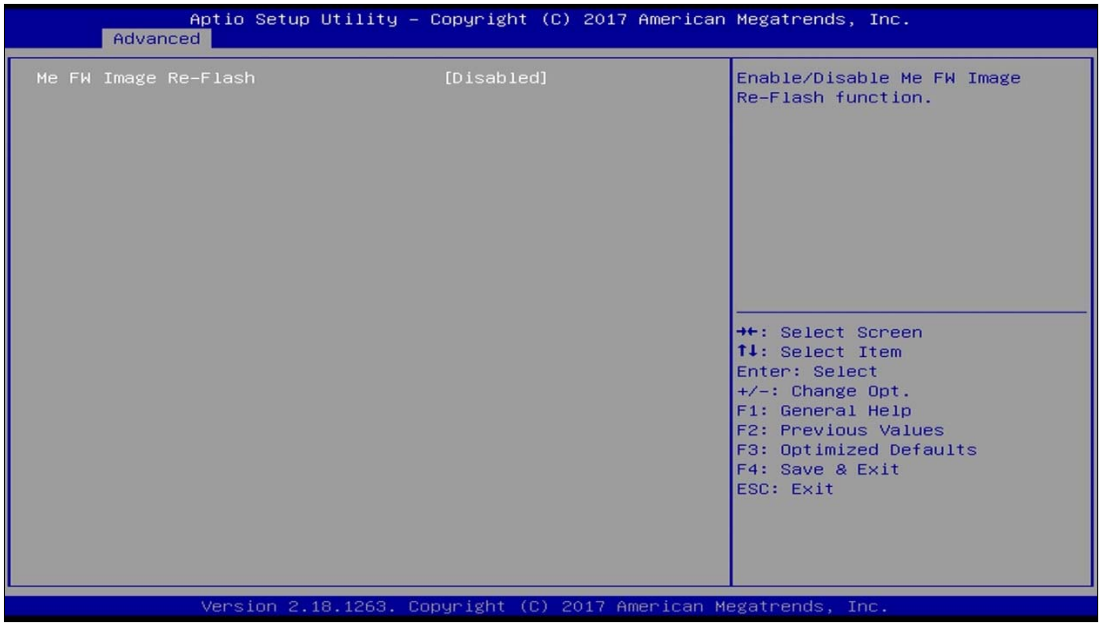
BIOS Setting	Description
MEBx hotkey Pressed	OEMFlag Bit 1: enables automatic MEBx hotkey press.
MEBx Selection Screen	OEMFlag Bit 2: enables MEBx selection screen with 2 options. • Press **1** to enter ME configuration screens. • Press **2** to initiate a remote connection. **Note:** Network access must be activated from MEBx Setup for this screen to be displayed.
Hide Unconfigure ME Confirmation Prompt	OEMFlag Bit 6: hides the unconfigure ME confirmation prompt when attempting ME unconfiguration.
MEBx OEM Debug Menu Enable	OEMFlag Bit 14: enables OEM debug menu in MEBx.
Unconfigure ME	OEMFlag Bit 15: Unconfigures ME with resetting MEBx password to default.

MEBx Resolution Settings:



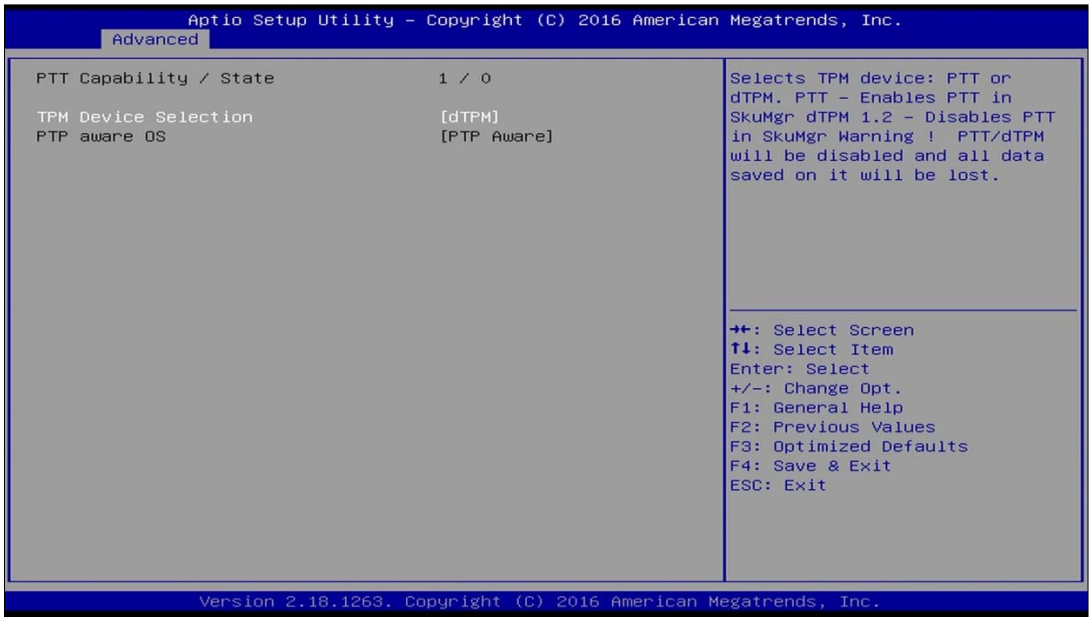
BIOS Setting	Description
Non-UI Mode Resloution	Sets resolution fro non-UI text mode.
UI Mode Resolution	Sets resolution for UI text mode.
Graphics Mode Resolution	Sets resolution for graphics mode.

4.10.3.2 Firmware Update Configuration



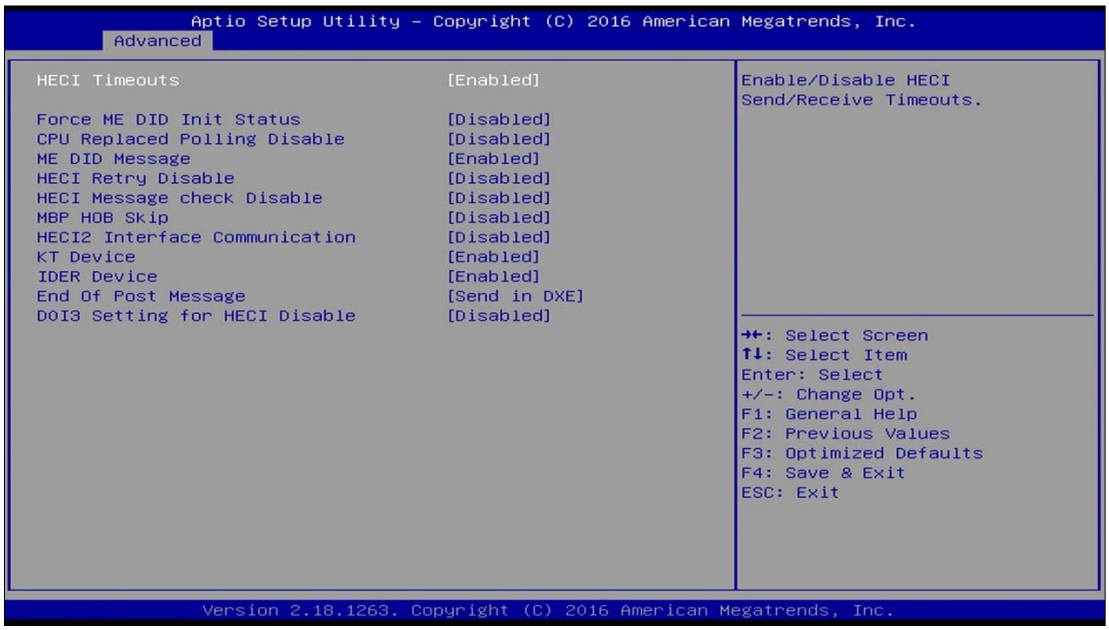
BIOS Setting	Description
ME FW Image RE-Flash	Enables / Disables ME FW Image Re-Flash function.

4.10.3.3 PTT Configuration



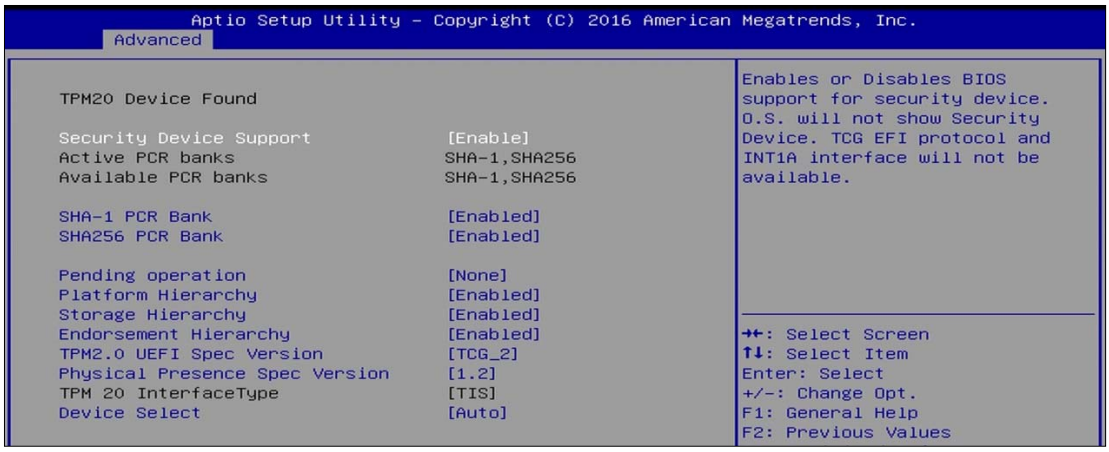
BIOS Setting	Description
TPM Device Selection	Selects TPM device: PTT or dTPM. • **PTT** enables PTT in SkuMgr. • **dTPM 1.2** disables PTT in SkuMgr warning. PTT/dTPM will be disabled and all data saved on it will be lost.

4.10.3.4 ME Debug Configuration



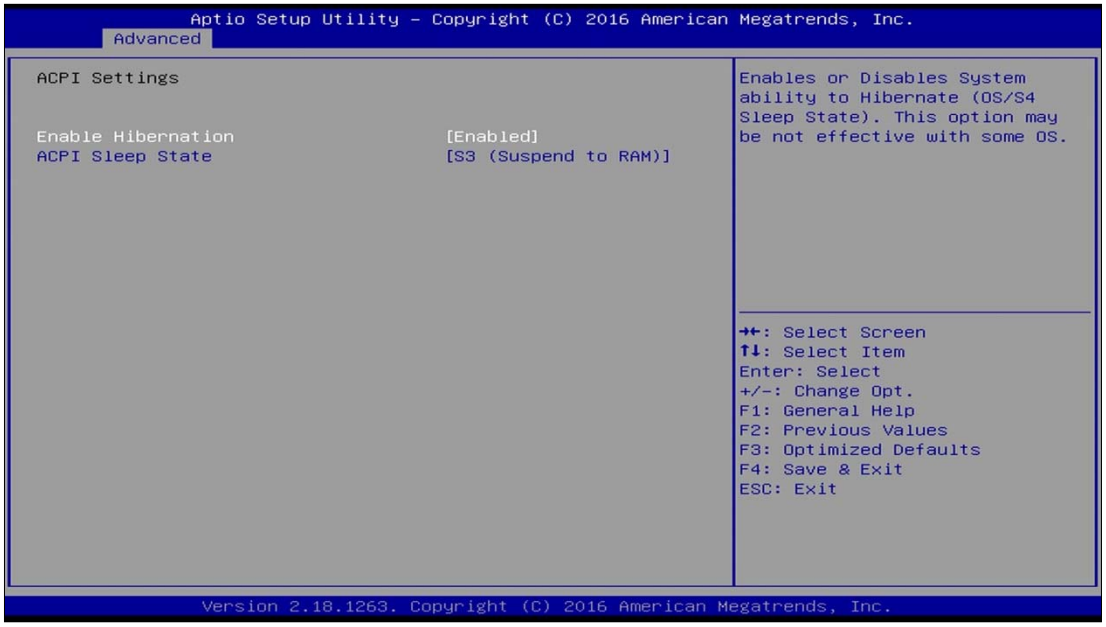
BIOS Setting	Description
HECI Timeouts	Enables / Disables HECI sending/receiving timeouts.
Force ME DID Init Status	Forces the DID initialization status value.
CPU Replaced Polling Disable	Disables CPU replacement polling loop.
ME DID Message	Enables / Disables ME DID message (disable will prevent the DID message from being sent).
HECI Retry Disable	Setting this option disables retry mechanism for all HECI APIs.
HECI Message Check Disable	Disables message check for BIOS boot path when sending messages.
MBP HDB Skip	Enables / Disables skip of MBP HDB.
HECI2 Interface Communicationn	Adds / Removes HECI2 device from PCI space.
KT Device	Enables / Disables KT device.
IDER Device	Enables / Disables IDER device.
End of Post Message	Enables / Disables end of Post message sent to ME.
DOI3 Setting for HECI Disable	Disables setting DOI3 bit for all HECI devices.

4.10.4 Trusted Computing



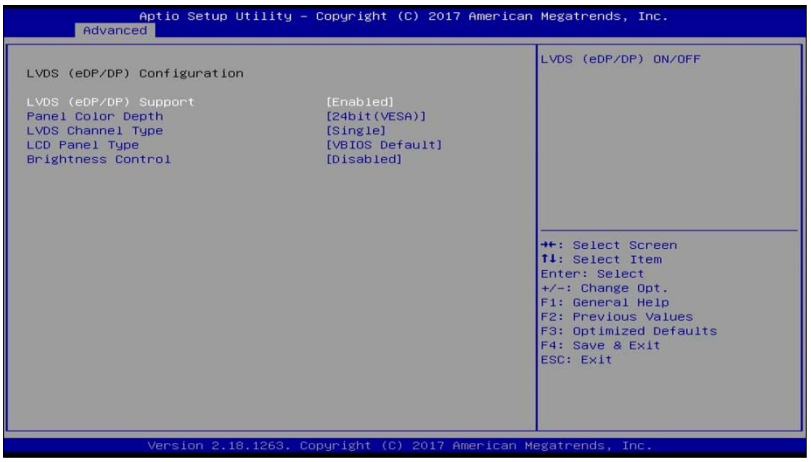
BIOS Setting	Description
Security Device Support	Enables / Disables BIOS support for security device. OS will not show security device. TCG EFI protocol and INTIA interface will not be available.
SHA-1 PCR Bank	Enables / Disables SHA-1 PCR Bank.
SHA256 PCR Bank	Enables / Disables SHA256 PCR Bank.
Pending operation	Schedule an operation for the security device. Note: Your computer will reboot during restart in order to change state of security device.
Platform Hierarchy	Enables / Disables platform hierarchy.
Storage Hierarchy	Enables / Disables storage hierarchy.
Endorsement Hierarchy	Enables / Disables endorsement hierarchy.
TPM2.0 UEFI Spec Version	Selects the supported TCG version based o your OS. • **TCG_1_2:** supports Windows 8 /10. • **TCG_2:** supports new TCG2 protocol and event format for Windows 10 or later.
Physical Presence Spec Version	Selects to show the PPI Spec Version (1.2 or 1.3) that the OS supports. **Note:** Some HCK tests might not support 1.3.
Device Select	• **TPM 1.2** will restrict support to TPM 1.2 devices only. • **TPM 2.0** will restrict support to TPM 2.0 devices only. • **Auto** will support both with the default being set to TPM 2.0 deices if not found, and TPM 1.2 device will be enumerated.

4.10.5 ACPI Settings



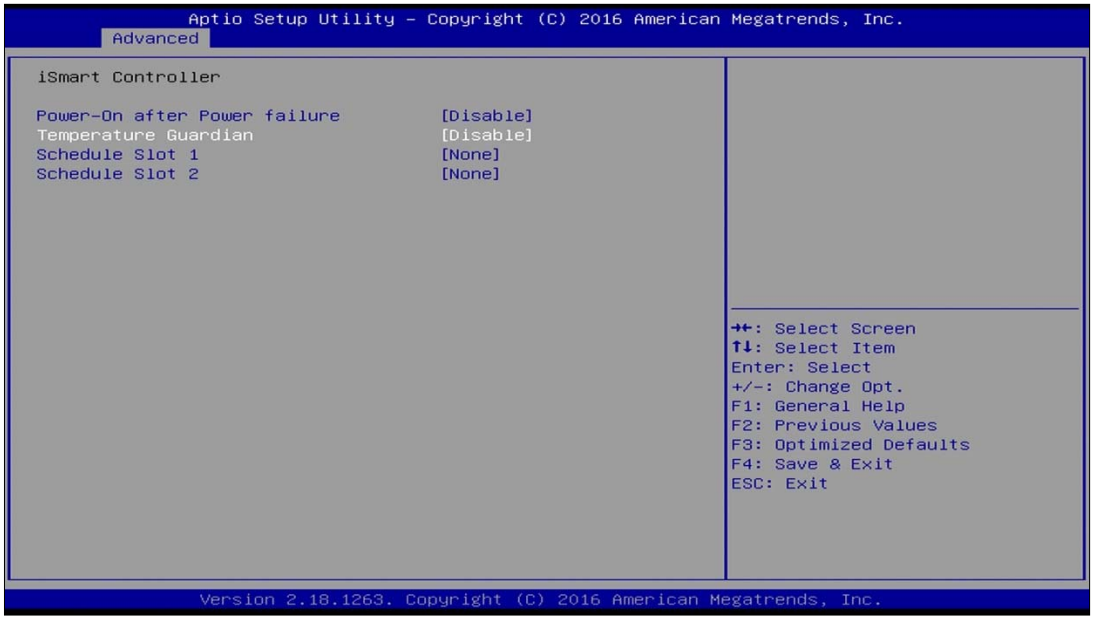
BIOS Setting	Description
Enable Hibernation	Enables / Disables the system ability to hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Selects an ACPI sleep state (Suspend Disabled or S3) where the system will enter when the Suspend button is pressed.

4.10.6 LVDS (eDP/DP) Configuration



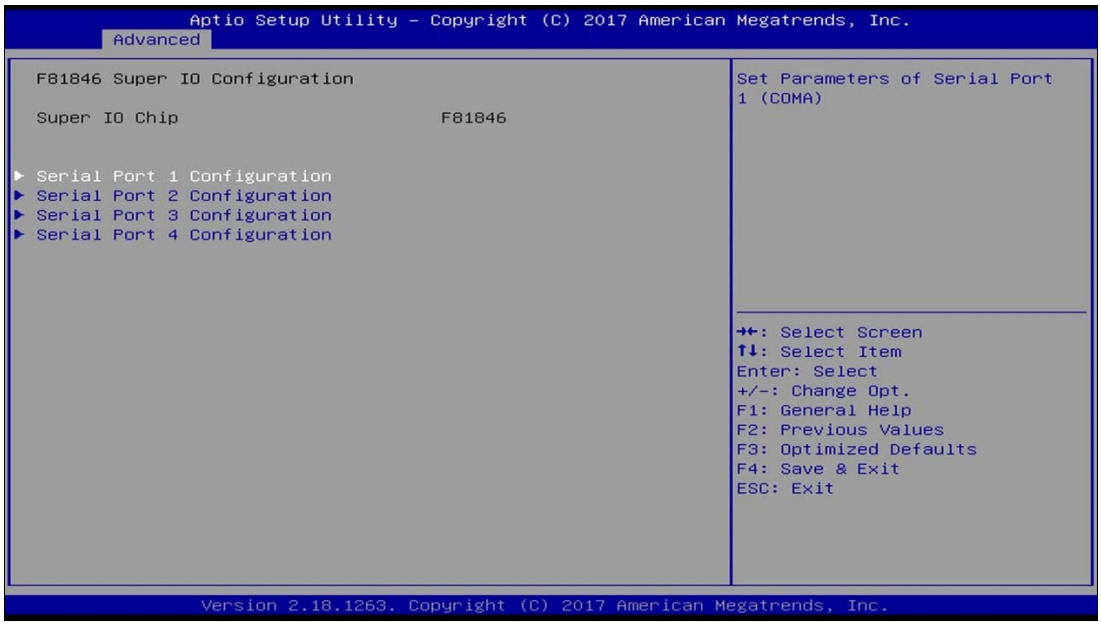
BIOS Setting	Description
LVDS (eDP/DP) Support	Enables / Disables LVDS (eDP/DP).
Panel Color Depth	Selects the panel collor depth. Options: 18 bit, 24 Bit (VESA), 24 bit (JEIDA)
LVDS Channel Type	Chooses the LVDS as single or dual channel.
LCD Panel Type	Selects LCD panel used by Intel Graphics Device by selecting the appropriate setup item. Resolution Options: VBIOS Default, 640 x 480, 800 x 600, 1024 x 768, 1280 x 1024, 1400 x 1050, 1366 x 768, 1600 x 1200, 1680 x 1050, 1920 x 1200, 1440 x 900, 1600 x 900, 1280 x 800, 1920 x 1080, 2048 x 1536
Brightness Control	Enables / Disables the brightness control.

4.10.7 iSMART Controller



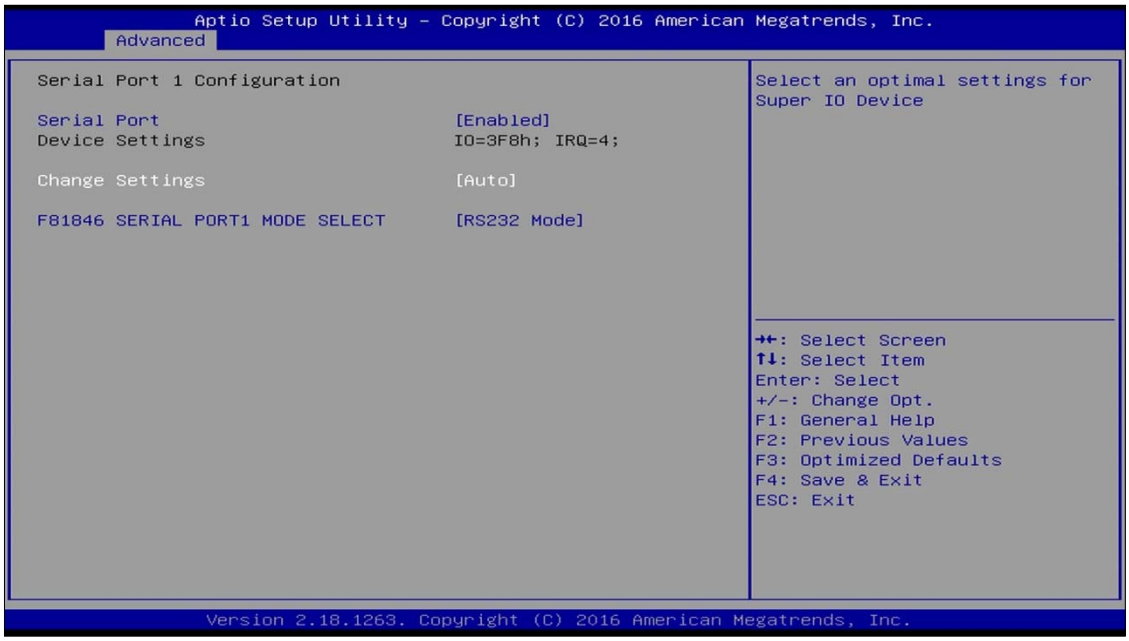
BIOS Setting	Description
Power-On after Power failure	Enables / Disables the system to be turned on automatically after a power failure.
Temperature Guardian	Generate the reset signal when system hands up on POST.
Schedule Slots	Sets up the hour / minute / day for the power-on schedule for the system. Options: • None • Power On • Power On / Off

4.10.8 F81846 Super IO Configuration



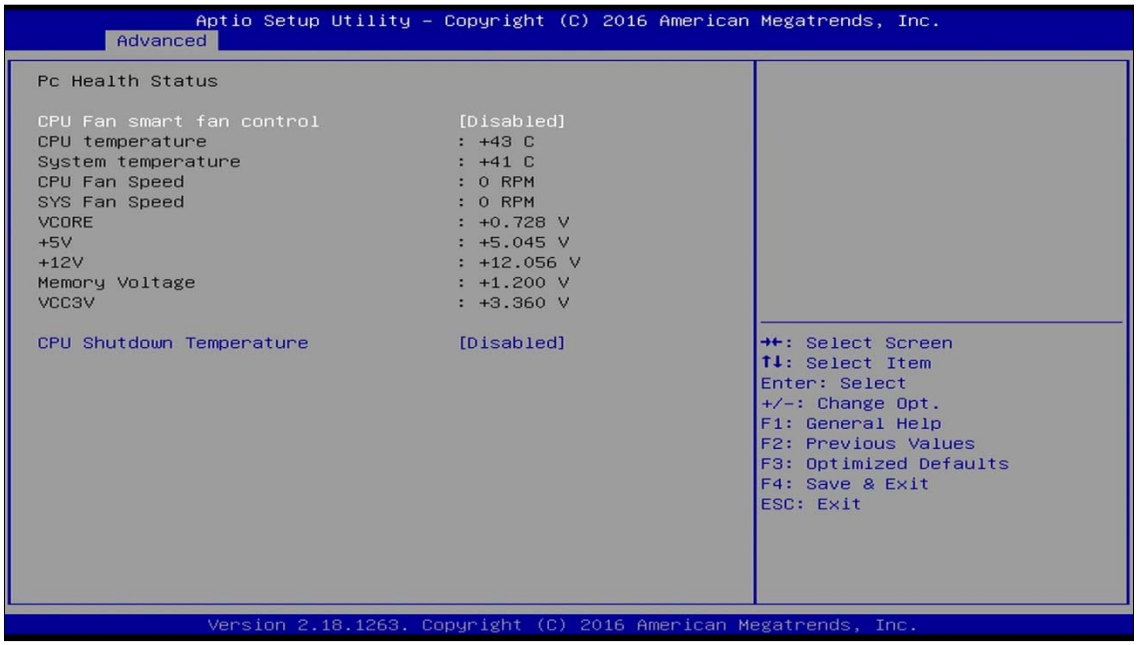
BIOS Setting	Description
Serial Ports Configuration	Sets parameters of serial ports. Enables / Disables the serial port and select an optimal setting for the Super IO device.

4.10.8.1 Serial Port 1 Configuration



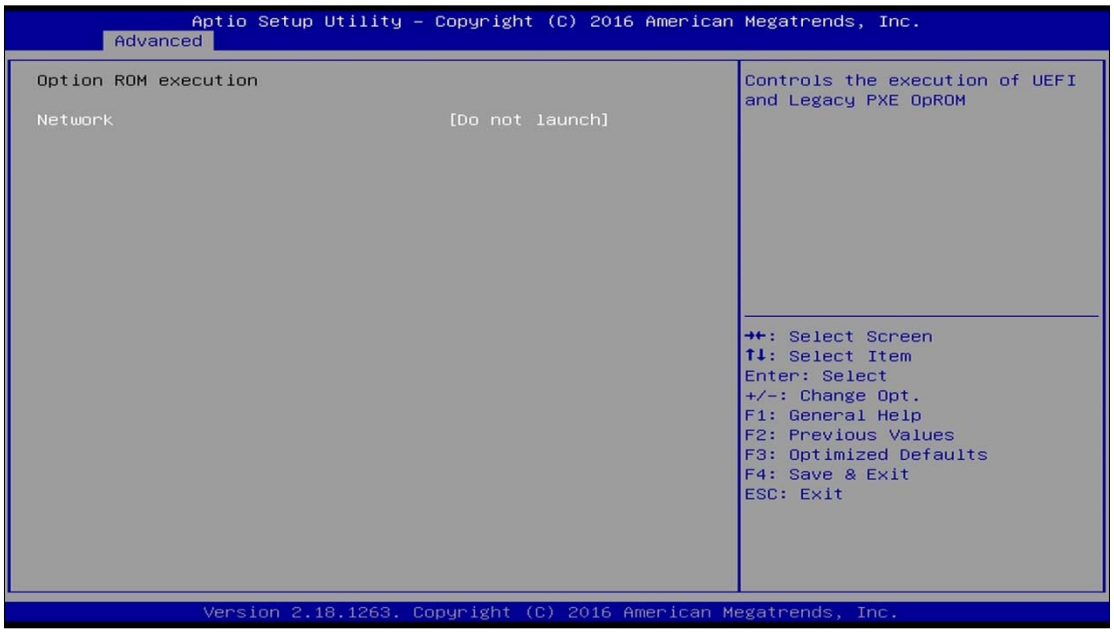
BIOS Setting	Description
Serial Port	Enables / Disables the serial port.
Change Settings	Selects an optimal settings for Super I/O device. Options: • Auto • IO = 3F8h; IRQ = 4 • IO = 3F8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2F8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 3E8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2E8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12
F81846 Serial Port 1 Mode Select	Changes the serial port mode to RS-232 / 422 / 485.

4.10.9 Hardware Monitor



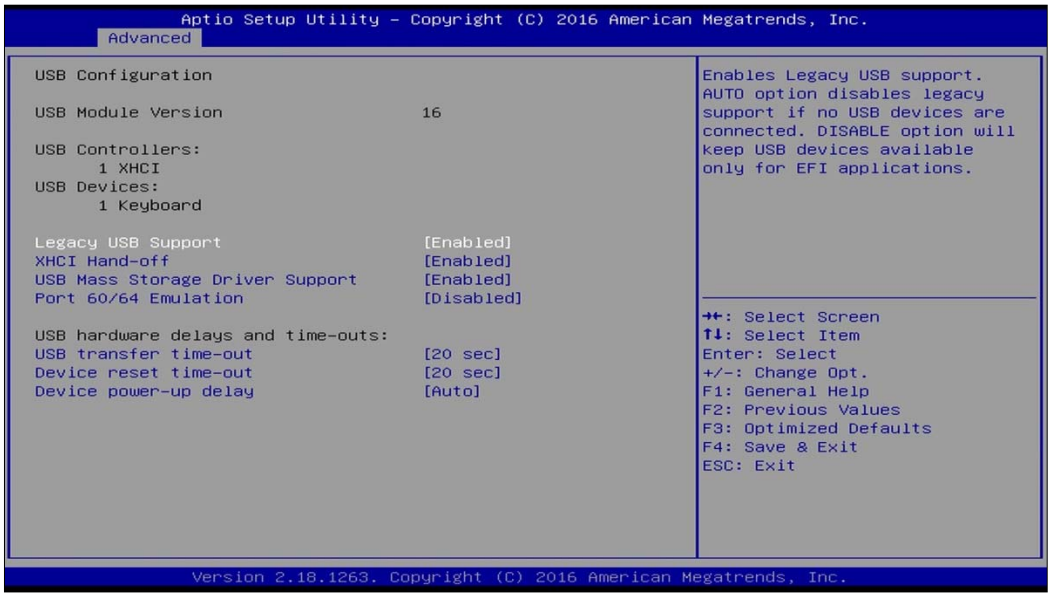
BIOS Setting	Description
CPU Fan smart fan control	Enables / Disables smart fan control.
Temperatures / Voltages	These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.
CPU Shutdown Temperature	Sets a threshold of temperature to shut down if CPU goes overheated. Options: Disabled / 70 °C / 75 °C / 80 °C / 85 °C / 90 °C / 95 °C

4.10.10 CSM Configuration



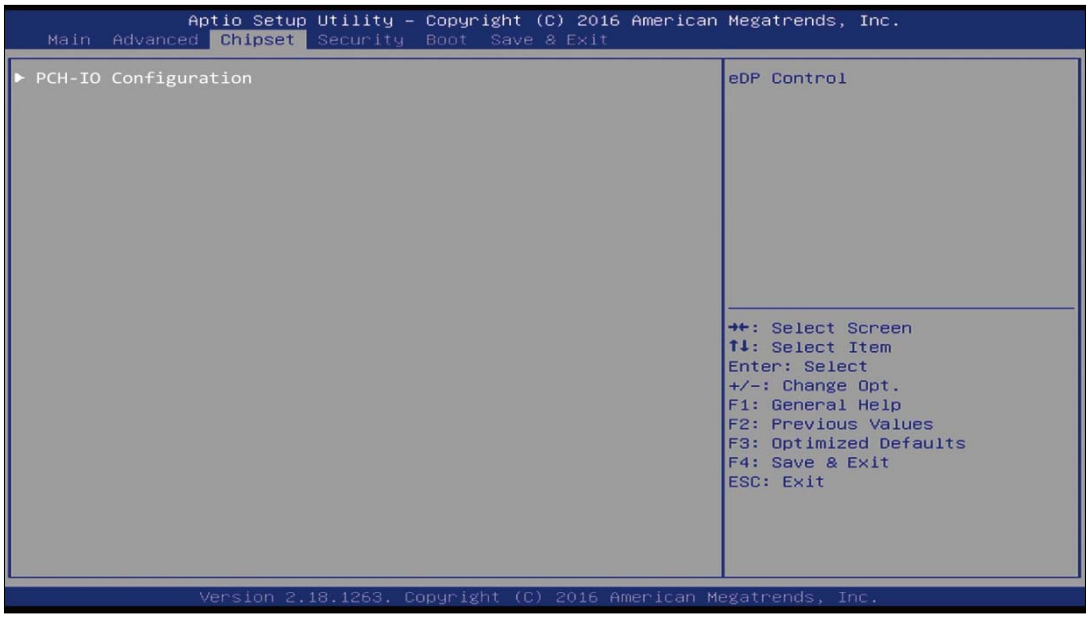
BIOS Setting	Description
Network	Controls the execution of UEFI and Legacy PXE OpROM.

4.10.11 USB Configuration

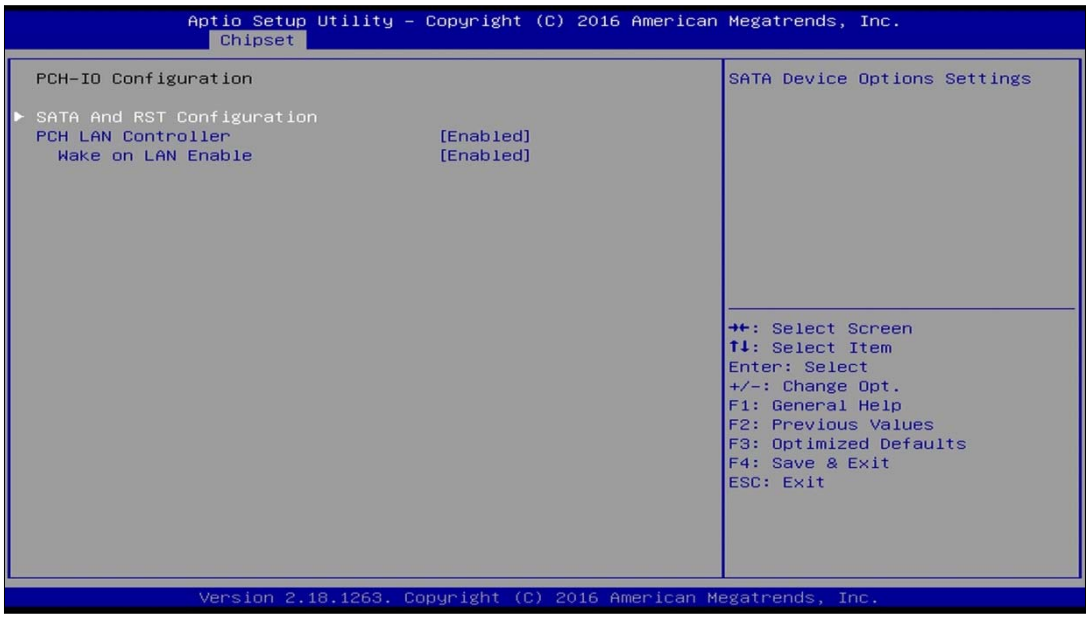


BIOS Setting	Description
Legacy USB Support	• **Enabled** enables Legacy USB support. • **Auto** disables legacy support if there is no USB device connected. • **Disabled** keeps USB devices available only for EFI applications.
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Enables / Disables the support for USB mass storage driver.
Port 60/64 Emulation	Enables / Disables the support for I/O port 60h / 64h emulation. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.
USB Transfer time-out	The time-out value (1 / 5 10 / 20 secs) for Control, Bulk, and Interrupt transfers.
Device reset time-out	Gives seconds (10 / 20 / 30 / 40 secs) to delay execution of Start Unit command to USB mass storage device.
Device power-up delay	The maximum time the device will take before it properly reports itself to the Host Controller. **Auto** uses default value for a Root port it is 100ms. But for a Hub port, the delay is taken from Hub descriptor.

4.11 Chipset Settings (IB917)

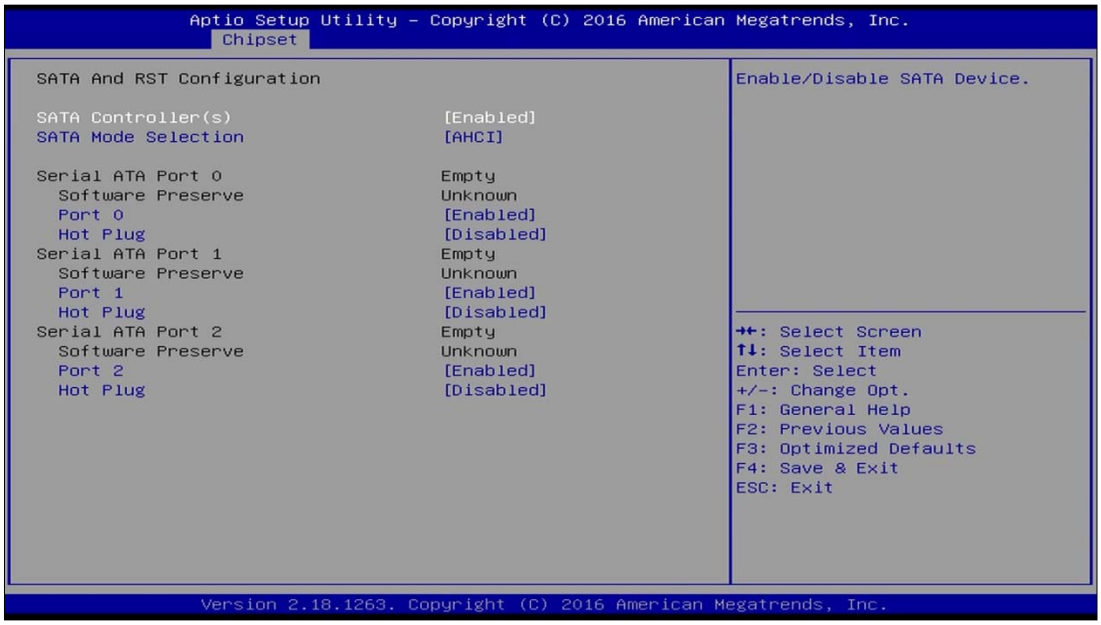


4.11.1 PCH-IO Configuration



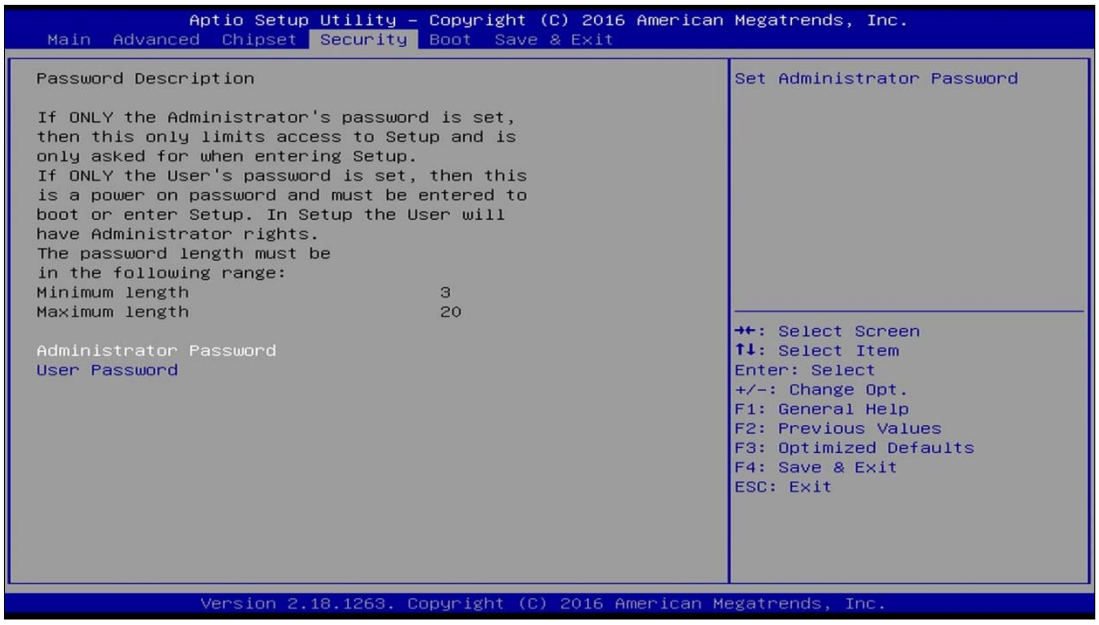
BIOS Setting	Description
SATA and RST Configuration	SATA device options and settings
PCH LAN Controller	Enables / Disables onboard NIC.
Wake on LAN Enable	Enables / Disables integrated LAN to wake the system.

4.11.1.1 SATA and RST Configuration:



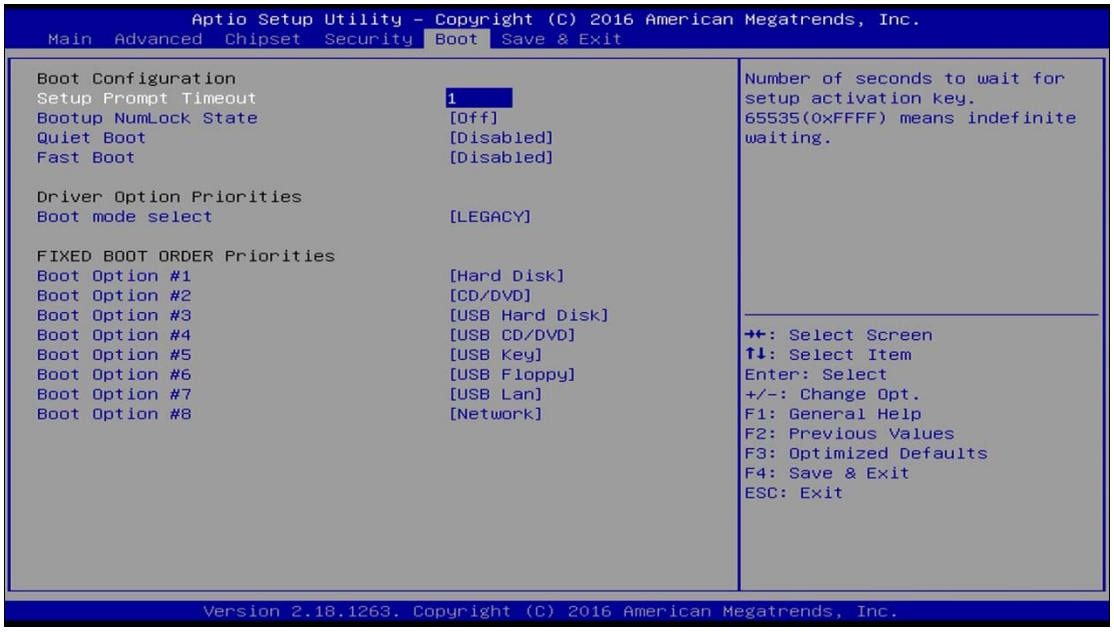
BIOS Setting	Description
SATA Controller(s)	Enables / Disables the Serial ATA.
SATA Mode Selection	Selects IDE or AHCI Mode.
Serial ATA Port 0~2	Enables / Disables Serial Port 0 ~ 2.
SATA Ports Hot Plug	Enables / Disables SATA Ports HotPlug.

4.12 Security Settings (IB917)



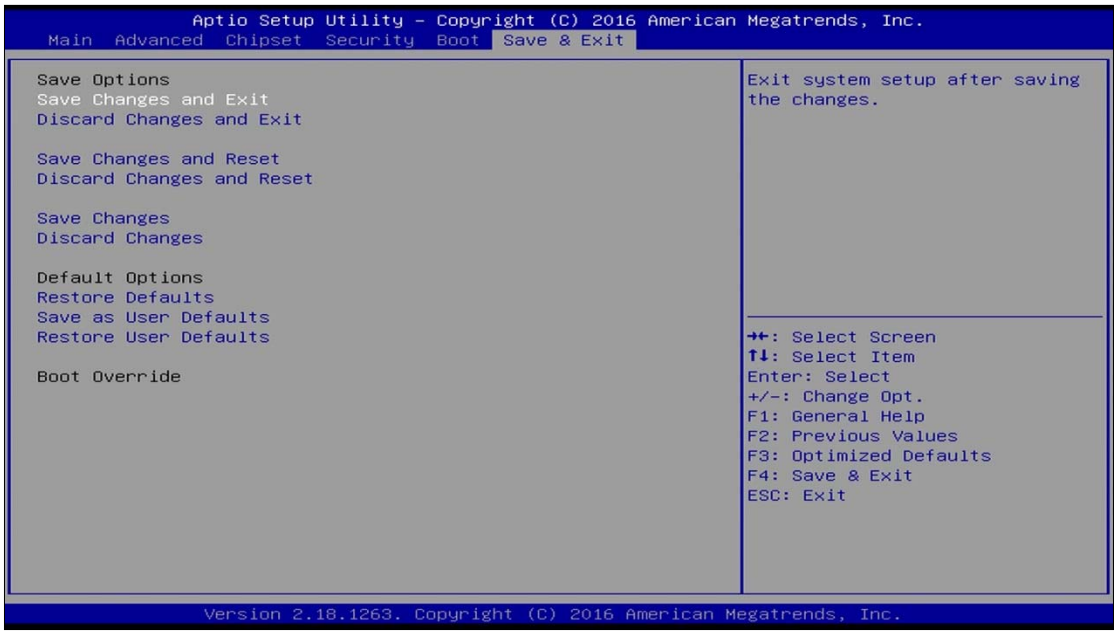
BIOS Setting	Description
Setup Administrator Password	Sets an administrator password for the setup utility.
User Password	Sets a user password.

4.13 Boot Settings (IB917)



BIOS Setting	Description
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	Selects the keyboard NumLock state.
Quiet Boot	Enables / Disables Quiet Boot option.
Fast Boot	Enables / Disables boot with initialization of a minimal set of devices required to launch the active boot option. Has no effect for BBS boot options.
Boot mode select	Selects a Boot mode, Legacy / UEFI / Dual.
Boot Option Priorities	Sets the system boot order priorities for hard disk, CD/DVD, USB, Network.

4.14 Save & Exit Settings (IB917)



BIOS Setting	Description
Save Changes and Exit	Exits system setup after saving the changes.
Discard Changes and Exit	Exits system setup without saving any changes.
Save Changes and Reset	Resets the system after saving the changes.
Discard Changes and Reset	Resets system setup without saving any changes.
Save Changes	Saves changes done so far to any of the setup options.
Discard Changes	Discards changes done so far to any of the setup options.
Restore Defaults	Restores / Loads defaults values for all the setup options.
Save as User Defaults	Saves the changes done so far as User Defaults.
Restore User Defaults	Restores the user defaults to all the setup options.

Appendix

This section (based on IB811F board) provides the mapping addresses of peripheral devices and the sample code of watchdog timer configuration.

- I/O Port Address Map
- Interrupt Request Lines (IRQ)
- Watchdog Timer Configuration

A. I/O Port Address Map (IB818F)

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0x00000A00-0x00000A0F	Motherboard resources
0x00000A10-0x00000A1F	Motherboard resources
0x00000A20-0x00000A2F	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000070-0x00000070	System CMOS/real time clock
0x00000080-0x0000008F	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x00000400-0x0000047F	Motherboard resources
0x00000500-0x000005FE	Motherboard resources
0x00000600-0x0000061F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x0000F040-0x0000F05F	Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4
0x0000D000-0x0000DFFF	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD9

Address	Device Description
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x000003E8-0x000003EF	Communications Port (COM3)
0x000002E8-0x000002EF	Communications Port (COM4)
0x0000E000-0x0000EFFF	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8
0x00000000-0x0000006F	PCI Express Root Complex
0x00000078-0x00000CF7	PCI Express Root Complex
0x00000D00-0x0000FFFF	PCI Express Root Complex
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x0000F000-0x0000F03F	Intel(R) HD Graphics
0x0000F090-0x0000F097	Standard SATA AHCI Controller
0x0000F080-0x0000F083	Standard SATA AHCI Controller
0x0000F060-0x0000F07F	Standard SATA AHCI Controller
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer

B. I/O Port Address Map (IB917)

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x00000A00-0x00000A0F	Motherboard resources
0x00000A10-0x00000A1F	Motherboard resources
0x00000A10-0x00000A1F	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000070-0x00000070	System CMOS/real time clock
0x00000080-0x00000080	Motherboard resources

Address	Device Description
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x00001800-0x000018FE	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x00001854-0x00001857	Motherboard resources
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x000003E8-0x000003EF	Communications Port (COM3)
0x000002E8-0x000002EF	Communications Port (COM4)
0x00000000-0x00000CF7	PCI Express Root Complex
0x00000D00-0x0000FFFF	PCI Express Root Complex
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer
0x0000E000-0x0000EFFF	Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #11 - 9D1A
0x0000F040-0x0000F05F	Mobile 6th/7th Generation Intel(R) Processor Family I/O SMBUS - 9D23
0x0000FF00-0x0000FFFE	Motherboard resources
0x00000060-0x00000060	Standard PS/2 Keyboard
0x00000064-0x00000064	Standard PS/2 Keyboard
0x0000F090-0x0000F097	Standard SATA AHCI Controller
0x0000F080-0x0000F083	Standard SATA AHCI Controller
0x0000F060-0x0000F07F	Standard SATA AHCI Controller
0x0000F000-0x0000F03F	Intel(R) HD Graphics 620
0x000003B0-0x000003BB	Intel(R) HD Graphics 620
0x000003C0-0x000003DF	Intel(R) HD Graphics 620

C. Interrupt Request Lines (IRQ) (IB818F)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 0	System timer
IRQ 3	Communications Port (COM2)
IRQ 4	Communications Port (COM1)
IRQ 4	PCI Data Acquisition and Signal Processing Controller
IRQ 5	Communications Port (COM3)
IRQ 5	PCI Data Acquisition and Signal Processing Controller
IRQ 6	PCI Data Acquisition and Signal Processing Controller
IRQ 7	PCI Data Acquisition and Signal Processing Controller
IRQ 8	High precision event timer
IRQ 10	Communications Port (COM4)
IRQ 14	Intel(R) Serial IO GPIO Host Controller - INT3452
IRQ 25	High Definition Audio Controller
IRQ 35	PCI Data Acquisition and Signal Processing Controller
IRQ 36	PCI Data Acquisition and Signal Processing Controller
IRQ 37	PCI Data Acquisition and Signal Processing Controller
IRQ 39	SDA Standard Compliant SD Host Controller
IRQ 54 ~ 204	Microsoft ACPI-Compliant System
IRQ 256 ~ 511	Microsoft ACPI-Compliant System
IRQ 4294967279	Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
IRQ 4294967280 ~ 285	Intel(R) I211 Gigabit Network Connection #2
IRQ 4294967286 ~ 291	Intel(R) I211 Gigabit Network Connection
IRQ 4294967292	Intel(R) Trusted Execution Engine Interface
IRQ 4294967293	Intel(R) HD Graphics
IRQ 4294967294	Standard SATA AHCI Controller

D. Interrupt Request Lines (IRQ) (IB917)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 0	System timer
IRQ 1	Standard PS/2 Keyboard
IRQ 3	Communications Port (COM2)
IRQ 4	Communications Port (COM1)
IRQ 5	Communications Port (COM3)
IRQ 7	Communications Port (COM4)
IRQ 8	System CMOS/real time clock
IRQ 11	Mobile 6th/7th Generation Intel(R) Processor Family I/O SMBUS - 9D23
IRQ 11	Mobile 6th/7th Generation Intel(R) Processor Family I/O Thermal subsystem - 9D31
IRQ 12	Microsoft PS/2 Mouse
IRQ 14	Motherboard resources
IRQ 16	High Definition Audio Controller
IRQ 54 ~ 204	Microsoft ACPI-Compliant System
IRQ 256 ~ 511	Microsoft ACPI-Compliant System
IRQ 4294967285	Intel(R) Management Engine Interface
IRQ 4294967286	Intel(R) I211 Gigabit Network Connection
IRQ 4294967287	Intel(R) I211 Gigabit Network Connection
IRQ 4294967288	Intel(R) I211 Gigabit Network Connection
IRQ 4294967289	Intel(R) I211 Gigabit Network Connection
IRQ 4294967290	Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
IRQ 4294967291	Intel(R) HD Graphics 620
IRQ 4294967292	Intel(R) Ethernet Connection I219-V
IRQ 4294967293	Standard SATA AHCI Controller
IRQ 4294967294	Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #11 - 9D1A

E. Watchdog Timer Configuration

The Watchdog Timer (WDT) is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven.

Under normal circumstance, you will need to restart the WDT at regular intervals before the timer counts to zero.

Sample Code 1:

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81964.H"
//---------------------------------------------------------------------------
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//---------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        char SIO;

        printf("Fintek 81964 watch dog program\n");
        SIO = Init_F81964();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81964, program abort.\n");
                return(1);
        }//if (SIO == 0)

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return (1);
        }

        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        if (bTime)
        {  EnableWDT(bTime); }
        else
        {  DisableWDT();        }
        return 0;
}
//---------------------------------------------------------------------------
```

```
void EnableWDT(int interval)
{
	unsigned char bBuf;

	bBuf = Get_F81964_Reg(0x2B);
	bBuf &= (~0x20);
	Set_F81964_Reg(0x2B,	bBuf);	//Enable WDTO

	Set_F81964_LD(0x07);		//switch to logic device 7
	Set_F81964_Reg(0x30,	0x01);	//enable timer

	bBuf = Get_F81964_Reg(0xF5);
	bBuf &= (~0x0F);
	bBuf |= 0x52;
	Set_F81964_Reg(0xF5,	bBuf);	//count mode is second

	Set_F81964_Reg(0xF6,	interval);//set timer

	bBuf = Get_F81964_Reg(0xFA);
	bBuf |= 0x01;
	Set_F81964_Reg(0xFA,	bBuf);	//enable WDTO output

	bBuf = Get_F81964_Reg(0xF5);
	bBuf |= 0x20;
	Set_F81964_Reg(0xF5,	bBuf);	//start counting
}
//-----------------------------------------------------------------------------
void DisableWDT(void)
{
	unsigned char bBuf;

	Set_F81964_LD(0x07);		//switch to logic device 7

	bBuf = Get_F81964_Reg(0xFA);
	bBuf &= ~0x01;
	Set_F81964_Reg(0xFA,	bBuf);	//disable WDTO output

	bBuf = Get_F81964_Reg(0xF5);
	bBuf &= ~0x20;
	bBuf |= 0x40;
	Set_F81964_Reg(0xF5,	bBuf);	//disable WDT
}
//-----------------------------------------------------------------------------


//-----------------------------------------------------------------------------
//
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// PURPOSE.
//
//-----------------------------------------------------------------------------
#include "F81964.H"
#include <dos.h>
//-----------------------------------------------------------------------------
unsigned int F81964_BASE;
void Unlock_F81964 (void);
void Lock_F81964 (void);
//-----------------------------------------------------------------------------
unsigned int Init_F81964(void)
{
	unsigned int result;
	unsigned char ucDid;
```

```
		F81964_BASE = 0x4E;
		result = F81964_BASE;

		ucDid = Get_F81964_Reg(0x20);
		if   (ucDid  ==  0x07)		//Fintek 81964
		{  goto     Init_Finish;  }

		F81964_BASE = 0x2E;
		result = F81964_BASE;

		ucDid = Get_F81964_Reg(0x20);
		if   (ucDid  ==  0x07)		//Fintek 81964
		{  goto     Init_Finish;  }

		F81964_BASE = 0x00;
		result = F81964_BASE;

Init_Finish:
		return (result);
}
//-----------------------------------------------------------------------------
void Unlock_F81964 (void)
{
		outportb(F81964_INDEX_PORT, F81964_UNLOCK);
		outportb(F81964_INDEX_PORT, F81964_UNLOCK);
}
//-----------------------------------------------------------------------------
void Lock_F81964 (void)
{
		outportb(F81964_INDEX_PORT, F81964_LOCK);
}
//-----------------------------------------------------------------------------
void Set_F81964_LD( unsigned char LD)
{
		Unlock_F81964();
		outportb(F81964_INDEX_PORT, F81964_REG_LD);
		outportb(F81964_DATA_PORT, LD);
		Lock_F81964();
}
//-----------------------------------------------------------------------------
void Set_F81964_Reg( unsigned char REG, unsigned char DATA)
{
		Unlock_F81964();
		outportb(F81964_INDEX_PORT, REG);
		outportb(F81964_DATA_PORT, DATA);
		Lock_F81964();
}
//-----------------------------------------------------------------------------
unsigned char Get_F81964_Reg(unsigned char REG)
{
		unsigned char Result;
		Unlock_F81964();
		outportb(F81964_INDEX_PORT, REG);
		Result = inportb(F81964_DATA_PORT);
		Lock_F81964();
		return Result;
}
//-----------------------------------------------------------------------------

//-----------------------------------------------------------------------------
//
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// PURPOSE.
//
```

```
//---------------------------------------------------------------------------
#ifndef      F81964_H
#define      F81964_H              1
//---------------------------------------------------------------------------
#define        F81964_INDEX_PORT     (F81964_BASE)
#define        F81964_DATA_PORT      (F81964_BASE+1)
//---------------------------------------------------------------------------
#define        F81964_REG_LD    0x07
//---------------------------------------------------------------------------
#define        F81964_UNLOCK   0x87
#define        F81964_LOCK       0xAA
//---------------------------------------------------------------------------
unsigned int Init_F81964(void);
void Set_F81964_LD( unsigned char);
void Set_F81964_Reg( unsigned char,
unsigned char); unsigned char
Get_F81964_Reg( unsigned char);
//---------------------------------------------------------------------------
#endif   //     F81964_H
```

Sample Code 2:

```
//---------------------------------------------------------------------------
//
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// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81866.H"
//---------------------------------------------------------------------------
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//---------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        char SIO;

        printf("Fintek 81866 watch dog program\n");
        SIO = Init_F81866();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81866, program abort.\n");
                return(1);
        }//if (SIO == 0)

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return (1);
        }
```

```
        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        if (bTime)
        {  EnableWDT(bTime); }
        else
        {  DisableWDT();        }
        return 0;
}
//-------------------------------------------------------------------------
void EnableWDT(int interval)
{
        unsigned char bBuf;

        bBuf = Get_F81866_Reg(0x2B);
        bBuf &= (~0x20);
        Set_F81866_Reg(0x2B,    bBuf);    //Enable WDTO

        Set_F81866_LD(0x07);              //switch to logic device 7
        Set_F81866_Reg(0x30,    0x01);    //enable timer

        bBuf = Get_F81866_Reg(0xF5);
        bBuf &= (~0x0F);
        bBuf |= 0x52;
        Set_F81866_Reg(0xF5,    bBuf);    //count mode is second

        Set_F81866_Reg(0xF6,    interval);//set timer

        bBuf = Get_F81866_Reg(0xFA);
        bBuf |= 0x01;
        Set_F81866_Reg(0xFA,    bBuf);    //enable WDTO output

        bBuf = Get_F81866_Reg(0xF5);
        bBuf |= 0x20;
        Set_F81866_Reg(0xF5,    bBuf);    //start counting
}
//-------------------------------------------------------------------------
void DisableWDT(void)
{
        unsigned char bBuf;

        Set_F81866_LD(0x07);              //switch to logic device 7

        bBuf = Get_F81866_Reg(0xFA);
        bBuf &= ~0x01;
        Set_F81866_Reg(0xFA,    bBuf);    //disable WDTO output

        bBuf = Get_F81866_Reg(0xF5);
        bBuf &= ~0x20;
        bBuf |= 0x40;
        Set_F81866_Reg(0xF5,    bBuf);    //disable WDT
}
//-------------------------------------------------------------------------


//-------------------------------------------------------------------------
//
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// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-------------------------------------------------------------------------
#include "F81866.H"
#include <dos.h>
//-------------------------------------------------------------------------
```

```
unsigned int F81866_BASE;
void Unlock_F81866 (void);
void Lock_F81866 (void);
//---------------------------------------------------------------------------
unsigned int Init_F81866(void)
{
        unsigned int result;
        unsigned char ucDid;

        F81866_BASE = 0x4E;
        result = F81866_BASE;

        ucDid = Get_F81866_Reg(0x20);
        if   (ucDid  ==  0x07)          //Fintek 81866
        {  goto     Init_Finish;  }

        F81866_BASE = 0x2E;
        result = F81866_BASE;

        ucDid = Get_F81866_Reg(0x20);
        if   (ucDid  ==  0x07)          //Fintek 81866
        {  goto     Init_Finish;  }

        F81866_BASE = 0x00;
        result = F81866_BASE;

Init_Finish:
        return (result);
}
//---------------------------------------------------------------------------
void Unlock_F81866 (void)
{
        outportb(F81866_INDEX_PORT, F81866_UNLOCK);
        outportb(F81866_INDEX_PORT, F81866_UNLOCK);
}
//---------------------------------------------------------------------------
void Lock_F81866 (void)
{
        outportb(F81866_INDEX_PORT, F81866_LOCK);
}
//---------------------------------------------------------------------------
void Set_F81866_LD( unsigned char LD)
{
        Unlock_F81866();
        outportb(F81866_INDEX_PORT, F81866_REG_LD);
        outportb(F81866_DATA_PORT, LD);
        Lock_F81866();
}
//---------------------------------------------------------------------------
void Set_F81866_Reg( unsigned char REG, unsigned char DATA)
{
        Unlock_F81866();
        outportb(F81866_INDEX_PORT, REG);
        outportb(F81866_DATA_PORT, DATA);
        Lock_F81866();
}
//---------------------------------------------------------------------------
unsigned char Get_F81866_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_F81866();
        outportb(F81866_INDEX_PORT, REG);
        Result = inportb(F81866_DATA_PORT);
        Lock_F81866();
        return Result;
```

```
}
//---------------------------------------------------------------------------



//---------------------------------------------------------------------------
//
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// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#ifndef      F81866_H
#define      F81866_H                1
//---------------------------------------------------------------------------
#define         F81866_INDEX_PORT     (F81866_BASE)
#define         F81866_DATA_PORT      (F81866_BASE+1)
//---------------------------------------------------------------------------
#define         F81866_REG_LD    0x07
//---------------------------------------------------------------------------
#define         F81866_UNLOCK   0x87
#define         F81866_LOCK        0xAA
//---------------------------------------------------------------------------
unsigned int Init_F81866(void);
void Set_F81866_LD( unsigned char);
void Set_F81866_Reg( unsigned char,
unsigned char); unsigned char
Get_F81866_Reg( unsigned char);
//---------------------------------------------------------------------------
#endif   //     F81866_H
```