Approval Sheet

Customer	
Product Number	**M4ME-AGM25CIK-F**
Module speed	**PC4-2666**
Pin	**288 pin**
Cl-tRCD-tRP	**19-19-19**
Operating Temp	**0℃~85℃**
Date	**27th May 2022**

Rev 1.0

The Total Solution For Industrial Flash Storage

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			CL	tRCD	tRP
		CL=15	CL=17	CL=19			
PC4-2666	**I**	2133	2400	2666	19	19	19

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- JEDEC Standard 288-pin Mini Registered Dual In-Line Memory Module
- Intend for PC4-2666 applications
- Inputs and Outputs are SSTL-12 compatible
- V_{DD}=V_{DDQ}= 1.2 Volt (1.14V~1.26V)
- V_{PP}=2.5 Volt (2.375V~2.75V)
- V_{DDSPD}=2.2-3.6V
- Low-Power auto self-refresh (LPASR)
- SDRAMs have 16 internal banks for concurrent operation (4 Bank Group of 4 banks each)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals.
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Gold Plating Thickness 30μ”
- Fly-By topology
- Terminated control, command and address bus
- Programmable /CAS Latency: 10,11,12,13,14,15,16,17,18,19,20
- On-die V_{REFDQ} generation and Calibration
- Temperature Sensor with SPD EEPROM
- RoHS and Halogen free *(Section 11)*
- Support ECC function

2. Ordering Information

DDR4 VLP Mini-RDIMM w/ ECC						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M4ME-AGM25CIK-F	16GB	PC4-2666	2Gx72	9	1	Y

3. Pin Configurations (Front side/Back side)

DDR4 2Gx8 base Mini-RDIMM w/ ECC

Front	Pins		Back
NC	1	145	VREFCA
NC	2	146	SAVE_n, NC
RFU	3	147	RFU
VSS	4	148	VSS
DQ0	5	149	DQ4
VSS	6	150	VSS
DQ1	7	151	DQ5
VSS	8	152	VSS
DQS0_c	9	153	DQS9_t %
DQS0_t	10	154	DQS9_c *
VSS	11	155	VSS
DQ2	12	156	DQ6
VSS	13	157	VSS
DQ3	14	158	DQ7
VSS	15	159	VSS
DQ8	16	160	DQ12
VSS	17	161	VSS
DQ9	18	162	DQ13
VSS	19	163	VSS
DQS1_c	20	164	DQS10_t %
DQS1_t	21	165	DQS10_c *
VSS	22	166	VSS
DQ10	23	167	DQ14
VSS	24	168	VSS
DQ11	25	169	DQ15
VSS	26	170	VSS
DQ16	27	171	DQ20
VSS	28	172	VSS
DQ17	29	173	DQ21
VSS	30	174	VSS
DQS2_c	31	175	DQS11_t %
DQS2_t	32	176	DQS11_c *
VSS	33	177	VSS
DQ18	34	178	DQ22
VSS	35	179	VSS
DQ19	36	180	DQ23
VSS	37	181	VSS
DQ24	38	182	DQ28
VSS	39	183	VSS
DQ25	40	184	DQ29
VSS	41	185	VSS
DQS3_c	42	186	DQS12_t %
DQS3_t	43	187	DQS12_c *
VSS	44	188	VSS
DQ26	45	189	DQ30
VSS	46	190	VSS
DQ27	47	191	DQ31
VSS	48	192	VSS
CB0, NC	49	193	CB4, NC
VSS	50	194	VSS
CB1, NC	51	195	CB5, NC
VSS	52	196	VSS
DQS8_c	53	197	DQS17_t %
DQS8_t	54	198	DQS17_c *
VSS	55	199	VSS
CB2, NC	56	200	CB6, NC
VSS	57	201	VSS
CB3, NC	58	202	CB7, NC
VSS	59	203	VSS

Front	Pins		Back
ALERT_n	60	204	RESET_n
CKE0	61	205	RFU
VDD	62	206	VDD
ACT_n	63	207	CKE1, NC
BG0	64	208	BG1
VDD	65	209	VDD
A12/BC_n	66	210	A11
A9	67	211	A7
VDD	68	212	VDD
A8	69	213	A5
A6	70	214	A4
VDD	71	215	VDD
A3	72	216	A2
A1	73	217	RFU
VDD	74	218	VDD
CK0_t	75	219	CK1_t
CK0_c	76	220	CK1_c
VDD	77	221	VDD
RFU	78	222	RFU
VTT	79	223	VTT
Key			
EVENT_n	80	224	PARITY
VDD	81	225	VDD
A0	82	226	BA1
BA0	83	227	A10/AP
VDD	84	228	VDD
RAS_n/A16	85	229	A14_WE_n
CS0_n	86	230	A15_CAS_n
VDD	87	231	VDD
ODT0	88	232	A13
CS1_n,NC	89	233	A17, NC
VDD	90	234	VDD
ODT1,NC	91	235	C1, CS3_n, NC
C0, CS2_n, NC	92	236	NC, C2
VDD	93	237	VDD
RFU	94	238	RFU
VSS	95	239	VSS

Front	Pins		Back
DQ32	96	240	DQ36
VSS	97	241	VSS
DQ33	98	242	DQ37
VSS	99	243	VSS
DQS4_c	100	244	DQS13_t %
DQS4_t	101	245	DQS13_c *
VSS	102	246	VSS
DQ34	103	247	DQ38
VSS	104	248	VSS
DQ35	105	249	DQ39
VSS	106	250	VSS
DQ40	107	251	DQ44
VSS	108	252	VSS
DQ41	109	253	DQ45
VSS	110	254	VSS
DQS5_c	111	255	DQS14_t %
DQS5_t	112	256	DQS14_c *
VSS	113	257	VSS
DQ42	114	258	DQ46
VSS	115	259	VSS
DQ43	116	260	DQ47
VSS	117	261	VSS
DQ48	118	262	DQ52
VSS	119	263	VSS
DQ49	120	264	DQ53
VSS	121	265	VSS
DQS6_c	122	266	DQS15_t %
DQS6_t	123	267	DQS15_c *
VSS	124	268	VSS
DQ50	125	269	DQ54
VSS	126	270	VSS
DQ51	127	271	DQ55
VSS	128	272	VSS
DQ56	129	273	DQ60
VSS	130	274	VSS
DQ57	131	275	DQ61
VSS	132	276	VSS
DQS7_c	133	277	DQS16_t %
DQS7_t	134	278	DQS16_c *
VSS	135	279	VSS
DQ58	136	280	DQ62
VSS	137	281	VSS
DQ59	138	282	DQ63
VSS	139	283	VSS
SA0	140	284	SA1
VDDSPD	141	285	SA2
SDA	142	286	SCL
VPP	143	287	VPP
VPP	144	288	VPP

CS pin will based on Chip and Module configuration, normal CS2 and CS3 will be NC

% These signals include TDQS_t, BDI_n and DM_n refer to below
Pin153=/DM0, /DBI0; Pin164=/DM1, /DBI1; Pin175=/DM2, /DBI2; Pin186=/DM3, /DBI3
Pin197=/DM8, /DBI8; Pin244=/DM4, /DBI4; Pin255=/DM5, /DBI5; Pin266=/DM6, /DBI6
Pin277=/DM7, /DBI7

* These signals include TDQS_c and NC refer to below
Pin154, 165, 176, 187, 198, 245, 256, 267, 278=NC

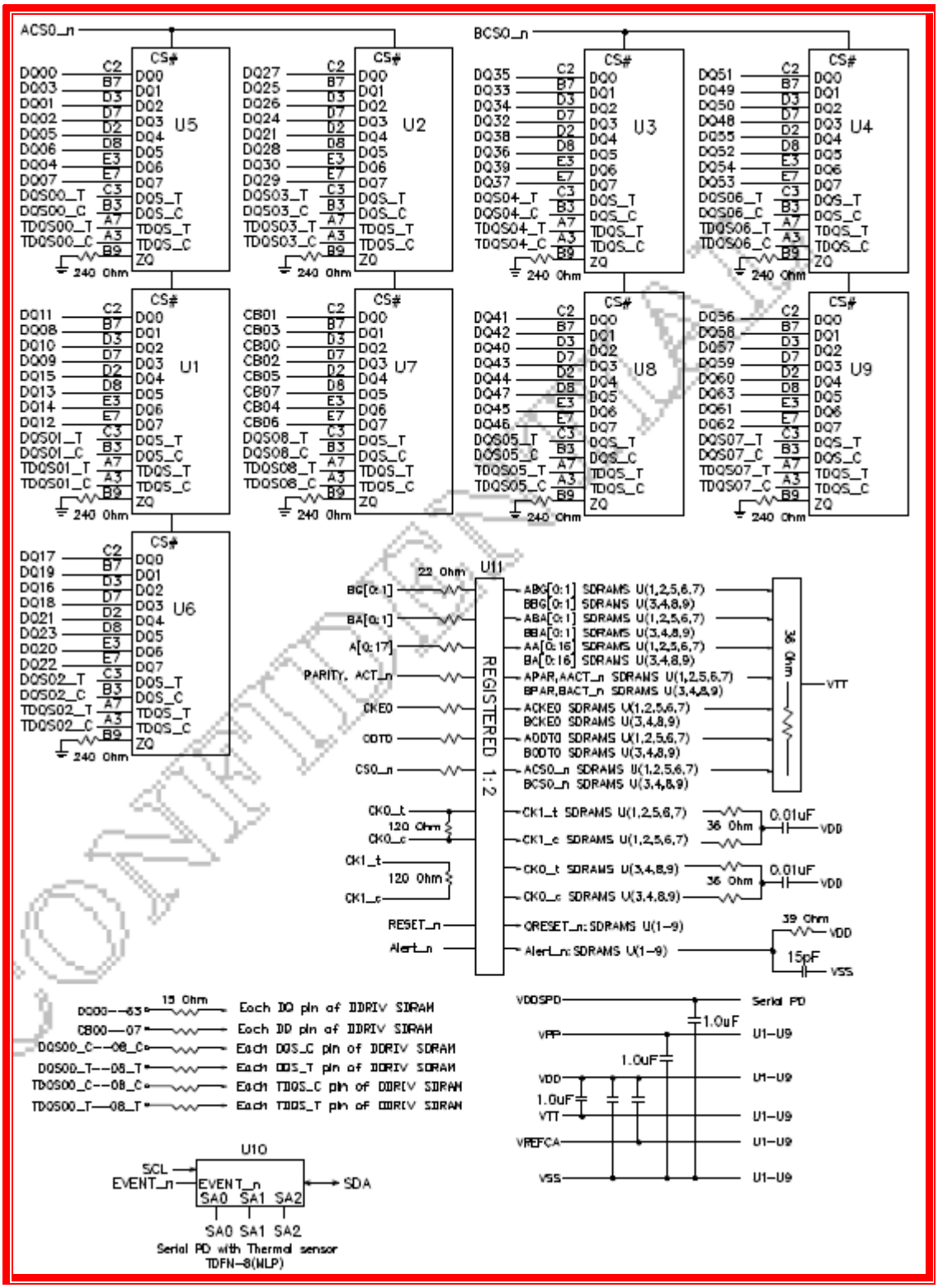
4. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0-A17	Register address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I2C serial bus data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0-SA2	I2C slave address select for SPD/TS and register
RAS_n	Register row address strobe input	PAR	Register parity input
CAS_n	Register column address strobe input	VDD	SDRAM core power supply
WE_n	Register write enable input	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input activate input	ALERT_n	Register ALERT_n output
DQ0-DQ63	DIMM memory data bus	RESET_n	Set Register and SDRAMs to a Known State
CB0-CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t-DQS17_t	Data buffer data strobes (positive)	VTT	SDRAM I/O termination supply
DQS0_c-DQS17_c	Data buffer data strobes (negative)	RFU	Reserved for future use
CK0_t,CK1_t	Register clock input (positive)		
CK0_c, CK1_c	Register clock input (negative)		

5. Function Block Diagram:

- (16GB, 1 Rank 2Gx8 DDR4 SDRAMs)



Rev 1.0

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6. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.4 to +1.5	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.4 to +1.5	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.4 to +1.5	V	4,6

Note:

1) Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM.

2) The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions.

3) Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

7. Operating Condition

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
$V_{REFCA(DC)}$	Input reference voltage command/ address bus	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	3
V_{TT}	Termination Voltage	0.49 × VDD	0.5 × VDD	0.51 × VDD	V	4

Note:

1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
4. VTT termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.

8. Operating, Standby, and Refresh Currents

- 16GB Mini-RDIMM w/ ECC (1 Rank 2Gx8 DDR4 SDRAMs)

Symbol	Proposed Conditions	Value		Units
		IDD Max.	IPP Max.	
IDD0	Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n:stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2;ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	552	27	mA
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0	-	-	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stableat 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	621	-	mA
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1	-	-	mA
IDD2N	Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banksclosed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	432	-	mA
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N	-	-	mA

IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern	468	-	mA
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled3	-	-	mA
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled3	-	-	mA
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled3	-	-	mA
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled3	-	-	mA
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	387	-	mA
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	423	-	mA
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern	531	18	mA

IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N	-	-	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	432	-	mA
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1314	-	mA
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R	-	-	mA
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled3, Other conditions: see IDD4R	-	-	mA
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	1053	-	mA
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W	-	-	mA
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions: see IDD4W	-	-	mA

IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled3, Other conditions: see IDD4W	-	-	mA
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled3, Other conditions: see IDD4W	-	-	mA
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	612	36	mA
IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B	-	-	mA
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B	-	-	mA
IDD6N	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	513	-	mA
IDD6E	Self-Refresh Current: Extended Temperature Range) TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	1017	-	mA

IDD6R	Self-Refresh Current: Reduced Temperature Range TCASE: 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	216	-	mA
IDD6A	Auto Self-Refresh Current TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	459	54	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1647	72	mA
IDD8	Maximum Power Down Current TBD	342	-	mA

9. Timing Parameters

Clock Timing				
Parameter	Symbol	MIN	MAX	Units
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	ns
Average Clock Period	tCK(avg)	0.750	<0.833	ns
Average high pulse width	tCH(avg)	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_ to t	tCK(avg)max + tJIT(per)max_tot	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.45	-	tCK(avg)
Clock Period Jitter- total	JIT(per)_tot	-38	38	ps
Clock Period Jitter- deterministic	JIT(per)_dj	-19	19	ps
Clock Period Jitter during DLL lock-ing period	tJIT(per, lck)	-30	30	ps
Cycle to Cycle Period Jitter	tJIT(cc)_to-tal	75		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	60		ps
Cumulative error across 2 cycles	tERR(2per)	-55	55	ps
Cumulative error across 3 cycles	tERR(3per)	-66	66	ps
Cumulative error across 4 cycles	tERR(4per)	-73	73	ps
Cumulative error across 5 cycles	tERR(5per)	-78	78	ps
Cumulative error across 6 cycles	tERR(6per)	-83	83	ps
Cumulative error across 7 cycles	tERR(7per)	-87	87	ps

Cumulative error across 8 cycles	tERR(8per)	-91	91	ps
Cumulative error across 9 cycles	tERR(9per)	-94	94	ps
Cumulative error across 10 cycles	tERR(10per)	-96	96	ps
Cumulative error across 11 cycles	tERR(11per)	-99	99	ps
Cumulative error across 12 cycles	tERR(12per)	-101	101	ps
Cumulative error across 13 cycles	tERR(13per)	-103	103	ps
Cumulative error across 14 cycles	tERR(14per)	-104	104	ps
Cumulative error across 15 cycles	tERR(15per)	-106	106	ps
Cumulative error across 16 cycles	tERR(16per)	-108	108	ps
Cumulative error across 17 cycles	tERR(17per)	-110	110	ps
Cumulative error across 18 cycles	tERR(18per)	-112	112	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)		ps
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	TBD	-	ps
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	TBD	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	TBD	-	ps
Command and Address hold time to CK_t, CK_c referenced	tIH(Vref)	TBD	-	ps

to Vref levels				
Control and Address Input pulse width for each input	tIPW	385	-	ps
Command and Address Timing				
Parameter	Symbol	MIN	MAX	Units
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 5 ns)	-	nCK
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S(1/ 2K)	Max(4nCK,3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,4.9ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/ 2K)	Max(4nCK,4.9ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,21ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,12ns)	-	ns
Delay from start of internal write transaction to internal read com-mand for different	tWTR_S	max(2nCK,2.5ns)	-	

bank group				
Delay from start of internal write transaction to internal read com-mand for same bank group	tWTR_L	max(4nCK,7.5ns)	-	
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (5nCK,3.75ns)	-	ns
delay from start of internal write transaction to internal read com-mand for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max (5nCK,3.75ns)	-	ns
delay from start of internal write transaction to internal read com-mand for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+max (5nCK,3.75ns)	-	ns
DLL locking time	tDLLK	854	-	nCK
Mode Register Set command cycle time	tMRD	8	-	nCK
Mode Register Set command up-date delay	tMOD	max(24nCK,15ns)	-	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
Multi Purpose Register Write Re-covery Time	tWR_MPR	tMOD (min) + AL + PL	-	-
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))		nCK
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	UI
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing	tPDA_H	0.5	-	UI

edge				
CS_n to Command Address Latency				
CS_n to Command Address Laten-cy	tCAL	5	-	nCK
DRAM Data Timing				
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.18	tCK(avg) /2
DQ output hold time from DQS_t,DQS_c	tQH	0.74	-	tCK(avg) /2
Data Valid Window per device: tQH - tDQSQ for a device	tDVWd	TBD	-	UI
Data Valid Window per device, per pin: tQH - tDQSQ each device's out-put	tDVWp	0.72	-	UI
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-310	170	Ps
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	170	ps
Data Strobe Timing				
DQS_t, DQS_c differential READ Preamble	tRPRE	0.9	-	tCK
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	-	tCK
DQS_t,DQS_c differential output high time	tQSH	0.4	-	tCK
DQS_t,DQS_c differential output low time	tQSL	0.4	-	tCK
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	tCK
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	tCK
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-310	170	ps
DQS_t and DQS_c high-impedance time	tHZ(DQS)	-	170	ps

(Referenced from RL+BL/2)				
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	tCK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	tCK
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	tCK
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	tCK
DQS_t, DQS_c rising edge output timing locatino from rising	tDQSCK (DLL On)	-170	170	ps
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)		270	ps
MPSM Timing				
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)		
Exit MPSM to commands not requiring a locked DLL	tXMP	txs(imin)		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)		
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	
Calibration Timing				
Power-up and RESET calibration time	tZQinit	1024	-	nCK
Normal operation Full	tZQoper	512	-	nCK

calibration time				
Normal operation Short calibration time	tZQCS	128	-	nCK
Reset/Self Refresh Timing				
Exit Reset from CKE HIGH to a valid command	command tXPR	max (5nCK,tRFC(min)+ 10ns)	-	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+1 0ns	-	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT(min)	tRFC4(min)+ 10ns	-	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	
Exit Self Refresh to commands re-quiring a locked DLL	tXSDLL	tDLLK(min)	-	
Minimum CKE low width for Self re-fresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	
Minimum CKE low width for Self re-fresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power- Down Entry (PDE)	tCKSRE	max(5nCK,10 ns)	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power- Down when CA Parity is enabled	tCKS-RE_PAR	max (5nCK,10ns) +PL	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10 ns)	-	
Power Down Timing				
Exit Power Down with DLL on	tXP	(4nCK,6ns)	-	

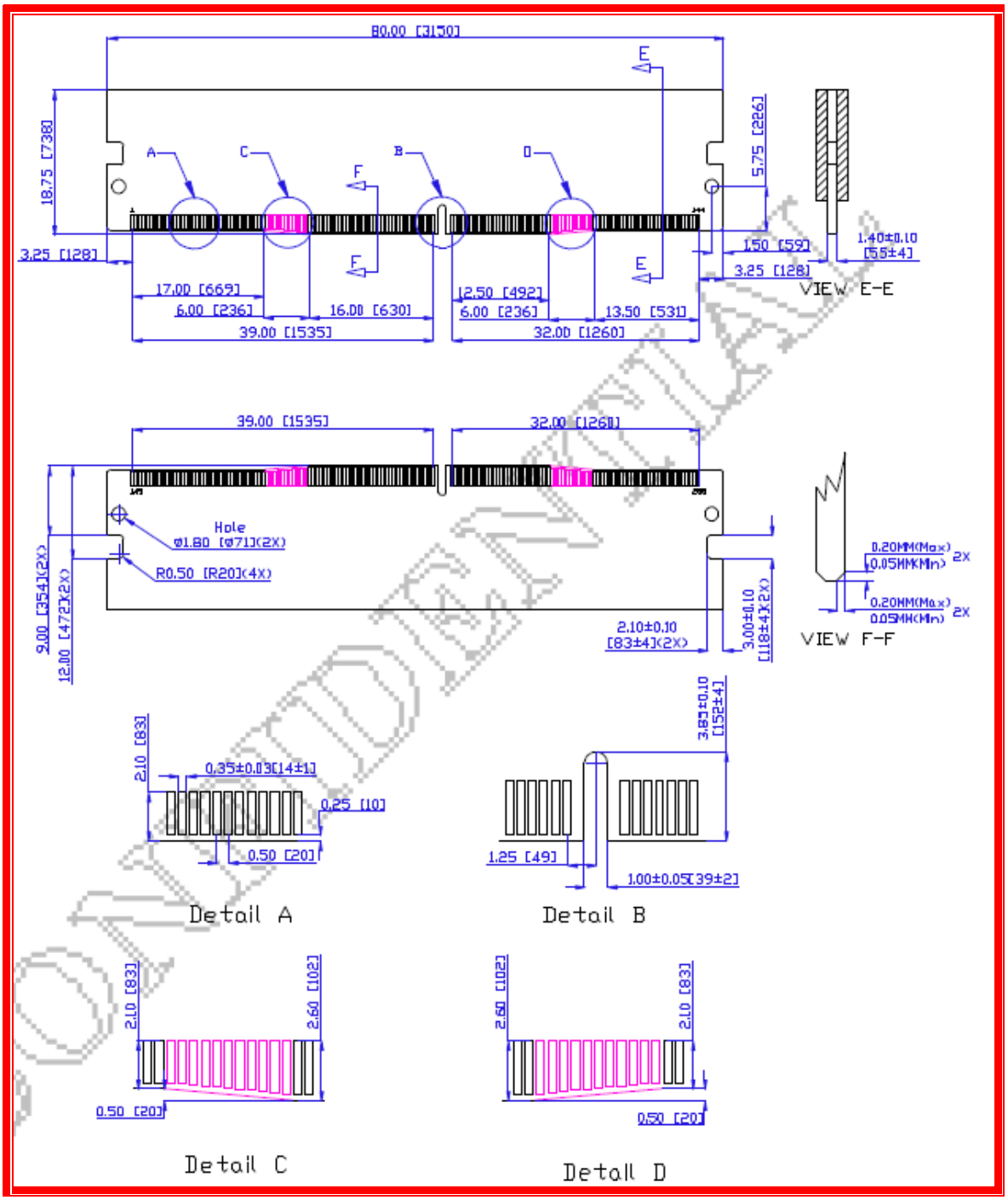
to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL				
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	
Command pass disable delay	tCPDED	4	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	2	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	2	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	
PDA Timing				
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)		
Mode Register Set command up-date delay in PDA mode	tMOD_PDA	tMOD		
ODT Timing				
Asynchronous RTT turn-on	tAONAS	1.0	9.0	ns

delay (Power-Down with DLL frozen)				
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	ns
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
Write Leveling Timing				
First DQS_t/DQS_n rising edge af-ter write leveling mode is pro-grammed	tWLMRD	40	-	nCK
DQS_t/DQS_n delay after write lev-eling mode is programmed	tWLDQSEN	25	-	nCK
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	tCK(avg)
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	tCK(avg)
Write leveling output delay	tWLO	0	9.5	ns
Write leveling output error	tWLOE		2	ns
CA Parity Timing				
Commands not guaranteed to be executed during this time	tPAR_UN-KNOWN	-	PL	
Delay from errant command to ALERT_n assertion	tPAR_ALER T_ON	-	PL+6ns	
Pulse width of ALERT_n signal when asserted	tPAR_ALER T_PW	80	160	nCK
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALER T_RSP	-	71	nCK
Parity Latency	PL	5		nCK
CRC Error Reporting				
CRC error to ALERT_n latency	tCRC_ALER T	3	13	ns

CRC ALERT_n pulse width	CRC_ALER T_PW	6	10	nCK
tREFI				
tRFC1 (min)	2Gb	160	-	ns
	4Gb	260	-	ns
	8Gb	350	-	ns
	16Gb	550	-	ns
tRFC2 (min)	2Gb	110	-	ns
	4Gb	160	-	ns
	8Gb	260	-	ns
	16Gb	350	-	ns
tRFC3 (min)	2Gb	90	-	ns
	4Gb	110	-	ns
	8Gb	160	-	ns
	16Gb	260	-	ns

10. PACKAGE DIMENSION

- (16GB, 1Rank 2Gx8 DDR4 base VLP Mini-RDIMM w/ ECC)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified

11. RoHS Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation

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Tel:(02)7703-3000 Internet: https://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Products: All Innodisk EM FLASH, DRAM and EP products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及(EU) 2015/863 關於 RoHS 之規範要求。
Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。
Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

三、 本公司聲明我們的產品符合 RoHS 指令的附件中(7a)、(7c-I)允許豁免。
We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.
※ (7a) Lead in high melting temperature type solders(i.e. lead-based alloys containing 85% by weight or more lead).
※ (7C-I) Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
鉛 (Pb)	< 1000 ppm
汞 (Hg)	< 1000 ppm
鎘 (Cd)	< 100 ppm
六價鉻 (Cr 6+)	< 1000 ppm
多溴聯苯 (PBBs)	< 1000 ppm
多溴二苯醚 (PBDEs)	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯 (DEHP)	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯 (BBP)	< 1000 ppm
鄰苯二甲酸二丁酯 (DBP)	< 1000 ppm
鄰苯二甲酸二異丁酯 (DIBP)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2020 / 03 / 03

12. REACH Declaration

innodisk

宜鼎國際股份有限公司

Innodisk Corporation

REACH Declaration

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: https://www.innodisk.com/

Innodisk Corporation pursues its social responsibility for global environmental preservation by committing to be compliant with REACH regulation (REGULATION (EC) No 1907/2006).
We hereby confirm that the product(s),
Scope: Flash Memory, DRAM Module and Embedded Peripherals Products.

■ The standard products of **not listed in** the ***Appendix2*** meet the requirements of REACH SVHC regulations(SVHCs < 0.1% in Article), as described in the candidate list table currently including 219 substances and shown on the ECHA website. (http://echa.europa.eu/de/candidate-list-table).

■ Contain(s) one or more hazardous substances or constituents exceeding 0.1 % by weight in article if not otherwise specified in candidate list table.
Where the threshold value is exceeded, the substances in question are to be declared in accompanying. (SVHCs > 0.1% in Article).

■ Comply with REACH Annex XVII.

Guarantor

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： 陳柏宏

Company Representative Title 公司代表人職稱： QA Manager 品保經理

Date 日期： 2021 / 07 / 12

Revision Log

Rev	Date	Modification
0.1	27th May 2022	Preliminary Edition
1.0	27th May 2022	Official Released