Approval Sheet

Customer	
Product Number	M4D0-4GSSPCRG
Module speed	PC4-17000
Pin	260 pin
Cl-tRCD-tRP	15-15-15
SDRAM Operating Temp	0℃~85℃
Date	16th January 2015

Approval by Customer

P/N:

Signature:

Date:

Sales: _____ **Sr. Technical Manager: John Hsieh**

Rev 1.0

innodisk

The Total Solution For Industrial Flash Storage

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
		CL=11	CL=13	CL=15			
PC4-17000	R	1600	1866	2133	14.06	14.06	47.06

- JEDEC Standard 260-pin Small-Outline Dual In-Line Memory Module
- Intend for PC4-17000 applications
- Inputs and Outputs are SSTL-12 compatible
- V_{DD}=V_{DDQ}= 1.2 Volt (TYP)
- V_{PP}=2.5 Volt (TYP)
- V_{DDSPD}=2.2-3.6V
- Low-Power auto self-refresh (LPASR)
- SDRAMs have 16 internal banks for concurrent operation (4 Bank Group of 4 banks each)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals.
- Data bus inversion (DBI) for data bus

- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Golden Connector
- Fly-By topology
- Golden Connector
- Terminated control, command and address bus
- Programmable /CAS Latency: 11, 13, 15
- Operation temperature – (0℃~85℃)
- On-die V_{REFDQ} generation and Calibration
- On-Board EEPROM
- ECC function support
- RoHS and Halogen free *(Section 13)*

-

2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for

heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T$_{OPR}$	Operating Temperature (ambient)	0 to +55	°C	1
T$_{STG}$	Storage Temperature	-50 to +100	°C	
H$_{OPR}$	Operating Humidity (relative)	10 to 90	%	
H$_{STG}$	Storage Humidity (without condensation)	5 to 95	%	
P$_{BAR}$	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2
1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification. 2. Up to 9850 ft.				

3. SDRAM Parameters by device density

RTT_Nom Setting	Parameter		4Gb	Units
tREFI	Average periodic refresh interval	0°C≦ T$_{CASE}$≦ 85°C	7.8	µs
		85°C≦ T$_{CASE}$≦ 95°C	3.9	µs

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4. Ordering Information

DDR4 ECC SODIMM					
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank
M4D0-4GSSPCRG	4GB	PC4-17000	512Mx72	9	1

5. Pin Configurations (Front side/Back side)

DDR4 512Mx8 base ECC SODIMM

| Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VSS	2	VSS	67	DQ29	68	VSS	133	A1	134	EVENT_n, NF	199	DM5_n/ DBI5_n	200	DQS5_t
3	DQ5	4	DQ4	69	VSS	70	DQ24	135	VDD	136	VDD	201	VSS	202	VSS
5	VSS	6	VSS	71	DQ25	72	VSS	137	CK0_t	138	CK1_t/NF	203	DQ46	204	DQ47
7	DQ1	8	DQ0	73	VSS	74	DQS3_c	139	CK0_c	140	CK1_c/NF	205	VSS	206	VSS
9	VSS	10	VSS	75	DM3_n/ DMI3_n	76	DQS3_t	141	VDD	142	VDD	207	DQ42	208	DQ43
11	DQS0_c	12	DM0_n/ DM10_n	77	VSS	78	VSS	143	PARITY	144	A0	209	VSS	210	VSS
13	DQS0_t	14	VSS	79	DQ30	80	DQ31	145	BA1	146	A10/AP	211	DQ52	212	DQ53
15	VSS	16	DQ6	81	VSS	82	VSS	147	VDD	148	VDD	213	VSS	214	VSS
17	DQ7	18	VSS	83	DQ26	84	DQ27	149	CS0_n	150	BA0	215	DQ49	216	DQ48
19	VSS	20	DQ2	85	VSS	86	VSS	151	WE_n/ A14	152	RAS_n/ A16	217	VSS	218	VSS
21	DQ3	22	VSS	87	CB5/NC	88	CB4/NC	153	VDD	154	VDD	219	DQS6_c	220	DM6_n/ DBI6_n
23	VSS	24	DQ12	89	VSS	90	VSS	155	ODT0	156	CAS_n/ A15	221	DQS6_t	222	VSS
25	DQ13	26	VSS	91	CB1/NC	92	CB0/NC	157	CS1_n	158	A13	223	VSS	224	DQ54
27	VSS	28	DQ8	93	VSS	94	VSS	159	VDD	160	VDD	225	DQ55	226	VSS
29	DQ9	30	VSS	95	DQS8_c	96	DM8_n/ DBI_n/NC	161	ODT1	162	C0/ CS2_n/NC	227	VSS	228	DQ50
31	VSS	32	DQS1_c	97	DQS8_t	98	VSS	163	VDD	164	VREFCA	229	DQ51	230	VSS
33	DM1_n/DBI_n	34	DQS1_t	99	VSS	100	CB6/NC	165	C1, CS3_n, NC	166	SA2	231	VSS	232	DQ60
35	VSS	36	VSS	101	CB2/NC	102	VSS	167	VSS	168	VSS	233	DQ61	234	VSS
37	DQ15	38	DQ14	103	VSS	104	CB7/NC	169	DQ37	170	DQ36	235	VSS	236	DQ57
39	VSS	40	VSS	105	CB3/NC	106	VSS	171	VSS	172	VSS	237	DQ56	238	VSS
41	DQ10	42	DQ11	107	VSS	108	RESET_n	173	DQ33	174	DQ32	239	VSS	240	DQS7_c
43	VSS	44	VSS	109	CKE0	110	CKE1	175	VSS	176	VSS	241	DM7_n/ DBI7_n	242	DQS7_t
45	DQ21	46	DQ20	111	VDD	112	VDD	177	DQS4_c	178	DM4_n/ DBI4_n	243	VSS	244	VSS
47	VSS	48	VSS	113	BG1	114	ACT_n	179	DQS4_t	180	VSS	245	DQ62	246	DQ63
49	DQ17	50	DQ16	115	BG0	116	ALERT_n	181	VSS	182	DQ39	247	VSS	248	VSS
51	VSS	52	VSS	117	VDD	118	VDD	183	DQ38	184	VSS	249	DQ58	250	DQ59
53	DQS2_c	54	DM2_n/ DBI2_n	119	A12	120	A11	185	VSS	186	DQ35	251	VSS	252	VSS
55	DQS2_t	56	VSS	121	A9	122	A7	187	DQ34	188	VSS	253	SCL	254	SDA
57	VSS	58	DQ22	123	VDD	124	VDD	189	VSS	190	DQ45	255	VDDSPD	256	SA0
59	DQ23	60	VSS	125	A8	126	A5	191	DQ44	192	VSS	257	VPP	258	VTT
61	VSS	62	DQ18	127	A6	128	A4	193	VSS	194	DQ41	259	VPP	260	SA1
63	DQ19	64	VSS	129	VDD	130	VDD	195	DQ40	196	VSS				
65	VSS	66	DQ28	131	A3	132	A2	197	VSS	198	DQS5_c				

Note:
1. NC = No Connect, RFU = Reserved for Future Use
2. Address A17 is only valid for 16 Gb x4 based SDRAMs.
3. RAS_n is a multiplexed function with A16.
4. CAS_n is a multiplexed function with A15.
5. WE_n is a multiplexed function with A14.
6. CBx are available for ECC function

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6. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
Ax	SDRAM address bus	SCL	Serial Clock for temperature sensor/SPD EEPROM
A10/AP	Auto-Precharge	DQx, CBx	Data input/output and check bit input/output:
A12/BC_n	Burst Chop	DM_n/ DBI_n/TDQS_t (DMU_n, DBIU_n), (DML_n/DBII_n)	Input data mask and data bus inversion:
ACT_n	Command Input	SDA	Serial Data
BAx	Bank Address Inputs	DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	Data strobe:
BGx	Bank Group Address Inputs	ALERT_n	Alert output
C0, C1,C2 (RDIMM or LRDIMM only)	Chip ID	EVENT_n	Temperature event
CKx_t CKx_c	Clock	TDQS_t, TDQS_c (x8 DRAM-based RDIMM only)	Termination data strobe:
CKEx	Clock enable	VDD	Module power supply: 1.20V (TYP)
CSx_n	Chip Select	VPP	DRAM activating power supply: 2.5V – 0.125V / +0.250V
ODTx	On-Die Termination	VREFCA	Reference voltage for control, command, and address pins
Parity	Parity of Command and Address	VSS	Ground
RAS_n/A16 CAS_n/A15 WE_n/A14	Command Input	VTT	Power supply for termination of address, command, and control VDD/2.
RESET_n	Active LOW asynchronous reset	VDDSPD	Power supply used to power the I2C bus for SPD.
SAx	Serial address Input	RFU	Reserved for future use.
NF	No function	NC	No Connect

7. Function Block Diagram:

- (4GB, 1 Rank 512Mx8 DDR4 SDRAMs)
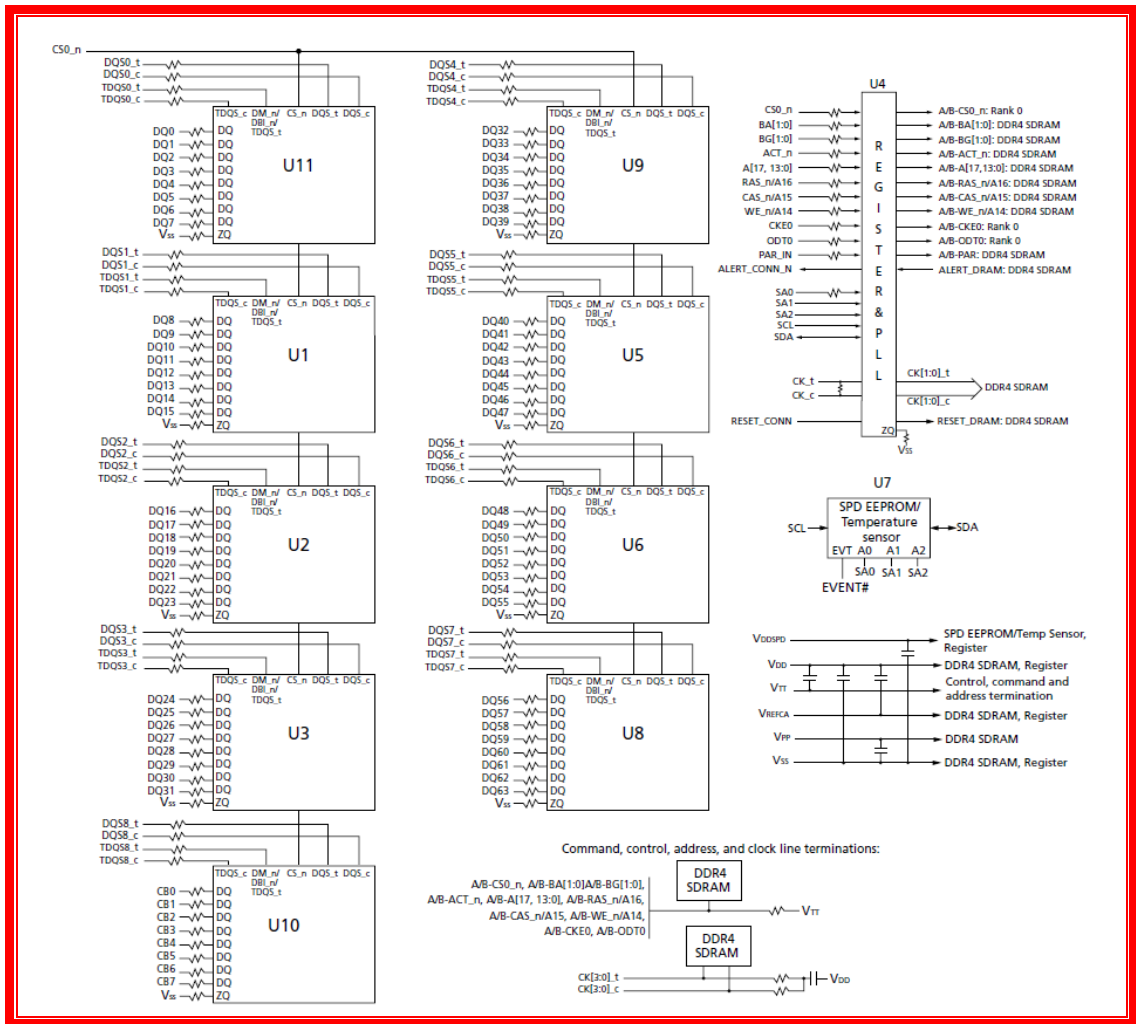
Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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8. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.3 to +1.5	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.3 to +1.5	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.3 to +1.5	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.

For measurement conditions, please refer to the JEDEC document JESD51-2.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.

3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 ℃ case temperature. Full specifications are supported in this range, but the following additional conditions apply:

  a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.

  b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

4. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

9. Module Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.4 to 1.5	V	
V_{DD}	Voltage on VDD supply relative to Vss	-0.4 to +1.5	V	1
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.4 to +1.5	V	1
V_{PP}	Voltage on VPP supply relative to Vss	-0.4 to +3.0	V	2

Note:

1. VDDQ tracks with VDD; VDDQ and VDD are tied together.

2. VPP must be greater than or equal to VDD at all times.

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10. Operating Condition

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
$V_{REFCA(DC)}$	Input reference voltage command/ address bus	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	3
I_{VTT}	Termination reference voltage (DC) – command/address bus	-750	-	750	mA	
V_{TT}	Termination Voltage	0.49 × VDD - 20mV	0.5 × VDD	0.51 × VDD + 20mV	V	4
I_I	Input leakage current; any input excluding ZQ; 0V < VIN < 1.1V	-2.0	-	2.0	µA	5
$I_{I/O}$	DQ leakage; 0V < Vin < VDD	-4.0	-	4.0	µA	5
I_{OZpd}	Output leakage current; VOUT = VDD; DQ is disabled	-	-	5.0	µA	5,6
I_{OZpu}	Output leakage current; VOUT =VSS; DQ and ODT are disabled; ODT is disabled with ODT input HIGH	V_{REF} + 0.125	-	V_{DDQ} + 0.3	µA	1
I_{OZpd}	VREFCA leakage; VREFCA = VDD/2 (after DRAM is initialized)	-2.0	-	2.0	µA	5

Note:

1. VDDQ tracks with VDD; VDDQ and VDD are tied together.

2. VPP must be greater than or equal to VDD at all times.

3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.

4. VTT termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.

5. Multiply by the number of DRAM die on the module.

6. Tied to ground. Not connected to edge connector.

11. Operating, Standby, and Refresh Currents

- 4GB SODIMM (1 Rank 512Mx8 DDR4 SDRAMs T_{CASE} = 0 °C ~ 70 °C)

Symbol	Proposed Conditions	Value		Units
		IDD Max.	IPP Max.	
IDD0	Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n:stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2;ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	315	36	mA
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0	350	36	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stableat 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	405	36	mA
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1	450	36	mA
IDD2N	Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banksclosed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	170	27	mA
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N	225	27	mA

IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern	180	27	mA
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled3	135	27	mA
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled3	180	27	mA
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled3	135	27	mA
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled3	135	27	mA
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	100	27	mA
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	160	27	mA
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern	295	27	mA

IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N	340	27	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	145	27	mA
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	945	27	mA
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R	980	27	mA
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled3, Other conditions: see IDD4R	955	27	mA
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	730	27	mA
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W	775	27	mA
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions: see IDD4W	745	27	mA

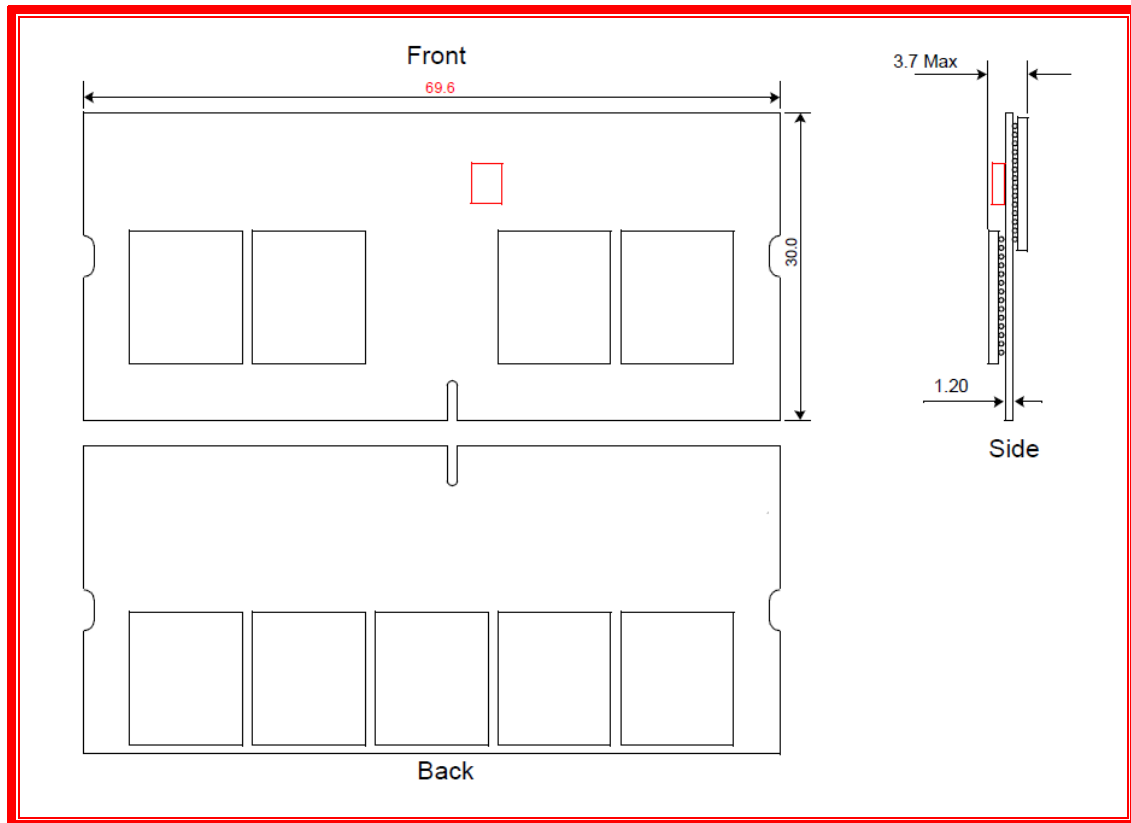|					
IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled3, Other conditions: see IDD4W	675	27	mA
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled3, Other conditions: see IDD4W	790	27	mA
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1150	162	mA
IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B	1160	135	mA
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B	880	99	mA
IDD6N	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	115	36	mA
IDD6E	Self-Refresh Current: Extended Temperature Range) TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	145	36	mA

IDD6R	Self-Refresh Current: Reduced Temperature Range TCASE: 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	90	27	mA
IDD6A	Auto Self-Refresh Current TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	115	36	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1350	68	mA
IDD8	Maximum Power Down Current TBD	68	18	mA

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12. PACKAGE DIMENSION

- (4GB, 1 Rank 512Mx8 DDR4 base SODIMM)

Note:

1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

2. The dimensional diagram is for reference only.

13. RoHS Declaration

innodisk

Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product M4D0-4GSSPCRG/-(X) complies with the requirement of RoHS directives 2011/65/EU and 2006/12/EC.

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3rd party test reports of the component/ raw materials used in the manufacture of products.

🔱 RoHS Exemptions Applied Of 7(C)-I for Resist..

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
Cd	＜ 100 ppm
Pb	＜ 1000 ppm
Hg	＜ 1000 ppm
Chromium VI（Cr+6）	＜ 1000 ppm
Polybromodiphenyl ether（PBDE）	＜ 1000 ppm
Polybrominated Biphenyls（PBB）	＜ 1000 ppm
Perfluorooctane Sulfonate (PFOS)	Not Contained

Date issued: 2015/01/06

Manufacturer: ：Innodsk Co., Ltd.
Address：221 5F, No. 237, Sec.1 Datong
Rd., Xizhi City, New Taipei City, Taiwan

Authorized Signature：

QA Dept. Director – *Ryan Tsai*

Revision Log

Rev	Date	Modification
0.1	14th January 2015	Preliminary Edition
1.0	14th January 2015	Official Released