IEI Integration Corp.

MODEL:

# WAFER-JL-N5105

**3.5" SBC with Intel® 10nm Jasper Lake Celeron® N5105 Processor with Dual Displays, DDR4, Triple Intel® 2.5 GbE, USB3.2, M.2, SATA, COM, SoC, RoHS**

# User Manual

Rev. 1.01 - September 21, 2022

RoHS Lead Free

# Revision

| Date | Version | Changes |
|---|---|---|
| September 20, 2022 | 1.01 | Added BIOS Section<br>Added SIM Moudle Installation<br>Added M.2 Moudle Removal and Replacement |
| March 25, 2022 | 1.00 | Initial release |

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# Manual Conventions

**WARNING**

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.

**CAUTION**

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.

**NOTE**

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

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Chapter

1

# Introduction

## 1.1 Introduction

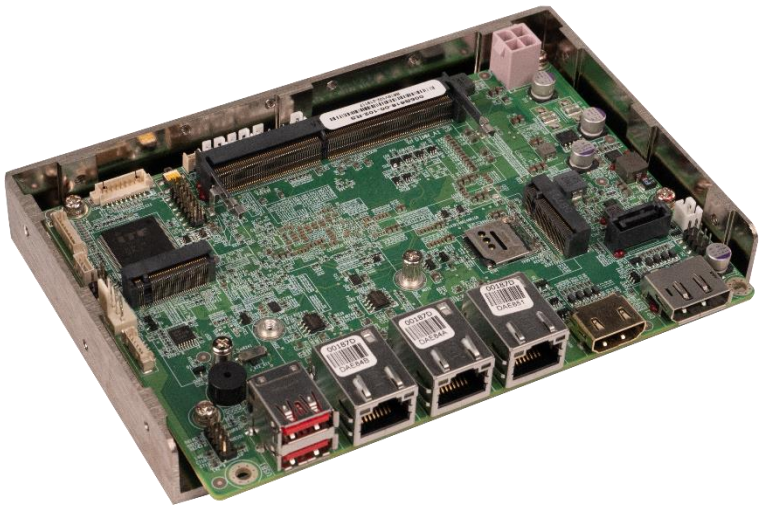


**Figure 1-1: WAFER-JL-N5105**

The WAFER-JL-N5105 is a 3.5" industrial motherboard equipped with an Intel® Celeron® N5105 quad-core Jasper Lake processor supporting 4 cores, 4 threads, turbo up-to 2.60 GHz with L3 cache, and supports one 260-pin 2933 MHz dual-channel DDR4 SDRAM SO-DIMM slot with up to 16 GB of memory.

The WAFER-JL-N5105 series includes a HDMI1.4 (up to 4096 x 2160@30Hz) connector and a DP1.4 (up to 4096 x 2160 @60Hz) connector for dual independent display.

Expansion and I/O include one M.2 A-key slot for Wi-Fi or Bluetooth expansions, one M.2 B-key slot with SIM holder for 5G module or NVMe storage expansions. Two USB 3.2 Gen 2 connectors on the rear panel, two USB 2.0 connectors by pin header and one SATA 6Gb/s connector. Serial device connectivity is provided by two internal RS-232 connectors. Three RJ-45 GbE connectors provide the system with smooth connections to an external LAN.

## 1.2 Features

Some of the WAFER-JL-N5105 motherboard features are listed below:

- Intel® Celeron® N5105 on-board SoC, 4 cores and 4 threads, 2.00GHz base frequency
- Three Intel® I225V 2.5GbE ports
- Two USB 3.2 Gen 2, two USB 2.0, two RS-232
- M.2 A key and M.2 B key expansions
- Support dual independent display via HDMI and DP

## 1.3 Connectors

The connectors on the WAFER-JL-N5105 are shown in the figure below.

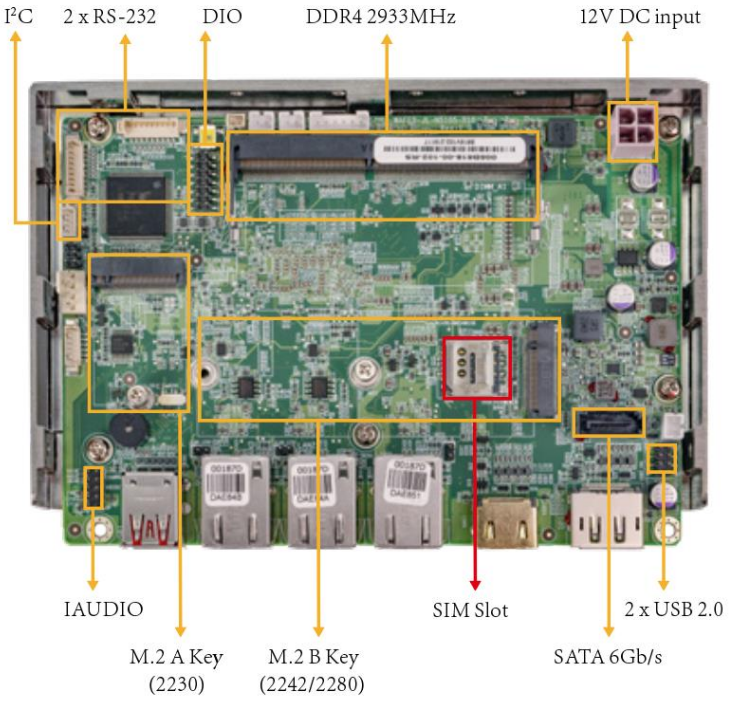



**Figure 1-2: Connectors**

## 1.4 Dimensions

The dimensions of the board are listed below:

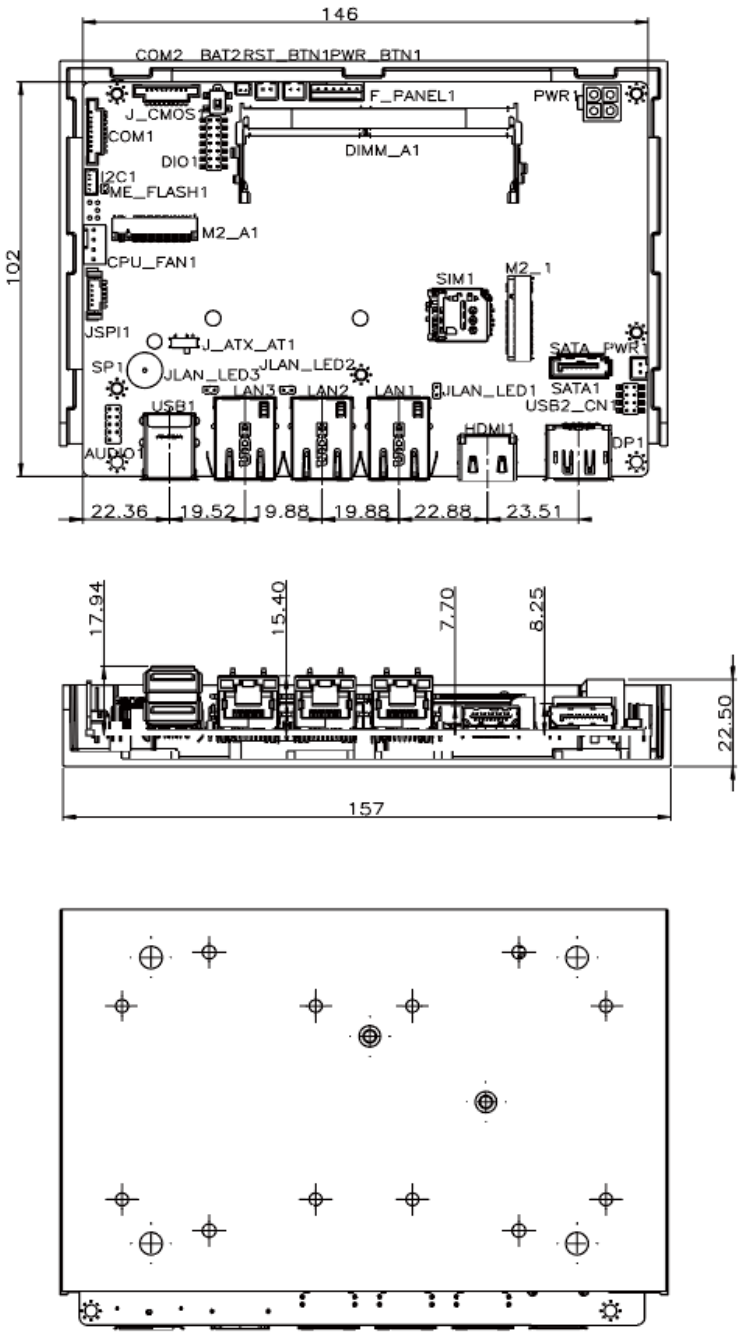



**Figure 1-3: Dimensions (mm)**

## 1.5 Data Flow

Shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

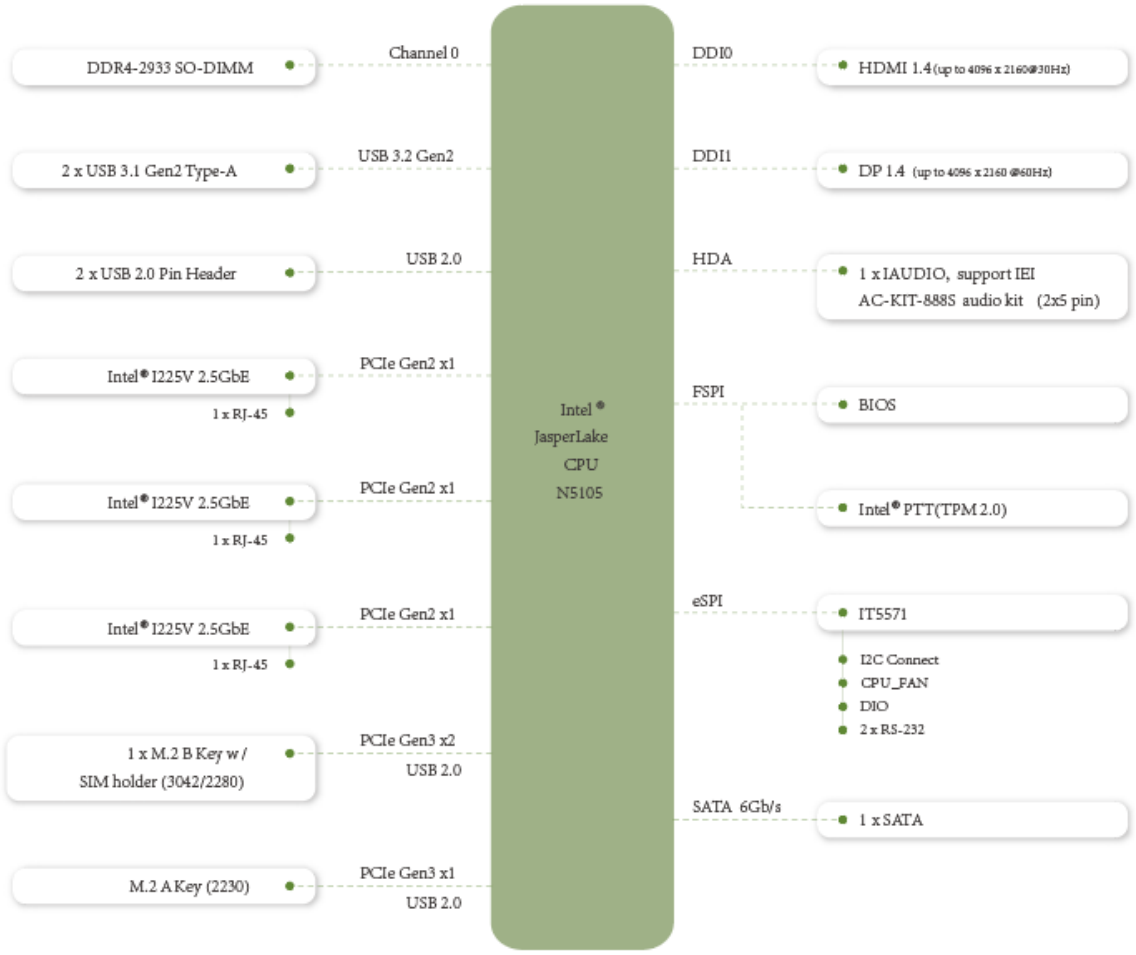



**Figure 1-4: Data Flow Diagram**

## 1.6 Technical Specifications

WAFER-JL-N5105 technical specifications are listed below.

| Specification | WAFER-JL-N5105 |
|---|---|
| **SoC** | Intel® Celeron® N5105 on-board SoC (up to 2.90GHz, Quad-core, 4M Cache, TDP=10W) |
| **BIOS** | AMI UEFI BIOS |
| **Memory** | One 260-pin 2933 MHz dual-channel DDR4 SO-DIMM (system max. 16GB) |
| **Graphics** | Intel® Gen 11 UHD Graphics |
| **Display Output** | Dual independent display<br>1 x DP 1.4 (up to 4096 x 2160 @60Hz)<br>1 x HDMI 1.4 (up to 4096 x 2160@30Hz) |
| **Ethernet** | 3 x Intel® I225V 2.5GbE controller (Colay with I225-LM) |
| **Digital I/O** | 12-bit digital I/O by 14-pin (2x7) header |
| **Embedded Controller** | ITE IT5571E |
| **Watchdog Timer** | Software programmable support 1~255 sec. system reset |
| **I/O Interface** | |
| **Audio Connector** | 1 x IAUDIO supports IEI AC-KIT-888S Audio Kit (2x5 pin) |
| **Ethernet** | 3 x RJ-45 GbE port |
| **Serial Ports** | 2 x RS-232 by 9-pin (1x9 pin, P=1.25) wafer |
| **USB Ports** | 2 x USB 3.2 Gen 2 on rear I/O<br>2 x USB 2.0 by 8-pin (2x4 pin, P=2.0) header |
| **Front Panel** | 1 x Power LED and HDD LED connector by 6-pin (1x6) wafer<br>1 x Power button connector by 2-pin wafer<br>1 x Reset button connector by 2-pin wafer |
| **LAN LED** | 3 x LAN link LED connector by 2-pin header |
| **Fan** | 1 x System Smart fan connector by 4-pin (1x4) wafer |
| **SMBus/I$^2$C** | 1 x I$^2$C connector by 4-pin (1x4) wafer |
| **Storage** | 1 x SATA 6Gb/s with 5 V SATA power connectors |

| Specification | WAFER-JL-N5105 |
|---|---|
| **Expansions** | 1 x M.2 2230 A key (PCIe Gen3 x1, USB 2.0)<br>1 x M.2 3042/2280 B key w/ SIM holder (PCIe Gen3 x2, USB 2.0) |
| **Environmental and Power Specifications** | |
| **Power Supply** | 12 V DC input only (AT/ATX support) |
| **Power Connector** | 1 x Internal power connector by 4-pin (2x2) connector |
| **Power Consumption** | 12V@2.45A (Intel® Pentium® Silver N6000 3.30 GHz TDP 6W with one 16GB 2933MHz DDR4 SO-DIMM) |
| **Operating Temperature** | 0°C ~ 60°C |
| **Storage Temperature** | -30°C ~ 70°C |
| **Humidity** | 5% ~ 95%, non-condensing |
| **Physical Specifications** | |
| **Dimensions** | 115mm x 165 mm |
| **Weight GW/NW** | 850g / 350g |

**Table 1-1: Technical Specifications**

Chapter

2

# Unpacking

## 2.1 Anti-static Precautions

**WARNING!**

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

Make sure to adhere to the following guidelines:

- ***Wear an anti-static wristband***: Wearing an anti-static wristband can prevent electrostatic discharge.
- ***Self-grounding***: Touch a grounded conductor every few minutes to discharge any excess static buildup.
- ***Use an anti-static pad***: When configuring any circuit board, place it on an anti-static mat.
- ***Only handle the edges of the PCB***: Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

## 2.2 Unpacking Precautions

When the WAFER-JL-N5105 is unpacked, please do the following:

- Follow the antistatic guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

## 2.3 Packing List

**NOTE:**

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the WAFER-JL-N5105 was purchased from or contact an IEI sales representative directly by sending an email to sales@ieiworld.com.

The WAFER-JL-N5105 is shipped with the following components:

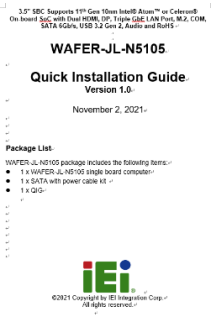
| Quantity | Item and Part Number | Image |
|---|---|---|
| 1 | WAFER-JL-N5105 single board computer |  |
| 1 | Power cable |  |
| 1 | SATA with power cable kit |  |
| 1 | Quick Installation Guide |   |

**Table 2-1: Packing List**

## 2.4 Optional Items

The following are optional components which may be separately purchased:

| Item and Part Number | Image |
|---|---|
| Dual-port USB 2.0 cable, 210mm, P=2.0<br>(**P/N** : CB-USB02A-RS) |  |
| RS-232 cable, 250 mm, p=1.25<br>(P/N : 32005-003500-200-RS) |  |
| Audio kit, 7.1 Channel<br>(P/N: AC-KIT-888S-R10) |  |
| Cooler module, 157 mm x 100 mm x 20 mm, with pad and fan<br>(P/N: 19XM0B619-0002001-000-RS) |  |
| Heatsink module, 157 mm x 100 mm x 20 mm, with pad<br>(P/N: 19XM0B619-0002002-000-RS) |  |

**Table 2-2: Optional Items**

Chapter

3

# Connectors

# 3.1 Peripheral Interface Connectors

This chapter details all the jumpers and connectors.

## 3.1.1 WAFER-JL-N5105 Layout

The figures below show all the connectors and jumpers.

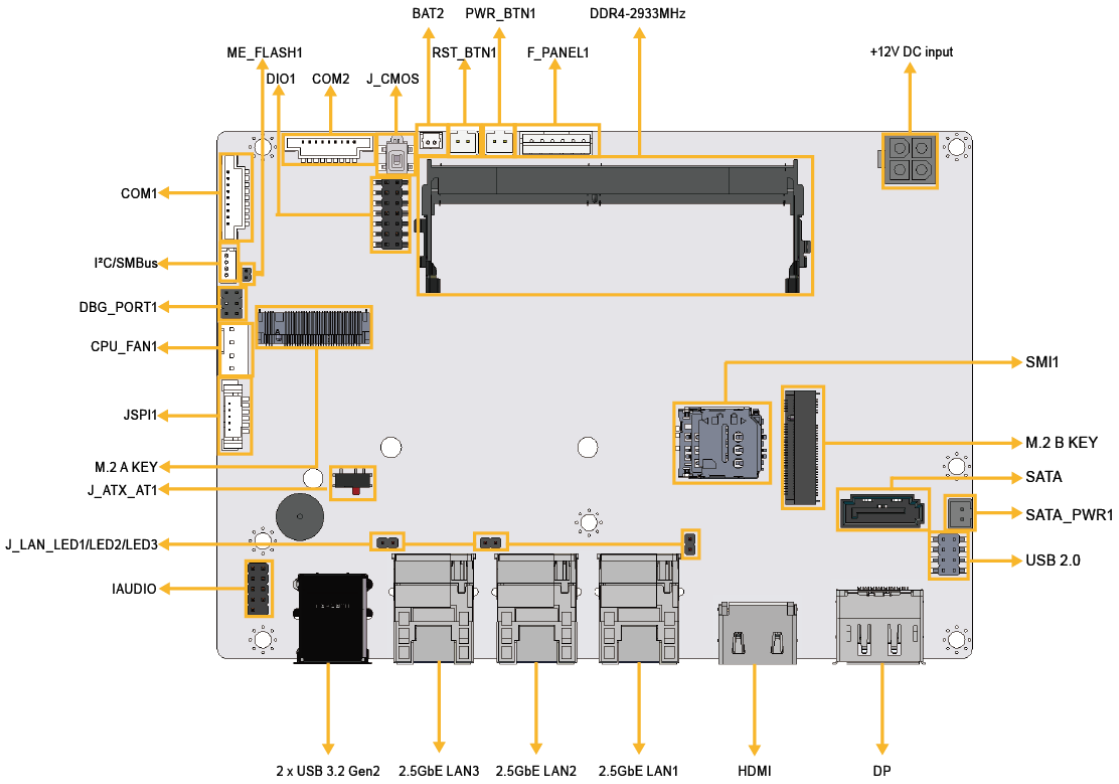



**Figure 3-1: Connector And Jumper Locations**

### 3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

| Connector | Type | Label |
|---|---|---|
| Clear CMOS button | Button | J_CMOS1 |
| AT/ATX power mode setting | 3-pin header | J_ATX_AT1 |
| ME override setting jumper | 2-pin header | ME_FLASH1 |
| Internal audio connector | 10-pin header | AUDIO1 |
| ATX 12V power connector | 4-pin Molex | PWR1 |
| Digital I/O connector | 14-pin header | DIO1 |
| Fan connector | 4-pin header | CPU_FAN1 |
| Power LED & HDD LED connector | 6-pin wafer | F_PANEL1 |
| LAN1 link LED connector | 2-pin header | JLAN_LED1 |
| LAN2 link LED connector | 2-pin header | JLAN_LED2 |
| LAN3 link LED connector | 2-pin header | JLAN_LED3 |
| Battery connector | 2-pin wafer | BAT2 |
| Power button connector | 2-pin wafer | PWR_BTN1 |
| Reset button connector | 2-pin wafer | RST_BTN1 |
| RS-232serial port connectors | 9-pin wafer | COM1, COM2 |
| SATA 6Gb/s connectors | 7-pin SATA connector | SATA1 |
| SATA power connector | 2-pin wafer | SATA_PWR1 |
| I2C connector | 4-pin wafer | I2C1 |
| Flash SPI ROM connector | 6-pin wafer | JSPI1 |
| Internal USB 2.0 connector | 8-pin header | USB2_CN1 |
| M.2 B-key slot | M.2 B-key slot | M2_1 |
| M.2 A-key slot | M.2 A-key slot | M2_A1 |
| SIM slot | 7-pin SIM holder | SIM1 |
| DDR4 SO-DIMM Socket | 260-pin SO-DIMM | DIMM_A1 |

**Table 3-1: Peripheral Interface Connectors**

### 3.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

| Connector | Type | Label |
|---|---|---|
| External 2.5GbE RJ-45 connectors | RJ45 | LAN1, LAN2, LAN3 |
| External USB 3.2 Gen 2x1 Type-A connector | USB 3.2 Gen 2 Type-A | USB1 |
| External DisplayPort connector | DP | DP1 |
| External HDMI connector | HDMI | HDMI1 |

**Table 3-2: Rear Panel Connectors**

## 3.2 Internal Peripheral Connectors

The section describes all of the connectors on the WAFER-JL-N5105.

### 3.2.1 Clear CMOS Button

**CN Label:** **J_CMOS1**

**CN Type:** Button

**CN Location:** See Figure 3-2

**CN Pinouts:** See **Table 3-3**

To clear the CMOS Setup (for example if you have forgotten the password, you should clear the CMOS and then reset the password), you should disconnect the RTC battery and press the button for about 3 seconds. This will set back to normal operation mode.

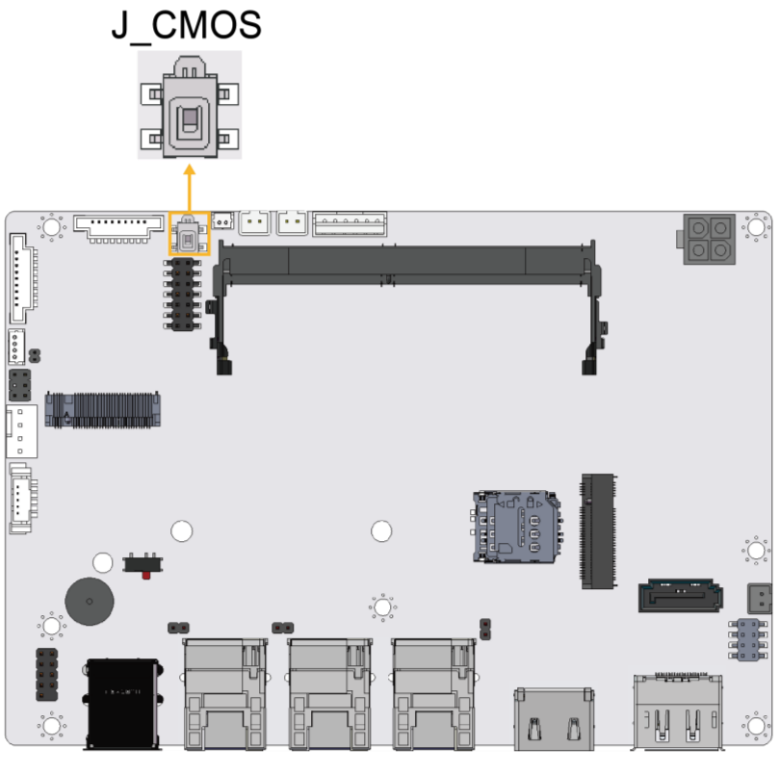



**Figure 3-2: Clear CMOS Location**

| PIN NO. | DESCRIPTION |
|---|---|
| NC (default) | Keep CMOS Setup<br>(Normal Operation) |
| Press button | Clear CMOS Setup |

**Table 3-3: Clear CMOS Pinouts**

### 3.2.2 AT/ATX Power Mode Setting

**CN Label:** **J_ATX_AT1**

**CN Type:** 3-pin switch

**CN Location:** See **Figure 3-3**

**CN Pinouts:** See Table 3-4

The AT/ATX power mode selection is made through the AT/ATX power mode switch which is shown in Figure3-3.

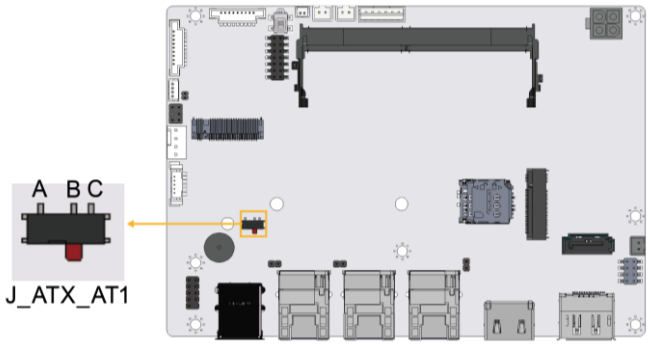



**Figure 3-3: AT/ATX Power Mode Switch Locations**

| PIN NO. | DESCRIPTION |
|---|---|
| Short A - B | ATX Power Mode (default) |
| Short B – C | AT Power Mode |

**Table 3-4: AT/ATX Power Mode Switch Pinouts**

### 3.2.3 ME Override Setting Jumper

**CN Label:** **ME_FLASH1**

**CN Type:** 2-pin header,P=1.27mm

**CN Location:** See Figure 3-4

**CN Pinouts:** See **Table 3-5**

The ME_FLASH1 connector is used for Flash Descriptor Security Overide or ME Debug Mode.

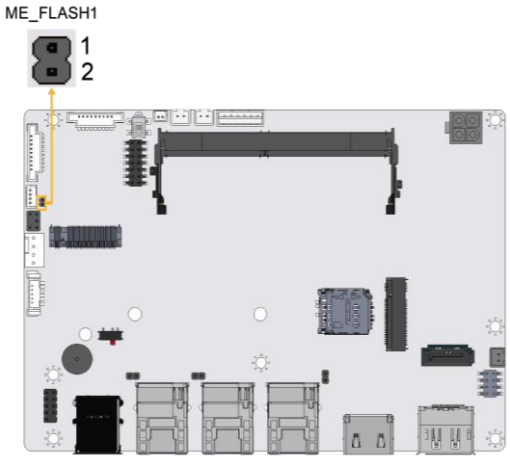



**Figure 3-4: ME Override Setting Jumper Locations**

| PIN NO. | DESCRIPTION |
|---|---|
| Open | Disable (default) |
| Short | Enable |

**Table 3-5: ME Override Setting Jumper Pinouts**

To update the ME firmware, please follow the steps below.

**Step 1:** Before turning on the system power, short the Flash Descriptor Security Override jumper.

**Step 2:** Update the BIOS and ME firmware, and then turn off the system power.

**Step 3:** Remove the metal clip on the Flash Descriptor Security Override jumper to its default setting.

**Step 4:** Restart the system. The system will reboot 2 ~ 3 times to complete the ME firmware update.

### 3.2.4 Audio Connector

**CN Label:** **AUDIO1**

**CN Type:** 10-pin header, p=2.00 mm

**CN Location:** See **Figure 3-5**

**CN Pinouts:** See **Table 3-6**

The audio connector is connected to external audio devices (AC-KIT-888S-R10) including speakers and microphones for the input and output of audio signals to and from the system.

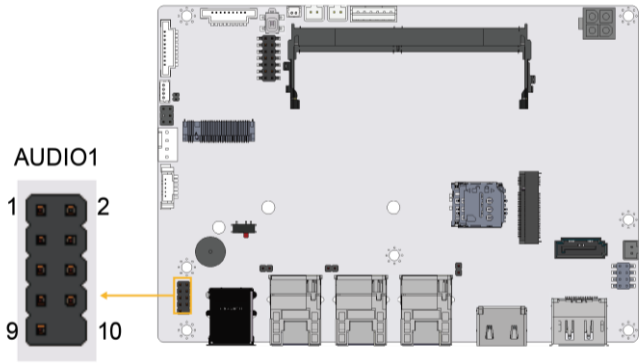



**Figure 3-5: Audio Connector Location**

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---|---|---|---|
| 1 | HDA_SYNC_R | 2 | HDA_BIT_CLK_R |
| 3 | HDA_SDOUT_R | 4 | HDA_PCBEEP_R |
| 5 | HDA_SDIN_R | 6 | HDA_RST#_R |
| 7 | P5V | 8 | GND |
| 9 | P12V | 10 | GND |

**Table 3-6: Audio Connector Pinouts**

### 3.2.5 ATX 12V Power Connector

**CN Label:** **PWR1**

**CN Type:** 4-pin Molex, p=4.2 mm

**CN Location:** See **Figure 3-6**

**CN Pinouts:** See **Table 3-7**

The connector supports the +12V power supply.

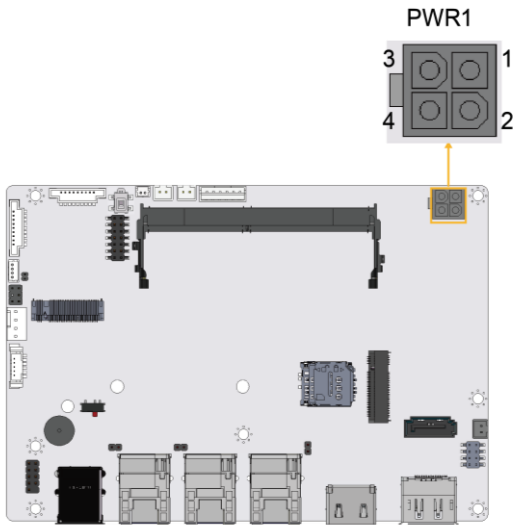



**Figure 3-6: ATX 12V Power Connector Location**

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---|---|---|---|
| 1 | GND | 2 | GND |
| 3 | +12V | 4 | +12V |

**Table 3-7: ATX 12V Power Connector Pinouts**

### 3.2.6 Digital I/O Connector

**CN Label:** **DIO1**

**CN Type:** 10-pin wafer, p=2.0 mm

**CN Location:** See **Figure 3-7**

**CN Pinouts:** See **Table 3-8**

The 12-bit digital I/O connector provides programmable input and output for external devices.

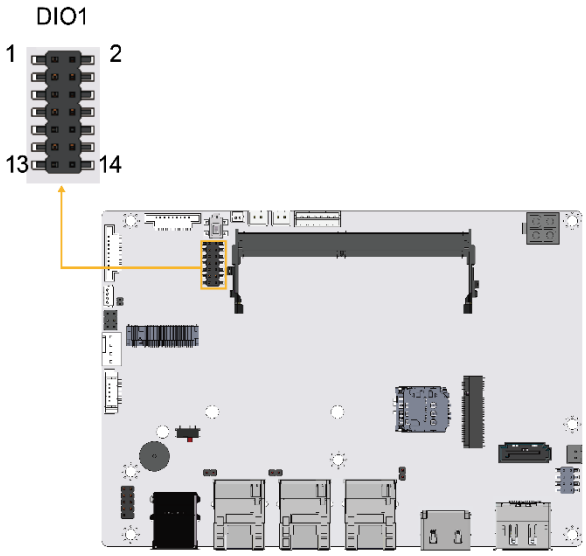



**Figure 3-7: Digital I/O Connector Location**

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---|---|---|---|
| 1 | GND | 2 | VCC |
| 3 | DOUT5 | 4 | DOUT4 |
| 5 | DOUT3 | 6 | DOUT2 |
| 7 | DOUT1 | 8 | DOUT0 |
| 9 | DIN5 | 10 | DIN4 |
| 11 | DIN3 | 12 | DIN2 |
| 13 | DIN1 | 14 | DIN0 |

**Table 3-8: Digital I/O Connector Pinouts**

### 3.2.7 Fan Connector

| | |
|---|---|
| **CN Label:** | **CPU_FAN1** |
| **CN Type:** | 4-pin wafer, p=2.54 mm |
| **CN Location:** | See **Figure 3-8** |
| **CN Pinouts:** | See **Table 3-9** |

The fan connector attaches to a smart cooling fan.

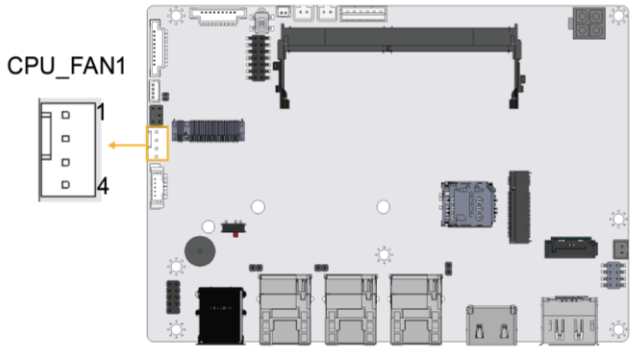



**Figure 3-8: Fan Connector Location**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | GND | 2 | +12V |
| 3 | FANIO | 4 | PWM |

**Table 3-9: Fan Connector Pinouts**

### 3.2.8 Power LED & HDD LED Connector

**CN Label:** **F_PANEL1**

**CN Type:** 6-pin wafer, p=2.00 mm

**CN Location:** See Figure 3-9

**CN Pinouts:** See **Table 3-10**

The front panel connector connects to the power LED indicator and HDD LED indicator on the system front panel.

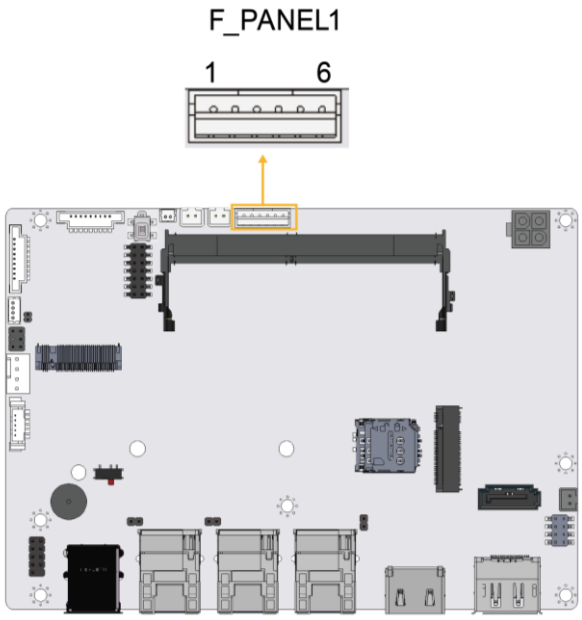



**Figure 3-9: Power LED & HDD LED Connector Location**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | VCC | 2 | GND |
| 3 | PWR_LED+ | 4 | PWR_LED- |
| 5 | HDD_LED+ | 6 | HDD_LED- |

**Table 3-10: Power LED & HDD LED Connector Pinouts**

### 3.2.9 LAN LED Connectors

**CN Label:** **JLAN_LED1, JLAN_LED2, JLAN_LED3**

**CN Type:** 2-pin header, p=2.00 mm

**CN Location:** See **Figure 3-10**

**CN Pinouts:** See **Table 3-11, Table 3-12** and **Table 3-13**

The LAN LED connectors connect to the LAN link LEDs on the system.

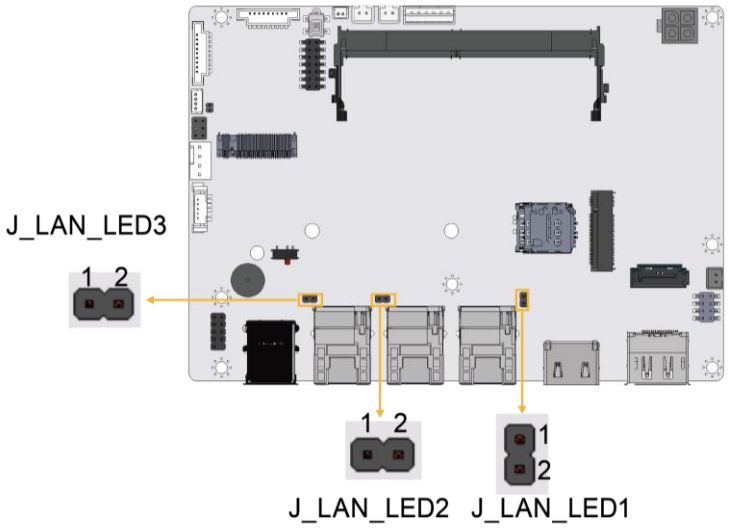



**Figure 3-10: LAN LED Connector Locations**

| Pin | Description |
|---|---|
| 1 | +3.3V |
| 2 | LAN1_LED_LNK#_ACT |

**Table 3-11: LAN1 LED Connector Pinouts**

| Pin | Description |
|---|---|
| 1 | +3.3V |
| 2 | LAN2_LED_LNK#_ACT |

**Table 3-12: LAN2 LED Connector Pinouts**

| Pin | Description |
|---|---|
| 1 | +3.3V |
| 2 | LAN3_LED_LNK#_ACT |

**Table 3-13: LAN3 LED Connector Pinouts**

### 3.2.10 Battery Connector

**CAUTION:**

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

**NOTE:**

It is recommended to attach the RTC battery onto the system chassis in which the WAFER-JL-N5105 is installed.

| | |
|---|---|
| **CN Label:** | **BAT2** |
| **CN Type:** | 2-pin wafer, p=1.25 mm |
| **CN Location:** | See **Figure 3-11** |
| **CN Pinouts:** | See **Table 3-14** |

The battery connector is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off.

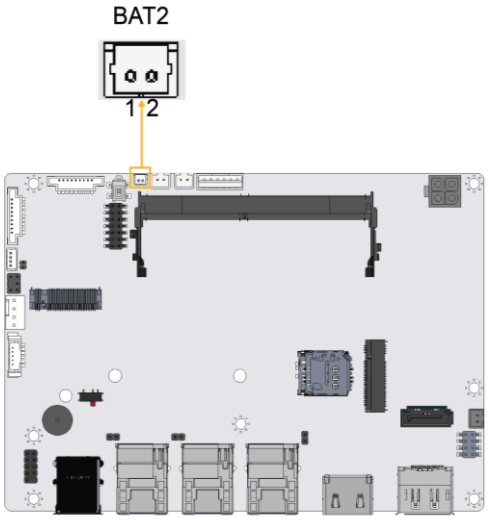



**Figure 3-11: Battery Connector Location**

| Pin | Description |
|---|---|
| 1 | VBAT+ |
| 2 | GND |

**Table 3-14: Battery Connector Pinouts**

### 3.2.11 Power Button Connector

**CN Label:** **PWR_BTN1**

**CN Type:** 2-pin wafer, p=2.00 mm

**CN Location:** See **Figure 3-12**

**CN Pinouts:** See **Table 3-15**

The power button connector is connected to a power switch on the system chassis to enable users to turn the system on and off.

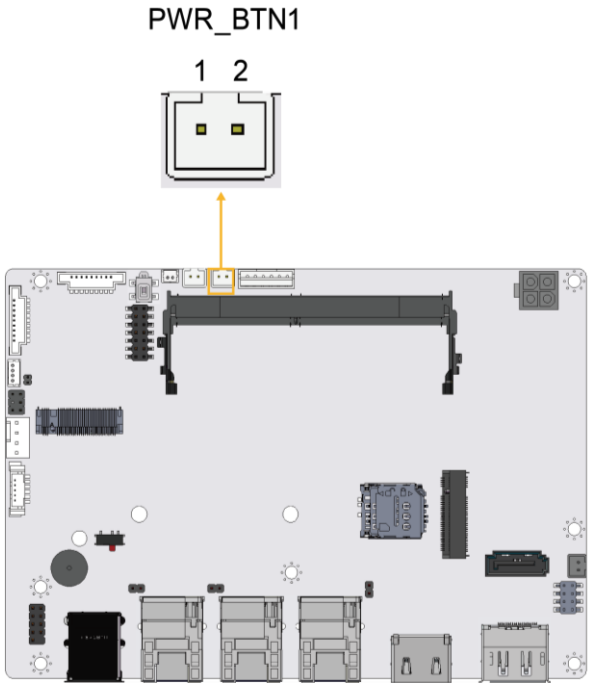



**Figure 3-12: Power Button Connector Location**

| Pin | Description |
|---|---|
| 1 | PWR_BTN+ |
| 2 | PWR_BTN- |

**Table 3-15: Power Button Connector Pinouts**

### 3.2.12 Reset Button Connector

| | |
|---|---|
| **CN Label:** | **RST_BTN1** |
| **CN Type:** | 2-pin wafer, p=2.00 mm |
| **CN Location:** | See **Figure 3-13** |
| **CN Pinouts:** | See **Table 3-16** |

The reset button connector is connected to a reset switch on the system chassis to enable users to reboot the system when the system is turned on.

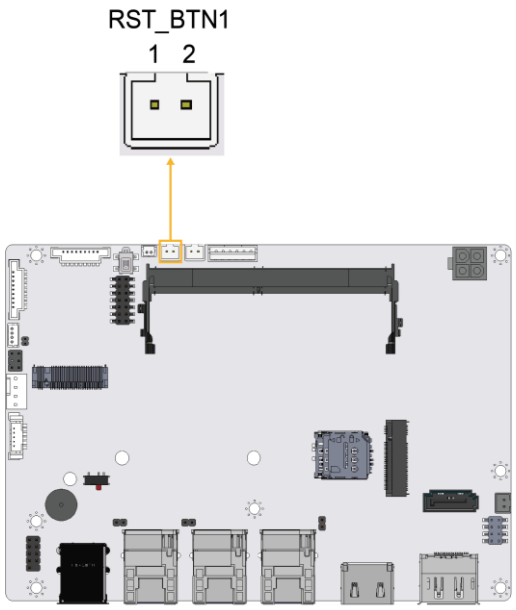



**Figure 3-13: Reset Button Connector Location**

| Pin | Description |
|---|---|
| 1 | RESET+ |
| 2 | RESET- |

**Table 3-16: Reset Button Connector Pinouts**

### 3.2.13 RS-232 Serial Port Connector

| | |
|---|---|
| **CN Label:** | **COM1,COM2** |
| **CN Type:** | 9-pin wafer, p=1.25 mm |
| **CN Location:** | See **Figure 3-14** |
| **CN Pinouts:** | See **Table 3-17** |

The serial connector provides RS-232 connection.

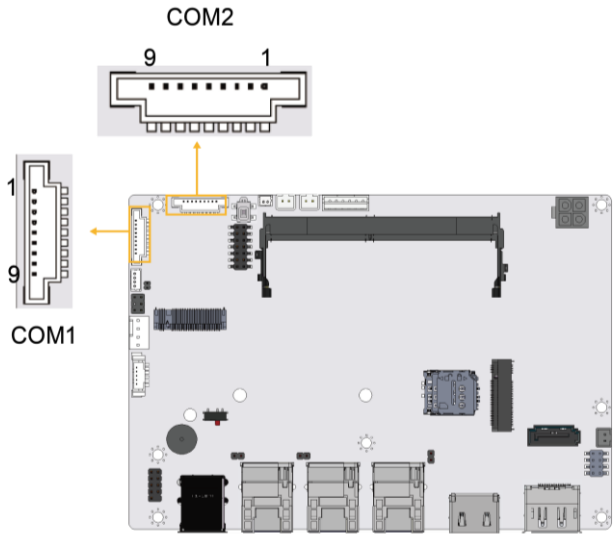



**Figure 3-14: RS-232 Serial Port Connector Location**

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---|---|---|---|
| 1 | DCD | 2 | DSR |
| 3 | RXD | 4 | RTS |
| 5 | TXD | 6 | CTS |
| 7 | DTR | 8 | RI |
| 9 | GND | | |

**Table 3-17: RS-232 Serial Port Connector Pinouts**

### 3.2.14 SATA 6Gb/s Drive Connector

| | |
|---|---|
| **CN Label:** | **SATA1** |
| **CN Type:** | 7-pin SATA connector |
| **CN Location:** | See **Figure 3-15** |
| **CN Pinouts:** | See **Table 3-18** |

The SATA 6Gb/s drive connector is connected to a SATA 6Gb/s drive. The SATA 6Gb/s drive transfers data at speeds as high as 6Gb/s.

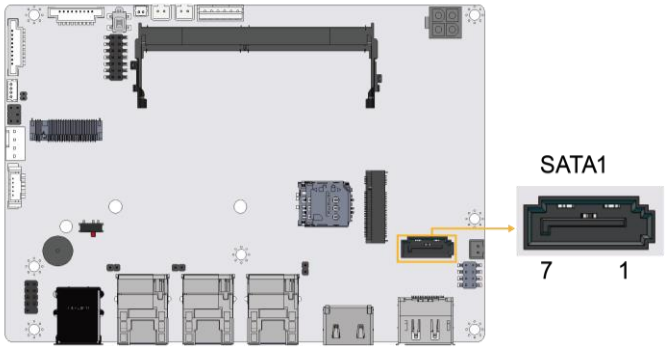



**Figure 3-15: SATA 6Gb/s Drive Connectors Location**

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---|---|---|---|
| 1 | GND | 5 | SATA_RX- |
| 2 | SATA_TX+ | 6 | SATA RX+ |
| 3 | SATA_TX- | 7 | GND |
| 4 | GND | 8 | N/C |

**Table 3-18: SATA 6Gb/s Drive Connectors Pinouts**

### 3.2.15 SATA Power Connector

| | |
|---|---|
| **CN Label:** | **SATA_PWR1** |
| **CN Type:** | 2-pin wafer, p=2.00 mm |
| **CN Location:** | See **Figure 3-16** |
| **CN Pinouts:** | See **Table 3-19** |

The SATA power connector provides +5 V power output to the SATA connector.

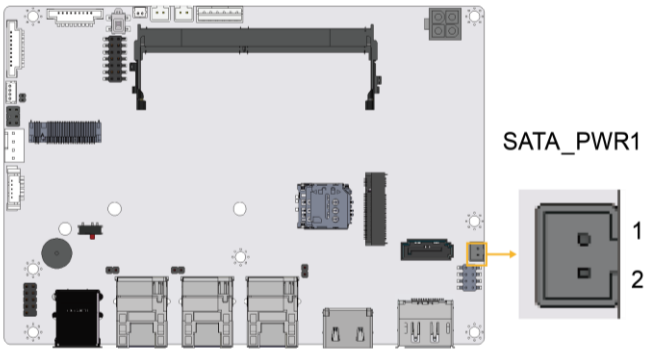



**Figure 3-16: SATA Power Connector Location**

| Pin | Description |
|---|---|
| 1 | +5V |
| 2 | GND |

**Table 3-19: SATA Power Connector Pinouts**

### 3.2.16 SMBus/I²C Connector

**CN Label:** **I2C1**

**CN Type:** 4-pin wafer, p=1.25 mm

**CN Location:** See **Figure 3-17**

**CN Pinouts:** See **Table 3-20**

The SMBus (System Management Bus) connector provides low-speed system management communications.

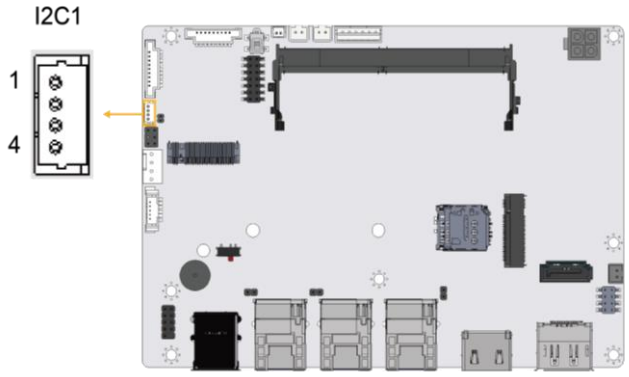



**Figure 3-17: SMBus Connector Location**

| Pin | Description |
|---|---|
| 1 | GND |
| 2 | SMB DATA |
| 3 | SMB CLK |
| 4 | +5V |

**Table 3-20: SMBus Connector Pinouts**

### 3.2.17 SPI Flash Connector

| | |
|---|---|
| **CN Label:** | **JSPI1** |
| **CN Type:** | 6-pin wafer, p=1.25 mm |
| **CN Location:** | See **Figure 3-18** |
| **CN Pinouts:** | See **Table 3-21** |

The 6-pin SPI Flash connector is used to flash the BIOS.

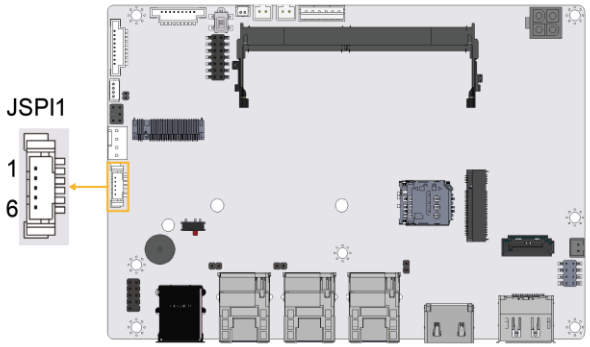



**Figure 3-18: SPI Flash Connector Location**

| Pin | Description |
|---|---|
| 1 | +3.3V |
| 2 | SPI_CS# |
| 3 | SPI SO |
| 4 | SPI CLK |
| 5 | SPI SI |
| 6 | GND |

**Table 3-21: SPI Flash Connector Pinouts**

### 3.2.18 USB 2.0 Connector

| | |
|---|---|
| **CN Label:** | **USB3** |
| **CN Type:** | 8-pin header, p=2.00 mm |
| **CN Location:** | See **Figure 3-19** |
| **CN Pinouts:** | See **Table 3-22** |

The USB connector provides two USB 2.0 ports by dual-port USB cable.

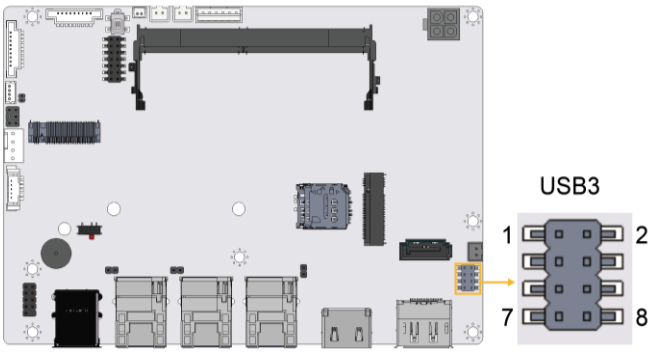



**Figure 3-19: USB Connector Location**

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---|---|---|---|
| 1 | VCC | 2 | GND |
| 3 | USB DATA- | 4 | USB DATA+ |
| 5 | USB DATA+ | 6 | USB DATA- |
| 7 | GND | 8 | VCC |

**Table 3-22: USB Connector Pinouts**

### 3.2.19 M.2 Slot, B-key

**CN Label:** **M2_1**

**CN Type:** M.2 B-key slot

**CN Location:** See **Figure 3-20**

**CN Pinouts:** See **Table 3-23**

The M.2 B key (3042/2280) slot with PCIe Gen3 x2 and USB 2.0 signal supports NVMe storage or 5G module with SIM holder

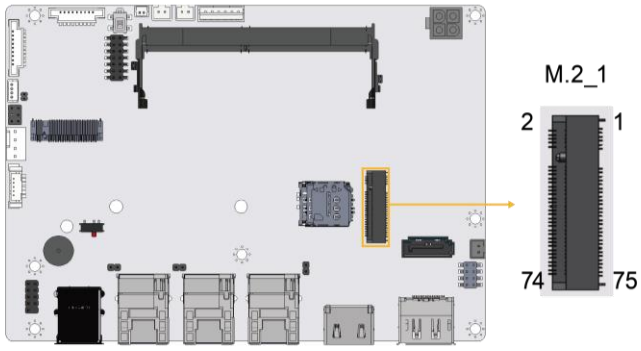



**Figure 3-20: M.2 B key Slot Location**

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---|---|---|---|
| 1 | CONFIG_3 | 2 | +3.3V |
| 3 | GND | 4 | +3.3V |
| 5 | GND | 6 | POWER_OFF |
| 7 | USB_D+ | 8 | W_DISABLE |
| 9 | USB_D- | 10 | DAS/DSS# |
| 11 | GND | 12 | Module Key |
| 13 | Module Key | 14 | Module Key |
| 15 | Module Key | 16 | Module Key |
| 17 | Module Key | 18 | Module Key |
| 19 | Module Key | 20 | N/C |
| 21 | CONFIG_0 | 22 | N/C |
| 23 | N/C | 24 | N/C |

| | | | |
|---|---|---|---|
| 25 | N/C | 26 | GNSS_DISABLE |
| 27 | GND | 28 | N/C |
| 29 | PCIE_RXN1 | 30 | UIM_RST |
| 31 | PCIE_RXP1 | 32 | UIM_CLK |
| 33 | GND | 34 | UIM_DATA |
| 35 | PCIE_TXN1 | 36 | UIM_VCC |
| 37 | PCIE_TXP1 | 38 | DEVSLP |
| 39 | GND | 40 | N/C |
| 41 | PCIE_RXN0 | 42 | N/C |
| 43 | PCIE_RXP0 | 44 | N/C |
| 45 | GND | 46 | N/C |
| 47 | PCIE_TXN0 | 48 | N/C |
| 49 | PCIE_TXP0 | 50 | PERST# |
| 51 | GND | 52 | CLKREQ# |
| 53 | REFCLKN | 54 | PEWAKE |
| 55 | REFCLKP | 56 | N/C |
| 57 | GND | 58 | N/C |
| 59 | N/C | 60 | N/C |
| 61 | N/C | 62 | N/C |
| 63 | N/C | 64 | N/C |
| 65 | N/C | 66 | N/C |
| 67 | WWAN_RST | 68 | N/C |
| 69 | PEDET | 70 | +3.3V |
| 71 | GND | 72 | +3.3V |
| 73 | GND | 74 | +3.3V |
| 75 | CONFIG_2 | | |

**Table 3-23: M. 2 B key Slot Pinouts**

### 3.2.20 M.2 Slot, A-key

**CN Label:** **M2_A1**

**CN Type:** M.2 A-key slot

**CN Location:** See **Figure 3-21**

**CN Pinouts:** See **Table 3-24**

The M.2 slot is keyed in the A position and accepts 2230 size of M.2 modules. The M.2 slot supports PCIe x2 and USB 2.0 signals.

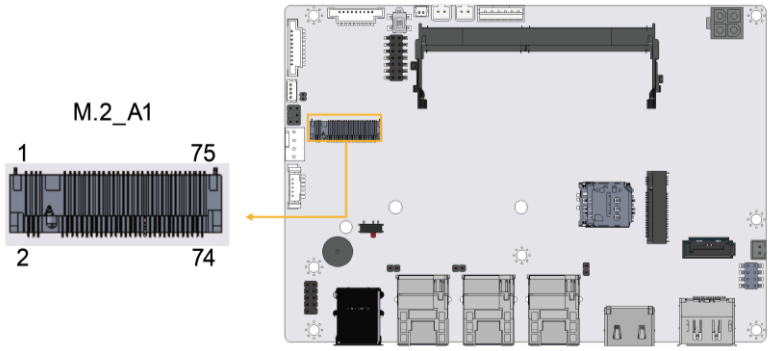



**Figure 3-21: M.2 A-key Slot Location**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | GND | 2 | +V3.3A |
| 3 | USB+ | 4 | +V3.3A |
| 5 | USB- | 6 | NC |
| 7 | GND | 8 | Module Key |
| 9 | Module Key | 10 | Module Key |
| 11 | Module Key | 12 | Module Key |
| 13 | Module Key | 14 | Module Key |
| 15 | Module Key | 16 | NC |
| 17 | NC | 18 | GND |
| 19 | NC | 20 | NC |
| 21 | NC | 22 | NC |

| Pin | Description | Pin | Description |
|---|---|---|---|
| 23 | GND | 24 | GND |
| 25 | NC | 26 | NC |
| 27 | NC | 28 | NC |
| 29 | GND | 30 | GND |
| 31 | NC | 32 | NC |
| 33 | GND | 34 | NC |
| 35 | PCIE_TX0+ | 36 | GND |
| 37 | PCIE_TX0- | 38 | NC |
| 39 | GND | 40 | NC |
| 41 | PCIE_RX0+ | 42 | NC |
| 43 | PCIE_RX0- | 44 | NC |
| 45 | GND | 46 | NC |
| 47 | CLK_PCIE0+ | 48 | NC |
| 49 | CLK_PCIE0- | 50 | NC |
| 51 | GND | 52 | BUF_PLT_RST# |
| 53 | PCIE_CLKREQ# | 54 | Pull Up +V3.3A |
| 55 | PCIE_WAKE# | 56 | Pull Up +V3.3A |
| 57 | GND | 58 | NC |
| 59 | PCIE_TX1+ | 60 | NC |
| 61 | PCIE_TX1- | 62 | NC |
| 63 | GND | 64 | NC |
| 65 | PCIE_RX1+ | 66 | NC |
| 67 | PCIE_RX1- | 68 | NC |
| 69 | GND | 70 | NC |
| 71 | CLK_PCIE1+ | 72 | +V3.3A |
| 73 | CLK_PCIE1- | 74 | +V3.3A |
| 75 | GND | | |

**Table 3-24: M.2 A-Key Slot Pinouts**

### 3.2.21 SIM Slot

**CN Label:** **SIM1**

**CN Type:** 7-PIN SIM holder

**CN Location:** See **Figure 3-22**

**CN Pinouts:** See **Table 3-25**

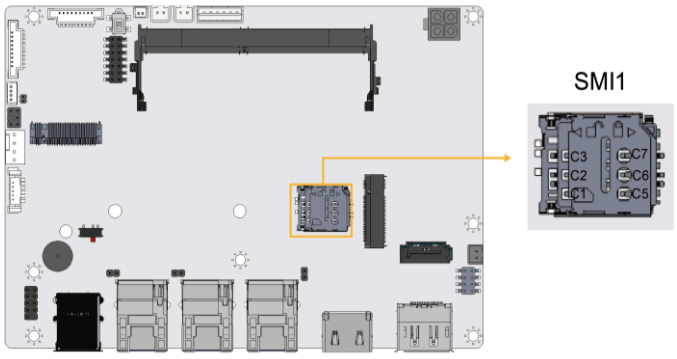



**Figure 3-22: SIM Slot Location**

| PIN NO. | DESCRIPTION |
|---|---|
| C1 | SIM_VCC |
| C2 | SIM_RST |
| C3 | SIM_Clock |
| C5 | GND |
| C6 | SIM_VPP |
| C7 | SIM_DATA |

**Table 3-25: SIM Slot Pinouts**

### 3.2.22 DDR4 SO-DIMM Socket

**CN Label:** **DIMM_A1**

**CN Type:** 260-pin DDR4 SO-DIMM socket

**CN Location:** See **Figure 3-23**

The SO-DIMM slot is for installing the DDR4 SO-DIMM.

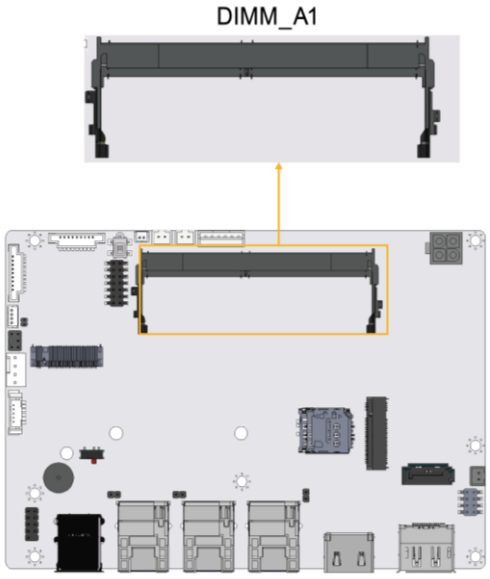



**Figure 3-23: DDR4 SO-DIMM Socket Location**

## 3.3 External Peripheral Interface Connector Panel

**Figure 3-24** shows the WAFER-JL-N5105 external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

- 1 x HDMI connector
- 1 x DP connector
- 3 x GbE RJ-45 connector
- 2 x USB 3.2 Gen 2 connector

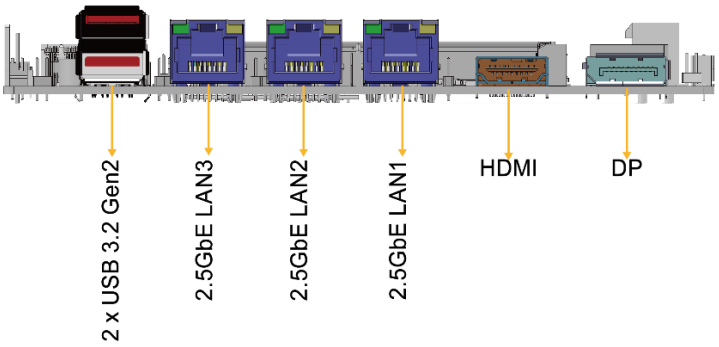



**Figure 3-24: External Peripheral Interface Connector**

### 3.3.1 External 2.5GbE RJ-45 Connectors

**CN Label:** **LAN1, LAN2, LAN3**

**CN Type:** RJ-45

**CN Location:** See **Figure 3-25**

**CN Pinouts:** See **Table 3-26**

The LAN connector connects to a local network. LAN LED location and pinouts see **Figure 3-26** and **Table 3-27.**

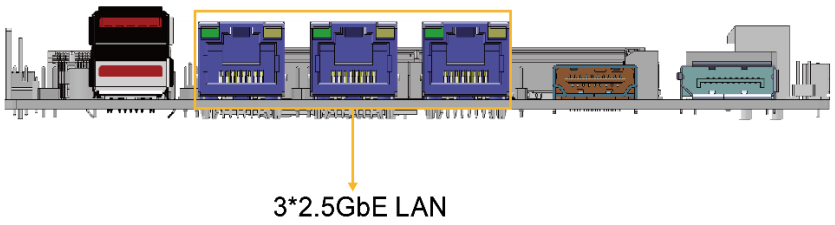



**Figure 3-25: LAN Location**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | MDI0P | 5 | MDI2P |
| 2 | MDI0N | 6 | MDI2N |
| 3 | MDI1P | 7 | MDI3P |
| 4 | MDI1N | 8 | MDI3N |

**Table 3-26: LAN Pinouts**

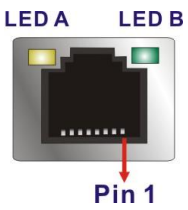



**Figure 3-26: LAN LED Location**

| LED | Description | LED | Description |
|---|---|---|---|
| A | on: linked<br>blinking: data is being sent/received | B | off: 100 Mb/s<br>orange: 1000 Mb/s<br>green: 2500 Mb/s |

**Table 3-27: LAN LED Pinouts**

### 3.3.2 External USB 3.2 Gen 2x1 Type-A

**CN Label:** **USB1, USB2**

**CN Type:** USB 3.2 Gen 2 port Type-A

**CN Location:** See **Figure 3-27**

**CN Pinouts:** See **Table 3-28**

The WAFER-JL-N5105 has four external USB 3.2 Gen 2 ports. The USB connector can be connected to a USB 2.0 or USB 3.2 device. The pinouts of USB 3.2 Gen 2 connectors are shown below.

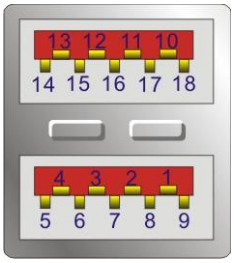



**Figure 3-27: USB 3.2 Gen 2 Port Location**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | VCC | 10 | VCC |
| 2 | USB_DATA0- | 11 | USB_DATA1- |
| 3 | USB_DATA0+ | 12 | USB_ DATA1+ |
| 4 | GND | 13 | GND |
| 5 | USB3_RX0- | 14 | USB3_RX1- |
| 6 | USB3_RX0+ | 15 | USB3_ RX1+ |
| 7 | GND | 16 | GND |
| 8 | USB3_TX0- | 17 | USB3_TX1- |
| 9 | USB3_TX0+ | 18 | USB3_TX1+ |

**Table 3-28: USB 3.2 Gen 2 Port Pinouts**

### 3.3.3 External DisplayPort Connector

**CN Label:** **DP1**

**CN Type:** External DP connector

**CN Location:** See Figure 3-28

**CN Pinouts:** See **Table 3-29**

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---|---|---|---|
| 1 | DATA_0P | 11 | GND |
| 2 | GND | 12 | DATA_3N |
| 3 | DATA_0N | 13 | CONFIG1 |
| 4 | DATA_1P | 14 | CONFIG2 |
| 5 | GND | 15 | AUX_P |
| 6 | DATA_1N | 16 | GND |
| 7 | DATA_2P | 17 | AUX_N |
| 8 | GND | 18 | DP HPD |
| 9 | DATA_2N | 19 | GND |
| 10 | DATA_3P | 20 | DP PWR |

**Table 3-29: External Display Port Connector Pinouts**

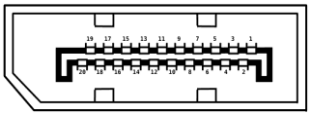


**Figure 3-28: External DisplayPort Connector Location**

### 3.3.4 External Interface Panel Connectors

**CN Label:** **HDMI1**

**CN Type:** HDMI connector

**CN Location:** See **Figure 3-29**

**CN Pinouts:** See Table 3-30

The HDMI connectors can connect to HDMI devices.

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | HDMI2_DATA2 | 2 | GND |
| 3 | HDMI2_DATA2# | 4 | HDMI2_DATA1 |
| 5 | GND | 6 | HDMI2_DATA1# |
| 7 | HDMI2_DATA0 | 8 | GND |
| 9 | HDMI2_DATA0# | 10 | HDMI2_CLK |
| 11 | GND | 12 | HDMI2_CLK# |
| 13 | N/C | 14 | N/C |
| 15 | HDMI2_SCL | 16 | HDM2I_SDA |
| 17 | GND | 18 | +5V |
| 19 | HDMI2_HPD | | |

**Table 3-30: HDMI Connector Pinouts**

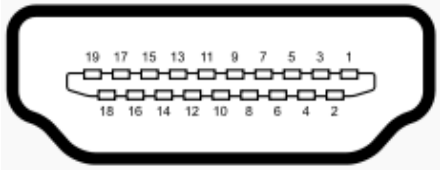



**Figure 3-29: HDMI Connector Pinout Locations**

Chapter

4

# Installation

## 4.1 Anti-static Precautions

**WARNING:**

Failure to take ESD precautions during the installation of the WAFER-JL-N5105 may result in permanent damage to the WAFER-JL-N5105 and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the WAFER-JL-N5105. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the WAFER-JL-N5105 or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- ***Wear an anti-static wristband***: Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- ***Self-grounding*** Before handling the board, touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- ***Use an anti-static pad***: When configuring the WAFER-JL-N5105, place it on an anti-static pad. This reduces the possibility of ESD damaging the WAFER-JL-N5105.
- ***Only handle the edges of the PCB***: When handling the PCB, hold the PCB by the edges.

## 4.2 Installation Considerations

**NOTE:**

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

**WARNING:**

The installation instructions described in this manual should be carefully followed in order to prevent damage to the WAFER-JL-N5105, WAFER-JL-N5105 components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
  - The user manual provides a complete description of the WAFER-JL-N5105 installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the WAFER-JL-N5105 on an antistatic pad:
  - When installing or configuring the motherboard, place it on an antistatic pad. This helps to prevent potential ESD damage.
- Turn all power to the WAFER-JL-N5105 off:
  - When working with the WAFER-JL-N5105, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the WAFER-JL-N5105 **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

## 4.3 SO-DIMM Installation

To install an SO-DIMM, please follow the steps below and refer to **Figure 4-1.**

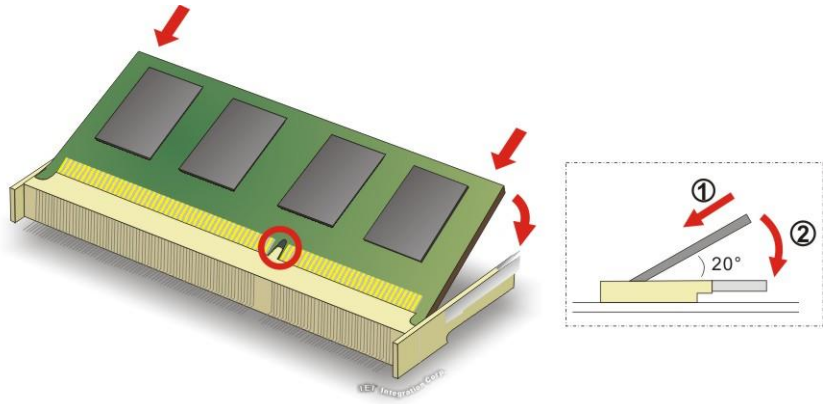



**Figure 4-1: SO-DIMM Installation**

**Step 1:** **Locate the SO-DIMM socket**. Place the board on an anti-static mat.

**Step 2:** **Align the SO-DIMM with the socket**. Align the notch on the memory with the notch on the memory socket.

**Step 3:** **Insert the SO-DIMM**. Push the memory in at a 20º angle. (See **Figure 4-1**)

**Step 4:** **Seat the SO-DIMM**. Gently push downwards and the arms clip into place. (See **Figure 4-1**)

**CAUTION**:

For dual channel configuration, always install two identical memory modules that feature the same capacity, timings, voltage, number of ranks and the same brand.

## 4.4 M.2 Module Installation

### 4.4.1 Installing M.2 Module

To install an M.2 module, please follow the steps below.

**Step 1:** Locate the M.2 module slot. See **Chapter 3**.

**Step 2:** Remove the retention screw secured on the motherboard.

**Step 3:** Line up the notch on the module with the notch on the slot. Slide the M.2 module into the socket at an angle of about 20º (**Figure 4-2)**.

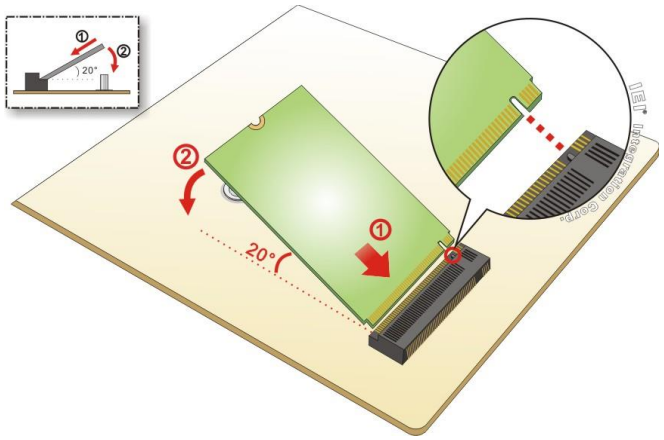



**Figure 4-2: Inserting the M.2 Module into the Slot at an Angle**

**Step 4:** Secure the M.2 module with the previously removed retention screw (**Figure 4-3**).

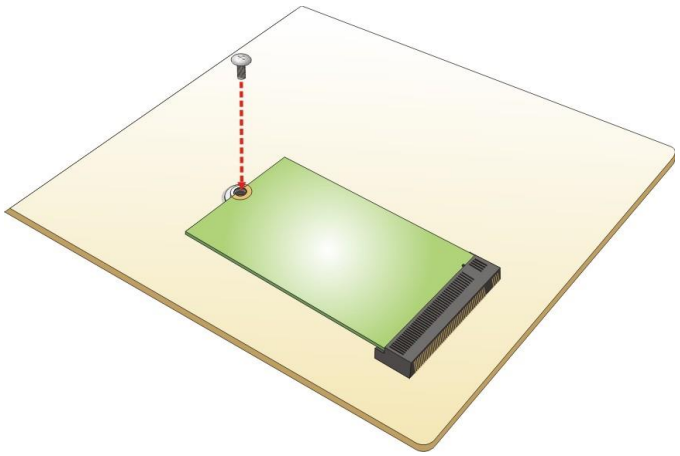


**Figure 4-3: Securing the M.2 Module**

### 4.4.2 M.2 Module Removal and Replacement

To remove the old M.2 module or replace it with other module in different sizes such as M.2 2242 to 2252/2280, please follow the steps below.

**Step 1:** To remove the M.2 module, remove the retention screw that secured the M.2 module.

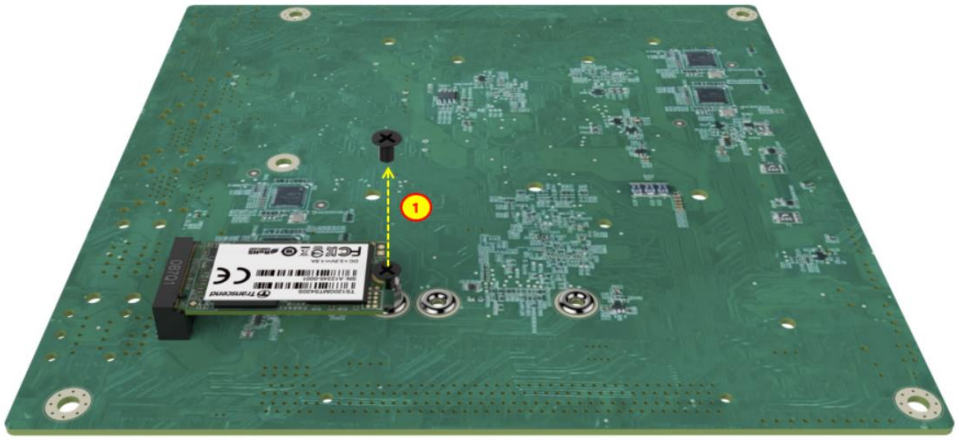



**Figure 4-4: Removing the Retention Screw**

**Step 2:** Remove the M.2 module secured on the motherboard.

**Step 3:** Use a plier or other available tools to rotate the standoff secured on the motherboard to remove it.

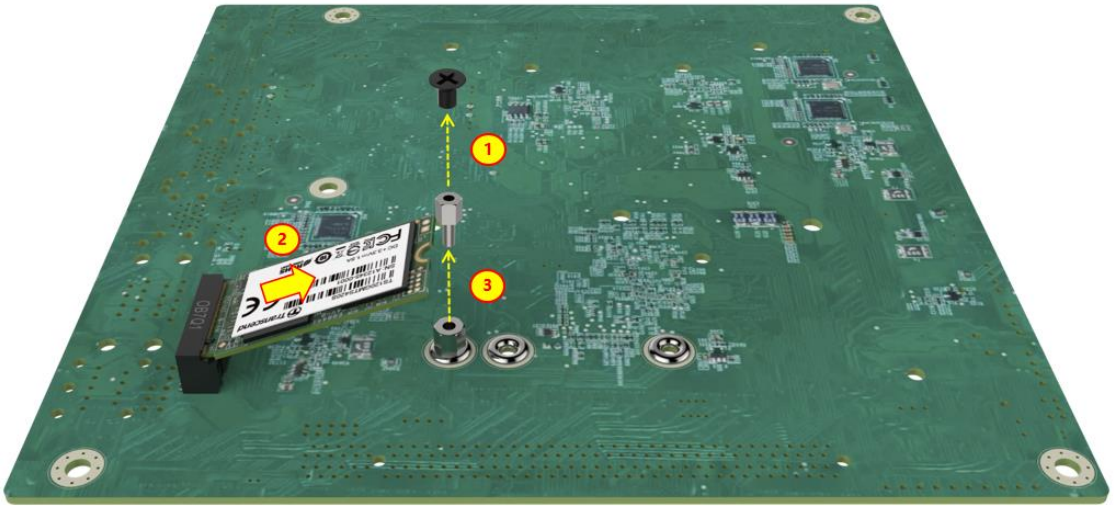



**Figure 4-5: Removing the M.2 Module and the Standoff**

#### 4.4.2.1 M.2 2252

To install an M.2 2252 module, please follow the steps below

**Step 4:** Install the previously removed standoff to the screw hole for the M.2 2252 module.

**Step 5:** Follow the instruction described in Section **4.4.1** to install the M.2 2252 module.

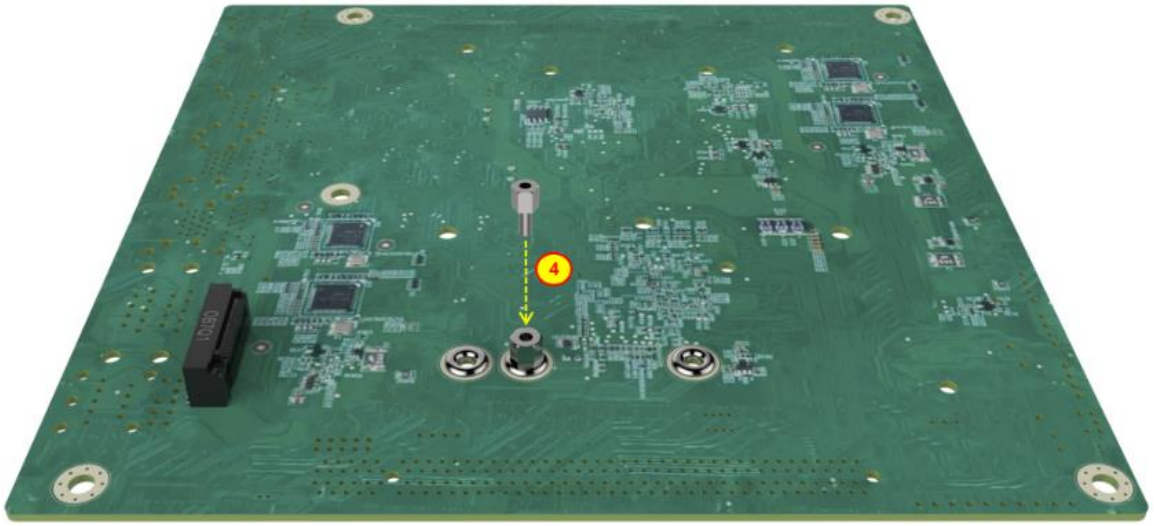



**Figure 4-6: Installing the Standoff into the 2252 Position**

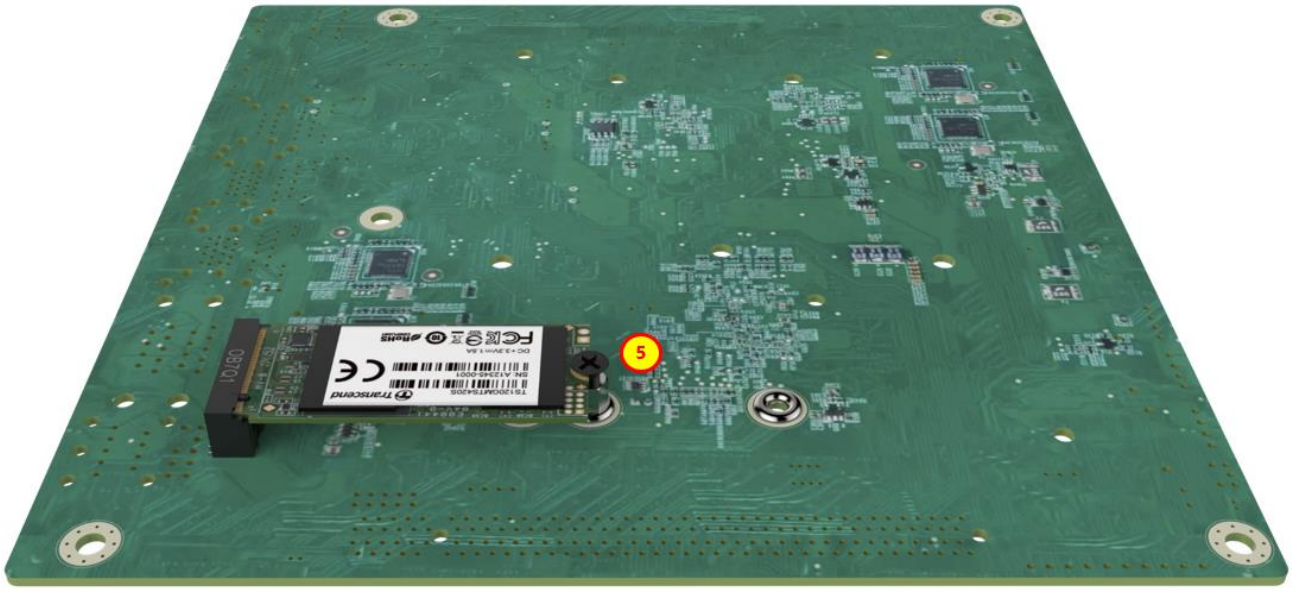



**Figure 4-7: Securing the M.2 2252 Module**

#### 4.4.2.2 M.2 2280

To install an M.2 2280 module, please follow the steps below

**Step 4:** Install the previously removed standoff to the screw hole for the M.2 2280 module.

**Step 5:** Follow the instruction described in Section **4.4.1** to install the M.2 2280 module.

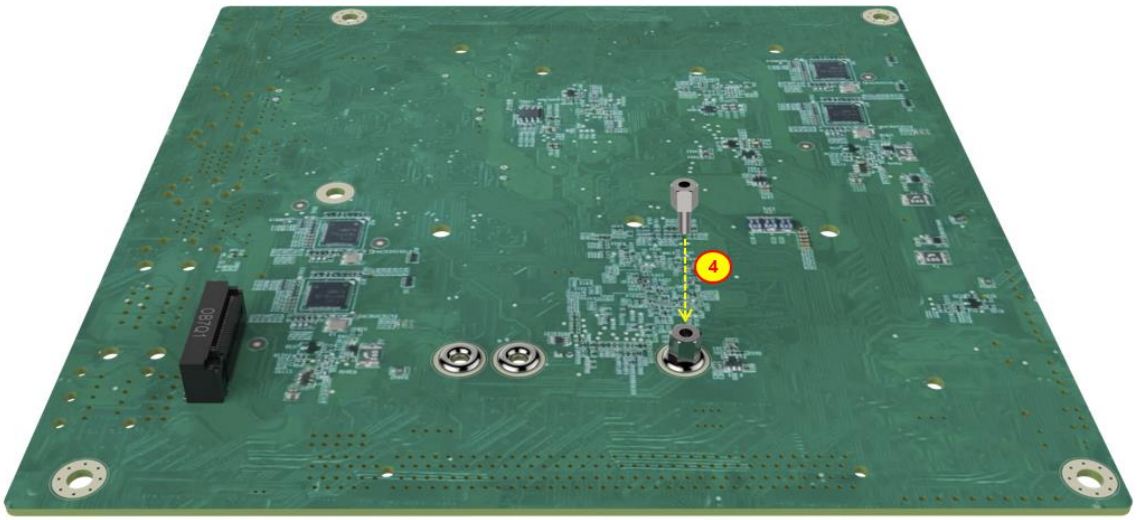



**Figure 4-8: Installing the Standoff into the 2252 Position**


**Figure 4-9: Securing the M.2 Module**

## 4.5 SIM Module Installation (Optional)

The SIM card slot allows installation of the SIM card based on M.2 B-key signals. To install a SIM card, please follow the steps below.

**Step 1:** Slide the upper cover to the release position according to the direction of the unlocking symbol **(See Figure 4-10).**

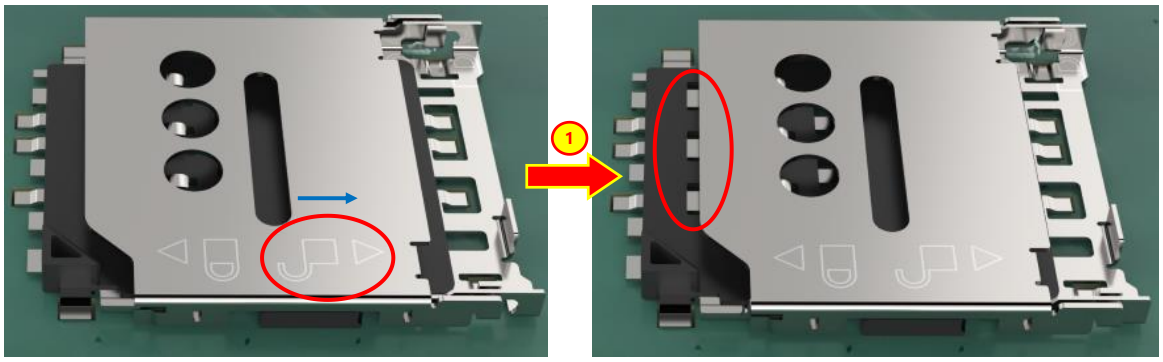



**Figure 4-10: Slide the Upper Cover to the Release Position**

**Step 2:** Open the upper cover of the SIM slot, and orient the SIM card to align with the notch of the SIM slot **(See Figure 4-11).**

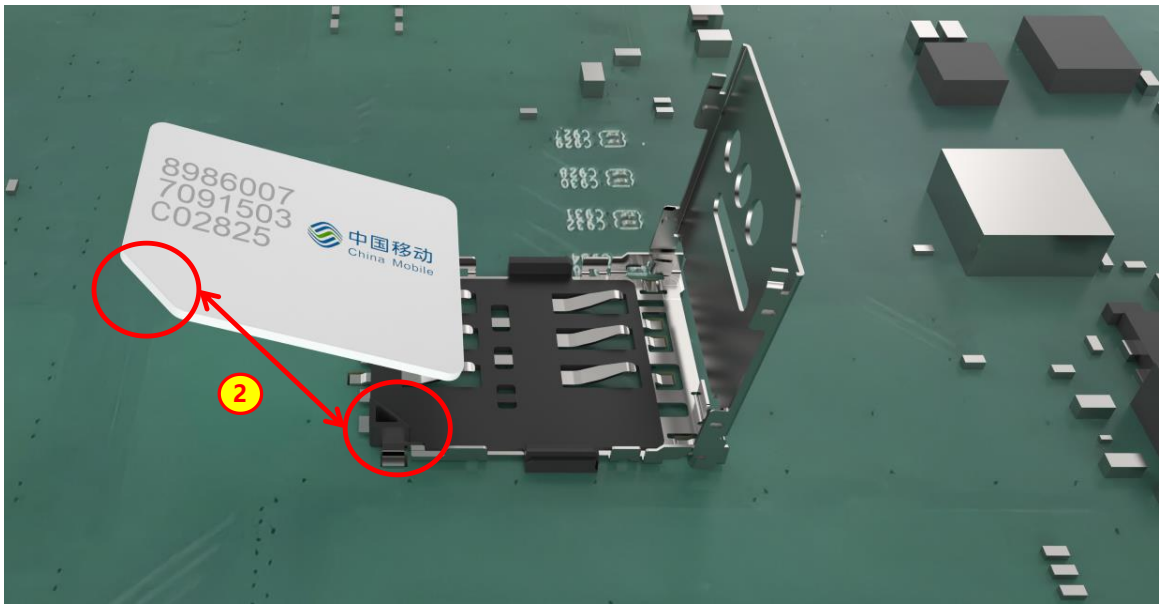



**Figure 4-11: Open the Upper Cover of the SIM Slot**

**Step 3:** Place the SIM card onto the SIM card slot, then close the upper cover of the SIM card slot **(See Figure 4-12).**

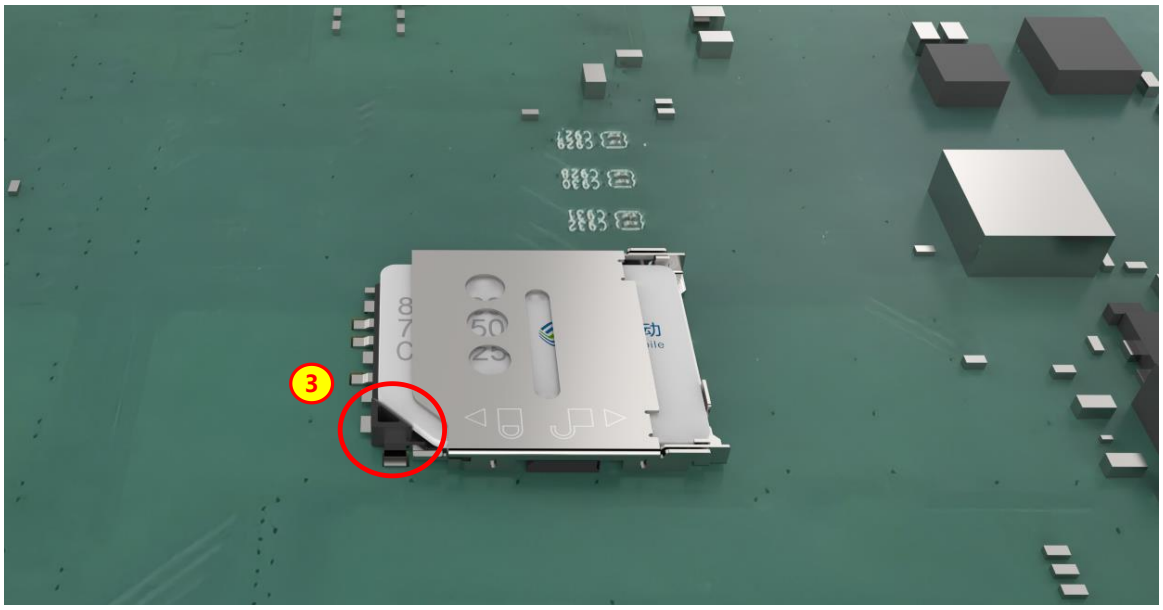



**Figure 4-12: Install the SIM Card and Close the Upper Cover**

**Step 4:** Slide the upper cover to the lock position according to the direction of the locking symbol **(See Figure 4-13).**

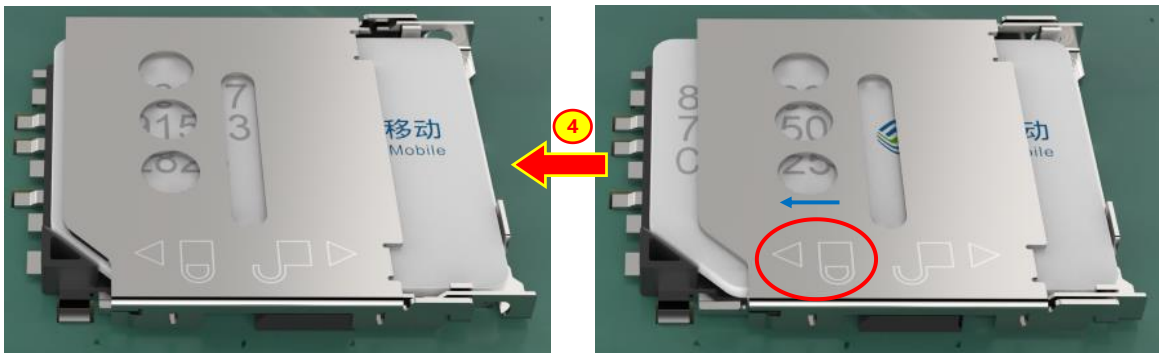



**Figure 4-13: Slide the Upper Cover to the Locking Position**

## 4.6 Chassis Installation

### 4.6.1 Heat Spreader

**WARNING:**

The heat spreader installed on the WAFER-JL-N5105 can only serve as a heat conductor, which needs additional heat dissipation mechanism to achieve suitable thermal condition. DO NOT put the WAFER-JL-N5105 with the heat spreader directly on a surface that cannot dissipate system heat, and never run the WAFER-JL-N5105 without the heat spreader secured to the board.

When the WAFER-JL-N5105 is shipped, it is secured to a heat spreader with five retention screws. The heat spreader must have a direct contact with a heat dissipation surface to ensure stable operation. In addition, a thin layer of thermal paste has to be applied onto the heat dissipation surface where it contacts the heat spreader.

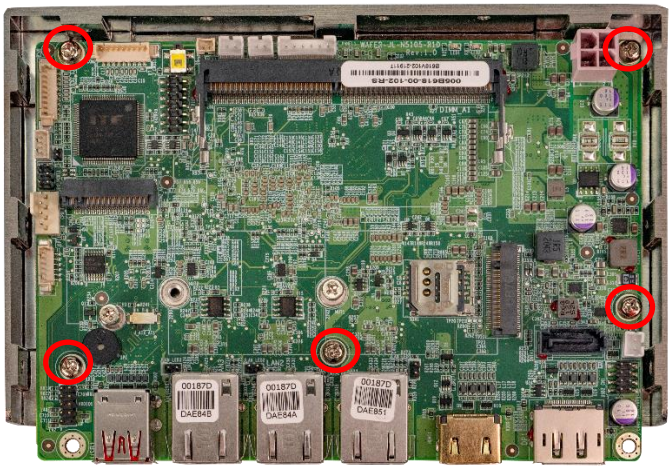


**Figure 4-14: Heat Sink Retention Screws**

IEI also provides two thermal solutions for customers to choose.

IEI has developed a highly efficient thermal solution for the 3.5" motherboard - IEI Heat Conduction Casing (IHCC). With its well-design structure, the IHCC can effectively improve heat transfer performance and cut time-to-market. It completely joints with the heat spreader for better CPU heat transfer in 0ºC–60ºC operating temperature using active cooling **(P/N: CM-WAFER-WF-R10, See Figure 4-15)**, and in 0ºC–45ºC operating temperature using passive cooling **(P/N: CM-WAFER-WOF-R10, See Figure 4-16).**

**Figure 4-15**: Active Cooling

**Figure 4-16: Passive Cooling**

### 4.6.1 Motherboard Installation

IEI recommend you to choose the DRPC-W-JL for the WAFER-JL-N5105 installation. The DRPC-W-JL is a compact embedded chassis designed for 3.5" single board computers. With its two-dimensional heat conduction and low wind resistance design on the surfaced, no extra thermal solution is needed to form the heat dissipation part. Users can get higher hardness, and benefit from the reduced production cost resulting from shortening manufacturing time. Furthermore, the height of aluminum extrusion can therefore be downsized to make the product light weight.

**Figure 4-17: DRPC-W-JL-R10**

**Figure 4-18: DRPC-W-JL-R10 with Extra Fan Cooling**

The WAFER-JL-N5105 is also well designed to fit into other chassis in the market. Each side of the heat spreader has several screw holes allowing the WAFER-JL-N5105 to be mounted into a chassis or a heat sink enclosure (please refer to Figure 1-3 for the detailed dimensions). The user has to design or select a chassis or a heat sink enclosure that has screw holes matching up with the holes on the heat spreader for installing the WAFER-JL-N5105. The following diagram shows an example of motherboard installation.

**Figure 4-19: Motherboard Installation Example**

## 4.7 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the on-board connectors

### 4.7.1 AT Power Connection

Follow the instructions below to connect the WAFER-JL-N5105 to an AT power supply.

**WARNING:**

Disconnect the power supply power cord from its AC power source to prevent a sudden power surge to the WAFER-JL-N5105.

**Step 1:** **Locate the power cable**. The power cable is shown in the packing list in **Chapter 2**.

**Step 2:** **Connect the power cable to the motherboard**. Connect the 4-pin (2x2) Molex type power cable connector to the power connector on the motherboard. **See Figure 4-20**

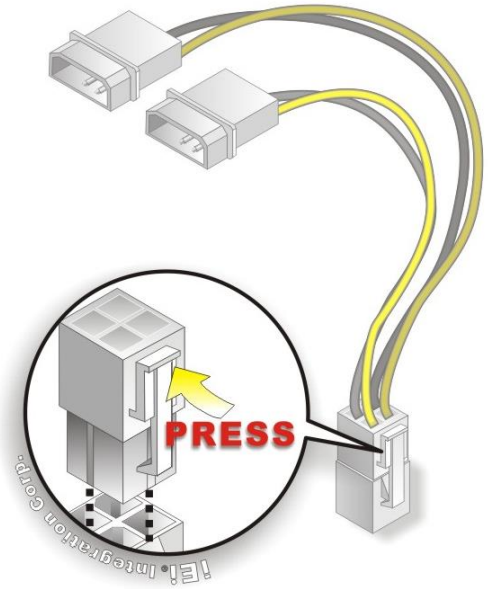



**Figure 4-20: Power Cable to Motherboard Connection**

**Step 3:** **Connect power cable to power supply**. Connect one of the 4-pin (1x4) Molex type power cable connectors to an AT power supply. **See Figure 4-21**

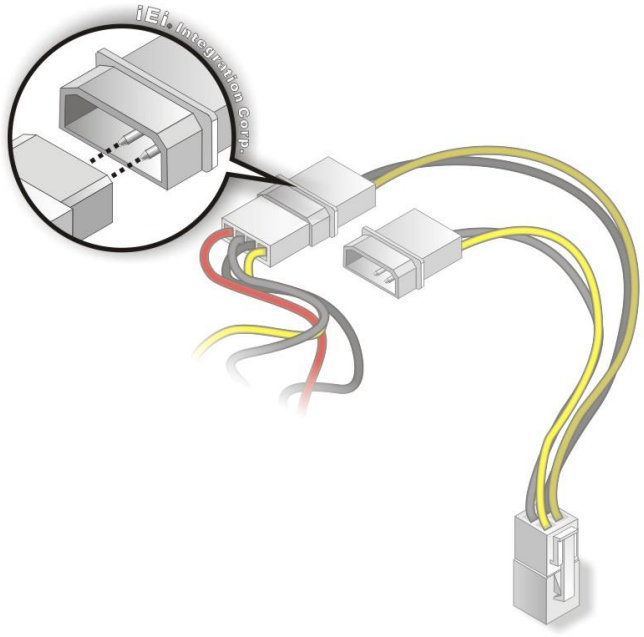


**Figure 4-21: Connect Power Cable to Power Supply**

### 4.7.2 7.1 Channel Audio Kit Installation

**NOTE:**

This item must be ordered separately, and connects to the audio connector. For further information please contact the nearest distributor, reseller or vendor or contact an IEI sales representative directly.

The audio kit attaches to the audio connector. The audio kit provides 7.1 channel audio. To install the audio kit, please refer to the steps below:

**Step 1:** **Connect the cable to the audio kit.** Connect the included cable to the audio kit. Make sure pin 1 aligns with the marked pin.

**Step 2:** **Conect the cable to the board**. Connect the other end of the cable to the board. Make sure to line up the marked pin 1.

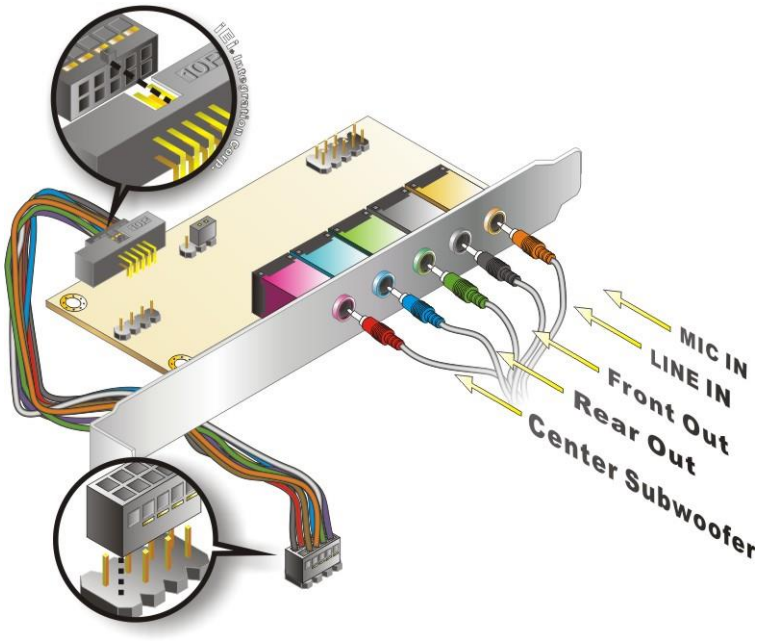



**Figure 4-22: 7.1 Channel Audio Kit**

**Step 3:** **Mount the audio kit onto the chassis**. Once the audio kit is connected to the board, secure the audio kit bracket to the system chassis.

**Step 4:** **Connect the audio devices**. Connect speakers and external audio sources to the audio jacks on the audio kit.

**Step 5:** **Install the driver**. Install the 7.1 channel audio driver included with the board.

### 4.7.3 RS-232 Cable Connection

The single RS-232 cable consists of one serial port connector attached to a serial communications cable that is then attached to a D-sub 9 male connector. To install the single RS-232 cable, please follow the steps below.

**Step 1:** **Locate the connector**. The location of the RS-232 connector is shown in **Chapter 3**.

**Step 2:** **Insert the cable connector.** Align the cable connector with the onboard connector. Make sure pin 1 on the board and connector line up. Pin 1 on the cable connector is indicated with a white dot. **See Figure 4-23.**

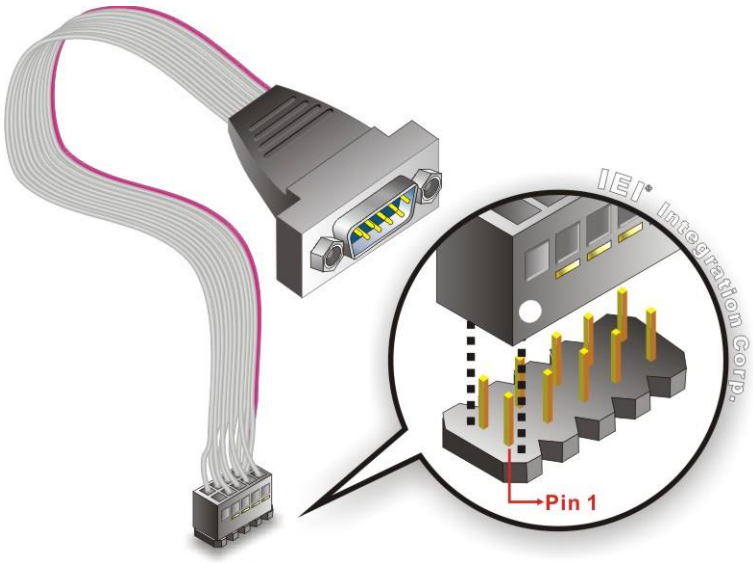



**Figure 4-23: Single RS-232 Cable Installation**

**Step 3:** **Secure the bracket**. The single RS-232 connector has two retention screws that must be secured to a chassis or bracket.

**Step 4:** **Connect the serial device**. Once the single RS-232 connector is connected to a chassis or bracket, a serial communications device can be connected to the system.

### 4.7.4 SATA Drive Connection

The WAFER-JL-N5105 is shipped with a SATA drive cable. To connect the SATA drive to the connector, please follow the steps below.

**Step 5:** **Locate the SATA connector and the SATA power connector.** The locations of the connectors are shown in **Chapter 3**.

**Step 6:** **Insert the cable connector**. Insert the cable connector into the on-board SATA drive connector and the SATA power connector. **See Figure 4-24.**

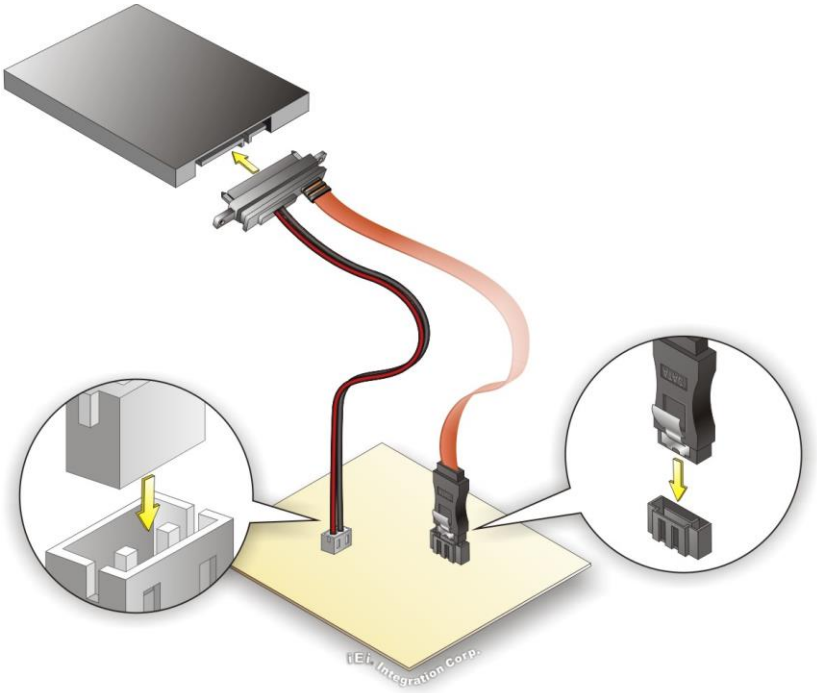


**Figure 4-24: SATA Drive Cable Connection**

**Step 7:** **Connect the cable to the SATA disk**. Connect the connector on the other end of the cable to the connector at the back of the SATA drive.

**Step 8:** To remove the SATA cable from the SATA connector, press the clip on the connector at the end of the cable.

Chapter

5

# Software Drivers

## 5.1 Available Drivers

All the drivers for the WAFER-JL-N5105 are available on IEI Resource Download Center (https://download.ieiworld.com). Type WAFER-JL-N5105 and press Enter to find all the relevant software, utilities, and documentation.

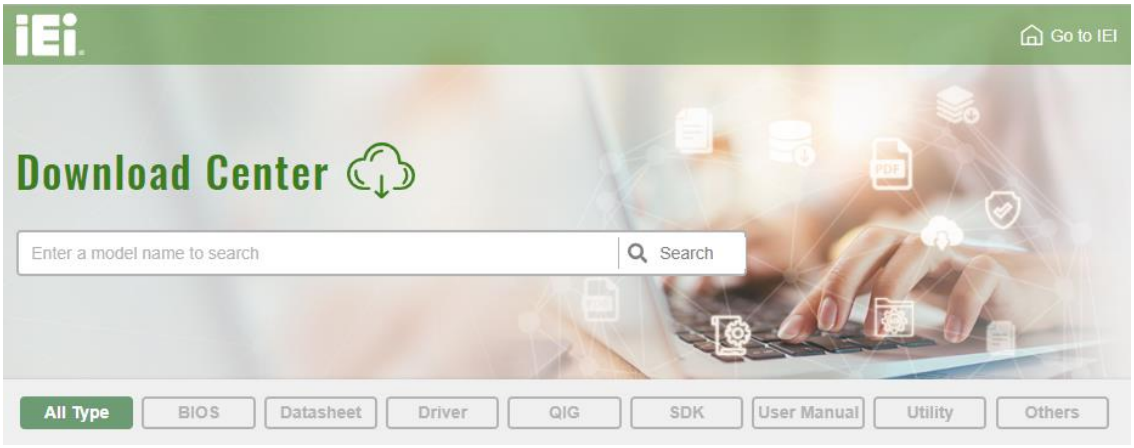
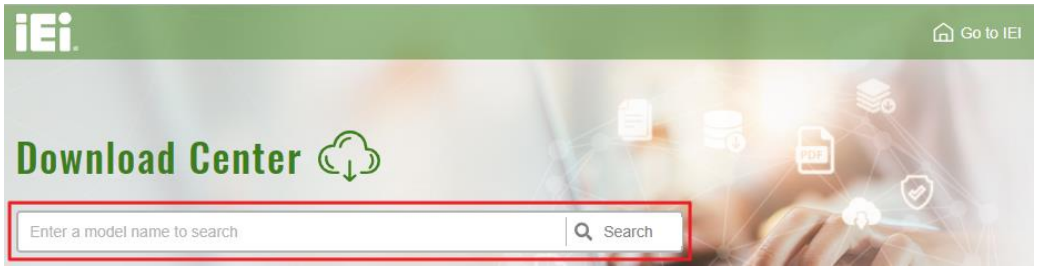



**Figure 5-1: IEI Resource Download Center**

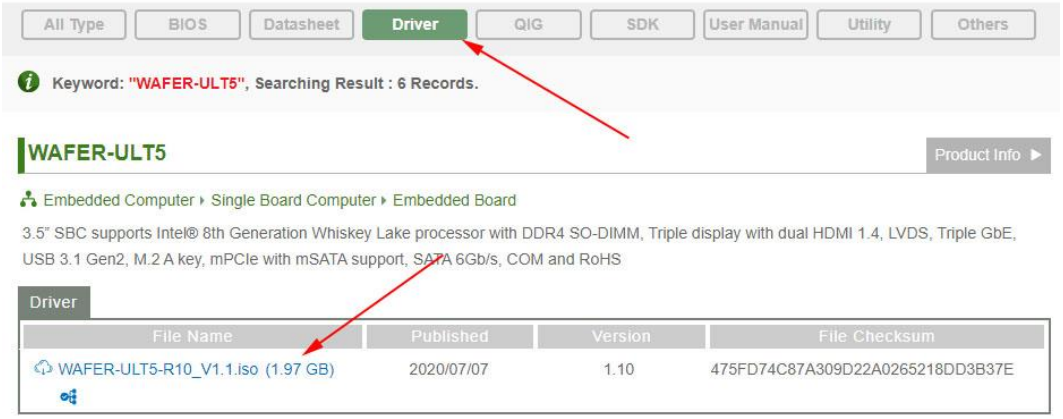
## 5.2 Driver Download

To download drivers from IEI Resource Download Center, follow the steps below.

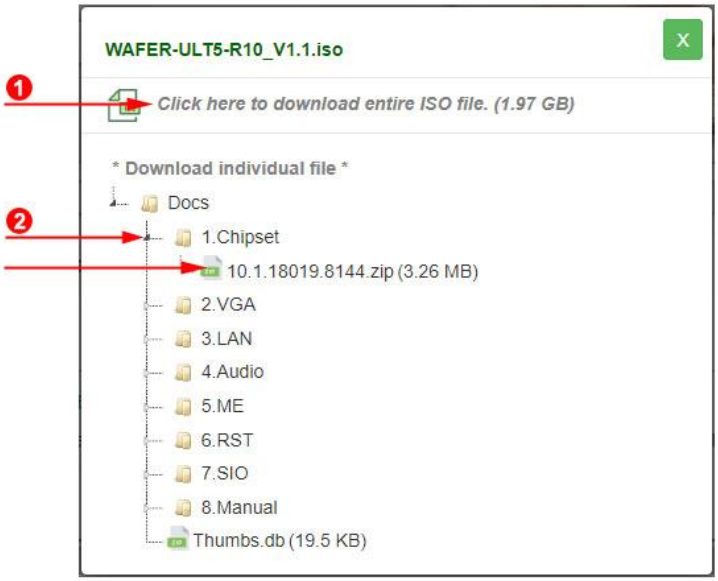
**Step 1:** Go to https://download.ieiworld.com. Type WAFER-JL-N5105 and press Enter.




**Step 2:** All product-related software, utilities, and documentation will be listed. You can choose **Driver** to filter the result.




**Step 3:** Click the driver file name on the page and you will be prompted with the following window. You can download the entire ISO file (❶), or click the small arrow to find an individual driver and click the file name to download (❷).




**NOTE:**

To install software from the downloaded ISO image file in Windows 8, 8.1 or 10, double-click the ISO file to mount it as a virtual drive to view its content.

Chapter

6

# BIOS

## 6.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.

**NOTE:**

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

### 6.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. Press the **DEL** or **F2** key as soon as the system is turned on or
2. Press the **DEL** or **F2** key when the "**Press DEL or F2 to enter SETUP**" message appears on the screen.

If the message disappears before the **DEL or F2** key is pressed, restart the computer and try again.

### 6.1.2 Using Setup

Use the arrow keys to highlight items, press **ENTER** to select, use the PageUp and PageDown keys to change entries, press **F1** for help and press **Esc** to quit. Navigation keys are shown in **Table 6-1**.

| Key | Function |
|---|---|
| Up arrow | Move to previous item |
| Down arrow | Move to next item |
| Left arrow | Move to the item on the left hand side |
| Right arrow | Move to the item on the right hand side |
| + | Increase the numeric value or make changes |
| - | Decrease the numeric value or make changes |
| Page Up | Move to the previous page |
| Page Dn | Move to the next page |
| Esc | Main Menu – Quit and not save changes into CMOS<br>Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu |
| F1 | General help, only for Status Page Setup Menu and Option Page Setup Menu |
| F2 | Load previous values |
| F3 | Load optimized defaults |
| F4 | Save changes and Exit BIOS |

**Table 6-1: BIOS Navigation Keys**

### 6.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window, press the **Esc** key.

### 6.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the clear CMOS button described in Chapter **4**.

### 6.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

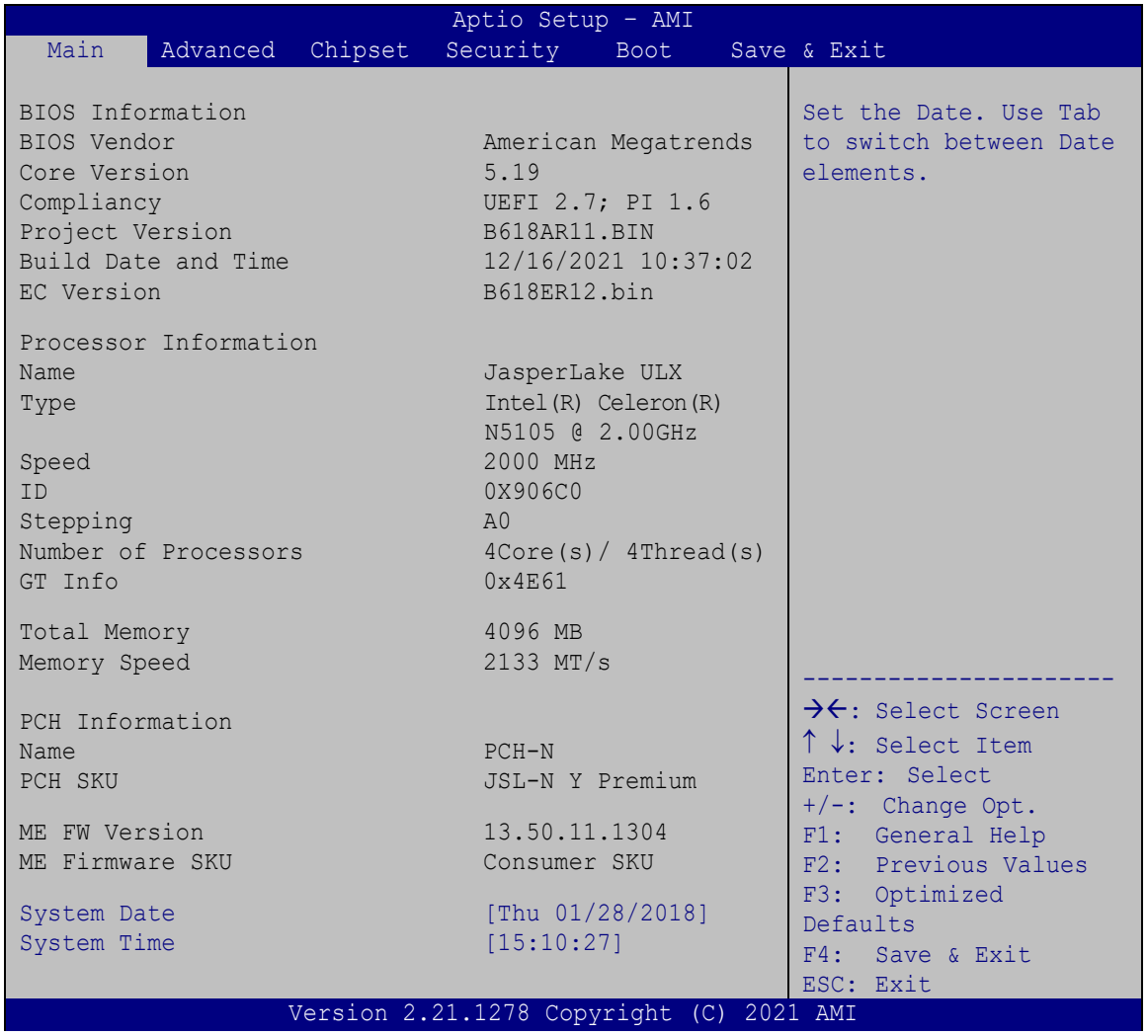
- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Security – Sets User and Supervisor Passwords.
- Boot – Changes the system boot configuration.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

## 6.2 Main

The **Main** BIOS menu (**BIOS Menu 1**) appears when the **BIOS Setup** program is entered.

The **Main** menu gives an overview of the basic system information.




**BIOS Menu 1: Main**

➔ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

➔ **System Time [xx:xx:xx]**

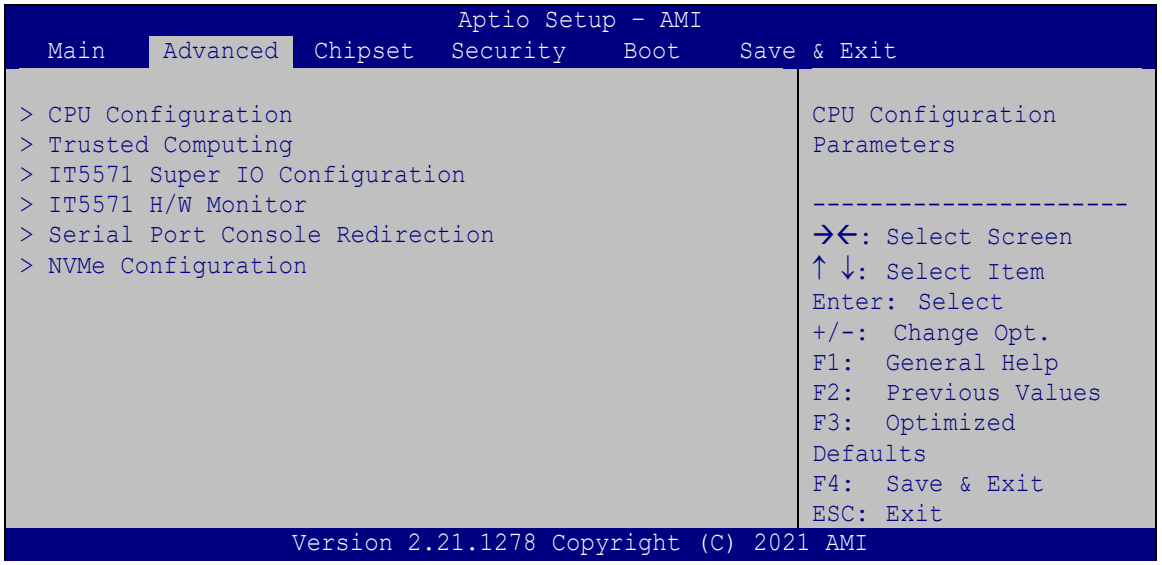
Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

## 6.3 Advanced

Use the **Advanced** menu (**BIOS Menu 2**) to configure the CPU and peripheral devices through the following sub-menus:

**WARNING!**

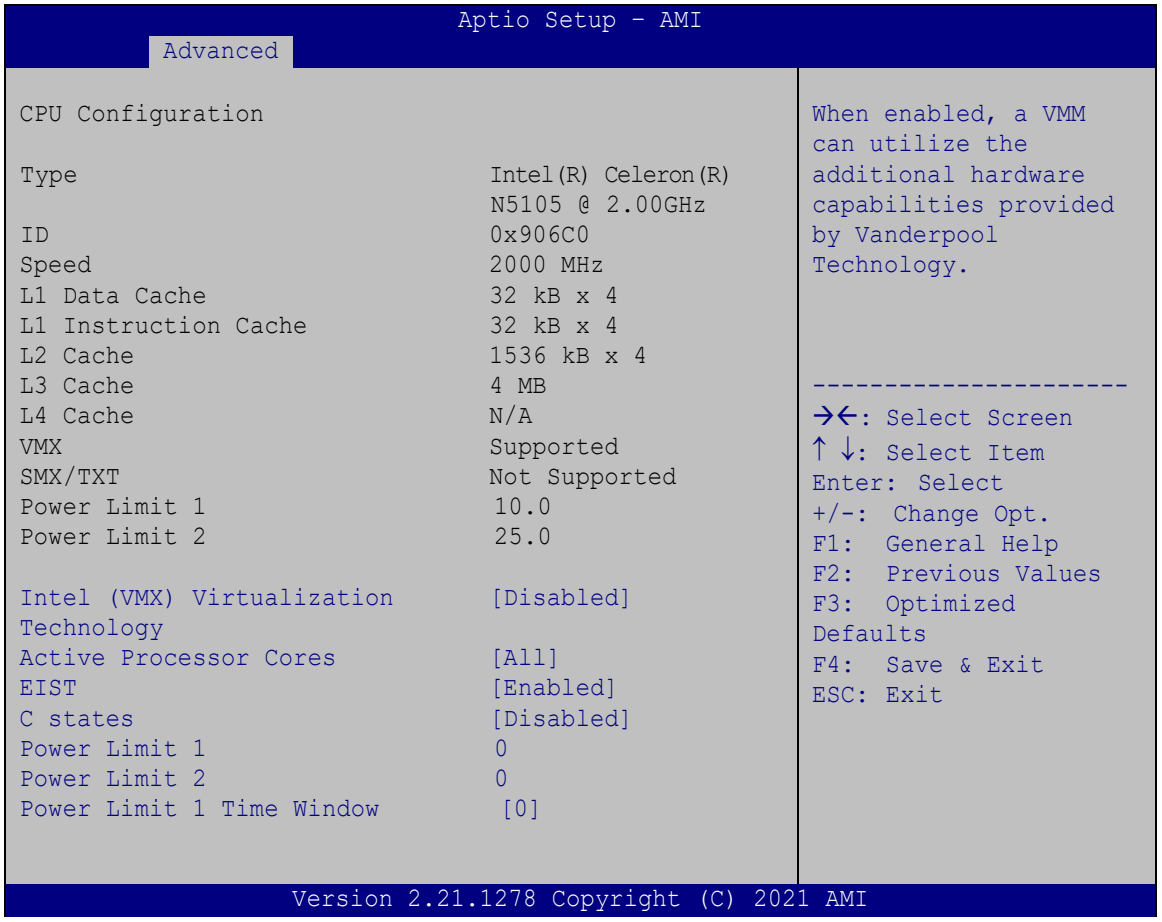
Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.




**BIOS Menu 2: Advanced**

### 6.3.1 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 3**) to view detailed CPU specifications or enable the Intel Virtualization Technology.




**BIOS Menu 3: CPU Configuration**

➔ **Intel (VMX) Virtualization Technology [Disabled]**

Use the **Intel (VMX) Virtualization Technology** option to enable or disable virtualization on the system. When combined with third party software, Intel® Virtualization technology allows several OSs to run on the same system at the same time.

| | | | |
|---|---|---|---|
| ➔ | **Disabled** | **DEFAULT** | Disables Intel Virtualization Technology. |
| ➔ | **Enabled** | | Enables Intel Virtualization Technology. |

➔ **Active Processor Cores [All]**

Use the **Active Processor Cores** BIOS option to enable numbers of cores in the processor package.

| | | | |
|---|---|---|---|
| ➔ | **All** | **DEFAULT** | Enable all cores in the processor package. |
| ➔ | **1** | | Enable one core in the processor package. |
| ➔ | **2** | | Enable two cores in the processor package. |
| ➔ | **3** | | Enable three cores in the processor package. |

➔ **EIST [Enabled]**

Use the **EIST** option to enable or disable the capability that allows more than two frequency ranges to be supported.

| | | | |
|---|---|---|---|
| ➔ | **Disabled** | | Disables the EIST Technology |
| ➔ | **Enabled** | **DEFAULT** | Enables the EIST Technology |

➔ **C states [Disabled]**

Use the **C states** option to enable or disable CPU power management which allows CPU to go to C states when it is not 100% utilized.

| | | | |
|---|---|---|---|
| ➔ | **Disabled** | **DEFAULT** | Disables CPU power management |
| ➔ | **Enabled** | | Enables CPU power management |

➔ **Power Limit 1 [0]**

Use the + or – key to change the **Power Limit 1** value. BIOS will program the default values for Limit 1 and Power Limit 1 Time Window. For 12.50W, enter 12500.

➔ **Power Limit 2 [0]**

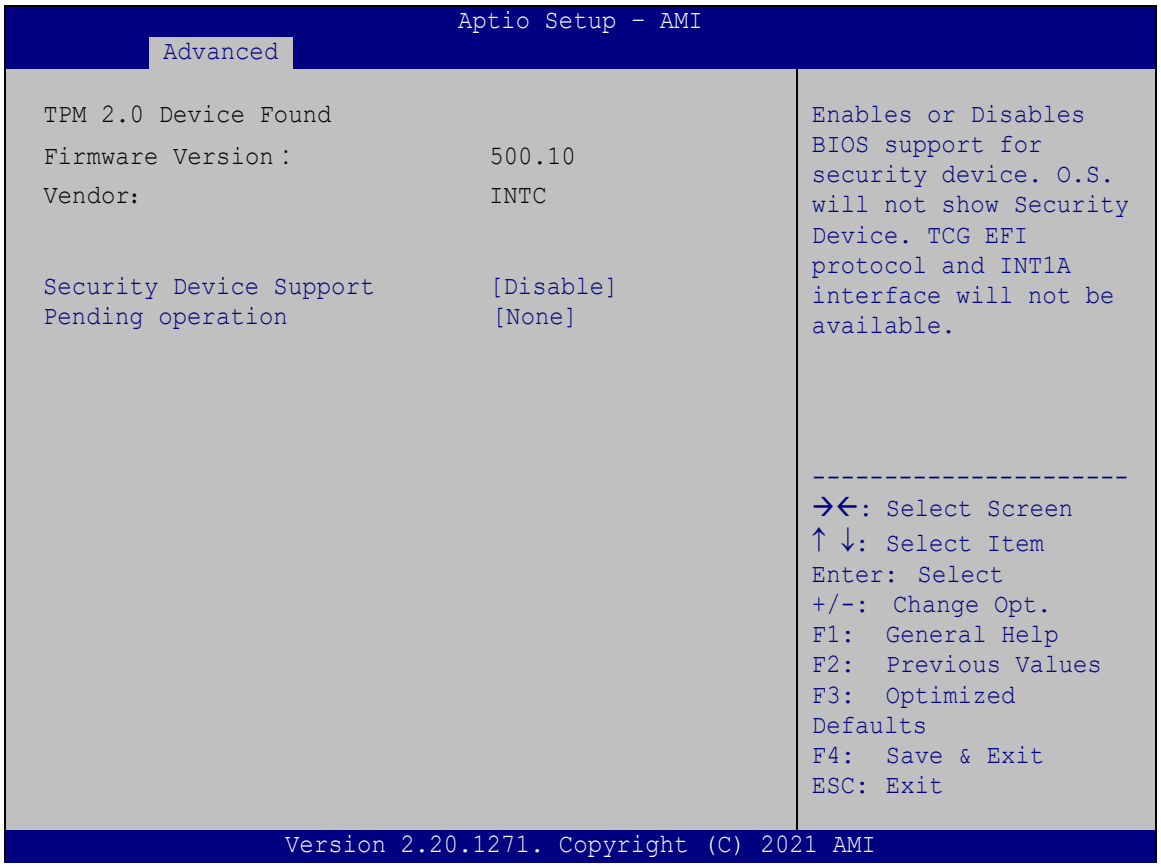
Use the + or – key to change the **Power Limit 2** value. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500.

➔ **Power Limit 1 Time Window [0]**

Use the **Power Limit 1 Time Window** option to select the PL1 time duration. The value may vary from 0 to 128. For 0 is the default value

### 6.3.2 Trusted Computing

Use the **Trusted Computing** menu (**BIOS Menu 4**) to configure settings related to the Trusted Computing Group (TCG) Trusted Platform Module (TPM).




**BIOS Menu 4: Trusted Computing**

➔ **Security Device Support [Disable]**

Use the **Security Device Support** option to configure support for the TPM.

| | | |
|---|---|---|
| ➔ **Disable** | **DEFAULT** | TPM support is disabled. |
| ➔ **Enable** | | TPM support is enabled. |

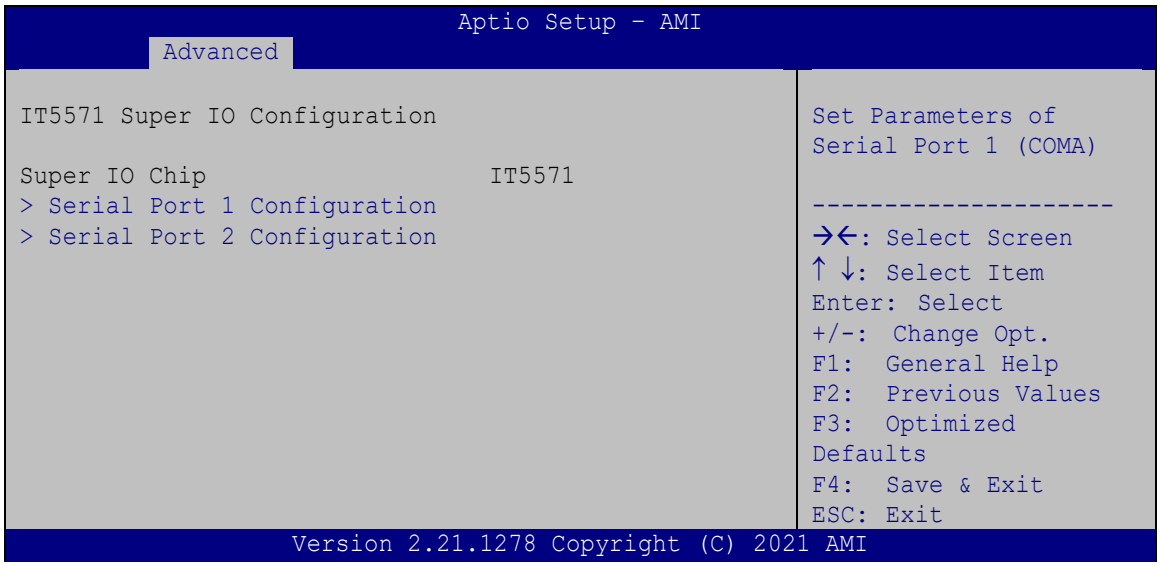
➔ **Pending Operation [None]**

Use the **Pending Operation** option to schedule an operation for the security device.

| | | |
|---|---|---|
| ➔ **None** | **DEFAULT** | TPM information is previous. |
| ➔ **TPM Clear** | | TPM information is cleared |

### 6.3.3 IT5571 Super IO Configuration

Use the **IT5571 Super IO Configuration** menu (**BIOS Menu 5**) to set or change the configurations for the parallel ports and serial ports.




**BIOS Menu 5: F81866 Super IO Configuration**

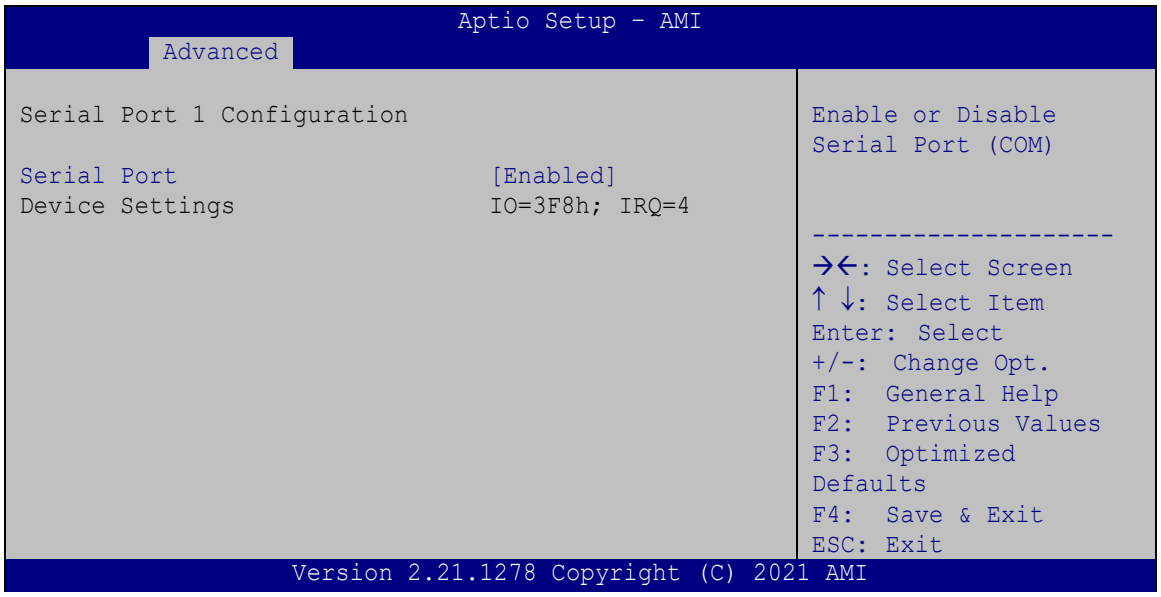
➔ **IT5571 Super IO Configuration**

The **IT5571 Super IO Configuration** lists a brief summary of the Super IO Chip information. The items shown in the system overview include:

- **Serial Port 1 Configuration: Set Parameters of Serial Port 1 (COMA)**
- **Serial Port 2 Configuration: Set Parameters of Serial Port 2 (COMB)**

### 6.3.3.1 Serial Port 1 Configuration

Use the **Serial Port 1 Configuration** submenu (**BIOS Menu 6**) to configure serial port 1.




**BIOS Menu 6: Serial Port 1 Configuration Menu**

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

| | | |
|---|---|---|
| ➔ **Disabled** | | Disable the serial port |
| ➔ **Enabled** | **DEFAULT** | Enable the serial port |

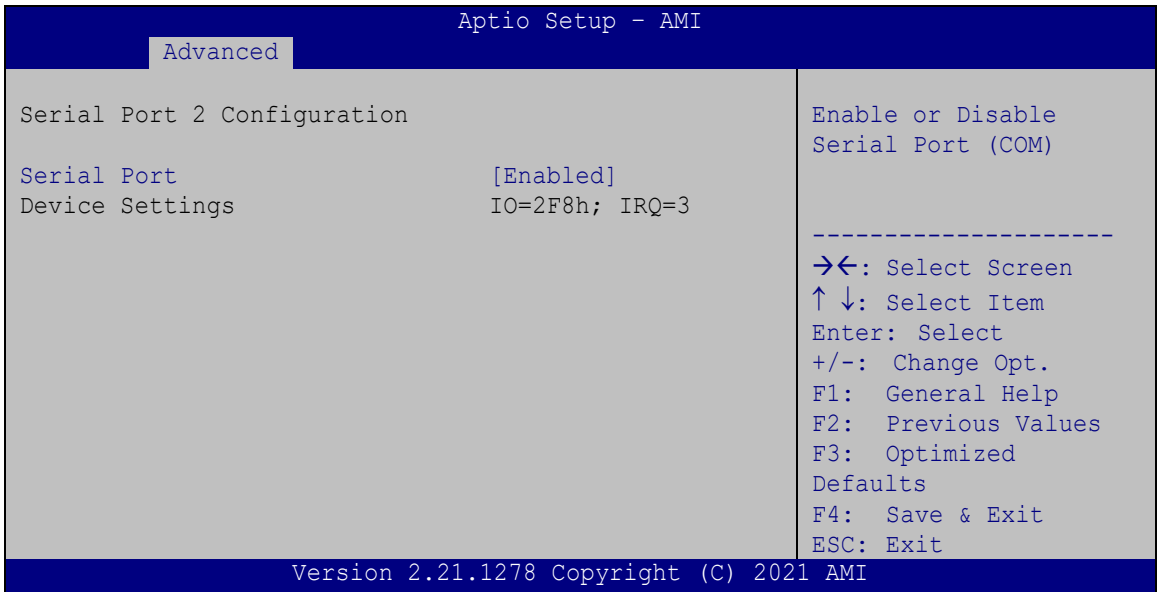
➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

| | |
|---|---|
| ➔ **IO=3F8h; IRQ=4** | Serial Port I/O port address is 3F8h and the interrupt address is IRQ4 |

### 6.3.3.2 Serial Port 2 Configuration

Use the **Serial Port 2 Configuration** submenu (**BIOS Menu 7**) to configure serial port 2.




**BIOS Menu 7: Serial Port 2 Configuration Menu**

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

| | | |
|---|---|---|
| ➔ **Disabled** | | Disable the serial port |
| ➔ **Enabled** | **DEFAULT** | Enable the serial port |

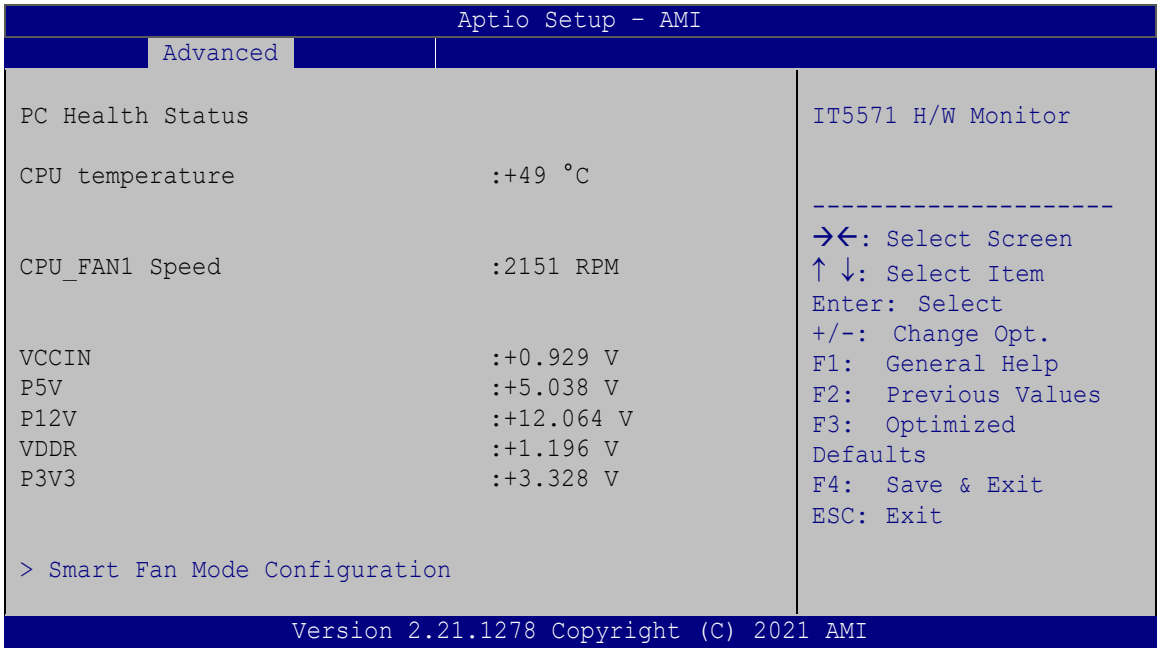
➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

| | |
|---|---|
| ➔ **IO=2F8h; IRQ=3** | Serial Port I/O port address is 2F8h and the interrupt address is IRQ3 |

### 6.3.4 IT5571 H/W Monitor

The **IT5571 H/W Monitor** menu (**BIOS Menu 8**) contains the fan configuration submenu, and displays the system temperature and CPU fan speed.




**BIOS Menu 8:IT5571 H/W Monitor**

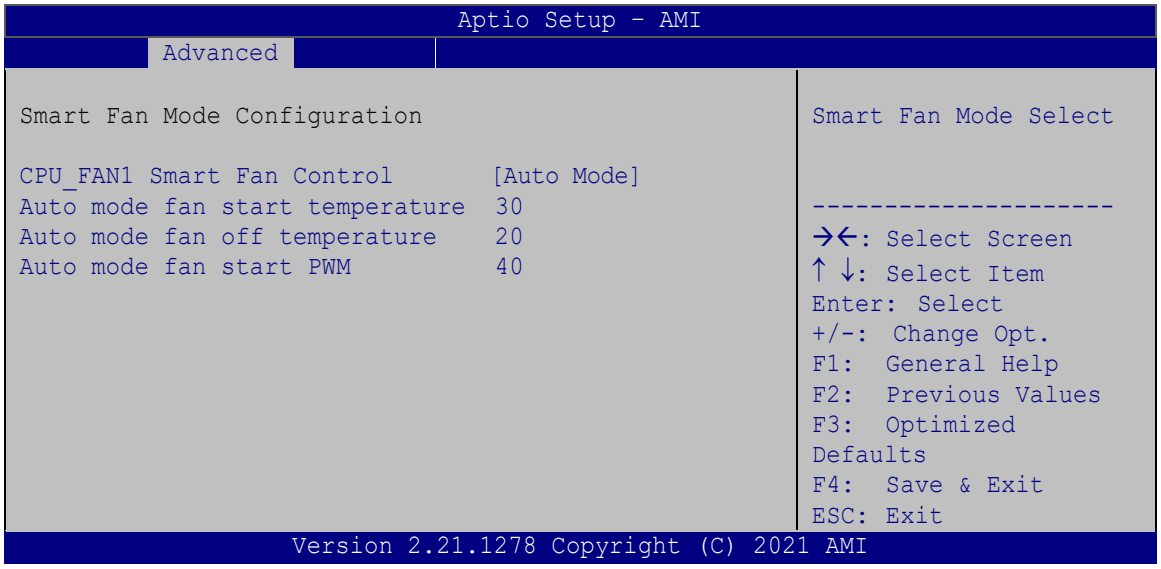
➔ **PC Health Status**

The following system parameters and values are shown. The system parameters that are monitored are:

- System Temperatures:
  - CPU Temperature
- Fan Speeds:
  - CPU Fan Speed
- Voltages:
  - VCCIN
  - P5V
  - P12V
  - VDDR
  - P3V3

### 6.3.4.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 9**) to configure the CPU/system fan temperature and speed settings.




**BIOS Menu 9: Smart Fan Mode Configuration**

➔ **CPU_FAN1 Smart Fan Control [Auto Mode]**

Use the **CPU_FAN1 Smart Fan Control** option to configure the CPU Smart Fan.

➔ **Manual Mode** The fan spins at the speed set in Manual Mode settings.

➔ **Auto Mode** **DEFAULT** The fan adjusts its speed using Auto Mode settings.

➔ **Auto mode fan start/off temperature**

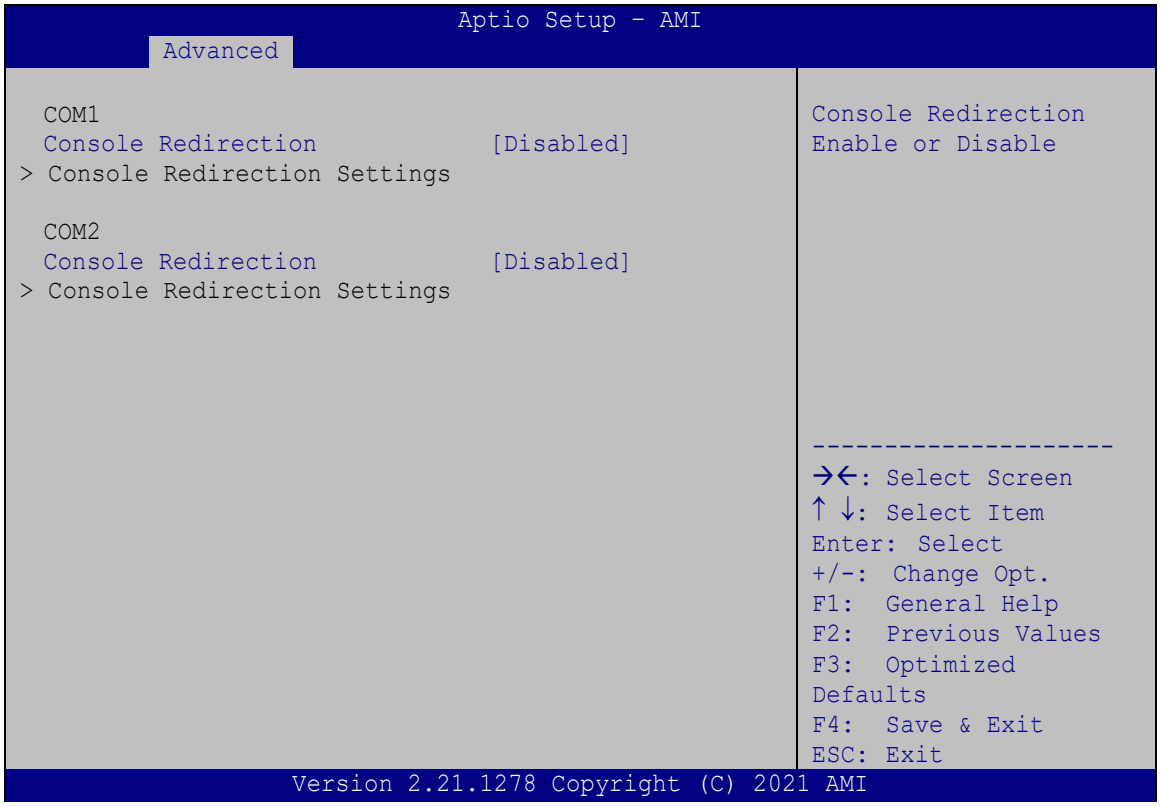
Use the + or – key to change the **Auto mode fan start/off temperature** value. Enter a decimal number between 1 and 100.

➔ **Auto mode fan start PWM**

Use the + or – key to change the **Auto mode fan start PWM** value. Enter a decimal number between 1 and 100.

### 6.3.5 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 10**) allows the console redirection options to be configured. Console redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.




**BIOS Menu 10: Serial Port Console Redirection**

➔ **Console Redirection [Disabled]**

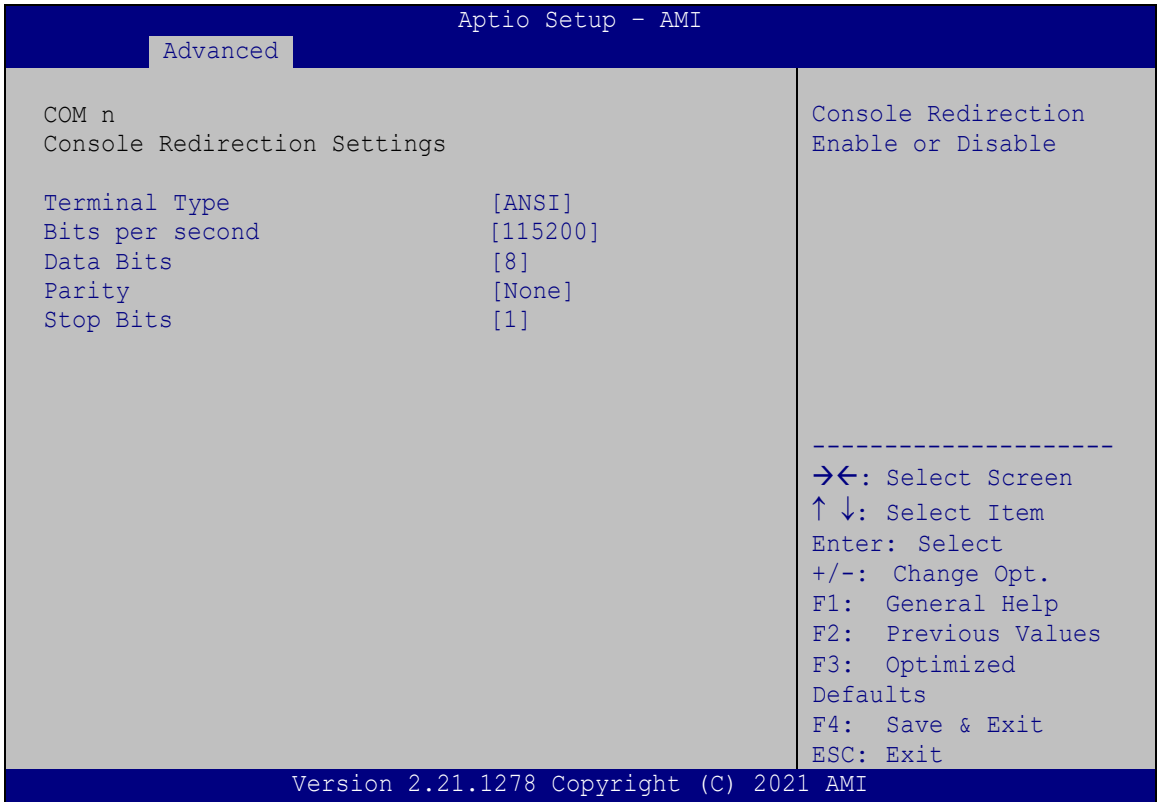
Use **Console Redirection** option to enable or disable the console redirection function.

| | | | |
|---|---|---|---|
| ➔ | **Disabled** | **DEFAULT** | Disabled the console redirection function |
| ➔ | **Enabled** | | Enabled the console redirection function |

The following options are available in the **Console Redirection Settings** submenu when the **Console Redirection** option is enabled.

### 6.3.5.1 Console Redirection Settings

The following options are available in the **Console Redirection Settings** submenu (**BIOS Menu 11**) when the **COM Console Redirection (for COM1 to COM2)** option is enabled.




**BIOS Menu 11: Console Redirection Settings**

➔ **Terminal Type [ANSI]**

Use the **Terminal Type** option to specify the remote terminal type.

| | | | |
|---|---|---|---|
| ➔ | **VT100** | | The target terminal type is VT100 |
| ➔ | **VT100+** | | The target terminal type is VT100+ |
| ➔ | **VT-UTF8** | | The target terminal type is VT-UTF8 |
| ➔ | **ANSI** | **DEFAULT** | The target terminal type is ANSI |

➔ **Bits per second [115200]**

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match the other side. Long or noisy lines may require lower speeds.

| | | |
|---|---|---|
| ➔ **9600** | | Sets the serial port transmission speed at 9600. |
| ➔ **19200** | | Sets the serial port transmission speed at 19200. |
| ➔ **57600** | | Sets the serial port transmission speed at 57600. |
| ➔ **115200** | **DEFAULT** | Sets the serial port transmission speed at 115200. |

➔ **Data Bits [8]**

Use the **Data Bits** option to specify the number of data bits.

| | | |
|---|---|---|
| ➔ **7** | | Sets the data bits at 7. |
| ➔ **8** | **DEFAULT** | Sets the data bits at 8. |

➔ **Parity [None]**

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

| | | |
|---|---|---|
| ➔ **None** | **DEFAULT** | No parity bit is sent with the data bits. |
| ➔ **Even** | | The parity bit is 0 if the number of ones in the data bits is even. |
| ➔ **Odd** | | The parity bit is 0 if the number of ones in the data bits is odd. |
| ➔ **Mark** | | The parity bit is always 1. This option does not provide error detection. |
| ➔ **Space** | | The parity bit is always 0. This option does not provide error detection. |

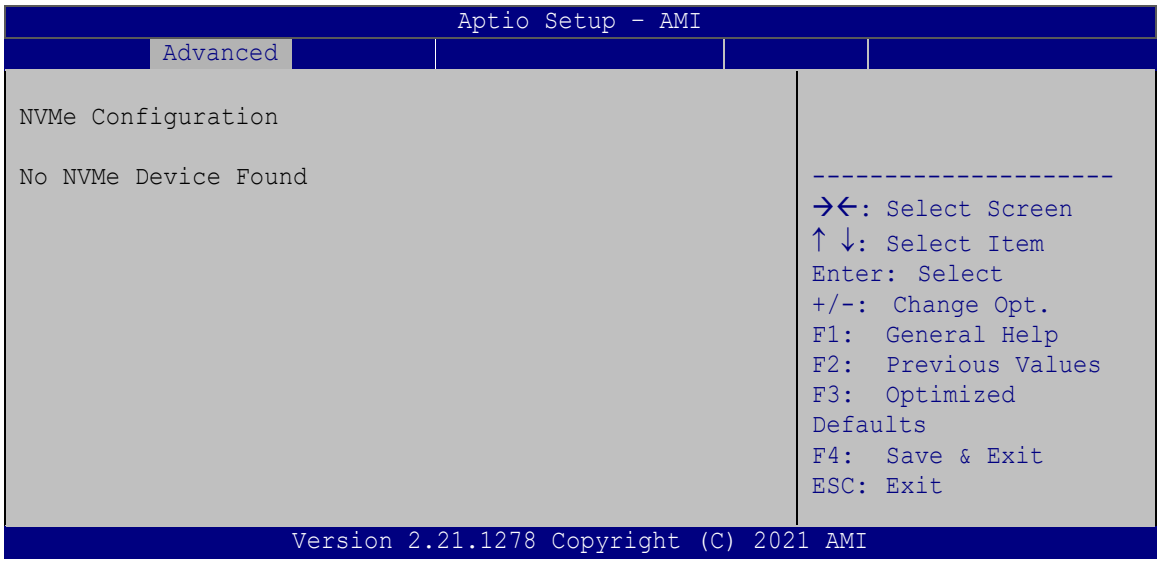
➔ **Stop Bits [1]**

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

| | | | |
|---|---|---|---|
| ➔ | **1** | **DEFAULT** | Sets the number of stop bits at 1. |
| ➔ | **2** | | Sets the number of stop bits at 2. |

### 6.3.6 NVMe Configuration

Use the **NVMe Configuration** (**BIOS Menu 12**) menu to display the NVMe controller and device information.



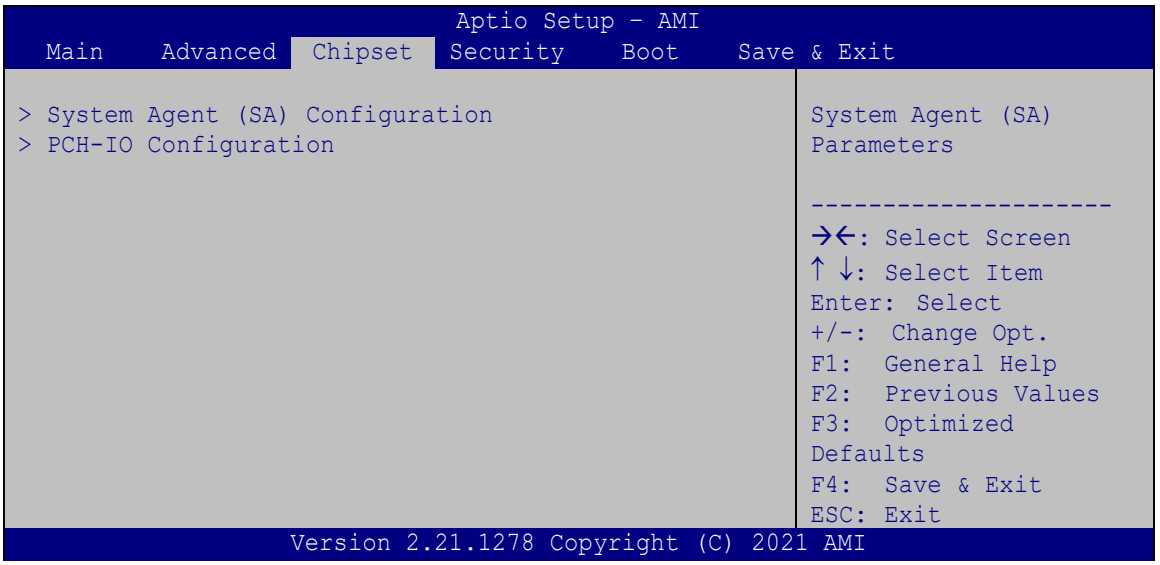

**BIOS Menu 12: NVMe Configuration**

## 6.4 Chipset

Use the **Chipset** menu (**BIOS Menu 13**) to access the PCH IO and System Agent (SA) configuration menus.

**WARNING!**

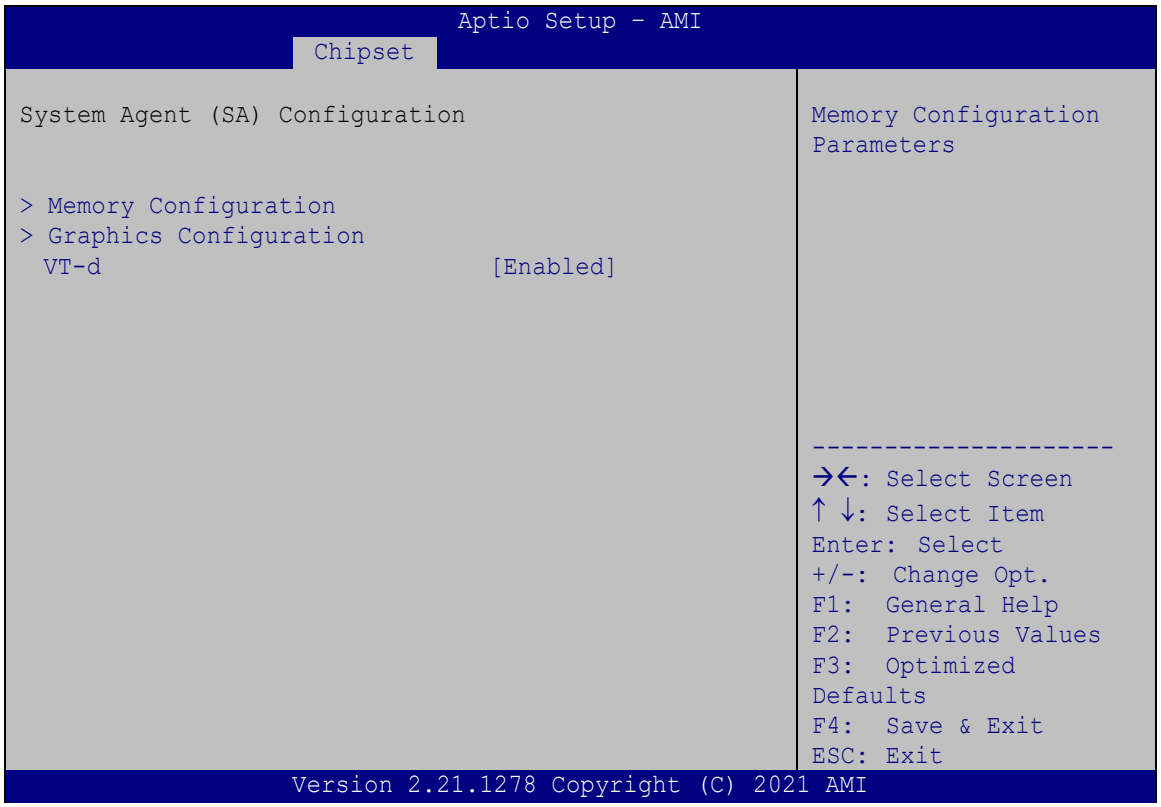
Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.




**BIOS Menu 13: Chipset**

### 6.4.1 System Agent (SA) Configuration

Use the **System Agent (SA) Configuration** menu (**BIOS Menu 14**) to configure the System Agent (SA) parameters.




**BIOS Menu 14: System Agent (SA) Configuration**

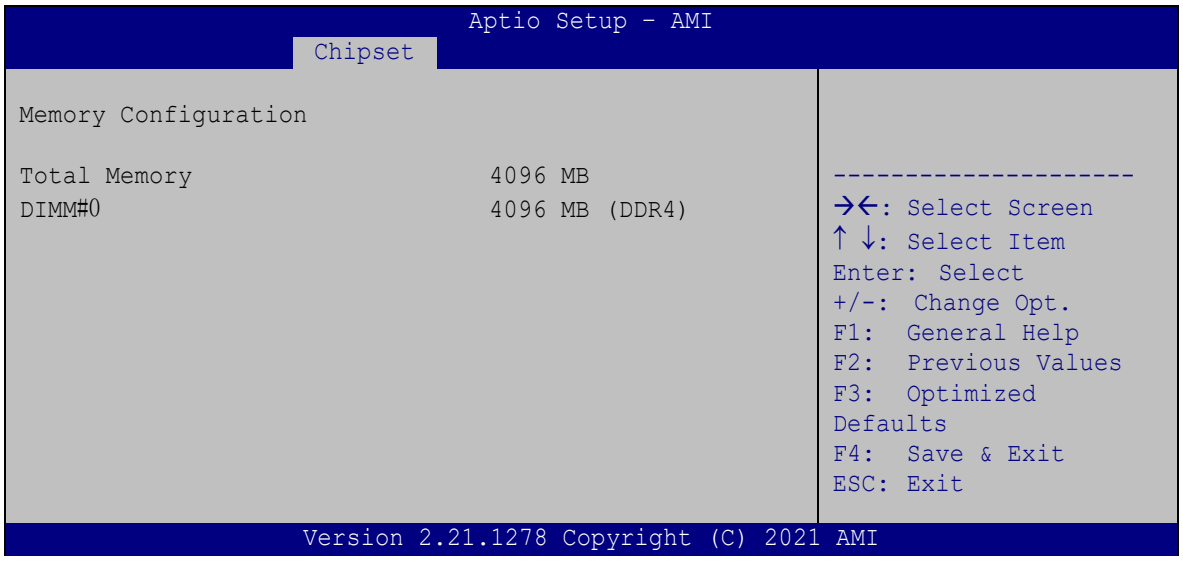
➔ **VT-d [Enabled]**

Use the **VT-d** option to enable or disable the VT-d capability.

| | | | |
|---|---|---|---|
| ➔ | **Disabled** | | Disable the VT-d capability |
| ➔ | **Enabled** | **DEFAULT** | Enable the VT-d capability |

### 6.4.1.1 Memory Configuration

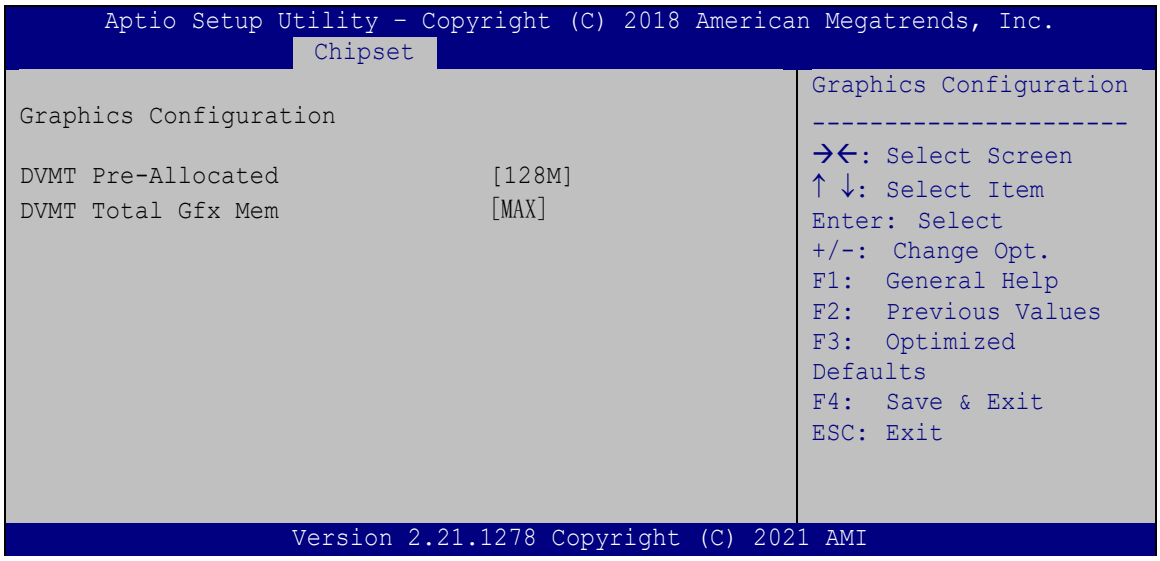
Use the **Memory Configuration** submenu (**BIOS Menu 15**) to view memory information.




**BIOS Menu 15: Memory Configuration**

### 6.4.1.2 Graphics Configuration

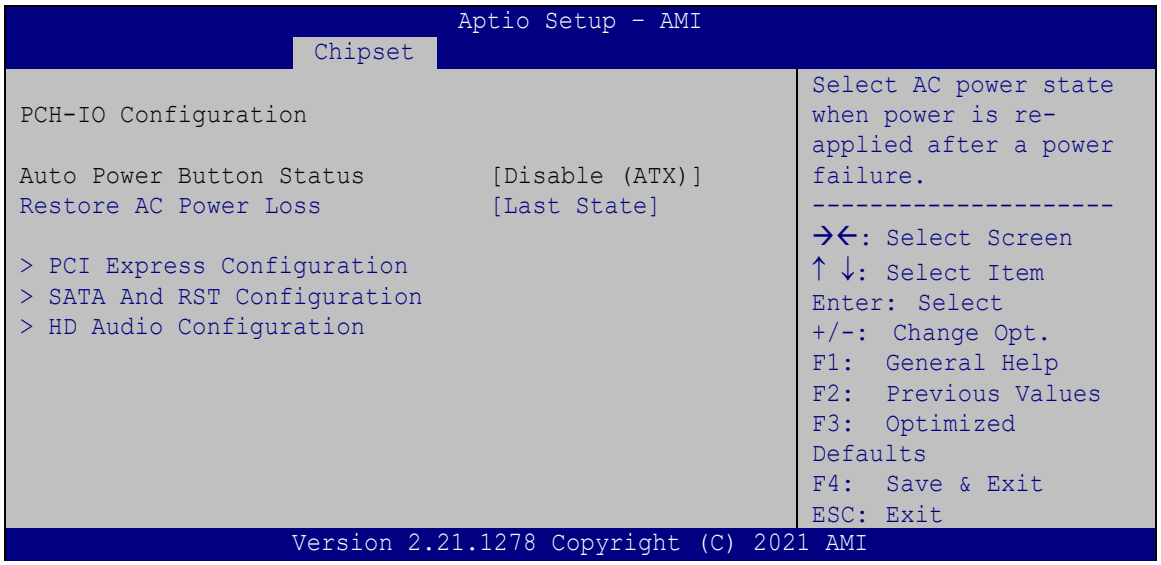
Use the **Graphics Configuration** (**BIOS Menu 16**) menu to view the information of the video device connected to the system.




**BIOS Menu 16: Graphics Configuration**

### 6.4.2 PCH-IO Configuration

Use the **PCH-IO Configuration** menu (**BIOS Menu 17**) to configure the PCH parameters.




**BIOS Menu 17: PCH-IO Configuration**

➔ **Auto Power Button Function [Disabled(ATX)]**

Use the **Auto Power Button Function** BIOS option to show the power mode state. Use the **J_ATX_AT1** to switch the AT/ATX power mode.

- ➔ **Enabled (AT)** The system power mode is AT.
- ➔ **Disabled (ATX)** The system power mode is ATX.

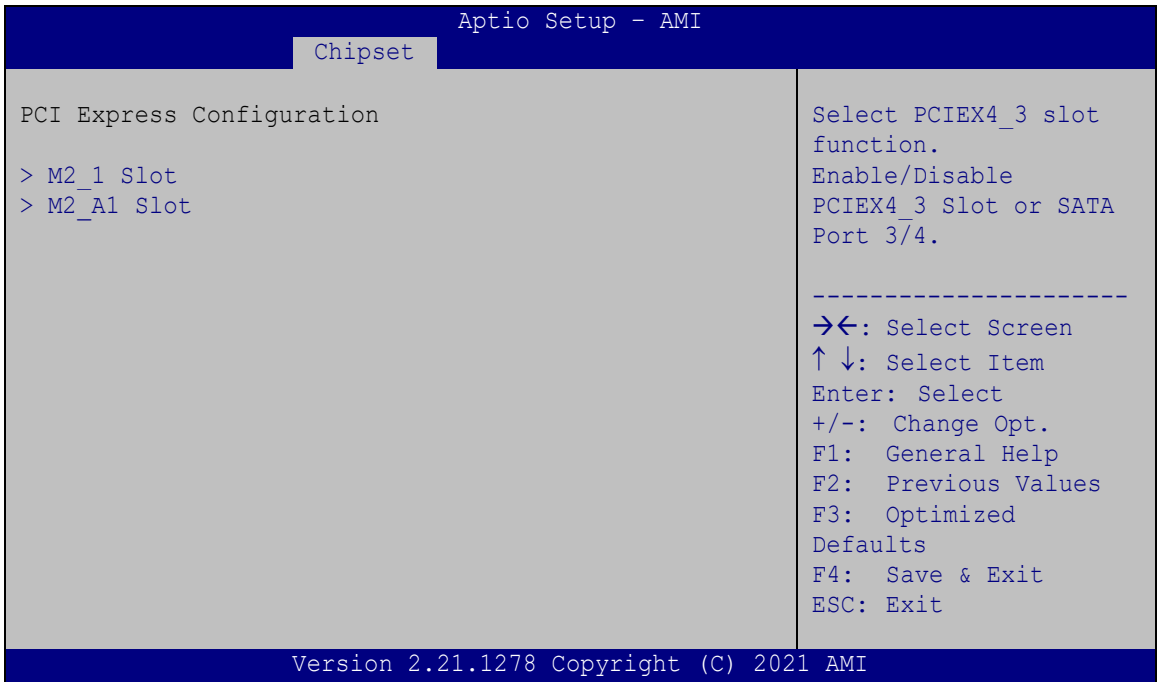
➔ **Restore AC Power Loss [Last State]**

Use the **Restore AC Power Loss** BIOS option to specify what state the system returns to if there is a sudden loss of power to the system.

- ➔ **Power Off** The system remains turned off
- ➔ **Power On** The system turns on
- ➔ **Last State** **DEFAULT** The system returns to its previous state. If it was on, it turns itself on. If it was off, it remains off.

### 6.4.2.1 PCI Express Configuration

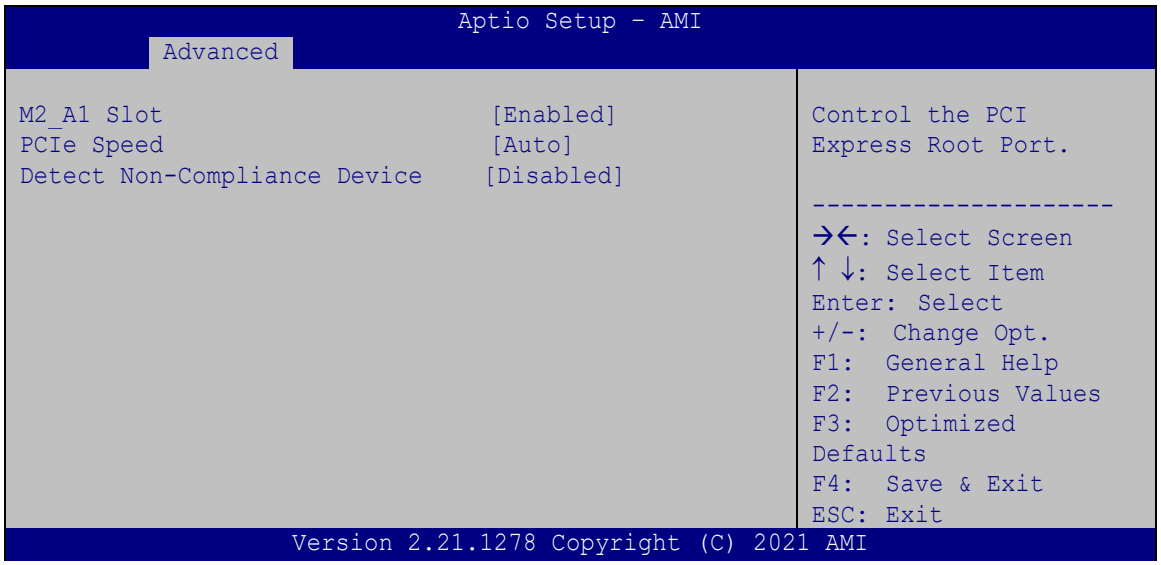
Use the **PCI Express Configuration** menu (**BIOS Menu 18**) to configure the PCI Express and M.2 slots.




**BIOS Menu 18: PCI Express Configuration**

#### 6.4.2.1.1 M2_1 and M2_A1 Slots

Use the **M2_1, M2_A1** submenu (**BIOS Menu 19**) to configure the PCI Root Port Setting.




**BIOS Menu 19: PCIe Slot Configuration Submenu**

➔ **M2_A1 Slot [Enabled]**

Use the **M2_A1 Slot** option to enable or disable the M.2 slot.

| | | | |
|---|---|---|---|
| ➔ | **Disabled** | | Disables the M.2 slot. |
| ➔ | **Enabled** | **DEFAULT** | Enables the M.2 slot. |

➔ **PCIe Speed [Auto]**

Use the **PCIe Speed** option to specify the PCI Express port speed .

| | | | |
|---|---|---|---|
| ➔ | **Auto** | **DEFAULT** | Auto mode. |
| ➔ | **Gen1** | | Configure PCIe Speed to Gen1. |
| ➔ | **Gen2** | | Configure PCIe Speed to Gen2. |
| ➔ | **Gen3** | | Configure PCIe Speed to Gen3. |

➔ **Detect Non-Compliance Device [Disabled]**

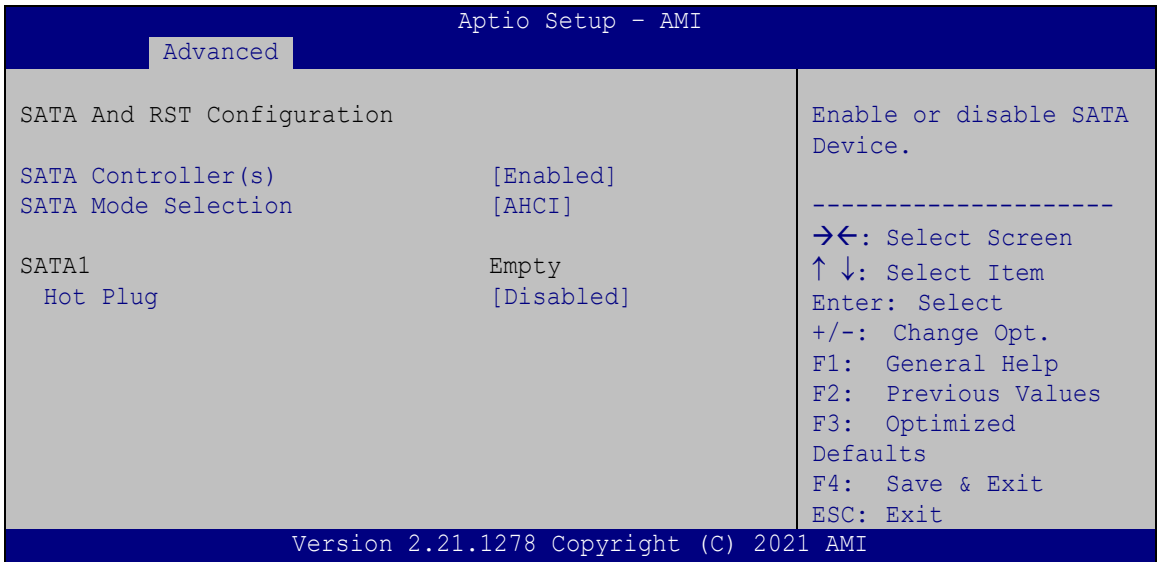
Use the **Detect Non-Compliance Device** option to configure whether to detect if a non-compliance PCI Express device is connected to the PCI Express port.

➔ **Disabled** **DEFAULT** Do not detect if a non-compliance PCI Express device is connected to the PCI Express port.

➔ **Enabled** Detect if a non-compliance PCI Express device is connected to the PCI Express port.

### 6.4.2.2 SATA And RST Configuration

Use the **SATA And RST Configuration** menu (**BIOS Menu 20**) to change and/or set the configuration of the SATA devices installed in the system.




**BIOS Menu 20: SATA Configuration**

➔ **SATA Controller(s) [Enabled]**

Use the **SATA Controller(s)** option to configure the SATA controller(s).

➔ **Enabled** **DEFAULT** Enables the on-board SATA controller(s).

➔ **Disabled** Disables the on-board SATA controller(s).

➔ **SATA Mode Selection [AHCI]**

Use the **SATA Mode Selection** option to determine how the SATA devices operate.

➔ **AHCI** **DEFAULT** Configures SATA devices as AHCI device.

➔ **Hot Plug [Disabled]**

Use the **Hot Plug** option to designate the correspondent SATA port as hot-pluggable.

| | | |
|---|---|---|
| ➔ **Disabled** | **DEFAULT** | Disables the hot-pluggable function of the SATA port. |
| ➔ **Enabled** | | Designates the SATA port as hot-pluggable. |

### 6.4.2.3 HD Audio Configuration

Use the **HD Audio Configuration** menu (**BIOS Menu 21**) to configure the PCH Azalia settings.


**BIOS Menu 21: HD Audio Configuration**

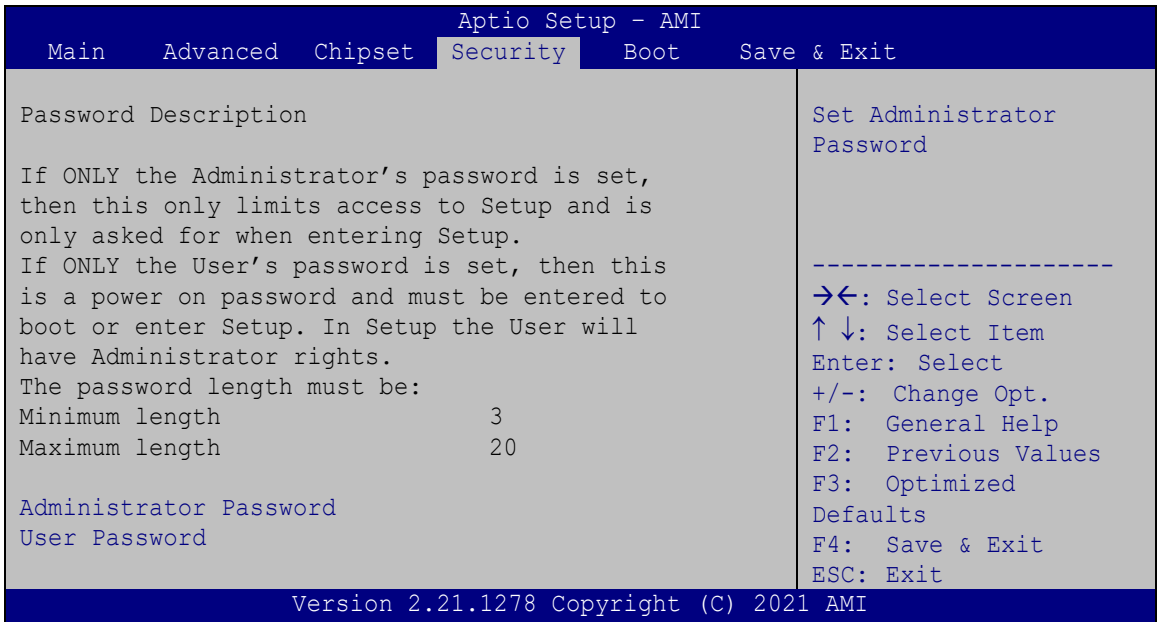
➔ **HD Audio [Enabled]**

Use the **HD Audio** option to enable or disable the High Definition Audio controller.

| | | |
|---|---|---|
| ➔ **Disabled** | | The onboard High Definition Audio controller is disabled. |
| ➔ **Enabled** | **DEFAULT** | The onboard High Definition Audio controller is enabled. |

## 6.5 Security

Use the **Security** menu (**BIOS Menu 22**) to set system and user passwords.




**BIOS Menu 22: Security**

➔ **Administrator Password**

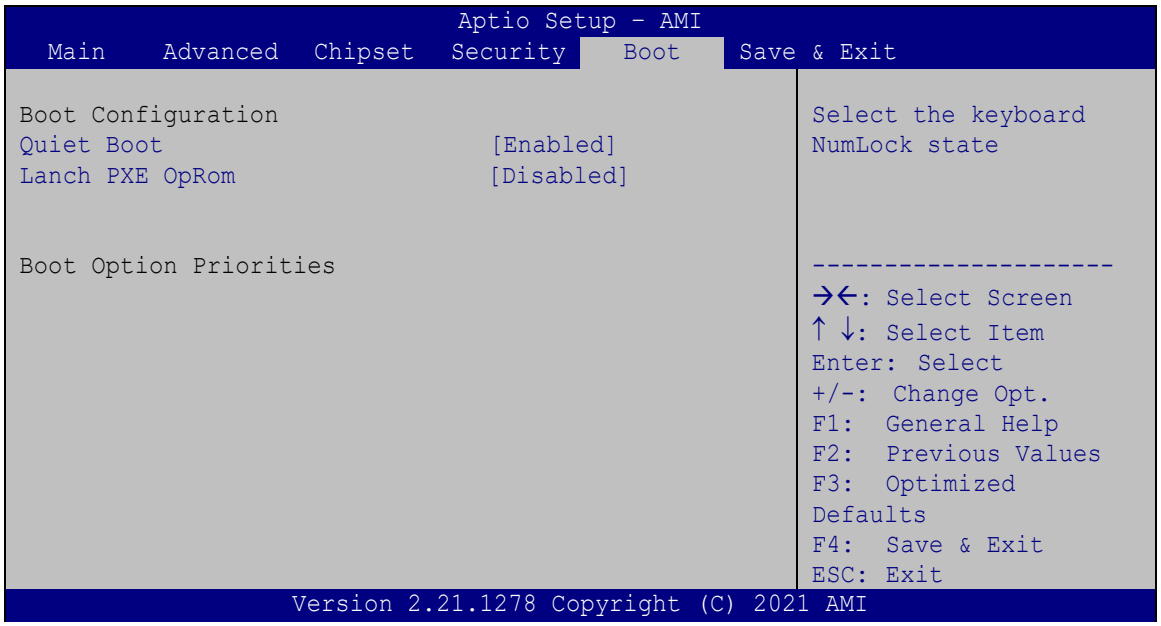
Use the **Administrator Password** to set or change a administrator password.

➔ **User Password**

Use the **User Password** to set or change a user password.

## 6.6 Boot

Use the **Boot** menu (**BIOS Menu 23**) to configure system boot options.




**BIOS Menu 23: Boot**

### 6.6.1 Boot Configuration

➔ **Quiet Boot [Enabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

| | | | |
|---|---|---|---|
| ➔ | **Disabled** | | Normal POST messages displayed |
| ➔ | **Enabled** | **DEFAULT** | OEM Logo displayed instead of POST messages |

➔ **Launch PXE OpROM [Disabled]**

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

| | | | |
|---|---|---|---|
| ➔ | **Disabled** | **DEFAULT** | Ignore all PXE Option ROMs |
| ➔ | **Enabled** | | Load PXE Option ROMs. |

### 6.6.2 Boot Option Priorities

Use the Boot Option # N to choose the system boots from the peripherals you selected The following Boot Options are listed as an example.

➔ **Boot Option #1**

Sets the system boot order **ADATA SP580** as the first priority.

➔ **Windows Boot Manager (P1: ADATA SSD SP580 240GB)**

➔ **Disabled**

➔ **Boot Option #2**

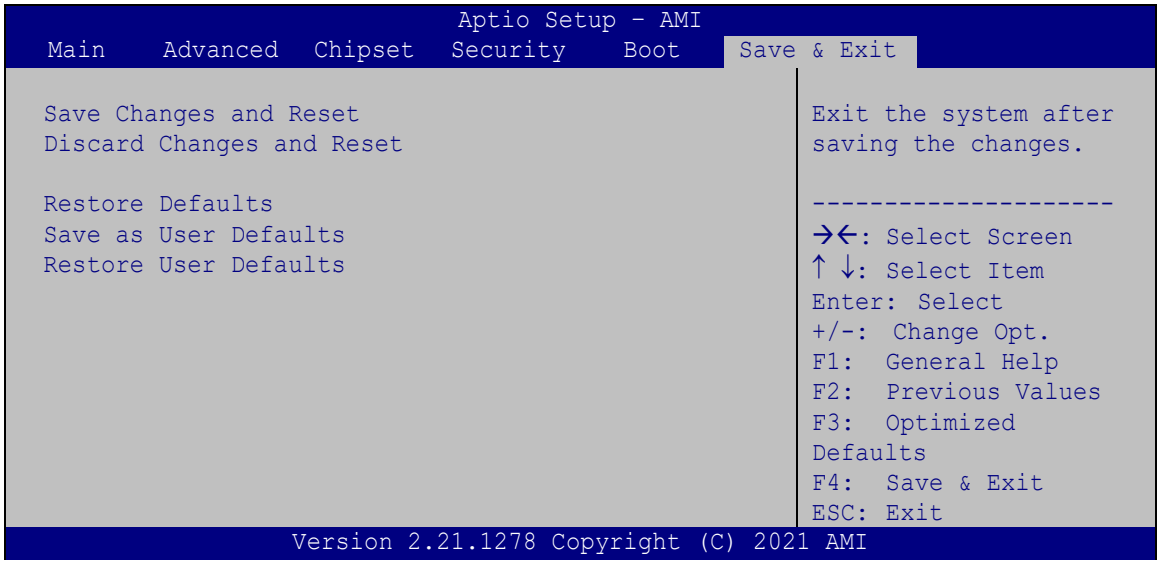
Sets the system boot order **UEFI: KingstonDataTraveler2.0** as the second priority.

➔ **UEFI: KingstonDataTraveler2.0, Partition 1**

➔ **Disabled**

## 6.7 Save & Exit

Use the **Save & Exit** menu (**BIOS Menu 24**) to load default BIOS values, optimal failsafe values and to save configuration changes.




**BIOS Menu 24: Save & Exit**

➔ **Save Changes and Reset**

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and reset the system.

➔ **Discard Changes and Reset**

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

➔ **Restore Defaults**

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

➔ **Save as User Defaults**

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

➔ **Restore User Defaults**

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Appendix

A

# Regulatory Compliance

## DECLARATION OF CONFORMITY

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

## FCC WARNING

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

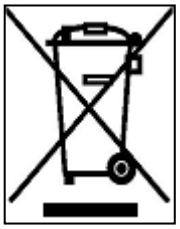
# Product Disposal

**CAUTION:**

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- Outside the European Union–If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the correct disposal method.
- Within the European Union–The device that produces less waste and is easier to recycle is classified as electronic device in terms of the European Directive 2012/19/EU (WEEE), and must not be disposed of as domestic garbage.



EU-wide legislation, as implemented in each Member State, requires that waste electrical and electronic products carrying the mark (left) must be disposed of separately from normal household waste. This includes monitors and electrical accessories, such as signal cables or power cords. When you need to dispose of your device, please follow the guidance of your local authority, or ask the shop where you purchased the product. The mark on electrical and electronic products only applies to the current European Union Member States.

Please follow the national guidelines for electrical and electronic product disposal.

Appendix

C

# BIOS Options

Below is a list of BIOS configuration options in the BIOS chapter.

Appendix

D

# Error Beep Code

## D.1 PEI Beep Codes

| Number of Beeps | Description |
|---|---|
| 1 | Memory not Installed |
| 1 | Memory was installed twice<br>(InstallPeiMemory routine in PEI Core called twice) |
| 2 | Recovery started |
| 3 | DXEIPL was not found |
| 3 | DXE Core Firmware Volume was not found |
| 4 | Recovery failed |
| 4 | S3 Resume failed |
| 7 | Reset PPI is not available |

## D.2 DXE Beep Codes

| Number of Beeps | Description |
|---|---|
| 1 | Invalid password |
| 4 | Some of the Architectural Protocols are not available |
| 5 | No Console Output Devices are found |
| 5 | No Console Input Devices are found |
| 6 | Flash update is failed |
| 7 | Reset protocol is not available |
| 8 | Platform PCI resource requirements cannot be met |

**NOTE:**

If you have any question, please contact IEI for further assistance.

Appendix

E

# Hazardous Materials Disclosure

# E.1 RoHS II Directive (2015/863/EU)

The details provided in this appendix are to ensure that the product is compliant with the RoHS II Directive (2015/863/EU). The table below acknowledges the presences of small quantities of certain substances in the product, and is applicable to RoHS II Directive (2015/863/EU).

Please refer to the following table.

| Part Name | Toxic or Hazardous Substances and Elements | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Lead (Pb) | Mercury (Hg) | Cadmium (Cd) | Hexavalent Chromium (CR(VI)) | Polybromina ted Biphenyls | Polybromina ted Diphenyl Ethers | Bis(2-ethylhexyl) phthalate | Butyl benzyl phthalate (BBP) | Dibutyl phthalate (DBP) | Diisobutyl phthalate (DIBP) |
| Housing | O | O | O | O | O | O | O | O | O | O |
| Printed Circuit Board | O | O | O | O | O | O | O | O | O | O |
| Metal Fasteners | O | O | O | O | O | O | O | O | O | O |
| Cable Assembly | O | O | O | O | O | O | O | O | O | O |
| Fan Assembly | O | O | O | O | O | O | O | O | O | O |
| Power Supply Assemblies | O | O | O | O | O | O | O | O | O | O |
| Battery | O | O | O | O | O | O | O | O | O | O |

O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in Directive (EU) 2015/863.

X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in Directive (EU) 2015/863.

## E.2 China RoHS

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有"环境友好使用期限"的标签，此期限是估算这些物质"不会有泄漏或突变"的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

| 部件名称 | 有毒有害物质或元素 | | | | | |
|---|---|---|---|---|---|---|
| | 铅 (Pb) | 汞 (Hg) | 镉 (Cd) | 六价铬 (CR(VI)) | 多溴联苯 (PBB) | 多溴二苯醚 (PBDE) |
| 壳体 | O | O | O | O | O | O |
| 印刷电路板 | O | O | O | O | O | O |
| 金属螺帽 | O | O | O | O | O | O |
| 电缆组装 | O | O | O | O | O | O |
| 风扇组装 | O | O | O | O | O | O |
| 电力供应组装 | O | O | O | O | O | O |
| 电池 | O | O | O | O | O | O |

O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求。