

MIO-5354

**Intel® Atom™ x7000RE Series and
Intel® Core™ i3-N305 and
Intel® Processor N97 on 3.5" SBC
(Code Name: Amston Lake / Alder
Lake-N)**

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This manual is for the MIO-5354.

Product Warranty (2 Years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced free of charge during the warranty period. For out-of-warranty repairs, customers will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details.

If you believe your product to be defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

Declaration of Conformity

CE

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class B

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Caution! *There is danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*



Technical Support and Assistance

1. Visit the Advantech web site at www.advantech.com/support where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
 - Product name and serial number
 - Description of your peripheral attachments
 - Description of your software (operating system, version, application software, etc.)
 - A complete description of the problem
 - The exact wording of any error messages

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- | | |
|--------------------------------------|-----------------------|
| ■ 1 x MIO-5354 SBC | |
| ■ 1 x SATA Cable 30 cm | (P/N: 1700006291) |
| ■ 1 x SATA Power Cable 35 cm | (P/N: 1700031583-01) |
| ■ 1 x Audio Cable 20 cm | (P/N: 1700019584-01) |
| ■ 2 x COM RS-232/422/485 Cable 20 cm | (P/N: 1700030404-01) |
| – 1 x Heatsink | (P/N: 1970005854T001) |
| – 1 x Cooler | (P/N: 1970005931T001) |

Optional Accessories

- | | |
|--------------------------------|----------------------|
| Dual USB 3.0 Cable 35 cm | (P/N: 1700032181-01) |
| COM3/COM4 Cable 20 cm | (P/N: 1700031582-01) |
| MIOe-PSE PoE Module Single 30W | (P/N: MIOE-PSE-SPA1) |

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Chapter 1

General Information

This chapter gives background information on the MIO-5354.

Sections include:

- Introduction
- Specifications
- Block Diagram

1.1 Introduction

MIO-5354 is a 3.5-inch (146 x 102 mm) single-board computer and is powered by Intel Atom® Processors x7000RE Series, Intel® Core™ i3-N305 Processors and Intel® Processor N97. The MIO-5354 can operate under -40~85°C extreme temperatures with a x7000RE series SoC and supports a wide power input range of 12~24V. The MIO-5354 supports single-channel DDR5-4800 SODIMM, up to 16GB with IB ECC support. It provides three independent displays via LVDS, DP 1.4, and HDMI 2.0, along with abundant I/O options: HDMI 2.0, 1 x 2.5GbE (with optional PoE support), 1 x GbE, 6 x USB, 4 x COM, 2 x CAN-FD, 1 x 8-bit GPIO, and 1 x I2C. Additionally, it includes 3 standalone M.2 slots: M.2 B-Key 2280, M.2 B-Key 3052, and M.2 E-Key 2230 for easy expansion.

The MIO-5354 includes the embedded SUSI API and EdgeBMC for out-of-band remote management with DeviceOn created by Advantech to monitor and control system operation effectively and remotely. Advantech has also validated the MIO-5354 for use with embedded operation systems, including Windows 11 LTSC and Ubuntu v24.04 LTS, making it ready for bundled shipment.

1.2 Specifications

Table 1.1: Specifications

Platform	Processor	x7835RE	x7433RE	x7211RE	i3-N305	N97
	Max. Frequency	3.60 GHz	3.40 GHz	3.20 GHz	3.80 GHz	3.60 GHz
	Base Frequency	1.30 GHz	1.50 GHz	1.00 GHz	1.80 GHz	2.00 GHz
	Core	8	4	2	8	4
	LLC	6MB	6MB	6MB	6MB	6MB
	CPU TDP	12W	9W	6W	15W	12W
	Chipset	Intel® 300 Series Chipset (SoC Integrated)				
	BIOS	AMI UEFI 256Mbit				
Memory	Technology	DDR5 4800 MT/s				
	Max. Capacity	Up to 16GB				
	Channel/Socket	Single Channel / One 262-pin SODIMM Slot				
	ECC Support	Support IB ECC by Platform				
Graphics	Controller	Intel® UHD Graphics				
	Max. Frequency	1.20 GHz	1.00 GHz	1.00 GHz	1.25 GHz	1.20 GHz
	Execution Units	32	32	16	32	24
	3D/HW Acceleration	DX12, OGL4.0, OCL1.2, HW Encode: HEVC/H265, AVC/H264, VP9, HW Decode: HEVC/H265, AVC/H264, VP9				
	LCD	1 x LVDS, Dual Channel 18-/24-bit, up to 1920 x 1080				
Display I/F	HDMI/DP	1 x HDMI 2.0, up to 4096 x 2160 x 24bpp@48-60Hz				
	Triple Display	3 simultaneous displays by LVDS + HDMI + DP				
	Controller	LAN1: i226; LAN2: i210				
Ethernet	Speed	LAN1: 2.5GbE; LAN2: GbE				
	Features	LAN1: Optional Support PoE. PSE compliant to IEEE 802.3at (30W with power module: MIOe-PSE) LAN2: Support EdgeBMC, Out of Band remote control				

Table 1.1: Specifications

External I/O	Ethernet	2 x RJ-45
	HDMI/DP	1 x HDMI + 1 x DP
	USB 3.2 / USB 2.0	2 x USB 3.2 + 2 x USB 2.0
Internal I/O	SATA	1 x SATA Gen III 6.0Gbps
	USB 3.0	2
	Serial Bus	1 x I ² C (*BOM option to SMBus by request)
	COM Port	2 x RS-232/422/485, 2 x RS-232
	CAN Bus	2 x CAN-FD, 2M/4M/8M bit/s or CAN 2.0, 1M bit/s
	GPIO	8-bit general purpose input output I/O
	Audio	Realtek ALC888s, Line-in/Line-out/MIC
	Inverter	5V @2A
	Smart Fan	12V, 2A (4-wire)
	Front Panel Control	Power-on, Reset, Buzzer, SATA LED, Power LED, Case Open
Board Features	Watchdog Timer	65536 level, 0~65535 sec
	TPM	Discrete TPM2.0
	iManager 3.0	SW API for Hardware Monitor, Smart Fan Control, Brightness Control, I2C, GPIO, WDT
Expansion	M.2 E-Key	1 x E-Key 2230 (PCIe x1, USB 2.0)
	M.2 B-Key	1 x B-Key 2280 (SATA or PCIe x1) 1 x B-Key 3052 (USB 3.0)
Power	Supply Voltage	Vin: DC 12V~24V $\pm$ 10%; RTC Battery: Lithium 3V/200mAH, support w/o CMOS Battery
	Connector	ATX 2pin 180D (*BOM Option to ATX 2pin 90D or DC-IN Jack by request)
	Power Management	AT, ATX
Environment	Temperature	Operating: Standard: 0 ~ 60°C (32 ~ 140°F) with 0.7m/s airflow; Extend: -40 ~ 85°C (-40 ~ 185°F) with 0.7m/s airflow
	Storage	-40 ~ 85°C (-40 ~ 185°F)
	Humidity	Operating: 40°C @ 95% relative humidity, non-condensing
	Vibration Resistance	3.5 Grms
Certification	EMC	CE, FCC Class B, ESD 8KV/15KV Criteria A
Mechanical	Dimensions	146 x 102 mm (5.7" x 4")
	Net Weight	145 g

*Note: Support by Request

1.3 Block Diagram

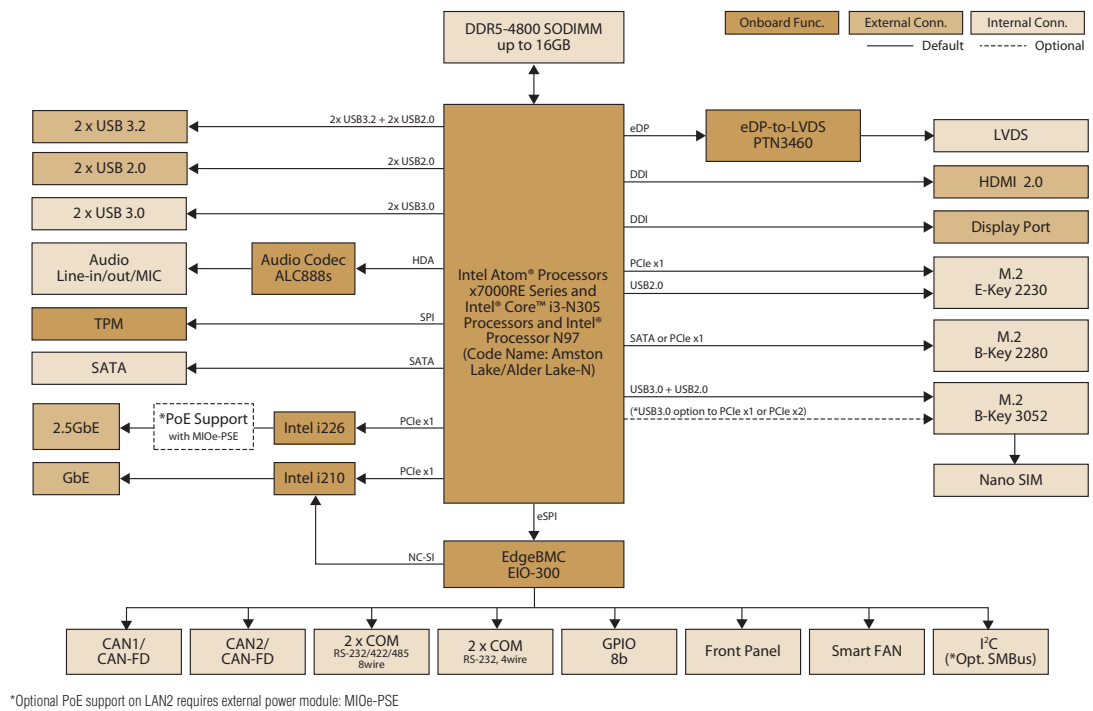


Figure 1.1 Block Diagram

Chapter 2

Mechanical

This chapter gives mechanical information for the MIO-5354.

Sections include:

- Mechanical Drawings

2.1 Board Layout: Dimensions

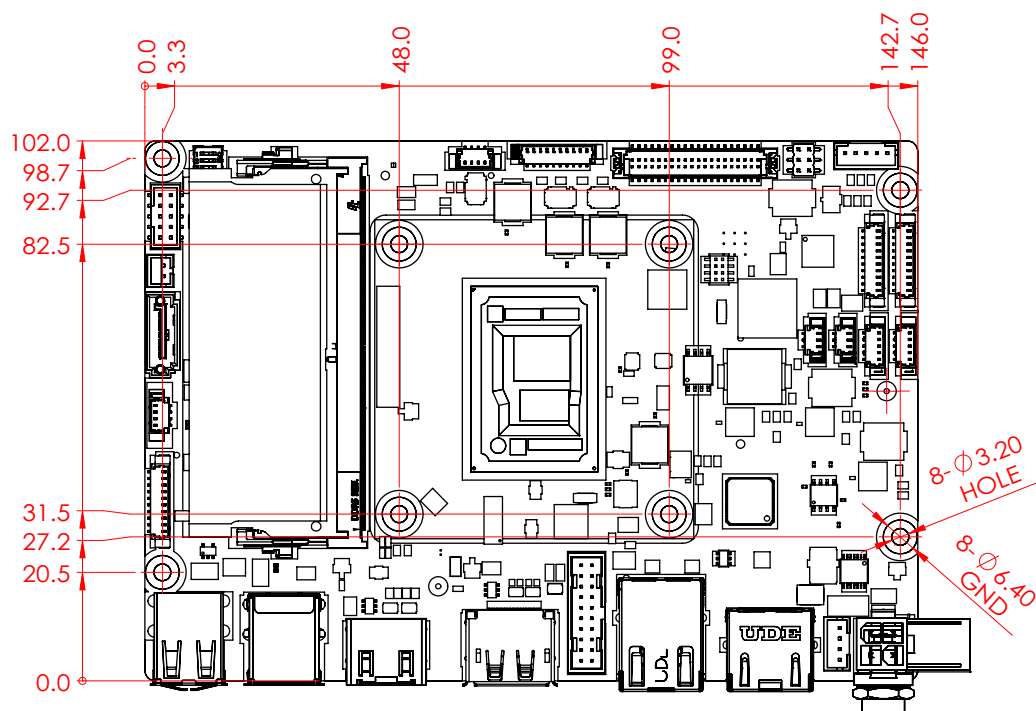


Figure 2.1 Mechanical Drawing (Top Side)

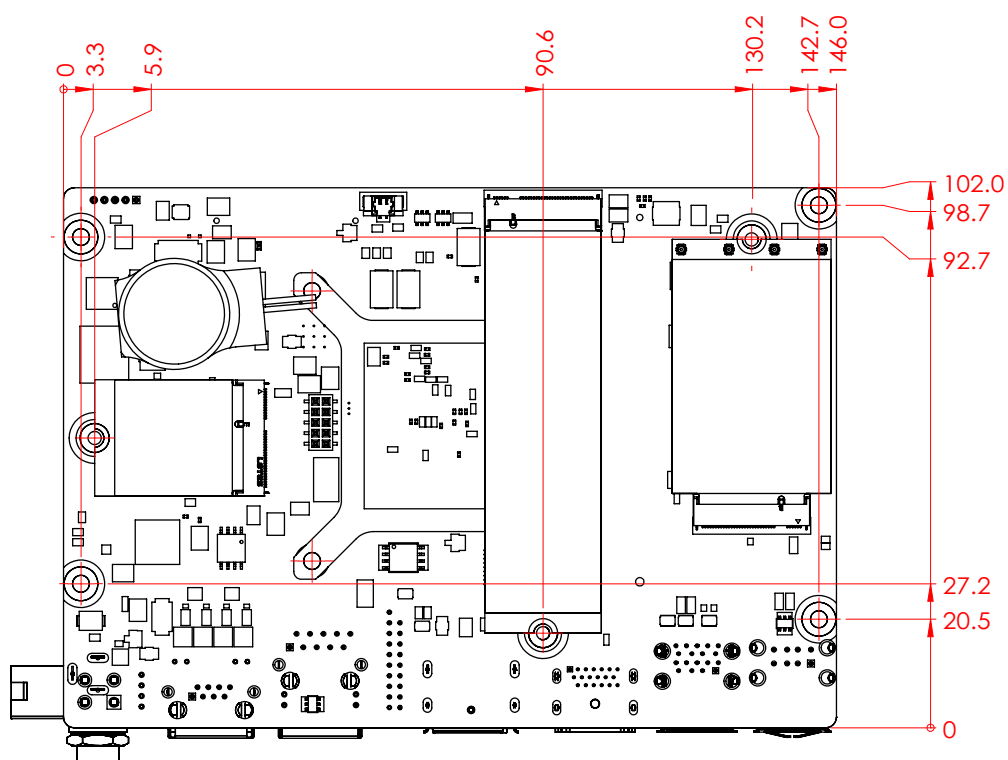


Figure 2.2 Mechanical Drawing (Bottom Side)

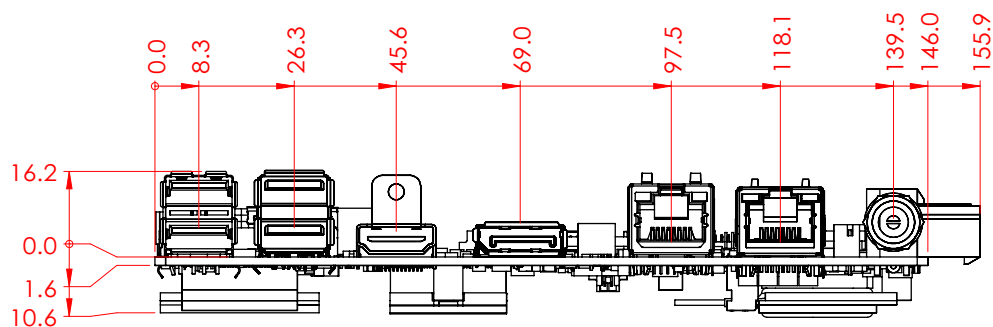


Figure 2.3 Mechanical Drawing (Coastline)

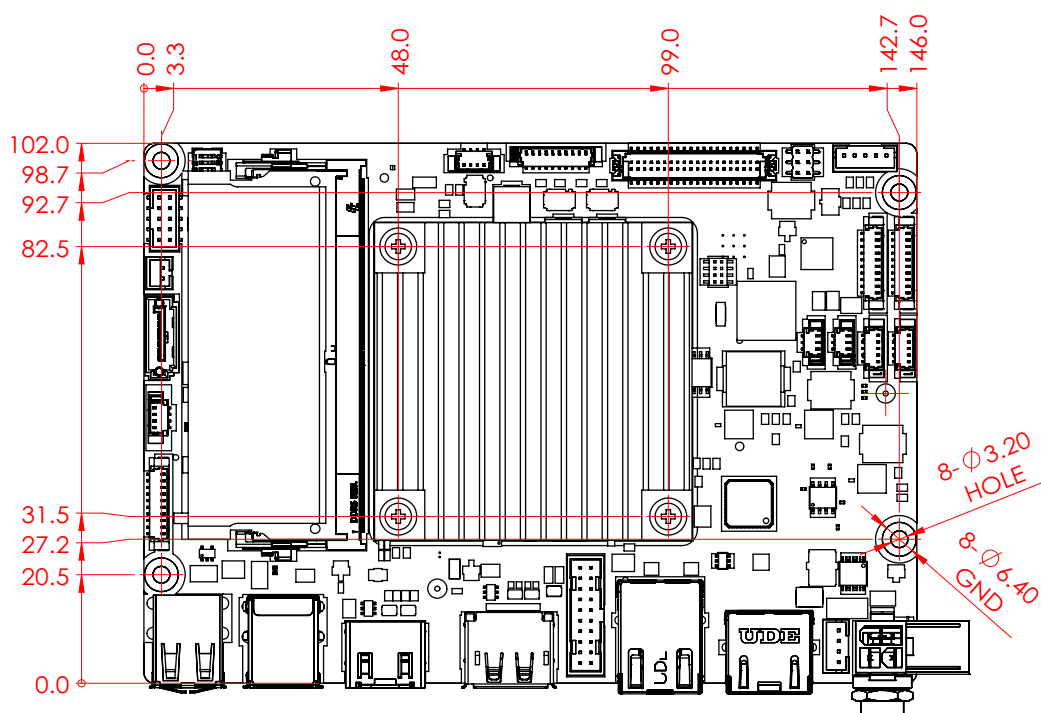


Figure 2.4 Mechanical Drawing with Heatsink (Top Side)

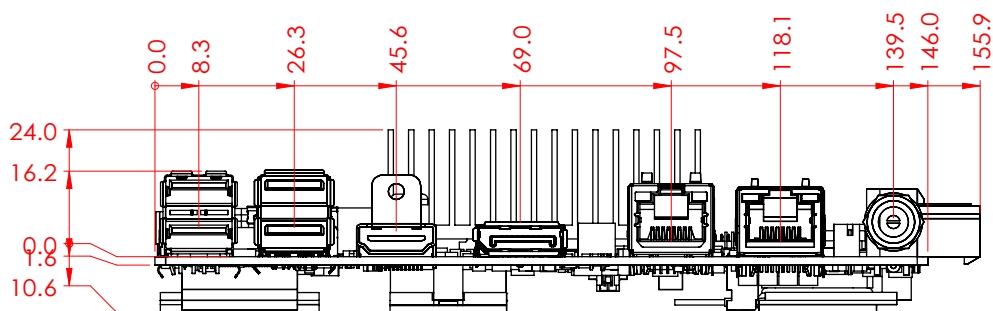


Figure 2.5 Mechanical Drawing with Heatsink (Coastline)

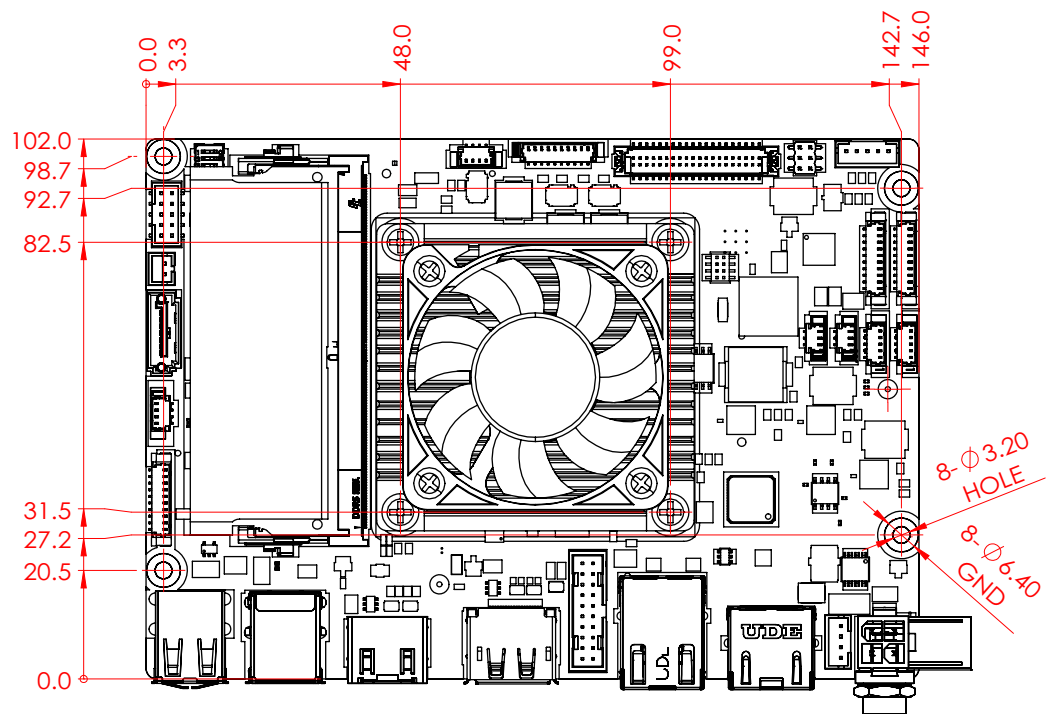


Figure 2.6 Mechanical Drawing with Cooler (Top Side)

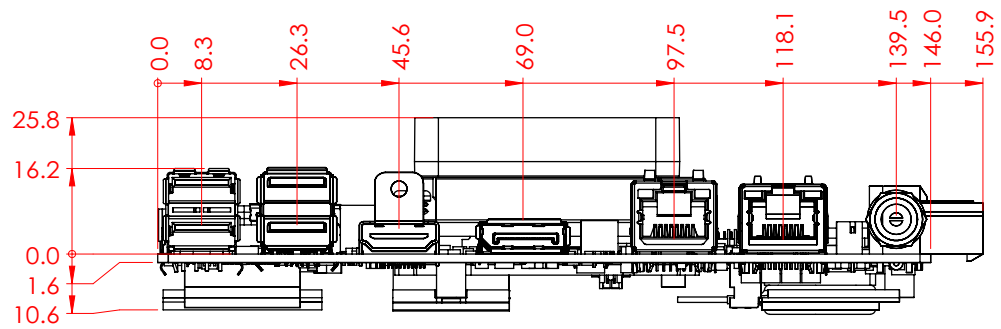


Figure 2.7 Mechanical Drawing with Cooler (Coastline)

Chapter 3

Installation

This chapter explains the setup procedures for the MIO-5354 hardware, including instructions on setting jumpers and connecting peripherals, switches, and indicators. Be sure to read all safety precautions before you begin the installation procedure.

3.1 Connector and Header List

Table 3.1: Connector and Header List

No.	Description	Location Name
1	DC input Connector	DCIN2
2	Internal USB3.1 Gen1 Connector	USB1
3	COM port Connector (RS232+RS422+RS485)	COM1
4	COM port Connector (RS232+RS422+RS485)	COM2
5	COM port Connector (RS232 only)	COM3
6	COM port Connector (RS232 only)	COM4
7	CAN Bus Connector	CANBUS1
8	CAN Bus Connector	CANBUS2
9	Audio Connector	AUDIO1
10	LVDS Connector	LVDS1
11	I2C/SMB Bus Connector	I2C_SMB1
12	FAN connector	FAN1
13	SATA Power Connector	SATAP1
14	Inverter Connector	BL1
15	GPIO Connector	GPIO1
16	Power/LED/Case Open/Buzzer Connector	FP1
17	M.2 B-Key (USB 3.0 + USB 2.0)	M2_B1
18	M.2 B-Key (SATA / PCIe x1)	M2_B2
19	M.2 B-Key (PCIe x1 + USB 2.0)	M2_E1
20	RTC Battery Connector	BAT1

3.2 Switches and Jumpers

Table 3.2: Switches and Jumpers

No.	Description	Location Name
21	Multifunction Switch	JCMOS1
22	Panel Voltage Selection	VDD1

3.3 Connector Locations

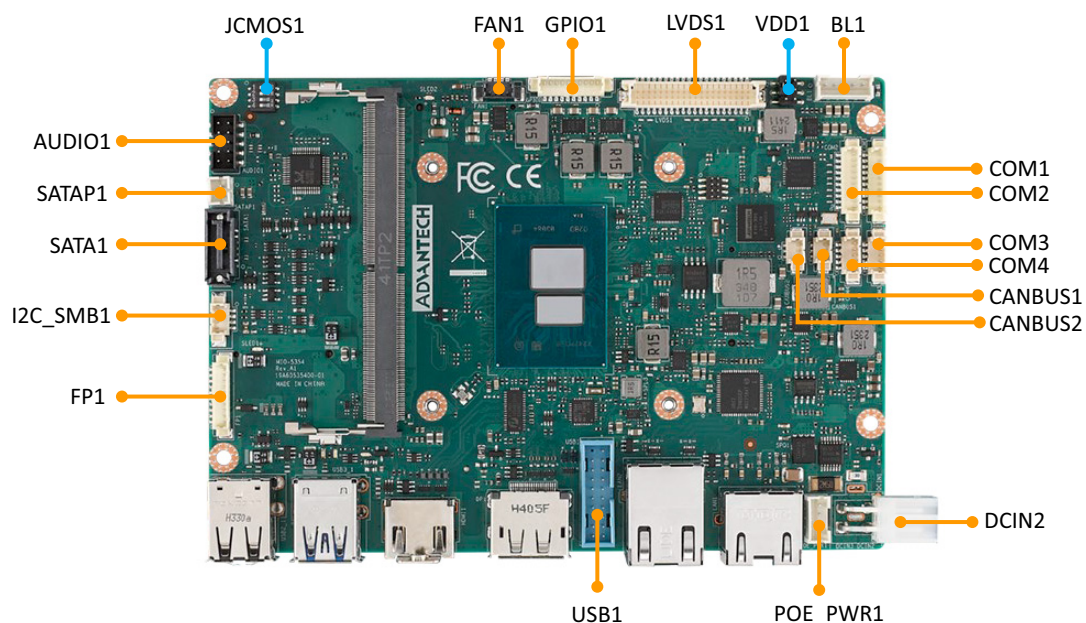


Figure 3.1 MIO-5354 Connector Locations (Top Side)

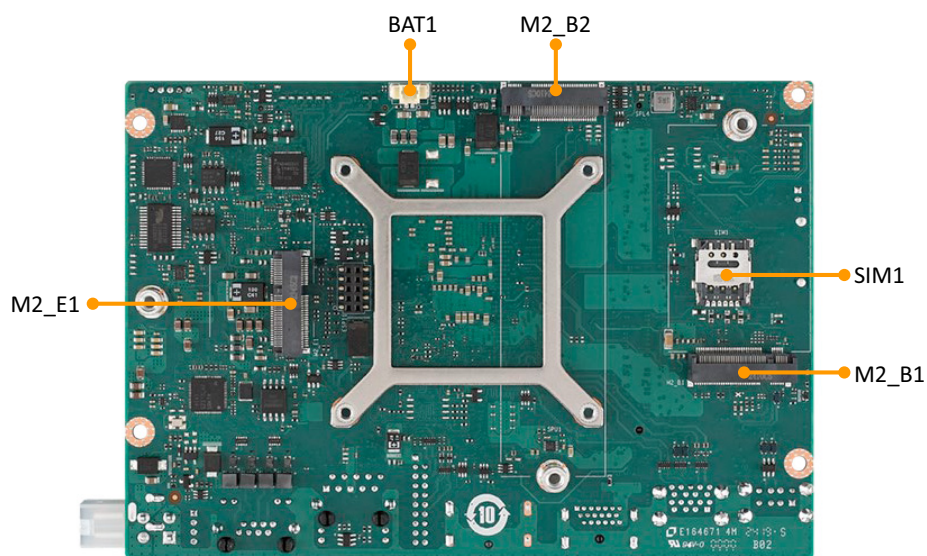
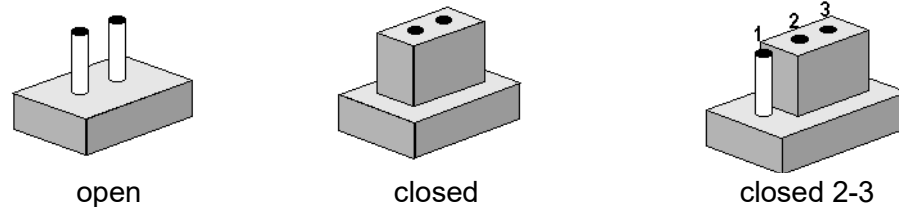


Figure 3.2 MIO-5354 Connector Locations (Bottom Side)

3.4 Setting Jumpers

You may configure your card to match the needs of your application by setting jumpers. A jumper is a metal bridge used to close an electric circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper, you connect the pins with the clip. To “open” a jumper, you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case you would connect either pins 1 and 2, or 2 and 3.

The jumper settings are schematically depicted in this manual as follows:



A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes. Generally, you simply need a standard cable to make most connections.

3.4.1 DC Input Connector (DCIN2)

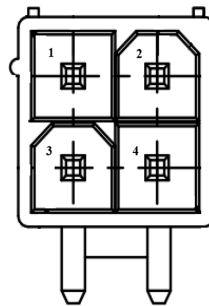


Table 3.3: DC Input Connector

Pin	Signal Pin Definition
1	GND
2	GND
3	+V12_DC_IN
4	+V12_DC_IN

3.4.2 Internal USB 3.1 Gen1 Connector (USB1)

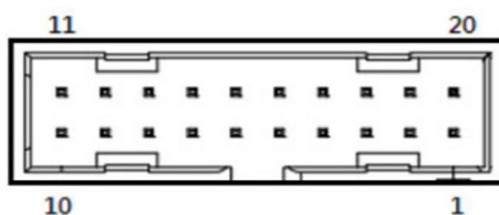


Table 3.4: Internal USB 3.1 Gen1 Connector

Pin	Signal Pin Definition
1	Vbus
2	IntA_P1_SSRX-
3	IntA_P1_SSRX+
4	GND
5	IntA_P1_SSTX-
6	IntA_P1_SSTX+
7	GND
8	IntA_P1_D-
9	IntA_P1_D+
10	NC
11	IntA_P2_D+
12	IntA_P2_D-
13	GND
14	IntA_P2_SSTX+
15	IntA_P2_SSTX-
16	GND
17	IntA_P2_SSRX+
18	IntA_P2_SSRX-
19	Vbus
20	No Pin

3.4.3 COM Port Connector (COM1)

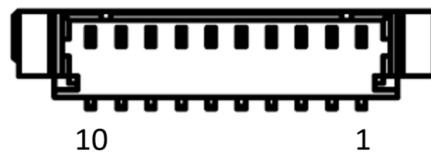


Table 3.5: COM Port Connector (COM1)

Pin	Signal Pin Definition
1	NC
2	COM1_z_RI#
3	COM1_DTR#
4	COM1_CTS#
5	COM1_TXD
6	COM1_RTS#
7	COM1_RXD
8	COM1_DSR#
9	COM1_DCD#
10	GND

3.4.4 COM Port Connector (COM2)

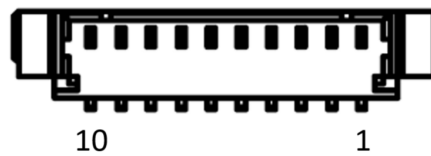


Table 3.6: COM Port Connector (COM2)

Pin	Signal Pin Definition
1	NC
2	COM2_RI#
3	COM2_DTR#
4	COM2_CTS#
5	COM2_TXD
6	COM2_RTS#
7	COM2_RXD
8	COM2_DSR#
9	COM2_DCD#
10	GND

3.4.5 COM Port Connector (COM3)



Table 3.7: COM Port Connector (COM3)

Pin	Signal Pin Definition
1	COM3_RS232-TXD
2	COM3_RS232-RTS#
3	COM3_RS232-RXD
4	COM3_RS232-CTS#
5	GND

3.4.6 COM Port Connector (COM4)



Table 3.8: COM Port Connector (COM4)

Pin	Signal Pin Definition
1	COM4_RS232-TXD
2	COM4_RS232-RTS#
3	COM4_RS232-RXD
4	COM4_RS232-CTS#
5	GND

3.4.7 CAN Bus Connector (CANBUS1)



Table 3.9: CAN Bus Connector (CANBUS1)

Pin	Signal Pin Definition
1	CAN1_D+
2	CAN1_D-
3	GND

3.4.8 CAN Bus Connector (CANBUS2)

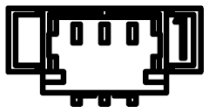


Table 3.10: CAN Bus Connector (CANBUS2)

Pin	Signal Pin Definition
1	CAN2_D+
2	CAN2_D-
3	GND

3.4.9 Audio Connector (AUDIO1)

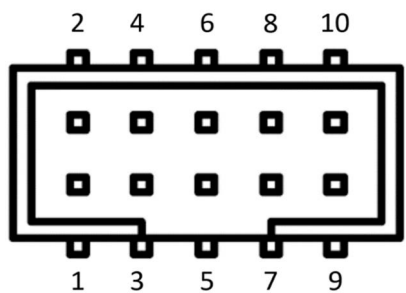


Table 3.11: Audio Connector (AUDIO1)

Pin	Signal Pin Definition
1	LOUTR
2	LINR
3	GND
4	GND
5	LOUTL
6	LINL
7	GND
8	NC
9	MIC1R
10	MIC1L

3.4.10 LVDS Connector (LVDS1)

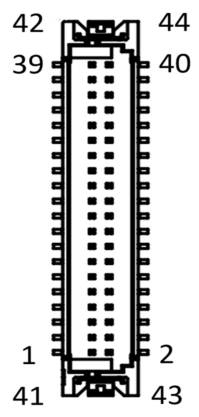


Table 3.12: LVDS Connector (LVDS1)

Pin	Signal Pin Definition
1	+V_LCD
2	+V_LCD
3	GND
4	GND
5	+V_LCD
6	+V_LCD
7	LVDS1_0_D0-
8	LVDS1_1_D0-
9	LVDS1_0_D0+
10	LVDS1_1_D0+
11	GND
12	GND
13	LVDS1_0_D1-
14	LVDS1_1_D1-
15	LVDS1_0_D1+
16	LVDS1_1_D1+
17	GND
18	GND
19	LVDS1_0_D2-
20	LVDS1_1_D2-
21	LVDS1_0_D2+
22	LVDS1_1_D2+
23	GND
24	GND
25	LVDS1_0_CLK-
26	LVDS1_1_CLK-
27	LVDS1_0_CLK+
28	LVDS1_1_CLK+
29	GND
30	GND
31	LVDS0_DDCCLK_AUX+
32	LVDS0_DDCDAT_AUX-
33	GND
34	GND
35	LVDS1_0_D3-
36	LVDS1_1_D3-
37	LVDS1_0_D3+
38	LVDS1_1_D3+
39	NC
40	LVDS1_VCON

3.4.11 I²C/SMB Connector (I²C_SMB1)

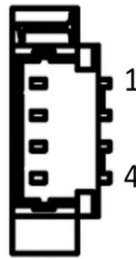


Table 3.13: I²C/SMB Connector (I²C_SMB1)

Pin	Signal Pin Definition
1	GND
2	EC_SMB0_z_DAT
3	EC_SMB0_z_CLK
4	+V3.3_DUAL

3.4.12 Fan Connector (FAN1)

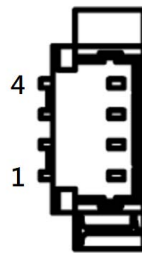


Table 3.14: Fan Connector (FAN1)

Pin	Signal Pin Definition
1	GND
2	+V12
3	FAN_SPEED
4	FAN_V5_PWM

3.4.13 SATA Power Connector (SATAP1)

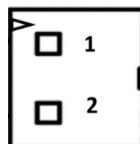


Table 3.15: SATA Power Connector (SATAP1)

Pin	Signal Pin Definition
1	5V
2	GND

3.4.14 Panel Inverter Connector (BL1)



Table 3.16: Panel Inverter Connector (BL1)

Pin	Signal Pin Definition
1	+V12_1_INVERTER_0
2	GND
3	LVDS1_Z_ENABKL
4	EC_LVDS1_Z_PWM
5	+V5_1_INVERTER_0

3.4.15 GPIO Connector (GPIO1)

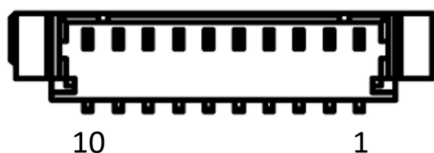


Table 3.17: GPIO Connector (GPIO1)

Pin	Signal Pin Definition
1	GND
2	SIO_GPIO7
3	SIO_GPIO2
4	SIO_GPIO6
5	SIO_GPIO1
6	SIO_GPIO5
7	SIO_GPIO0
8	SIO_GPIO4
9	+V5A_GPIO
10	SIO_GPIO3

3.4.16 Power / LED / Case Open / Buzzer Connector (FP1)

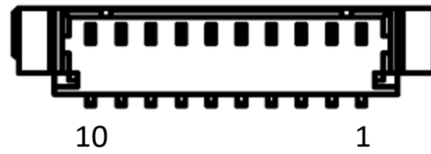


Table 3.18: Power / LED / Case Open / Buzzer Connector (FP1)

Pin	Signal Pin Definition
1	GND
2	BUZZER-
3	BUZZER+
4	CASEOPEN#
5	FP_HDD_a_LED#
6	FP_A_PSIN#
7	FP_A_RST#
8	220 ohm PU to +V3.3
9	NC
10	330 ohm PU to +V5

3.4.17 M.2 B-Key (M2_B1)

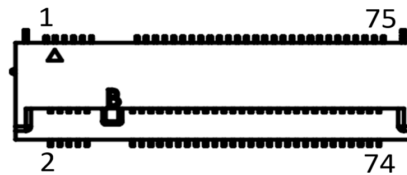


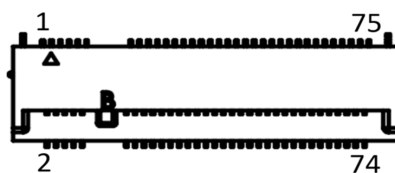
Table 3.19: M.2 B-Key (M2_B1)

Pin	Signal Pin Definition	Pin	Signal Pin Definition
74	3.3V (Suspend)	75	CONFIG_2
72	3.3V (Suspend)	73	GND
70	3.3V (Suspend)	71	GND
68	SUSCLK (3.3V)	69	CONFIG_1
66	NC	67	RESET# (1.8V)
64	NC	65	NC
62	NC	63	NC
60	NC	61	NC
58	NC	59	NC
56	NC	57	GND
54	PEWAKE# (3.3V)	55	REFCLKp
52	CLKREQ# (3.3V)	53	REFCLKn
50	PERST# (3.3V)	51	GND
48	NC	49	PERp0
46	NC	47	PERn0
44	NC	45	GND
42	NC	43	PETp0
40	NC	41	PETn0
38	NC	39	GND

Table 3.19: M.2 B-Key (M2_B1)

36	UIM_PWR	37	USB3.1-Rx+
34	UIM_DATA	35	USB3.1-Rx-
32	UIM_CLK	33	GND
30	UIM_RESET	31	USB3.1-Tx+
28	NC	29	USB3.1-Tx-
26	NC	27	GND
24	NC	25	NC
22	NC	23	NC
20	NC	21	CONFIG_0
10	LED_1# (3.3V)	11	GND
8	W_DISABLE1# (3.3V)	9	USB_D-
6	FULL_CARD_POWER_OFF# (1.8V)	7	USB_D+
4	3.3V (Suspend)	5	GND
2	3.3V (Suspend)	3	GND
		1	CONFIG_3

3.4.18 M.2 B-Key (M2_B2)

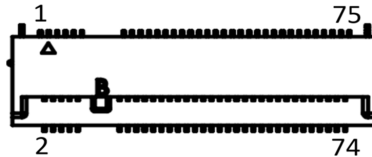
**Table 3.20: M.2 B-Key (M2_B2)**

Pin	Signal Pin Definition	Pin	Signal Pin Definition
74	3.3V (Suspend)	75	CONFIG_2
72	3.3V (Suspend)	73	GND
70	3.3V (Suspend)	71	GND
68	SUSCLK (3.3V)	69	CONFIG_1
66	NC	67	NC
64	NC	65	NC
62	NC	63	NC
60	NC	61	NC
58	NC	59	NC
56	NC	57	GND
54	PEWAKE# (3.3V)	55	REFCLKp
52	CLKREQ# (3.3V)	53	REFCLKn
50	PERST# (3.3V)	51	GND
48	NC	49	PERp0 / SATA-A+
46	NC	47	PERn0 / SATA-A-
44	NC	45	GND
42	NC	43	PETp0 / SATA-B-
40	NC	41	PETn0 / SATA-B+
38	NC	39	GND
36	NC	37	NC
34	NC	35	NC

Table 3.20: M.2 B-Key (M2_B2)

32	NC	33	GND
30	NC	31	NC
28	NC	29	NC
26	NC	27	GND
24	NC	25	NC
22	NC	23	NC
20	NC	21	CONFIG_0
10	LED_1# (3.3V)	11	GND
8	W_DISABLE1# (3.3V)	9	NC
6	FULL_CARD_POWER_OFF# (1.8V)	7	NC
4	3.3V (Suspend)	5	GND
2	3.3V (Suspend)	3	GND
		1	CONFIG_3

3.4.19 M.2 E-Key (M2_E1)

**Table 3.21: M.2 E-Key (M2_E1)**

Pin	Signal Pin Definition	Pin	Signal Pin Definition
74	3.3V (Suspend)	75	GND
72	3.3V (Suspend)	73	NC
70	NC	71	NC
68	NC	69	GND
66	NC	67	NC
64	NC	65	NC
62	NC	63	GND
60	NC	61	NC
58	NC	59	NC
56	W_DISABLE1# (3.3V)	57	GND
54	W_DISABLE2# (3.3V)	55	PEWAKE0# (3.3V)
52	PERST0# (3.3V)	53	CLKREQ0# (3.3V)
50	SUSCLK (3.3V)	51	GND
48	NC	49	REFCLKn0
46	NC	47	REFCLKp0
44	NC	45	GND
42	NC	43	PETn0
40	NC	41	PETp0
38	NC	39	GND
36	NC	37	PERn0
34	NC	35	PERp0
32	NC	33	GND
29	NC	29	NC

Table 3.21: M.2 E-Key (M2_E1)			
30	M2B1_SATA_DEVSLP_R	30	M2B1_SATA_DEVSLP_R
31	GND	31	GND
32	NC	32	NC
22	NC	23	NC
20	NC	21	NC
18	GND	19	NC
16	NC	17	NC
14	NC	15	NC
12	NC	13	NC
10	NC	11	NC
8	NC	9	NC
6	NC	7	GND
4	3.3V (Suspend)	5	USB_D-
2	3.3V (Suspend)	3	USB_D+
		1	GND

3.4.20 RTC Battery Connector (BAT1)

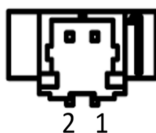


Table 3.22: RTC Battery Connector (BAT1)	
Pin	Signal Pin Definition
1	+VBAT_b1
2	GND

3.4.21 Multifunction Switch (JCMOS1)

Table 3.23: Multifunction Switch (JCMOS1)		
Function	Switch Settings	
AT/ATX selection		
	*AT mode	ATX mode
Load CMOS Date		
	*Normal	Load BIOS Default
COM1 TERM RX Enable		
	*Disable	Enable
COM2 TERM RX Enable		
	*Disable	Enable
*Default Setting		

3.4.22 Panel Voltage Selection (VDD1)

Table 3.24: Panel Voltage Selection

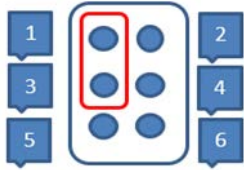
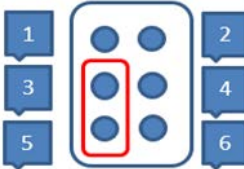
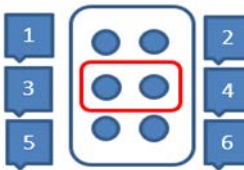
Function	Jumper Setting
Panel Voltage Setting: +V3.3 (Default)	
Panel Voltage Setting: +V5	
Panel Voltage Setting: +V12	

Table 3.25: Panel Voltage Selection (VDD1)

Pin	Signal Pin Definition
1	+V3.3
2	NC
3	+V_LVDS_LCD
4	+V12
5	+V5
6	NC

Chapter 4

AMI BIOS Setup

AMIBIOS has been integrated into a plethora of motherboards for decades. With the AMIBIOS Setup program, you can modify BIOS settings and control various system features. This chapter describes the basic navigation of the MIO-5354 BIOS setup screens.



AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in battery-backed CMOS so it retains the setup information when the power is turned off.

4.1 Entering Setup

Turn on the computer and check for the patch code. If there is a number assigned to the patch code, it means that the BIOS supports your CPU. If there is no number assigned to the patch code, please contact an Advantech application engineer to obtain an up-to-date patch code file. This will ensure that your CPU's system status is valid. After ensuring that you have a number assigned to the patch code, press and you will immediately be allowed to enter Setup.

4.1.1 Main Setup

When you first enter the BIOS Setup Utility, you will encounter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

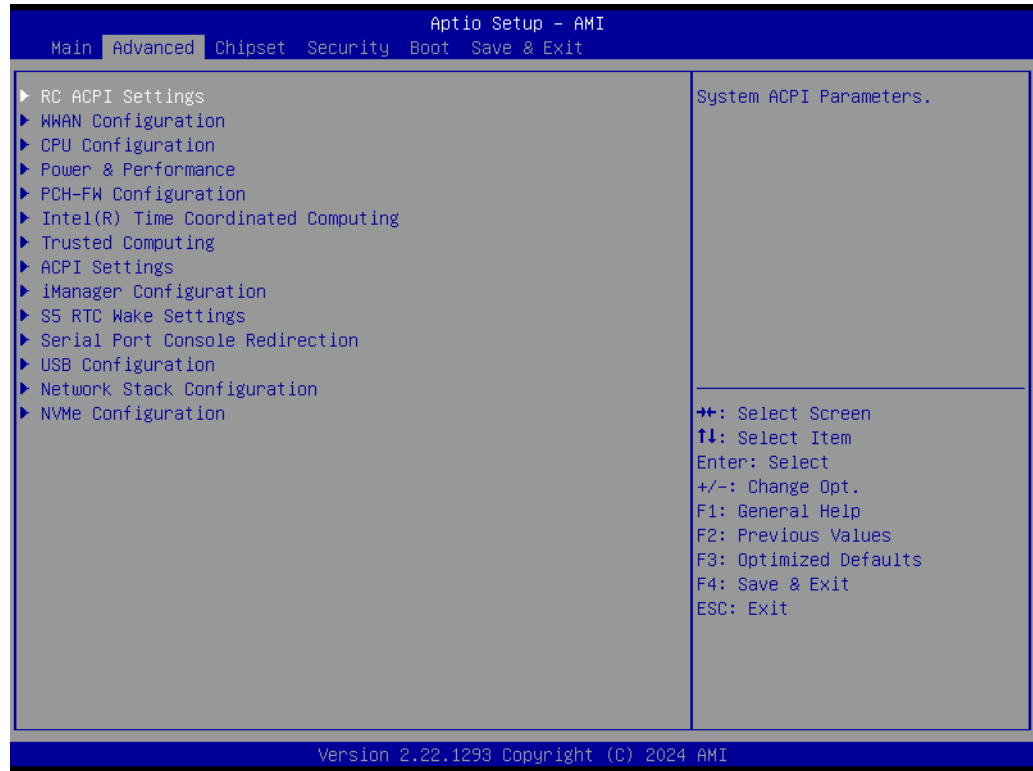
■ System Time / System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard.

Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

4.1.2 Advanced BIOS Features Setup

Select the Advanced tab from the MIO-5354 Setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub-menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screens are shown below. The sub-menus are described on the following pages.



4.1.2.1 RC ACPI Settings



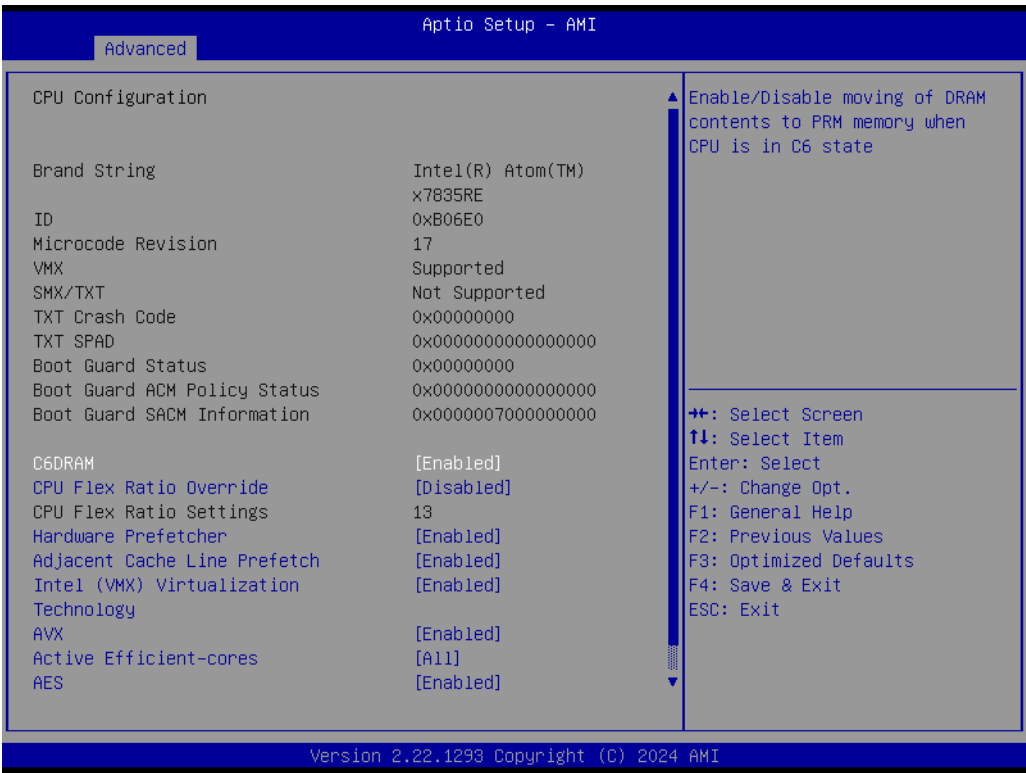
- **PTID Support**
Enable/Disable to load the PTID Table.
- **Native PCIE Enable**
Enable/Disable PCIE Native Control reported in the ACPI Table.
- **Native ASPM**
Choose if the ASPM feature is controlled by the OS or BIOS.
- **BDAT ACPI Table Support**
Enable/Disable support for the BDAT ACPI Table.
- **Low Power S0 Idle Capability**
Enable/Disable ACPI Low Power S0 Idle Capability under the OS.

4.1.2.2 WWAN Configuration



- **WWAN Device**
Select the M.2 WWAN Device options to enable 5G-M80 (MediaTek) Modems.

4.1.2.3 CPU Configuration



- **C6DRAM**

Enable/Disable moving of DRAM contents to PRM memory when the CPU is in C6 state.

■ **CPU Flex Ratio Override**

Enable/Disable CPU Flex Ratio Programming.

■ **Hardware Prefetcher**

This item allows users to enable or disable the hardware prefetcher feature.

■ **Adjacent Cache Line Prefetch**

This item allows users to enable or disable the adjacent cache line prefetch feature.

■ **Intel® (VMX) Virtualization Technology**

When Enabled, a VMM can utilize the additional hardware capability provided by Vanderpool Technology.

■ **AVX**

Enable/Disable the AVX 2/3 Instructions.

■ **Active Efficient-cores**

Number of E-cores to enable in each processor package.

■ **AES**

Enable/Disable AES (Advanced Encryption Standard).

■ **MachineCheck**

Enable/Disable Machine Check.

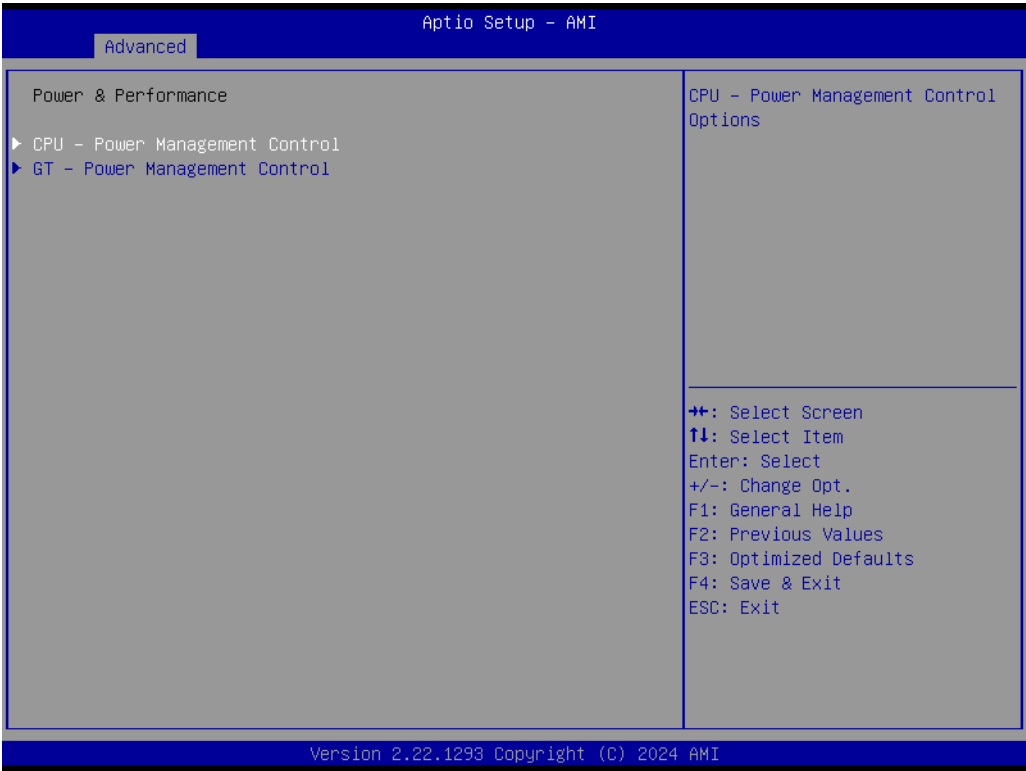
■ **MonitorMWait**

Enable/Disable MonitorMWait.

■ **Intel® Trusted Execution Technology**

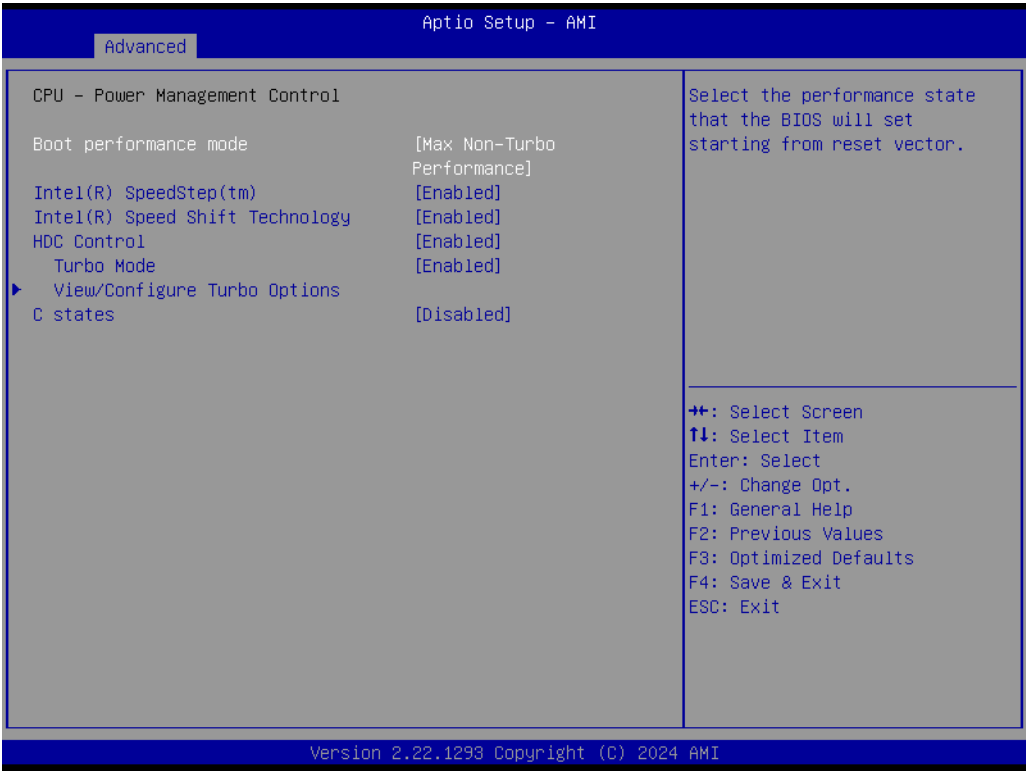
Enables utilization of additional hardware capability provided by Intel® Trusted Execution Technology.

4.1.2.4 Power & Performance



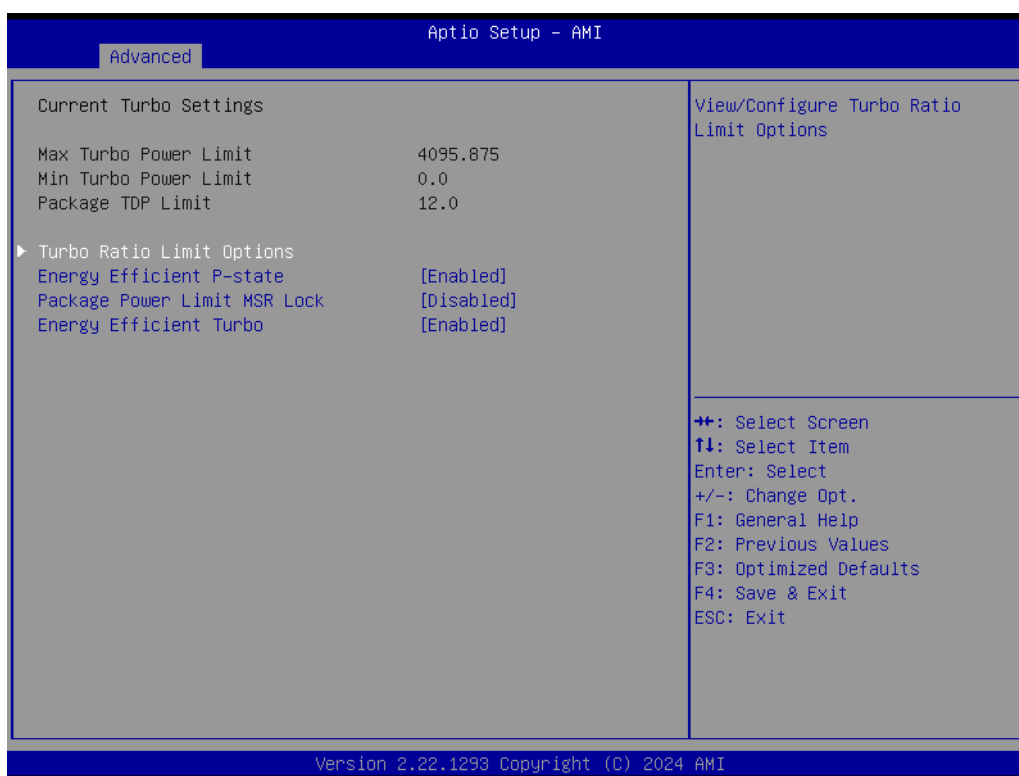
- **CPU – Power Management Control**
CPU – Power Management Control Options.
- **GT – Power Management Control**
GT – Power Management Control Options.

CPU - Power Management Control



- **Boot Performance mode**
Select the performance state that the BIOS will set before OS handoff.
- **Intel® SpeedStep™**
Allows more than two frequency ranges to be supported.
- **Intel® Speed Shift Technology**
Enable/Disable Intel® Speed Shift Technology support.
- **HDC Control**
Enable/Disable Intel HDC.
- **Turbo Mode**
Enable/Disable processor turbo mode.
- **View/Configure Turbo Options**
View and Configure Turbo Options.
- **C states**
Enable/Disable CPU Power Management.

View/Configure Turbo Options



- **Turbo Ratio Limit Option**
View/Configure Turbo Ratio Limit Options.
- **Energy Efficient P-state**
Enable/Disable the Energy Efficient P-state feature.
- **Package Power Limit MSR Lock**
Enable/Disable locking of Package Power Limit settings.
- **Energy Efficient Turbo**
Enable/Disable the Energy Efficient Turbo feature.

■ Current Turbo Ratio Limit Settings

Aptio Setup - AMI

Advanced

Current Turbo Ratio Limit Settings				
E-core Turbo Ratio Limit	Numcore0	1		
E-core Turbo Ratio Limit	Numcore1	2		
E-core Turbo Ratio Limit	Numcore2	3		
E-core Turbo Ratio Limit	Numcore3	4		
E-core Turbo Ratio Limit	Numcore4	5		
E-core Turbo Ratio Limit	Numcore5	6		
E-core Turbo Ratio Limit	Numcore6	7		
E-core Turbo Ratio Limit	Numcore7	8		
E-core Turbo Ratio Limit	Ratio0	36		
E-core Turbo Ratio Limit	Ratio1	35		
E-core Turbo Ratio Limit	Ratio2	33		
E-core Turbo Ratio Limit	Ratio3	33		
E-core Turbo Ratio Limit	Ratio4	30		
E-core Turbo Ratio Limit	Ratio5	30		
E-core Turbo Ratio Limit	Ratio6	30		
E-core Turbo Ratio Limit	Ratio7	30		
E-core Turbo Ratio Limit	Numcore0	1		
E-core Turbo Ratio Limit	Numcore1	2		
E-core Turbo Ratio Limit	Numcore2	3		
E-core Turbo Ratio Limit	Numcore3	4		
E-core Turbo Ratio Limit	Numcore4	5		
E-core Turbo Ratio Limit	Numcore5	6		

Efficient-core Turbo Ratio Limit Numcore0 defines the core range, the turbo ratio is defined in E-core Turbo Ratio Limit Ratio0. If value is zero, this entry is ignored.

++: Select Screen
 ↑↓: Select Item
 Enter: Select
 +/-: Change Opt.
 F1: General Help
 F2: Previous Values
 F3: Optimized Defaults
 F4: Save & Exit
 ESC: Exit

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Advanced

E-core Turbo Ratio Limit	Ratio0	36		
E-core Turbo Ratio Limit	Ratio1	35		
E-core Turbo Ratio Limit	Ratio2	33		
E-core Turbo Ratio Limit	Ratio3	33		
E-core Turbo Ratio Limit	Ratio4	30		
E-core Turbo Ratio Limit	Ratio5	30		
E-core Turbo Ratio Limit	Ratio6	30		
E-core Turbo Ratio Limit	Ratio7	30		
E-core Turbo Ratio Limit	Numcore0	1		
E-core Turbo Ratio Limit	Numcore1	2		
E-core Turbo Ratio Limit	Numcore2	3		
E-core Turbo Ratio Limit	Numcore3	4		
E-core Turbo Ratio Limit	Numcore4	5		
E-core Turbo Ratio Limit	Numcore5	6		
E-core Turbo Ratio Limit	Numcore6	7		
E-core Turbo Ratio Limit	Numcore7	8		
E-core Turbo Ratio Limit	Ratio0	36		
E-core Turbo Ratio Limit	Ratio1	35		
E-core Turbo Ratio Limit	Ratio2	33		
E-core Turbo Ratio Limit	Ratio3	33		
E-core Turbo Ratio Limit	Ratio4	30		
E-core Turbo Ratio Limit	Ratio5	30		
E-core Turbo Ratio Limit	Ratio6	30		
E-core Turbo Ratio Limit	Ratio7	30		

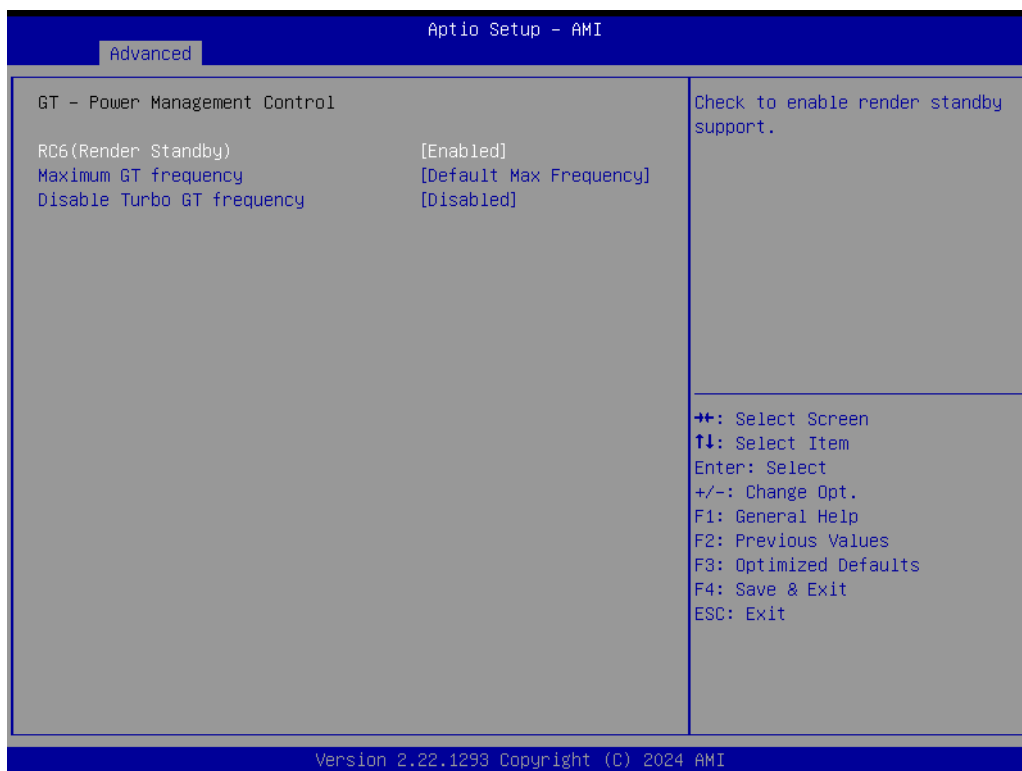
Efficient-core Turbo Ratio Limit Ratio7 defines the turbo ratio (max is 85 irrespective of the core extension mode), the core range is defined in E-core Turbo Ratio Limit Numcore7.

++: Select Screen
 ↑↓: Select Item
 Enter: Select
 +/-: Change Opt.
 F1: General Help
 F2: Previous Values
 F3: Optimized Defaults
 F4: Save & Exit
 ESC: Exit

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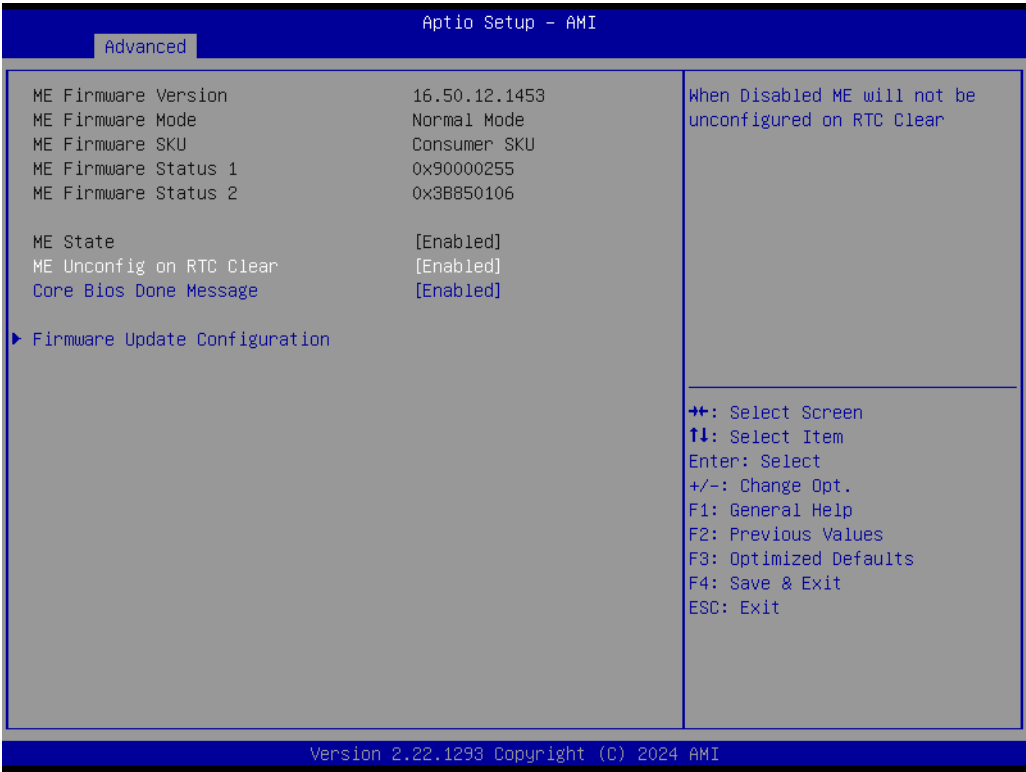
- E-core Turbo Ratio Limit Numcore x
 Efficient-core Turbo Ratio Limit Numcore x defines the core range.

GT - Power Management Control



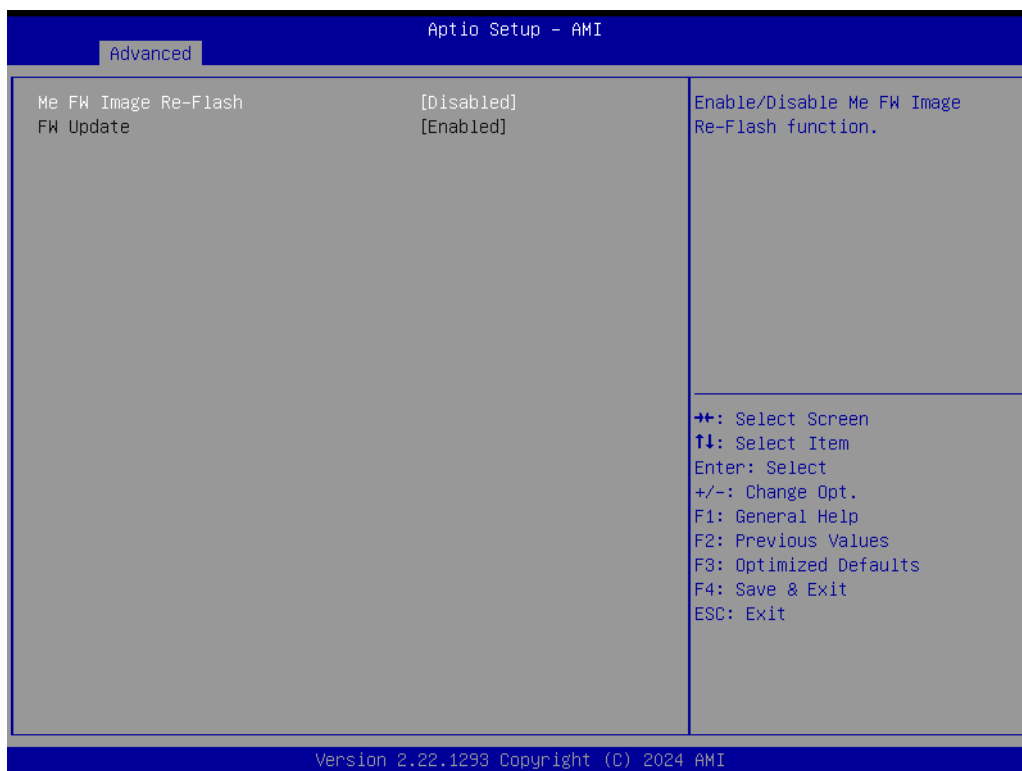
- **RC6(Render Standby)**
Check to enable render standby support.
- **Maximum GT frequency**
Maximum GT frequency limited by user.
- **Disable Turbo GT frequency**
Enable/Disable Turbo GT frequency.

4.1.2.5 PCH-FW Configuration



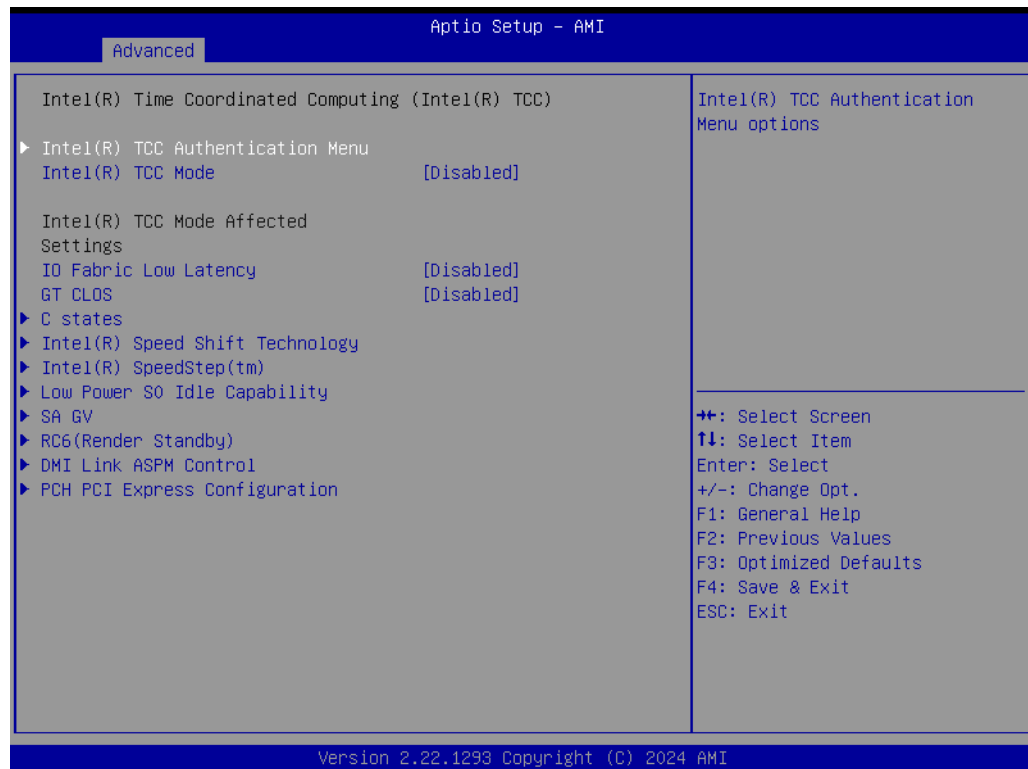
- **ME State**
When Disabled, ME will be put ME into Temporarily Disabled Mode.
- **ME Unconfig on RTC Clear**
When Disabled, ME will not be unconfigured on RTC Clear.
- **Core BIOS Done Message**
Enable/Disable Core BIOS Done message sent to ME.
- **Firmware Update Configuration**
Configure Management Engine Technology Parameters.

Firmware Update Configuration



- ME FW Image Re-Flash
Enable/Disable ME FW Image Re-Flash function.
- FW Update
Enable/Disable ME FW Update function.

4.1.2.6 Intel® Time Coordinated Computing (Intel® TCC)



- **Intel® TCC Authentication Menu**
Intel® TCC Authentication Menu Options
- **Intel® TCC Mode**
Enable or Disable Intel® TCC Mode. When enabled, this will modify system settings to improve real-time performance. The full list of settings and their current state are displayed below when Intel® TCC mode is enabled.
- **Intel® TCC Mode Affected Settings**
- **IO Fabric Low Latency**
Enable or Disable IO Fabric Low Latency. This will turn off some power management in the PCH IO fabrics. This option provides the most aggressive IO Fabric performance setting. S3 state is NOT supported.
- **GT CLOS**
Enable or Disable Graphics Technology (GT) Class of Service. Enable will reduce Gfx LLC allocation to minimize impact of Gfx workload on LLC.
- **C state**
Enable/Disable CPU Power Management. Allow CPU to go to C states when it's not 100% utilized.
- **Intel® Speed Shift Technology**
Enable/Disable Intel® Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.
- **Intel® SpeedStep™**
Allow more than two frequency ranges to be supported.
- **Low Power S0 Idle Capability**
This variable determines if we enable ACPI Lower Power S0 Idle Capability (Mutually exclusive with Smart connect). While this is enabled, it also disables the 8254 timer for SLP_S0 support.

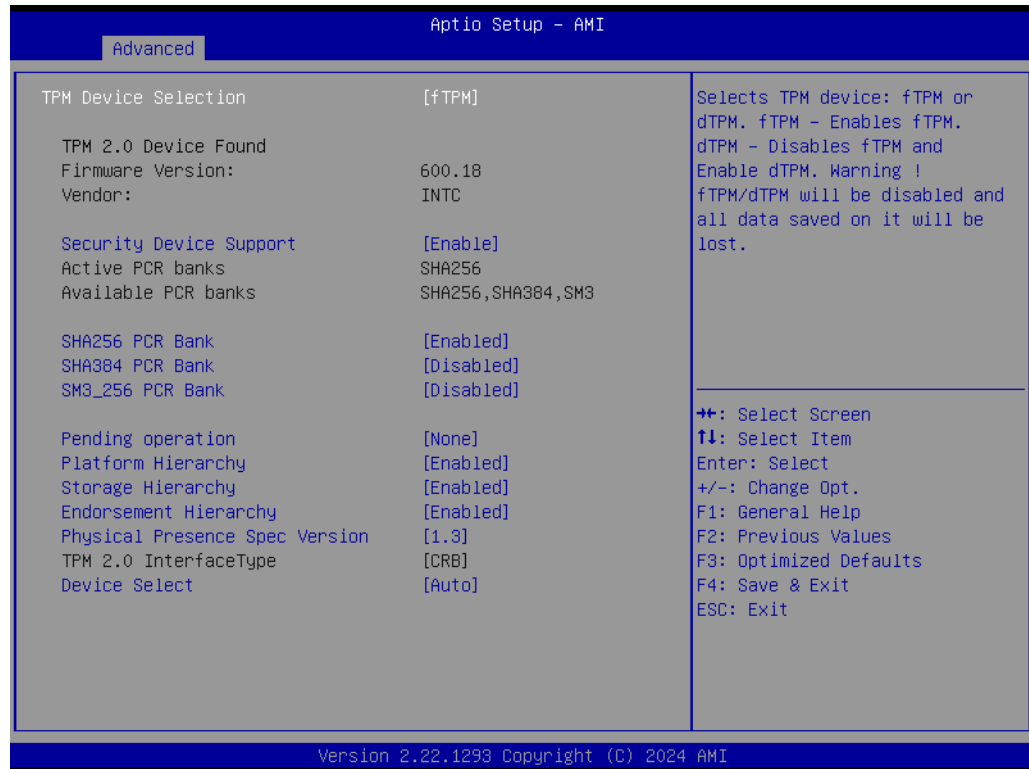
- **SA GV**
System Agent Geyserville. This can disable, fix to a specific point, or enable frequency switching.
- **RC6 (Render Standby)**
Check to enable render standby support.
- **DMI Link ASPM Control**
The control of Active State Power Management of the DMI Link.
- **PCH PCI Express Configuration**
PCI Express Configuration Setting.

Intel® TCC Authentication



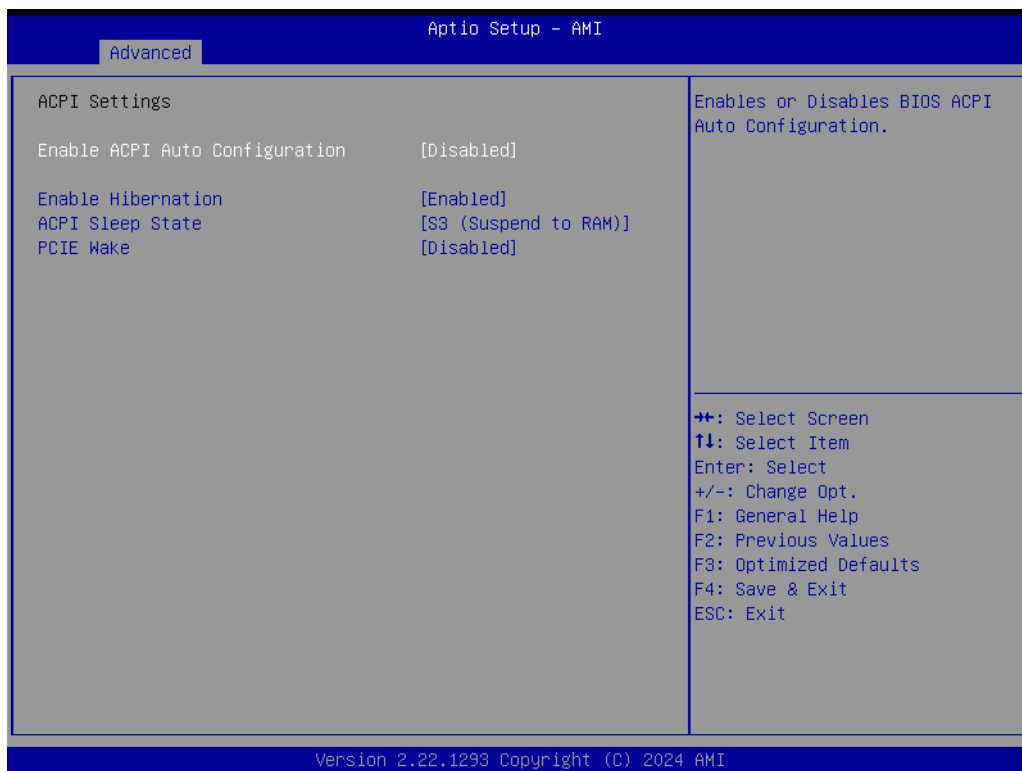
- Intel® TCC Authentication determines the key to be used. OEM Enrolled Key is built in by the OEM. Non-OEM Enrolled Key can be added by the user.

4.1.2.7 Trusted Computing



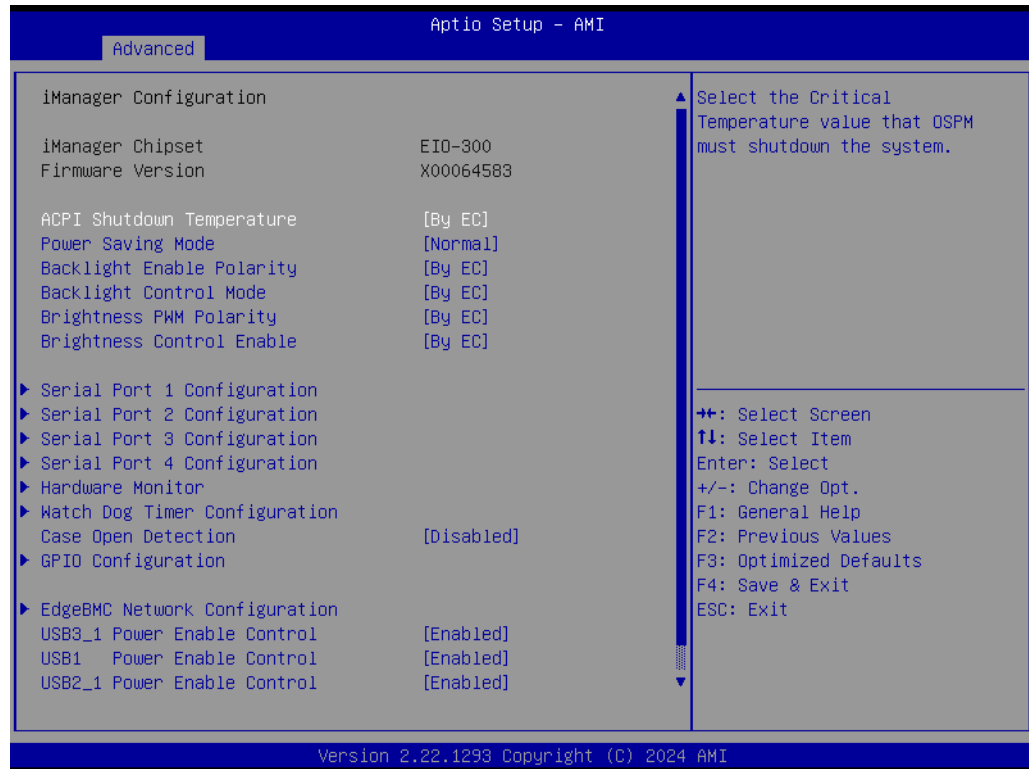
- **TPM Device Selection**
Select TPM device: fTPM or dTPM.
- **Security Device Support**
Enable or disable BIOS support for a security device.
- **SHA-1 PCR Bank**
Enable or Disable SHA-1 PCR Bank.
- **SHA256 PCR Bank**
Enable or Disable SHA256 PCR Bank.
- **SHA384 PCR Bank**
Enable or Disable SHA384 PCR Bank.
- **Pending operation**
Schedule an Operation for the Security Device.
- **Platform Hierarchy**
Enable or Disable Platform Hierarchy.
- **Storage Hierarchy**
Enable or Disable Storage Hierarchy.
- **Endorsement Hierarchy**
Enable or Disable Endorsement Hierarchy.
- **Physical Presence Spec Version**
Select to tell the OS to support PPI Spec Version 1.2 or 1.3.
- **TPM 2.0 Interface Type**
- **Device Select**
TPM 1.2 will restrict support to TPM 1.2 devices. TPM 2.0 will restrict support to TPM 2.0 devices. Auto will support both with the default set to TPM 2.0 devices. If not found, TPM 1.2 devices will be enumerated.

4.1.2.8 ACPI Settings



- **Enable ACPI Auto Configuration**
Enable or Disable BIOS ACPI auto configuration.
- **Enable Hibernation**
Enables or Disables the system ability to hibernate (OS/S4 Sleep State). This option may not be effective with some OS.
- **ACPI Sleep State**
Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
- **PCIe Wake**
Enable or disable PCIe to wake the system from S5.

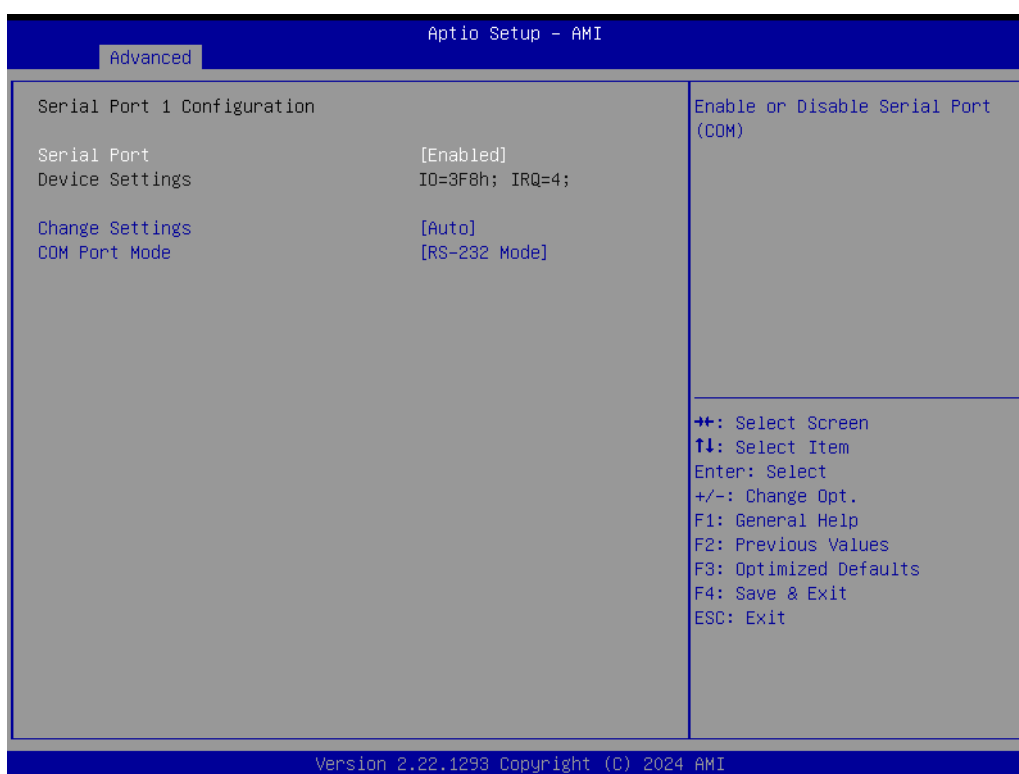
4.1.2.9 iManager Configuration



- **ACPI Shutdown Temperature**
Select the Critical Temperature value at which the OSPM must shut down the system.
- **Power Saving Mode**
Select Power Saving Mode.
- **Backlight Enable Polarity**
Switch Backlight Enable Polarity for Native or Invert.
- **Backlight Control Mode**
Switch Backlight Control to PWM or DC mode.
- **Brightness PWM Polarity**
Backlight Control Brightness PWM Polarity for Native or Invert.
- **Brightness Control Enable**
Choose to control the LVDS brightness value by EC or User override during the POST stage.
- **Serial Port 1 Configuration**
Set Parameters of Serial Port 1 (COMA).
- **Serial Port 2 Configuration**
Set Parameters of Serial Port 2 (COMB).
- **Serial Port 3 Configuration**
Set Parameters of Serial Port 3 (COMC).
- **Serial Port 4 Configuration**
Set Parameters of Serial Port 4 (COMD).
- **Hardware Monitor**
Monitor hardware Status.
- **Watch Dog Timer Configuration**

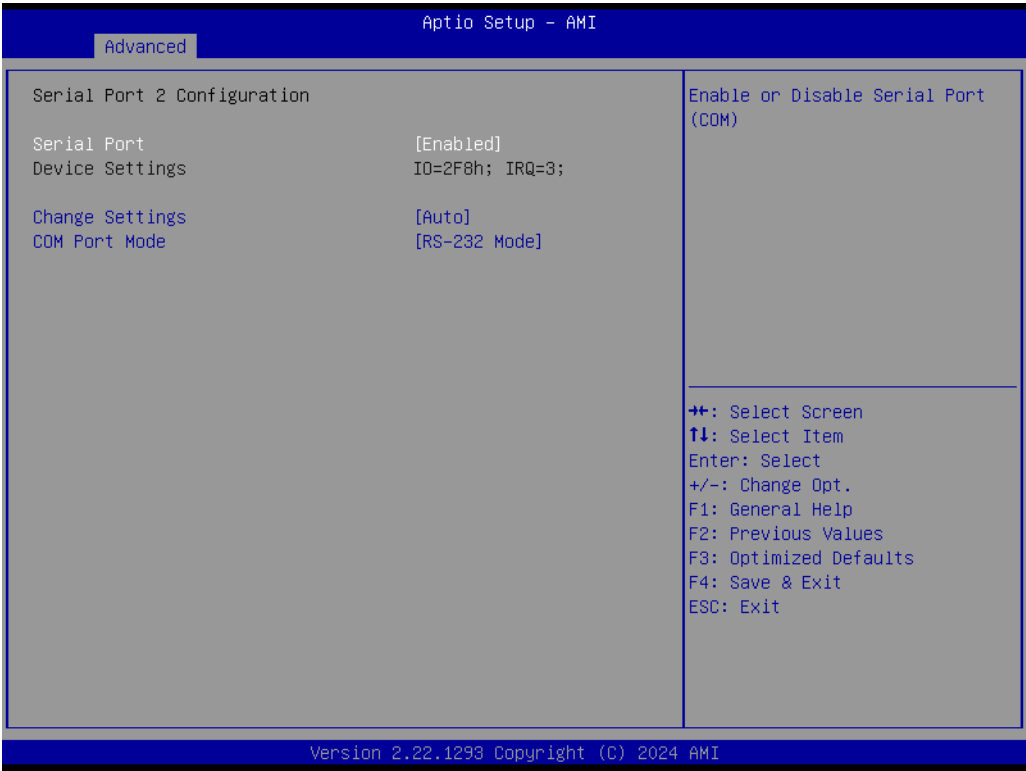
- Watch Dog Timer Configuration Page.
- **Case Open Detection**
Enable or Disable Case Open Detect Function.
- **GPIO Configuration**
GPIO Configuration Settings.
- **EdgeBMC Network Configuration**
Configure EdgeBMC Network Parameters.
- **USB3_1 Power Enable Control 1/2/3**
Enable or Disable USB3_1 Rear Port Power in S4/S5.
- **USB1 Power Enable Control 1/2/3**
Enable or Disable USB1 Internal Port Power in S4/S5.
- **USB2_1 Power Enable Control 1/2/3**
Enable or Disable USB2_1 Rear Port Power in S4/S5.

Serial Port 1 Configuration



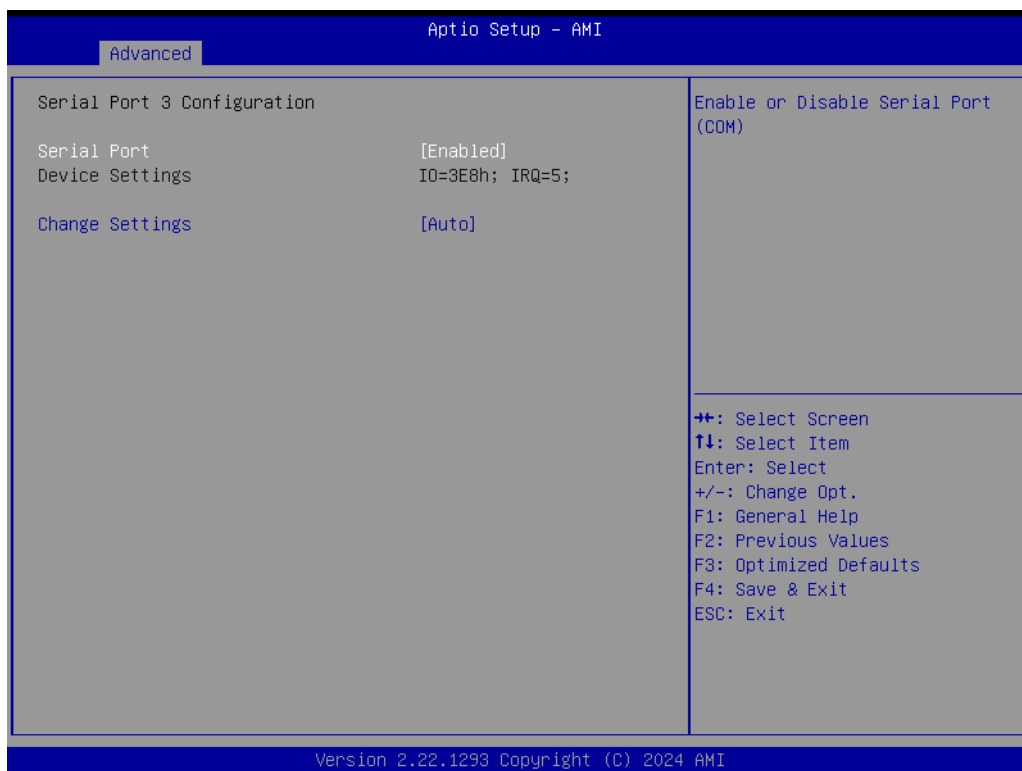
- **Serial Port**
Enable or Disable Serial Port (COM).
- **Change Settings**
Select an optimal settings for a Super IO device.
- **COM Port Mode**
COM Port Mode Select.

Serial Port 2 Configuration



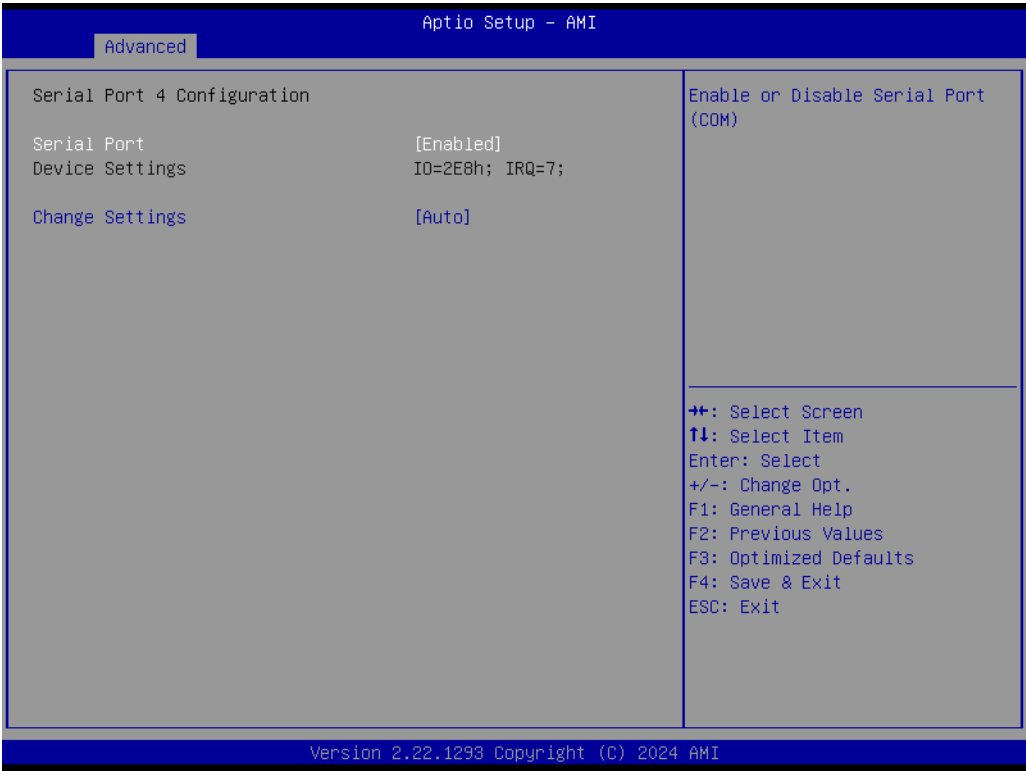
- **Serial Port**
Enable or Disable Serial Port (COM).
- **Change Settings**
Select an optimal setting for a Super IO device.
- **COM Port Mode**
COM Port Mode Select.

Serial Port 3 Configuration



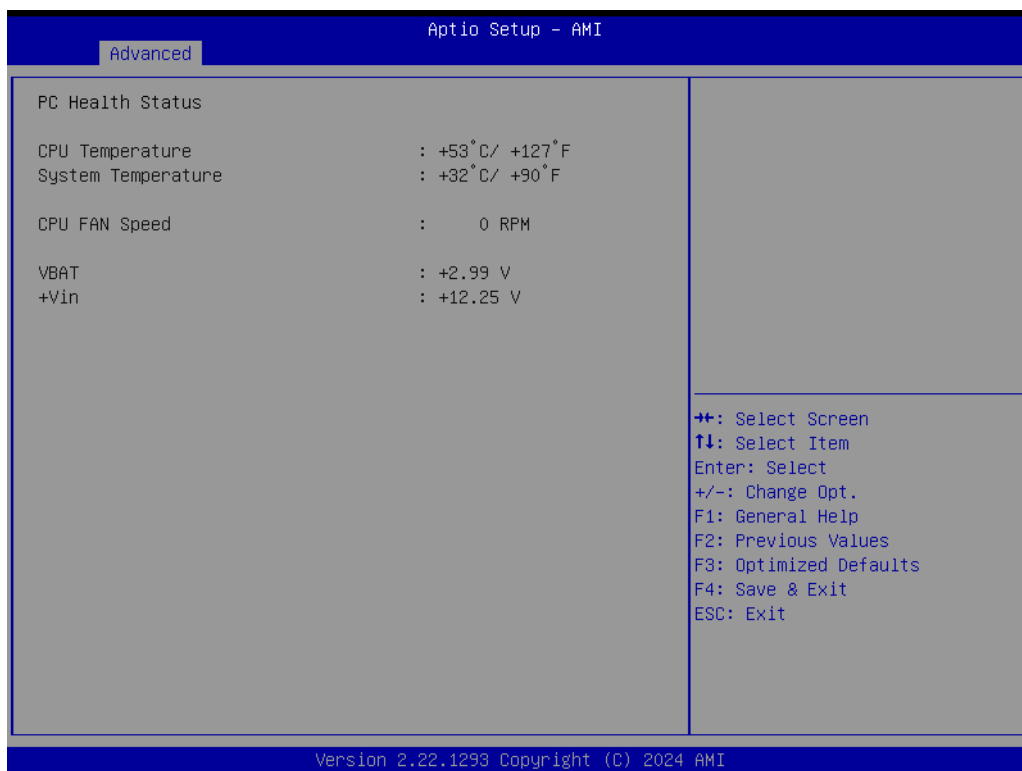
- **Serial Port**
Enable or Disable Serial Port (COM).
- **Change Settings**
Select optimal settings for a Super IO device.

Serial Port 4 Configuration



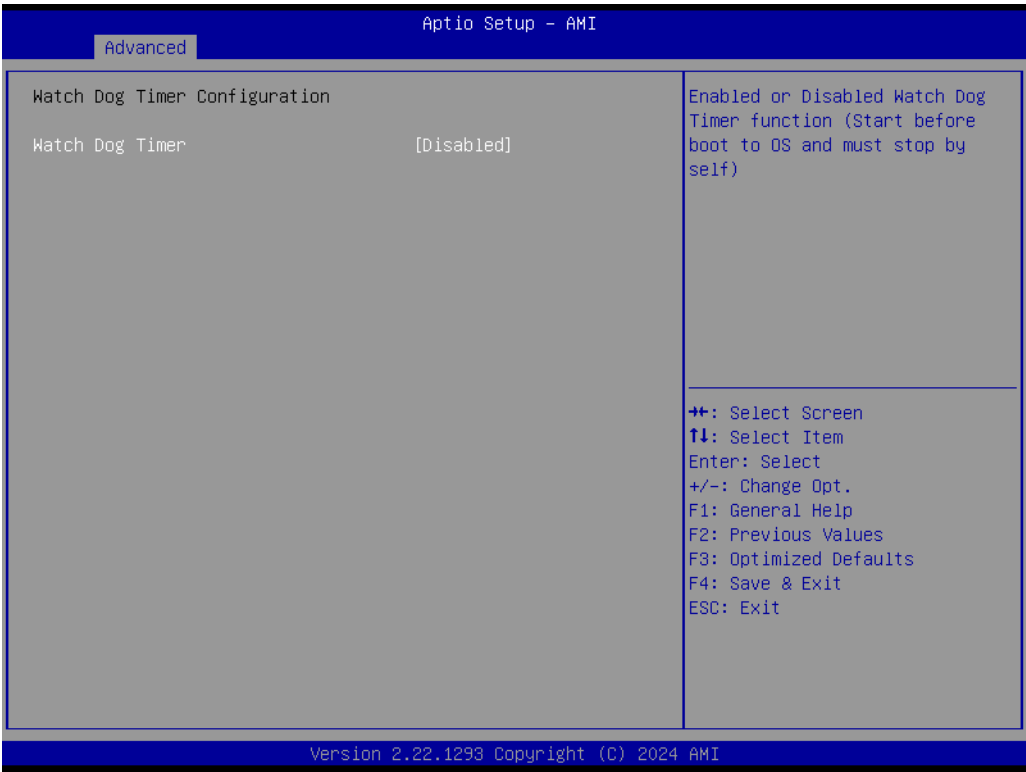
- **Serial Port**
Enable or Disable Serial Port (COM).
- **Change Settings**
Select optimal settings for a Super IO device.

HW Monitor



- **CPU Temperature**
- **System Temperature**
- **CPU FAN Speed**
- **VBAT**
The Voltage of RTC Battery.
- **+Vin**
The Voltage of System DC-IN.

Watch Dog Timer Configuration



- **Watch Dog Timer**
Enabled or Disabled Watch Dog Timer Function (Start before boot to OS and must stop by self).

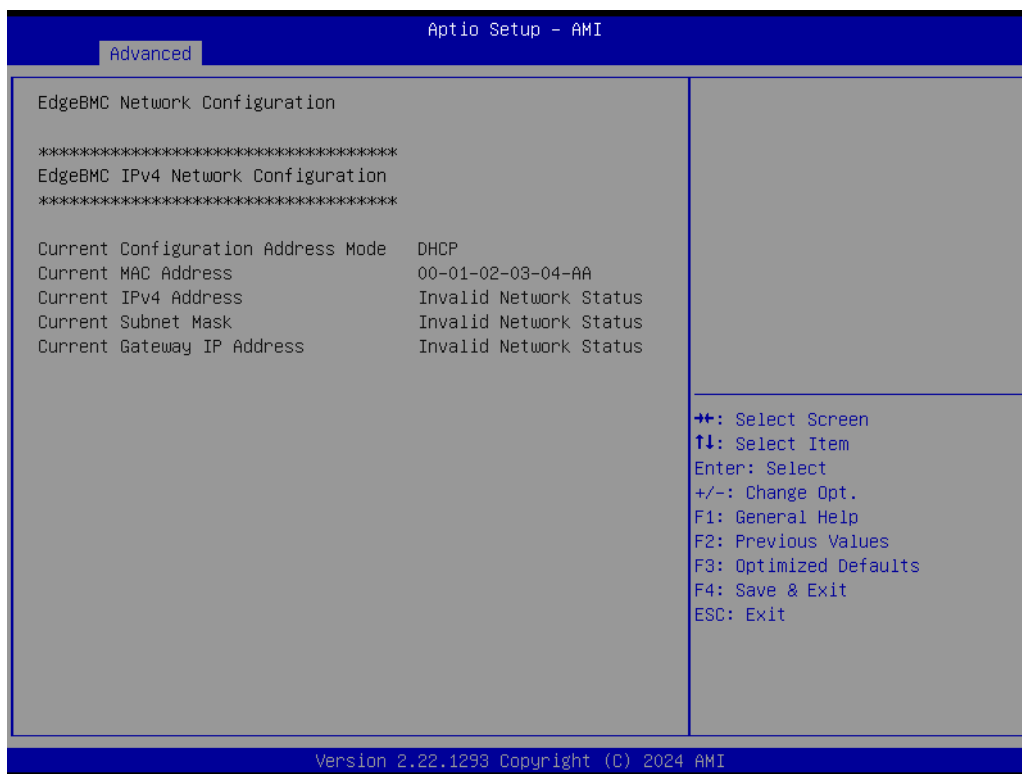
GPIO Configuration



■ GPIO Control Enable

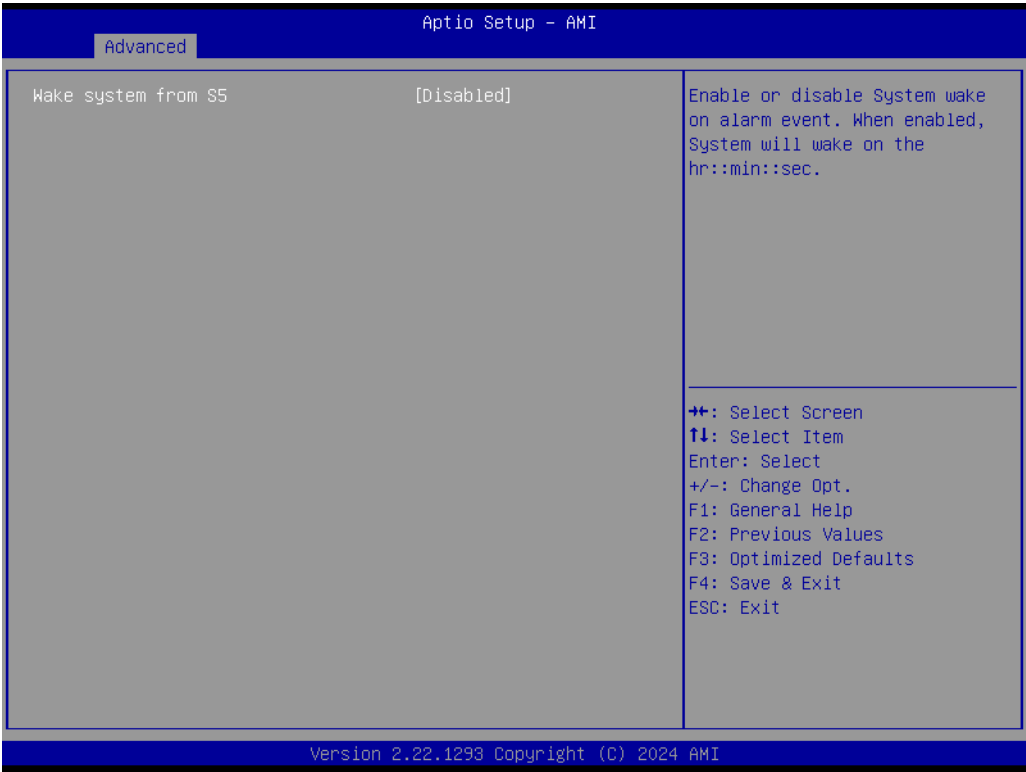
Choose to control GPIO by EC or user override during POST stage.

EdgeBMC Network Configuration



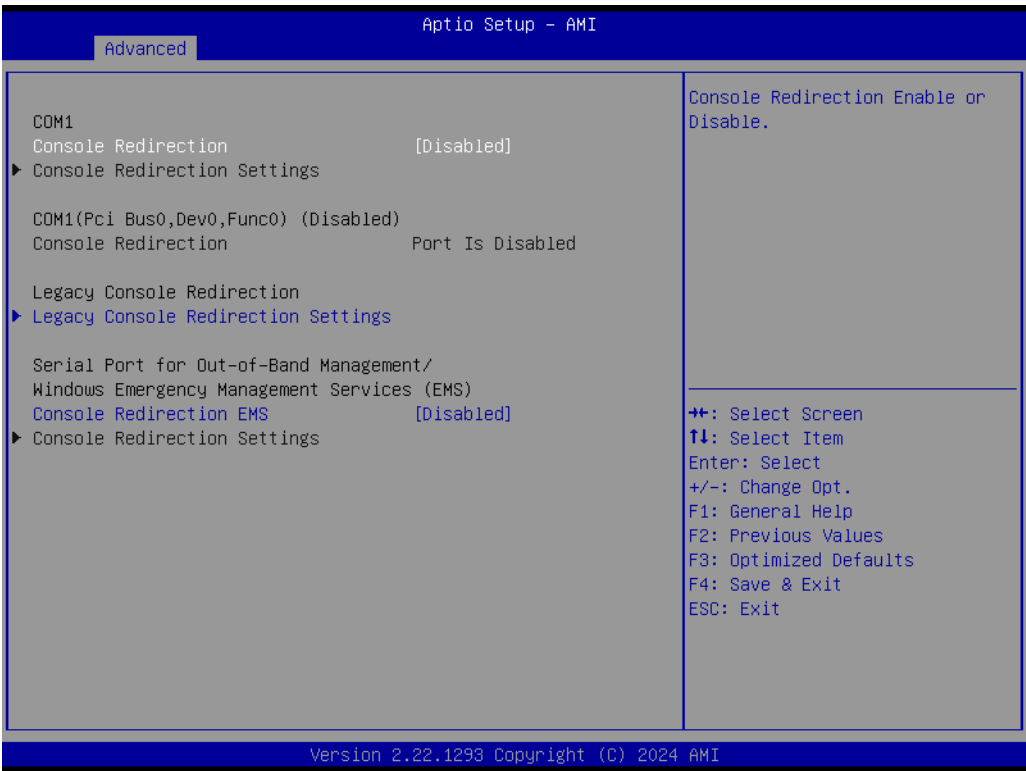
■ EdgeBMC Network Configuration

4.1.2.10 S5 RTC Wake Settings



- **Wake system from S5**
Enable/Disable System wake-on-alarm event. Select FixedTime for the system to wake at the hr:min:sec specified.

4.1.2.11 Serial Port Console Redirection



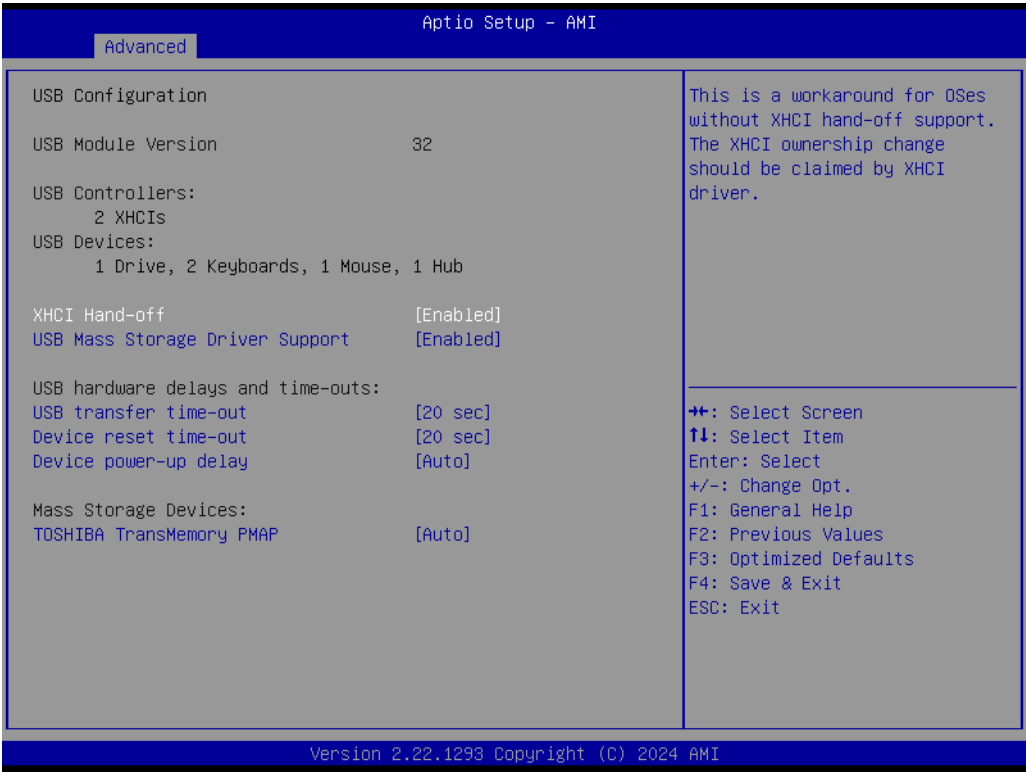
- **Console Redirection**
This item allows users to enable or disable console redirection for Microsoft Windows Emergency Management Services (EMS).
- **Legacy Console Redirection**
This item allows users to configure legacy console redirection detail settings.
- **Console Redirection EMS**
This item allows users to enable or disable console redirection for Microsoft Windows Emergency Management Services (EMS).

Legacy Console Redirection Settings



- **Redirection COM port**
Select a COM port to display redirection of Legacy OS and Legacy OPRM Messages.
- **Resolution**
On Legacy OS, the Number of Rows and Columns supported redirection
- **Redirect After POST**
When Bootloader is selected, the Legacy Console Redirection is disabled before booting to a legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting fir this option is set to Always Enable.

4.1.2.12 USB Configuration



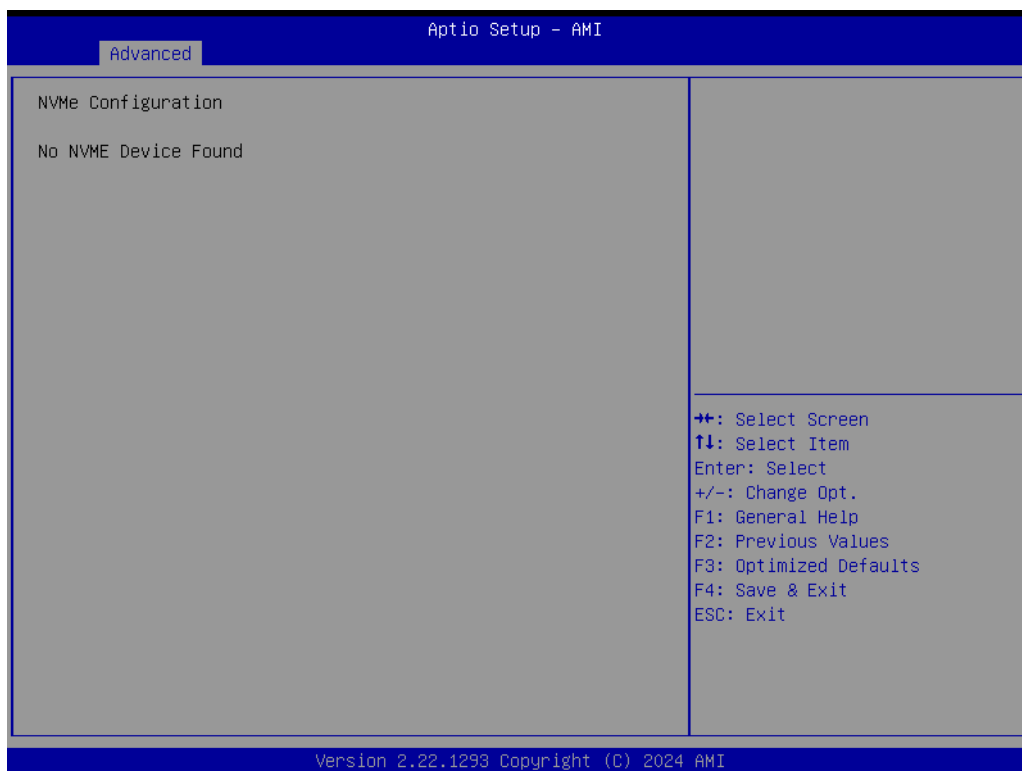
- **XHCI Hand-off**
This is a workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI driver.
- **USB Mass Storage Driver Support**
Enable/Disable USB Mass Storage Driver Support.
- **USB transfer time-out**
Time-out value for control, bulk, and interrupt transfers.
- **Device reset time-out**
USB mass storage device start unit command time-out.
- **Device power-up delay**
Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses the default value: for a Root port it is 100 ms, for a Hub port the delay is taken from the Hub descriptor.

4.1.2.13 Network Stack Configuration



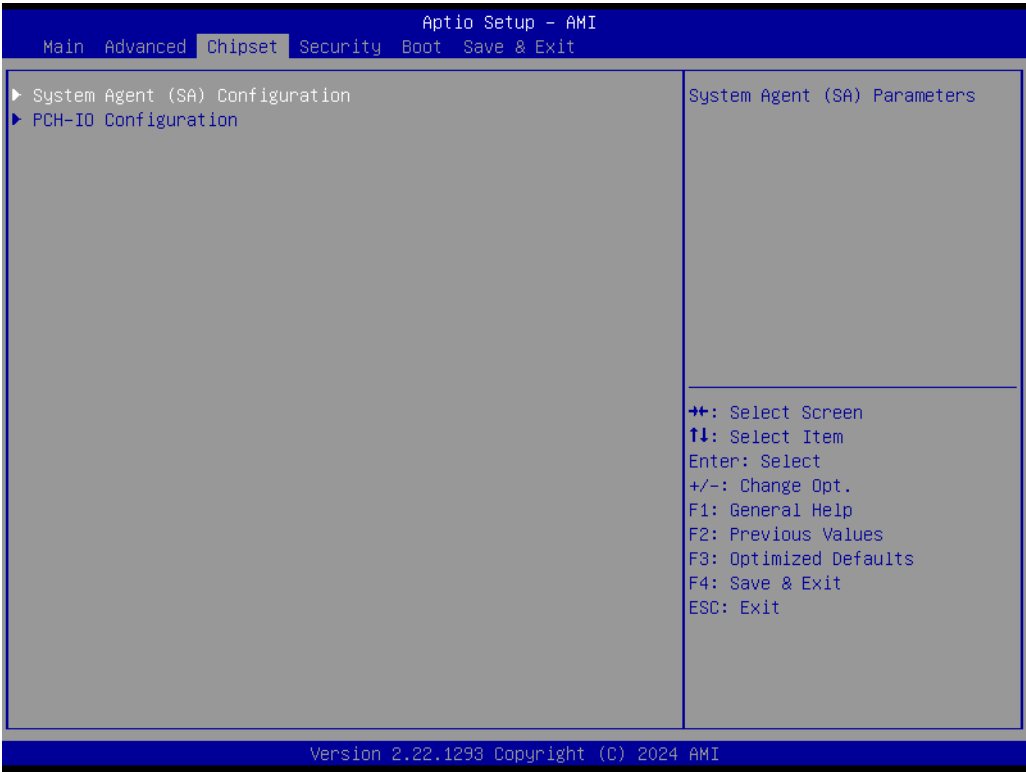
- **Network Stack**
Enable/Disable UEFI Network Stack.

4.1.2.14 NVMe Configuration

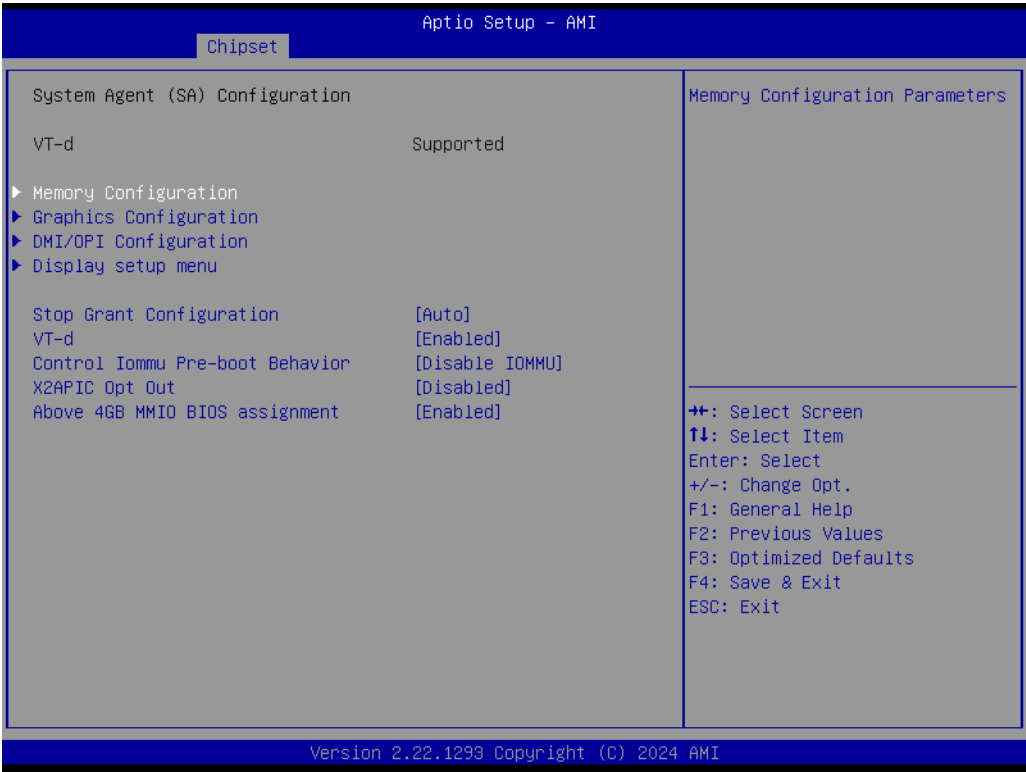


4.1.3 Chipset Configuration

Select the Chipset tab from the MIO-5354 setup screen to enter the Chipset BIOS Setup screen. You can display a Chipset BIOS Setup option by highlighting it using the <Arrow> keys. All Plug and Play BIOS Setup options are described in this section. The Plug and Play BIOS Setup screen is shown below.



4.1.3.1 System Agent (SA) Configuration



- **Memory Configuration**
Memory Configuration Parameters.
- **Graphics Configuration**
Graphics Configuration Parameters.
- **DMI/OPI Configuration**
Control various DMI functions.
- **Display Setup Menu**
Display Configuration settings.
- **Stop Grant Configuration**
Automatic/Manual stop grant configuration.
- **VT-d**
VT-D capability.
- **Control Iommu Pre-Boot Behavior**
Enable IOMMU in the Pre-boot environment.
- **X2APIC Opt Out**
Enable/Disable X2APIC Opt Out Bit.
- **Above 4GB MMIO BIOS assignment**
Enable/Disable above 4GB Memory Mapped IO BIOS assignment.

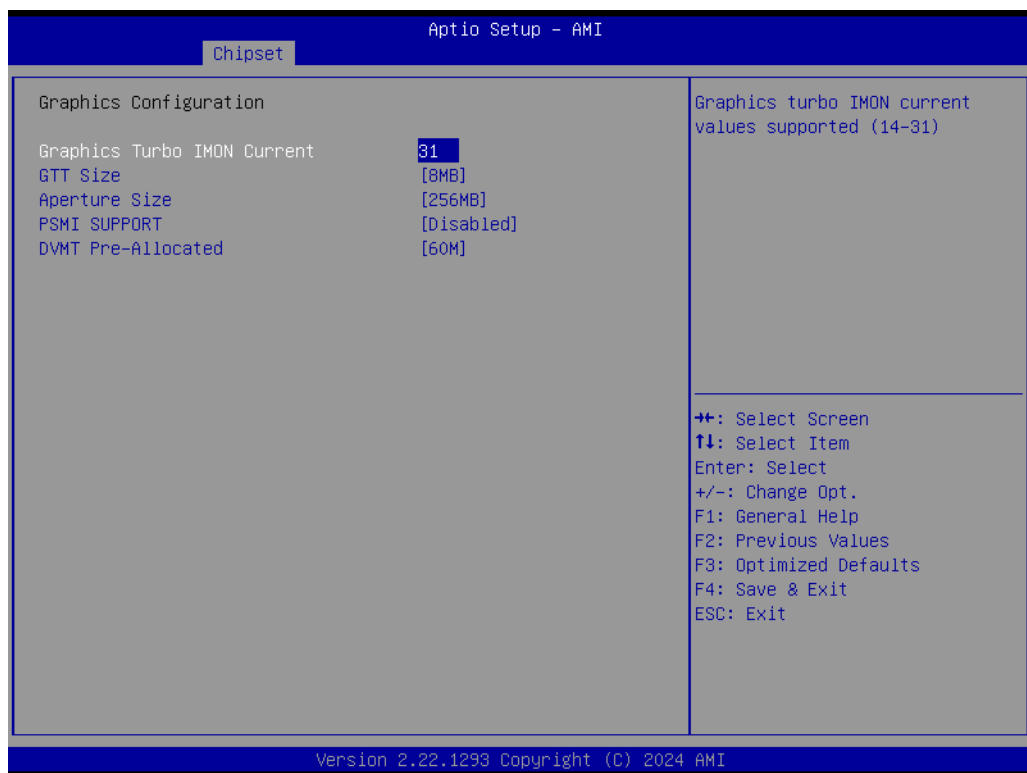
Memory Configuration



- **Memory Test on Warm Boot**
Enable/Disable Base Memory Test Run on Warm Boot.
- **Max TOLUD**
Maximum Value of TOLUD.
- **SA GV**
System Agent Geyserville.

- **Gear Ratio**
Gear ratio when SAGV is disabled.
- **Memory Scrambler**
Enable/Disable Memory Scrambler support.
- **Force ColdReset**
Force ColdReset OR Choose MrcColdBoot mode.
- **In-Band ECC Support**
Enable/Disable In-Band ECC.
- **Memory Remap**
Enable/Disable Memory Remap above 4GB.

Graphics Configuration



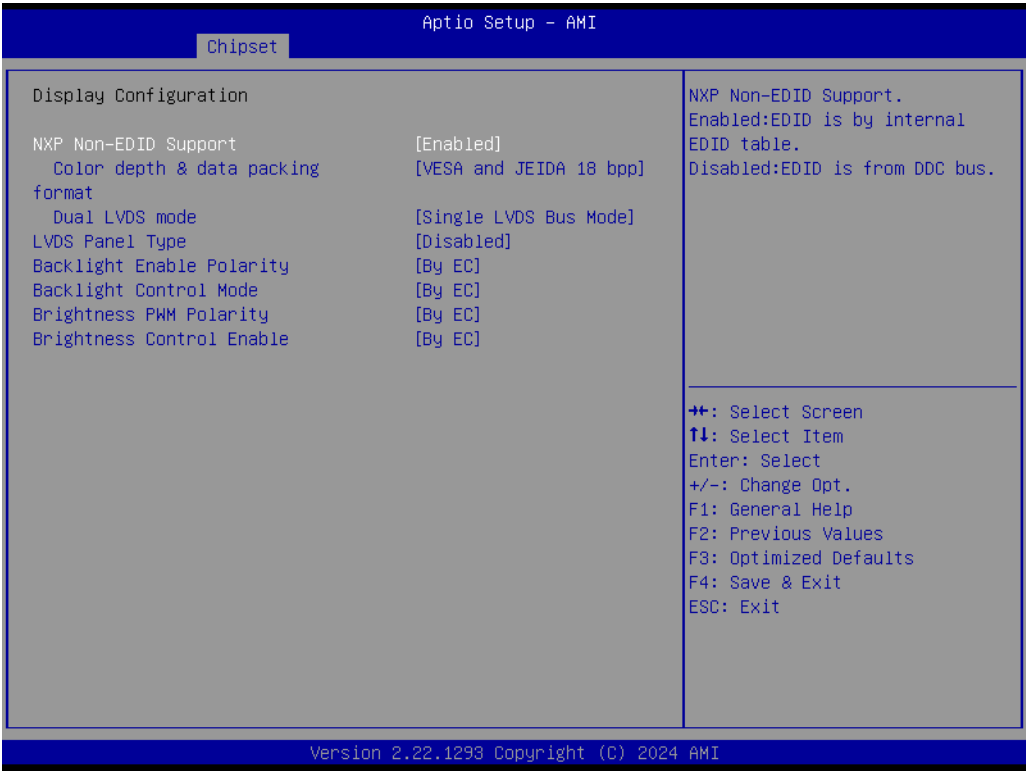
- **Graphics Turbo IMON Current**
Graphics turbo IMON current values supported.
- **GTT Size**
Select the GTT Size.
- **Aperture Size**
Select the Aperture Size.
- **PSMI Support**
Enable/Disable PSMI.
- **DVMT Pre-Allocated**
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.

DMI/OPI Configuration



- **DMI Gen3 ASPM**
DMI Gen3 ASPM Support.
- **DMI ASPM**
DMI ASPM Support.

Display Setup Menu



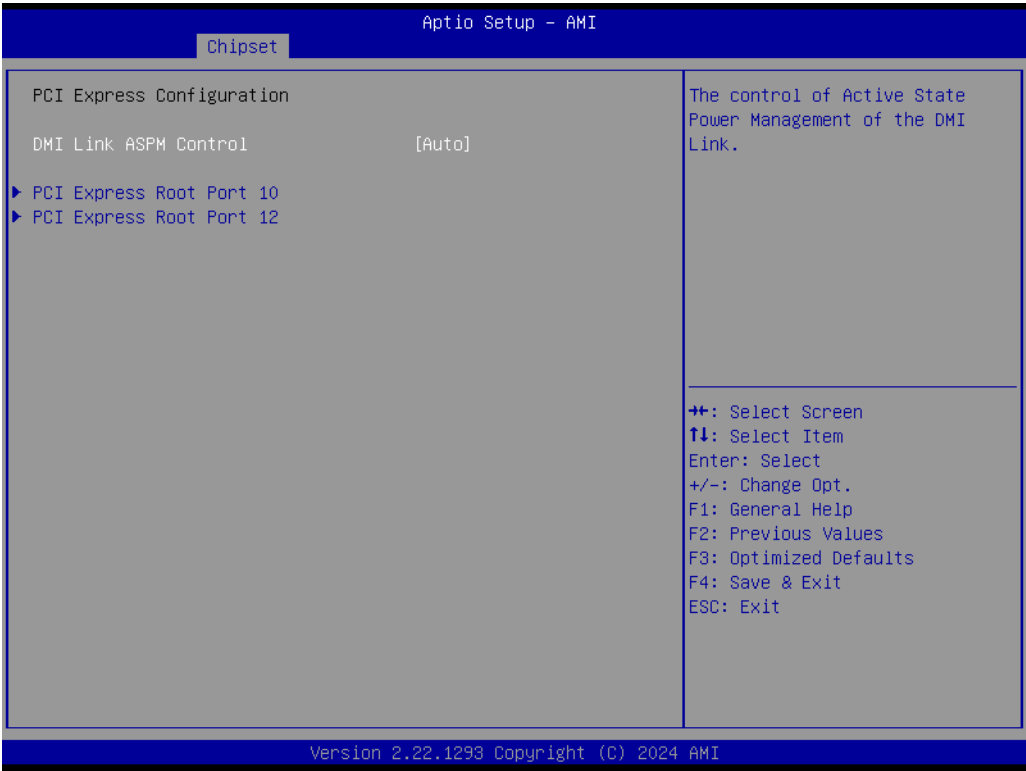
- **NXP Non-EDID Support**
Non-EDID Support.
- **Color Depth & Data Packing**
Color depth and data packing format for Non-EDID Support.
- **Dual LVDS Mode**
Select LVDS bus to Single bus mode or Dual bus mode.
- **LVDS Panel Type**
This item allows the user to select the LVDS panel resolution type.
- **Backlight Enable Polarity**
Switch Backlight Enable Polarity for Native or Invert.
- **Backlight Control Mode**
Switch Backlight Control Mode to PWM or DC mode.
- **Brightness PWM Polarity**
Backlight Control Brightness PWN Polarity for Native or Invert.
- **Brightness Control Enable**
Choose to control LVDS brightness value by EC or user override during POST stage.

4.1.3.2 PCH-IO Configuration



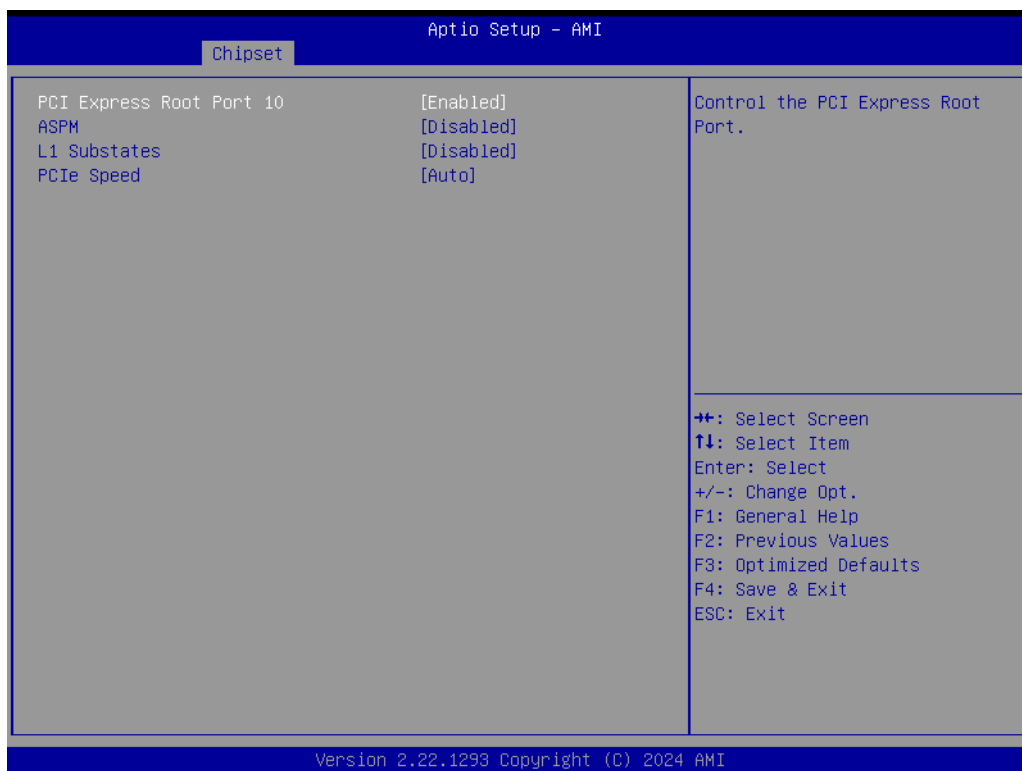
- **PCI Express Configuration**
PCI Express Configuration Settings.
- **SATA Configuration**
SATA Device Options Settings.
- **USB Configuration**
USB Configuration Settings.
- **Security Configuration**
Security Configuration Settings.
- **HD Audio Configuration**
HD Audio Subsystem Configuration Settings.
- **Onboard LAN1 Controller**
Select to Enable or Disable onboard LAN1 Controller.
- **LAN1 PXE ROM**
Enable or Disable onboard LAN1's PXE option ROM.
- **Onboard LAN2 Controller**
Select to Enable or Disable onboard LAN2 Controller.
- **LAN2 PXE ROM**
Enable or Disable onboard LAN2's PXE option ROM.
- **SPD Write Disable**
Enable/Disable setting SPD Write Disable.

PCI Express Configuration



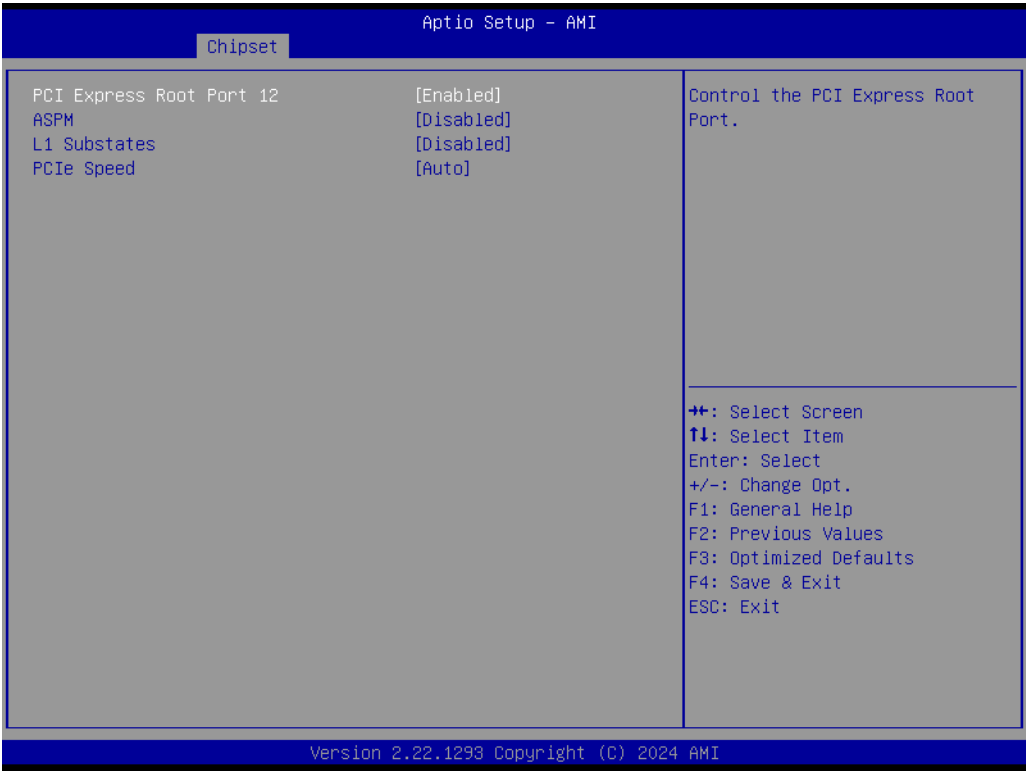
- **DMI Link ASPM Control**
This item controls Active State Power Management of the DMI Link.
- **PCI Express Root Port 10/12**
PCI Express Port 10/12 Settings.

PCI Express Root Port 10



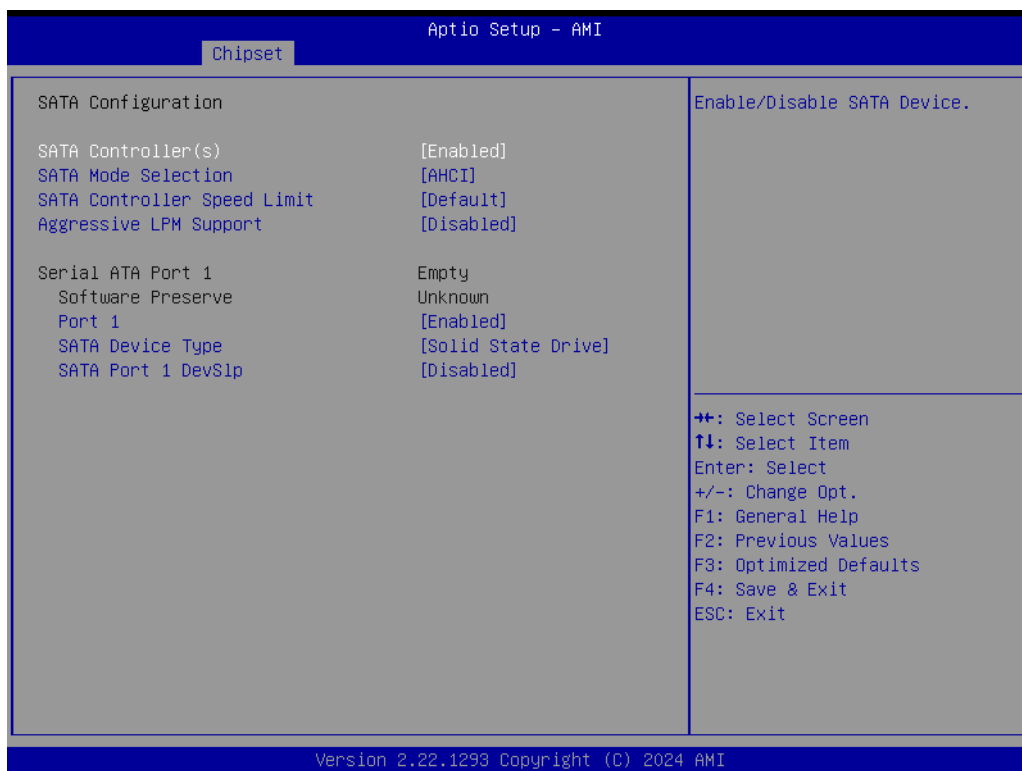
- **PCI Express Root Port 10**
Control the PCI Express Root Port.
- **ASPM**
Set the ASPM Level.
- **L1 Substates**
PCI Express L1 Substates settings.
- **PCIe Speed**
Configure PCIe Speed.

PCI Express Root Port 12



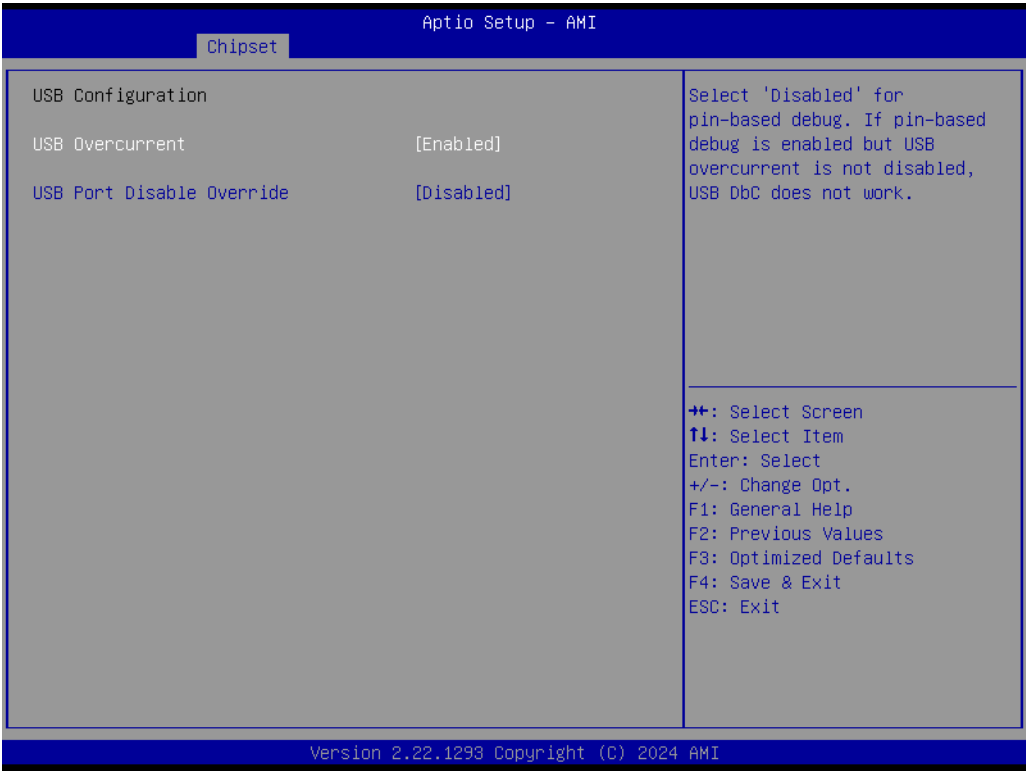
- **PCI Express Root Port 12**
Control the PCI Express Root Port.
- **ASPM**
Set the ASPM Level.
- **L1 Substates**
PCI Express L1 Substates settings.
- **PCIe Speed**
Configure PCIe Speed.

SATA Configuration



- **SATA Controller(s)**
Enable/Disable SATA Device.
- **SATA Mode Selection**
Determine how the SATA controller operates.
- **SATA Controller Speed Limit**
Indicates the maximum speed the SATA controller can support.
- **Aggressive LPM Support**
Enable PCH to aggressively enter link power state.

USB Configuration



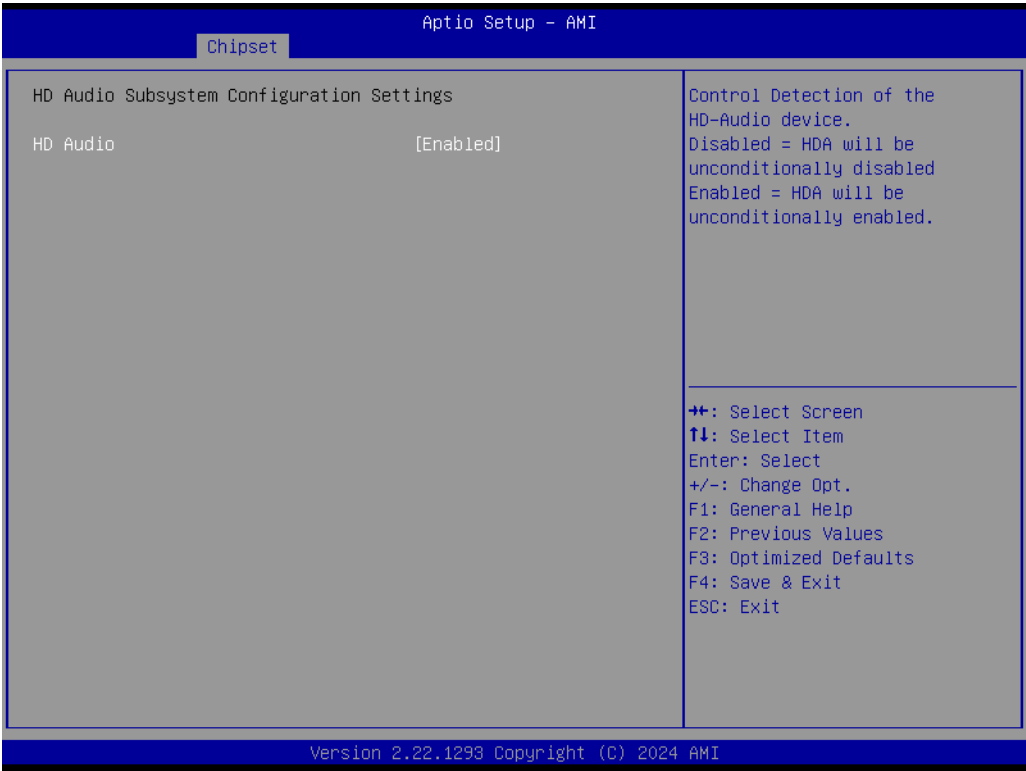
- **USB Overcurrent**
Select "Enabled" if Overcurrent functionality is used.
- **USB Port Disable Override**
Selectively Enable/Disable the corresponding USB Port from reporting a device connection to the controller.

Security Configuration



- **RTC Memory Lock**
Enable will lock bytes 38h-3Fh in the lower/upper 128-byte bank of RTC RAM.
- **BIOS Lock**
Enable or Disable the PCH BIOS Lock Enable feature.
- **Force unlock on all GPIO pads**
If Enabled, BIOS will force all GPIO pads to be in the unlock state.

HD Audio Configuration



- **HD Audio**
Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled. Enabled = HDA will be unconditionally enabled.

4.1.4 Security

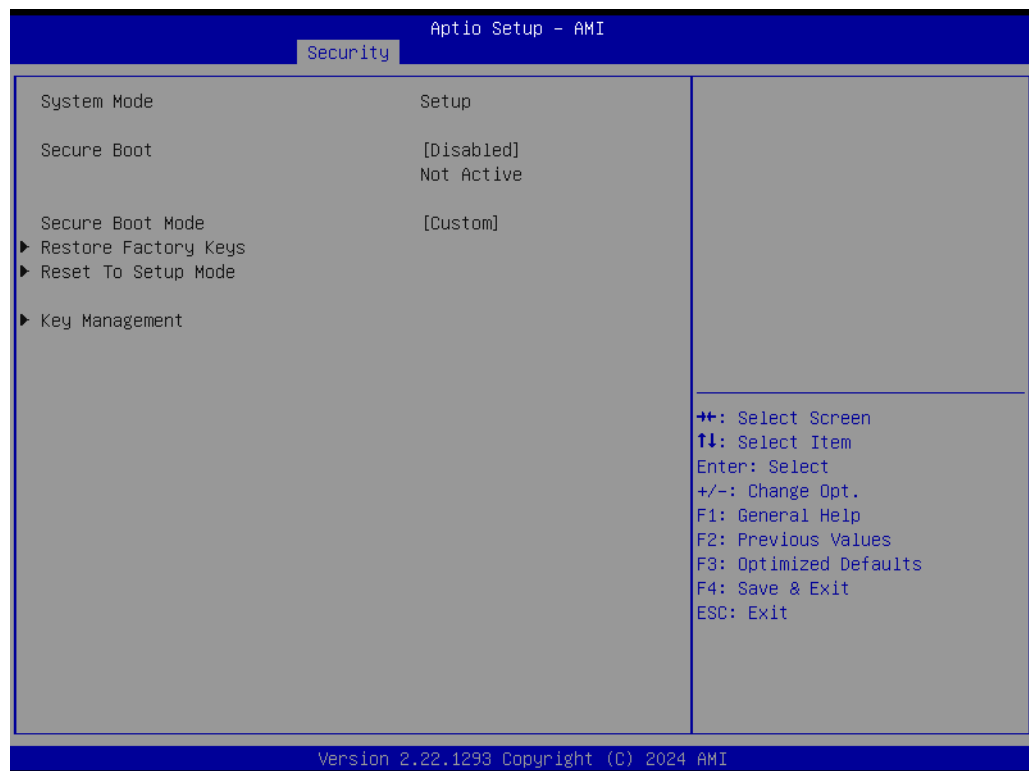
Select Security Setup from the MIO-5354 Setup main BIOS setup menu. All Security Setup options, such as password protection and virus protection are described in this section.



To access the sub-menu for the following items, select the item and press <Enter>:

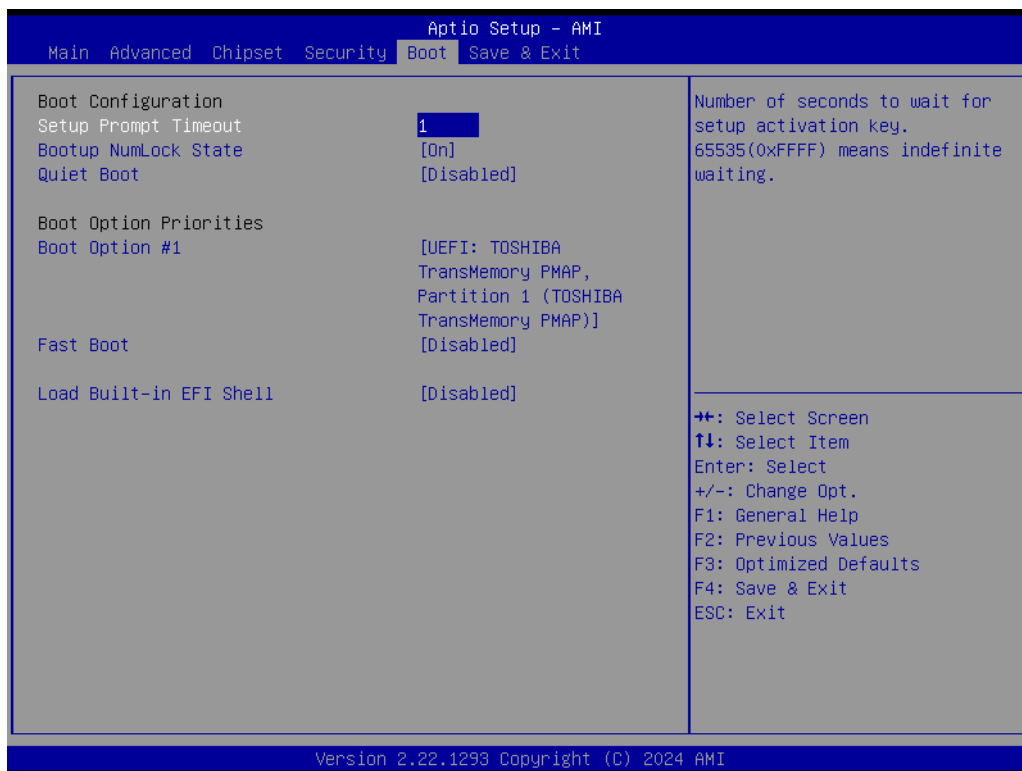
- **Change Administrator / User Password**
Select this option and press <ENTER> to access the sub-menu, and then type in the password.
- **Secure Boot**
Secure Boot Configurations.

4.1.5 Secure Boot



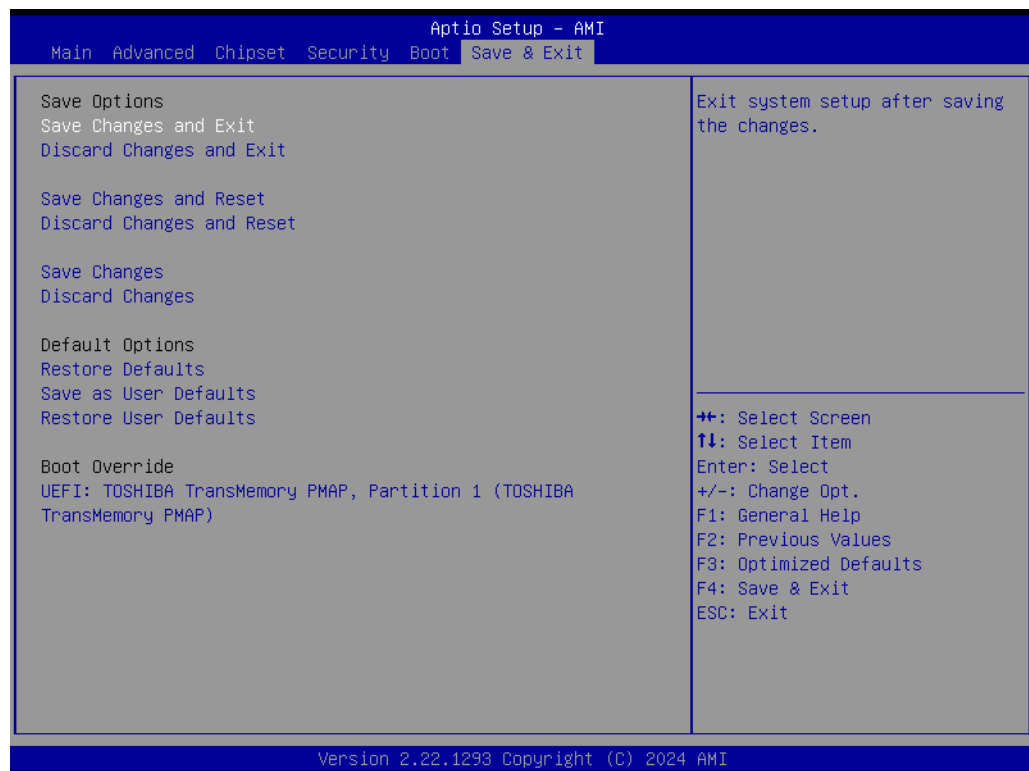
- **Secure Boot**
The Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled, and the System is in User mode. The mode change requires a platform reset.
- **Secure Boot Mode**
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.
- **Restore Factory Keys**
Force System to User Mode. Install factory default Secure Boot Key databases.
- **Key Management**
Enables expert users to modify Secure Boot Policy variables without variable authentication.

4.1.6 Boot



- **Setup Prompt Timeout**
This is the number of seconds that the firmware will wait before initiating the original default boot selection. A value of 0 indicates that the default boot selection is to be initiated immediately on boot. A value of 65535(0xFFFF) indicates that firmware will wait for user input before booting. This means the default boot selection is not automatically started by the firmware.
- **Bootup NumLock State**
Select the keyboard NumLock state.
- **Quiet Boot**
Enables or disables the Quiet Boot option.
- **Boot Option #1**
Sets the system boot order.
- **Fast Boot**
Enable/Disables boot with initialization of a minimal set of devices required to launch the active boot option. It has no effect on BBS boot options.
- **Load Built-in EFI Shell**
Load/Unload Internal Built-in EFI Shell image inside the BIOS. (Built-in EFI Shell will still be loaded if no bootable device is found).

4.1.7 Save & Exit



- **Save Changes and Exit**
This item allows you to exit system setup after saving the changes.
- **Discard Changes and Exit**
This item allows you to exit system setup without saving any changes.
- **Save Changes and Reset**
This item allows you to reset the system after saving the changes.
- **Discard Changes and Reset**
This item allows you to reset system setup without saving any changes.
- **Save Changes**
This item allows you to save changes done so far to any of the options.
- **Discard Changes**
This item allows you to discard changes done so far to any of the options.
- **Restore Defaults**
This item allows you to restore/load default values for all the options.
- **Save as User Defaults**
This item allows you to save the changes done so far as user defaults.
- **Restore User Defaults**
This item allows you to restore the user defaults to all the options.
- **Boot Override**
Boot device select can override your boot priority.

Appendix **A**

System Assignments

This appendix contains information of a detailed nature.

Sections include:

- System I/O Ports
- 1st MB Memory Map
- Interrupt Assignments

A.1 System I/O Ports

Table A.1: System I/O Ports

Address Range (Hex)	Device
20h-2Dh	Programmable Interrupt Controller
2Eh-2Fh	Motherboard resources
30h-3Dh	Programmable Interrupt Controller
40h-43h	System Timer/Counter
4Eh-4Fh	Motherboard resources
50h-53h	System Timer/Counter
60h-6Fh	8042 (keyboard controller) / NMI Controller / Microcontroller
70h-7Fh	Real-time Controller
80h-8Fh	Debug Port / Reserved
90h-9Fh	Debug Port / Reset Generator
A0h-ADh	Programmable Interrupt Controller
B0h-B1h	Programmable Interrupt Controller
B2h-B2h	Motherboard resources
B4h-BDh	Programmable Interrupt Controller
290h-29Fh	Motherboard resources.
2E8h-2EFh	Communications Port (COM4)
2F8h-2FFh	Communications Port (COM2)
3E8h-3EFh	Communications Port (COM3)
3F8h-3FFh	Communications Port (COM1)
4D0h-4D1h	Programmable Interrupt Controller
680h-69Fh	Motherboard resources
A00h-AFFh	Motherboard resources
164Eh-164Fh	Motherboard resources
1854h-1857h	Motherboard resources
2000h-20FEh	Motherboard resources
CF9h-CF9h	Reset Generator

A.2 1st MB Memory Map

Table A.2: 1st MB Memory Map

Addr. Range (Hex)	Device
E0000h - FFFFFh	System board
D0000h - DFFFFh	PCI Bus
C0000h - CFFFFh	System board
A0000h - BFFFFh	PCI Bus
A0000h - BFFFFh	Intel® HD Graphics
00000h - 9FFFFh	System board

A.3 Interrupt Assignments

Table A.3: Interrupt Assignments	
Interrupt#	Interrupt source
NMI	Parity error detected
IRQ0	System Timer
IRQ1	Using SERIRQ, Keyboard Emulation
IRQ2	Interrupt from Controller 2 (cascade)
IRQ3	Communications Port (COM2)
IRQ4	Communications Port (COM1)
IRQ5	Communications Port (COM3)
IRQ6	Reserved
IRQ7	CANBUS
IRQ8	System CMOS / Real Time Clock
IRQ9	Microsoft ACPI-Compliant System
IRQ10	Reserved
IRQ11	Reserved
IRQ12	Available
IRQ13	Numeric Data Processor
IRQ14	GPIO Controller
IRQ15	Communications Port (COM4)



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