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ICF 4000

Customer:	
Customer	
Part	
Number:	
Innodisk	
Part	
Number:	
Innodisk	
Model Name:	
Date:	

Innodisk	Customer				
Approver	Approver				

Total Solution For Industrial Flash Storage

Table of contents

1.	INTRODUCTION	
2.	FEATURES	9
3.	PIN ASSIGNMENT	10
4	PIN DESCRIPTION	12
 E		
э.	SPECIFICATIONS	
5	CE AND FCC COMPATIBILITY	20
5	0.2 ROHS COMPLIANCE	
5	5.3 ENVIRONMENTAL SPECIFICATIONS	20
	5.3.1 Temperature Ranges	
	5.3.2 Humidity	
	5.3.3 Insertion	
	5.3.4 Shock and Vibration	
	5.3.5 Mean Time between Failures (MTBF)	
5	ERROR DETECTION AND CORRECTION	21
5	5.5 WRITE PROTECT FUNCTION SUPPORT(OPTIONAL)	21
5	6.6 WEAR-LEVELING	21
5	5.7 NAND FLASH MEMORY AND ENDURANCE	21
5	5.8 Reliability	22
5	9.9 MECHANICAL IMENSIONS	22
5	5.10 ELECTRICAL SPECIFICATIONS	23
	5.10.1 DC Characteristic	23
	5.10.2 Timing Specifications	23
5	.11 TRANSFER FUNCTION	39
	5.11.1 I/O Transfer function	39
	5.11.2 Common Memory Transfer Function	40
	5.11.3 True IDE Mode I/O Transfer Function	41
5	5.12 CONFIGURATION REGISTER	42
	5.12.1 Configuration Option Register (200h in Attribute Memory)	42
	5.12.2 Card Configuration and Status Register (202h in Attribute Memory)	43
	5.12.3 Pin Replacement register (204h in Attribute Memory)	44
	5.12.4 Socket and Copy Register (206h in Attribute Memory)	44
5	5.13 SOFTWARE INTERFACE	45
	5.13.1 CF-ATA Drive Register Set Definition and Protocol	45
	5.13.2 I/O Primary and Secondary Address Configurations	46
	5.13.3 Contiguous I/O Mapped Addressing	46
	5.13.4 Memory Mapped Addressing	47
	5.13.5 True IDE Mode Addressing	49

5.13.6 CF-ATA Register	
5.14 HARDWARE RESET(ONLY FOR MEMORY CARD MODE AND I/O CARD MODE)	53
5.15 Power On Reset	54
5.16 SUPPORTED IDE COMMANDS	55
5.16.1 Check power mode – 98H or E5H	
5.16.2 Execute Device Diagnostic – 90H	
5.16.3 Erase Sector(s) – C0H	
5.16.4 Format Track – 50H	
5.16.5 Identify Device – ECH	
5.16.6 Idle -97H or E3H	66
5.16.7 Idle immediate - 95H or E1H	
5.16.8 Initialize Device Parameters - 91H	
5.16.9 Read Buffer - E4H	
5.16.10Read DMA - C8H	
5.16.11Read Long Sector - 22H or 23H	
5.16.12Read Sector(s) - 20H or 21H	69
5.16.13Read Verify Sector(s) - 40H or 41H	
5.16.14Recalibrate - 1XH	
5.16.15Request Sense - 03H	
5.16.16Seek - 7XH	
5.16.17Set Features – EFH	
5.16.18Set Sleep Mode - 99H or E6H	
5.16.19Standby - 96H or E2H	
5.16.20Standby Immediate - 94H or E0H	
5.16.21 Write Buffer - E8H	
5.16.22 Write DMA – CAH	
5.16.23Write Sector(s) - 30H or 31H	
5.17 Device Parameters	76
6. INNODISK PART NUMBER RULE	

REVISION HISTORY

Revision	Description Date						
1.0	Release First Version	Jan. 2011					
1.1	Modify the capacity	Feb. 2011					
1.2	Add power on reset timing for each mode	Feb. 2011					
2.0	1. Add the capacity of 16GB and 32GB	Mar. 2011					
	2. updated CHS table with LBA information						
2.1	Add part number rule	Mar. 2011					
2.2	Modify the part number rule	Mar. 2011					
2.3	Updated CHS table with LBA information	April. 2011					
2.4	Add note about hardware reset timing	May. 2012					
2.5	Add insertion specification	Sep. 2012					
2.6	Modify transfer mode	Dec. 2012					
2.7	Add Toshiba flash	May. 2013					
2.8	Add TBW	July. 2013					
2.9	Modify Device parameters	Oct. 2013					
3.0	Modify power consumption	Feb. 2014					
3.1	Modify the TBW	Aug. 2015					
	Rearranging format						
3.2	Add Write Protect feature	Oct. 2015					
	Add 8GB capacity						
3.3	Updated CE/FCC certification (EN 55032)	Apr. 2017					
3.4	Revise transfer mode.	Aug. 2019					
3.5	Revise True IDE Mode I/O Decoding info.	Oct. 2021					
	Remove Appendix						
3.6	Update Mechanical Dimensions	Nov., 2024					

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List of Tables	
TABLE 1: ICF4000 PIN ASSIGNMENTS	10
TABLE 2: ICF4000 PIN DESCRIPTION	
TABLE 3: SHOCK/VIBRATION TEST FOR ICF4000	
TABLE 4: ICF 4000 MTBF	
TABLE 5: RELIABILITY	
TABLE 6: ATTRIBUTE MEMORY READ TIMING	
TABLE 7: CONFIGURATION REGISTER (ATTRIBUTE MEMORY) WRITE TIMING	
TABLE 8: COMMON MEMORY READ TIMING	
TABLE 9: COMMON MEMORY WRITE TIMING	
TABLE 10: I/O READ TIMING	
TABLE 11: I/O WRITE TIMING	
TABLE 12: READ/WRITE TIMING SPECIFICATIONS, PIO MODE 0-6	
TABLE 13: READ/WRITE TIMING SPECIFICATIONS, MULTIWORD DMA MODE 0-4	
TABLE 14: TIMING DIAGRAM, ULTRA DMA MODE 0-4	
TABLE 15: PCMCIA MODE I/O FUNCTION	
TABLE 16: COMMON MEMORY FUNCTION	40
TABLE 17: TRUE IDE MODE I/O FUNCTION	41
TABLE 18: CONFIGURATION OPTION REGISTER	
TABLE 19: INFORMATION FOR CONFIGURATION OPTION REGISTER	
TABLE 20:ICF4000 CONFIGURATION	
TABLE 21: CARD CONFIGURATION AND STATUS REGISTER	
TABLE 22: INFORMATION FOR CARD CONFIGURATION AND STATUS REGISTER	
TABLE 23: PIN REPLACEMENT REGISTER	44
TABLE 24: INFORMATION FOR PIN REPLACEMENT REGISTER	44
TABLE 25: SOCKET AND COPY REGISTER	45
TABLE 26: INFORMATION FOR SOCKET AND COPY REGISTER	
TABLE 27: I/O CONFIGURATION	
TABLE 28: PRIMARY AND SECONDARY I/O DECODING	
TABLE 29: CONTIGUOUS I/O DECODING	
TABLE 30: MEMORY MAPPED DECODING	47
TABLE 31: TRUE IDE MODE I/O DECODING	49
TABLE 32: DATA REGISTER	50
TABLE 33: ERROR REGISTER	50
TABLE 34: FEATURE REGISTER	50
TABLE 35: SECTOR COUNT REGISTER	50
TABLE 36: SECTOR NUMBER REGISTER	50
TABLE 37: Cylinder Low Register	51
TABLE 38: CYLINDER HIGH REGISTER	51
TABLE 39: DEVICE/HEAD REGISTER	51

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TABLE 40: STATUS REGISTER	52
TABLE 41: DEVICE CONTROL REGISTER	52
TABLE 42: DRIVE ADDRESS REGISTER	53
TABLE 43: TIMING DIAGRAM, HARDWARE RESET	53
TABLE 44: TIMING DIAGRAM, POWER ON RESET	54
TABLE 45: TIMING SPECIFICATION FOR EACH MODE	55
TABLE 46: IDE COMMANDS	55
TABLE 47: DIAGNOSTIC	57
TABLE 48: IDENTIFY DEVICE INFORMATION	59
TABLE 49: EXTENDED ERROR CODES	71
TABLE 50: FEATURE SUPPORTED	72
TABLE 51: DEVICE PARAMETERS	76

List of Figures

FIGURE 1 MECHANICAL DIMENSION OF ICF4000	22
FIGURE 2: ATTRIBUTE MEMORY READ TIMING DIAGRAM	24
FIGURE 3 CONFIGURATION REGISTER (ATTRIBUTE MEMORY) WRITE TIMING DIAGRAM	25
FIGURE 4 COMMON MEMORY READ TIMING DIAGRAM	27
FIGURE 5 COMMON MEMORY WRITE TIMING DIAGRAM	29
FIGURE 6 I/O READ TIMING DIAGRAM	30
FIGURE 7 I/O WRITE TIMING DIAGRAM	32
FIGURE 8 READ/WRITE TIMING DIAGRAM, PIO MODE	33
FIGURE 9 READ/WRITE TIMING DIAGRAM, MULTIWORD DMA MODE	34
FIGURE 10 ULTRA DMA MODE DATA-IN BURST INITIATION TIMING DIAGRAM	36
FIGURE 11 ULTRA DMA MODE DATA-OUT BURST INITIATION TIMING DIAGRAM	36
FIGURE 12 SUSTAINED ULTRA DMA MODE DATA-IN BURST TIMING DIAGRAM	37
FIGURE 13 SUSTAINED ULTRA DMA MODE DATA-OUT BURST TIMING DIAGRAM	37
FIGURE 14 TIMING DIAGRAM, HARDWARE RESET	54
FIGURE 15 TIMING DIAGRAM, POWER ON RESET	54



1. Introduction

The Innodisk Industrial CompactFlash[®] 4000 Memory Card (iCF4000) products provide high capacity solid-state flash memory that electrically complies with the Personal Computer Memory Card International Association (PCMCIA) ATA (PC Card ATA) standard. (In Japan, the applicable standards group is JEIDA.) The CompactFlash[®] and PCMCIA cards support True IDE Mode that is electrically compatible with an IDE disk drive. The original CF form factor card can be used in any system that has a CF slot. Designed to replace traditional rotating disk drives, Innodisk Industrial CompactFlash[®] 4000 Memory Cards are embedded solid-state data storage systems for mobile computing and the industrial work place. The Industrial CompactFlash[®] features an extremely lightweight, reliable, low-profile form factor.

Industrial CompactFlash[®] 4000 (iCF4000) supports advanced PIO (0-6), Multiword DMA (0-4), Ultra DMA (0-4) transfer modes, multi-sector transfers, and LBA addressing.



2. Features

The Industrial ATA products provide the following system features:

- Capacities: 128MB~8GB
- Fully compatible with CompactFlash® specification version 3.0
- Fully compatible with PC Card Standard.
- Fully compatible with the IDE standard interface, ATA Standard
- Three access modes
 - PC Card Memory Mode
 - PC Card I/O Mode
 - True IDE Mode
- ECC (Error Correction Code) function: 4 bits/ per 512 byte
- +3.3V/+5V single power supply operation
- Support Auto Stand-by and Sleep Mode.
- Power Consumption

Voltage	5V	3.3V
Read	143mA (Max.)	125mA (Max.)
Write	129mA (Max.)	120mA (Max.)
Idle	1.5mA (Typ./max.)	0.7mA (Typ./max.)

- Support transfer modes: PIO(0-6), Multiword DMA(0-4) and Ultra DMA(0-4)
- MTBF 3,000,000 hours
- Data retention: 10 years
- R/W performance:
 - Single: 128MB~2GB
 - Read: 20Mbytes/s. (MAX)
 - Write: 10Mbytes/s (MAX)
 - Dual: 1GB~8GB
 - Read: 40Mbytes/s. (MAX)
 - Write: 20Mbytes/s (MAX)
- Operating temperature range:
 - Standard Grade: 0°C ~ +70°C
 - Industrial Grade: -40°C ~ +85°C
- Storage temperature range: -55°C ~ +95°C



3. Pin Assignment

See Table 1 for iCF4000 pin assignments.

PC Card Memory Mode			PC C	ard I/O M	1ode	True IDE Mode		
Pin No.	Name	1/0	Pin No.	Name	I/0	Pin No.	Name	I/O
1	GND		1	GND		1	GND	
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	-CE1	I	7	-CE1	Ι	7	-CS0	Ι
8	A10	I	8	A10	Ι	8	A10 ²	I
9	-OE	I	9	-OE	Ι	9	-ATA SEL	I
10	A09	I	10	A09	Ι	10	A09 ²	I
11	A08	I	11	A08	Ι	11	A08 ²	I
12	A07	I	12	A07	Ι	12	A07 ²	I
13	VCC		13	VCC		13	VCC	
14	A06	I	14	A06	Ι	14	A06 ²	I
15	A05	I	15	A05	Ι	15	A05 ²	Ι
16	A04	I	16	A04	Ι	16	A04 ²	Ι
17	A03	I	17	A03	Ι	17	A03 ²	I
18	A02	I	18	A02	Ι	18	A02	Ι
19	A01	I	19	A01	Ι	19	A01	Ι
20	A00	Ι	20	A00	Ι	20	A00	Ι
21	D00	I/O	21	D00	I/O	21	D00	I/O
22	D01	I/O	22	D01	I/O	22	D01	I/O
23	D02	I/O	23	D02	I/O	23	D02	I/O
24	WP	0	24	-IOIS16	0	24	-IOCS16	0
25	-CD2	0	25	-CD2	0	25	-CD2	0
26	-CD1	0	26	-CD1	0	26	-CD1	0
27	D11 ¹	I/O	27	D11 ¹	I/O	27	D11 ¹	I/O
28	D12 ¹	I/O	28	D12 ¹	I/O	28	D12 ¹	I/O
29	D13 ¹	I/O	29	D13 ¹	I/O	29	D13 ¹	I/O
30	D14 ¹	I/O	30	D14 ¹	I/O	30	D14 ¹	I/O
31	D15 ¹	I/O	31	D15 ¹	I/O	31	D15 ¹	I/O
32	-CE21	I	32	-CE21	I	32	-CS1 ¹	Ι

Table 1: iCF4000 Pin Assignments

33	-VS1	0	33	-VS1	0	33	-VS1	0
							-IORD ⁷	
34	-IORD	Ι	34	-IORD	Ι	34	HSTROBE ⁸	Ι
							-HDMARDY ⁹	
25		т	25		т	25	-IOWR ⁷	т
22	-1000	L	22	-1000	L	55	STOP ^{8, 9}	T
36	-WE	Ι	36	-WE	Ι	36	-WE ³	Ι
37	READY	0	37	-IREQ	0	37	INTRQ	0
38	VCC		38	VCC		38	VCC	
39	-CSEL ⁵	Ι	39	-CSEL ⁵	Ι	39	-CSEL	Ι
40	-VS2	0	40	-VS2	0	40	-VS2	0
41	RESET	Ι	41	RESET	Ι	41	-RESET	Ι
							IORDY ¹	
42	-WAIT	0	42	-WAIT	0	42	-DDMARDY ⁸	0
							DSTROBE ⁹	
43	-INPACK	0	43	-INPACK	0	43	DMARQ	0
44	-REG	I	44	-REG	Ι	44	-DMACK ⁶	Ι
45	BVD2	0	45	-SPKR	0	45	-DASP	I/O
46	BVD1	0	46	-STSCHG	0	46	-PDIAG	I/O
47	D081	I/O	47	D081	I/O	47	D08 ¹	I/O
48	D091	I/O	48	D091	I/O	48	D091	I/O
49	D101	I/O	49	D101	I/O	49	D101	I/O
50	GND		50	GND		50	GND	

Note:

1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.

- 2) The signal should be grounded by the host.
- 3) The signal should be tied to VCC by the host.
- 4) The mode is optional for CF+ Cards, but required for CompactFlash[®] Storage Cards.
- 5) The –CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.
- 6) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition
- 7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.
- 8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.
- 9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.



4. Pin Description

Table 2 describes the pin descriptions for iCF4000

Pin No.	Pin Name	I/ 0	Mode	Description	
8,10,11 , 12,14,1 516,17, 18 19, 20	A10 - A0		PC Card Memory Mode	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash [®] Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash [®] Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers.	
8,10,11 , 12,14,1 516,17, 1819, 20	A10 - A0	I	PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.	
18,19,2 0	A2 - A0		True IDE Mode	In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.	
BVD1 I	PC Card Memory Mode	This signal is asserted high, as BVD1 is not supported.			
46	-STSCHG O Mode	PC Card I/O Mode	This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card configuration and Status Register.		
	-PDIAG		True IDE Mode	In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.	
	45 BVD2 PC Card BVD2 Mode I/ PC Card Memory Mode I/O I/O Mode		PC Card Memory Mode	This signal is asserted high, as BVD2 is not supported.	
45			PC Card I/O Mode	This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.	
	-DASP		True IDE	In the True IDE Mode, this input/output is the Disk	

Table 2: iCF4000 Pin Description



			Mode	Active/Slave Present signal in the Master/Slave
		──	<u> </u>	handshake protocol.
26.25	-CD1,		PC Card Memory Mode	These Card Detect pins are connected to ground on the CompactFlash [®] Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash [®] Storage Card or CF+ Card is fully inserted into its socket.
26, 25	-CD2	U	PC Card I/O Mode	This signal is the same for all modes.
			True IDE Mode	This signal is the same for all modes.
	-CE1, -CE2		PC Card Memory Mode	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7.
7, 32	-CE1, -CE2	I	PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
	-CS0, -CS1		True IDE Mode	In the True IDE Mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While -DMACK is asserted, -CS0 and -CS1 shall be held negated and the width of the transfers shall be 16 bits.
		Ι	PC Card Memory Mode	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
39	-CSEL		PC Card I/O Mode	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
			True IDE Mode	This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.

2,3,4,5, 631,30,	D15 - D00	I/ O	PC Card Memory Mode	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
2928,2 7,4948, 47,232			PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
2,21			True IDE Mode	In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
			PC Card Memory Mode	Ground.
1, 50	GND	-	PC Card I/O Mode	This signal is the same for all modes.
			True IDE Mode	This signal is the same for all modes.
	-INPACK		PC Card Memory Mode	This signal is not used in this mode.
		PC Card I/O Mode	The Input Acknowledge signal is asserted by the CompactFlash [®] Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash [®] Storage Card or CF+ Card and the CPU.	
43	DMARQ	0	True IDE Mode	This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by –IORD and –IOWR. This signal is used in a handshake manner with –DMACK, i.e., the device shall wait until the host asserts –DMACK before negating DMARQ, and reasserting DMARQ if there is more data to transfer. DMARQ shall not be driven when the device is not selected. While a DMA



				operation is in progress, -CS0 and -CS1 shall be held
				negated and the width of the transfers shall be 16
				bits. If there is no hardware support for DMA mode in
				the host, this output signal is not used and should not
				be connected at the host. In this case, the BIOS must
				report that DMA mode is not supported by the host
				so that device drivers will not attempt DMA mode. A
				host that does not support DMA mode and
				implements both PCMCIA and True-IDE modes of
				operation need not alter the PCMCIA mode
				connections while in True-IDE mode as long as this
				does not prevent proper operation in any mode.
			PC Card	
			Memory	This signal is not used in this mode.
			Mode	
	-IORD		DC Cand	This is an I/O Read strobe generated by the host.
		-	PC Card I/O Mode	This signal gates I/O data onto the bus from the
				CompactFlash [®] Storage Card or CF+ Card when the
				card is configured to use the I/O interface.
	-IORD			In True IDE Mode, while Ultra DMA mode is not
				active, this signal has the same function as in PC
				Card I/O Mode.
34		Ι		In True IDE Mode when Ultra DMA mode DMA Read is
-н		ARDY		active, this signal is asserted by the host to indicate
	-HDMARDY			that the host is read to receive Ultra DMA data-in
			True IDE	bursts. The host may negate –HDMARDY to pause an
			Mode	Ultra DMA transfer.
				In True IDE Mode when Ultra DMA mode DMA Write
				is active, this signal is the data out strobe generated
	HCTDORE			by the host. Both the rising and falling edge of
	HSTRODE			HSTROBE cause data to be latched by the device.
				The host may stop generating HSTROBE edges to
				pause an Ultra DMA data-out burst.
			PC Card	
	-IOWR		Memory	This signal is not used in this mode.
			Mode	
35		Ι	PC Card I/O Mode	The I/O Write strobe pulse is used to clock I/O data
	-IOWR			on the Card Data bus into the CompactFlash $^{ m extsf{ iny R}}$
				Storage Card or CF+ Card controller registers when
				the CompactFlash [®] Storage Card or CF+ Card is



-IOWR Frue IDE Supported, this signal must be negated beform Mode entering Ultra DMA mode protocol.	the
-IOWR Signal (trailing edge). In True IDE Mode, while Ultra DMA mode protocol not active, this signal has the same function as in 1 Card I/O Mode. When Ultra DMA mode protocol True IDE supported, this signal must be negated before Mode entering Ultra DMA mode protocol.	circ
-IOWR In True IDE Mode, while Ultra DMA mode protocol not active, this signal has the same function as in I Card I/O Mode. When Ultra DMA mode protocol True IDE supported, this signal must be negated beform Mode entering Ultra DMA mode protocol.	
-IOWR -IOWR Card I/O Mode. When Ultra DMA mode protocol True IDE supported, this signal must be negated befor Mode entering Ultra DMA mode protocol.	ol is
-IOWR Card I/O Mode. When Ultra DMA mode protocol True IDE supported, this signal must be negated befor Mode entering Ultra DMA mode protocol.	PC
True IDE supported, this signal must be negated before Mode entering Ultra DMA mode protocol.	l is
Mode entering Ultra DMA mode protocol.	ore
In True IDE Mode, while Ultra DMA mode protocol	ol is
STOP active, the assertion of this signal causes t	the
termination of the Ultra DMA burst.	
PC Card This is an Output Enable strobe generated by t	the
Memory host interface. It is used to read data from t	the
-OE CompactFlash® Storage Card or CF+ Card in Memo	ory
Mode and to read	
9 I the CIS and configuration registers.	
PC Card In PC Card I/O Mode, this signal is used to read t	the
-OE I/O CIS and configuration registers.	
Mode	
-ATA SEL	be
Mode grounded by the host.	
In Memory Mode, this signal is set high when the	the
Compactriasities Storage Card of CF+ Card is ready	
when the card is husy. At newer up and at Reset, t	tow
BEADY signal is hold low (husy) until t	the
CompactElash® Storago Card or CE+ Card b	hac
completed its power up or reset function. No acce	
PC Card of any type should be made to the CompactElact	coo ch®
READY Memory Storage Card or CE+ Card during this time. Not	
Mode Mode	sod
with RESET continuously disconnected or asserted	od
the Reset function of the RESET pin is disable	ed,
Consequently, the continuous assertion of RES	SFT
from the application of power shall not cause t	the
READY signal to remain continuously in the bu	usv
state.	
PC Card I/O Operation – After the CompactFlash [®] Stora	age
	I/O
-IREQ I/O Card or CF+ Card has been configured for I	est.



				This line is strobed low to generate a pulse mode
		_		interrupt or held low for a level mode interrupt.
	INTRQ		True IDE Mode	In True IDE Mode signal is the active high Interrupt Request to the host.
	-REG		PC Card Memory Mode PC Card I/O	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.
		-	Mode	This is a DMA Acknowledge signal that is asserted by
44	-DMACK	Ι	True IDE Mode	the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the –DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
41	RESET	I	PC Card Memory Mode	The CompactFlash [®] Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash [®] Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
	RESET		PC Card I/O	This signal is the same as the PC Card Memory Mode signal.



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			Mode	
	DECET		True IDE	In the True IDE Mode, this input pin is the active low
	-KESEI		Mode	hardware reset from the host.
			PC Card Memory Mode	+5 V, +3.3 V power.
13, 38	VCC	-	PC Card I/O Mode	This signal is the same for all modes.
			True IDE Mode	This signal is the same for all modes.
			PC Card Memory Mode	Voltage Sense Signals. –VS1 is grounded on the Card and sensed by the Host so that the CompactFlash [®] Storage Card or CF+ Card CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.
33, 40	-VS1, -VS2	0	PC Card I/O Mode	This signal is the same for all modes.
			True IDE Mode	This signal is the same for all modes.
	-WAIT		PC Card Memory Mode	The –WAIT signal is driven low by the CompactFlash [®] Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
	-WAIT		PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
42	IORDY	0		In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.
	-DDMARD Y	-	True IDE Mode	In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate –DDMARDY to pause an Ultra DMA transfer.
	DSTROBE			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of



				DSTROBE cause data to be latched by the host. The
				device may stop generating DSTROBE edges to
				pause an Ultra DMA data-out burst.
				This is a signal driven by the host and used for
			PC Card	strobing memory write data to the registers of the
			Memory	CompactFlash [®] Storage Card or CF+ Card when the
			Mode	card is configured in the memory interface mode. It
26		T		is also used for writing the configuration registers.
30	-WE	1	PC Card I/O	In PC Card I/O Mode, this signal is used for writing the configuration registers.
				In True IDE Mode, this input signal is not used and
			Mode	should be connected to VCC by the bost
			Houe	Memory Mode – The CompactElash® Storage Card or
	WP	0	PC Card	CE+ Card does not have a write protect switch. This
			Memory Mode	signal is held low after the completion of the reset
				initialization sequence.
				I/O Operation – When the CompactFlash [®] Storage
				Card or CF+ Card is configured for I/O Operation Pin
24			PC Card	24 is used for the -I/O Selected is 16 Bit Port
	-101516		I/O Mada	(-IOIS16) function. A Low signal indicates that a 16
			Mode	bit or odd byte only operation can be performed at
				the addressed port.
			True IDE Mode	In True IDE Mode this output signal is asserted low
	-IOCS16			when this device is expecting a word data transfer
				cycle.

5. Specifications

5.1 CE and FCC Compatibility

iCF4000 conforms to CE and FCC requirements.

5.2 RoHS Compliance

iCF4000 is fully compliant with RoHS directive.

5.3 Environmental Specifications

5.3.1 Temperature Ranges

Operating Temperature Range:

- Standard Grade: 0°C to +70°C
- Industrial Grade: -40°C to +85°C

Storage Temperature Range: -55°C to +95°C

5.3.2 Humidity

Relative Humidity: 10-95%, non-condensing

5.3.3 Insertion

Compact Flash card 50pins connector : >10,000 times

5.3.4 Shock and Vibration

Table 3: Shock/Vibration Test for iCF4000

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2 KHz, 20 g, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms, 1500 g, 3 axes	IEC 68-2-27

5.3.5 Mean Time between Failures (MTBF)

Table 4 summarizes the MTBF prediction results for various iCF4000 configurations. The analysis was performed using a RAM CommanderTM failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- Mean Time between Failures (MTBF): A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Product	Condition	MTBF (Hours)
iCF4000	Telcordia SR-332 GB, 25°C	3,000,000

5.4 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements a algorithm that can correct 4 bits per 512 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

5.5 Write Protect Function Support(Optional)

Innodisk CF card within the write-protect function could prevent the CF card from modification and deletion. Write-protected data in CF card could only be read, that is, users could not write to it, edit it, append data to it, or delete it.

When users would like to make sure that neither themselves nor others could modify or destroy the file, users could switch on write-protection. Thus Innodisk CF card would process write-protect mechanism and disable flash memory to be written-in any data. Only while the system power-off, users could switch on write-protection. Write-protection could not be switched-on, after OS booting.

5.6 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the **erase cycle limit** or **write endurance limit** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

iCF4000 uses a wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime.

5.7 NAND Flash Memory and Endurance

Innodisk CF4000 uses Single Level Cell (SLC) NAND flash memory, which is non-volatility, high reliability and high speed memory storage.



5.8 Reliability

Ia	Die 5: Reliability
Parameter	Value
Read Cycles	Unlimited Read Cycles
Wear-Leveling Algorithm	Support
Bad Blocks Management	Support
Error Correct Code	Support
TBW(Sequential Write)	
128MB	6.58
256MB	13.18
512MB	26.36
1GB	52.73
2GB	105.46
4GB	210.9
8GB	421.8

-l:-b:l:#

5.9 Mechanical imensions

Mechanical Dimension: 42.80±0.1/36.40±0.15/3.30±0.1mm (W/T/H)



Figure 1 Mechanical Dimension of iCF4000



5.10 Electrical Specifications

5.10.1 DC Characteristic

Item	Symbol	Rating	Uni t
Transitiveltere	N	+5 DC ± 0.5	V
Input voltage	VIN	+3.3 DC ± 0.3	

5.10.2 Timing Specifications

5.10.2.1 Attribute Memory Read Timing Specification

Attribute Memory access time is defined as 300ns. Detailed timing specs are shown in Table 6.

Speed Version			300ns	
Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Read cycle time	tc(R)	tAVAV	300	
Address access time	ta(A)	tAVQV		300
Card enable access time	ta(CE)	tELQV		300
Output enable access time	ta(OE)	tGLQV		150
Output disable time from CE	tdis(CE)	tEHQZ		100
Output disable time from OE	tdis(OE)	tGHQZ		100
Address setup time	tsu(A)	tAVGL	30	
Output enable time from CE	ten(CE)	tELQNZ	5	
Output enable time from OE	ten(OE)	tGLQNZ	5	
Data valid from address change	tv(A)	tAXQX	0	

Table 6: Attribute Memory Read Timing

Note: All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -CE signal or both the -OE signal and the -WE signal shall be de-asserted between consecutive cycle operations.





Figure 2: Attribute Memory Read Timing Diagram

5.10.2.2 Configuration Register (Attribute Memory) Write Timing Specification

The Card Configuration write access time is defined as 250ns. Defined timing specifications are shown in Table 7.

Speed Version			250ns	
Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Write cycle time	tc(W)	tAVAV	250	
Write pulse width	tw(WE)	tWLWH	150	
Address setup time	tsu(A)	tAVWL	30	
Write recovery time	trec(WE)	tWMAX	30	
Data setup time for WE	tsu(D-WEH)	tDVWH	80	
Data hold time	th(D)	tWMDX	30	

Table 7: Configuration Register (Attribute Memory) Write Timing

Note: All times are in nanoseconds. Din signifies data provided by the system to theCompactFlashstoragecardorCF+card.





Figure 3 Configuration Register (Attribute Memory) Write Timing Diagram

5.10.2.3 Common Memory Read Timig Specification

Cycle Ti	me Mode:		250	ns	120	ns	100	ns	80n	s
-		TEEE	Mi	Max	Mi	Мах	Mi	Max	Mi	Ма
Item	Symbol	Symbol	n	ne	n	ns.	n	ns.	n	x
		Symbol	ns.	115.	ns.		ns.		ns.	ns.
Output enable access time	ta(OE)	tGLQV		125		60		50		40
Output disable time from OE	tdis(OE)	tGHQZ		100		60		50		40
Address setup time	tsu(A)	tAVGL	30		15		10		10	
Address hold time	th(A)	tGHAX	20		15		15		10	
CE setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE hold followin g OE	th(CE)	tGHEH	20		15		15		10	
Wait delay falling from OE	tv(WT-O E)	tGLWTV		35		35		35		Na
Data setup for wait release	tv(WT)	tQVWTH		0		0		0		Na
Wait	tw(WT)	tWTLWT		350		350		350		Na

Table 8: Common Memory Read Timing



Industrial CompactFlash Card 4000

width	Н	(300	(300	(300	
time		0 for	0 for	0 for	
		CF+)	CF+)	CF+)	

Note:

1) -WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.



Figure 4 Common Memory Read Timing Diagram

5.10.2.4 Common Memory Write Timing Specification

Cycle Ti	me Mode:		250	ns	120	ns	100	ns	80ns	
		TEEE	Mi	Max	Mi	Max	Mi	Max	Mi	Ма
Item	Symbol	Symbol	n	ns	n	ns.	n	ns.	n	x
		Symbol	ns.	113.	ns.		ns.		ns.	ns.
Data Setup before WE	tsu(D-WE H)	tDVWH	80		50		40		30	
Data Hold followin g WE	th(D)	tWMDX	30		15		10		10	
WE	tw(WE)	tWLWH	15		70		60		55	

Table 9: Common Memory Write Timing



Pulse			0							
Address										
Setup	tsu(A)	tAVWL	30		15		10		10	
Time		-			_		_		_	
CE										
Setup	tsu(CE)	tEI WI	0		0		0		0	
before			U		Ū		Ū		C	
WE										
Write	trac(ME)	+\\/\/\	20		15		15		15	
v Time		LVVMAA	30		13		13		10	
Address										
Hold	th(A)	tGHAX	20		15		15		15	
Time										
CE Hold										
followin	th(CE)	tGHEH	20		15		15		10	
g WE										
Walt										
Falling	tv(WT-WE	+WI WTV		35		35		35		Na
from)			55		55		55		nu -
WE										
WE										
High		+\//ТН\//								
from	tv(WT)	Н	0		0		0		na	
Wait										
Release				250		250		250		
Wait				350		350		350		
Width	tw(WT)	tWTLWT		0		0		0		Na
Time		Н		for		for		for		nu
-				CF+)		CF+)		CF+)		

Notes:

1) -WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is



intentionally less in this specification.





5.10.2.5 I/O Input (Read) Timing Specification

Cycle Time M	lode:		250	ns	120	ns	100) ns	80 ns	
Itom	Symbol	IEEE	Min	Max	Min	Max	Min	Max	Min	Max
Item	Symbol	Symbol	ns.	ns.	ns.	ns.	ns.	ns.	ns.	ns.
Data Delay	td(IORD)	tlGLQV		100		50		50		45
after IORD										
Data Hold	th(IORD)	tIGHQ	0		5		5		5	
following		Х								
IORD										
IORD Width		tlGLIG	165		70		65			
Time	tw(IORD)	Н	105		70		65		55	
Address	tsuA(IOR	tAVIGL	70		25		25		15	
Setup before	D)									
IORD										
Address Hold	thA(IOR	tIGHAX	20		10		10		10	
following	D)									
IORD										
CE Setup	tsuCE(IO	tELIGL	5		5		5		5	
before IORD	RD)									
CE Hold	thCE(IOR	tIGHEH	20		10		10		10	
following	D)									
IORD										
REG Setup	tsuREG	tRGLI	5		5		5		5	
before IORD	(IORD)	GL								

REG Hold following IORD	thREG (IORD)	tighr Gh	0		0		0		0	
INPACK Delay Falling from IORD3	tdfINPAC K (IORD)	tlGLIA L	0	45	0	na1	0	na1	0	na1
INPACK Delay Rising from IORD3	tdrINPAC K (IORD)	tighia H		45		na1		na1		na1
IOIS16 Delay Falling from Address3	tdfIOIS1 6 (ADR)	tAVISL		35		na1		na1		na1
IOIS16 Delay Rising from Address3	tdrIOIS1 6 (ADR)	tAVIS H		35		na1		na1		na1

Notes:

1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this spec.



Figure 6 I/O Read Timing Diagram

5.10.2.6 Timing Specification

Cycle Time Mo	ode:		250	ns	120)ns	100)ns	80ns	
		TEEE	Mi	Max	Mi	Max	Mi	Max	Mi	Ма
Item	Symbol	Symbol	n	ne	n	ns.	n	ns.	n	x
		Symbol	ns.	115.	ns.		ns.		ns.	ns.
Data Setup before IOWR	tsu(IOWR)	tDVIW H	60		20		20		15	
IOWR Width Time	tw(IOWR)	tlWLIW H	16 5		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		25	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		20		10		10	
CE Setup before IOWR	tsuCE(IOW R)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20		20		10		10	
REG Setup before IOWR	tsuREG(IO WR)	tRGLI WL	5		5		5		5	
REG Hold following IOWR	thREG(IOW R)	tlWHR GH	0		0		0		0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35		Na1		Na1		Na 1
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35		Na1		Na1		Na 1

Table 11: I/O Write Timing

Notes:

1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA specification of 12 µs but is intentionally less in this specification.



Figure 7 I/O Write Timing Diagram



5.10.2.7 True IDE PIO Mode Read/Write Timing Specification



Figure 8 Read/Write Timing Diagram, PIO Mode

					-			
пт	O timing naramators	Mode	Mode	Mode	Mode	Mode	Mode	Mode
PI	o tining parameters	0	1	2	3	4	5	6
t ₀	Cycle time (min.)	600	383	240	180	120	100	80
	Address valid to							
t_1	HIOR-/HIOW- setup	70	50	30	30	25	15	10
	(min.)							
÷	HIOR-/HIOW- 16-bit	165	125	100	80	70	65	FF
L2	(min.)	105	125	100	80	70	05	55
÷	HIOR-/HIOW- Register	200	200	200	80	70	65	FF
L2	8-bit (min.)	290	290	290	80	70	5 100 15 65 65 25 20 5 15 20 5 20 5 15 20 5 20 5 20	55
+	HIOR-/HIOW- recovery				70	25	25	20
L2i	time (min.)	-	-	-	70	25	25	20
t ₃	HIOW- data setup (min.)	60	45	30	30	20	20	15
t4	HIOW- data hold (min.)	30	20	15	10	10	5	5
t5	HIOR- data setup (min.)	50	35	20	20	20	15	10
t ₆	HIOR- data hold (min.)	5	5	5	5	5	5	5
t ₆	HIOR- data tri-state	20	20	20	20	20	20	20
z	(max.)	50	50	50	50	50	20	20

Table 12: Read/Write Timing Specifications, PIO Mode 0-6

t7	Address valid to IOCS16- assertion (max.)	90	50	40	n/a	n/a	n/a	n/a
t ₈	Address valid to IOCS16- released (max.)	60	45	30	n/a	n/a	n/a	n/a
t9	HIOR-/HIOW- to address valid hold	20	15	10	10	10	10	10
t _R D	Read data valid to IORDY active (min.)	0	0	0	0	0	0	0
tA	IORDY setup time	35	35	35	35	35	n/a	n/a
tΒ	IORDY pulse width (max.)	1250	1250	1250	1250	1250	n/a	n/a
tc	IORDY assertion to release (max.)	5	5	5	5	5	n/a	n/a

5.10.2.8 True IDE Multiword DMA Mode Read/Write Timing Specification



Figure 9 Read/Write Timing Diagram, Multiword DMA Mode

Table 13: Read/Write Timing Specifications	, Multiword DMA Mode 0-4
--------------------------------------------	--------------------------

Mu	ltiword DMA timing	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	
parameters							
t ₀	Cycle time (min.)	480	150	120	100	80	
t⊳	HIOR-/HIOW- assertion width (min.)	215	80	70	65	55	
tE	HIOR- data access (max.)	150	60	50	50	45	
t _F	HIOR- data hold (min.)	5	5	5	5	5	
t _G	HIOR-/HIOW- data setup (min.)	100	30	20	15	10	
tн	HIOW- data hold (min.)	20	15	10	5	5	
tı	DMACK to HIOR-/HIOW- setup (min.)	0	0	0	0	0	
tı	HIOR-/HIOW- to DMACK hold (min.)	20	5	5	5	5	
t _K R	HIOR- negated width (min.)	50	50	25	25	20	
t _K w	HIOW- negated width (min.)	215	50	25	25	20	
t _L R	HIOR- to DMARQ delay (max.)	120	40	35	35	35	
t∟ w	HIOW- to DMARQ delay (max.)	40	40	35	35	35	
tм	CS1-, CS0- valid to HIOR-/HIOW-	50	30	25	10	5	
t_{N}	CS1-, CS0- hold	15	10	10	10	10	
tz	DMACK-	20	25	25	25	25	



5.10.2.9 True IDE Ultra DMA Mode Read/Write Timing Specification







Figure 11 Ultra DMA Mode Data-out Burst Initiation Timing Diagram
innodisk



Figure 12 Sustained Ultra DMA Mode Data-in Burst Timing Diagram



Figure 13 Sustained Ultra DMA Mode Data-out Burst Timing Diagram

	Table 14: Thinky L	nayi	am,	UILI			oue	U-4			
		Mode Mode M		Мос	de Mo		de Moo		le		
1114	DMA timing nerometers	0		1		2		3		4	
UILIA	DMA tilling parameters	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
			•	-	-	•	•	-	•	-	•
t _{2CY}	Typical sustained average	24	_	16		12		90	-	60	-
С	two cycle time	0	-	0	-	0	-				
+	Cycle time allowing for	11		72		54		20		25	
LCYC	asymmetry and clock	2	-	13	-	54	-	59	-	23	-

in a Diagra 111+ 1/1. Ti do Δ Л

	variations (from STROBE										
	edge to STROBE edge)										
t _{2CY} c	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	23 0	-	15 3	-	11 5	-	86	-	57	-
t_{DS}	Data setup time (at recipient)	15	-	10	-	7	-	7	-	5	-
t _{DH}	Data hold time (at recipient)	5	-	5	-	5	-	5	-	5	-
t _{DVS}	Data valid setup time at sender (from data bus being valid until STROBE edge)	70	-	48	-	31	-	20	-	6.7	-
t _{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	6.2	-	6.2	-	6.2	-	6.2	-	6.2	-
t _{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	-	23 0	-	20 0	-	17 0	-	13 0	-	12 0
tLI	Limited interlock time	0	15 0	0	15 0	0	15 0	0	10 0	0	10 0
t _{MLI}	Interlock time with minimum	20		20		20	-	20	-	20	-
t _{UI}	Unlimited interlock time	0	-	0	-	0	-	0	-	0	-
t _{AZ}	Maximum time allowed for output drivers to release (from being asserted or negated)	-	10	-	10	-	10	-	10	-	10
t _{ZAH}	Minimum delay time	20	-	20	-	20	-	20	-	20	-
t _{ZAD}	required for output drivers to assert or negate (from released state)	0	-	0	-	0	-	0	-	0	-
t _{en∨}	Envelope time (from DMACK- to STOP and HDMARDY- during data out burst initiation)	20	70	20	70	20	70	20	55	20	55
t _{RFS}	Ready-to-final-STROBE time	-	75	-	70	-	60	-	60	-	60

	(no STROBE edges shall be sent this long after negation of DMARDY-)										
t _{RP}	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY-)	16 0	-	12 5	-	10 0	-	10 0	-	10 0	-
t _{IOR} DYZ	Pull-up time before allowing IORDY to be released	-	20	-	20	-	20	-	20	-	20
t _{zio} RDY	Minimum time device shall wait before driving IORDY	0	-	0	-	0	-	0	-	0	-
t _{АСК}	Setup and hold times for DMACK- (before assertion or negation)	20	-	20	-	20	-	20	-	20	-
t _{ss}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	50		50	-	50	-	20	-	20	-

5.11 Transfer Function

5.11.1 I/O Transfer function

The I/O transfer to or from the iCF4000 can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal –IOIS16 is asserted by the iCF4000. Otherwise, the –IOIS16 signal is de-asserted. When a 16 bit transfer is attempted and the –IOIS16 signal is not asserted by the iCF4000, the system shall generate a pair of 8 bit references to access the word's even byte and odd byte. The iCF4000 permits both 8 and 16 bit accesses to all of its I/O addresses, so –IOIS 16 is asserted for add address to which the iCF4000 responds. The iCF4000 may request the host to extend the length of an input cycle until data ready by asserting the –WAIT signal at the start of the cycle.

Function Cod	le	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15~D8	D7~D0
Standby Mode	j	Х	Н	Н	Х	Х	Х	High Z	High Z
Byte Input Ac	cess	L	Н	L	L	L	Н	High Z	Even-Byte
(8 bits)		L	н	L	Н	L	Н	High Z	Odd-Byte
Byte Ou	tput	L	Н	L	L	Н	L	Don't	Even-Byte
Access		L	н	L	н	н	L	Care	Odd-Byte
(8 bits)								Don't	

Table 15: PCMCIA Mode I/O Function



							Care	
Word Input	L	L	L	L	L	Н	Odd-Byte	Even-Byte
Access								
(16bits)								
Word Output	L	L	L	L	Н	L	Odd-Byte	Even-Byte
Access (16bits)								
I/O Read Inhibit	Н	Х	Х	Х	L	Н	Don't	Don't Care
							Care	
I/O Write Inhibit	Н	Х	Х	Х	Н	L	High Z	High Z
High Byte Input	L	L	Н	Х	L	Н	Odd-Byte	High Z
Only (8 bits)								
High Byte Output	L	L	Н	Х	Н	L	Odd-Byte	Don't Care
Only (8bits)								

5.11.2 Common Memory Transfer Function

The Common Memory transfer to or from iCF4000 can be either 8 or 16 bits. The iCF4000 permits both 8 and 16 bit access to all of its Common Memory addresses. The iCF4000 request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the –WAIT signal at the start of the cycle.

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15~D8	D7~D0
Standby Mode	Х	Н	Н	Х	Х	Х	High Z	High Z
Byte Read Access	Н	Н	L	L	L	Н	High Z	Even-Byte
(8 bits)	н	н	L	Н	L	н	High Z	Odd-Byte
Byte Write Access	Н	Н	L	L	Н	L	Don't	Even-Byte
(8 bits)	н	н	L	н	н	L	Care	Odd-Byte
							Don't	
							Care	
Word Input Access	Н	L	L	Х	L	Н	Odd-Byte	Even-Byte
(16bits)								
Word Output Access	Н	L	L	Х	Н	L	Odd-Byte	Even-Byte
(16bits)								
Odd Byte Read Only	н	L	н	Х	L	Н	Odd-Byte	High Z
(8 bits)								
Odd Byte Write Only	Н	L	Н	X	Н	L	Odd-Byte	Don't Care
(8bits)								

Table 16: Common Memory Function

5.11.3 True IDE Mode I/O Transfer Function

The iCF4000 can be configured in a True IDE Mode of operation. The iCF4000 is configured in this mode only when -OE input signal is grounded by the host during the power off to power on cycle.

Function	-CS1	-CS0	-A0~	-DMACK	-IORD	-IOW	D15~D8	D7~D0
Code			A2			R		
	L	L	X	Х	Х	Х	Undefined	Undefined
							In/Out	In/Out
	L	X	X	L	L	Х	Undefined	Undefined
							Out	Out
Invalid Mode	L	Х	X	L	Х	L	Undefined	Undefined
							In	In
	Х	L	X	L	L	х	Undefined	Undefined
							Out	Out
	Х	L	X	L	Х	L	Undefined	Undefined
							In	In
Standby	н	Н	X	Н	Х	Х	High Z	High Z
Mode								
Task File	Н	L	1-7h	Н	Н	L	Don't Care	Data In
Write								
Task File Read	Н	L	1-7h	Н	L	Н	High Z	Data In
PIO Data	н	L	0	Н	Н	L	Odd-Byte	Even-Byte
Register Write							In	In
DMA Data	н	Н	X	L	Н	L	Odd-Byte	Even-Byte
Register Write							In	In
Ultra DMA	н	Н	X	L	See Not	e 1	Odd-Byte	Even-Byte
Data Register							In	In
Write						1		
PIO Data	Н	L	0	Н	L	Н	Odd-Byte	Even-Byte
Register Read							Out	Out
DMA Data	Н	Н	X	L	L	Н	Odd-Byte	Even-Byte
Register Read							Out	Out
Ultra DMA	н	н	X	L	See Not	e 2	Odd-Byte	Even-Byte
Data Register							Out	Out
Read						1		
Control	L	н	6h	Н	Н	L	Don't Care	Control In
Register Write								

Table 17: True IDE Mode I/O Function

Industrial CompactFlash Card 4000

Alt Status	L	Н	6h	Н	L	Н	High Z	Status Out
Read								
Drive Address	L	Н	7h	Н	L	Н	High Z	Data Out

Note1: In Ultra DMA Data Register Write mode the signals –IORD, -IOWR and IORDY are redefined and used as follows: -IORD as HSTROBE, -IOWR as STOP and IORDY as –DDMARDY. Data transfers with each edge of HSTROBE.

Note2: In Ultra DMA Data Register Read mode the signals –IORD, -IOWR and IORDY are redefined and used as follows: -IORD as –HDMARDY H, -IOWR as STOP and IORDY as DSTROBE. Data transfer with each edge of DSTROBE.

5.12 Configuration Register

5.12.1 Configuration Option Register (200h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the iCF4000.

			onngura	lion opti	on Regis			
Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevelREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Table 18: Configuration Option Register

Table 19: Information for Configuration Option Register

Name	Description						
SRSET	Soft Reset: Setting this bit to one (1), waiting the minimum reset						
	time and returning to zero(0) places the iCF4000 in the reset state.						
	Setting this bit to one (1) is equivalent to assertion of the +RESET						
	signal except that the SRESET bit is not cleared. Returning this bit						
	to zero (0) leaves the iCF4000 in the same un-configured, Reset						
	state as following power-up and hardware reset. This bit is PCMCIA						
	Soft Reset is considered a hard Reset by the ATA Commands.						
	Contrast with Soft Reset in the Device Control Register.						
LevelREQ	This bit is set to one (1) then Level Mode Interrupt is selected, and						
	zero (0) then Pulse Mode is selected. Set to zero (0) by Reset.						
Conf5-0	Configuration Index: Set to zero (0) by reset. It is used to select						
	operation mode of the iCF4000 as shown below						

Note: Conf5 and Conf4 are reserved for CompactFlash Storage cards and shall be written as zero(0).



Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte
						system decoded
						boundary
0	0	0	0	1	0	Primary I/O Mapped,
						1F0h~1F7h/3F6h ~
						3F7h
0	0	0	0	1	1	Secondary I/O Mapped,
						170h~177h/376h ~
						377h

Table 20:iCF4000 Configuration

5.12.2 Card Configuration and Status Register (202h in Attribute Memory)

The Card configuration and Status Register contains information about the Card's condition.

			-			-		
Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PweDwn	0	0

Table 21: Card Configuration and Status Register

Table 22: Information for Card Configuration and Status Register

Name	Description
Changed	Indicates that one or both of the Pin Replacement
	register CReady. Or CWProt bits are set to one(1). When
	the changed bit is set. –STSCHG Pin 46 us held low if the
	SigChg bit is a One(1) and the iCF4000 is configured for
	I/O interface.
SigChg	This bit is set and reset by the host to enable and disable
	a state-change "single" from the Status Register, the
	Changed bit controls pin 46, the Changed Status single.
	If no state change single is descried, this bit is set to
	zero(0) and pin46 (-STSCHG) single is then held high
	while the iCF4000 is configured for I/O.
IOis8	The host sets this bit to one (1) if the iCF4000 is to be
	configured in an 8 bit I/O Mode. The iCF4000 is always
	configured for both 8 and 16 bit I/O, so this bit is ignored.



PwrDwn	This bit indicates whether the host requests iCF4000 to
	be in the power saving or active mode. When the bit is
	one (1), the iCF4000 enter a power down mode. The
	PwrDwn is zero (0), the host is requesting the iCF4000 to
	enter the active mode. The PCMCIA READY value
	becomes false (busy) when this bit is changed. READY
	shall not become true (ready) until the power state
	requested has been entered. The iCF4000 automatically
	powers down when it is idle and powers back up when it
	receives a command.
Int	This bit represents the internal state of the interrupt
	request. This value is available whether or not the I/O
	interface has been configured. This signal remains true
	until the condition that caused the interrupt request has
	been serviced. If interrupts are disabled by the $-IEN$ bit
	in the Device Control Register, this bit is a zero (0).

5.12.3 Pin Replacement register (204h in Attribute Memory)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CReady	0	1	1	RReady	0
Write	0	0	CReady	0	0	0	MReady	0

Table 23: Pin Replacement Register

Table 24: Information for Pin Replacement Register

Name	Description
CReady	This bit is set to one (1) when the bit RReady changes state.
	This bit can also be written by the host.
RReady	This bit is used to determine the internal state of the READY
	signal. This bit may be used to determine the state of the
	READY signal as this pin has been reallocated for use as
	Interrupt Request on an I/O card. When written, this bit acts
	as a mask(MReady) for writing the corresponding bit CReady.
MReady	This bit acts as a mask for writing corresponding bit CReady.

5.12.4 Socket and Copy Register (206h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register. This register is used for identification of the card from the other card.



Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	0	Obsolete	0	0	0	0
				(Drive				
				#)				
Write	0	0	0	Obsolete	Х	Х	Х	Х
				(Drive				
				#)				

Table 25: Socket and Copy Register

Table 26: Information for Socket and Copy Register

Name	Description
Obsolete(Drive	This bit is obsolete and should be written
#)	as 0.

5.13 Software Interface

5.13.1 CF-ATA Drive Register Set Definition and Protocol

The iCF4000 can be configured as a high performance I/O device through:

- a) The standard PC-AT disk I/O address 1F0h-1F7h, 3F6h-3F7h (primary) or 170h-177h, 376h-377h (secondary) with IRQ14 (or other available IRQ).
- b) Any system decode 16 byte I/O block using any available IRQ.
- c) Memory space

The communication to or from the card is done using the Task File register, which provide all the necessary register for control and status information related to the storage medium. The PCMCIA interface connects peripherals to the host using four register mapping methods.

Standard Configurations											
Config Index	I/O o	· Add	ress	Description							
	Memory										
0	Memory	0h-l	Fh,	Memory Mapped							
		400	h-7FFh								
1	I/O	XX0	h-XXFh	I/O Mapped	16						
				Contiguous							
				Registers							
2	I/O	1F0	h-1F7h,	Primary	I/O						
		3F6	h-3F7h	Mapped							
3	I/O	170	h-177h,	Secondary	I/O						
		376	h-377h	Mapped							

Table 27: I/O Configuration



-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Note					
0	1F(17)h	0	0	0	0	Even RD Data	Even WR Data	1,2					
0	1F(17)h	0	0	0	1	Error Register	Features	1,2					
0	1F(17)h	0	0	1	0	Sector Count	Sector Count Sector Count						
0	1F(17)h	0	0	1	1	Sector No.	Sector No.						
0	1F(17)h	0	1	0	0	Cylinder Low	Cylinder Low						
0	1F(17)h	0	1	0	1	Cylinder High	Cylinder High						
0	1F(17)h	0	1	1	0	Select	Select						
						Card/Head	Card/Head						
0	1F(17)h	0	1	1	1	Status	Command						
0	3F(37)h	0	1	1	0	Alt Status Device Control							
0	3F(37)h	0	1	1	1	Drive Address	Reserved						

Table 28: Primary and Secondary I/O Decoding

5.13.2 I/O Primary and Secondary Address Configurations

Note 1) Register 0 is accessed with -CE1 low and -CE2 low (and A0=Don't care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte access to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers, which lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

Note2) A byte access to register 0 with -CE1 high and -CE2 low access the error (read) or feature (write) register.

5.13.3 Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the card, the registers are accessed in the block of I/O space decoded by the system as follows:

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Note
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count Sector Count		
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card/Head Select Card/Head		
0	0	1	1	1	7	Status	Command	

Table 29: Contiguous I/O Decoding



0	1	0	0	0	8	Dup Even RD Data	Dup. Even	WR	2
							Data		
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd	WR	2
							Data		
0	1	1	0	1	D	Dup. Error	Dup. Feature		2
0	1	1	1	0	Е	Alt Status	Device Ctl		
0	1	1	1	1	F	Drive Address	Reserved		

Note 1) Register 0 is accessed with -CE1 low and -CE2 low (and A0=Don't care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte access to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

Note 2) A byte access to register 0 with -CE1 high and -CE2 low access the error (read) or feature (write) register.

Note 3) Address lines that are not indicated are ignored by the card for accessing all the registers in this table.

5.13.4 Memory Mapped Addressing

When the card registers are accessed via memory references, the register appears in the common memory space window: 0-2K bytes as follows:

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Note
1	0	Х	0	0	0	0	0	Even RD	Even WR	1,2
								Data	Data	
1	0	Х	0	0	0	1	1	Error	Features	1,2
1	0	Х	0	0	1	0	2	Sector	Sector	
								Count	Count	
1	0	Х	0	0	1	1	3	Sector No. Sector No.		
1	0	Х	0	1	0	0	4	Cylinder	Cylinder	
								Low	Low	
1	0	Х	0	1	0	1	5	Cylinder	Cylinder	
								High	High	
1	0	Х	0	1	1	0	6	Select	Select	
								Card/Head	Card/Head	
1	0	Х	0	1	1	1	7	Status	Command	
1	0	Х	1	0	0	0	8	Dup Even	Dup. Even	2
								RD Data	WR Data	

Table 30: Memory Mapped Decoding

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Industrial CompactFlash Card 4000

1	0	Х	1	0	0	1	9	Dup.	Odd	Dup.	Odd	2
								RD Data	а	WR Dat	WR Data	
1	0	Х	1	1	0	1	D	Dup. Er	ror	Dup.		2
										Feature	9	
1	0	Х	1	1	1	0	Е	Alt Status		Device Ctl		
1	0	Х	1	1	1	1	F	Drive		Reserved		
								Address				
1	1	Х	Х	Х	Х	0	8	Even	RD	Even	WR	3
								Data		Data		
1	1	Х	Х	Х	Х	1	9	Odd	Rd	Odd	WR	3
								Data		Data		

Note 1) Register 0 is accessed with -CE1 low and -CE2 low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte access to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte accesses to register 0 with -CE1 high and -CE2 low access the error (read) or feature (write) register.

Note 2) Register at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the register is byte accessed in the order 9 then 8 the data shall be transferred odd byte then even byte. Repeated byte accessed to register 8 or 0 shall access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 shall access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to register 8 then 9 shall access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 are not supported. However, repeated alternating byte accesses to register 8 then 9 shall access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

Note 3) Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 K byte memory window to the data register is provide so that hosts can perform memory block moves to the data register when the register lies in memory space.

Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction, Some PCMCIA socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently. Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the card. A word access to address at offset 8 shall provide even data on the low-order byte of the data bus, along with odd data at offset 9 on the high-order byte of the bus.



5.13.5 True IDE Mode Addressing

When the iCF4000 is configured in the True IDE mode, the I/O decoding is as follows:

-CS1	-CS0	A2	A1	A0	-DMACK	-IORD=0	-IOWR=0	Note
1	0	0	0	0	1	PIO RD Data	PIO WR Data	8 or
								16 bit
1	1	Х	Х	Х	0	DMA RD Data	DMA WR Data	16 bit
1	0	0	0	1	1	Error Register	Features	8 bit
1	0	0	1	0	1	Sector Count	Sector Count	8 bit
1	0	0	1	1	1	Sector No.	Sector No.	8 bit
1	0	1	0	0	1	Cylinder Low	Cylinder Low	8 bit
1	0	1	0	1	1	Cylinder High	Cylinder High	8 bit
1	0	1	1	0	1	Select	Select	8 bit
						Card/Head	Card/Head	
1	0	1	1	1	1	Status	Command	8 bit
0	1	1	1	0	1	Alt Status	Device Control	8 bit

Table 31: True IDE Mode I/O Decoding

5.13.6 CF-ATA Register

The following section describes the hardware registers used by the host software to issue commands to the iCF4000.

Note:

In accordance with the PCMCIA specification: each of the registers below that is located at an odd offset address may be accessed in the PC Card Memory or PC Card I/O modes at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when -CE1 is high and -CE2 is low unless -IOIS16 is high (not asserted by the card) and an I/O cycle us being performed.

In True IDE Mode of operation, the size of the transfer is based solely on the register being addressed. All registers are 8 bit only except for the Data Register, which is normally 16 bits, but can be programmed to use 8 bit transfers for Non-DMA operations through the use of the Set Features command. The data register is also 8 bits during a portion of the Read Long and Write Long commands, which exist solely for historical reasons and should not be used.

5.13.6.1 Data Register

The Data Register is a 16 bit register, and it is used to transfer data blocks between the card and the host. This register overlaps the Error Register. This register can be accessed in word and byte mode.



Table 32: Data Register

Data	Data Register														
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

5.13.6.2 Error Register

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

Table 3	3: Error	Register
---------	----------	----------

BBK	UNC	0	IDNF	0	ABRT	0	AMNF
D7	D6	D5	D4	D3	D2	D1	D0

5.13.6.3 Feature Register

This register provides information regarding features of the card that the host can utilize. This register is also accessed in PC Card modes on data D15-D8 during a write operation to Offset 0 with -CE2 low and -CE1 high.

Table 34: Feature Register

Feature Re	gister				Feature Register									
D7	D6	D5	D4	D3	D2	D1	D0							

5.13.6.4 Sector Count Register

This registers the number of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

Table 35: Sector Count Register

Sector Cou	nt Register						
D7	D6	D5	D4	D3	D2	D1	D0

5.13.6.5 Sector Number Register

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for iCF4000 data access for the subsequent command.

 Table 36: Sector Number Register

Sector Nun	Sector Number Register									
D7	D6	D5	D4	D3	D2	D1	D0			



5.13.6.6 Cylinder Low Register

This Register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

Table 37: Cylinder Low Register

Cylinder Lo	w Register						
D7	D6	D5	D4	D3	D2	D1	D0

5.13.6.7 Cylinder High Register

This Register contains the high order 8 bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

Table 38: Cylinder High Register

Cylinder Hi	Cylinder High Register									
D7	D6	D5	D4	D3	D2	D1	D0			

5.13.6.8 Device/Head Register

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing.

Table 39: Device/Head Registe	Table	39:	Device,	/Head	Registe
-------------------------------	-------	-----	---------	-------	---------

1	LBA	1	DRV	HS3	HS2	HS1	HS0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: this bit is set 1.

Bit6: LBA is a flag to select either Cylinder/Head/Sector or Logical Block Address mode. When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected.

Bit5: this bit is set 1.

Bit4: DRV is the drive number. When DRV=0, drive (card) 0 is selected. When DRV=1, drive (card) 1 is selected. Setting this bit to1 is obsolete in PCMCIA modes of operation.

Bit3: When operation in the Cylinder/Head/Sector mode, this is bit 3 of the head number. It is bit 27 in the Logical Block Address mode.

Bit2: When operation in the Cylinder/Head/Sector mode, this is bit 2 of the head number. It is bit 26 in the Logical Block Address mode.

Bit1: When operation in the Cylinder/Head/Sector mode, this is bit 1 of the head number. It is bit 25 in the Logical Block Address mode.

Bit0: When operation in the Cylinder/Head/Sector mode, this is bit 0 of the head number. It is bit 24 in the Logical Block Address mode.

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5.13.6.9 Status Register

These registers return the iCF4000 status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not.

BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR
D7	D6	D5	D4	D3	D2	D1	D0

Table 40: Status Register

Bit7: the busy bit is set when the iCF4000 has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit set to a 1.

Bit6: RDY indicates whether the device is capable of performing iCF4000 operations. This bit is cleared at power up and remains cleared until the card is ready to accept a command.

Bit5: This bit, if set, indicates a write fault has occurred.

Bit4: This bit is set when the iCF4000 is ready.

Bit3: The Data Request is set when the iCF4000 requires that information be transferred either to or from the host through the Data register.

During the data transfer of DMA commands, the card shall not asserted DMARD unless either the BUST bit, the DRQ, or both are set to one.

Bit2: This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit1: This bit is always to 0.

Bit0: This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information description the error.

5.13.6.10 Device Control Register

This register is used to control the iCf4000 interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY.

Х	Х	Х	Х	Х	SW Rst	-IEn	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 41: Device Control Register

Bit7-3: These bits are ignored.

Bit2: This bit is set to 1 in order to force the iCF4000 to perform a Soft Reset operation. This does not change PCMCIA Card Configuration Register as a hardware Reset does. The Card remains in Reset until this bit is reset to '0'.



Bit1: the Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupt from the iCF4000 are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset. **Bit0**: This bit is ignored.

5.13.6.11 Drive Address Register

This register is provide for compatibility with the AT disk drive interface.

Х	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0
D7	D6	D5	D4	D3	D2	D1	D0

Bit7: this bit is unknown.

Bit6: this bit is – when a write operation is in progress; otherwise, it is 1.

Bit5: this bit is the negation of bit 3 in the Drive/Head register.

Bit4: this bit is the negation of bit 2 in the Drive/Head register.

Bit3: this bit is the negation of bit 1 in the Drive/Head register.

Bit2: this bit is the negation of bit 0 in the Drive/Head register.

Bit1: this bit is 0 when drive 1 is active and selected.

Bit0: this bit is 0 when the drive 0 is active and selected..

5.14 Hardware Reset(Only for Memory Card mode and I/O Card Mode)

	Item	Min.	Max.	Normal	Unit
ts∪(RESET)	Reset Setup	20	-	-	ms
	Time				
t _{REC} (VCC)	-CE Recover	1	-	-	us
	Time				
t _{PR}	VCC rising up	0.1	100	-	ms
	time				
tpf	VCC falling	3	300	-	ms
	down time				
tw(RESET)	Reset pulse	10	-	-	ms
t _H (Hi-ZRESET)	width	0	-	-	
t _s (Hi-ZRESET)		0	-	-	

Table 43: Timing Diagram, Hardware Reset



Hardware Reset Timing



Figure 14 Timing Diagram, Hardware Reset

Note: It shows the electric character of our controller. It is irrelevant to power supply or prevention from sudden power loss protection.

5.15 Power On Reset

When the VCC power reaches to 2.7V, the disk drive will be reset.

		-	=			
	Item	Min.	Max.	Normal	Unit	Note
ts∪(RESET)	-CE Setup Time	20	I	I	ms	
t _{PR}	-VCC Rising Up	0.1	100	-	ms	
	Time					

Table 44: Timing Diagram, Power On Reset

Power on Reset Timing



Figure 15 Timing Diagram, Power On Reset



Each timing specification is shown as Table 45.

Table 45: Timing specification for each mode

Timing	Mode	mini	Max.	Note
tBSY_PORST	PC Card	5ms	500ms	
	True IDE	5ms	500ms	Slave configuration
		400ms	1 second	Master without slave
				device
		5ms	32 seconds	Master with slave device

5.16 Supported IDE Commands

iCF4000 supports the commands listed in Table 46.

Table	46:	IDE	Commands
-------	-----	-----	----------

Class	Command	Code		FR	SC	SN	СҮ	DH	LBA
1	Check Power Mode	98H E5H	or	-	-	-	-	D	-
1	Execute Device Diagnostic	90H		-	-	-	-	D	-
1	Erase Sector(s)	COH		-	Y	Y	Y	Y	Y
2	Format Track	50H		-	Y	-	Y	Y	Y
1	Identify Device	ECH		-	-	-	-	D	-
1	Idle	97H E3H	or	-	Y	-	-	D	-
1	Idle immediate	95H E1H	or	-	-	-	-	D	-
1	Initialize Device Parameters	91H		-	Y	-	-	Y	-
1	Read Buffer	E4H		-	-	-	-	D	-
1	Read DMA	C8H		-	Y	Y	Y	Y	Y
1	Read Long Sector	22H 23H	or	-	-	Y	Y	Y	Y
1	Read Sector(s)	20H 21H	or	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40H 41H	or	-	Y	Y	Y	Y	Y
1	Recalibrate	1XH		-	-	-	-	D	-
1	Request Sense	03H		-	-	-	-	D	-
1	Seek	7XH		-	-	Y	Y	Υ	Y
1	Set Features	EFH		Y	-	-	-	D	-
1	Set Sleep Mode	99H	or	-	-	-	-	D	-

		E6H							
1	Standby	96H	or	-	-	-	-	D	-
	Standby	E2H							
1	Standby Immodiate	94H	or	-	-	-	-	D	-
	Standby Immediate								
2	Write Buffer	E8H		-	-	-	-	D	-
2	Write DMA	CAH		-	Y	Y	Y	Y	Y
2	Write Sector(c)	30H	or	-	Y	Y	Y	Y	Y
	write Sector(s)	31H							
2	Write Sector(s) without	201		-	Y	Y	Y	Y	Y
	Erase	J01							

Defines:

FR: Feature Register

SC: Sector Count Register

SN: Sector Number Register

CY: Cylinder Registers

DH: Card/Device/Head Register

LBA: LBA Block Address Mode Supported

Y: The register contains a valid parameter for this command. For Card/Device/Head Register Y means both the CompactFlash Storage Card and head parameter are used; D – only the CompactFlash Storage Card parameter is valid and not the head parameter; C – The register contains command specific data (see command description for use).

5.16.1 Check power mode – 98H or E5H

Register	7	6	5	4	3	2	1	0
Command(7)	98h or	E5h						
C/D/H(6)	Х			Drive	Х			
Cylinder	Х							
High(5)								
Cylinder Low(4)	Х							
Sector	Х							
Number(3)								
Sector Count(2)	Х							
Feature(1)	Х							

This command checks the power mode:

If the CompactFlash Storage is in, going to, or recovering from the sleep mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt.

If the compactFlash Storage Card is in idle mode, the CompactFlash Storage



Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

Register	7	6	5	4	3	2	1	0
Command(7)	90h							
C/D/H(6)	Х			Drive	Х			
Cylinder	Х							
High(5)								
Cylinder Low(4)	Х							
Sector	Х							
Number(3)								
Sector Count(2)	Х							
Feature(1)	Х							

5.16.2 Execute Device Diagnostic – 90H

This command performs the internal diagnostic tests implemented by the CompactFlash Storage Card. When the diagnostic command is issued in a PCMCIA configuration mode, this command runs only on the CompactFlash Storage Card that is addressed by the Drive/Head register. This is because PCMCIA card interface does not allow for direct inter-drive communication (such as the ATA PDIAG and DASP signals). When the diagnostic command is issued in the True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices. The Diagnostic codes are shown in Table 47. Diagnostic Codes are returned in the Error Register at the end of the command.

	5
Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controller Microprocessor Error
8Xh	Slave Error in True IDE Mode

Table 47: Diagnostic

5.16.3 Erase Sector(s) – COH

Register	7	6	5	4	3	2	1	0
Command(7)	C0h	C0h						
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder	Cylinde	Cylinder High (LBA 23-16)						
High(5)								



Cylinder Low(4)	Cylinder Low (LBA 15-8)
Sector	Sector Number (LBA 7-0)
Number(3)	
Sector Count(2)	Sector Count
Feature(1)	X

This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

5.16.4 Format Track – 50H

Register	7	6	5	4	3	2	1	0	
Command(7)	50h	50h							
C/D/H(6)	1	1 LBA 1 Drive Head (LBA 27-24)							
Cylinder	Cylinde	Cylinder High (LBA 23-16)							
High(5)									
Cylinder Low(4)	Cylinde	Cylinder Low (LBA 15-8)							
Sector	X (LBA	X (LBA 7-0)							
Number(3)									
Sector Count(2)	Count(Count(LBA mode only)							
Feature(1)	X								

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the CompactFlash Storage Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the CompactFlash Storage Card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

5.16.5 Identify Device – ECH

Register	7	6	5	4	3	2	1	0
Command(7)	ECh							
C/D/H(6)	Х	Х	Х	Drive	Х			
Cylinder	Х							
High(5)								
Cylinder Low(4)	Х							
Sector	Х							
Number(3)								
Sector Count(2)	Х							
Feature(1)	Х							

The Identify Device command enables the host to receive parameter information from the CompactFlash Storage Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 49. All reserved bits or words are zero. Hosts should not depend in Obsolete words in Identify Device containing 0. Table 48 specifies each filed in the data returned by the Identify Device Command. In Table 48, X indicates a numeric nibble vale specific to the card and aaaa indicates an ASCII string specific to the particular drive.

Word	Description	Value
	General Configuration	
	Bit 15 0=ATA device	
	Bit 14:8 Retired	
0	Bit 7:6 Obsolete	045Ab
0	Bit 5:3 Retired	
	Bit 2 Response incomplete	
	Bit 1 Retired	
	Bit 0 reserved	
1	Number of logical cylinders	XXXXh
2	Specific configuration	0000h
3	Number of logical heads	0010h
4-5	Retired	0000h 0200h
6	Number of logical sectors per logical track	00XXh
7-8	Number of sectors per card	XXXXh
9	Retired	0000h
10-19	Serial number in 20 ASCII	Aaaa
20-21	Retired	0002h 0001h
22	Obsolete	0004h
23-26	Firmware revision in 8 ASCII	Аааа
27-46	Model number in 40 ASCII	Аааа
	15-8: 80	
	7-0: 00h Reserved	
47	01h-FFh: Maximum number of sectors that shall be	80 XXh
	transferred per DRQ data block on READ/WRITE	
	Multiple commands	
	Trusted Computing feature set options	
48	15 shall be cleared to zero	0000h
	14 shall be set to one	

Table 48: IDENTIFY DEVICE information



	13:1 Reserved for the Trusted Computing Group	
	0 0 = Trusted Computing feature set is not supported	
	Capabilities	
	15-14: Reserved for the IDENTIFY PACKET DEVICE	
	command.	
	13: 1=Standby timer values as specified in this	
	standard are supported	
	0:Standby timer values shall be managed by the	
	device	
49	12: Reserved for the IDENTIFY PACKET DEVICE	0F00h
	command	
	11: 1=IORDY supported	
	0=IORDY may be disabled	
	10 1: IORDY may be disabled	
	9 1=LBA supported	
	8 1=DMA supported.	
	7-0 Retired	
	Capabilities	
	15: Shell be cleared to zero	
50	14: Shall be set to one	0000
50	13:2 Reserved	000011
	1 Obsolete	
	0 0	
51	PIO data transfer cycle timing mode	0200h
52	Obsolete	0000h
	15 Free-fall control Sensitivity	
	00h: Vendor's recommended setting	
53	7:3 Reserved	0007b
55	2: 1=the fields reported in word 88 are valid	000711
	1: 1=the fields reported in words (70:64) are valid	
	0: Obsolete	
54	Number of current logical cylinders	XXXXh
55	Number of current logical heads	XXXXh
56	Number of current logical sectors per logical track	XXXXh
57-58	Current capacity in sectors	XXXXh
	15:9 Reserved	
	8 0:Multiple sector setting is invalid	
59	7:0 Current setting for number of logical sectors that	01XXh
	shall be transferred per DRQ data block on	
	READ/WRITE Multi commands	



60-61	Total number of user address sectors(DWord)	XXXXXXXXh		
62	Obsolete	0000h		
63	Multi-word DMA transfer(Not support)	0007h		
<u> </u>	15-8 Reserved	00021-		
64	7-0 PIO modes supported	00030		
	Minimum Multiword DMA transfer cycle time per word			
65	15-0 Cycle time in nanoseconds	0078h		
	In PCMCIA mode this value shall be 0h			
	Manufacturer's recommended Multiword DMA transfer			
66	cycle time per word	0078b		
00	15-0 Cycle time in nanoseconds	007011		
	In PCMCIA mode this value shall be 0h			
67	Minimum PIO transfer cycle time without flow control	0078b		
	15-0 Cycle time in nanoseconds			
68	Minimum PIO transfer cycle time with IORDY flow control	0078b		
	15-0 Cycle time in nanoseconds	007011		
69-74	Reserved	0000h		
75	No DMA QUEUED command supports	0000h		
	Serial ATA Capabilities			
	15:11 Reserved for Serial ATA			
	10 1= Supports Phy Event Counters			
	9 1= Supports receipt of host initiated power			
	management			
76	Requests	0000h		
	8 0= No Support native Command Queuing			
	7:3 Reserved for future SATA signaling speed grades			
	2 1=Supports SATA Gen2 Signaling Speed (3.0Gb/s)			
	1 1=Support SATA Gen1 Signaling Speed (1.5Gb/s)			
	0 Shall be cleared to zero			
77	Reserved for Serial ATA	0000h		
	Serial ATA features supported			
78	15:7 Reserved for Serial ATA			
	6 0=Device not supports Software Settings			
	Preservation			
	5 Reserved for Serial ATA	0000b		
	4 0= Device not supports in-order data delivery	000011		
	3 0= Device not supports initiating power management			
	2 0= Device not supports DMA Setup auto-activation			
	1 0= Device not supports non-zero buffer offsets			
	0 Shall be cleared to zero			

	Serial ATA feature enabled	
	15:7 Reserved for Serial ATA	
	6 0=Software Settings Preservation not enabled	
	5 0=Reserved for Serial ATA	
79	4 0= In-order data delivery not enabled	0000h
	3 0= Device initiated power management not enabled	
	2 0= DMA setup auto-activation not enabled	
	1 0= Non-zero buffer offsets not enabled	
	0 Shall be cleared to zero	
80-81	ATA Version support (ATA5)	0020 0000h
	Command and feature sets supported	
	15 0 = Obsolete	
	14 0 = NOP Command not supported	
	13 0 = READ BUFFER Command not supported	
	12 0 = WRITE BUFFER Command not supported	
	11 0 = Obsolete	
	10 0 = Host Protected Area Feature Set not supported	
	9 0 = DEVICE RESET Command not supported	
	8 0 = SERVICE Interrupt not supported	
82	7 0 = RELEASE Interrupt not supported	7008h
	6 1 = Look-ahead supported	
	5 1 = Write Cache supported	
	4 0 = indicate that the PACKET feature set is not	
	supported	
	3 1 = mandatory Power Management Feature Set	
	supported	
	2 0 = Obsolete	
	1 0 = Security Mode Feature Set not supported	
	0 1 = SMART Feature Set supported	
	Command and feature sets supported	
	15 Shall be cleared to zero	
	14 Shall be set to one	
	13 0 = FLUSH CACHE EXT Command not supported	
	12 1 = mandatory FLUSH CACHE Command supported	
83	11 0 = Device Configuration Overlay feature set not	5004h
	supported	
	10 0 = 48-Bit Address feature set not supported	
	9 0 = Automatic Acoustic Management feature set not	
	supported	
	8 0 = SET MAX security extension not supported	

	7 0 = See Address Offset Reserved Area Boot, INCITS	
	TR27:2001	
	6 0 = SET FEATURES subcommand not required to	
	spin-up after power-up	
	5 0 = Power-Up in Standby feature set supported	
	4 0 = Removable Media Status Notification feature set	
	not supported	
	3 0 = Advanced Power Management feature set not	
	supported	
	2 0 = CFA feature set not supported	
	1 0 = READ/WRITE DMA QUEUED not supported	
	0 1 = DOWNLOAD MICROCODE Command supported	
	Command Set/Feature Supported Extension	
	15 Shall be cleared to zero	
	14 Shall be set to one	
	13-6 Reserved	
	5 0 = General Purpose Logging feature set not	
04	supported	4000b
04	4 reserved	400011
	3 0 = Media Card Pass Through Command feature set	
	not supported	
	2 0 = Media Serial Number not supported	
	1 0 = SMART self-test not supported	
	0 1 = SMART Error Logging not supported	
	Command and feature sets supported or enabled	
	15 0 = Obsolete	
	14 0 = NOP Command not enabled	
	13 0 = READ BUFFER Command not enabled	
	12 0 = WRITE BUFFER Command not enabled	
	11 Obsolete	
	10 0 = Host Protected Area feature set not enabled	
85	9 0 = DEVICE RESET Command not enabled	7008
85	8 0 = SERVICE Interrupt not enabled	7008
	7 0 = RELEASE Interrupt not enabled	
	6 0 = Look-ahead not enabled	
	5 0 = Write Cache not enabled	
	4 Shall be cleared to zero to indicate that the PACKET	
	Command feature set is not supported.	
	3 1 = Power Management Feature Set enabled	
	2 0 = Removable Media feature set not enabled	



	1 0 = Security Mode Feature Set not enabled							
	0 0 = SMART Feature Set not enabled							
	Command set/feature enabled							
	15-14 0 = Reserved							
	13 0 = FLUSH CACHE EXT Command not supported							
	12 1 = FLUSH CACHE Command supported							
	11 0 = Device Configuration Overlay not supported							
	10 0 = 48-Bit Address features set not supported							
	9 0 = Automatic Acoustic Management feature set not enabled							
	8 0 = SET MAX security extension not enabled by SET							
	MAX SETPASSWORD							
86	7 0 = Reserved	1004h						
	6 0 = SET FEATURES subcommand required to spin-up							
	after power-up not enabled							
	5 0 = Power-Up in Standby feature set not enabled							
	4 0 = Obsolete							
	3 1 = Advanced Power Management feature set enabled							
	2 0 = CFA feature set not supported							
	1 0 = READ/WRITE DMA QUEUED Command not							
	supported							
	0 1 = DOWNLOAD MICROCODE Command supported							
	Command and feature sets supported or enabled							
	15 Shall be cleared to zero							
	14 Shall be set to one							
	13 1 = IDLE IMMEDIATE with UNLOAD FEATURE							
	supported							
	12 0 = Reserved for Technical Report, INCITS							
	TR-37-2004							
	11 0 = Reserved for Technical Report, INCITS							
87	TR-37-2004	4000h						
	10:9 0 = Obsolete							
	8 0 = 64-Bit World Wide Name not supported							
	7 0 = WRITE DMA QUEUED FUA EXT Command not							
	supported							
	6 0 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA							
	EXT commands not supported							
	5 0 = General Purpose Logging feature set not							
	supported							
	4 0 = Obsolete							

	3 0 = Media Card Pass Through Command feature set	
	not supported	
	2 0 = Media Serial Number is not valid	
	1 0 = SMART Self-Test not supported	
	0 0 = SMART Error-Logging not supported	
	Ultra DMA modes	
	15 Reserved	
	14 0 = Ultra DMA mode 6 is not supported	
	13 1= Ultra DMA mode 5 is selected	
	0= Ultra DMA mode 5 is not selected	
	12 1= Ultra DMA mode 4 is selected	
	0= Ultra DMA mode 4 is not selected	
	11 1= Ultra DMA mode 3 is selected	
	0= Ultra DMA mode 3 is not selected	
	10 1= Ultra DMA mode 2 is selected	
	0= Ultra DMA mode 2 is not selected	
88	9 1= Ultra DMA mode 1 is selected	XX1Fh
	0= Ultra DMA mode 1 is not selected	
	8 1= Ultra DMA mode 0 is selected	
	0= Ultra DMA mode 0 is not selected	
	7 Reserved	
	6 0= Ultra DMA mode 6 is not supported	
	5 1= Ultra DMA mode 5 and below are supported	
	4 1= Ultra DMA mode 4 and below are supported	
	3 1= Ultra DMA mode 3 and below are supported	
	2 1= Ultra DMA mode 2 and below are supported	
	1 1= Ultra DMA mode 1 and below are supported	
	0 1= Ultra DMA mode 0 is supported	
20	Time required for Normal Erase mode SECURITY ERASE	0000
89	UNIT command	00001
00	Time required for Enhanced erase mode SECURITY ERASE	0000
90	UNIT command	00001
91	Current advanced power management level value	0000h
92	Master Password Identifier	0000h
93	Hardware reset result	404Fh
	Current automatic acoustic management value	
94	15:8 Vendor's recommended acoustic management value	0000h
	7:0 Current automatic acoustic management value.	
95-126	Reserved	0000h



127	Obsolete	0000h	
	Security Status		
	15:9 Reserved		
	8 Security level 0 = high, 1 = Maximum		
	7:6 Reserved		
179	5 1= Enhanced security erase supported	VVVVb	
120	4 1= Security count expired	~~~~	
	3 0= Security frozen.		
	2 0 = Security not locked		
	1 0= Security not enabled		
	0 0= Security not supported		
129-159	Vendor specific	XXXXh	
160	CFA power mode 1	A064h	
161-162	Reserved	0000h	
163-164	Reserved	0012 001Bh	
165-175	Reserved	0000h	
176-205	Current media serial number	0000h	
206-254	Reserved	0000h	
	Integrity word		
255	15:8 Check Sum	XXXXh	
	7:0 Signature		

5.16.6 Idle -97H or E3H

Register	7	6	5	4	3	2	1	0			
Command(7)	97h or	97h or E3h									
C/D/H(6)	Х	X Drive X									
Cylinder	Х										
High(5)											
Cylinder Low(4)	Х										
Sector	Х										
Number(3)											
Sector Count(2)	Timer	Count (5	5 msec i	ncreme	nts)						
Feature(1)	Х										

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA sepecification.



5.16.7 Idle immediate - 95H or E1H

Register	7	6	5	4	3	2	1	0			
Command(7)	95h or	95h or E1h									
C/D/H(6)	Х			Drive	Х						
Cylinder	Х										
High(5)											
Cylinder Low(4)	Х										
Sector	Х										
Number(3)											
Sector Count(2)	Х										
Feature(1)	Х										

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt.

5.16.8 Initialize Device Parameters - 91H

Register	7	6	5	4	3	2	1	0			
Command(7)	91h	91h									
C/D/H(6)	Х	0	Х	Drive	Max He	ead (no.	of head	ls-1)			
Cylinder	Х										
High(5)											
Cylinder Low(4)	Х										
Sector	Х										
Number(3)											
Sector Count(2)	Number of sectors										
Feature(1)	Х	X									

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Device/Head registers are used by this command.

5.16.9 Read Buffer - E4H

Register	7	6	5	4	3	2	1	0
Command(7)	E4h							
C/D/H(6)	Х			Drive	Х			
Cylinder	Х							
High(5)								
Cylinder Low(4)	Х							
Sector	Х							
Number(3)								
Sector Count(2)	Х							

Feature(1)

Х

The Read Buffer command enables the host to read the current contents of the CompactFlash Storage Card's sector buffer. This command has the same protocol as the Read Sector(s) command.

5.16.10 Read DMA - C8H

Register	7	6	5	4	3	2	1	0			
Command(7)	C8	C8									
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-	24)				
Cylinder	Cylinde	Cylinder High (LBA 23-16									
High(5)											
Cylinder Low(4)	Cylinde	er Low (LBA 15-	8							
Sector	Sector	Numbe	(LBA 7-0	C							
Number(3)											
Sector Count(2)	Sector	Sector Count									
Feature(1)	Х	X									

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 request 256 sectors. The transfer begins at he sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, cleat BSY. The Card asserts DMAREQ while data is available to be transferred. The Card asserts DMAREQ while data is available to be transferred. The Nost then reads the (512 & sector –count) bytes of data from the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts –DMACK while it is ready to transfer data by DMA and asserts –IORD once for each 16 bit word to be transferred to the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder, head, and sector number of the sector where the occurred. The amount of data transferred is indeterminate.

When a Read DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

5.16.11 Read Long Sector - 22H or 23H



Register	7	6	5	4	3	2	1	0		
Command(7)	22h or 23h									
C/D/H(6)	1	1 LBA 1 Drive Head (LBA 27-24)								
Cylinder	Cylinde	Cylinder High (LBA 23-16)								
High(5)										
Cylinder Low(4)	Cylinde	er Low (LBA 15-	8)						
Sector	Sector	Numbe	r (LBA 7	'-0)						
Number(3)										
Sector Count(2)	X									
Feature(1)	X									

The Read Long command performs similarly to the Read Sector(s) command except that is returns 516 bytes of data instead of 512 bytes. During a Read Long command, the CompactFlash Storage Card does not check the ECC bytes to determine if there consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

5.16.12	Read Sector(s) - 20H or 21H	

Register	7	6	5	4	3	2	1	0		
Command(7)	20h or	20h or 21h								
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-	·24)			
Cylinder	Cylinde	er High	(LBA 23	-16)						
High(5)										
Cylinder Low(4)	Cylinde	er Low (LBA 15-	·8)						
Sector	Sector	Numbe	r (LBA 7	'-0)						
Number(3)										
Sector Count(2)	Sector	Sector Count								
Feature(1)	Х	X								

This command reads from 1 to 256 sectors as specified in the Sector Count Register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has buffer, sets DRQ, cleats BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder head, and sector number of the sector 2where the error occurred. The flawed data is pending in the sector buffer.



Register	7	6	5	4	3	2	1	0		
Command(7)	40h or	40h or 41h								
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-	24)			
Cylinder	Cylinde	Cylinder High (LBA 23-16)								
High(5)										
Cylinder Low(4)	Cylinde	er Low (LBA 15-	8)						
Sector	Sector	Numbe	r (LBA 7	-0)						
Number(3)										
Sector Count(2)	Sector	Sector Count								
Feature(1)	Х									

5.16.13 Read Verify Sector(s) - 40H or 41H

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash Storage Card sets BSY. When the requested sectors have been verified, the CompactFlash Storage Card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified. If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

5.16.14 Recalibrate - 1XH

Degister	7	6	F	4	2	C	1	0			
Register	/	0	5	4	3	2	T	0			
Command(7)	1Xh	1Xh									
C/D/H(6)	1	LBA	1	Drive	Х						
Cylinder	Х										
High(5)											
Cylinder Low(4)	Х										
Sector	Х										
Number(3)											
Sector Count(2)	Х										
Feature(1)	х										

This command is effectively a NOP command to the CompactFlash Storage Card and is provided for compatibility.

5.16.15 Request Sense - 03H



C/D/H(6)	1	LBA	1	Drive	Х
Cylinder	Х				
High(5)					
Cylinder Low(4)	Х				
Sector	Х				
Number(3)					
Sector Count(2)	Х				
Feature(1)	Х				

This command requests extended error information for the previous command. Table49 defines the valid extended error codes for the CompactFlash Storage Card Series product. The extended error code is returned to the host in the Error Register.

Extended Error	Description						
Code							
01h	Self Test OK						
09h	Miscellaneous Error						
20h	Invalid Command						
21h	Invalid Address						
2Fh	Address Overflow						
35h, 36h	Supply or generated Voltage Out of						
	Tolerance						
11h	Uncorrected ECC Error						
18h	Corrected ECC Error						
05h,30-34h, 37h, 3Eh	Self Test or Diagnostic Failed						
10h, 14h	ID Not Found						
3Ah	Spare Sectors Exhausted						
1Fh	Data Transfer Error/Aborted Command						
0Ch,	Corrupted Media Format						
38h,3Bh,3Ch,3Fh							
03h	Write/ Erase Failed						
22h	Power Level 1 Disabled						

Table 49: Extended Error Codes

5.16.16 Seek - 7XH

Register	7	6	5	4	3	2	1	0
Command(7)	7Xh							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-	·24)	
Cylinder	Cylinder High (LBA 23-16)							
High(5)								



Cylinder Low(4)	Cylinder Low (LBA 15-8)
Sector	X (LBA 7-0)
Number(3)	
Sector Count(2)	X
Feature(1)	X

This command is effectively a NOP command to the CompactFlash Storage Card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

5.16.17 Set Features – EFH

Register	7	6	5	4	3	2	1	0
Command(7)	EFh							
C/D/H(6)	Х			Drive	Х			
Cylinder	Х							
High(5)								
Cylinder Low(4)	Х							
Sector	Х							
Number(3)								
Sector Count(2)	Config							
Feature(1)	Feature	е						

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the CompactFlash Storage Card shall return command aborted. Table 50: Feature Supported defines all features that are supported.

Table	50:	Feature	Supported
		. catal c	Supporteu

Feature	Operation		
02h	Enable Write Cache.		
03h	Set transfer mode based on value in Sector Counter		
	register.		
55h	Disable Read Look Ahead.		
66h	Disable Power on Reset (POR) establishment of defaults at		
	Soft reset.		
82h	Disable Write cache.		
9Ah	Set the host current source capability. Allows tradeoff		
	between current drawn and read/write speed.		
AAh	Enable Read Look Ahead.		
BBh	4 Bytes of data apply on Read/Write Long commands.		
CCh	Enable Power on Reset (POR) establishment of defaults at		
	Soft Reset.		


If the Sector Count Register contains a valid value and the block count is supported, the value is loaded and execution is enabled for all subsequent Read Multiple and Write Multiple commands. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write multiple disabled.

Register	7	6	5	4	3	2	1	0				
Command(7)	99h or	99h or E6h										
C/D/H(6)	Х			Drive	X							
Cylinder	Х											
High(5)												
Cylinder Low(4)	Х											
Sector	Х											
Number(3)												
Sector Count(2)	Х											
Feature(1)	Х											

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds.

5.16.19 Standby - 96H or E2H

Register	7	6	5	4	3	2	1	0				
Command(7)	96h or	J6h or E2h										
C/D/H(6)	Х			Drive	x							
Cylinder	Х											
High(5)												
Cylinder Low(4)	Х											
Sector	Х											
Number(3)												
Sector Count(2)	Х											
Feature(1)	Х											

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, cleat BSY and return interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not



required).

5.16.20 Standby Immediate - 94H or E0H

Register	7	6	5	4	3	2	1	0				
Command(7)	94h or	94h or E0h										
C/D/H(6)	Х			Drive	X							
Cylinder	Х											
High(5)												
Cylinder Low(4)	Х											
Sector	Х											
Number(3)												
Sector Count(2)	Х											
Feature(1)	Х											

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

5.16.21 Write Buffer - E8H

Register	7	6	5	4	3	2	1	0
Command(7)	E8h							
C/D/H(6)	Х			Drive	Х			
Cylinder	Х							
High(5)								
Cylinder Low(4)	Х							
Sector	Х							
Number(3)								
Sector Count(2)	Х							
Feature(1)	Х							

The Write Buffer command enables the host to overwrite contents of the CompactFlash Storage Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfer 512 bytes.

5.16.22 Write DMA – CAH

Register	7	6	5	4	3	2	1	0			
Command(7)	CAh	CAh									
C/D/H(6)	1	1 LBA 1 Drive Head (LBA 27-24)									
Cylinder	Cylinde	Cylinder High (LBA 23-16)									
High(5)											

Cylinder Low(4)	Cylinder Low(LBA 15-8)
Sector	Sector Number (LBA 7-0)
Number(3)	
Sector Count(2)	Sector Count
Feature(1)	X

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The host then writes the (512*sector count) bytes of data to the Card using DMA. While DMAREQ is asserted by the Card, the host asserts –DMACK while it is ready to transfer data by DMA and asserts –IOWR once for each 16 bit word to be transferred from the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecovertable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The sector where the error occurred. The amount of data transferred is indeterminate. When a write DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

Register	7	6	5	4	3	2	1	0		
Command(7)	30h or	30h or 31h								
C/D/H(6)	1	LBA	1	Drive	Head(LBA 27-24)					
Cylinder	Cylinde	Cylinder High (LBA 23-16)								
High(5)										
Cylinder Low(4)	Cylinde	Cylinder Low (LBA 15-8)								
Sector	Sector	Numbe	r (LBA 7	'-0)						
Number(3)										
Sector Count(2)	Sector	Count								
Feature(1)	Х									

5.16.23 Write Sector(s) - 30H or 31H

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the CompactFlash Storage Card sets BST, then sets DRQ and clears BSDY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY shall be set and DRQ shall be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It shall remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

5.17 Device Parameters

iCF4000 device parameters are listed in Table 51.

			-		
Capacity	Cylinders	Heads	Sectors	Capacity(MB)	LBA
128MB	480	16	32	120	245760
256MB	984	16	32	246	503808
512MB	1001	16	63	492.68	1009008
1GB	2002	16	63	985.36	2018016
2GB	4003	16	63	1970.23	4035024
4GB	8006	16	63	3940.45	8070048
8GB	16000	16	63	7875	16128000

Table 51: Device parameters

6. Innodisk Part Number Rule

CODE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CODE	D	С	1	Μ	-	5	1	2	D	3	1	С	X	S	В	-	X
Description	Disk	CF	-400	0	-	Ca	рас	ity	Ca	atego	ory	Operation Temp.	Internal Control	СН		-	Customized Code
								D	efi	niti	on						
	Со	de	1 st ((Di	sk)						Со	de 13 th (Interna	al Co	ontr	ol C	ode)
D : Disk						1: 1	L st P	CB version,	default s	ettin	g						
Code	2 nd	~ 4	th (For	m l	Fac	tor)		3: F	Rem	ovable Mod	e +UltraD	MA			
C1M:CF, Type	e I, iCl	F 40	00							4: F	refo	ormat, Fixe	d Mode +	PIO	Mode	e 4	
C1S : CF Write	e Prote	ect								5:	Pre-1	formatted -	+ UltraDM	A 4			
										6: F	Pre-f	ormatted +	- Remova	ble +	-Ultra	aDMA	A 4
Co	de 6	th ~	8 th	(Ca	apa	city	/)			7: Fixed Mode + PIO Mode 4							
128:128MB										8: Fixed Mode + MwDMA Mode 2							
256:256MB										9: Removable Mode + PIO Mode 4							
512:512MB																	
01G:1GB										Code 14 th (Channel of data transfer)							
02G:2GB										S: Single Channel							
04G:4GB										D: Dual Channel							
08G:8GB																	
Co	de 9 ^t	^h ∼	11 ^t	th	(Se	erie	s)			Code 15 th							
D31:iCF 4000	0									в:	Tos	hiba SLC					
										T: I	Micr	on SLC					
Code 12	th (O	per	atio	on 1	Ten	ıpe	rat	ure)	Code 17 th							
C : Standard Grade (0 ~ +70 $^{\circ}$ C)						Cus	tom	ized code									
W : Industrial	Grade	e (-4	0 °C	~ -	+85	°C)				Customized function							