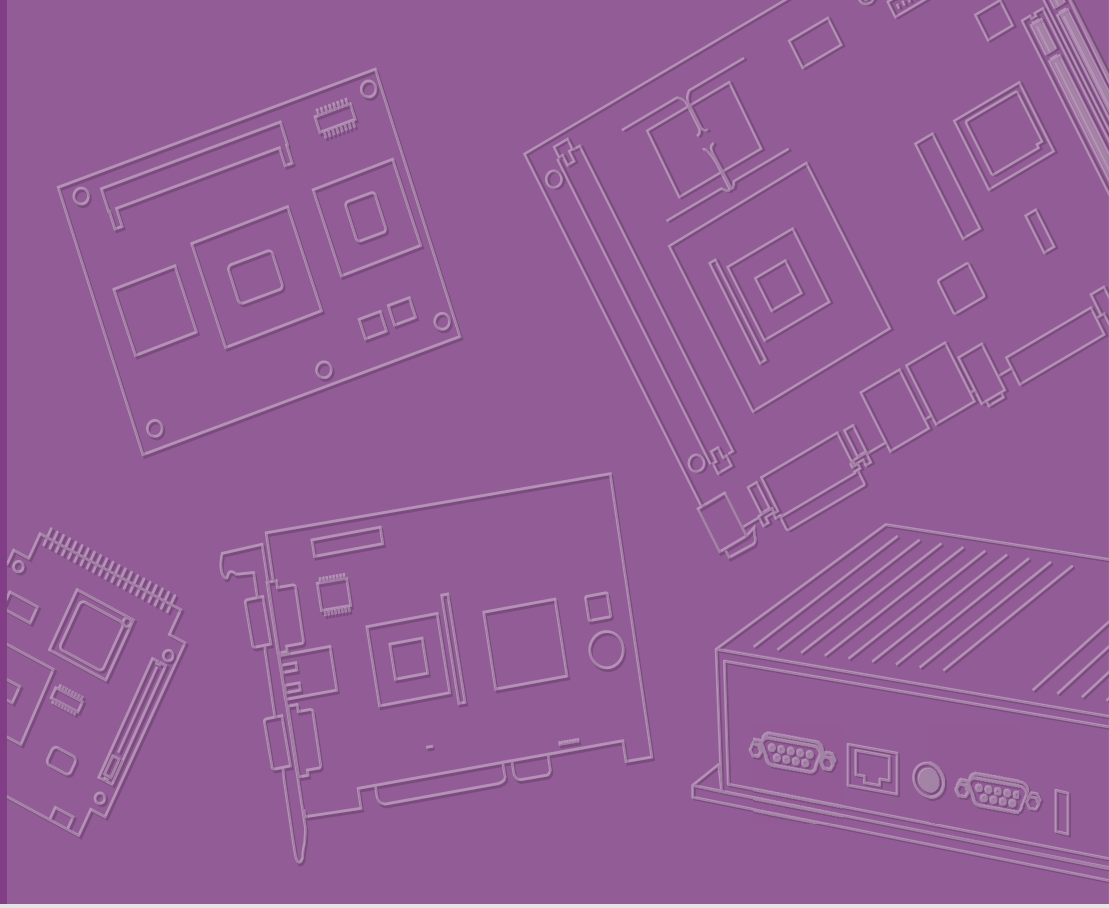

User Manual

SOM-C350

12th/13th Gen Intel® Core™ Processors (Alder Lake S/Raptor Lake S) COM-HPC Client Size C Module

ADVANTECH

Enabling an Intelligent Planet

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Acknowledgments

Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Part No. 2006C35002 Edition 3

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Declaration of Conformity

CE

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by Electrostatic Discharge (ESD) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class B

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FM

This equipment has passed the FM certification. According to the National Fire Protection Association, work sites are classified into different classes, divisions, and groups based on hazard considerations. This equipment is compliant with the specifications of Class I, Division 2, Groups A, B, C and D indoor hazards.

Technical Support and Assistance

1. Visit the Advantech website at http://support.advantech.com where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions, and Notes

Warning! *Warnings indicate conditions, which if not observed, can cause personal injury!*

Caution! *Cautions are included to help you avoid damaging hardware or losing data.*

There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

Note! *Notes provide optional additional information.*

Document Feedback

To assist us in making improvements to this manual, we would welcome comments and constructive criticism. Please send all such, in writing to: support@advantech.com

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- SOM-C350 CPU module
- 1 x heatspreader (1970005474T001)

Selection Guide w/ P/N

Part No.	CPU	Cores (P+E)	CPU TDP	CPU Threads	P-Cores Freq.	E-Cores Freq.	Graphic Execution Units	Temp
SOM-C350C9-RU3A1	i9-12900E	16C (8+8)	65W	24	2.3GHz/ 5.0GHz	1.7GHz/ 3.8GHz	32 EU	0 ~ 60 °C
SOM-C350C7-RU1A1	i7-12700E	12C (8+4)	65W	20	2.1GHz/ 4.8GHz	1.6GHz/ 3.6GHz	32 EU	0 ~ 60 °C
SOM-C350C5-RU9A1	i5-12500E	6C (6+0)	65W	12	2.9GHz/ 4.5GHz	NA	32 EU	0 ~ 60 °C
SOM-C350C3RH2A1	i3-12100E	4C (4+0)	60W	8	3.2GHz/ 4.2GHz	NA	24 EU	0 ~ 60 °C
SOM-C350PTRH6A1	G7400E	2C (2+0)	46W	4	3.6GHz	NA	16 EU	0 ~ 60 °C

P/N	CPU SKU	Cores (P+E)	CPU TDP	CPU Threads	P-Cores Freq.	E-Cores Freq.	Graphic Execution Units	Temp
SOM-C350RC9R-S8A1	i9-13900E	24C (8+16)	65W	32	1.8GHz/ 5.2GHz	1.3GHz/ 4.0GHz	32 EU	0~60°C
SOM-C350RC7R-U1A1	i7-13700E	16C (8+8)	65W	24	1.9GHz/ 5.1GHz	1.3GHz/ 3.9GHz	32 EU	0~60°C
SOM-C350RC5R-U4A1	i5-13500E	14C (6+8)	65W	24	2.4GHz/ 4.6GHz	1.5GHz/ 3.3GHz	24 EU	0~60°C
SOM-C350RC3R-H3A1	i3-13100E	4C (4+0)	65W	8	3.3GHz/ 4.4GHz	NA	24 EU	0~60°C

Packing list

Part No.	Description	Quantity
-	SOM-C350 COM module	1
1970005474T001	Heatspreader of SOM-C350	1

Development Board

P/N	96 BOM
SOM-DH3000-00A1	COM-HPC Development Board for Client Pinout with 5mm High Board to Board Connector (Alderlake-S)
SOM-DH3000R-00A1	COM-HPC Development Board for Client Pinout with 5mm High Board to Board Connector (Raptorlake-S)

Optional Accessories

Part No.	Description
1970005475T001	Semi-Cooler 120 x 120 x 34 mm
1970005473T001	QFCS 2.0 120 x 143 x 29 mm

Safety Instructions

1. Read these safety instructions carefully.
2. Keep this User Manual for later reference.
3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
5. Keep this equipment away from humidity.
6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. DO NOT COVER THE OPENINGS.
8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
12. Never pour any liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If one of the following situations arises, get the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated into the equipment.
    - The equipment has been exposed to moisture.
    - The equipment does not work well, or you cannot get it to work according to the user's manual.
    - The equipment has been dropped and damaged.
    - The equipment has obvious signs of breakage.
15. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -40 °C (-40 °F) OR ABOVE 85 °C (185 °F) . THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.
16. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.
17. The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

Acronyms

Term	Define
AC'97	Audio CODEC (Coder-Decoder)
ACPI	Advanced Configuration Power Interface – standard to implement power saving modes in PC-AT systems
BIOS	Basic Input Output System – firmware in PC-AT system that is used to initialize system components before handing control over to the operating system
CAN	Controller-area network (CAN or CAN-bus) is a vehicle bus standard designed to allow microcontrollers to communicate with each other within a vehicle without a host computer
DDI	Digital Display Interface – containing DisplayPort, HDMI/DVI, and SDVO
EAPI	Embedded Application Programmable Interface Software interface for COM Express® specific industrial function ■ System information ■ Watchdog timer ■ I2C Bus ■ Flat Panel brightness control ■ User storage area ■ GPIO
GbE	Gigabit Ethernet
GPIO	General purpose input output
HDA	Intel High Definition Audio (HD Audio) refers to the specification released by Intel in 2004 for delivering high definition audio that is capable of playing back more channels at higher quality than AC'97
I2C	Inter Integrated Circuit – 2 wire (clock and data) signaling scheme allowing communication between integrated circuit, primarily used to read and load register values
ME	Management Engine
PC-AT	"Personal Computer – Advanced Technology" – an IBM trademark term used to refer to Intel based personal computer in 1990s
PEG	PCI Express Graphics
RTC	Real Time Clock – battery backed circuit in PC-AT systems that keeps system time and date as well as certain system setup parameters
SPD	Serial Presence Detect – refers to serial EEPROM on DRAMs that has DRAM Module configuration information
TPM	Trusted Platform Module, chip to enhance the security features of a computer system
UEFI	Unified Extensible Firmware Interface
WDT	Watchdog Timer

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Chapter 1

General Information

This chapter details background information on the SOM-C350 CPU Computer on Module.

Sections include:

- Introduction
- Functional Block Diagram
- Product Specification

1.1 Introduction

The Advantech SOM-C350 is a cutting-edge COM-HPC Client Module that incorporates 12th Gen Intel® Core™ processors (Alder Lake-S) or 13th Gen Intel® Core™ processors (Raptor Lake-S) , delivering robust 16-core computing performance while operating within a 65Watt TDP envelope. This module is purpose-built for testing equipment and high-end medical applications, offering exceptional capabilities.

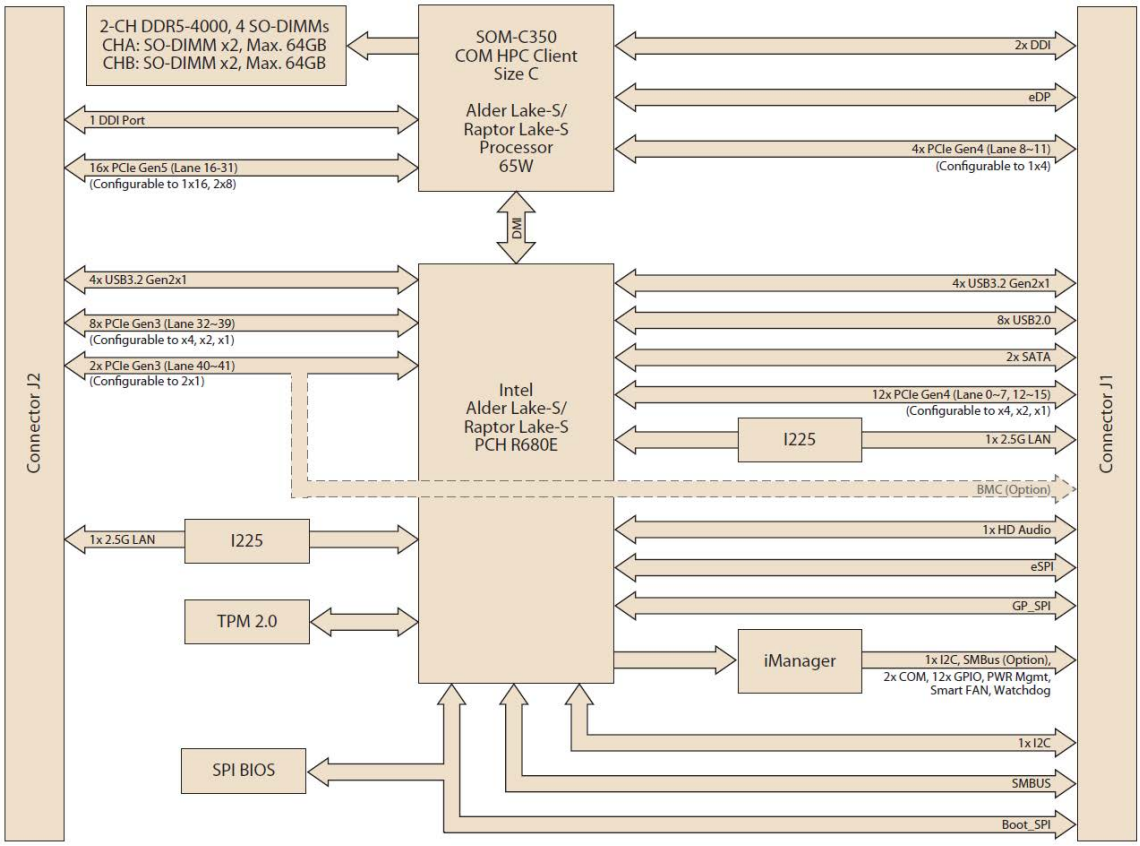
SOM-C350 is equipped with Intel Iris Xe graphics and comes pre-loaded with Advantech's comprehensive Edge AI Suite software toolkit, ensuring seamless integration into AI-driven applications. It is thoughtfully designed to support up to 128GB of DDR5 memory operating at 3600MHz, and it features a wide range of high-speed I/O interfaces, including PCIe Gen 5 (16GT/s), 2.5Gbase-T, and USB 3.2 Gen2 (10Gbps).

What sets the SOM-C350 apart is its ability to drive three independent 8K displays via DisplayPort 1.4/HDMI 2.1, in addition to offering an eDP interface and three DDI interfaces. Furthermore, it can be configured to handle two 8K HDR outputs simultaneously, making it a standout solution for graphics-intensive applications.

With an on-board TPM2.0 for enhanced security, a 12V power input, and the ability to operate within a wide temperature range of 0 to 60°C (thanks to the inclusion of a heat spreader and QFCS), the SOM-C350 is both reliable and versatile.

To cater to a variety of requirements, Advantech has integrated its iManager (SUSI 4) software, which offers support for multi-level watchdog timers, voltage and temperature monitoring, thermal protection and mitigation, LCD backlight control, and embed-ded storage management. It's worth noting that all Advantech COM-HPC modules come with iManager and WISE-PaaS/RMM for comprehensive functionality and management capabilities.

1.2 Functional Block Diagram



1.3 Product Specifications

1.3.1 Compliance

- PICMG COM-HPC Revision 1.10
- Dimension: 160 x 120 mm (6.29 x 4.7 in)
- Pin-out Client Type compatible

1.3.2 Feature List

Table 1.1: Feature List

Feature Type	Connector	Feature	COM HPC Define		SOM-C350
			Max.	Min.	
Display	J1	eDP	1	0	1
	J1	DDI0	1	0	1
	J1	DDI1	1	0	1
	J2	DDI2	1	0	1
Expansion	J1	PCI Express x1	16	0	16
	J2	PCI Express x1	32	0	26

Serial	J1	SMBus	1	0	1
	J1	I^2C Bus	2	0	2
	J1	IPMB	1	0	0
	J1	UART	2	0	2
I/O	J1-J2	NBASE-T (max. 10G)	2	0	2
	J2	ETH KR (max 25G)	2	0	0
	J2	ETH KR CEI	1	0	0
	J1	USB 2.0	8	0	8
	J1-J2	USB 3.2 Gen 2x2 (Optional BIOS)	4	0	4
	J1	USB C PD I2C	1	0	1
	J1	Soundwire/DMIC	2	0	1
	J1	I2S/2xSNDW	1	0	1
	J1	HD Audio	1	0	1
	J1	SATA	2	0	1
	J1	eSPI	1	0	1
	J1	BOOT_SPI	1	0	1
	J1	GP_SPI	1	0	1
	J1	GPIO	12	0	12
	J1	MISC	1	0	0
	J1	Functional Safety	1	0	0
	J1	Fan PWM/Tachometer	2	0	2
	J1	Trusted Platform Modules	1	0	1
PowerI	J1-J2	Power	28	0	28
	J1-J2	Standby Power	2	0	2
	J1-J2	GND	207	0	207
	J1	RSVD	30	0	23

1.3.3 Processor System

Table 1.2:

CPU	Cores (P+E)	P-Cores Base/ Max Freq.	E-Cores Base/ Max Freq.	Cache (MB)	TDP(W)
i9-12900E	16C (8+8)	2.3GHz/5.0GHz	1.7GHz/3.8GHz	14	65W
i7-12700E	12 (8+4)	2.1GHz/4.8GHz	1.6GHz/3.6GHz	12	65W
i5-12500E	6 (6+0)	2.9GHz/4.5GHz	NA	7.5	65W
i3-12100E	4 (4+0)	3.2GHz/4.2GHz	NA	5	60W
G7400E	2 (2+0)	3.6GHz	NA	2.5	46W

Table 1.3:

CPU SKU	Cores (P+E)	P-Cores Base/ Max Freq.	E-Cores Base/ Max Freq.	Cache (MB)	CPU TDP
i9-13900E	24C (8+16)	1.8GHz/5.2GHz	1.3GHz/4.0GHz	36	65W
i7-13700E	16C (8+8)	1.9GHz/5.1GHz	1.3GHz/3.9GHz	30	65W
i5-13500E	14C (6+8)	2.4GHz/4.6GHz	1.5GHz/3.3GHz	24	65W
i3-13100E	4C (4+0)	3.3GHz/4.4GHz	NA	12	65W

1.3.4 Memory

There are a total of 4 memory sockets on SOM-C350, two on the top side by default and two on the bottom side. These support 128GB max capacity with 262pin SO-DIMM sockets (dual-channel).

1.3.5 Graphics/Audio

Graphics Core: 12th gen Intel Iris Xe Graphics Core supports DX12, OGL4.5, OCL2.1, and MPEG2, HEVC/AVC/VP9/SCC HW decode/encode/transcode acceleration.

Table 1.4:

CPU	Graphic Core	Base Freq.	Max Freq.
i9-12900E	Gen12 Iris Xe Graphic	300	1550
i7-12700E	Gen12 Iris Xe Graphic	300	1500
i5-12500E	Gen12 Iris Xe Graphic	300	1450
i3-12100E	Gen12 Iris Xe Graphic	300	1400
G7400E	Gen12 Iris Xe Graphic	300	1350

Table 1.5:

CPU SKU	Graphic Core	Base Freq.	Max Freq.
i9-13900E	Intel® UHD Graphics 770	300	1650
i7-13700E	Intel® UHD Graphics 770	300	1600
i5-13500E	Intel® UHD Graphics 770	300	1550
i3-13100E	Intel® UHD Graphics 730	300	1500

1.3.6 Expansion Interfaces

- **PCIe Gen5**

Up to 16 PCI Express Lanes: Supports default 1 Port PCIe x16 compliant to PCIe Gen5 (32.0 GT/s) specifications, configurable to 1 PCIe x16 or 2 PCIe x8. The configurable combinations may need BIOS modification. Please contact the Advantech sales or FAE for more details.

- **PCIe Gen4 (CPU)**

Up to 4 PCI Express Lanes: Supports default 1 ports PCIe x4 compliant to PCIe Gen4 (16.0 GT/s) specifications, configurable only to PCIe x4.

- **PCIe Gen4 (PCH)**

Up to 12 PCI Express Lanes: Supports default 3 PCIe x4 compliant to PCIe Gen4 (16.0 GT/s) specifications, configurable to PCIe x4 or PCIe x2 or PCIe x1. Several configurable combinations may need BIOS modification. Please contact the Advantech sales or FAE for more details.

- **PCIe Gen3**

Up to 10 PCI Express Lanes: Supports default 2 PCIe x2, 1 PCIe x4, 2 PCIe x1 compliant to PCIe Gen3 (8.0 GT/s) specifications, configurable to PCIe x4 or PCIe x2 or PCIe x1. Several configurable combinations may need BIOS modification. Please contact the Advantech sales or FAE for more details.

Table 1.6:																
Client Type	**Primary J1**															
PCIe Lane	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15
Default	X4				X4				NVME0 or GP x4				X4			
Option 1	X2		X2		X2		X2		NA				X2		X2	
Option 2	X2		x1	x1	X2		x1	x1	NA				X2		x1	x1
Option 3	x1	x1	x1	x1	x1	x1	x1	x1	NA				x1	x1	x1	x1

Table 1.7:																
Client Type	**Primary J2**															
PCIe Lane	P16	P17	P18	P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31
Default	Hi BW Link x16															
Option 1	Hi BW Link x8								Hi BW Link x8							

Table 1.8:										
Client Type	**Primary J2**									
PCIe Lane	P32	P33	P34	P35	P36	P37	P38	P39	P40	P41
Default	X2		X2		x4				x1	x1
Option 1	x4				X2		X2		NA	NA
Option 2	X2		x1	x1	X2		x1	x1	NA	NA
Option 3	x1	x1	x1	x1	x1	x1	x1	x1	NA	

1.3.7 Serial Bus

- **SMBus**
  Support SMBus 2.0 specification.
- **I²C Bus**
  Supports I²C bus 7-bit and 10-bit address modes. Support standard mode up to 100 Kb/s, fast mode up to 400 Kb/s.

1.3.8 I/O

- **Gigabit Ethernet**
  Ethernet: Intel I225 Gigabit LAN supports 10/100/1000 Mbps & 2.5 Gbps Speed.
- **SATA**
  Supports 2 ports SATA Gen3 (6.0 Gb/s), backward compliant to SATA Gen2 (3.0 Gb/s) and Gen1 (1.5 Gb/s). The maximum data rate is 600 MB/s. Supports AHCI 1.3.1 mode (does not support IDE mode).
- **USB 3.2/USB 2.0**
  COM-HPC supports USB 3.2 but SOM-C350 supports 8 USB 3.2 Gen2 (10 Gbps) ports and 8 USB 2.0 (480 Mbps) ports. For USB 3.2, the product supports LPM (U0, U1, U2, and U3) for power efficiency.
  For USB 3.2 Gen2x2, it needs BIOS modification. Please contact the Advantech sales or FAE for more details.
  Notice: Advantech strongly recommends using a certificated cable to maximize USB 3.2 gen2 performance.

- **USB 3.2**

Table 1.9: USB 3.2

Client Type	P00	P01	P10	P11	P20	P21	P30	P31
SoC	P1	P2	P3	P4	P7	P8	P9	P10
Client Type	OC_01		OC_23		OC_45		OC_67	
SoC USB_OC#	OC_01		OC_23		OC_45		OC_67	

- **USB 2.0**

Table 1.10: USB 2.0

Client Type	P00	P01	P02	P03	P04	P05	P06	P07
SoC	P1	P2	P3	P4	P5	P6	P7	P8
Client Type	OC_01		OC_23		OC_45		OC_67	
SoC USB_OC#	OC_01		OC_23		OC_45		OC_67	

- **SPI Bus**

  Supports BIOS flash only. SPI clock can be 50MHz, with a capacity up to 256Mb.

- **GPIO**

  12 programmable general purpose Input or output (GPIO).

- **Watchdog**

  Supports multi-level watchdog time-out output. Provides 1-65535 level, from 100ms to 109.22 minute intervals.

- **Serial port**

  2 x 2-wire serial port (Tx/Rx) supports 16550 UART compliance.

  – Programmable FIFO or character mode
  – 16-byte FIFO buffer on transmitter and receiver in FIFO mode
  – Programmable serial-interface characteristics: 5, 6, 7, or 8-bit character
  – Even, odd, or no parity bit selectable
  – 1, 1.5, or 2 stop bit selectable
  – Baud rate up to 115.2K

- **TPM**

  Supports optional TPM 2.0 module.

- **Smart Fan**

  Supports 1 Fan PWM control signals and 1 tachometer input for fan speed detection. Provides 1 on module with connector and the other to the carrier board following PICMG COM HPC R1.10 specifications.

- **BIOS**

  The BIOS chip is on module by default. Users can place BIOS chip on the carrier board with appropriate design and jumper setting in BSEL#[2:0]

Table 1.11:

BSEL #2	BSEL #1	BSEL S#0	Boot up destination/function
NA	NA	Open	Boot from Module's SPI BIOS
NA	NA	GND	Boot from Carrier SPI BIOS

Note! *If system COMS is cleared, strongly suggest to go BIOS setup menu and load default setting at the first time boot up.*

The standard module has no jumper at SCN2, so BIOS settings are kept without a RTC coin battery, if you need to restore the BIOS to default settings, follow the steps below:

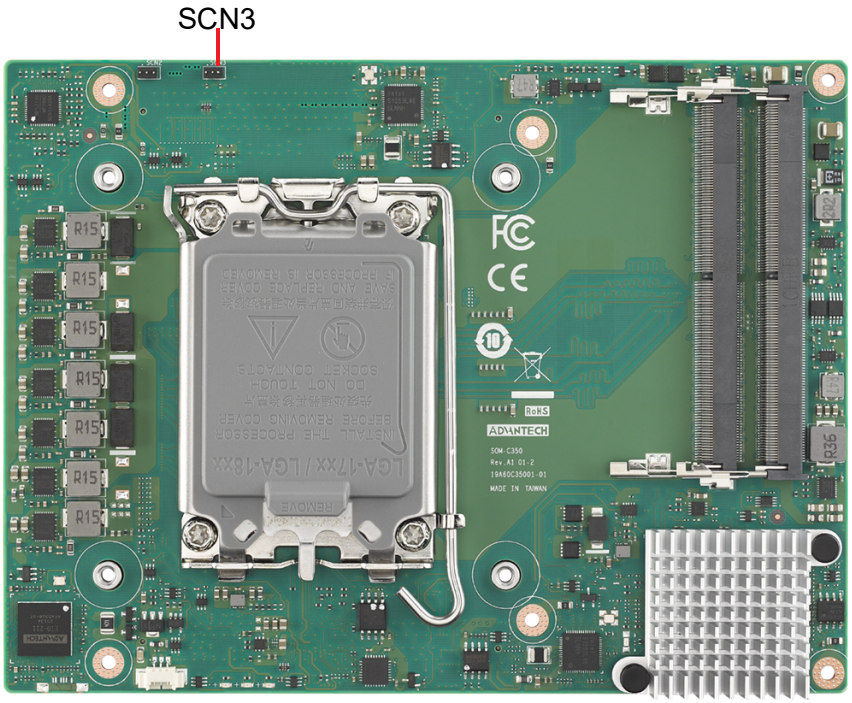
Table 1.12:

Pin	Function
2	N/A [Default]
2-3	BIOS Clear_CMOS load default setting

Reserved

or

BIOS Default Settings



1. Remove the coin battery
2. Put jumper on SCN3 pin2-3
3. Turn on power supply
4. The system will boot up a few times
5. The BIOS will load default setting successfully

1.3.9 Power Management

- **Power Supply**

Supports both ATX and AT power modes. VSB is for suspended power and can be optional if not required by standby (suspend-to-RAM) support. RTC battery may be optional if date/timekeeping is not required.

- Vin: 12V +/- 5%
- VSB: 5V +/- 5% (Suspend power)
- RTC Battery Power: 2.0V - 3.3V

- **PWROK**

  Power-good from the main power supply. A high value indicates the power level is good. This signal can be used to postpone module startup allowing Carrier-based FPGAs or other configurable devices time to be programmed.

- **Power Sequence**

  According to PICMG COM Express R1.10 specification.

- **Wake Event**

  Various wake event support allows users to apply different scenarios.
  - Wake-on-LAN(WOL): Wake to S0 from S3/S4/S5
  - USB Wake: Wake to S0 from S3
  - PCIe Device Wake: depends on user inquiry and may need customized BIOS

1.3.10 Advantech S5 ECO Mode (Deep Sleep Mode)

Advantech iManager provides additional features allowing the system to enter a very low suspended power mode - S5 ECO mode. In this mode, the module will cut all power, including suspended and active power to the chipset, and keep an on-module controller active. Only power under 50MW will be consumed, meaning user battery packs can last longer. While this mode is enabled in the BIOS, the system (or module) only allows power button boot instead of other methods such as WOL.

1.3.11 Environmental Specifications

- **Temperature**
  - Operating: 0 ~ 60 °C (32 ~ 140 °F)
  - Storage: -40 ~ 85 °C (-40 ~ 185 °F)
- **Humidity**
  - Operating: 40 °C @ 95% relative humidity, non-condensing
  - Storage: 60 °C @ 95% relative humidity, non-condensing
- **Vibrations**

  IEC60068-2-64: Random vibration test under non-operation mode, 3.5 Grms. For operation, Please contact the Advantech sales or FAE for more details

- **Drop Test (Shock)**

  Federal Standard 101 Method 5007 test procedure with standard packing

- **EMC**

  CE EN55032 Class B and FCC Certifications: validate with standard development boards in Advantech chassis

1.3.12 MTBF

Please refer Advantech SOM-C350 Refresh Series Reliability Prediction report on the website: Link: http://com.advantech.com

1.3.13 OS Support

The mission of Advantech Embedded Software Services is to "Enhance the quality of life with Advantech platforms and Microsoft Windows Embedded technology." We enable Windows Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from

the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows Embedded software solutions easily and widely available to the embedded computing community.

To install drivers, please connect to the website http://support.advantech.com.tw to download the setup file.

1.3.14 Advantech iManager

Supports APIs for GPIO, smart fan control, multi-stage watchdog timer, temperature sensor, and hardware monitoring. Follows PICMG EAPI 1.0 specifications with backward compatibility.

1.3.15 Power Consumption

Table 1.13: Power Consumption Table (Watt.)

VCC=12V, VSB=5V	Active Power Domain			Suspend Power Domain		Mechanical off
Power State	S0 Max. Load	S0 Burn-in	S0 Idle	S5	S5 Deep Sleep	RTC (uA)
SOM-C350C9R-U3A1	231.2	88.77	12.64	1.322	0.33	5.34

- **Hardware Configuration:**
  1. MB: SOM-C350C9R-U3A1
  2. DRAM: 32GB DDR5 3200MHz x 4pcs
  3. Carrier board: SOM-DH3000-00A1
- **Test Conditions:**
  1. Test temperature: room temperature (about 25 °C)
  2. Test voltage: rated voltage DC +12V
  3. Test loading:
     - Maximum load mode: According to Intel thermal/power test tools.
     - Burn-in mode: Burn-in test V8.1 Pro (1023) for 64-bit Windows. (CPU, RAM, 2D&3D Graphics, and Disk with 100%)
     - Idle mode: DUT power management off and not running any program.

1.3.16 Performance

To compare performance or benchmark data with other modules, please refer to the “Advantech COM Performance & Power Consumption Table.”

1.3.17 Pin Description

Advantech provides useful checklists for schematic design and layout routing. The schematic checklist will specify details about each pin’s electrical properties and how to connect them in different scenarios. The layout checklist will specify the layout constraints and recommendations for trace length, impedance, and other necessary information during design.

Please contact your nearest Advantech branch office or call for getting the design documents and further advance supports.

Chapter 2

Mechanical Information

This chapter details mechanical information on the SOM-C350 CPU Computer on Module.

Sections include:

- Board Information
- Mechanical Diagram
- Assembly Diagram

2.1 Board Information

The figures below indicate the main chips on SOM-C350 Computer-on-Module. Please be aware of these positions while designing your own carrier board to avoid mechanical issues and ensure thermal solution contact points for best thermal dissipation performance.

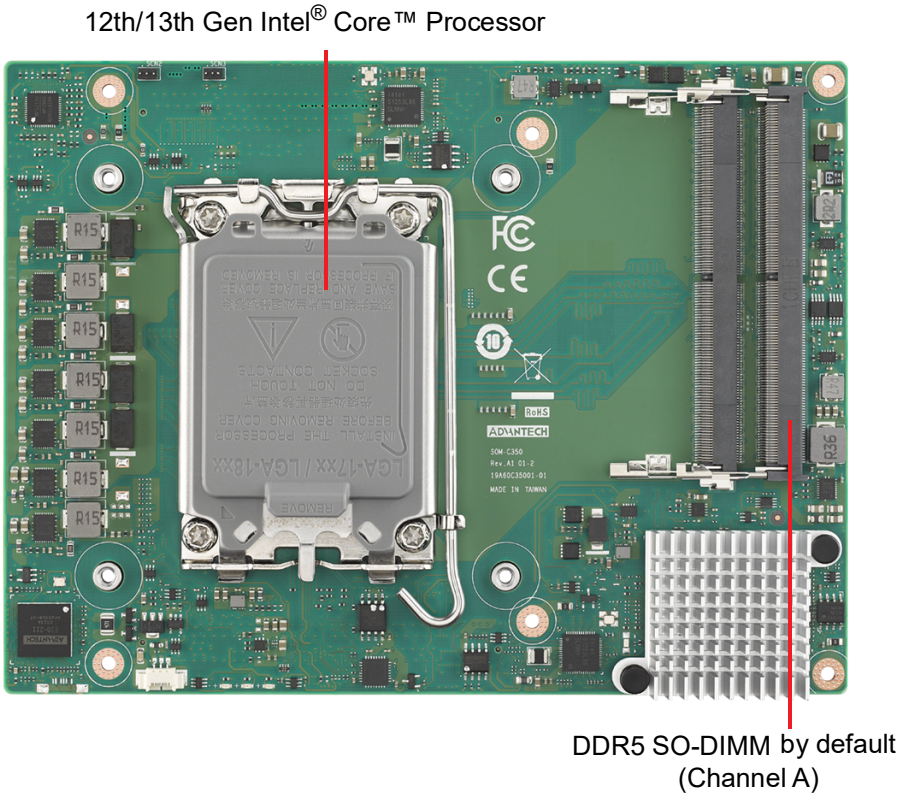


Figure 2.1 Board Chips ID - Front

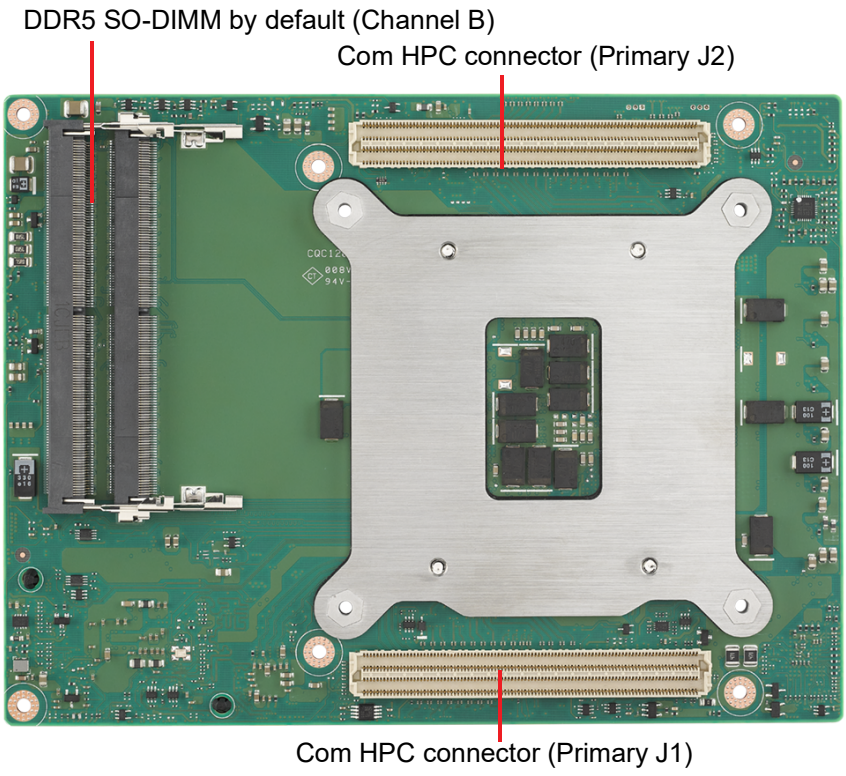


Figure 2.2 Board Chips ID - Rear

2.2 Mechanical Diagrams

For more details about 2D/3D models, please find on Advantech COM support service website http://com.advantech.com.

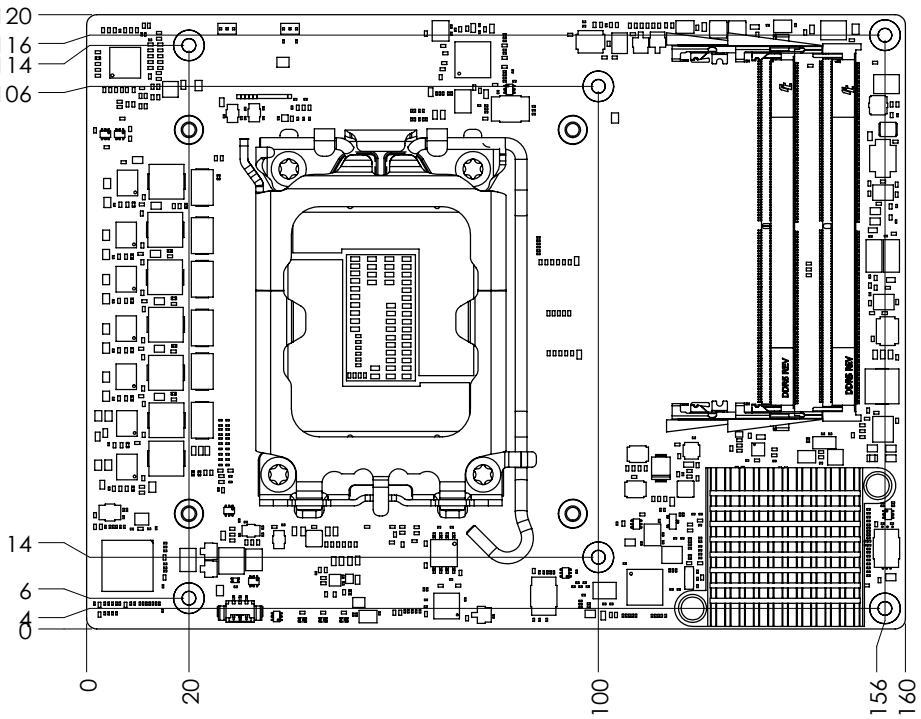


Figure 2.3 Board Mechanical Diagram - Front

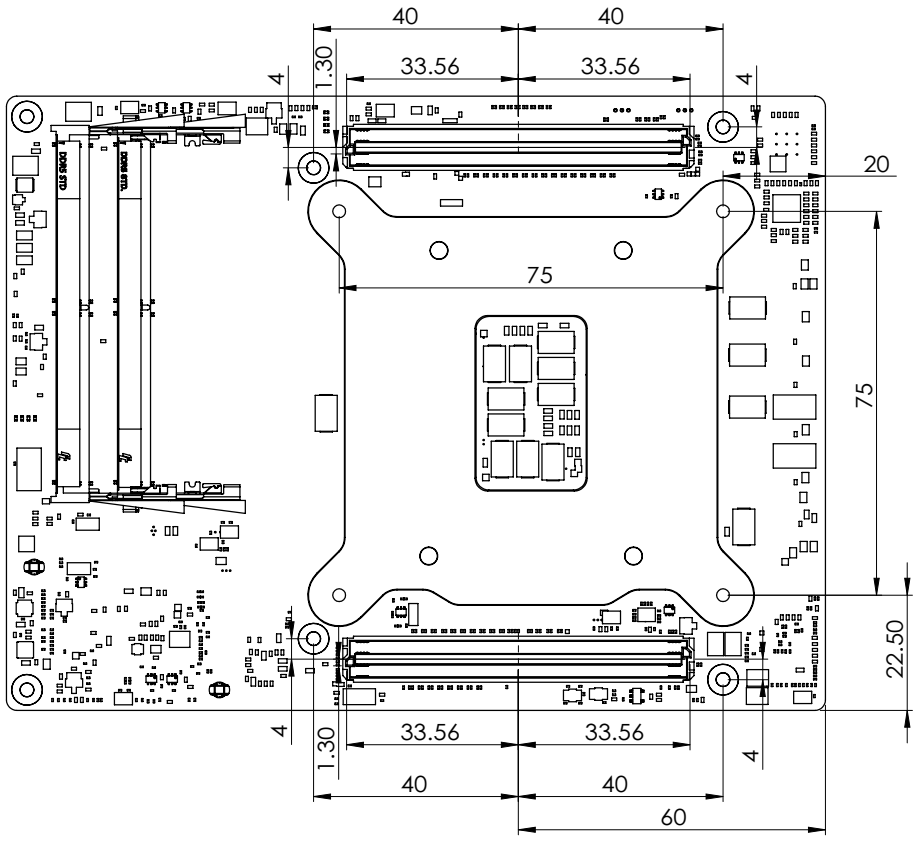


Figure 2.4 Board Mechanical Diagram - Rear

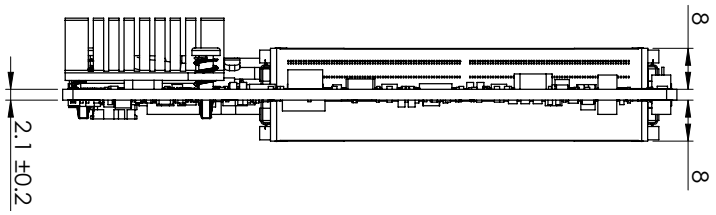


Figure 2.5 Board Mechanical Diagram - Side

2.3 Assembly Diagrams

These figures demonstrate the assembly order from the thermal module, to the COM module, to the carrier board.

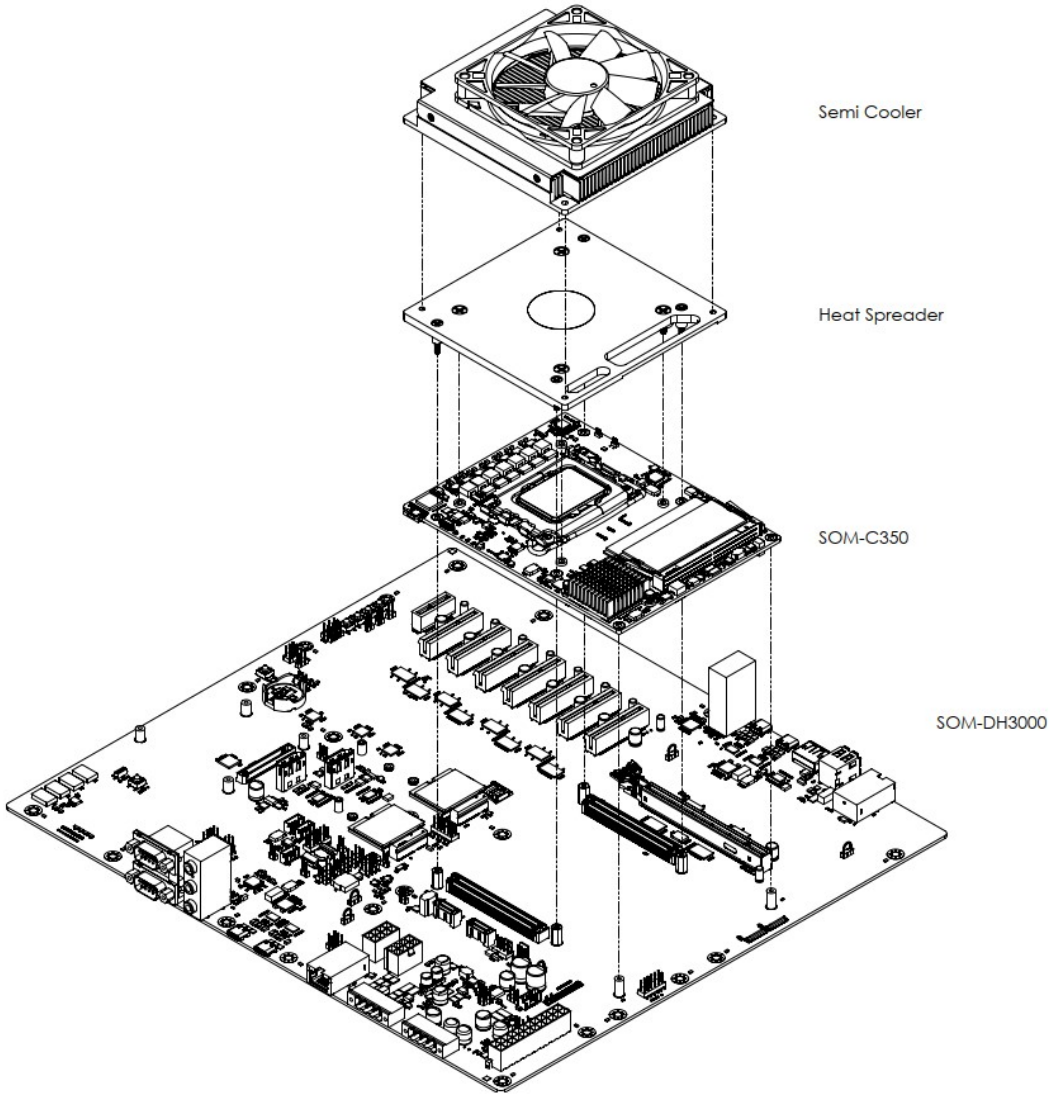


Figure 2.6 Assembly Diagram

There are 6 reserved screw holes for SOM-C350 to be pre-assembled with heat spreader.

2.4 Assembly Diagrams

Since the COM-HPC board-to-board connector consists of 400 pins per connector, it is essential to vertically align the module and carrier board during assembly. Please adhere to the recommended orientation, as illustrated in the provided figures, to prevent any potential damage to the board-to-board connector.

2.4.1 Allowable Initial Angular Misalignment

Mating Angle Requirements:

TABLE 1	
ROW	"A"=DEG
4	9.05
6	5.84
8	4.63
10	3.56
16	2.22

TABLE 2			
NO OF POS	"B"=DEG	NO OF POS	"B"=DEG
10	11.97	60	2.37
20	6.88	70	2.00
30	4.82	80	1.71
40	3.63	90	1.49
50	2.88	100	1.31

TABLE 3			
NO OF POS	"C"=DEG	NO OF POS	"C"=DEG
10	3.69	60	1.46
20	2.82	70	1.30
30	2.29	80	1.17
40	1.92	90	1.07
50	1.66	100	0.98

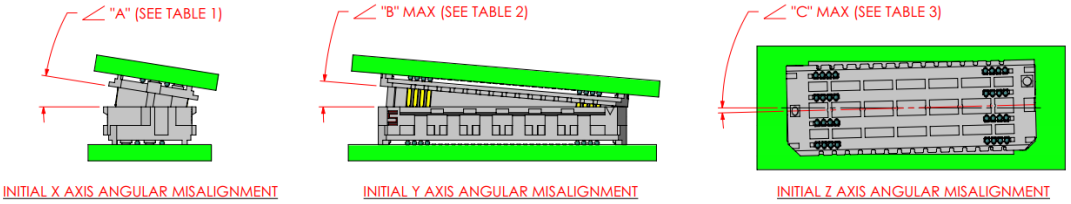


Figure 2.7 Initial Angular Misalignment

2.4.2 Allowable Final Angular Misalignment

TABLE 4	
ROW	"D"=DEG
4	3.95
6	2.56
8	1.89
10	1.50
16	0.92

TABLE 5			
NO OF POS	"E"=DEG	NO OF POS	"E"=DEG
10	3.30	60	0.79
20	2.02	70	0.69
30	1.46	80	0.61
40	1.14	90	0.54
50	0.93	100	0.49

TABLE 6			
NO OF POS	"F"=DEG	NO OF POS	"F"=DEG
10	1.12	60	0.27
20	0.69	70	0.23
30	0.50	80	0.21
40	0.39	90	0.19
50	0.32	100	0.17

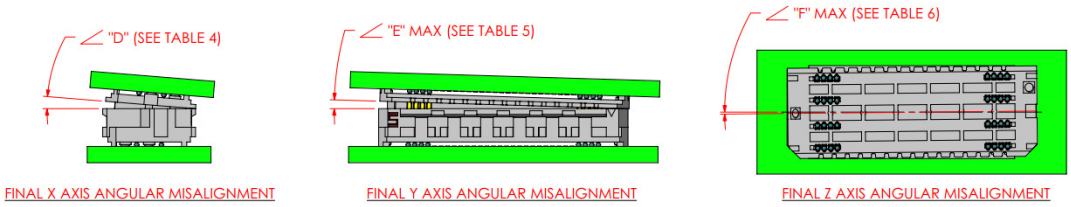


Figure 2.8 Final Angular Misalignment

2.5 CPU Package Design

Please consider the CPU and chip height tolerance when designing your thermal solution.

Table 2.1: CPU and CPU Socket Height and Tolerance

Item	LGA 1700
IHS to MB Height (validated range)	6.529 ~ 7.532 mm

Chapter 3

BIOS Operation

This chapter details BIOS setup information for the SOM-C350 CPU Computer on Module.

Sections include:

- Introduction
- Entering Setup
- Hot / Operation Key
- Exit BIOS Setup Utility

3.1 Introduction

AMI BIOS has been a staple in motherboards for more than a decade. Through the AMI BIOS Setup Utility, users gain the ability to customize BIOS settings and manage a range of system features. This section provides an overview of how to navigate the BIOS Setup Utility for fundamental configuration.

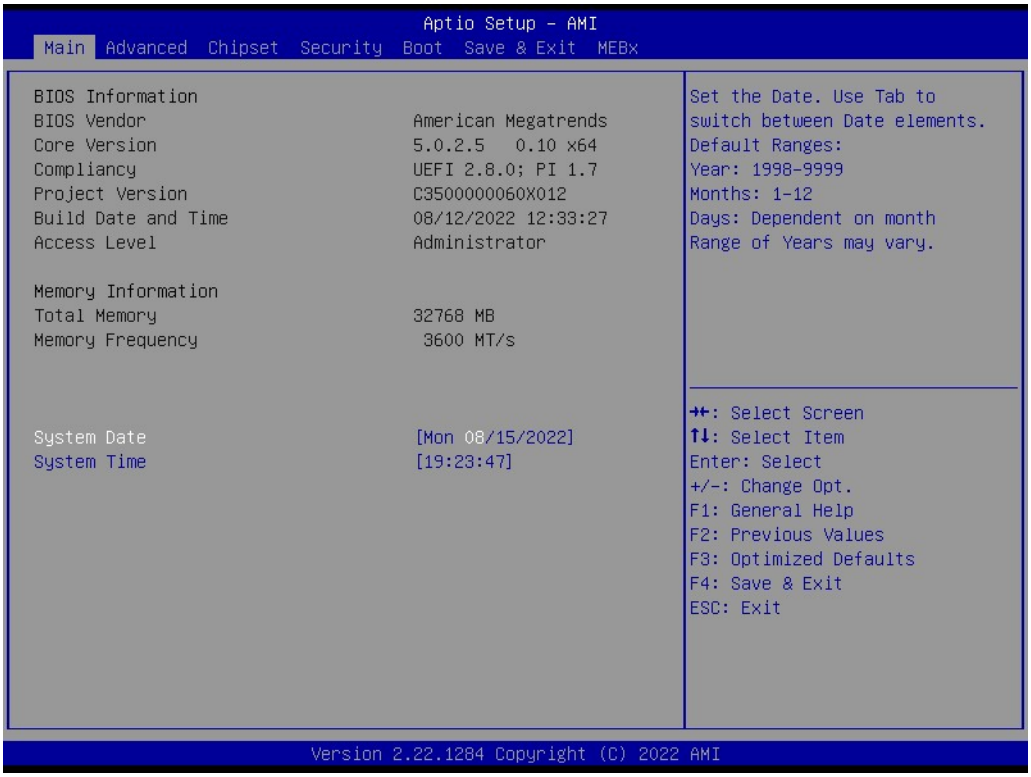


Figure 3.1 Setup Program Initial Screen

AMI's BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in flash ROM so it retains the Setup information when the power is turned off.

3.2 Entering Setup

Turn on the computer and then press <DEL> or <ESC> to enter the Setup menu.

3.2.1 Main Setup

When users first enter the BIOS Setup Utility, users will enter the Main setup screen. Users can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.

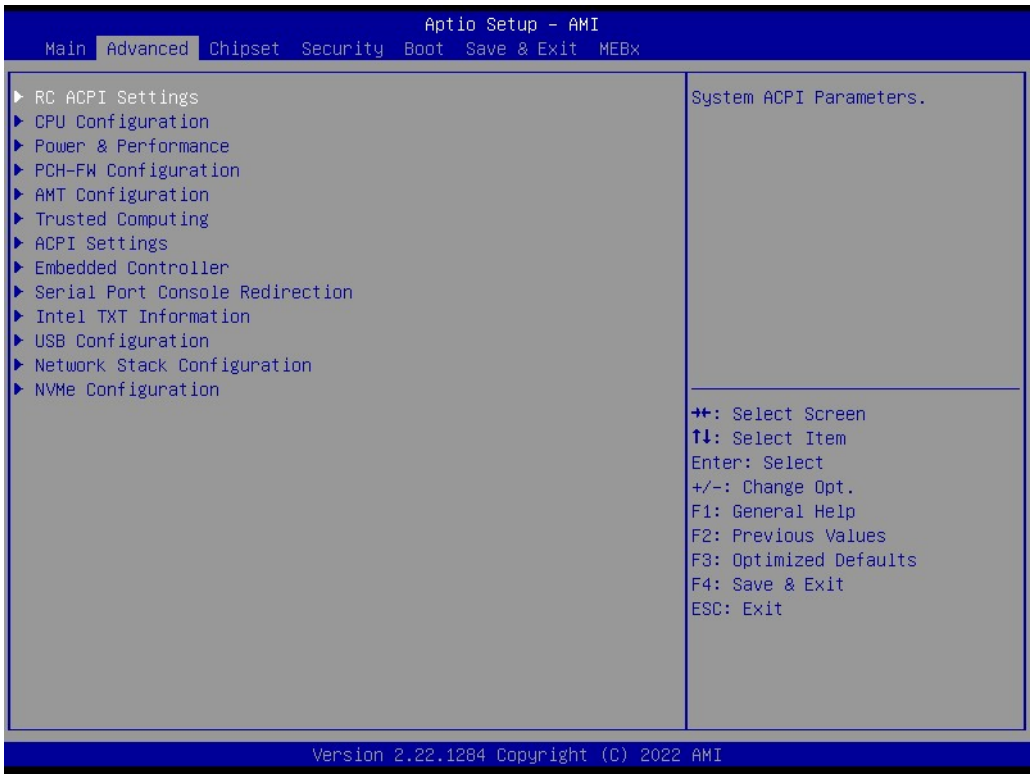


Figure 3.2 Main setup screen

The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

- **System time/System date**

  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM: SS format.

3.2.2 Advanced BIOS Features Setup

Select the Advanced tab from the SOM-C350 setup screen to enter the Advanced BIOS Setup screen. Users can select any item in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. Users can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screens are shown below. The sub menus are described on the following pages.

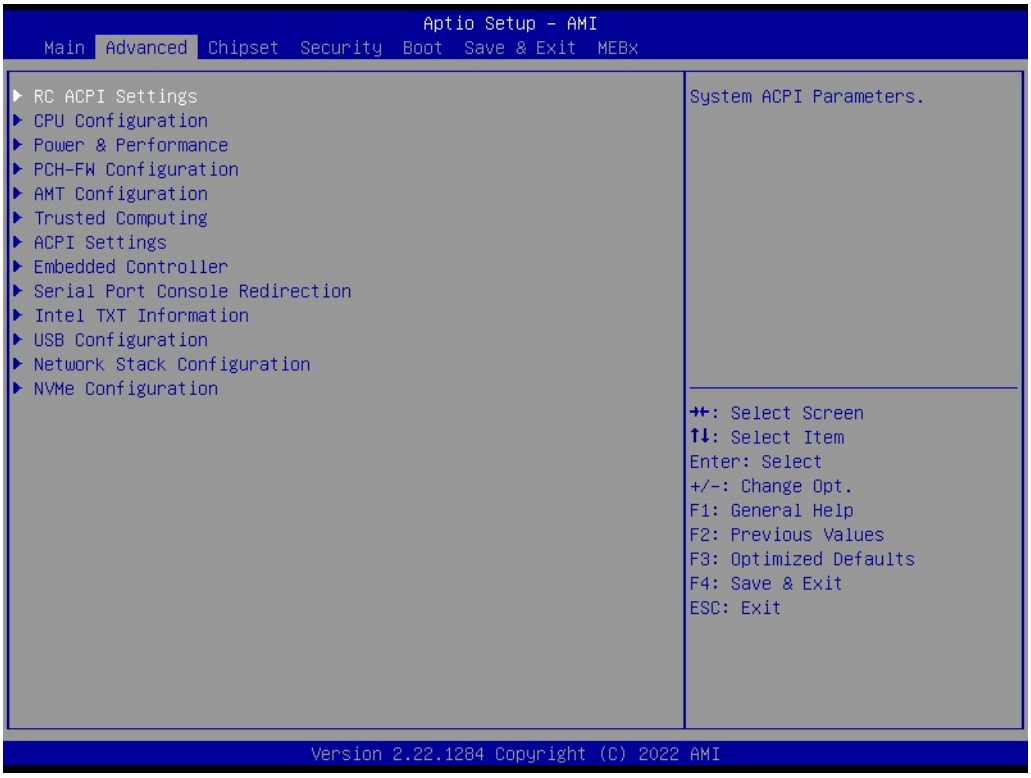


Figure 3.3 Advanced BIOS features setup screen

- **RC ACPI Settings**
  System ACPI Parameters.
- **CPU Configuration**
  CPU Configuration Parameters.
- **Power & Performance**
  Power & Performance Options.
- **PCH-FW Configuration**
  Configure Management Engine Technology Parameters.
- **AMT Configuration**
  Configure Intel(R) Active Management Technology Parameters.
- **Trusted Computing**
  Trusted Computing Settings.
- **ACPI Settings**
  ACPI Sleep State.
- **Embedded Controller**
  Embedded Controller Parameters.
- **Serial Port Console Redirection**
  Console Redirection Settings.

- **Intel TXT Information**
  Display Intel TXT information.
- **USB Configuration**
  USB Configuration Parameters.
- **Network Stack Configuration**
  Network Stack Settings.
- **NVMe Configuration**
  NVMe controller and driver information.

3.2.2.1 RC ACPI Settings

Figure 3.4 RC ACPI Settings

- **Low Power S0 Idle Capability**
  This variable determines if we enable ACPI Lower Power S0 Idle Capability (Mutually exclusive with Smart connect). While this is enabled, it also disables 8254 timer for SLP_S0 support.

3.2.2.2 Active Performance-cores

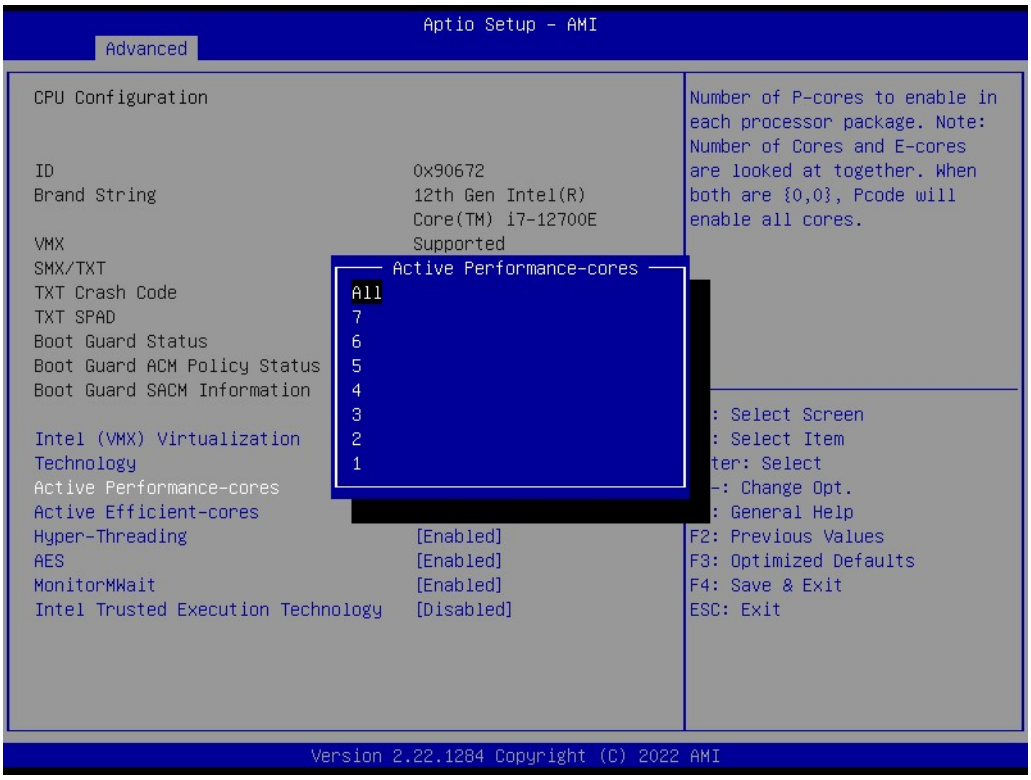


Figure 3.5 Active Performance-cores

- **Active Performance-cores**
  Number of P-cores to enable in processor package. Note: Number of Cores and E-cores are locked at together. When both are {0,0}, Pcode will enable all cores.

3.2.2.3 Active Efficient-cores

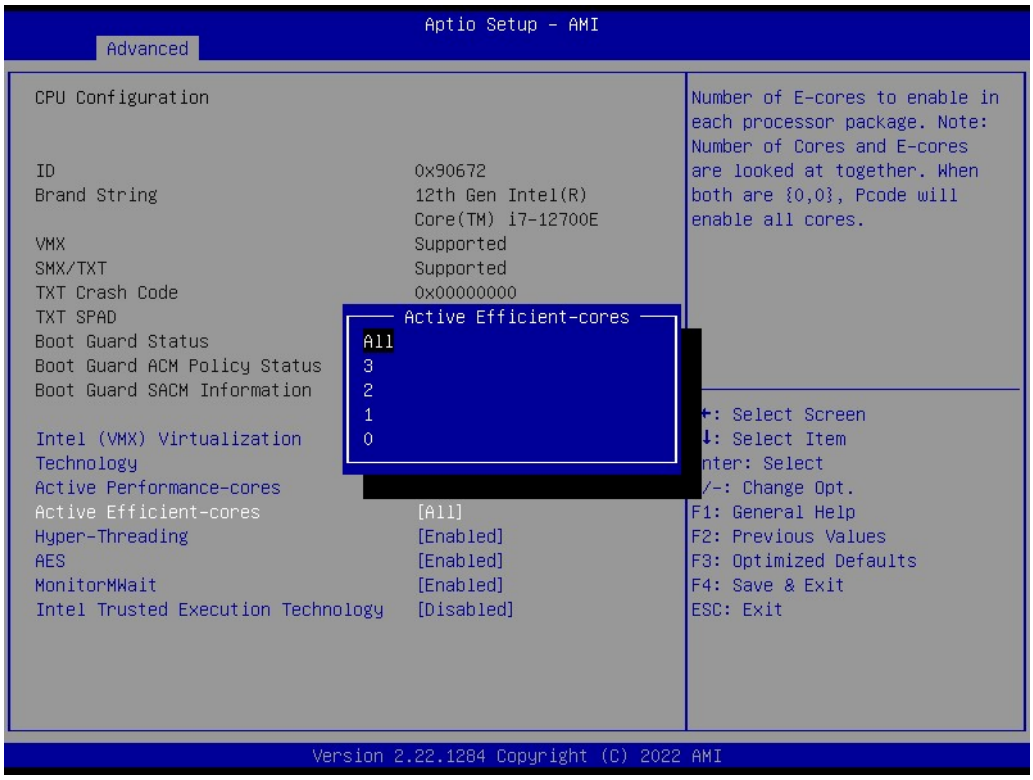


Figure 3.6 Active Efficient-cores

- **Active Efficient-cores**
  Number of E-cores to enable in each processor package. Note: Number of Cores and E-cores are locked at together. When both are {0,0}, Pcode will enable all cores.
- **Hyper-Threading**
  Enable or Disable Hyper-Threading Technology.
- **AES**
  Enable/Disable AES (Advanced Encryption Standard).
- **MonitorMwait**
  Enable/Disable Monitor Mwait.
- **Intel Trusted Execution Technology**
  Enables utilization of additional hardware capabilities provided by Intel (R) Trusted Execution Technology.

3.2.2.4 Power & Performance

Figure 3.7 Power & Performance

- **CPU - Power Management Control**
  CPU - Power Management Control Options.
- **GT - Power Management Control**
  GT - Power Management Control Options.

CPU - Power Management Control

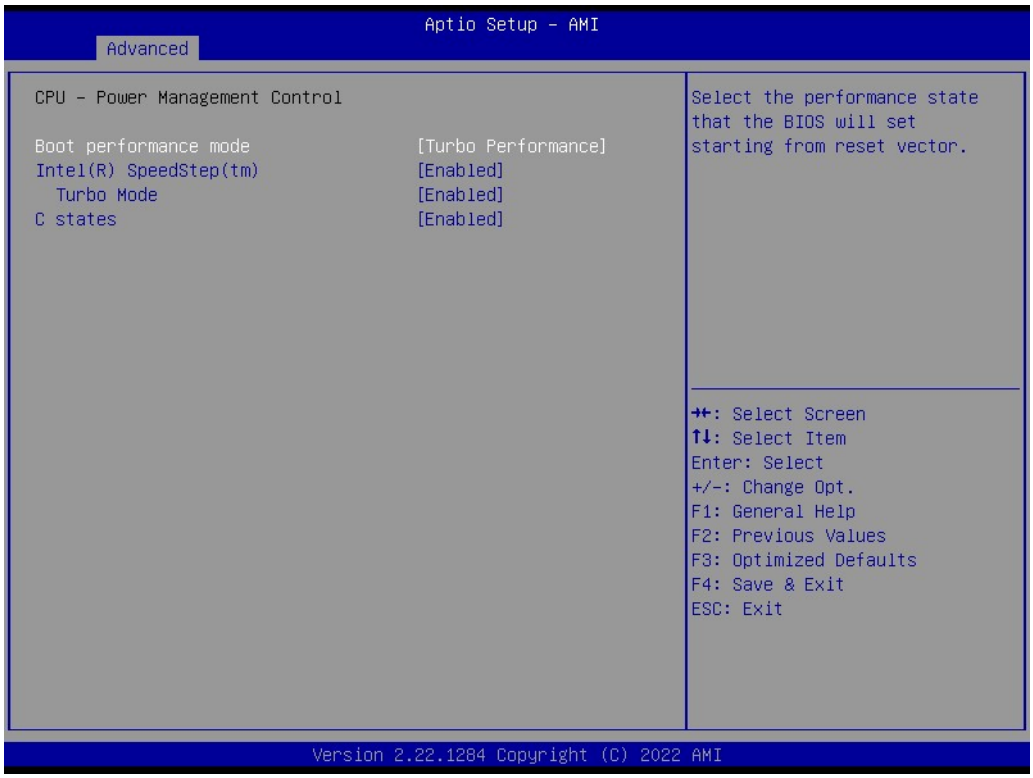


Figure 3.8 Power & Performance

– **Boot performance mode**

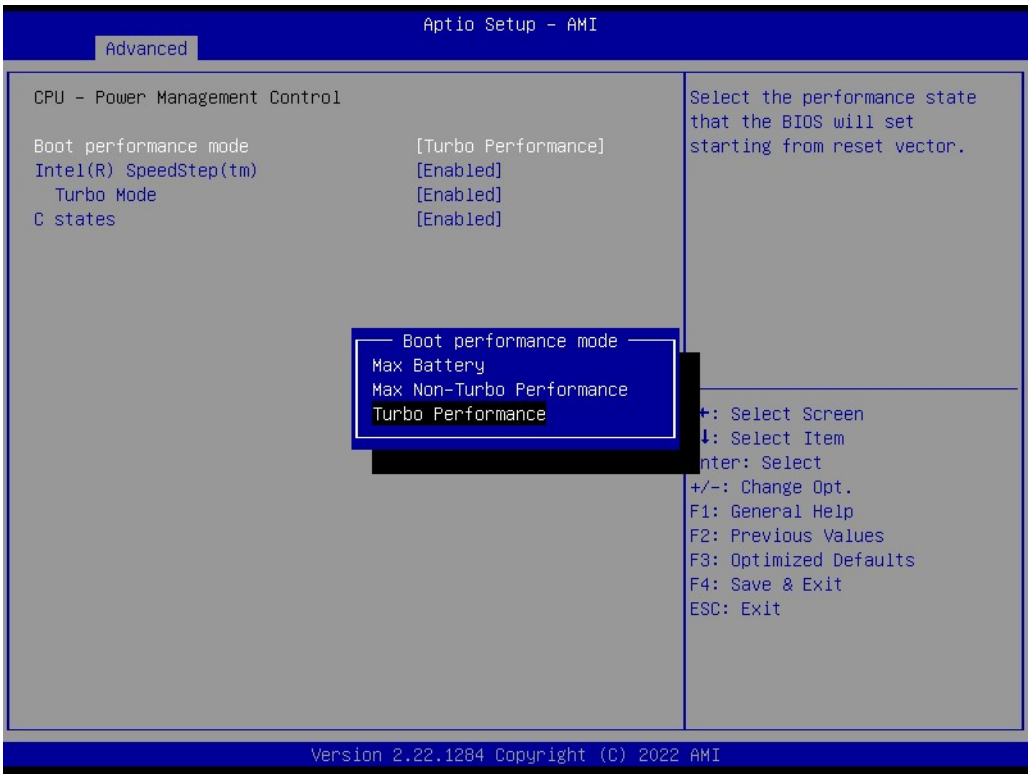


Figure 3.9 Power & Performance

- Boot performance mode

Select the performance state that the BIOS will set starting from reset vector.

- Intel(R) SpeedStep(tm)

Allows more than two frequency ranges to be supported.

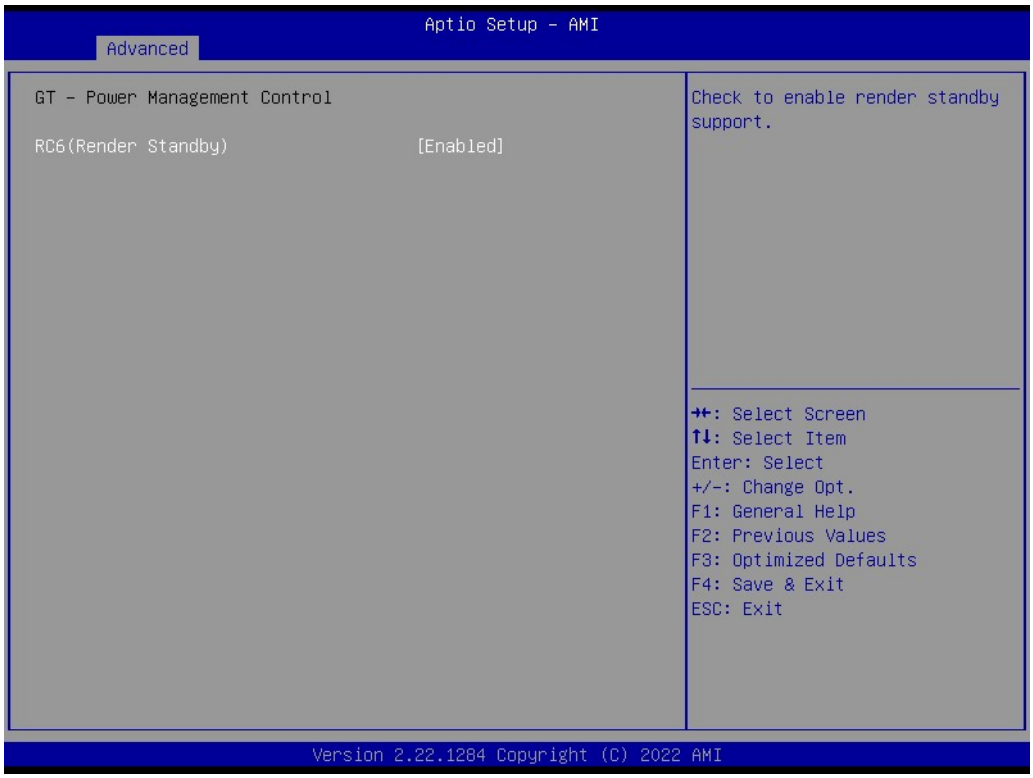
-Turbo Mode

Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.

-C states

Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.

GT - Power Management Control



– **RC6(Render Standby)**
Check to enable render standby support.

3.2.2.5 PCH-FW Configuration

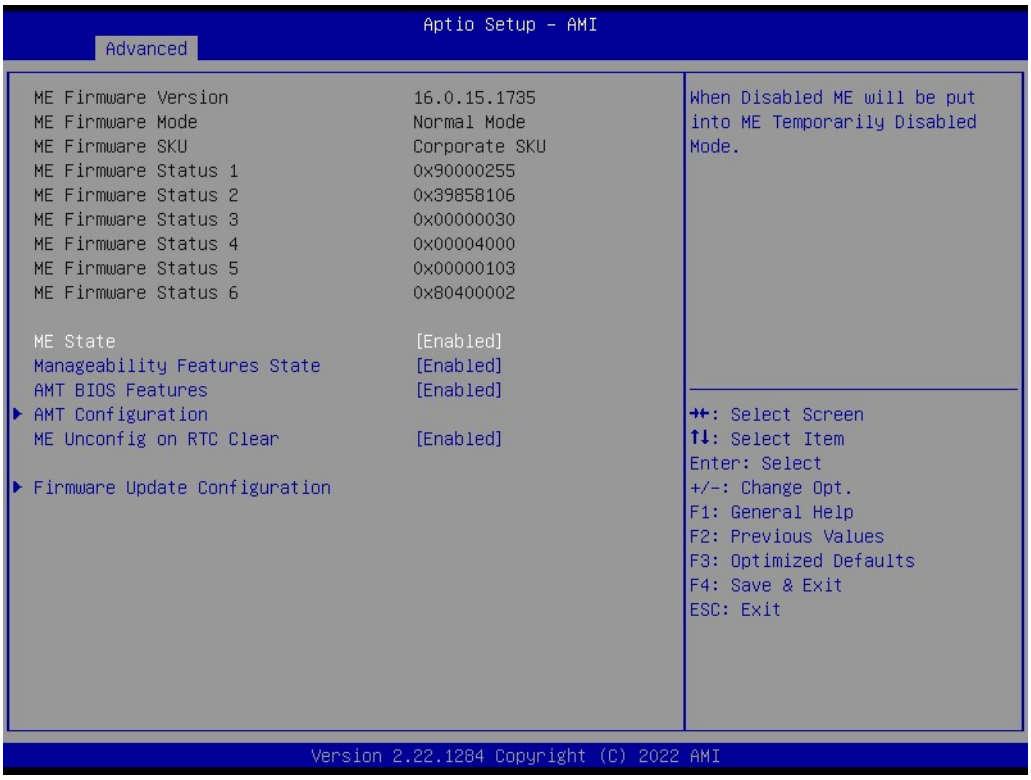


Figure 3.10 Embedded Controller Configuration

- **AMT Configuration**
  Configure Intel(R) Active Management Technology Parameters.
- **ME Unconfig on RTC Clear**
  When Disabled ME will not be unconfigured on RTC clear.
- **Firmware Update Configuration**
  Configure Management Engine Technology Parameters.

AMT configuration

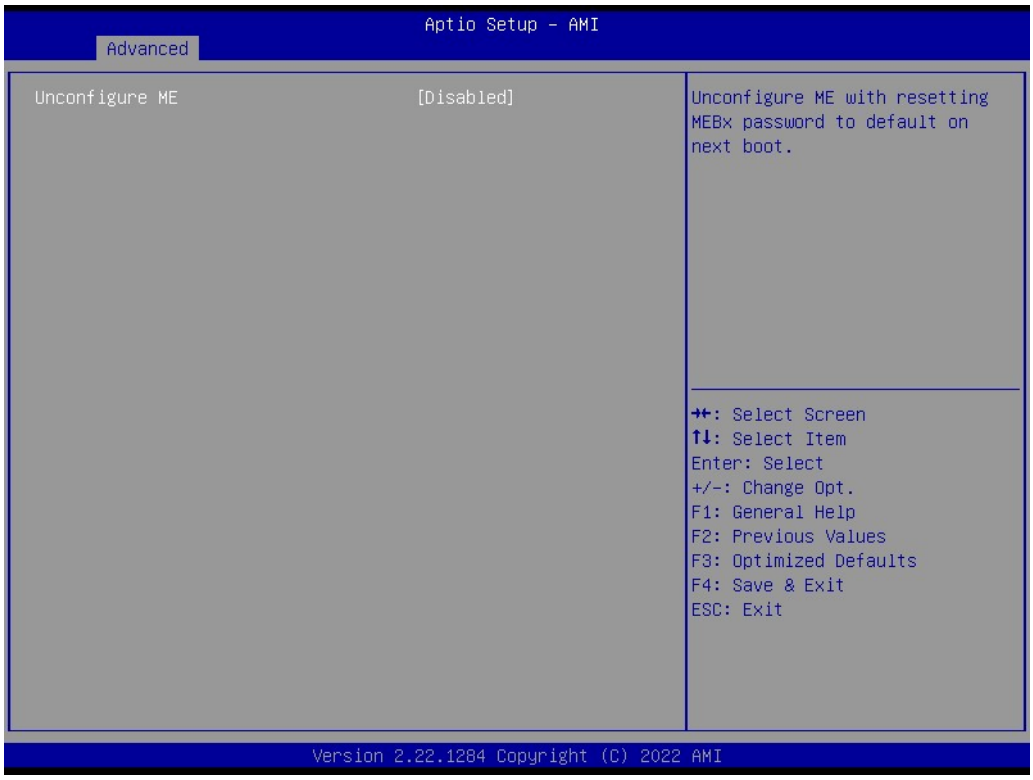


Figure 3.11 AMT Configuration

3.2.2.6 Trusted Computing

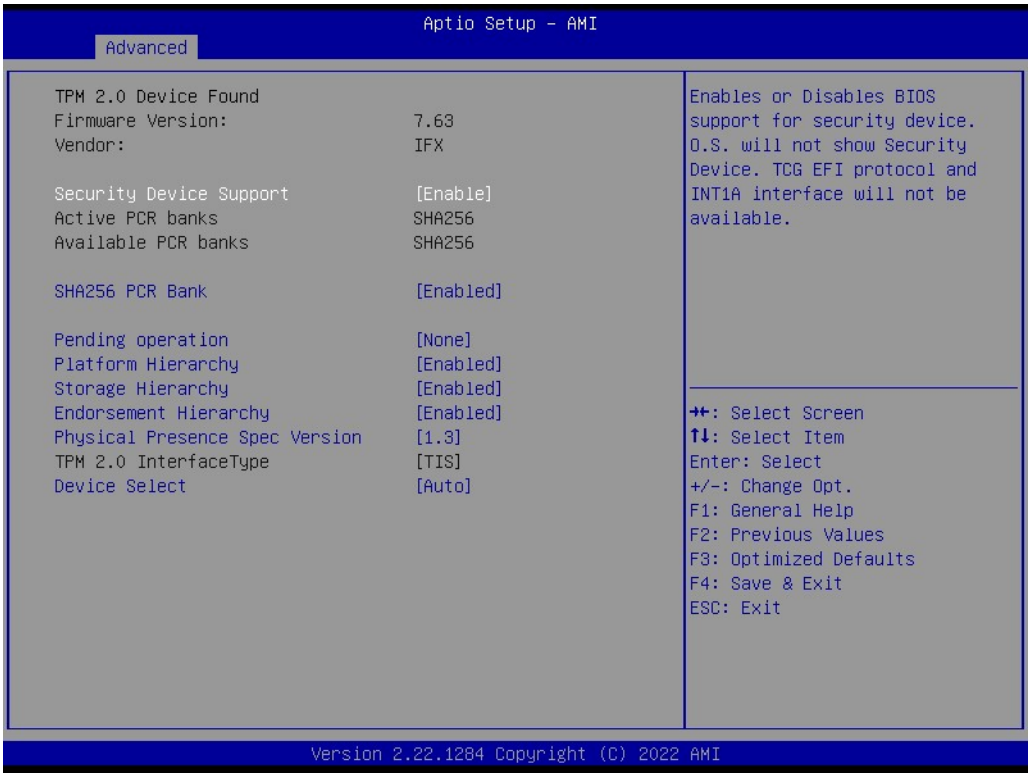


Figure 3.12 Trusted Computing

- **SHA256 PCR Bank**
  Enable or Disable SHA256 PCR Bank.
- **Pending operation**
  Pending operation.
- **Platform Hierarchy**
  Enable or Disable Platform Hierarchy.
- **Storage Hierarchy**
  Enable or Disable Storage Hierarchy.
- **Endorsement Hierarchy**
  Enable or Disable Endorsement Hierarchy.
- **Physical Presence Spec Version**
  Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.
- **Device Select**
  TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.
- **Disable Block Sid**
  Override to allow SID authentication in TCG Storage device.

Pending operation

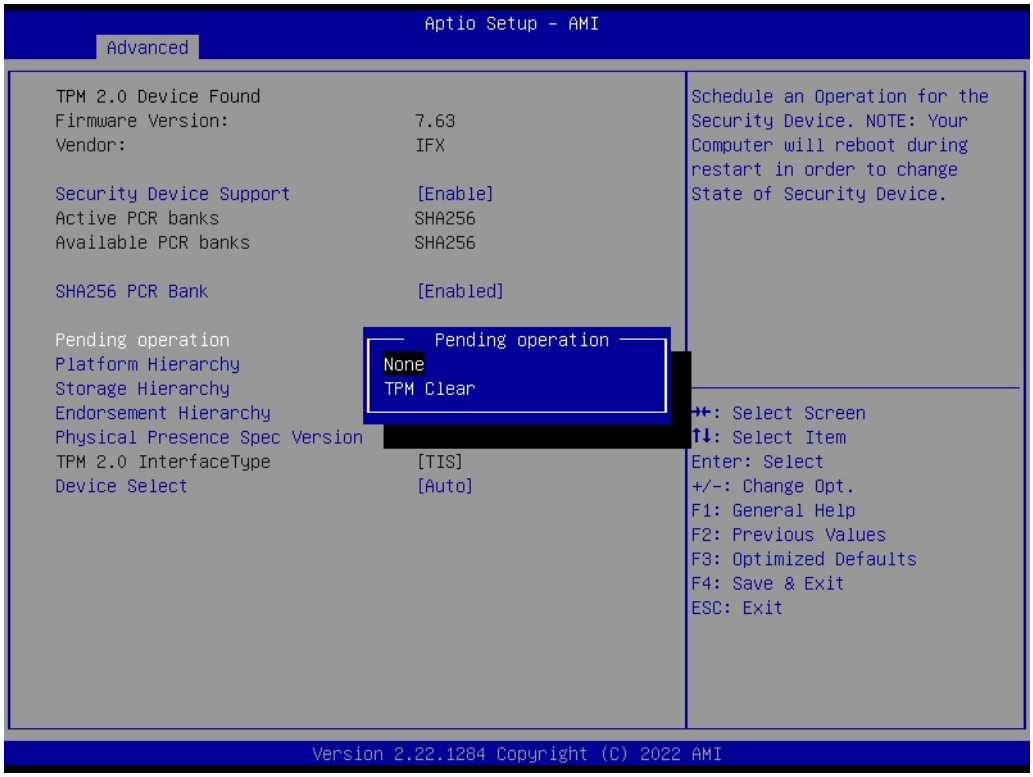


Figure 3.13 Pending operation

Physical Presence Spec Version

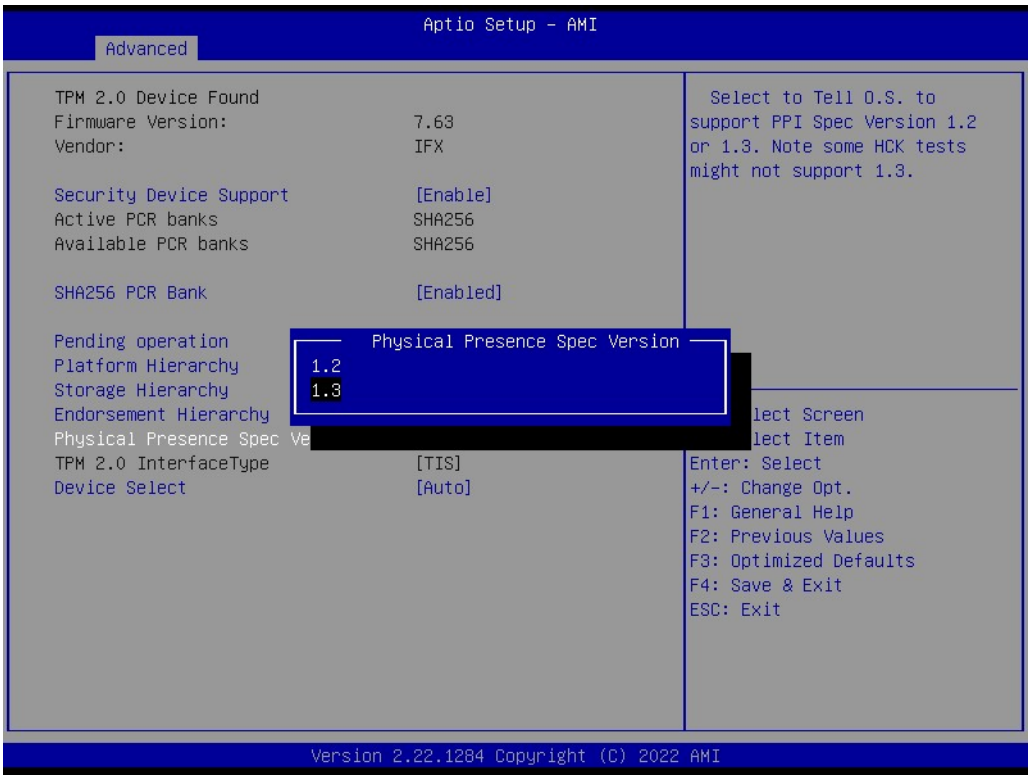


Figure 3.14 Physical Presence Spec Version

Device Select

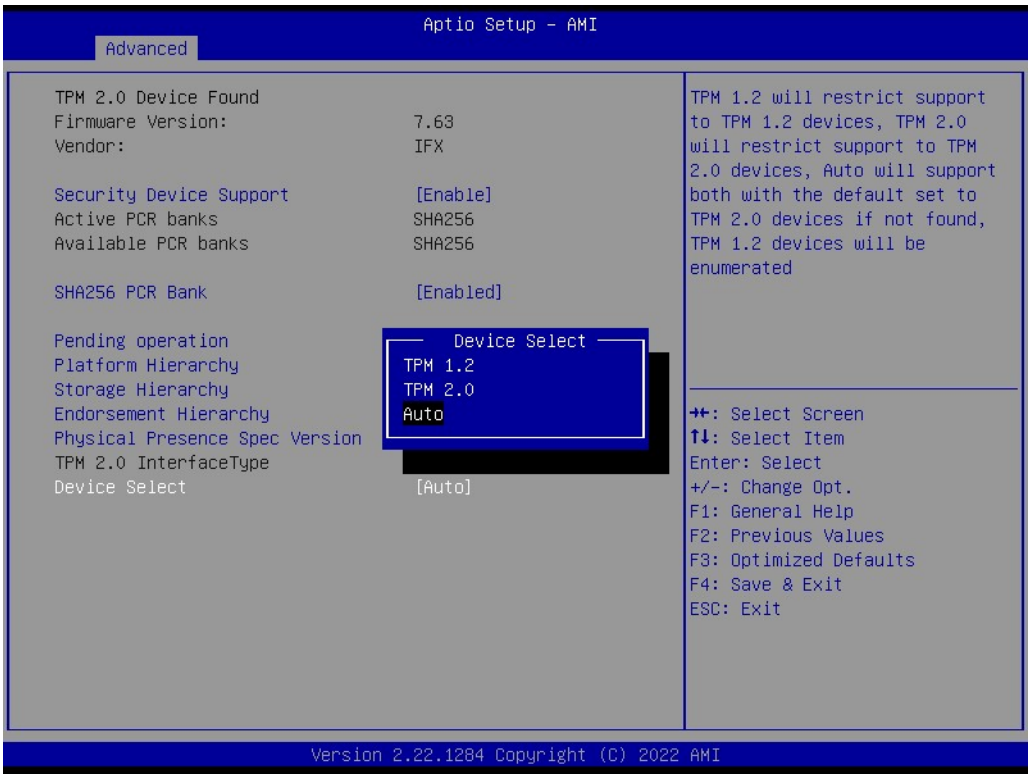


Figure 3.15 Device Select

3.2.2.7 ACPI Settings

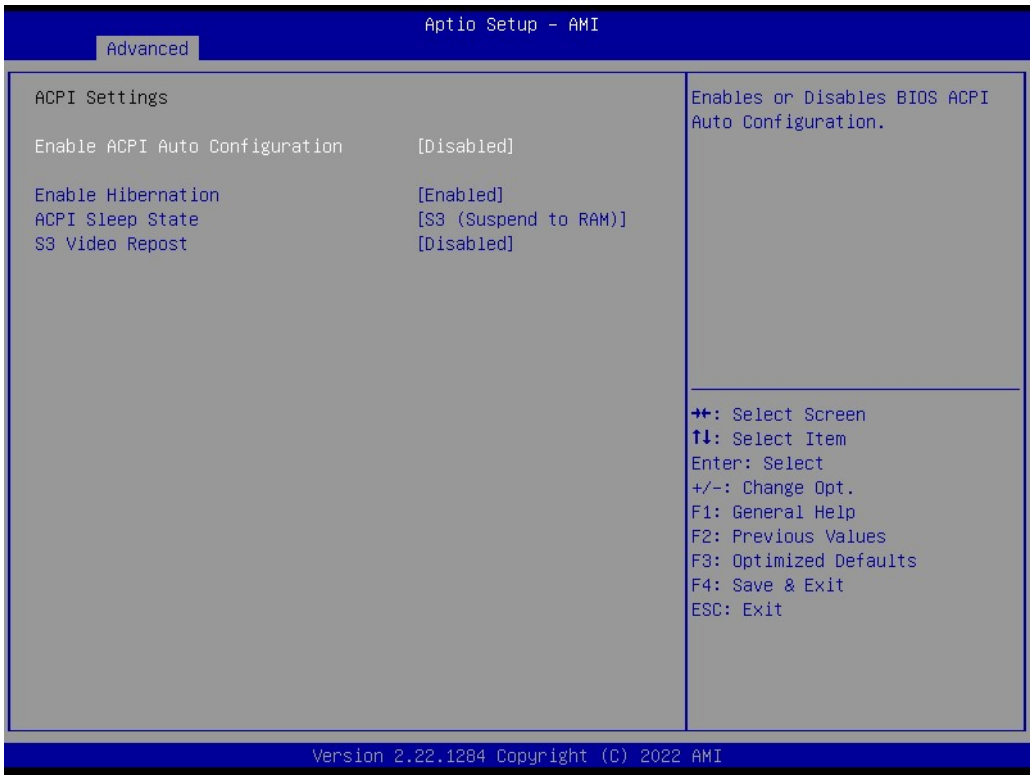


Figure 3.16 ACPI Settings

- **Enable ACPI Auto Configuration**
  Enables or Disables BIOS ACPI Auto Configuration.
- **Enable Hibernation**
  Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
- **ACPI Sleep State**
  Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
- **S3 Video Repost**
  Enable or Disable S3 Video Repost.

3.2.2.8 Embedded Controller

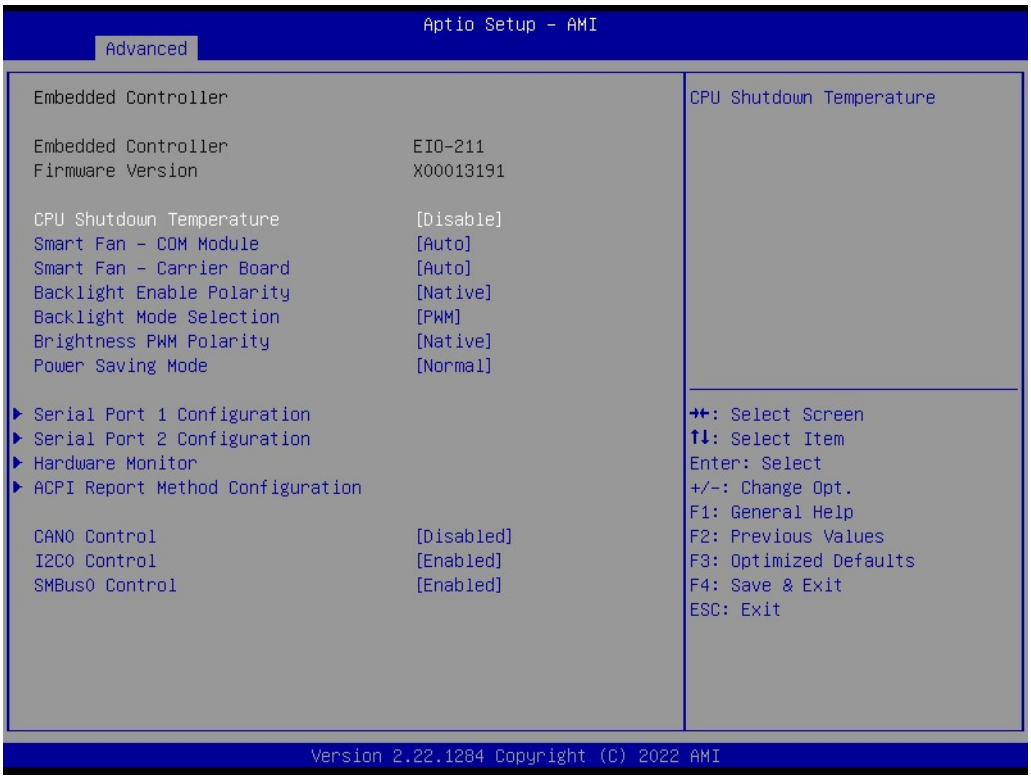


Figure 3.17 Embedded Controller

- **CPU Shutdown Temperature**
  CPU Shutdown Temperature.
- **Smart Fan - COM Module**
  Control COM Module Smart FAN function.
- **Smart Fan - Carrier Board**
  Control Carrier Board Smart FAN function. Get value from EC and only set value when Save Changes.
- **Backlight Enable Polarity**
  Switch Backlight Enable Polarity for Native or Invert.
- **Backlight Mode Selection**
  Switch Backlight Control to PWM or DC mode.
- **Brightness PWM Polarity**
  Backlight Control Brightness PWM Polarity for Native or Invert.
- **Power Saving Mode**
  Select Power Saving Mode.
- **Serial Port 1 Configuration**
  Set Parameters of Serial Port 1 (COMA).
- **Serial Port 2 Configuration**
  Set Parameters of Serial Port 2 (COMB).
- **Hardware Monitor**
  Monitor hardware status.
- **ACPI Report Method Configuration**
  Select ACPI Reporting Method for EC Devices.

- **CAN0 Control**
  Enable/Disable CAN0 controller on RDC-IS200.
- **I2C0 Control**
  Enable/Disable I2C0 controller on RDC-IS200.
- **SMBus0 Control**
  Enable/Disable SMBus0 controller on RDC-IS200.

- **Serial Port 1 Configuration**

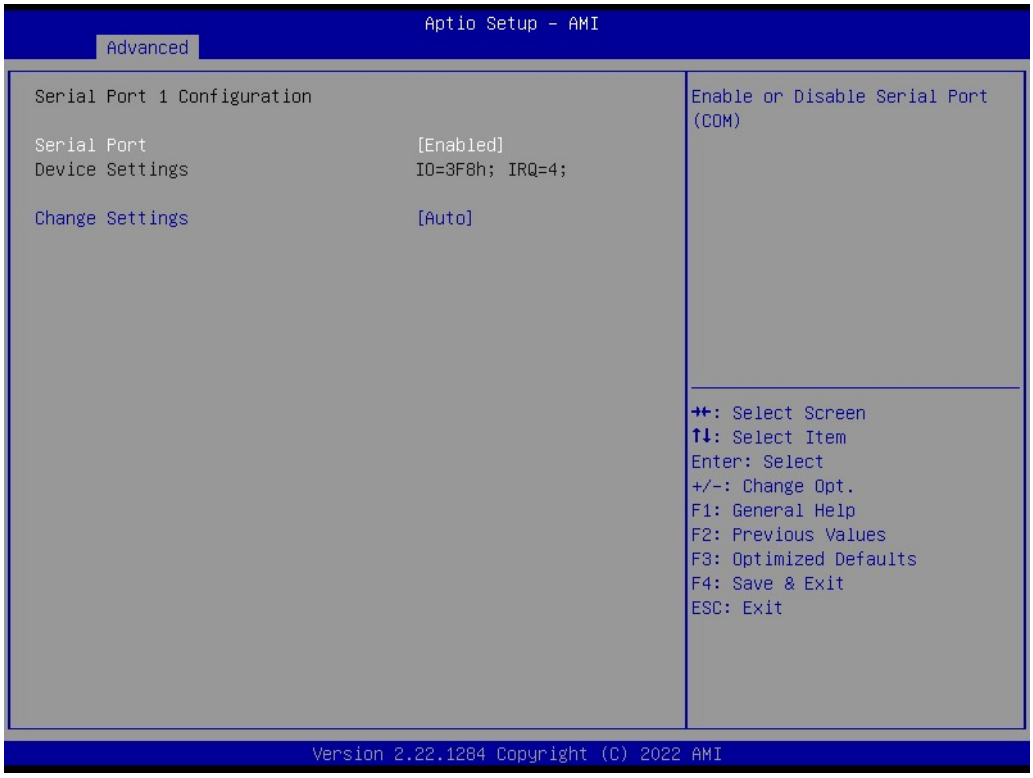


Figure 3.18 Serial Port 1 Configuration

– **Serial Port**
  Enable or Disable Serial Port (COM).
– **Change Settings**
  Select an optimal settings for Super IO Device.

Serial Port 2 Configuration

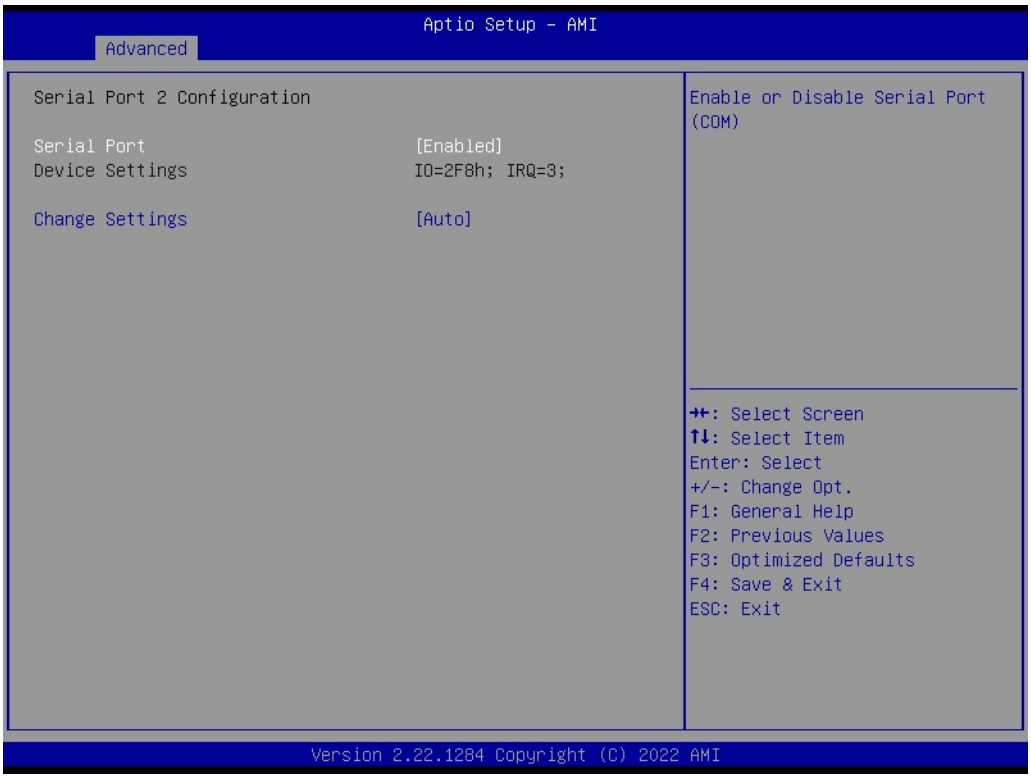


Figure 3.19 Serial Port 2 Configuration

- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select an optimal settings for Super IO Device.

Hardware Monitor

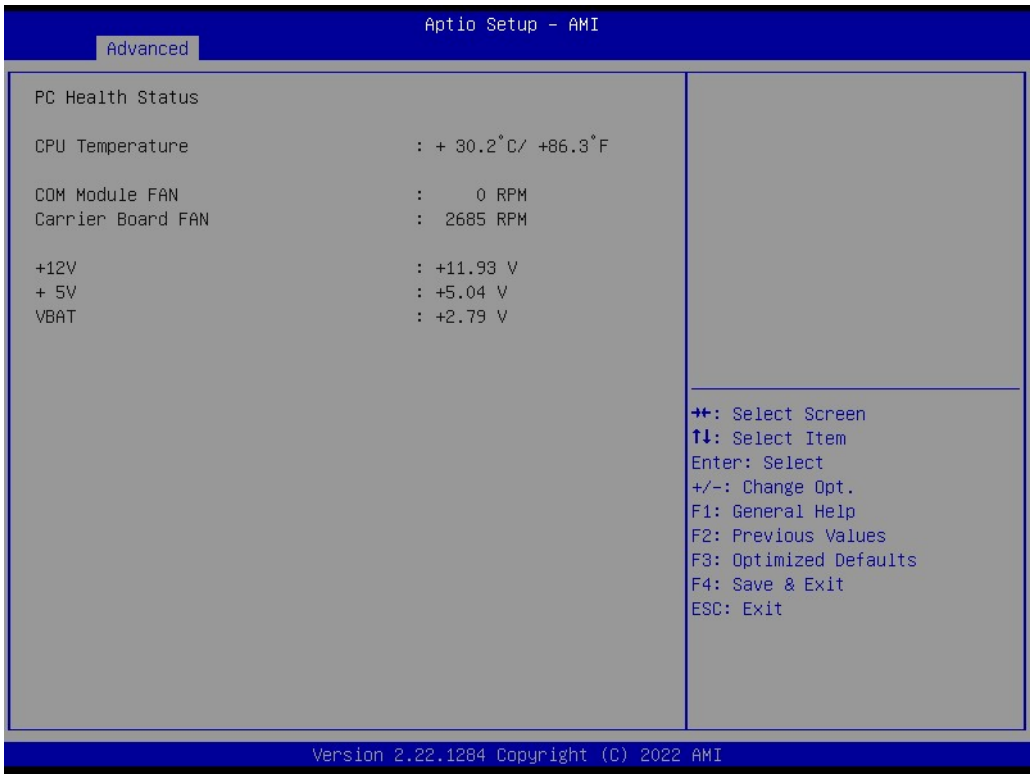


Figure 3.20 Hardware Monitor

ACPI Report Method Configuration

Figure 3.21 ACPI Report Method Configuration

- **ACPI Report Method for CAN Bus**
  Select the ACPI reporting method for EC CAN Bus.
  PNP0C02 -> Reported as reserved motherboard resource.
  Otherwise -> Reported vendor _HID. (Driver installation is necessary.)
- **ACPI Report Method for I2C Bus**
  Select the ACPI reporting method for EC I2C Bus.
  PNP0C02 -> Reported as reserved motherboard resource.
  Otherwise -> Reported vendor _HID. (Driver installation is necessary.)
- **ACPI Report Method for SMBus**
  Select the ACPI reporting method for EC SMBus.
  PNP0C02 -> Reported as reserved motherboard resource.
  Otherwise -> Reported vendor _HID. (Driver installation is necessary.)
- **ACPI Report Method for GPIO**
  Select the ACPI reporting method for EC GPIO.
  PNP0C02 -> Reported as reserved motherboard resource.
  Otherwise -> Reported vendor _HID. (Driver installation is necessary.)

3.2.2.9 Serial Port Console Redirection

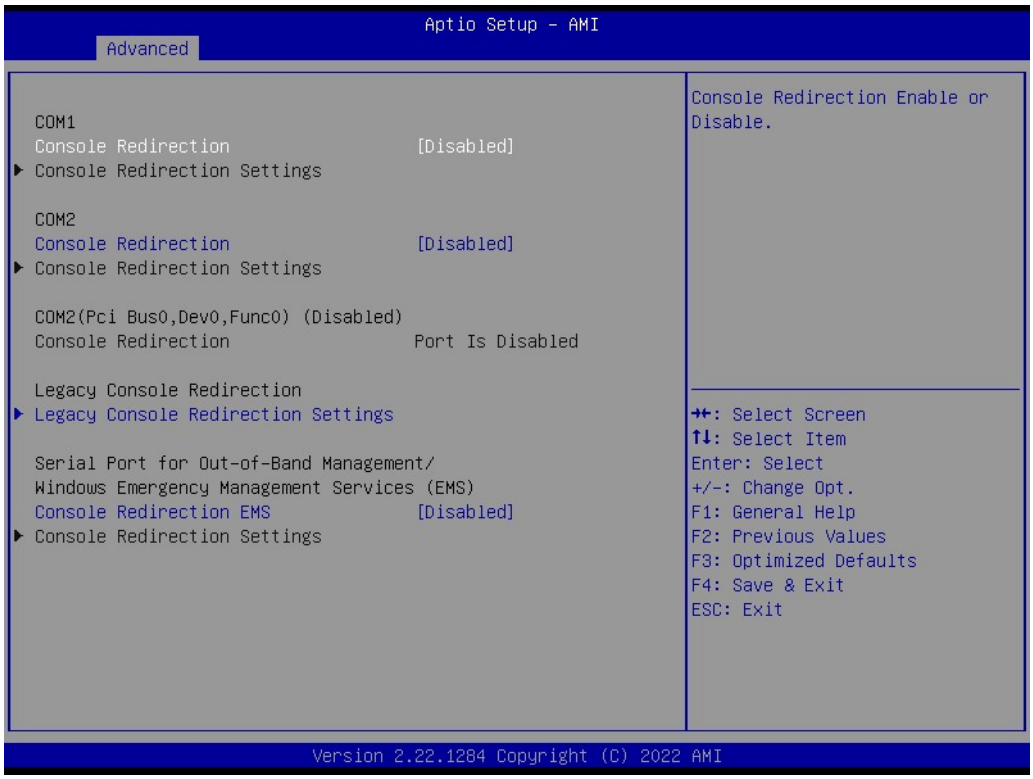


Figure 3.22 Serial Port Console Redirection

- **COM1 Console Redirection**
  Console Redirection Enable or Disable.
- **Console Redirection Settings**
  The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
- **COM2 Console Redirection**
  Console Redirection Enable or Disable.
- **Console Redirection Settings**
  The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
- **Legacy Console Redirection**
  Legacy Console Redirection Settings
- **Console Redirection EMS**
  Console Redirection Enable or Disable.
- **Console Redirection Settings**
  The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

COM1 Console Redirection Settings

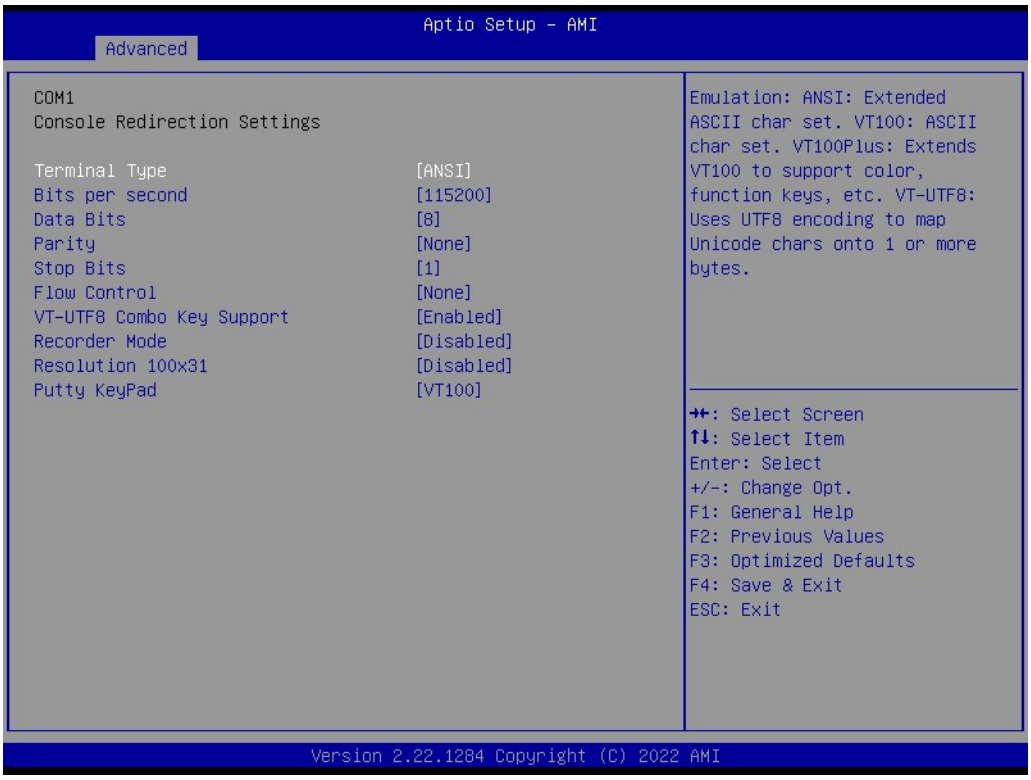


Figure 3.23 COM1 Console Redirection Settings

- **Terminal Type**
  Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100Plus: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
- **Bits per second**
  Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
- **Data Bits**
  Data Bits.
- **Parity**
  A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
- **Stop Bits**
  Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
- **Flow Control**
  Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
- **VT-UTF8 Combo Key Support**
  Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.

– **Recorder Mode**
  With this mode enabled only text will be sent. This is to capture Terminal data.
– **Resolution 100x31**
  Enables or disables extended terminal resolution.
– **Putty KeyPad**
  Select FunctionKey and KeyPad on Putty.

Legacy Console Redirection Settings

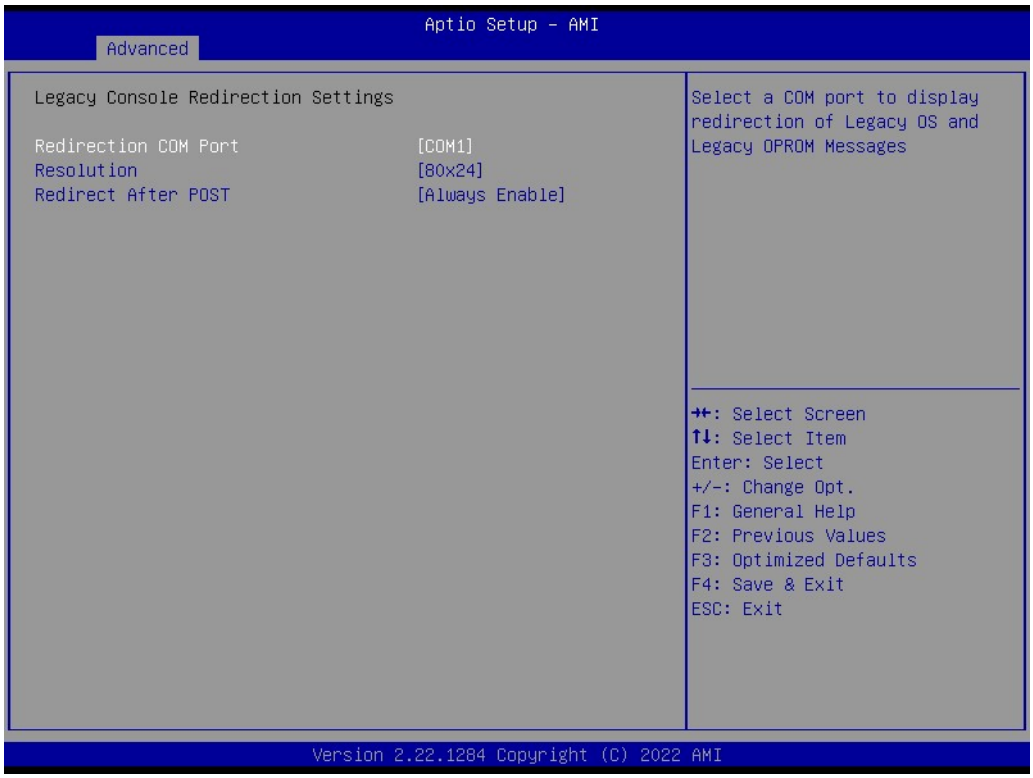


Figure 3.24 Legacy Console Redirection Settings

– **Redirection COM Port**
  Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages.
– **Resolution**
  On Legacy OS, the Number of Rows and Columns supported redirection.
– **Redirect After POST**
  When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

Console Redirection Settings

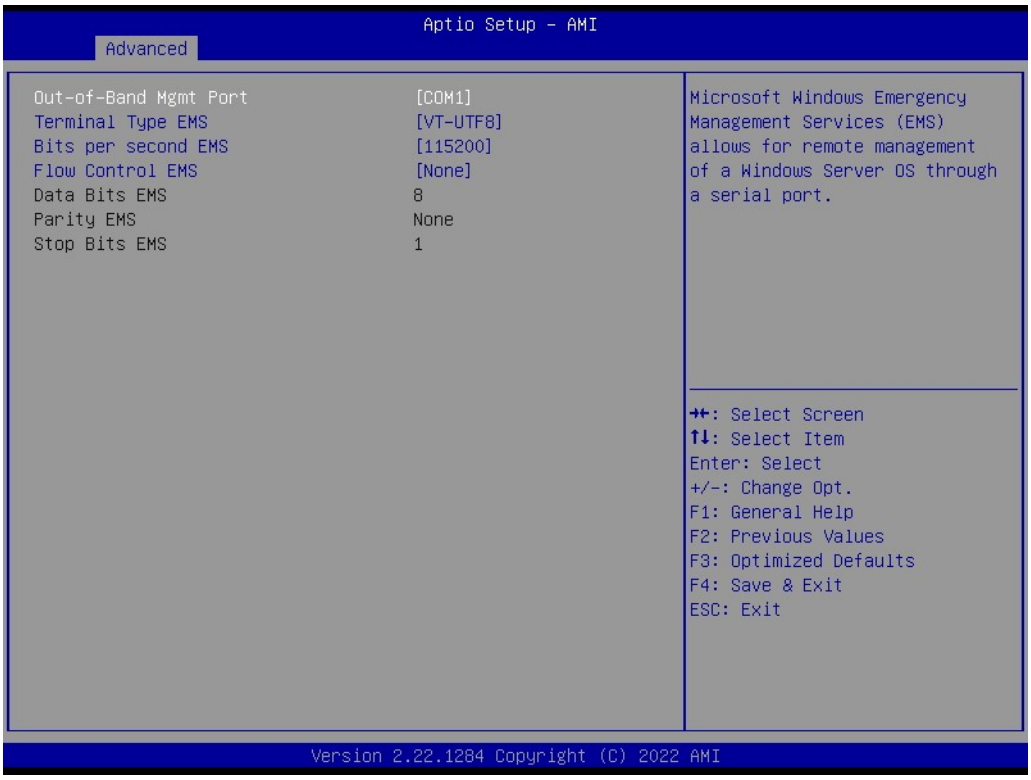


Figure 3.25 Console Redirection Settings

- **Out-of-Band Mgmt Port**
  Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.
- **Terminal Type**
  VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.
- **Bits per second**
  Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
- **Flow Control EMS**
  Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
- **Data Bits EMS**
- **Parity EMS**
  A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
- **Stop Bits EMS**
  Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

3.2.2.10 Intel TXT Information

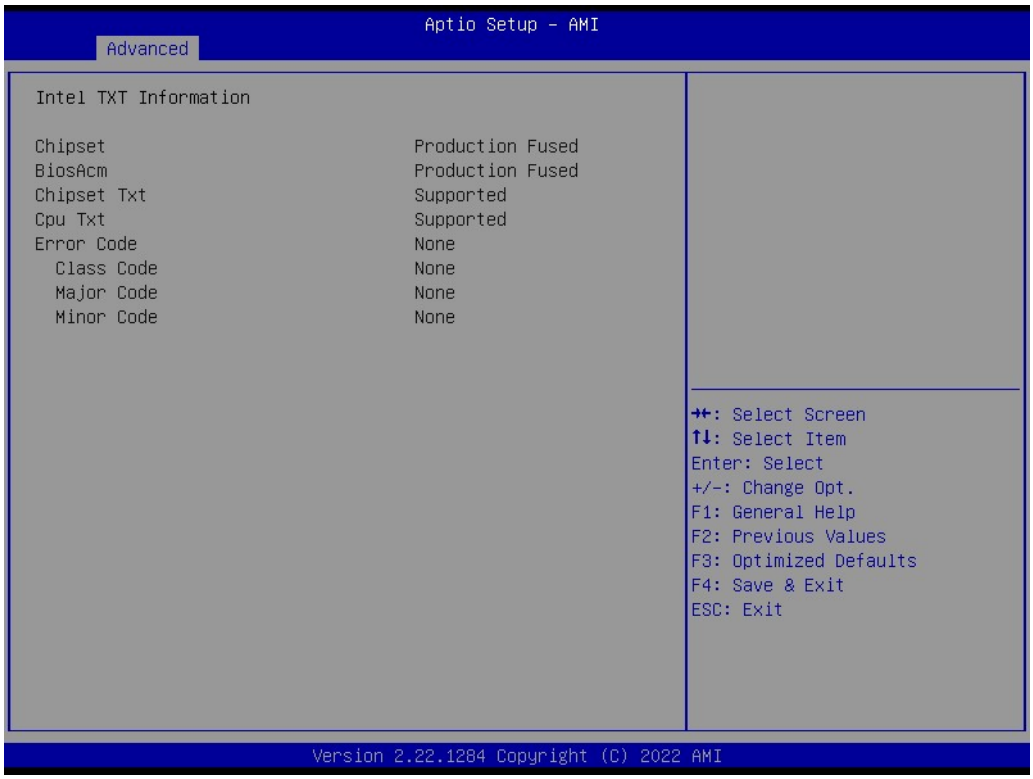


Figure 3.26 Intel TXT Information

3.2.2.11 USB Configuration

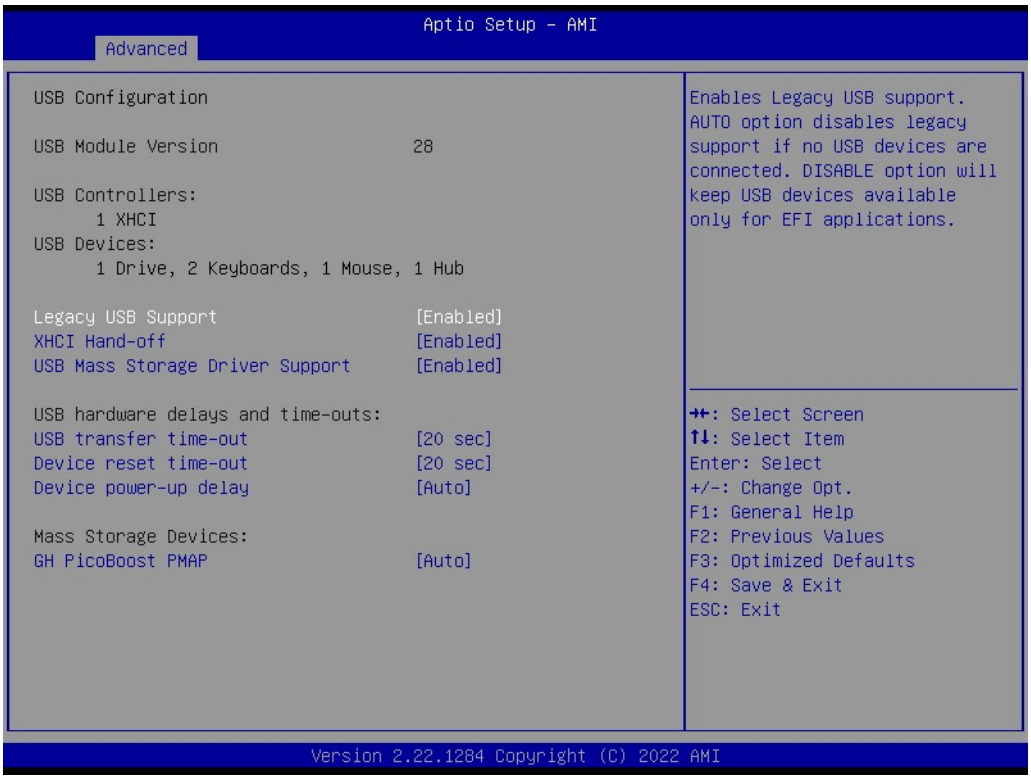


Figure 3.27 USB Configuration

- **Legacy USB Support**
  Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
- **XHCI Hand-off**
  This is a workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
- **USB Mass Storage Driver Support**
  Enable/Disable USB Mass Storage Driver Support.
- **USB transfer time-out**
  The time-out value for Control, Bulk, and Interrupt transfers.
- **Device reset time-out**
  USB mass storage device Start Unit command time-out.
- **Device power-up delay**
  Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.
- **GH PicoBoost PMAP**
  Mass storage device emulation type. ‘Auto’ enumerates devices according to their media format. Optical drivers are emulated as ‘CDROM’, drivers with no media will be emulated according to a driver type.

3.2.2.12 Network Stack Configuration

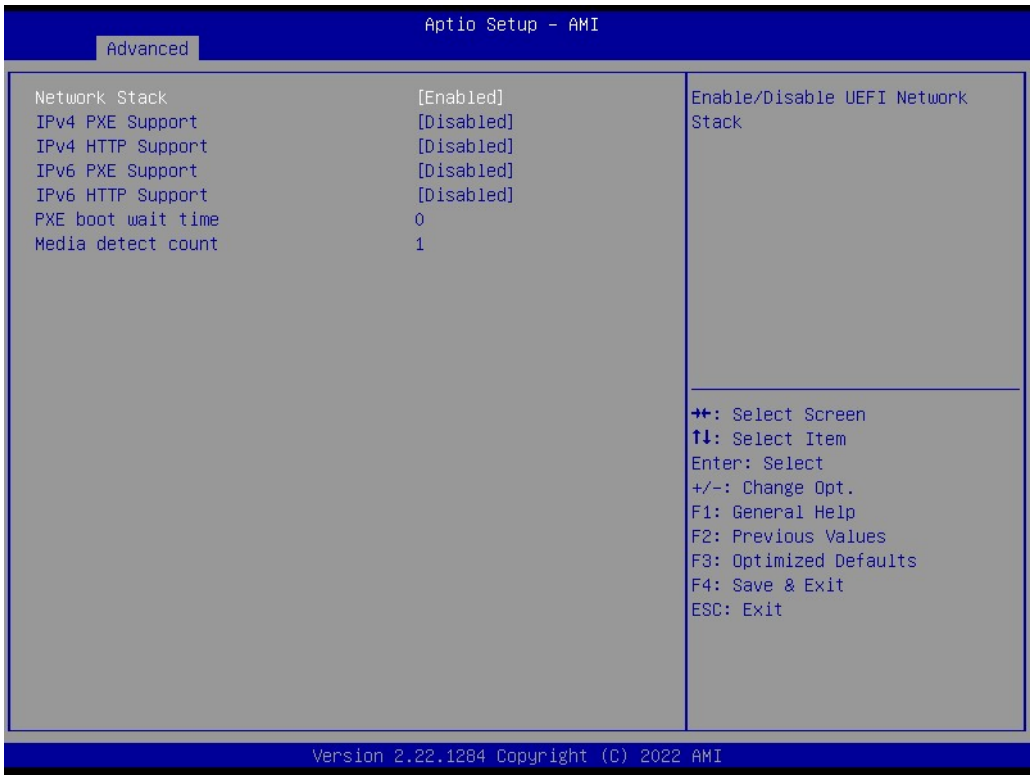


Figure 3.28 Network Stack Configuration

- **Network Stack**
  Enable/Disable UEFI Network Stack.
- **IPv4 PXE support**
  Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
- **IPv4 HTTP Support**
  Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.
- **IPv6 PXE Support**
  Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.
- **IPv6 HTTP Support**
  Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.
- **PXE boot wait time**
  Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.
- **Media detect count**
  Number of times presence of media will be checked. Use either +/- or numeric keys to set the value.

3.2.2.13 NVME Configuration

Figure 3.29 NVME Configuration

3.2.3 Chipset Setup

Figure 3.30 Chipset Setup

- **System Agent (SA)Configuration**
  System Agent Parameters.
- **PCH-I0 Configuration**
  PCH parameters.

3.2.3.1 System Agent (SA) Configuration

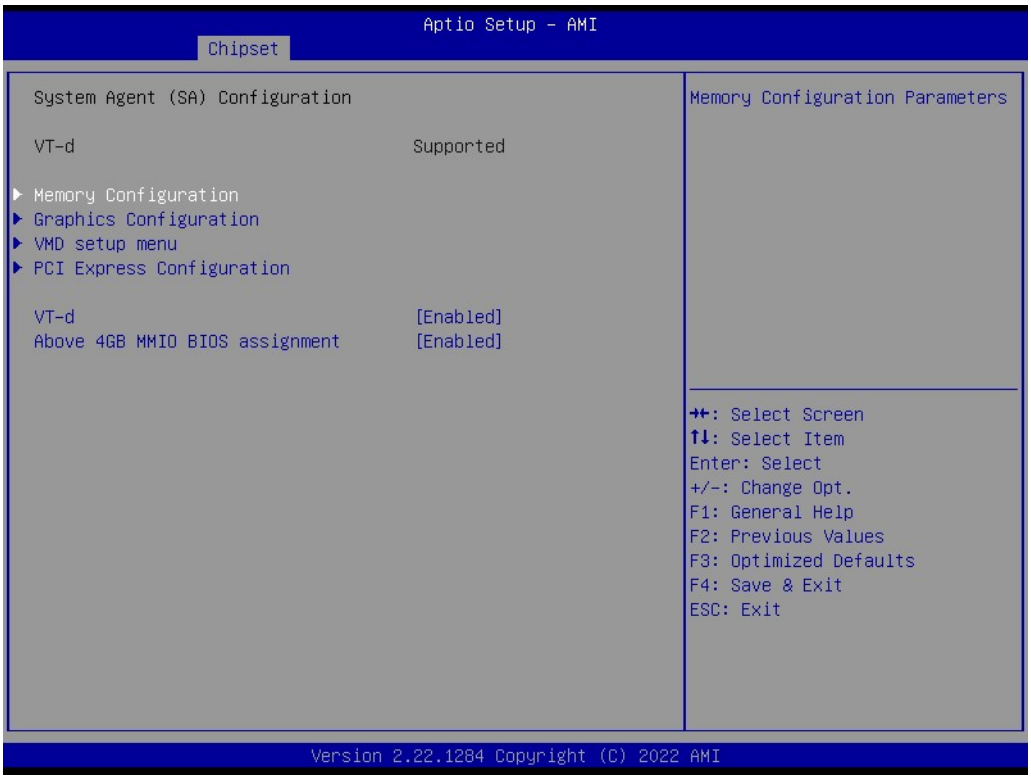


Figure 3.31 System Agent (SA) Configuration

- **Memory Configuration**
  Memory Configuration Parameters.
- **Graphic Configuration**
- **VMD setup menu**
  VMD Configuration.
- **PCI Express Configuration**
  PCI Express Configuration Settings.
- **VT-d**
  VT-d capability.
- **Above 4GB MMIO BIOS assignment**
  Enable/Disable above 4GB memory mapped IO BIOS assignment. This is enabled automatically when aperture size is set to 2048MB.

Memory Configuration

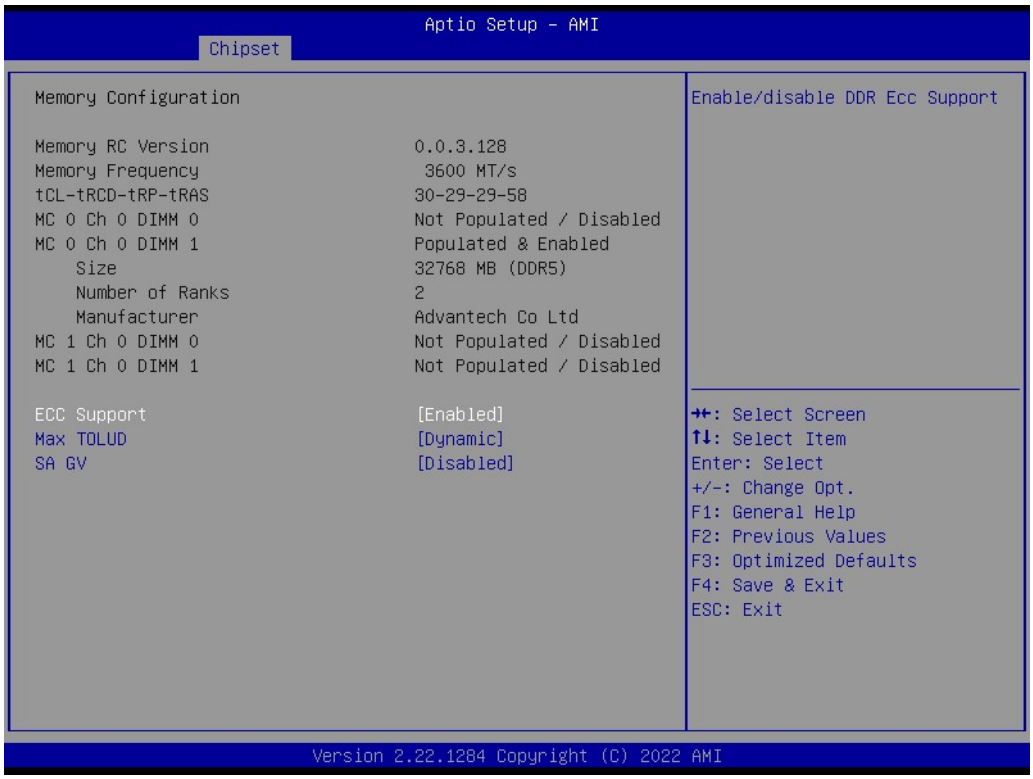


Figure 3.32 Memory Configuration

- **ECC Support**
  Enable/disable DDR ECC Support.
- **Max TOLUD**
  Maximum value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on the largest MMIO length of installed graphic controller.
- **SA GV**
  System Agent Geyserville. Can disable, fix to a specific point, or enable frequency switching.

Graphics Configuration

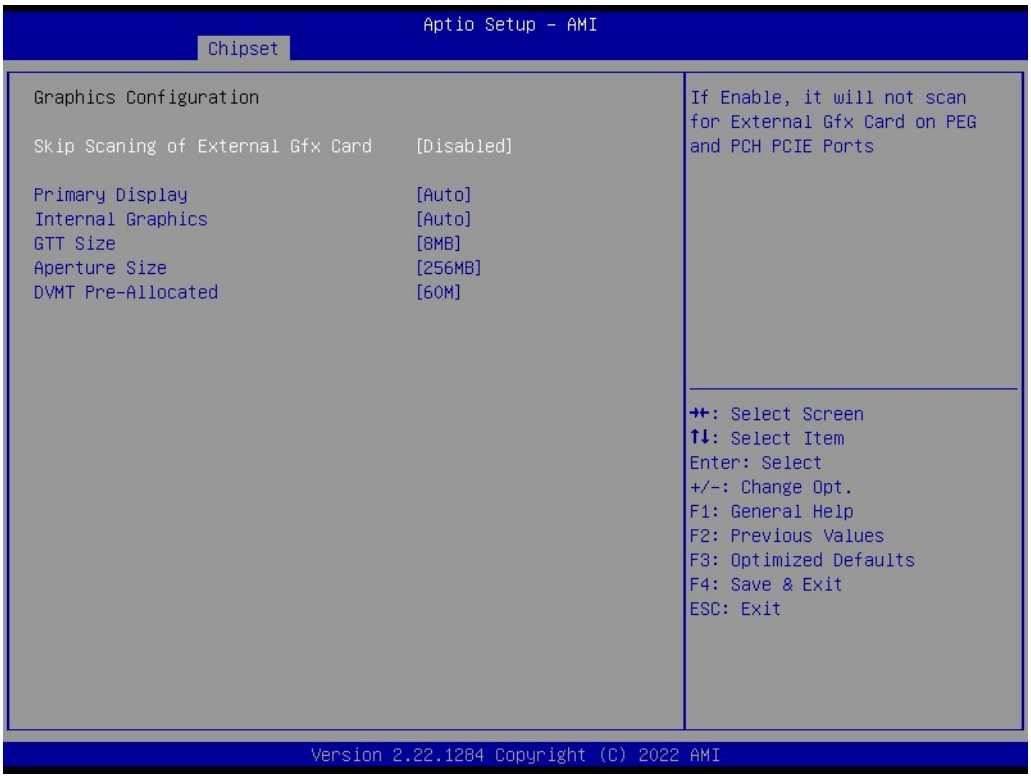


Figure 3.33 Graphics Configuration

- **Skip Scanning of External Gfx Card**
  If Enabled, it will not scan for External Gfx Card on PEG and PCH PCIE Ports.
- **Primary Display**
  Choose the Primary Display Graphics Device from IGFX, PEG, or PCI, or opt for HG to enable Hybrid Graphics.
- **Internal Graphics**
  Keep IGFX enabled base on the setup options.
- **GTT Size**
  Select the GTT size.
- **Aperture Size**
  Select the aperture size. Note: Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM support.
- **DVMT Pre-Allocated**
  Select DVMT5.0 pre-allocated (fixed) Graphics Memory size is used by the internal graphics device.

VMD Setup Menu

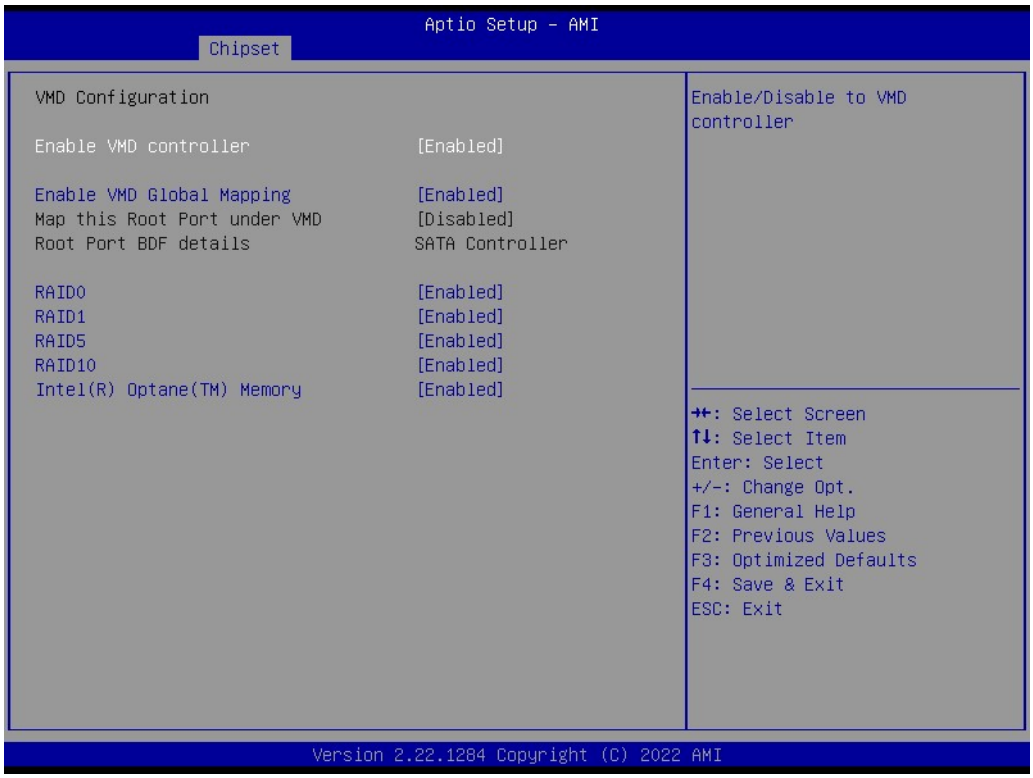


Figure 3.34 VMD Setup Menu

- **Enable VMD controller**
  Enable/Disable to VMD controller.
- **Enable VMD Global Mapping**
  Enable/Disable to VMD Global Mapping.
- **Map this Root Port under VMD**
- **RAID0**
  Enable/Disable RAID0 feature.
- **RAID1**
  Enable/Disable RAID1 feature.
- **RAID5**
  Enable/Disable RAID5 feature.
- **RAID10**
  Enable/Disable RAID10 feature.
- **Intel(R) Optane(TM) Memory**
  Enable/Disable System Acceleration with Intel(R) Optane(TM) Memory feature.

PCI Express Configuration

Figure 3.35 PCI Express Configuration

- **PEG PCIe Port Config**
  Config PEG PCIe Lane 0~15 setting.
- **PCI Express Root Port 1**
- **PCI Express Root Port 2**
- **PCI Express Root Port 3**

– **PCI Express Root Port 1**

Figure 3.36 PCI Express Root Port 1

- PCI Express Root Port 1

Control the PCI Express Root Port.

- Connection Type

Built-In: a built-in device is connected to this rootport. SlotImplemented bit will be clear. Slot: this rootport connects to user-accessible slot. SlotImplemented bit will be set.

- ASPM

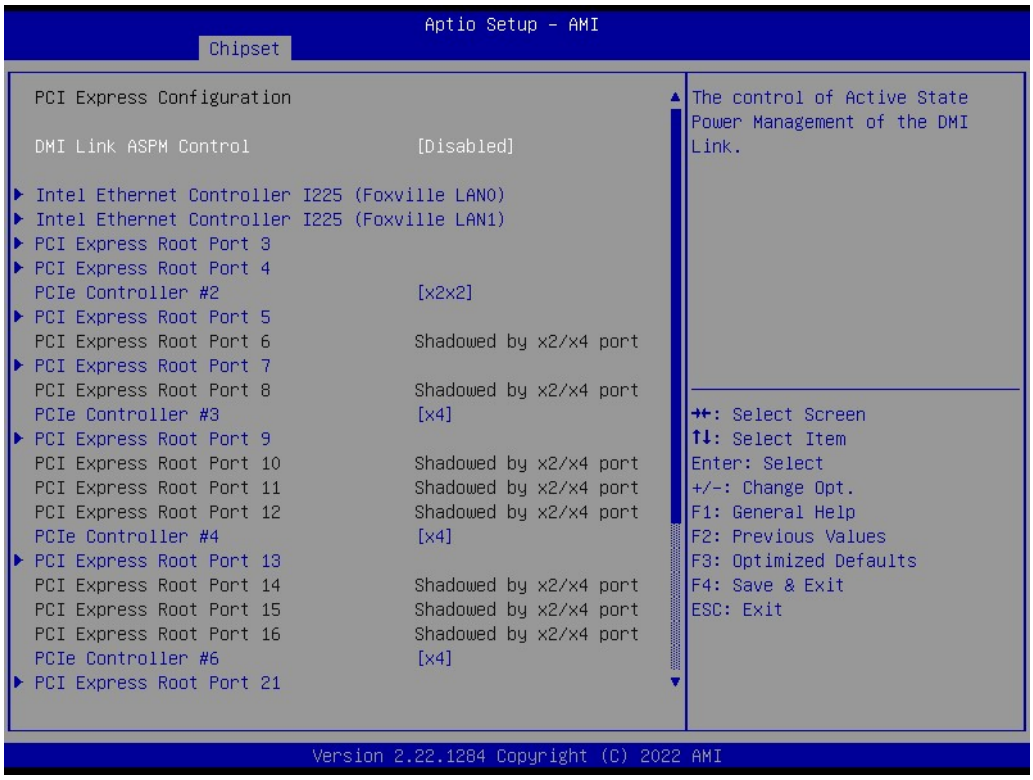
PCI Express Active State Power Management settings.

3.2.3.2 PCH-IO Configuration

Figure 3.37 PCH-IO Configuration

- **PCI Express Configuration**
  PCI Express Configuration settings.
- **SATA Configuration**
  SATA device option settings.
- **USB Configuration**
  USB Configuration settings.
- **Security Configuration**
  Security Configuration settings.
- **HD Audio Configuration**
  HD audio subsystem configuration settings.
- **Seriallo Configuration**
  Seriallo configuration settings.
- **State After G3**
  Specify what state to go to when power is re-applied after a power failure (G3 state).
- **PCIe Ref Pll SSC**
  PCIe Ref Pll SSC Percentage. AUTO - Keep H/W default, no BIOS override. Range is 0.0%-0.5%.
- **IOTG PLL SSCEN (CPU side SSC)**
  Enable/Disable IOTG PLL SSCEN.
- **SPD Write Disable**
  Enable/Disable setting SPD Write Disable. For security recommendations, SPD write disable bit must be set.

PCI Express Configuration



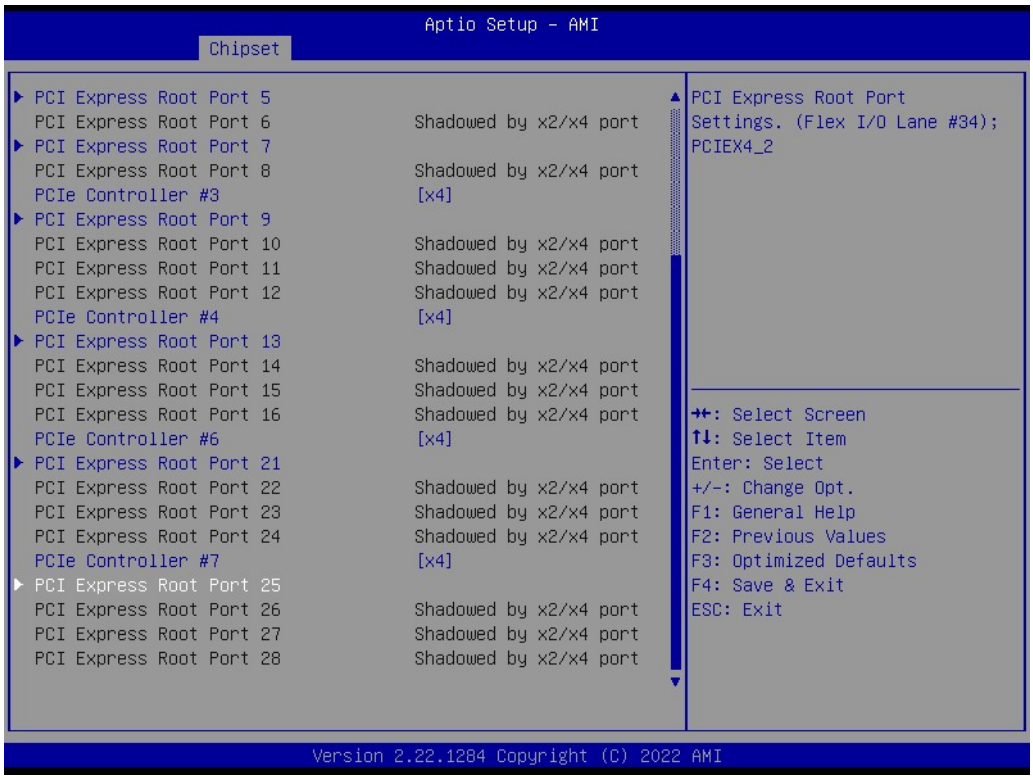


Figure 3.38 PCI Express Configuration

- **Intel Ethernet Controller I225 (Foxville LAN0)**
  PCI Express Root Port Settings.(Flex I/O Lane #10); CN2.
- **Intel Ethernet Controller I225 (Foxville LAN0)**
  PCI Express Root Port Settings. (Flex I/O Lane #11); CN3.

- **PCI Express Root Port 3**
  PCI Express Root Port Settings. (Flex I/O Lane #12); PCIEX4_6.
- **PCI Express Root Port 4**
  PCI Express Root Port Settings. (Flex I/O Lane #13); PCIEX4_6.
- **PCIe Controller #2**
  PCIe Controller #2 (Port 5-8).
- **PCI Express Root Port 5**
  PCI Express Root Port Settings. (Flex I/O Lane #14); M2B1.
- **PCI Express Root Port 6**
- **PCI Express Root Port 7**
  PCI Express Root Port Settings. (Flex I/O Lane #16); M2E1.
- **PCI Express Root Port 8**
- **PCIe Controller #3**
  PCIe Controller #3 (Port 9-12).
- **PCI Express Root Port 9**
  PCI Express Root Port Settings. (Flex I/O Lane #18); PCIEX4_5.
- **PCI Express Root Port 10**
- **PCI Express Root Port 11**
- **PCI Express Root Port 12**
- **PCIe Controller #4**
  PCIe Controller #4 (Port 13-16).
- **PCI Express Root Port 13**
  PCI Express Root Port Settings. (Flex I/O Lane #22); PCIEX4_4.
- **PCI Express Root Port 14**
- **PCI Express Root Port 15**
- **PCI Express Root Port 16**
- **PCIe Controller #6**
  PCIe Controller #6 (Port 21-24).
- **PCI Express Root Port 21**
  PCI Express Root Port Settings. (Flex I/O Lane #30); PCIEX4_1.
- **PCI Express Root Port 22**
- **PCI Express Root Port 23**
- **PCI Express Root Port 24**
- **PCIe Controller #7**
  PCIe Controller #7 (Port 25-28).
- **PCI Express Root Port 25**
  PCI Express Root Port Settings. (Flex I/O Lane #34); PCIEX4_2.
- **PCI Express Root Port 26**
- **PCI Express Root Port 27**
- **PCI Express Root Port 28**

– **Intel Ethernet Controller I225**

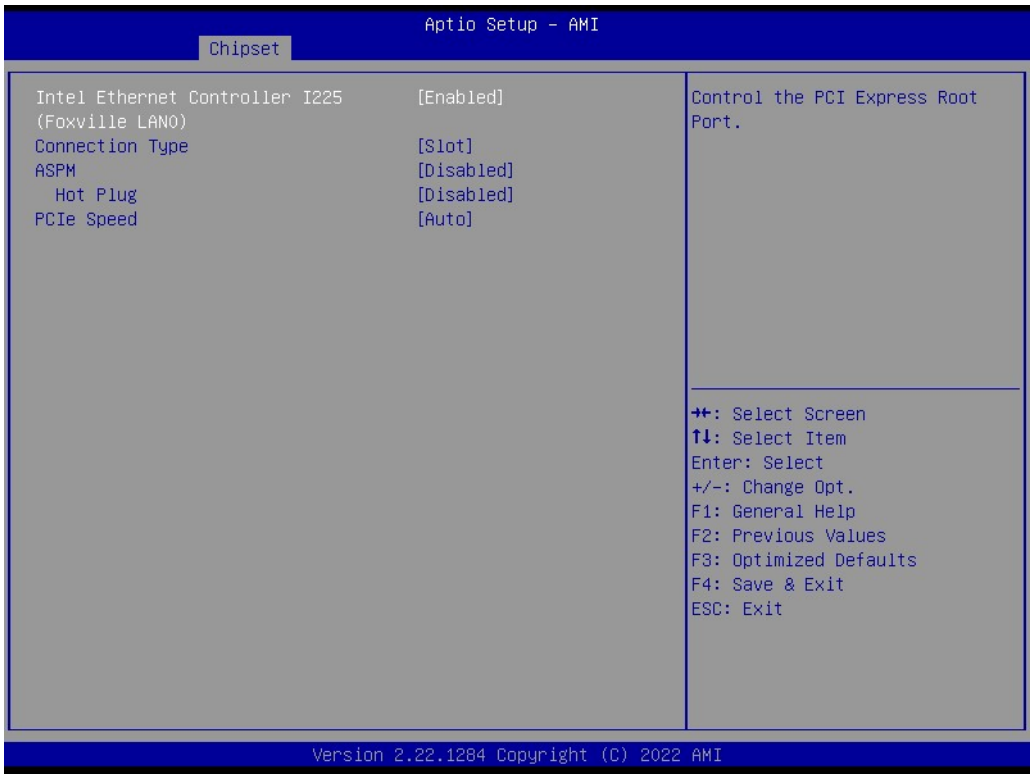


Figure 3.39 Intel Ethernet Controller I225

- **Intel Ethernet Controller I225 (Foxville LAN0)**

Control the PCI express root port.

- Connection Type

Built-In: a built-in device is connected to this rootport. SlotImplemented bit will be clear. Slot: this rootport connects to user-accessible slot. SlotImplemented bit will be set.

- ASPM

PCI Express Active State Power Management settings.

- Hot plug

PCI Express hot plug enable/disable.

- PCIe Speed

Configure PCIe Speed.

– **PCIE Express Root Port 5**

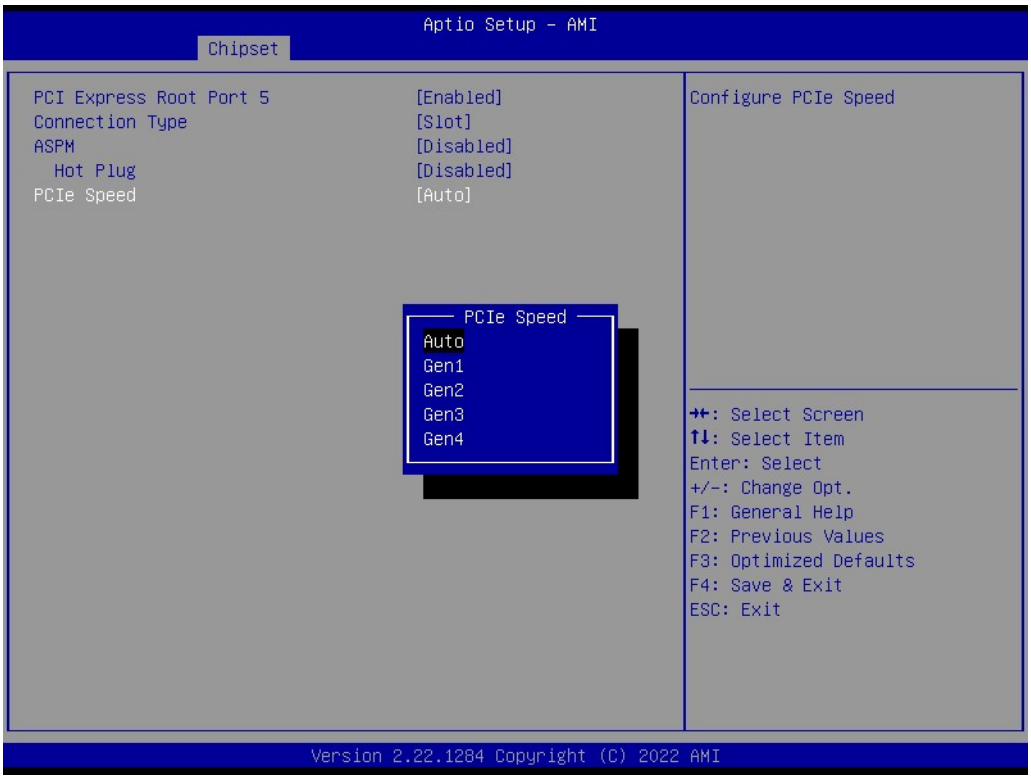


Figure 3.40 PCIE Express Root Port 5

- PCIE Express Root Port 5

Control the PCI express root port.

- Connection Type

Built-In: a built-in device is connected to this rootport. SlotImplemented bit will be clear. Slot: this rootport connects to user-accessible slot. SlotImplemented bit will be set.

- ASPM

PCI Express Active State Power Management settings.

- Hot plug

PCI Express hot plug enable/disable.

- PCIe Speed

Configure PCIe Speed.

SATA Configuration

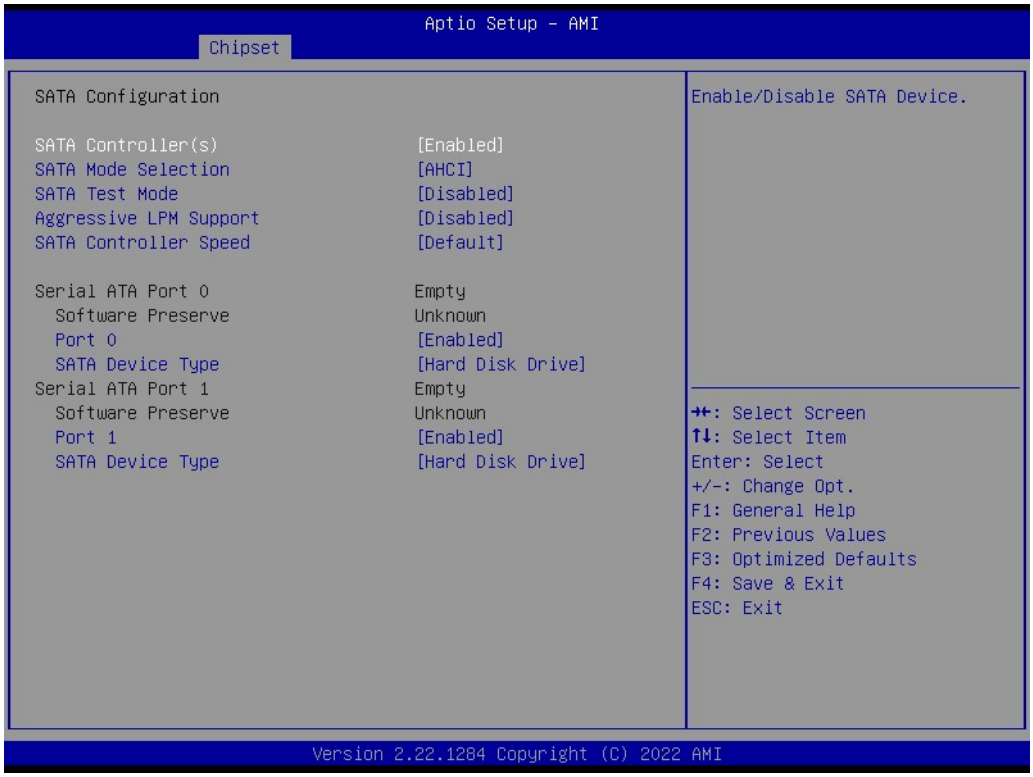


Figure 3.41 SATA Drives

- **SATA Controller(s)**
  Enable/Disable SATA Device.
- **SATA Mode Selection**
  Determines how SATA controller(s) operate.
- **SATA Test Mode**
  Test Mode Enable/Disable (Loop Back).
- **Aggressive LPM Support**
  Enable PCH to aggressively enter link power state.
- **SATA Controller Speed**
  Indicates the maximum speed the SATA controller can support.
- **Port 0**
  Enable or Disable SATA Port.
- **SATA Device Type**
  Identify if the SATA port is connected to a Solid State Drive or Hard Disk Drive.

USB Configuration

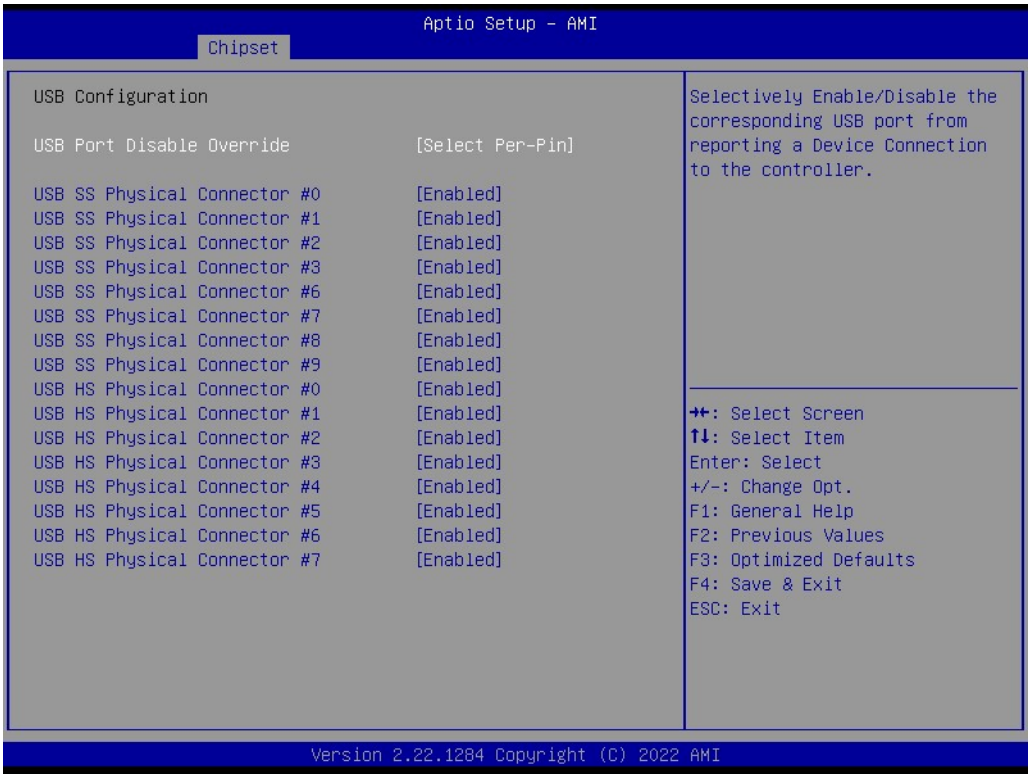


Figure 3.42 USB Configuration

- **USB Port Disable Override**
  Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.
- **USB SS Physical Connector #0**
  Enable/Disable this USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.

Security Configuration

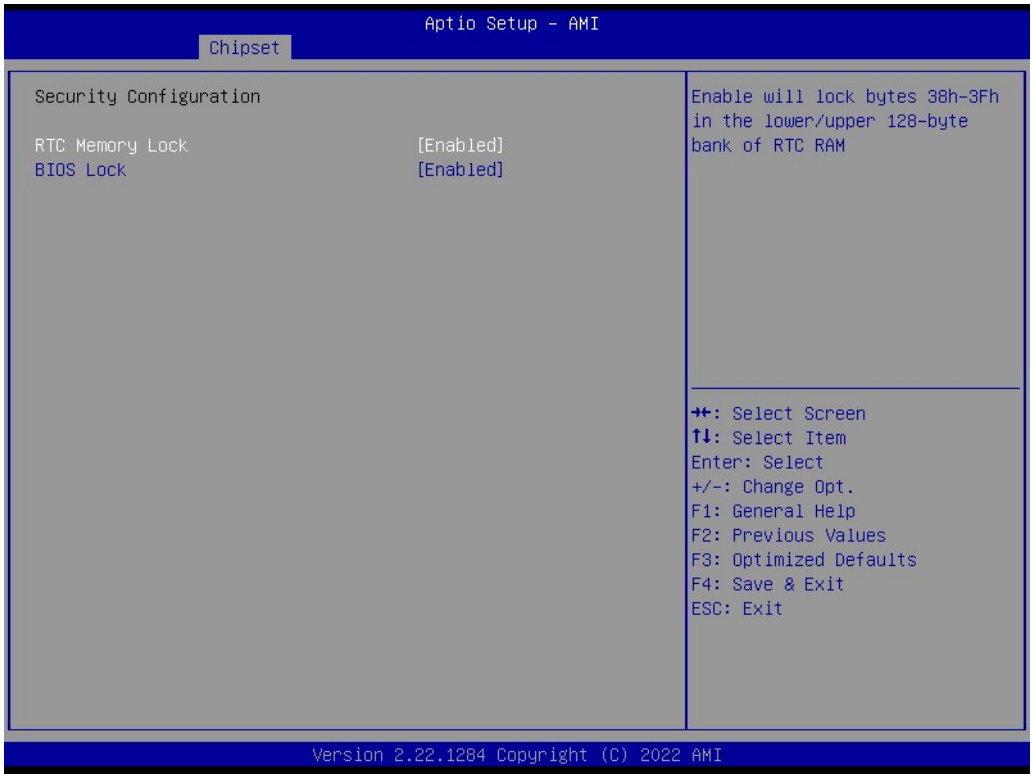


Figure 3.43 Security Configuration

- **RTC Memory Lock**
  Enable will lock bytes 38h-3Fh in the lower/upper 126-byte bank of RTC RAM.
- **BIOS Lock**
  Enable/Disable the PCH BIOS lock enable feature. Needs to be enabled to ensure SMM protection of flash.

HD Audio Subsystem Configuration Settings

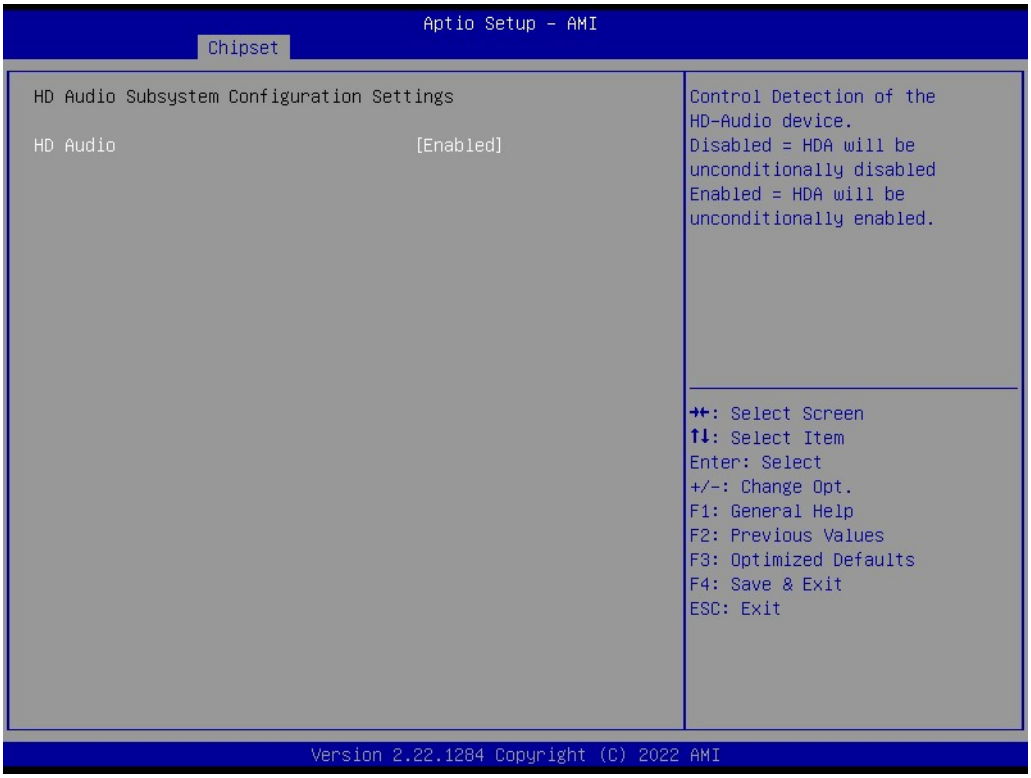


Figure 3.44 HD Audio Subsystem Configuration Settings

– **HD Audio**

Control Detection of the HD-Audio device. Disabled=HDA will be unconditionally disabled. Enabled=HDA will be unconditionally enabled.

- **Seriallo Configuration**

Figure 3.45 Seriallo Configuration

3.2.4 Security Chipset

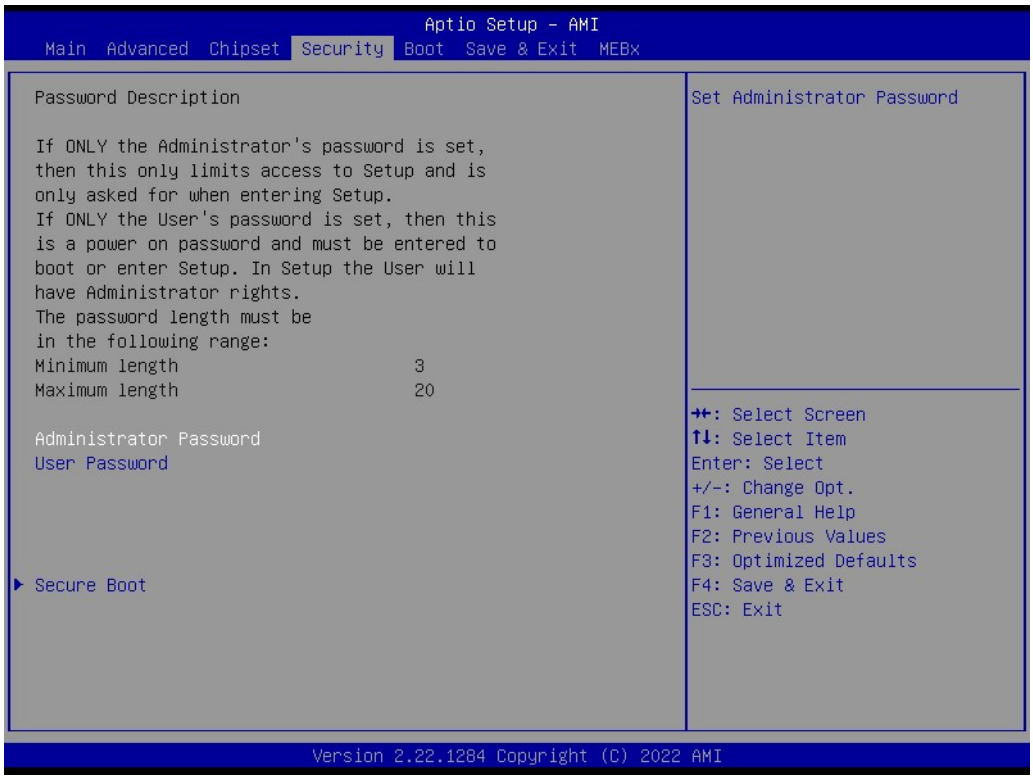


Figure 3.46 Security Chipset

- **Administrator Password**
  Set Setup Administrator Password.
- **User Password**
  Set User Password.
- **Secure Boot**
  Secure Boot Configuration.

3.2.4.1 Secure Boot

Figure 3.47 Secure Boot

- **Secure Boot**
  Secure Boot feature is Active if Secure Boot is Enabled, Platform Key(PK) is enrolled and the System is in User mode. The mode change requires platform reset.
- **Secure Boot Mode**
  Secure Boot mode options:
  Standard or Custom.
  In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.

3.2.4.2 Boot Setup

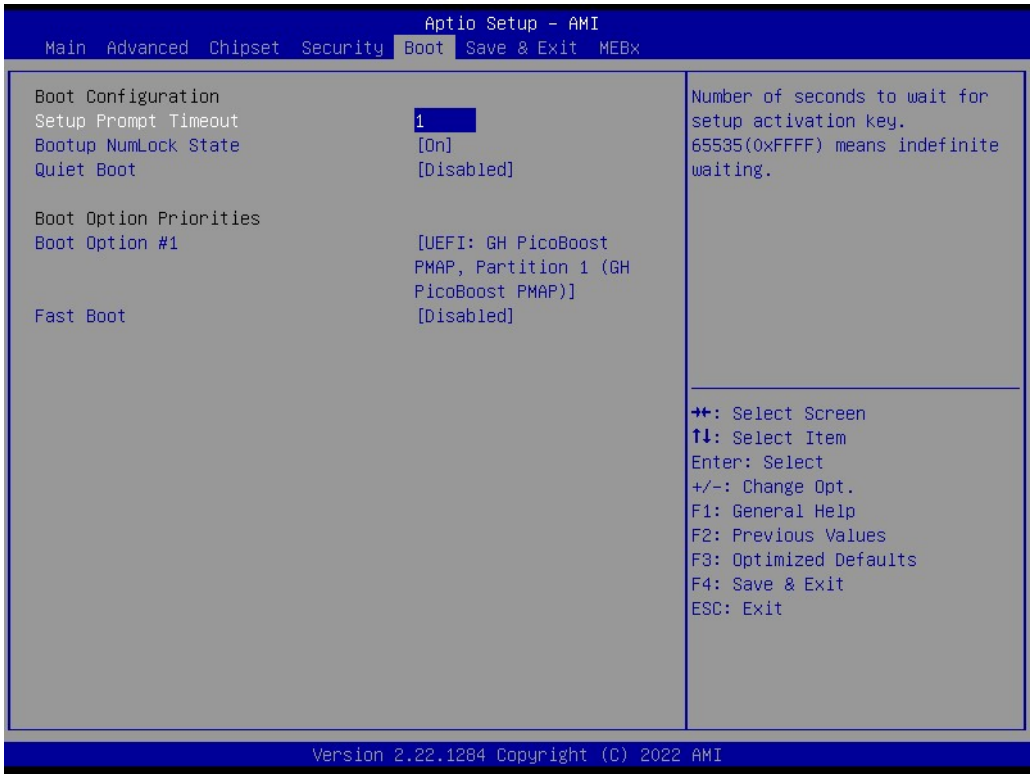


Figure 3.48 Boot Setup

- **Setup Prompt Timeout**
  Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
- **Bootup NumLock State**
  Select the keyboard NumLock state.
- **Quiet Boot**
  Enables or disables Quiet Boot option.
- **Boot Option #1**
  Sets the system boot order.
- **Fast Boot**
  Enable or Disable FastBoot features. Most probes are skipped to reduce time during boot.

3.2.5 Save & Exit

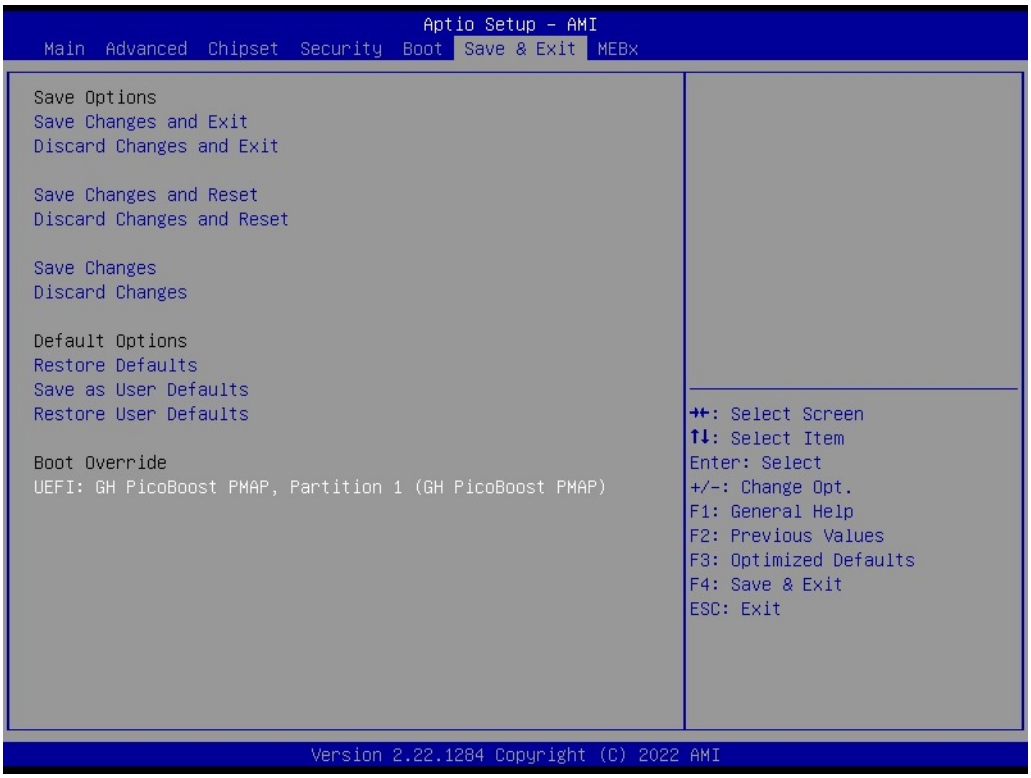


Figure 3.49 Save & Exit

- **Save Changes and Exit**
  Exit system setup after saving the changes.
- **Discard Changes and Exit**
  Exit system setup without saving any changes.
- **Save Changes and Reset**
  Reset the system after saving the changes.
- **Discard Changes and Reset**
  Reset system setup without saving any changes.
- **Save Changes**
  Save Changes done so far to any of the setup options.
- **Discard Changes**
  (005B) Discard Changes done so far to any of the setup options.
- **Restore Defaults**
  Restore/Load Default values for all the setup options.
- **Save as User Defaults**
  Save the changes done so far as User Defaults.
- **Restore User Defaults**
  Restore the User Defaults to all the setup options.
- **Boot Override**

3.2.6 MEBx Login

- **Intel® ME Password**
  MEBx Login.

Chapter 4

S/W Introduction & Installation

Sections include:

- S/W Introduction
- Driver Installation
- Advantech iManager

4.1 S/W Introduction

Advantech Embedded Software Services is dedicated to enriching the quality of life through the fusion of Advantech platforms and Microsoft Windows embedded technology. Our mission involves empowering the embedded computing community by seamlessly integrating Windows Embedded software products into Advantech platforms. By doing so, we relieve customers from the complexities of managing multiple vendors, including hardware suppliers, system integrators, and embedded OS distributors. Ultimately, our objective is to make Windows Embedded Software solutions effortlessly accessible and broadly accessible to the embedded computing community.

4.2 Driver Installation

The Intel Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured.

4.2.1 Windows Driver Setup

To install the drivers on a windows-based OS, please connect to the internet and go to http://support.advantech.com.tw to download the drivers that you want to install and follow Driver Setup instructions to complete the installation.

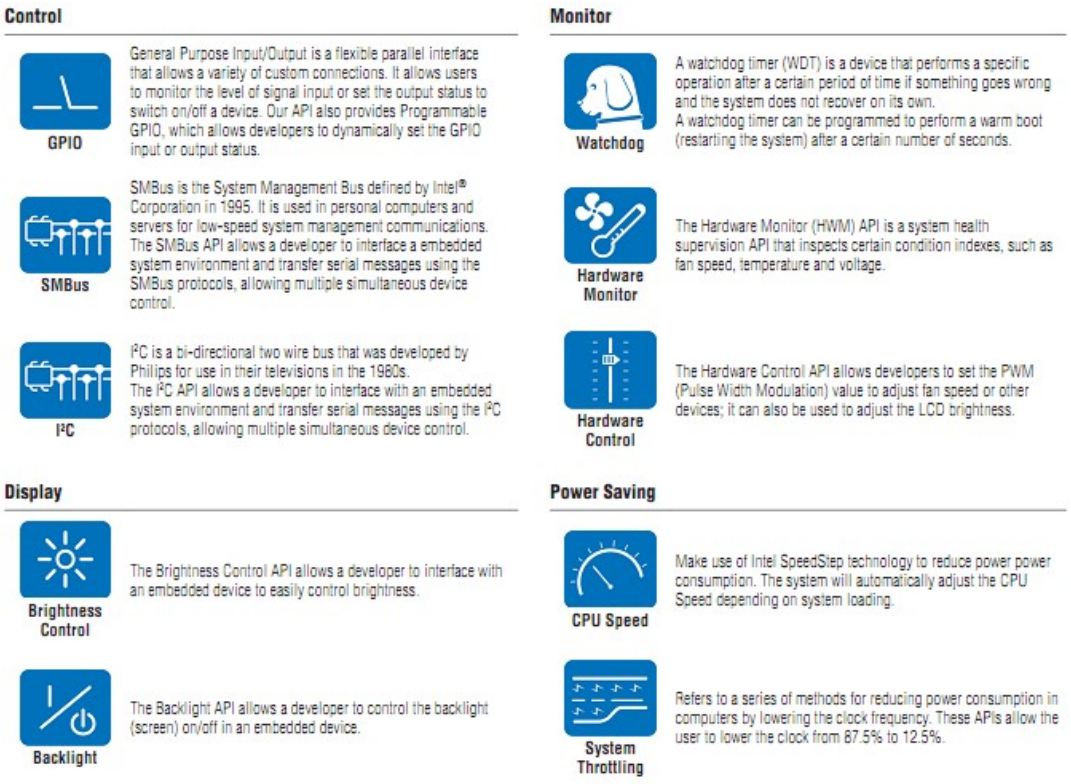
4.2.2 Other OS

Linux Ubuntu

4.3 Advantech iManager

Advantech's platforms come equipped with iManager, a micro-controller that provides embedded features for system integrators. Embedded features have been moved from the OS/BIOS level to the board level, to increase reliability and simplify integration.

iManager runs whether the operating system is running or not; it can count the boot times and running hours of the device, monitor device health, and provide an advanced watchdog to handle errors as they happen. iManager also comes with a secure & encrypted EEPROM for storing important security keys or other customer information. All the embedded functions are configured through the API and provide corresponding utilities to demonstrate. These APIs comply with PICMG EAPI (Embedded Application Programmable Interface) specifications and makes these embedded features easier to integrate, speed development schedules, and provide customer's with software continuity while upgrading hardware. More details of how to use the APIs and utilities, please refer to the Advantech iManager 2.0 Software API User Manual.



Appendix A

Pin Assignment

This appendix details information about the hardware pin assignment of the SOM-C350 CPU System on Module.

Sections include:

- SOM-C350 Client Size Pin Assignment

A.1 SOM-C350 Pin Assignment

This section provides the pin assignment for SOM-C350 on the COM HPC connector, in accordance with the COM-HPC Revision 1.10 Client Type pin-out definitions. For comprehensive information on how to utilize these pins, and to access design guidance, checklists, reference schematics, and additional hardware/software support, we encourage you to reach out to Advantech.

Table A.1: J1 Connector Rows A and B

Pin#	Row A Description	SOM-C350 Difference	Pin#	Row B Description	SOM-C350 Difference
J1.A1	VCC		J1.B1	VCC	
J1.A2	VCC		J1.B2	PWRBTN#	
J1.A3	VCC		J1.B3	VCC	
J1.A4	VCC		J1.B4	THERMTRIP#	
J1.A5	VCC		J1.B5	VCC	
J1.A6	VCC		J1.B6	TAMPER#	
J1.A7	VCC		J1.B7	VCC	
J1.A8	VCC		J1.B8	SUS_S3#	
J1.A9	VCC		J1.B9	VCC	
J1.A10	GND		J1.B10	WD_STROBE#	
J1.A11	BATLOW#		J1.B11	WD_OUT	
J1.A12	PLTRST#		J1.B12	GND	
J1.A13	GND		J1.B13	USB5-	
J1.A14	USB7-		J1.B14	USB5+	
J1.A15	USB7+		J1.B15	GND	
J1.A16	GND		J1.B16	USB4-	
J1.A17	USB6-		J1.B17	USB4+	
J1.A18	USB6+		J1.B18	GND	
J1.A19	GND		J1.B19	I2S_LRCLK/SNDW_CLK3/ HDA_SYNC	
J1.A20	DDI1_SDA_AUX+		J1.B20	I2S_DOUT/SNDW_DAT3/ HDA_SDO	
J1.A21	DDI1_SCL_AUX-		J1.B21	I2S_MCLK/HDA_RST	
J1.A22	GND		J1.B22	I2S_DIN/SNDW_DAT2/ HDA_SDI	
J1.A23	DDI1_PAIR0-		J1.B23	I2S_CLK/SNDW_CLK2/HDA_B-CLK	
J1.A24	DDI1_PAIR0+		J1.B24	VCC_5V_SBY	
J1.A25	GND		J1.B25	USB67_OC#	
J1.A26	DDI1_PAIR1-		J1.B26	USB45_OC#	
J1.A27	DDI1_PAIR1+		J1.B27	USB23_OC#	
J1.A28	GND		J1.B28	USB01_OC#	
J1.A29	DDI1_PAIR2-		J1.B29	SML1_CLK	
J1.A30	DDI1_PAIR2+		J1.B30	SML1_DAT	
J1.A31	GND		J1.B31	PMCALERT#	
J1.A32	DDI1_PAIR3-		J1.B32	SML0_CLK	
J1.A33	DDI1_PAIR3+		J1.B33	SML0_DAT	
J1.A34	GND		J1.B34	USB_PD_ALERT#	
J1.A35	eDP_AUX-/DSI_TX0-		J1.B35	USB_PD_I2C_CLK	
J1.A36	eDP_AUX+/DSI_TX0+		J1.B36	USB_PD_I2C_DAT	
J1.A37	GND		J1.B37	USB_RT_ENA	
J1.A38	eDP_TX0-/DSI_TX1-		J1.B38	USB1_LSRX	NA
J1.A39	eDP_TX0+/DSI_TX1+		J1.B39	USB1_LSTX	NA
J1.A40	GND		J1.B40	USB0_LSRX	NA
J1.A41	eDP_TX1-/DSI_TX2-		J1.B41	USB0_LSTX	NA
J1.A42	eDP_TX1+/DSI_TX2+		J1.B42	GND	
J1.A43	GND		J1.B43	USB0_AUX-	NA
J1.A44	eDP_TX2-/DSI_CLK-		J1.B44	USB0_AUX+	NA

J1.A45	eDP_TX2+/DSI_CLK+	J1.B45	LID#	
J1.A46	GND	J1.B46	SLEEP#	
J1.A47	eDP_TX3-/DSI_TX3-	J1.B47	VCC_BOOT_SPI	
J1.A48	eDP_TX3+/DSI_TX3+	J1.B48	BOOT_SPI_CS#	
J1.A49	GND	J1.B49	BSEL0	
J1.A50	eSPI_IO0	J1.B50	BSEL1	
J1.A51	eSPI_IO1	J1.B51	BSEL2	
J1.A52	eSPI_IO2	J1.B52	eSPI_ALERT0#	
J1.A53	eSPI_IO3	J1.B53	eSPI_ALERT1#	
J1.A54	eSPI_CLK	J1.B54	eSPI_CS0#	
J1.A55	GND	J1.B55	eSPI_CS1#	NA
J1.A56	PCIe_CLKREQ0_LO#	J1.B56	eSPI_RST#	
J1.A57	PCIe_CLKREQ0_HI#	J1.B57	GND	
J1.A58	GND	J1.B58	PCIe_BMC_RX-	
J1.A59	PCIe_BMC_TX-	J1.B59	PCIe_BMC_RX+	
J1.A60	PCIe_BMC_TX+	J1.B60	GND	
J1.A61	GND	J1.B61	PCIe08_RX-	
J1.A62	PCIe08_TX-	J1.B62	PCIe08_RX+	
J1.A63	PCIe08_TX+	J1.B63	GND	
J1.A64	GND	J1.B64	PCIe09_RX-	
J1.A65	PCIe09_TX-	J1.B65	PCIe09_RX+	
J1.A66	PCIe09_TX+	J1.B66	GND	
J1.A67	GND	J1.B67	PCIe10_RX-	
J1.A68	PCIe010_TX-	J1.B68	PCIe10_RX+	
J1.A69	PCIe010_TX+	J1.B69	GND	
J1.A70	GND	J1.B70	PCIe11_RX-	
J1.A71	PCIe11_TX-	J1.B71	PCIe11_RX+	
J1.A72	PCIe11_TX+	J1.B72	GND	
J1.A73	GND	J1.B73	PCIe12_RX-	
J1.A74	PCIe12_TX-	J1.B74	PCIe12_RX+	
J1.A75	PCIe12_TX+	J1.B75	GND	
J1.A76	GND	J1.B76	PCIe13_RX-	
J1.A77	PCIe13_TX-	J1.B77	PCIe13_RX+	
J1.A78	PCIe13_TX+	J1.B78	GND	
J1.A79	GND	J1.B79	PCIe14_RX-	
J1.A80	PCIe14_TX-	J1.B80	PCIe14_RX+	
J1.A81	PCIe14_TX+	J1.B81	GND	
J1.A82	GND	J1.B82	PCIe15_RX-	
J1.A83	PCIe15_TX-	J1.B83	PCIe15_RX+	
J1.A84	PCIe15_TX+	J1.B84	GND	
J1.A85	GND	J1.B85	TEST#	NA
J1.A86	VCC_RTC	J1.B86	RSMRST_OUT#	
J1.A87	SUS_CLK	J1.B87	UART1_TX	
J1.A88	GPIO_00	J1.B88	UART1_RX	
J1.A89	GPIO_01	J1.B89	UART1_RTS#	
J1.A90	GPIO_02	J1.B90	UART1_CTS#	
J1.A91	GPIO_03	J1.B91	IPMB_CLK	NA
J1.A92	GPIO_04	J1.B92	IPMB_DAT	NA
J1.A93	GPIO_05	J1.B93	GP_SPI_MOSI	
J1.A94	GPIO_06	J1.B94	GP_SPI_MISO	
J1.A95	GPIO_07	J1.B95	GP_SPI_CS0#	
J1.A96	GPIO_08	J1.B96	GP_SPI_CS1#	NA
J1.A97	GPIO_09	J1.B97	GP_SPI_CS2#	NA
J1.A98	GPIO_10	J1.B98	GP_SPI_CS3#	NA
J1.A99	GPIO_11	J1.B99	GP_SPI_CLK	
J1.A100	TYPE0	J1.B100	GP_SPI_ALERT#	

Table A.2: J1 Connector Rows C and D

Pin#	Row C Description	SOM-C350 Difference	Pin#	Row D Description	SOM-C350 Difference
J1.C1	VCC		J1.D1	VCC	
J1.C2	RSTBTN#		J1.D2	VCC	
J1.C3	VCC		J1.D3	VCC	
J1.C4	CARRIER_HOT#		J1.D4	VCC	
J1.C5	VCC		J1.D5	VCC	
J1.C6	VIN_PWROK		J1.D6	VCC	
J1.C7	VCC		J1.D7	VCC	
J1.C8	SUS_S4_S5#		J1.D8	VCC	
J1.C9	VCC		J1.D9	VCC	
J1.C10	GND		J1.D10	WAKE0#	
J1.C11	FAN_PWMOUT		J1.D11	WAKE1#	
J1.C12	FAN_TACHIN		J1.D12	GND	
J1.C13	GND		J1.D13	USB1-	
J1.C14	USB3-		J1.D14	USB1+	
J1.C15	USB3+		J1.D15	GND	
J1.C16	GND		J1.D16	USB0-	
J1.C17	USB2-		J1.D17	USB0+	
J1.C18	USB2+		J1.D18	GND	
J1.C19	GND		J1.D19	DDI0_SDA_AUX-	
J1.C20	SNDW_DMIC_CLK1		J1.D20	DDI0_SCL_AUX+	
J1.C21	SNDW_DMIC_DAT1		J1.D21	GND	
J1.C22	GND		J1.D22	DDI0_PAIR0-	
J1.C23	SNDW_DMIC_CLK0		J1.D23	DDI0_PAIR0+	
J1.C24	SNDW_DMIC_DAT0		J1.D24	GND	
J1.C25	GND		J1.D25	DDI0_PAIR1	
J1.C26	DDI0_DDC_AUX_SEL		J1.D26	DDI0_PAIR1+	
J1.C27	DDI1_DDC_AUX_SEL		J1.D27	GND	
J1.C28	DDI0_HPD		J1.D28	DDI0_PAIR2-	
J1.C29	DDI1_HPD		J1.D29	DDI0_PAIR2+	
J1.C30	eDP_HPD/DSI_HPD		J1.D30	GND	
J1.C31	eDP_VDD_EN/DSI_VDD_EN		J1.D31	DDI0_PAIR3-	
J1.C32	eDP_BKLT_EN/DSI_BKLT_EN		J1.D32	DDI0_PAIR3+	
J1.C33	eDP_BKLT_CTL/DSI_B-KLT_CTL		J1.D33	GND	
J1.C34	GND		J1.D34	AC_PRESENT	
J1.C35	USB1_AUX-	NA	J1.D35	RSVD	
J1.C36	USB1_AUX+	NA	J1.D36	GND	
J1.C37	GND		J1.D37	USB1_SSTX0-	
J1.C38	USB1_SSRX0-	?	J1.D38	USB1_SSTX0+	
J1.C39	USB1_SSRX0+		J1.D39	GND	
J1.C40	GND		J1.D40	USB1_SSTX1-	
J1.C41	USB1_SSRX1-		J1.D41	USB1_SSTX1+	
J1.C42	USB1_SSRX1+		J1.D42	GND	
J1.C43	GND		J1.D43	USB0_SSTX0-	
J1.C44	USB0_SSRX0-		J1.D44	USB0_SSTX0+	
J1.C45	USB0_SSRX0+		J1.D45	GND	
J1.C46	GND		J1.D46	USB0_SSTX1-	
J1.C47	USB0_SSRX1-		J1.D47	USB0_SSTX1+	
J1.C48	USB0_SSRX1+		J1.D48	GND	
J1.C49	GND		J1.D49	SATA0_RX-	
J1.C50	BOOT_SPI_IO0		J1.D50	SATA0_RX+	
J1.C51	BOOT_SPI_IO1		J1.D51	GND	
J1.C52	BOOT_SPI_IO2		J1.D52	SATA0_TX-	
J1.C53	BOOT_SPI_IO3		J1.D53	SATA0_TX+	
J1.C54	BOOT_SPI_CLK		J1.D54	GND	
J1.C55	GND		J1.D55	SATA1_RX-	

J1.C56	PCIe_REFCLK0_HI-	J1.D56	SATA1_RX+
J1.C57	PCIe_REFCLK0_HI+	J1.D57	GND
J1.C58	GND	J1.D58	SATA1_TX-
J1.C59	PCIe_REFCLK0_LO-	J1.D59	SATA1_TX+
J1.C60	PCIe_REFCLK0_LO+	J1.D60	GND
J1.C61	GND	J1.D61	PCIe00_TX-
J1.C62	PCIe00_RX-	J1.D62	PCIe00_TX+
J1.C63	PCIe00_RX+	J1.D63	GND
J1.C64	GND	J1.D64	PCIe01_TX-
J1.C65	PCIe01_RX-	J1.D65	PCIe01_TX+
J1.C66	PCIe01_RX+	J1.D66	GND
J1.C67	GND	J1.D67	PCIe02_TX-
J1.C68	PCIe02_RX-	J1.D68	PCIe02_TX+
J1.C69	PCIe02_RX+	J1.D69	GND
J1.C70	GND	J1.D70	PCIe03_TX-
J1.C71	PCIe03_RX-	J1.D71	PCIe03_TX+
J1.C72	PCIe03_RX+	J1.D72	GND
J1.C73	GND	J1.D73	PCIe04_TX-
J1.C74	PCIe04_RX-	J1.D74	PCIe04_TX+
J1.C75	PCIe04_RX+	J1.D75	GND
J1.C76	GND	J1.D76	PCIe05_TX-
J1.C77	PCIe05_RX-	J1.D77	PCIe05_TX+
J1.C78	PCIe05_RX+	J1.D78	GND
J1.C79	GND	J1.D79	PCIe06_TX-
J1.C80	PCIe06_RX-	J1.D80	PCIe06_TX+
J1.C81	PCIe06_RX+	J1.D81	GND
J1.C82	GND	J1.D82	PCIe07_TX-
J1.C83	PCIe07_RX-	J1.D83	PCIe07_TX+
J1.C84	PCIe07_RX+	J1.D84	GND
J1.C85	GND	J1.D85	NBASET0_MDI0-
J1.C86	SMB_CLK	J1.D86	NBASET0_MDI0+
J1.C87	SMB_DAT	J1.D87	GND
J1.C88	SMB_ALERT#	J1.D88	NBASET0_MDI1-
J1.C89	UART0_TX	J1.D89	NBASET0_MDI1+
J1.C90	UART0_RX	J1.D90	GND
J1.C91	UART0_RTS#	J1.D91	NBASET0_MDI2-
J1.C92	UART0_CTS#	J1.D92	NBASET0_MDI2+
J1.C93	I2C0_CLK	J1.D93	GND
J1.C94	I2C0_DAT	J1.D94	NBASET0_MDI3-
J1.C95	I2C0_ALERT#	J1.D95	NBASET0_MDI3+
J1.C96	I2C1_CLK	J1.D96	GND
J1.C97	I2C1_DAT	J1.D97	NBASET0_LINK_MAX#
J1.C98	NBASET0_SDP	J1.D98	NBASET0_LINK_MID#
J1.C99	NBASET0_CTREF	J1.D99	NBASET0_LINK_ACT#
J1.C100	TYPE1	J1.D100	TYPE2

Table A.3: J1 Connector Rows E and F

Pin#	Row E Description	SOM-C350 Difference	Pin#	Row F Description	SOM-C350 Difference
J2.E1	RAPID_SHUTDOWN		J2.F1	FUSA_STATUS0	NA
J2.E2	GND		J2.F2	FUSA_STATUS1	NA
J2.E3	DDI2_SDA_AUX-		J2.F3	FUSA_ALERT#	NA
J2.E4	DDI2_SCL_AUX+		J2.F4	FUSA_SPI_CS#	NA
J2.E5	GND		J2.F5	FUSA_SPI_CLK	NA
J2.E6	DDI2_PAIR0-		J2.F6	FUSA_SPI_MISO	NA
J2.E7	DDI2_PAIR0+		J2.F7	FUSA_SPI_MOSI	NA
J2.E8	GND		J2.F8	FUSA_SPI_ALERT	NA
J2.E9	DDI2_PAIR1-		J2.F9	FUSA_VOLTAGE_ERR#	NA
J2.E10	DDI2_PAIR1+		J2.F10	PROCHOT#	NA
J2.E11	GND		J2.F11	CATERR#	NA
J2.E12	DDI2_PAIR2-		J2.F12	RSVD	
J2.E13	DDI2_PAIR2+		J2.F13	RSVD	
J2.E14	GND		J2.F14	RSVD	
J2.E15	DDI2_PAIR3-		J2.F15	RSVD	
J2.E16	DDI2_PAIR3+		J2.F16	RSVD	
J2.E17	GND		J2.F17	RSVD	
J2.E18	DDI2_DDC_AUX_SEL		J2.F18	RSVD	
J2.E19	DDI2_HPD		J2.F19	GND	
J2.E20	GND		J2.F20	PCIe32_RX-	
J2.E21	PCIe32_TX-		J2.F21	PCIe32_RX+	
J2.E22	PCIe32_TX+		J2.F22	GND	
J2.E23	GND		J2.F23	PCIe33_RX-	
J2.E24	PCIe33_TX-		J2.F24	PCIe33_RX+	
J2.E25	PCIe33_TX+		J2.F25	GND	
J2.E26	GND		J2.F26	PCIe34_RX-	
J2.E27	PCIe34_TX-		J2.F27	PCIe34_RX+	
J2.E28	PCIe34_TX+		J2.F28	GND	
J2.E29	GND		J2.F29	PCIe35_RX-	
J2.E30	PCIe35_TX-		J2.F30	PCIe35_RX+	
J2.E31	PCIe35_TX+		J2.F31	GND	
J2.E32	GND		J2.F32	PCIe36_RX-	
J2.E33	PCIe36_TX-		J2.F33	PCIe36_RX+	
J2.E34	PCIe36_TX+		J2.F34	GND	
J2.E35	GND		J2.F35	PCIe37_RX-	
J2.E36	PCIe37_TX-		J2.F36	PCIe37_RX+	
J2.E37	PCIe37_TX+		J2.F37	GND	
J2.E38	GND		J2.F38	PCIe38_RX-	
J2.E39	PCIe38_TX-		J2.F39	PCIe38_RX+	
J2.E40	PCIe38_TX+		J2.F40	GND	
J2.E41	GND		J2.F41	PCIe39_RX-	

J2.E42	PCIe39_TX-		J2.F42	PCIe39_RX+	
J2.E43	PCIe39_TX+		J2.F43	GND	
J2.E44	GND		J2.F44	PCIe16_RX-	
J2.E45	PCIe16_TX-		J2.F45	PCIe16_RX+	
J2.E46	PCIe16_TX+		J2.F46	GND	
J2.E47	GND		J2.F47	PCIe17_RX-	
J2.E48	PCIe17_TX-		J2.F48	PCIe17_RX+	
J2.E49	PCIe17_TX+		J2.F49	GND	
J2.E50	GND		J2.F50	PCIe18_RX-	
J2.E51	PCIe18_TX-		J2.F51	PCIe18_RX+	
J2.E52	PCIe18_TX+		J2.F52	GND	
J2.E53	GND		J2.F53	PCIe19_RX-	
J2.E54	PCIe19_TX-		J2.F54	PCIe19_RX+	
J2.E55	PCIe19_TX+		J2.F55	GND	
J2.E56	GND		J2.F56	PCIe20_RX-	
J2.E57	PCIe20_TX-		J2.F57	PCIe20_RX+	
J2.E58	PCIe20_TX+		J2.F58	GND	
J2.E59	GND		J2.F59	PCIe21_RX-	
J2.E60	PCIe21_TX-		J2.F60	PCIe21_RX+	
J2.E61	PCIe21_TX+		J2.F61	GND	
J2.E62	GND		J2.F62	PCIe22_RX-	
J2.E63	PCIe22_TX-		J2.F63	PCIe22_RX+	
J2.E64	PCIe22_TX+		J2.F64	GND	
J2.E65	GND		J2.F65	PCIe23_RX-	
J2.E66	PCIe23_TX-		J2.F66	PCIe23_RX+	
J2.E67	PCIe23_TX+		J2.F67	GND	
J2.E68	GND		J2.F68	RSVD	
J2.E69	RSVD		J2.F69	RSVD	
J2.E70	RSVD		J2.F70	GND	
J2.E71	RSVD		J2.F71	NBASET1_MDI0-	
J2.E72	RSVD		J2.F72	NBASET1_MDI0+	
J2.E73	RSVD		J2.F73	GND	
J2.E74	RSVD		J2.F74	NBASET1_MDI1-	
J2.E76	RSVD		J2.F76	GND	
J2.E77	RSVD		J2.F77	NBASET1_MDI2-	
J2.E78	NBASET1_CTREF		J2.F78	NBASET1_MDI2+	
J2.E79	NBASET1_SDP		J2.F79	GND	
J2.E80	NBASET1_LINK_MID#		J2.F80	NBASET1_MDI3-	
J2.E81	NBASET1_LINK_ACT#		J2.F81	NBASET1_MDI3+	
J2.E82	NBASET1_LINK_MAX#		J2.F82	GND	
J2.E83	GND	?	J2.F83	RSVD	
J2.E84	RSVD		J2.F84	RSVD	
J2.E85	RSVD		J2.F85	GND	
J2.E86	GND		J2.F86	ETH0_TX-	NA
J2.E87	ETH0_RX-	NA	J2.F87	ETH0_TX+	NA

J2.E88	ETH0_RX+	NA	J2.F88	GND	
J2.E89	GND		J2.F89	ETH1_TX-	NA
J2.E90	ETH1_RX-	NA	J2.F90	ETH1_TX+	NA
J2.E91	ETH1_RX+	NA	J2.F91	GND	
J2.E92	GND		J2.F92	PCIe_REFCLK2-	
J2.E93	PCIe_REFCLK1-		J2.F93	PCIe_REFCLK2+	
J2.E94	PCIe_REFCLK1+		J2.F94	GND	
J2.E95	GND		J2.F95	RSVD	
J2.E96	PCIe_CLKREQ1#		J2.F96	ETH0-1_PRSNT#	NA
J2.E97	PCIe_CLKREQ2#		J2.F97	ETH0-1_PHY_RST#	NA
J2.E98	PCIe_CLKREQ_OUT0#		J2.F98	ETH0_SDP	NA
J2.E99	PCIe_CLKREQ_OUT1#		J2.F99	ETH1_SDP	NA
J2.E100	PCIe_PERST_IN0#		J2.F100	PCIe_PERST_IN1#	

Table A.4: J1 Connector Rows G and H

Pin#	Row G Description	SOM-C350 Difference	Pin#	Row H Description	SOM-C350 Difference
J2.G1	VCC_5V_SBY		J2.H1	GND	
J2.G2	GND		J2.H2	USB2_SSTX0-	
J2.G3	USB2_SSRX0-		J2.H3	USB2_SSTX0+	
J2.G4	USB2_SSRX0+		J2.H4	GND	
J2.G5	GND		J2.H5	USB2_SSTX1-	
J2.G6	USB2_SSRX1-		J2.H6	USB2_SSTX1+	
J2.G7	USB2_SSRX1+		J2.H7	GND	
J2.G8	GND		J2.H8	USB3_SSTX0-	
J2.G9	USB3_SSRX0-		J2.H9	USB3_SSTX0+	
J2.G10	USB3_SSRX0+		J2.H10	GND	
J2.G11	GND		J2.H11	USB3_SSTX1-	
J2.G12	USB3_SSRX1-		J2.H12	USB3_SSTX1+	
J2.G13	USB3_SSRX1+		J2.H13	GND	
J2.G14	GND		J2.H14	USB2_AUX-	NA
J2.G15	USB3_LSRX	NA	J2.H15	USB2_AUX+	NA
J2.G16	USB3_LSTX	NA	J2.H16	GND	
J2.G17	USB2_LSRX	NA	J2.H17	USB3_AUX-	NA
J2.G18	USB2_LSTX	NA	J2.H18	USB3_AUX+	NA
J2.G19	PEG_LANE_REV#		J2.H19	GND	
J2.G20	GND		J2.H20	PCIe40_TX-	
J2.G21	PCIe40_RX-		J2.H21	PCIe40_TX+	
J2.G22	PCIe40_RX+		J2.H22	GND	
J2.G23	GND		J2.H23	PCIe41_TX-	
J2.G24	PCIe41_RX-		J2.H24	PCIe41_TX+	
J2.G25	PCIe41_RX+		J2.H25	GND	
J2.G26	GND		J2.H26	PCIe42_TX-	NA
J2.G27	PCIe42_RX-	NA	J2.H27	PCIe42_TX+	NA
J2.G28	PCIe42_RX+	NA	J2.H28	GND	
J2.G29	GND		J2.H29	PCIe43_TX-	NA
J2.G30	PCIe43_RX-	NA	J2.H30	PCIe43_TX+	NA
J2.G31	PCIe43_RX+	NA	J2.H31	GND	
J2.G32	GND		J2.H32	PCIe44_TX-	NA
J2.G33	PCIe44_RX-	NA	J2.H33	PCIe44_TX+	NA
J2.G34	PCIe44_RX+	NA	J2.H34	GND	
J2.G35	GND		J2.H35	PCIe45_TX-	NA
J2.G36	PCIe45_RX-	NA	J2.H36	PCIe45_TX+	NA
J2.G37	PCIe45_RX+	NA	J2.H37	GND	

J2.G38	GND		J2.H38	PCIe46_TX-	NA
J2.G39	PCIe46_RX-	NA	J2.H39	PCIe46_TX+	NA
J2.G40	PCIe46_RX+	NA	J2.H40	GND	
J2.G41	GND		J2.H41	PCIe47_TX-	NA
J2.G42	PCIe47_RX-	NA	J2.H42	PCIe47_TX+	NA
J2.G43	PCIe47_RX+	NA	J2.H43	GND	
J2.G44	GND		J2.H44	PCIe24_TX-	
J2.G45	PCIe24_RX-		J2.H45	PCIe24_TX+	
J2.G46	PCIe24_RX+		J2.H46	GND	
J2.G47	GND		J2.H47	PCIe25_TX-	
J2.G48	PCIe25_RX-		J2.H48	PCIe25_TX+	
J2.G49	PCIe25_RX+		J2.H49	GND	
J2.G50	GND		J2.H50	PCIe26_TX-	
J2.G51	PCIe26_RX-		J2.H51	PCIe26_TX+	
J2.G52	PCIe26_RX+		J2.H52	GND	
J2.G53	GND		J2.H53	PCIe27_TX-	
J2.G54	PCIe27_RX-		J2.H54	PCIe27_TX+	
J2.G55	PCIe27_RX+		J2.H55	GND	
J2.G56	GND		J2.H56	PCIe28_TX-	
J2.G57	PCIe28_RX-		J2.H57	PCIe28_TX+	
J2.G58	PCIe28_RX+		J2.H58	GND	
J2.G59	GND		J2.H59	PCIe29_TX-	
J2.G60	PCIe29_RX-		J2.H60	PCIe29_TX+	
J2.G61	PCIe29_RX+		J2.H61	GND	
J2.G62	GND		J2.H62	PCIe30_TX-	
J2.G63	PCIe30_RX-		J2.H63	PCIe30_TX+	
J2.G64	PCIe30_RX+		J2.H64	GND	
J2.G65	GND		J2.H65	PCIe31_TX-	
J2.G66	PCIe31_RX-		J2.H66	PCIe31_TX+	
J2.G67	PCIe31_RX+		J2.H67	GND	
J2.G68	GND		J2.H68	RSVD	
J2.G69	RSVD		J2.H69	RSVD	
J2.G70	RSVD		J2.H70	GND	
J2.G71	GND		J2.H71	CSI1_RX0-	NA
J2.G72	CSI0_RX0-	NA	J2.H72	CSI1_RX0+	NA
J2.G73	CSI0_RX0+	NA	J2.H73	GND	
J2.G74	GND		J2.H74	CSI1_RX1-	NA
J2.G75	CSI0_RX1-	NA	J2.H75	CSI1_RX1+	NA
J2.G76	CSI0_RX1+	NA	J2.H76	GND	
J2.G77	GND		J2.H77	CSI1_RX2-	NA
J2.G78	CSI0_RX2-	NA	J2.H78	CSI1_RX2+	NA
J2.G79	CSI0_RX2+	NA	J2.H79	GND	
J2.G80	GND		J2.H80	CSI1_RX3-	NA
J2.G81	CSI0_RX3-	NA	J2.H81	CSI1_RX3+	NA
J2.G82	CSI0_RX3+	NA	J2.H82	GND	
J2.G83	GND		J2.H83	CSI1_CLK-	NA
J2.G84	CSI0_CLK-	NA	J2.H84	CSI1_CLK+	NA
J2.G85	CSI0_CLK+	NA	J2.H85	GND	
J2.G86	GND		J2.H86	CSI1_I2C_CLK	NA
J2.G87	CSI0_I2C_CLK	NA	J2.H87	CSI1_I2C_DAT	NA
J2.G88	CSI0_I2C_DAT	NA	J2.H88	CSI1_MCLK	NA
J2.G89	CSI0_MCLK	NA	J2.H89	CSI1_RST#	NA
J2.G90	CSI0_RST#	NA	J2.H90	CSI1_ENA	NA
J2.G91	CSI0_ENA	NA	J2.H91	GND	
J2.G92	GND		J2.H92	PCIe_REFCLKIN0-	NA
J2.G93	RSVD		J2.H93	PCIe_REFCLKIN0+	NA
J2.G94	RSVD		J2.H94	GND	
J2.G95	GND		J2.H95	PCIe_REFCLKIN1-	NA
J2.G96	ETH0-1_I2C_CLK	NA	J2.H96	PCIe_REFCLKIN1+	NA
J2.G97	ETH0-1_I2C_DAT	NA	J2.H97	GND	

J2.G98	ETH0-1_PHY_INT#	NA	J2.H98	ETH0-1_MDIO_CLK	NA
J2.G99	ETH0-1_INT#	NA	J2.H99	ETH0-1_MDIO_DAT	NA
J2.G100	PCIe_WAKE_OUT0#		J2.H100	PCIe_WAKE_OUT1#	

Appendix B

Watchdog Timer

This appendix details information about the watchdog timer programming on the SOM-C350 CPU System on Module.

Sections include:

- Watchdog Timer Programming

B.1 Programming the Watchdog Timer

Table B.1: Programming the Watchdog Timer

Trigger Event	Note
IRQ	BIOS setting default disable**
NMI	N/A
SCI	Power button event
Power Off	Support
H/W Restart	Support
External WDT	Support

Note!

The updated Watchdog Timer driver now offers automatic IRQ number selection from the BIOS and configuration in the EC. This feature is exclusively supported in Windows 8.1 and Windows 10.

In alternative operating systems, the IRQ number will continue to be determined based on the BIOS settings, following the usual procedure. For more in-depth information, please consult the iManager & Software API User Manual.

Appendix C

Programming GPIO

This Appendix details illustration of the General Purpose Input and Output pin settings.

Sections include:

- GPIO Register

C.1 GPIO Register

Table C.1: GPIO Register

GPIO Byte Mapping	H/W Pin Name
BIT0	GPI0
BIT1	GPI1
BIT2	GPI2
BIT3	GPI3
BIT4	GPI4
BIT5	GPI5
BIT6	GPI6
BIT7	GPI7
BIT8	GPI8
BIT9	GPI9
BIT10	GPI10
BIT11	GPI11

For details, please refer to *iManager & Software API User Manual*.
https://github.com/ADVANTECH-Corp/SUSI

Appendix D

System Assignments

This appendix gives you the information about the system resource allocation on the SOM-C350 CPU System on Module.

Sections include:

- System I/O ports
- Interrupt Assignments
- 1st MB Memory Map

D.1 System I/O Ports

Table D.1: System I/O Ports

Addr.Range(Hex)	Device
0x00000299-0x0000029A	Motherboard resources
0x000002C0-0x000002DF	Motherboard resources
0x000002A0-0x000002BF	Motherboard resources
0x000002A0-0x000002BF	Motherboard resources
0x00000290-0x0000029F	Motherboard resources
0x0000029E-0x000002AD	Motherboard resources
0x00000060-0x0000006F	Motherboard resources
0x00000200-0x0000027F	Motherboard resources
0x00000300-0x0000037F	Motherboard resources
0x00000280-0x0000028F	Motherboard resources
0x00000280-0x0000028F	Motherboard resources
0x000002F0-0x000002F7	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x00000062-0x00000062	Microsoft ACPI-Compliant Embedded Controller
0x00000066-0x00000066	Microsoft ACPI-Compliant Embedded Controller
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x00001854-0x00001857	Motherboard resources
0x00003090-0x00003097	Standard SATA AHCI Controller
0x00003080-0x00003083	Standard SATA AHCI Controller
0x00003060-0x0000307F	Standard SATA AHCI Controller
0x00000000-0x00000CF7	PCI Express Root Complex
0x00000D00-0x0000FFFF	PCI Express Root Complex
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller

Table D.1: System I/O Ports	
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x00002000-0x000020FE	Motherboard resources
0x000000F0-0x000000F0	Numeric data processor
0x0000FFF8-0x0000FFFF	Intel(R) Active Management Technology - SOL (COM3)
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer
0x00003000-0x0000303F	Intel(R) UHD Graphics 770

D.2 Interrupt Assignments

Table D.2: Interrupt Assignments	
Interrupt#	**Interrupt Source**
IRQ0	System timer
IRQ 27	Intel(R) Serial IO I2C Host Controller - 43E8
IRQ 4294967294	Intel(R) PCI Express Root Port #5 - 43BC
IRQ 4	Communications Port (COM1)
IRQ 3	Communications Port (COM2)
IRQ 14	Intel(R) Serial IO GPIO Host Controller - INT34C6
IRQ 6	Motherboard resources
IRQ 4294967293	Standard SATA AHCI Controller
IRQ54-68	Microsoft ACPI-Compliant System
IRQ69	Trusted Platform Module 2.0
IRQ70-511	Microsoft ACPI-Compliant System
IRQ13	Numeric data processor
IRQ 19	Intel(R) Active Management Technology - SOL (COM3)
IRQ 16	High Definition Audio Controller
IRQ 4294967281	Intel(R) Ethernet Controller (3) I225-LM
IRQ 4294967291	Intel(R) UHD Graphics
IRQ 4294967280	Intel(R) Management Engine Interface #1

D.3 1st MB Memory Map

Table D.3: 1st MB Memory Map

Addr. Range (Hex)	Device
0xFFEFA000-0xFFEFAFFF	Intel(R) Serial IO I2C Host Controller - 43E8
0xFEDC0000-0xFEDC7FFF	Motherboard resources
0xFEDA0000-0xFEDA0FFF	Motherboard resources
0xFEDA1000-0xFEDA1FFF	Motherboard resources
0xC0000000-0xCFFFFFFF	Motherboard resources
0xFED20000-0xFED7FFFF	Motherboard resources
0xFED90000-0xFED93FFF	Motherboard resources
0xFED45000-0xFED8FFFF	Motherboard resources
0xFEE00000-0xFEEFFFFF	Motherboard resources
0x50400000-0x506FFFFF	Intel(R) PCI Express Root Port #5 - 43BC
0x50400000-0x506FFFFF	PCI Express Root Complex
0x1128000-0x11280FF	Intel(R) SMBus - 43A3
0xFED00000-0xFED003FF	High precision event timer
0xFE000000-0xFE01FFFF	Motherboard resources
0xFE04C000-0xFE04FFFF	Motherboard resources
0xFE050000-0xFE0AFFFF	Motherboard resources
0xFE0D0000-0xFE0FFFFF	Motherboard resources
0xFE200000-0xFE7FFFFF	Motherboard resources
0xFF000000-0xFFFFFFFF	Motherboard resources
0xFD000000-0xFD68FFFF	Motherboard resources
0xFD6C0000-0xFD6CFFFF	Motherboard resources
0xFD6F0000-0xFDFFFFFF	Motherboard resources
0xFD6E0000-0xFD6EFFFF	Intel(R) Serial IO GPIO Host Controller - INT34C6
0xFD6D0000-0xFD6DFFFF	Intel(R) Serial IO GPIO Host Controller - INT34C6
0xFD6B0000-0xFD6BFFFF	Intel(R) Serial IO GPIO Host Controller - INT34C6
0xFD6A0000-0xFD6AFFFF	Intel(R) Serial IO GPIO Host Controller - INT34C6
0xFD690000-0xFD69FFFF	Intel(R) Serial IO GPIO Host Controller - INT34C6
0x50700000-0x50701FFF	Standard SATA AHCI Controller
0x50703000-0x507030FF	Standard SATA AHCI Controller
0x50702000-0x507027FF	Standard SATA AHCI Controller
0xA0000-0xBFFFF	PCI Express Root Complex
0xE0000-0xE3FFF	PCI Express Root Complex
0xE4000-0xE7FFF	PCI Express Root Complex
0xE8000-0xEBFFF	PCI Express Root Complex
0xEC000-0xEFFFF	PCI Express Root Complex
0xF0000-0xFFFFF	PCI Express Root Complex
0x1100000-0x110FFFF	Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
0xFED40000-0xFED44FFF	Trusted Platform Module 2.0
0xFE010000-0xFE010FFF	Intel(R) SPI (flash) Controller - 43A4
0xBFFFF000-0xBFFFFFFF	Intel(R) Active Management Technology - SOL (COM3)
0xFFEFC000-0xFFEFFFFF	High Definition Audio Controller
0xFFF00000-0xFFFFFFFF	High Definition Audio Controller

Table D.3: 1st MB Memory Map	
0x1110000-0x111FFFF	Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
0x50500000-0x505FFFFF	Intel(R) Ethernet Controller (3) I225-LM
0x50600000-0x50603FFF	Intel(R) Ethernet Controller (3) I225-LM
0x0000-0xFFFFFF	Intel(R) UHD Graphics
0x0000-0xFFFFFFF	Intel(R) UHD Graphics
0xFFEFB000-0xFFEFBFFF	Intel(R) Management Engine Interface #1
0xFFEFA000-0xFFEFAFFF	Intel(R) Serial IO I2C Host Controller - 43E8

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All product specifications are subject to change without notice.