

Approval Sheet

Customer	
Product Number	M3UW-2GSFACN9-I
Module speed	PC3-10600
Pin	240 pin
Cl-tRCD-tRP	9-9-9
SDRAM Operating Temp	0°C~85°C
Date	9 th January 2016

Approval by Customer

P/N:

Signature:

Date:

Sales: _____

Sr. Technical Manager: John Hsieh

Rev 1.0

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)
		CL=7	CL=9	CL=11			
PC3-10600	N	1066	1333	1333	13.5	13.5	13.5

- JEDEC Standard 240-pin Dual In-Line Memory Module
- Intend for PC3-10600 applications
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.5 Volt (+/-0.075)
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8 μ s ($T_c \leq +85^{\circ}\text{C}$)
- 14/10/2 Addressing (row/column/rank)-2GB
- SDRAM operating temperature range $0^{\circ}\text{C} \leq T_c \leq +85^{\circ}\text{C}$
- Programmable Device Operation:
 - Burst Type: Sequential or Interleave
 - Device CAS# Latency: 9
 - Burst Length: switch on-the-fly: BL=8 or BC 4
- RoHS Compliant (*Section 12*)

2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +65	°C	1
TSTG	Storage Temperature	-50 to +100	°C	
HOPR	Operating Humidity (relative)	10 to 90	%	
HSTG	Storage Humidity (without condensation)	5 to 95	%	
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2
1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification. 2. Up to 9850 ft.				

3. DRAM Parameters by device density

RTT_Nom Setting	Parameter		1Gb	Units
tRFC	REF command ACT or REF command time		110	ns
tREFI	Average periodic refresh interval	$0^{\circ}\text{C} \leq \text{T}_{\text{CASE}} \leq 85^{\circ}\text{C}$	7.8	μs
		$85^{\circ}\text{C} \leq \text{T}_{\text{CASE}} \leq 95^{\circ}\text{C}$	3.9	μs

4. Ordering Information

DDR3 UDIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M3UW-2GSFACN9-I	2GB	PC3-10600	256Mx64	16	2	N

5. Pin Configurations (Front side/Back side)

X64 UDIMM

DDRIII-240pins DIMM Front								DDRIII-240pins DIMM Back							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	31	DQ26	61	A2	91	DQ41	121	VSS	161	VSS	181	A1	211	VSS
2	VSS	32	VSS	62	VDD	92	VSS	122	DQ4	162	DM3	182	VDD	212	DM6
3	DQ0	33	/DQ83	63	CK1/NC	93	/DQ85	123	DQ6	163	NC	183	VDD	213	NC
4	DQ1	34	DQ83	64	/CK1/NC	94	DQ85	124	VSS	164	VSS	184	CK0	214	VSS
5	VSS	35	VSS	65	VDD	95	VSS	125	DM0	165	DQ30	185	/CK0	215	DQ48
6	/DQ80	36	DQ28	66	VDD	96	DQ42	126	NC	166	DQ31	186	VDD	216	DQ47
7	DQ80	37	DQ27	67	VREFCA	97	DQ43	127	VSS	167	VSS	187	NC	217	VSS
8	VSS	38	VSS	68	NC	98	VSS	128	DQ8	168	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	VDD	99	DQ48	129	DQ7	169	CB5	189	VDD	219	DQ53
10	DQ3	40	CB1	70	A10	100	DQ49	130	VSS	180	VSS	190	BA1	220	VSS
11	VSS	41	VSS	71	BA0/BA1	101	VSS	131	DQ12	181	DM8	191	VDD	221	DM8
12	DQ8	42	NC, /DQ88	72	VDD	102	/DQ88	132	DQ13	182	NC	192	RA3	222	NC
13	DQ9	43	NC DQ88	73	WE	103	DQ88	133	VSS	183	VSS	193	CB0	223	VSS
14	VSS	44	VSS	74	CA3	104	VSS	134	DM1	184	CB8	194	VDD	224	DQ54
15	/DQ81	45	CB2	75	VDD	105	DQ50	135	NC	185	CB7	195	ODT0	225	DQ55
16	DQ81	46	CB3	76	CS1	106	DQ51	136	VSS	186	VSS	196	A13	226	VSS
17	VSS	47	VSS	77	ODT1	107	VSS	137	DQ14	187	NC,TEST	197	VDD	227	DQ80
18	DQ10	48	NC	78	VDD	108	DQ58	138	DQ15	188	RESET	198	NC	228	DQ81
19	DQ11	49	NC	79	NC/SA2	109	DQ57	139	VSS	189	NC CKE1	199	VSS	229	VSS
20	VSS	50	CKE0	80	VSS	110	VSS	140	DQ20	170	VDD	200	DQ38	230	DM7
21	DQ16	51	VDD	81	DQ32	111	/DQ87	141	DQ21	171	A15/BA3	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQ87	142	VSS	172	A14	202	VSS	232	VSS
23	VSS	53	NC	83	VSS	113	VSS	143	DM2	173	VDD	203	DM4	233	DQ82
24	/DQ82	54	VDD	84	/DQ84	114	DQ58	144	NC	174	A12/NC	204	NC	234	DQ83
25	DQ82	55	A11	85	DQ84	115	DQ59	145	VSS	175	A9	205	VSS	235	VSS
26	VSS	56	A7	86	VSS	116	VSS	146	DQ22	176	VDD	206	DQ38	236	VDD8PD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A6	88	DQ35	118	SCL	148	VSS	178	A8	208	VSS	238	SDA
29	VSS	59	A4	89	VSS	119	VSS	149	DQ28	179	VDD	209	DQ44	239	VSS
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

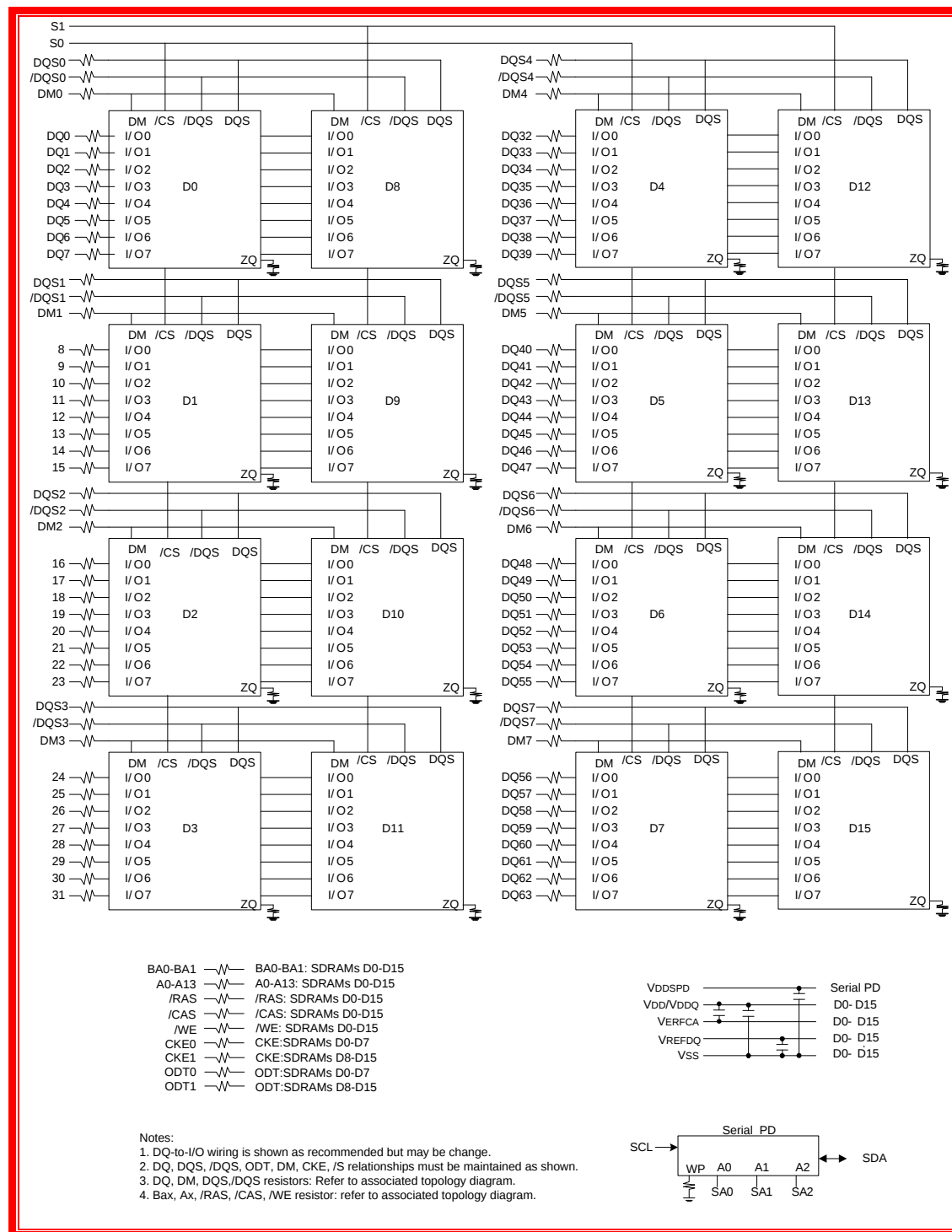
6. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
/RAS	SDRAM row address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
/CAS	SDRAM column address strobe	V _{DD}	Power Supply
/WE	SDRAM write enable	V _{DDID}	V _{DD} Identification Flag
/S0 - /S1	DIMM Rank Select Lines	V _{DDQ}	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	V _{REFDQ}	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	V _{REFCA}	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	V _{SS}	Ground
DQS0 – DQS8 /DQS0-/DQS8	SDRAM data strobes	V _{DDSPD}	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	/Reset	Reset enable
CK0 – CK1 /CK0 - /CK1	Differential SDRAM Clocks	Event#	Reserved for optional temperature-sensing hardware
RSVD	Reserved for future use.	V _{TT}	SDRAM I/O termination supply.

7. Function Block Diagram:

- (2GB, 2 Rank, 128Mx8 DDR3 SDRAMs)



8. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T _{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T _{STG}	Storage Temperature		-55 to 100	°C	4,5
V _{IN} , V _{OUT}	Voltage on any pins relative to Vss		-0.4 to +1.975	V	4
V _{DD}	Voltage on VDD supply relative to Vss		-0.4 to +1.975	V	4,6
V _{DDQ}	Voltage on VDDQ supply relative to Vss		-0.4 to +1.975	V	4,6

Note:

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM.

For measurement conditions, please refer to the JEDEC document JESD51-2.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.

3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

- a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
- b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

9. DRAM AC & DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
V _{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V _{DDQ}	Supply Voltage	1.425	1.5	1.575	V	1,2
Single Ended AC/DC Input Levels						
V _{IH} (DC)	DC Input High (Logic1) Voltage	V _{REF} + 0.1	-	V _{DD}	V	3
V _{IL} (DC)	DC Input Low (Logic 0) Voltage	V _{SS}	-	V _{REF} - 0.1	V	3
V _{IH} (AC)	AC Input High (Logic1) Voltage	V _{REF} + 0.175	-	-	V	3
V _{IL} (AC)	AC Input Low (Logic 0) Voltage	-	-	V _{REF} - 0.175	V	3
V _{REFDQ} (DC)	Reference Voltage for DQ, DM inputs	0.49V _{DDQ}	0.5V _{DDQ}	0.51V _{DDQ}	V	4,5
V _{REFCA} (DC)	Reference Voltage for ADD,CMD inputs	0.49V _{DDQ}	0.5V _{DDQ}	0.51V _{DDQ}	V	4,5
Single Ended AC/DC output Levels						
V _{OH} (DC)	DC output high measurement level (for IV curve linearity)	-	0.8 x V _{DDQ}	-	V	
V _{OM} (DC)	DC output mid measurement level (for IV curve linearity)	-	0.5 x V _{DDQ}	-	V	
V _{OL} (DC)	DC output low measurement level (for IV curve linearity)	-	0.2 x V _{DDQ}	-	V	
V _{OH} (AC)	AC output high measurement level (for output SR)	-	V _{TT} + 0.1 x V _{DDQ}	-	V	6
V _{OL} (AC)	AC output low measurement level (for output SR)		V _{TT} - 0.1 x V _{DDQ}	-	V	6

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Differential AC/DC Input Levels						
V_{IHdiff}	Differential Input high	+0.2	-	Note 9	V	7
V_{ILdiff}	Differential Input logic Low	Note 9	-	-0.2	V	7
V_{IHdiff}(ac)	Differential Input high ac	2* (V _{IH} (AC)- V _{REF})	-	Note 9	V	8
V_{ILdiff}(ac)	Differential Input logic Low ac	Note 9	-	2* (V _{REF} - V _{IL} (AC))	V	8
Differential AC and DC Output Levels						
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	-	+ 0.2 x V _{DDQ}	-	V	10
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	-	- 0.2 x V _{DDQ}	-	V	10
Note: - Under all conditions V_{DDQ} must be less than or equal to V_{DD}. - V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together. - For DQ and DM, V_{ref} = V_{refDQ}. For input only pins except RESET#, V_{ref} = V_{refCA}. - The ac peak noise on V_{ref} may not allow V_{ref} to deviate from V_{ref}(DC) by more than +/-1% V_{DD} (for reference: approx. +/- 15 mV). - For reference: approx. V_{DD}/2 +/- 15 mV. - The swing of $\pm 0.1 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 - Used to define a differential signal slew-rate. - For CK - CK# use V_{IH}/V_{IL}(ac) of ADD/CMD and V_{REFCA}; for DQS - DQS#, DQSL, DQSL#, DQSU, DQSU# use V_{IH}/V_{IL}(ac) of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here. - These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (V_{IH}(dc) max, V_{IL}(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot. - The swing of $\pm 0.2 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.						

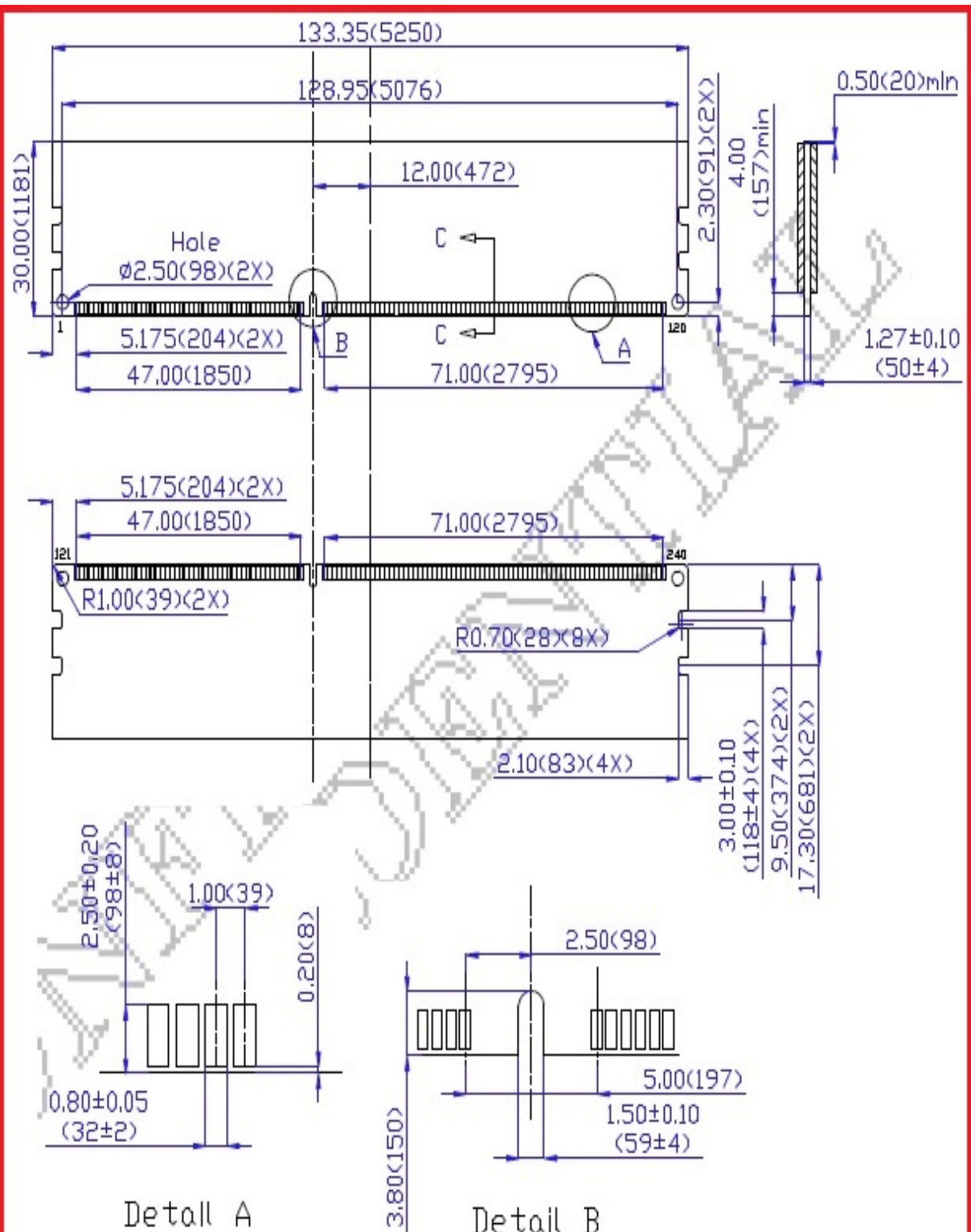
10. Operating, Standby, and Refresh Currents

- 2GB UDIMM (2 Rank, 128Mx8 DDR3 SDRAMs $T_{CASE} = 0^{\circ}C \sim 70^{\circ}C$)

Symbol	Parameter/Condition		PC3-10600	Unit
I DD0	One bank; Active - Precharge		TBD	mA
I DD1	One bank; Active - Read - Precharge		TBD	mA
I DD2N	Precharge Standby Current		TBD	mA
I DD2P	Precharge Power Down Current	Fast Mode	TBD	mA
	Precharge Power Down Current	Slow Mode	TBD	mA
I DD2Q	Precharge Quiet Standby Current		TBD	mA
I DD3N	Active Standby Current		TBD	mA
I DD3P	Active Power-Down Current		TBD	mA
I DD4R	Operating Current Burst Read		TBD	mA
I DD4W	Operating Current Burst Write		TBD	mA
I DD5B	Burst Refresh Current		TBD	mA
I DD6	Self-Refresh Current: Normal Temperature Range		TBD	mA
I DD7	Operating Bank Interleave Read Current		TBD	mA
I DD8	RESET Low Current		TBD	mA

11. PACKAGE DIMENSION

- (2GB, 2 Rank 128Mx8 DDR3 base UDIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

Rev 1.0

January 2016

2008©InnoDisk Corp. All rights reserved
InnoDisk Corp. reserves the right to change the Products and Specification without notices.

12. RoHS Declaration

innodisk	宜鼎國際股份有限公司 Innodisk Corporation														
Tel: (02) 7703-3000 Fax: (02) 7703-3555 Internet: http://www.innodisk.com/															
RoHS 自我宣告書 (RoHS Declaration of Conformity)															
Manufacturer Product: All Innodisk EM Flash and Dram products															
一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 關於 RoHS 之規範要求。 Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement															
二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。 Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.															
<table border="1"> <thead> <tr> <th>Name of hazardous substance</th> <th>Limited of RoHS ppm (mg/kg)</th> </tr> </thead> <tbody> <tr> <td>Cd</td> <td>< 100 ppm</td> </tr> <tr> <td>Pb</td> <td>< 1000 ppm</td> </tr> <tr> <td>Hg</td> <td>< 1000 ppm</td> </tr> <tr> <td>Chromium VI (Cr+6)</td> <td>< 1000 ppm</td> </tr> <tr> <td>Polybromodiphenyl ether (PBDE)</td> <td>< 1000 ppm</td> </tr> <tr> <td>Polybrominated Biphenyls (PBB)</td> <td>< 1000 ppm</td> </tr> </tbody> </table>	Name of hazardous substance	Limited of RoHS ppm (mg/kg)	Cd	< 100 ppm	Pb	< 1000 ppm	Hg	< 1000 ppm	Chromium VI (Cr+6)	< 1000 ppm	Polybromodiphenyl ether (PBDE)	< 1000 ppm	Polybrominated Biphenyls (PBB)	< 1000 ppm	
Name of hazardous substance	Limited of RoHS ppm (mg/kg)														
Cd	< 100 ppm														
Pb	< 1000 ppm														
Hg	< 1000 ppm														
Chromium VI (Cr+6)	< 1000 ppm														
Polybromodiphenyl ether (PBDE)	< 1000 ppm														
Polybrominated Biphenyls (PBB)	< 1000 ppm														
立 保 證 書 人 (Guarantor)															
Company name 公司名稱： <u>Innodisk Corporation 宜鼎國際股份有限公司</u>															
Company Representative 公司代表人： <u>Richard Lee 李鐘亮</u>															
Company Representative Title 公司代表人職稱： <u>CEO 執行長</u>															
Date 日期： <u>2014 / 07 / 29</u>															
 (Company Stamp/公司大小章)															

Revision Log

Rev	Date	Modification
0.1	5 th January 2016	Preliminary Edition
1.0	5 th January 2016	Official released.