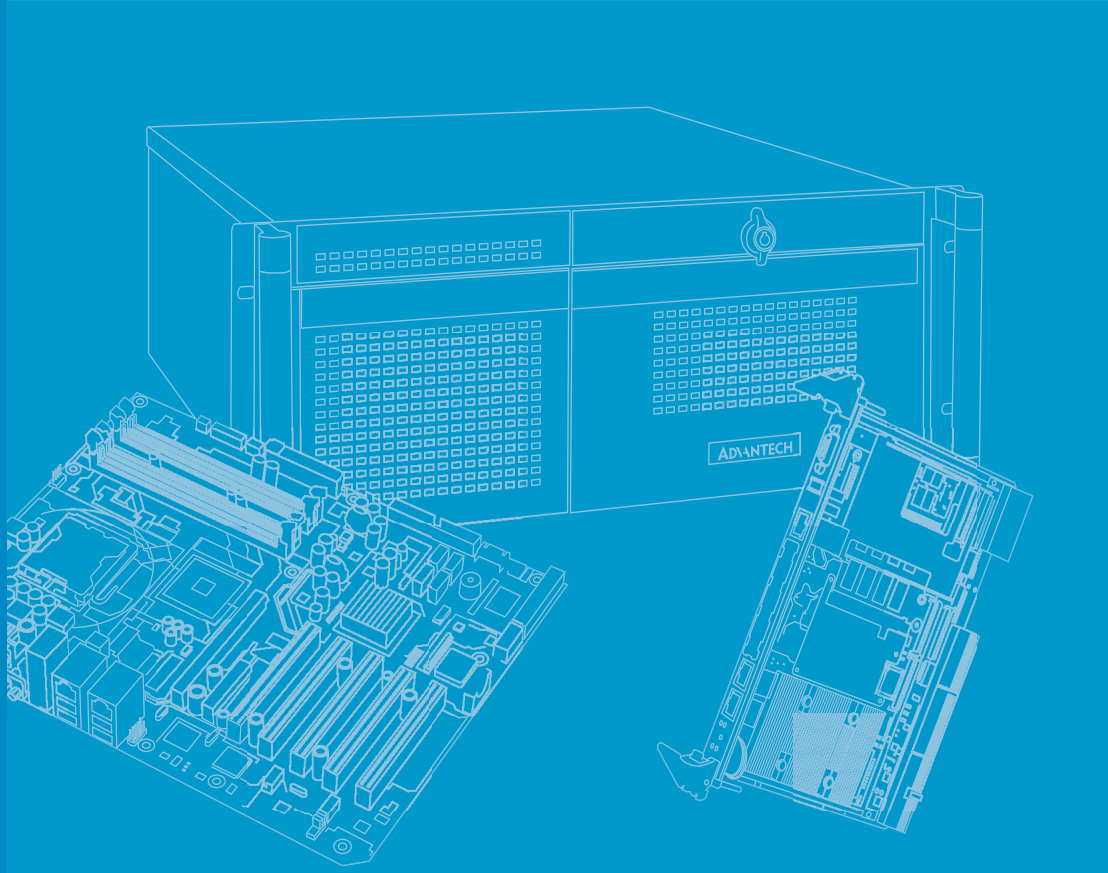

User Manual

ITA-5231 Series

Fanless Embedded Industrial Computer with 6th Gen Intel® Core™ i Processor for Railway Applications

ADVANTECH

Enabling an Intelligent Planet

Copyright

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Product Warranty (2 years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced free of charge during the warranty period. For out-of-warranty repairs, customers are billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you believe your product is defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any messages displayed onscreen when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandize authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photograph of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

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Technical Support and Assistance

1. Visit the Advantech website at http://support.advantech.com to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

A Message to the Customer

Advantech Customer Services

Each and every Advantech product is built to the most exacting specifications to ensure reliable performance in the harsh and demanding conditions typical of industrial environments. Whether your new Advantech equipment is destined for a laboratory or factory floor, you can be assured that your product will provide the reliability and ease of operation for which the name Advantech has come to be known. Your satisfaction is our primary concern. Below is a guide to Advantech's customer services. To ensure you get the full benefit of our services, please follow the instructions carefully.

Technical Support

We want you to get the best performance possible from your products. If you encounter technical difficulties, we are here to help. You can find answers to the most frequently asked questions in your product documentation. These answers are typically a lot more detailed than the ones provided over the phone.Therefore, please consult this manual first. If you still cannot find the answer, gather all the information or questions that apply to your problem, and with the product close at hand, call your dealer. Our dealers are well trained and ready to give you the support you need to get the most from your Advantech products. In fact, most problems reported are minor and can be easily solved over the phone.

In addition, free technical support is available from Advantech engineers every business day. We are always ready to give advice about application requirements or specific information regarding the installation and operation of any of our products.

Initial Inspection

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the list, contact your dealer immediately.

- 1 x ITA-5231 series industrial computer
- 1 x ITA-5231 accessory box
- 1 x Warranty card

If any of these items are missing or damaged, contact your distributor or sales representative immediately. We have carefully inspected the ITA-5231 mechanically and electrically before shipment. It should be free of marks and scratches and in perfect working order upon receipt. As you unpack the ITA-5231, check it for signs of shipping damage (for example, box damage, scratches, dents). If it is damaged or fails to meet the specifications, notify our service department or your local sales representative immediately. Also, please notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After inspection, we will make arrangements to repair or replace the unit.

Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for future reference.
3. Disconnect the equipment from any power outlet before cleaning. Use only a damp cloth for cleaning. Do not use liquid or spray detergents.
4. For pluggable equipment, the power outlet socket must be located near the equipment and easily accessible.
5. Protect the equipment from humidity.
6. Place the equipment on a reliable surface during installation. Dropping or letting it fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. Do not cover the openings.
8. Ensure that the voltage of the power source is correct before connecting the equipment to a power outlet.
9. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage from transient overvoltage.
12. Never pour liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If one of the following occurs, have the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated the equipment.
    - The equipment has been exposed to moisture.
    - The equipment is malfunctioning, or does not operate according to the user manual.
    - The equipment has been dropped and damaged.
    - The equipment shows obvious signs of breakage.

15. Do not leave the equipment in an environment with a storage temperature of below -40 °C (-104 °F) or above 55 °C (131 °F) as this may cause damage. The equipment should be kept in a controlled environment.
16. CAUTION: The battery is at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

In accordance with IEC 704-1:1982 specifications, the sound pressure level at the operator's position does not exceed 70 dB (A).

DISCLAIMER: These instructions are provided according to the IEC 704-1 specifications. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from the PC chassis before manual handling. Do not touch any components on the CPU card or other cards while the PC is powered on.
- Disconnect the power before making any configuration changes. A sudden rush of power after connecting a jumper or installing a card may damage sensitive electronic components.

Battery Information

Batteries, battery packs, and accumulators must not be disposed of as unsorted household waste. Please use the public collection system to return, recycle, or treat such items in compliance with local regulations.

Warnings, Cautions, and Notes

Warning! *Warnings indicate conditions that if not observed may cause personal injury!*

Caution! *Cautions are included to help prevent hardware damage and data losses.*

For example,

“The battery is at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.”

Note! *Notes provide additional optional information.*

Contents

Chapter 1

Overview

- Introduction
- Specifications
- Power Information
- Environment Specifications
- Dimension Diagram

1.1 Introduction

ITA-5231 is a compact and fanless embedded industrial computer equipped with a 6th generation Intel® Core™ i processor and wide voltage input range. Specifically designed for intelligent transportation and road surveillance applications, this powerful computing platform can withstand 24/7 operation.

1.2 Specifications

- **Processer and Chipset:** Intel® Core™ i7/i5/Celeron® processor + Intel® QM170 chipset
- **BIOS:** AMI SPI 128 MB Flash
- **Memory:** On-board 8 GB DDR4 2133 MHz
- **Display:** Intel® HD Graphics 530 (Core i)
  - VGA: 1920x1200 @ 60 Hz
  - DVI: 1920x1200 @ 60 Hz
- **DP Extension:**
  - HDMI: 4096x2160 @ 24 Hz, 24 bpp
  - DVI: 1920x1200 @ 60 Hz
  - VGA: 1920x1200 @ 60 Hz
- **EDP Extension:** LVDS
- **Storage:** Supports 2 x 2.5" SSD (default 1 x ITA-EM-ST51-00A1E)
  - Up to 4 x 2.5" SSD
  - 1 x Full-size mSATA (on main board)
- **Expansion:** 3 x Full-size mini PCIe socket (2 with SIM slot)
- **Ethernet:** 3 x 10/100/1000Mbps with M12 X-coded (female) controller: Intel® I210-IT
- **USB:** 2 x USB 3.0 (Type A), 1 x USB 2.0 with M12, A-coded (F) 4-pin
- **DVI:** 1 x DVI-I
- **Series I/O:** 2 x RS-232/422/485 with 2 KV isolation; supports auto-flow control, DB9 type
- **Digital I/O:** 1 x DI/DO (4 bit) with 2KV isolation, DB9 type
- **Audio:** 1 x Speaker-Out with 2 x 4W 4Ω speakers, 1 x Mic-In
- **Optional I/O Modules:**
  - 1 x ITA-EM-SR51: 4 x RS232/422/484 with 2KV isolation
  - 1 x ITA-EM-CN51: 2 x CAN ports
  - 1 x ITA-EM-NC51: 2 x M12 copper LAN ports
  - 1 x ITA-EM-PE51: 2 x M12 PoE ports
  - 1 x ITA-EM-BA51: Battery module
- **Dimensions (W x H x D):**
  427 x 88 x 195.8 mm (16.8 x 3.46 x 7.7 in)
  482.6 x 88 x 221.3 mm (19 x 3.46 x 8.71 in) with mounting kit
- **Net Weight:** 7.5 kg (16.53 lb)

1.3 Power Information

The ITA-5231's power design is compliant with the EN 50155 S2/C1 standard.

Table 1.1: Power Input				
DC-In Voltage	24V	48V	72V	110V
Voltage Range (0.7~1.25)	16.8 ~ 30V	33.6 ~ 60V	50.4 ~ 90V	77 ~ 137.5V
Transient (0.6~1.4/0.1s)	14.4 ~ 33.6V	28.8 ~ 67.2V	43.2 ~ 100.8V	66 ~ 154V
Power Connector	1 x M12 S-coded (M) 4-pin			

1.4 Environmental Specifications

Table 1.2: Environmental Specifications	
Operating Temperature	EN50155 Tx level: -40 ~ 70 °C (-40 ~ 158 °F) with industrial storage
Safety Certificate Temperature Range	-10 ~ 50 °C (14 ~ 122 °F) with industry level accessory
Storage Temperature	-40 ~ 85 °C (-40 ~ 185 °F)
Humidity	95% @ 40 ºC, non-condensing
Vibration	2 Grms @ 5 ~ 500 Hz, random, 1 hr/axis (SSD/mSATA)
Shock	10G, IEC-68-2-27, half-sine wave, 11 ms duration
Bump	10G, IEC60068-2-27:1987, half-sine wave, 16 ms duration
Safety	UL, CCC, BSMI, CE, FCC

The shock and vibration test were conducted according to the EN 61373, Category 1 - Body mounted, Class B specifications with acceptable results..

1.5 Dimensions

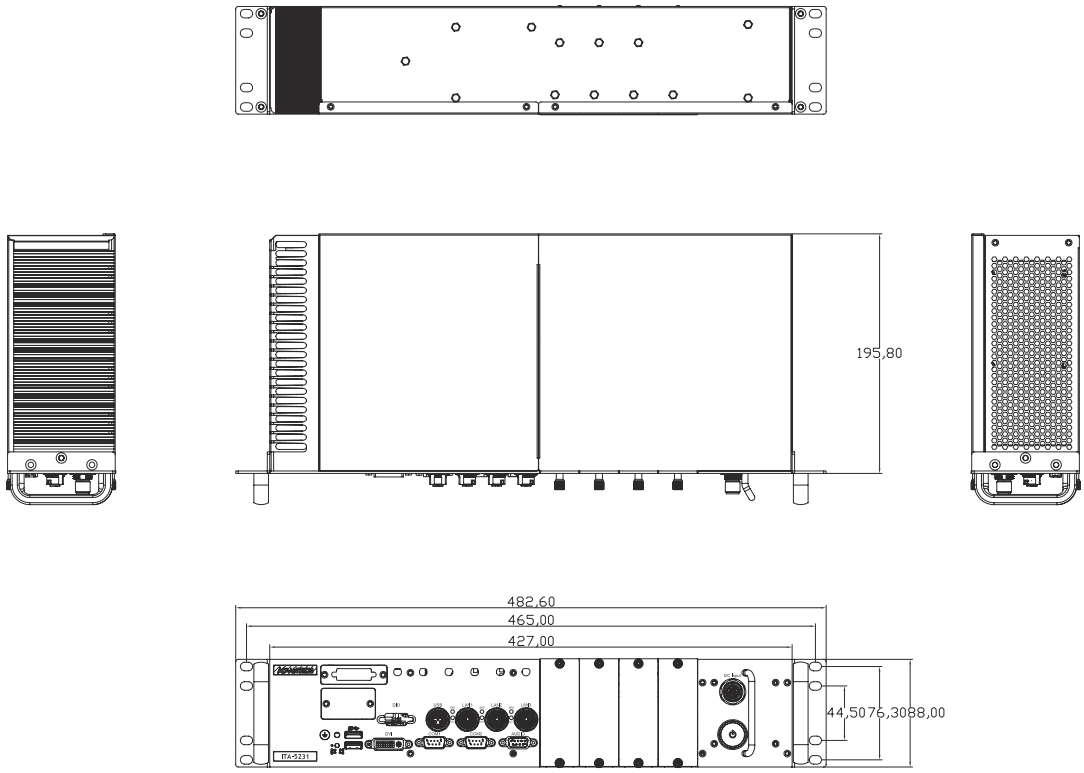


Figure 1.1 ITA-5231 System Diagram

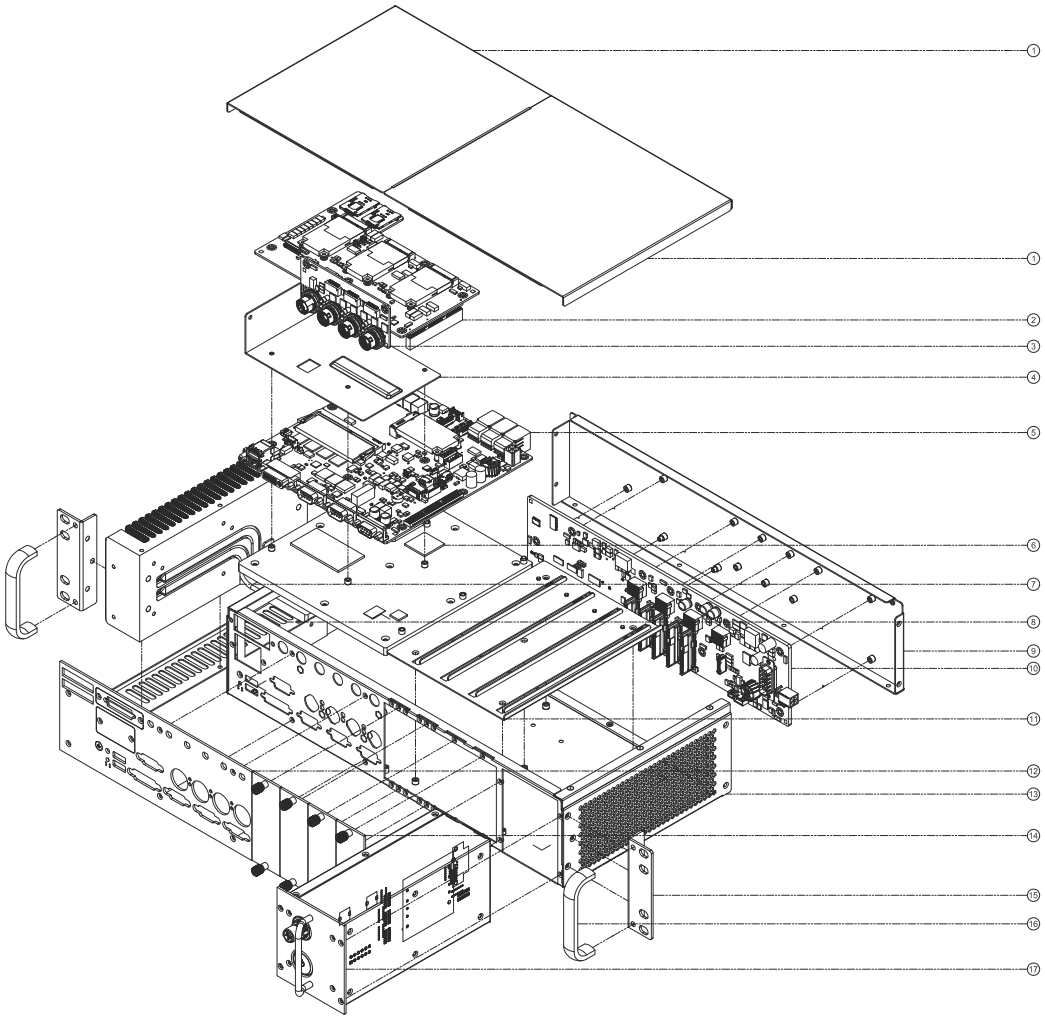


Figure 1.2 ITA-5231 Exploded Diagram

Table 1.3: Parts List			
1	Top cover	10	Rear board
2	Carrier board	11	Rail bracket
3	LAN extension board	12	Front panel
4	Carrier board bracket	13	Right panel
5	Main board	14	Empty bracket with screws
6	Bottom heatsink	15	Ear bracket
7	Side heatsink	16	Handle
8	Chassis	17	Power module
9	Rear panel		

Chapter 2

H/W Installation

- Introduction
- Jumpers and Connectors
- I/O Connectors

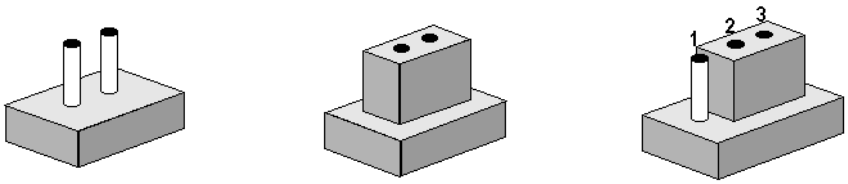
2.1 Introduction

The following sections show the internal jumper settings and external connector pin assignments for system configuration according to applications.

2.2 Jumpers and Connectors

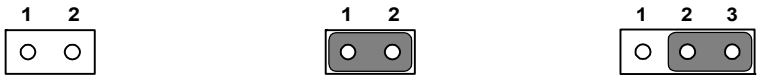
2.2.1 Jumper Description

ITA-5231 can be configured for specific applications by setting jumpers. A jumper is a metal bridge used to close an electric circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To close a jumper, remove the clip. Some jumpers may have three pins, labelled 1, 2, and 3. For these jumpers, connect either Pins 1 and 2, or Pins 2 and 3.



Open Closed 2-3 Closed

The jumper settings are schematically depicted in this manual as shown below.



Open Closed 2-3 Closed

A pair of needle-nose pliers may be helpful when working with jumpers. If you have concerns about the best hardware configuration for your application, contact your local distributor or sales representative before making any changes. For most connection, only a standard cable is required.

2.2.2 Jumper and Connector Locations

The main board features a number of connectors and jumpers for system configuration. The location of each jumper and connector on the main board is shown in Figure 2.1. The function of each of the connectors and jumpers is listed in Table 2.1 below.

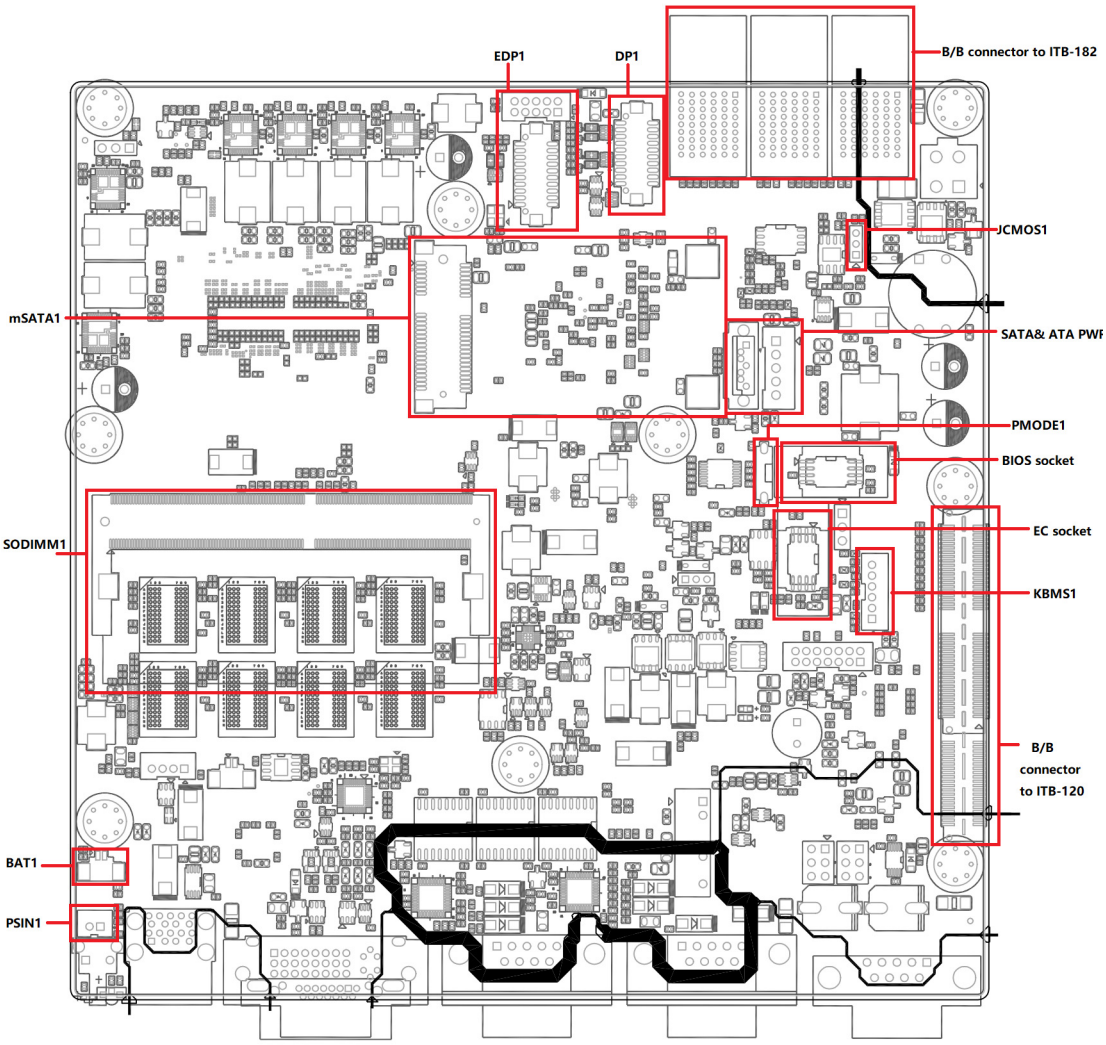


Figure 2.1 Jumper and Connector Locations on Main Board

Table 2.1: Jumpers and Switches

Name	Function
PSIN1	Power button pin header
BAT1	RTC battery pin header
JCOMS1	Clear CMOS settings
PMOD1	ATX, AT mode switch

Table 2.2: BAT1 (RTC Battery Pin Header)	
Pin	**Setting**
1	Power (3.3V)
2	GND

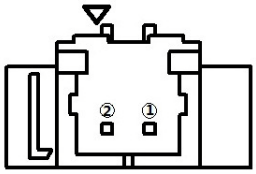


Table 2.3: JCMOS1 (Clear CMOS Settings)	
Pin	**Setting**
1-2	Default*
2-3	Clear CMOS
*Default	

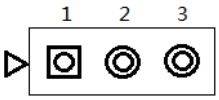
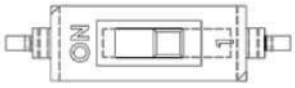


Table 2.4: PMOD1 (AT, ATX Switch)	
Pin	**Setting**
On	AT
Off	ATX*
*Default	



2.3 I/O Connectors

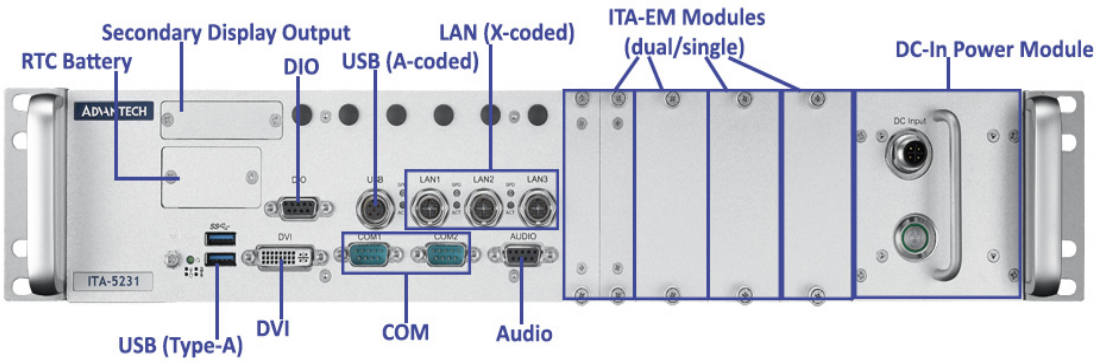


Figure 2.2 ITA-5231 I/O View

2.3.1 COM Connector

ITA-5231 is equipped with two RS-232/422/485 DB9 connectors. The default setting is RS-232.

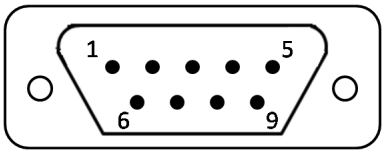


Table 2.5: COM Connector Pin Definitions

	RS-232	RS-422	RS-485
Pin	**Signal Name**	**Signal Name**	**Signal Name**
1	DCD	TxD(-)	DATA-
2	RxD	TxD(+)	DATA+
3	TxD	RxD(+)	NC
4	DTR	RxD(-)	NC
5	GND	GND	GND
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

2.3.2 Audio Connector

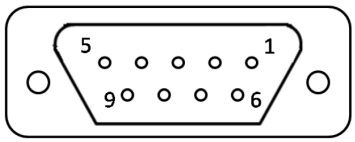


Table 2.6: Audio Connector Pin Definitions

Pin	Signal Name	Pin	Signal Name
1	MICR	6	LOUTR
2	GND_AUD	7	GND_AUD
3	GND_AUD	8	Front_JD
4	MIC_JD	9	LOUTL
5	MICL		

2.3.3 Digital I/O Connector

ITA-5231 provides one DIO (8 bit) with DB9 type connector (four DI and four DO).

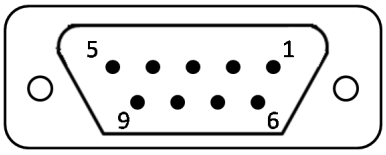


Table 2.7: Digital I/O Connector Pin Definitions

Pin	Signal Name	Pin	Signal Name
1	GPI1	6	GPO1
2	GPI2	7	GPO2
3	GPI3	8	GPO3
4	GPI4	9	GPO4
5	GND		

2.3.4 USB Connector

ITA-5231 features two USB 3.0 ports with a Type-A connector and one USB 2.0 port with an M12 A-coded female connector. The USB interface can be disabled via the system BIOS utility.

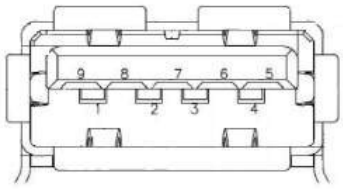


Table 2.8: USB 3.0 Connector Pin Definitions

Pin	Signal Name	Pin	Signal Name
1	+V5(VCC)	6	StdA_SSRX+
2	D-	7	GND_DRAIN
3	D+	8	StdA_SSTX-
4	GND	9	StdA_SSTX+
5	StdA_SSRX-		

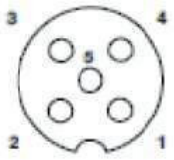


Table 2.9: USB 2.0 Connector Pin Definitions

Pin	Signal Name	Pin	Signal Name
1	+5V	4	NC
2	D-	5	GND
3	D+		

2.3.5 Ethernet

ITA-5231 provides three 10/100/1000 Mbps Ethernet ports with an M12, X-coded connector.

Table 2.10: Ethernet Connector Pin Definitions

Pin	Signal Name	Pin	Signal Name
1	MDI0+	5	MDI3+
2	MDI0-	6	MDI3-
3	MDI1+	7	MDI2-
4	MDI1-	8	MDI2+

2.3.6 Power Input

Table 2.11: Power Connector Pin Definitions

Pin	Signal Name	Pin	Signal Name
1	PWR	3	GND
2	PWR	4	NC

2.3.7 DVI-I

ITA-5231 reserves the main display output as DVI-I as a default. There is the option to convert this to DVI-D +VGA via a Y-cable.

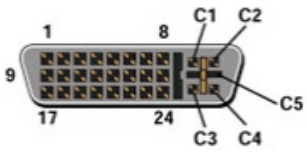


Table 2.12: DVI-I

Pin	Signal Name	Pin	Signal Name
1	T.M.D.S. Data2-	16	Hot Plug Detect
2	T.M.D.S. Data2+	17	T.M.D.S. Data0-
3	Ground	18	T.M.D.S. Data0+
4	VGA DCC Clock	19	Ground
5	VGA DCC Data	20	Ground
6	DDC Clock	21	Ground
7	DDC Data	22	DVI Detect
8	Analog Vertical Sync	23	T.M.D.S. Clock+
9	T.M.D.S. Data1-	24	T.M.D.S. Clock-
10	T.M.D.S. Data1+	C1	Analog Red
11	Ground	C2	Analog Green
12	Ground	C3	Analog Blue
13	Ground	C4	Analog Horizontal Sync
14	+5V Power	C5	Ground
15	Ground		

2.3.8 LED Indicators

The ITA-5231 front panel features LEDs that are used to indicate system health and active status. The LED indicator behaviors are described and explained in the table below.

Item	LED	Status	Color	Description
1	PWR	On	Green	The system is powered on and functioning normally
		Off		
2	HDD	On	Yellow	Data is being received/transmitted
		Off		Not active
3	FAULT_SYS	On	Red	System fault detected
		Off		
4	Battery	On	Yellow	Battery still has charge
			Red	Battery fully discharged
			Blinking red	Battery low power alarm
		Off		Battery is fully recharged

Chapter 3

System Setup

- mSATA Installation
- ITA-EM Module Installation
- RTC Battery Installation
- Antenna Installation

3.1 Introduction

The following sections provide instructions for installing the hardware modules into the ITA-5231 system.

3.2 mSATA Installation

ITA-5231 features one mSATA slot on the main board and three mini-PCIe slots on the carrier board.

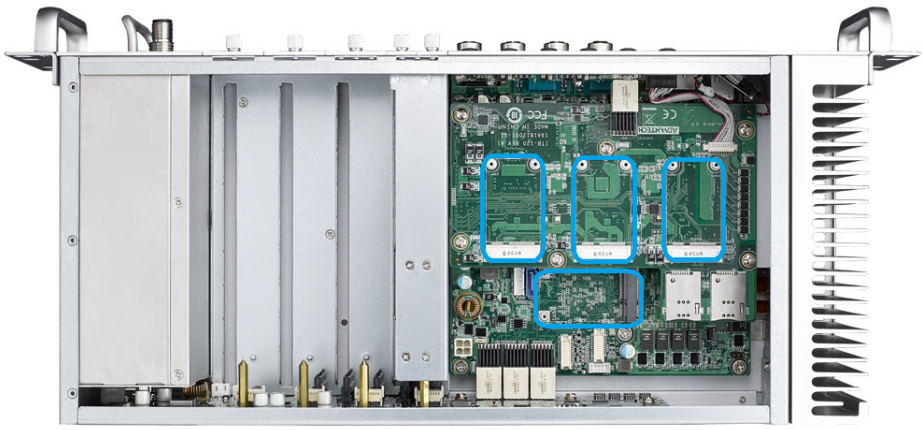


Figure 3.1 Mini-PCIe and mSATA Locations on Main Board

1. Open the top cover of the device.
2. Loosen the screws to remove the dual-SSD bracket. Remove the carriage bracket for the easy-swap module.
3. Insert the mSATA or mini-PCIe module.
4. Affix the module in place using two screws.

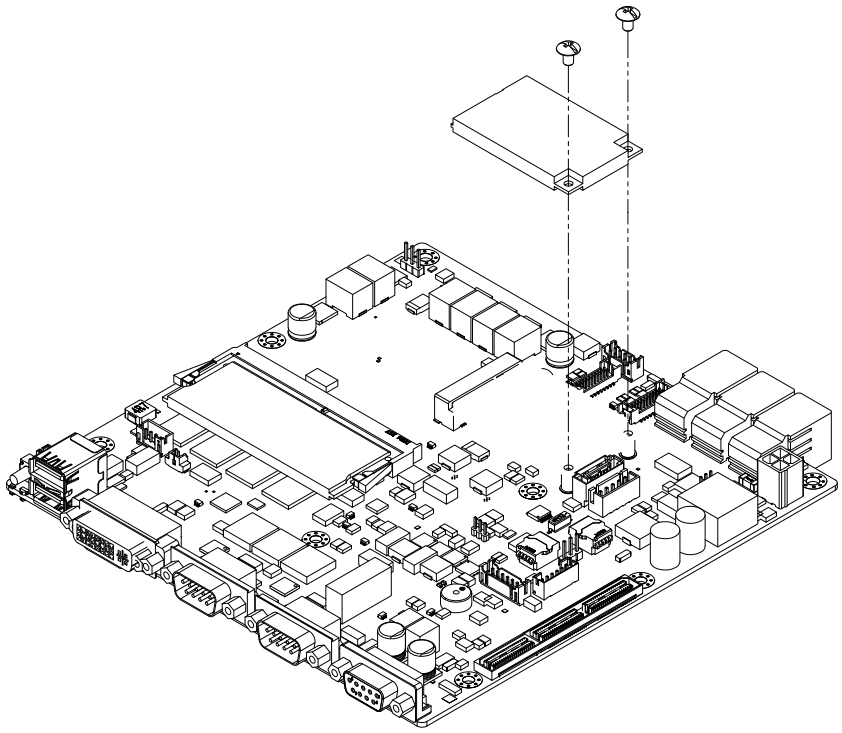


Figure 3.2 mSATA Installation

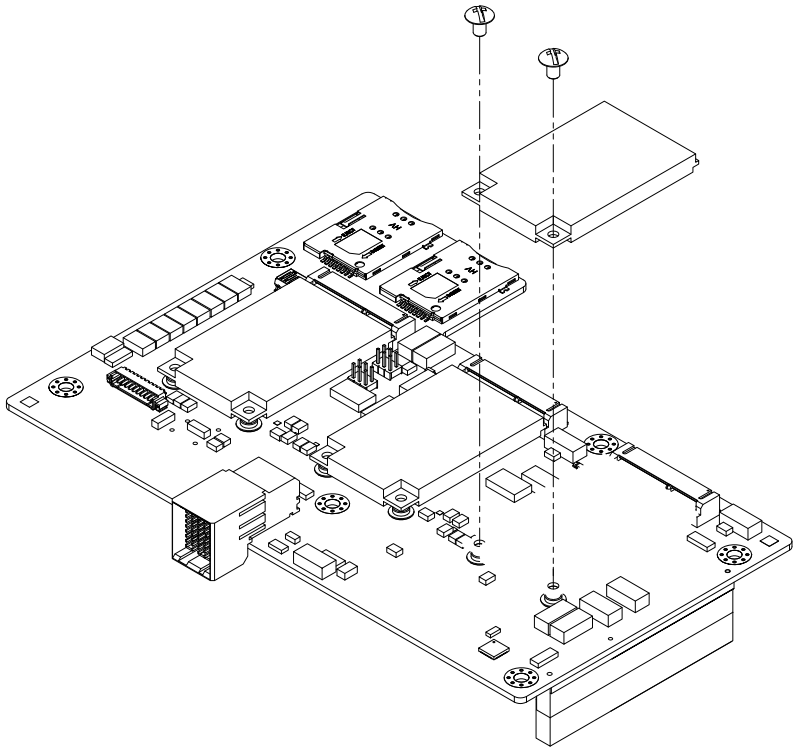


Figure 3.3 Mini-PCIe Installation

3.3 SSD Installation

ITA-5231 is equipped with one dual-SSD module socket[1] that features two brackets[2]. To install an SDD, follow the instructions provided on the next page.

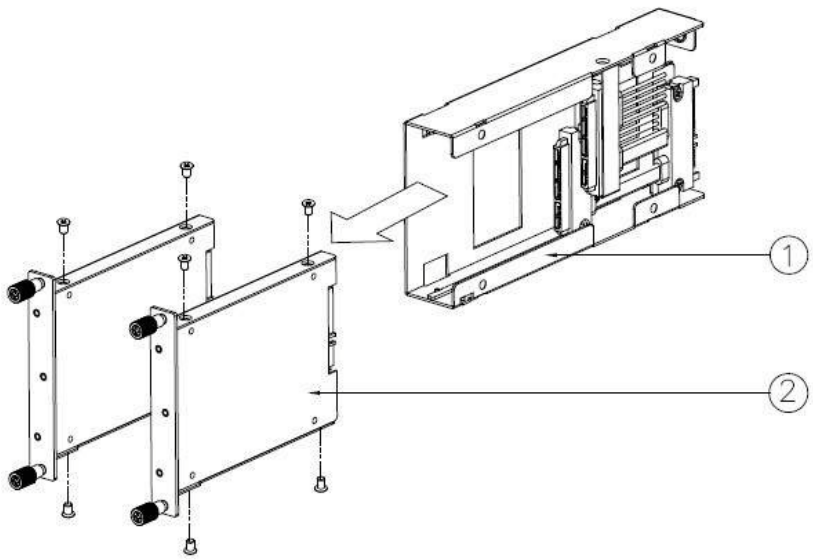


Figure 3.4 SSD Bracket

1. Loosen the screws on the front panel and pull out the dual SSD bracket.
2. Install the SSD onto the bracket and secure it in place using 4 screws.

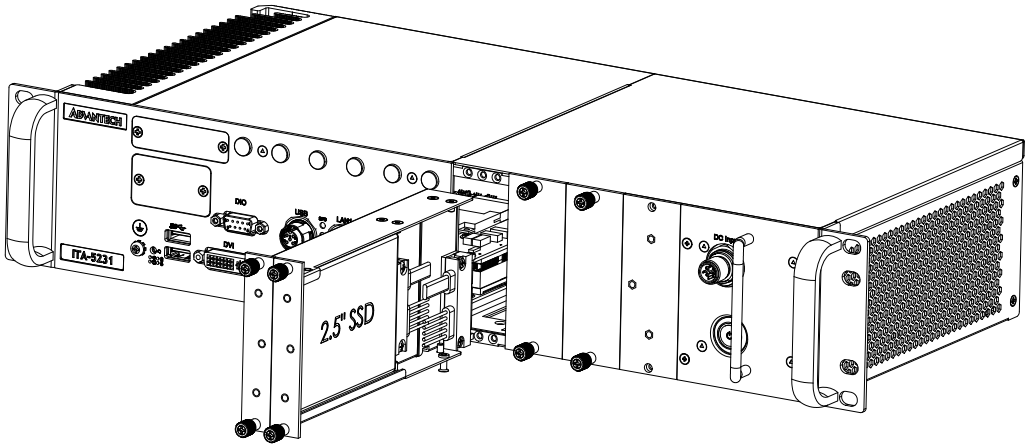


Figure 3.5 SSD Module Installation

3.4 ITA-EM Easy-Swap Module Installation

ITA-5231 reserves a blank bracket for installing an easy-swap module to extend the system I/O. The SSD modules in the dual-SDD bracket can be removed and replaced with other easy-swap modules.

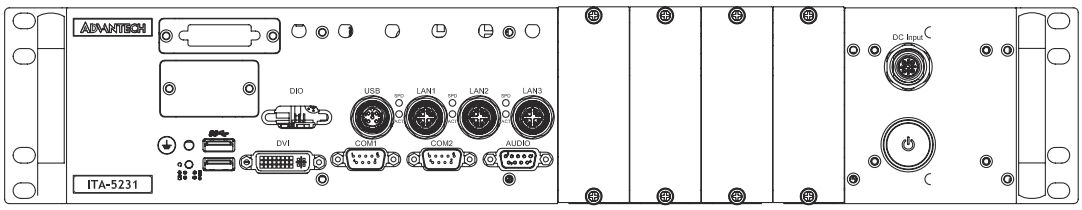


Figure 3.6 ITA-5231 Front View

1. Loosen the screws in the front panel and remove the blank bracket.
2. Insert the ITA-EM module into the bracket and secure it in place using 4 screws.

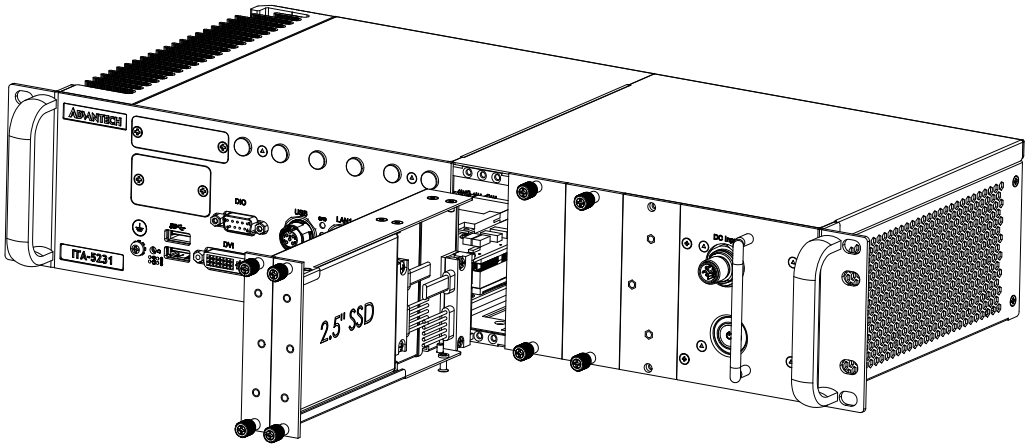


Figure 3.7 Easy-Swap Module Installation

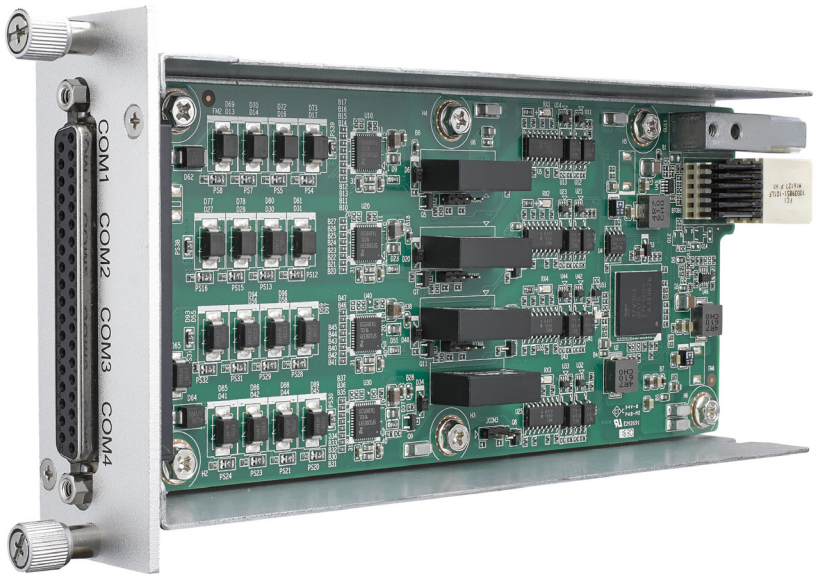


Figure 3.8 COM Module (ITA-EM-SR51-001AE)

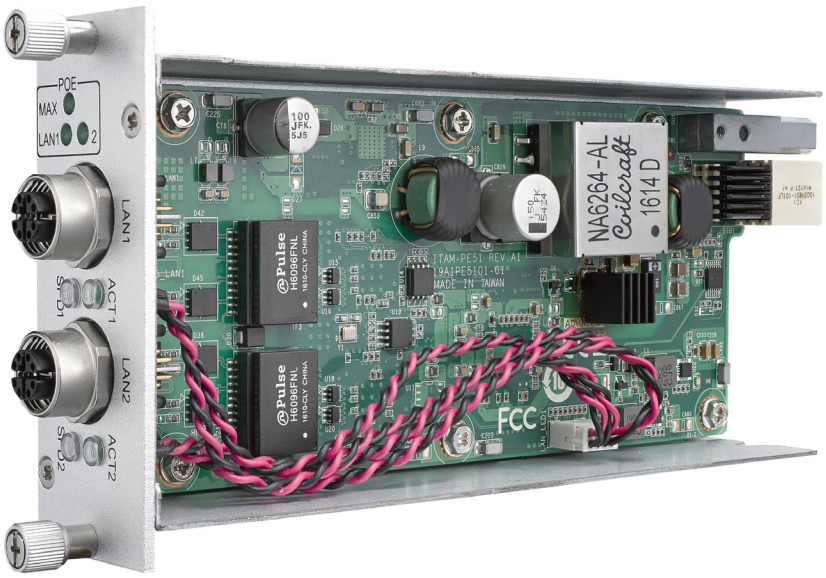


Figure 3.9 PoE Module (ITA-EM-PE51-001AE)

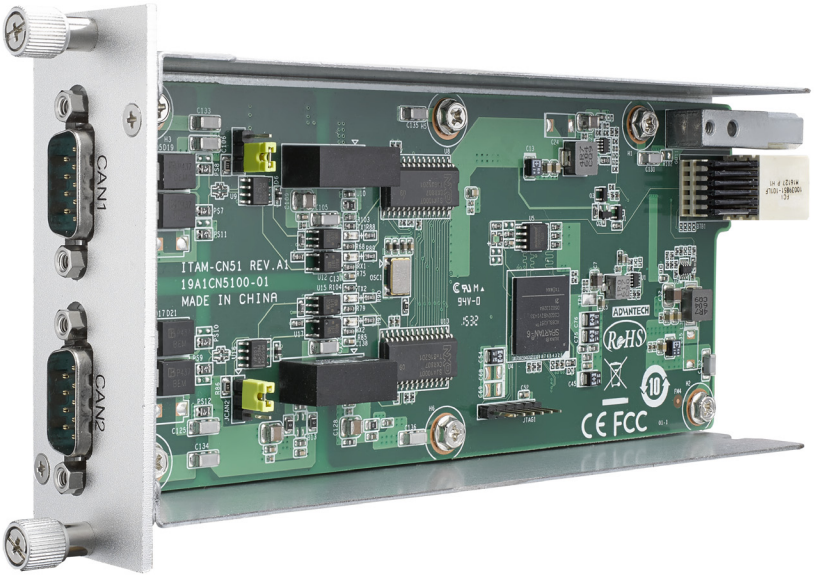


Figure 3.10 CAN Module (ITA-EM-CN51-001AE)

Figure 3.11 Battery Module (ITA-EM-BA51-00A1E)

3.5 RTC Battery Installation

The RTC battery can be accessed via the front panel.

1. Open the RTC battery port cover.
2. Insert the RTC battery into the holder and connect the cable.
3. Close and lock the RTC battery port cover.

Note! *The RTC battery settings can be configured using the BIOS utility. The +VBAT should be >2.6V. The standard battery lifetime is 3 years+. Users can change the RTC battery according to voltage requirements.*

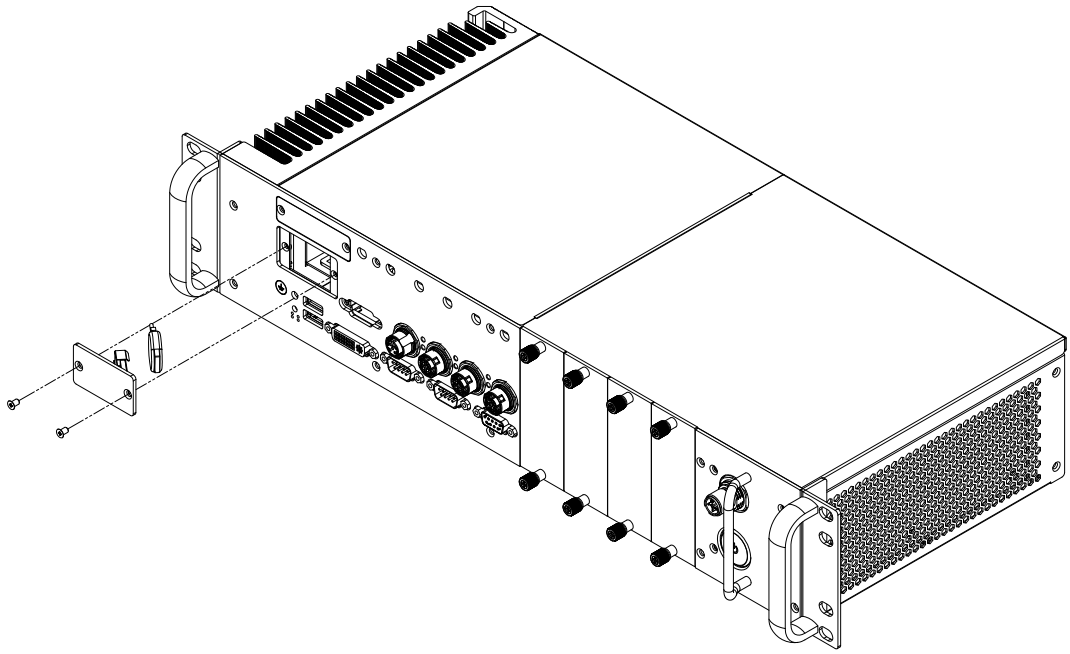


Figure 3.12 RTC Battery Installation

3.6 Antenna Installation

ITA-5231 features antenna connectors on the front panel.

1. Open the top cover of the device.
2. Loosen the screws to remove the dual-SSD bracket. Remove the carriage bracket for the easy-swap module. Insert the mini-PCIe module and secure it in place using 2 screws.
3. Install antennas on both sides of the chassis.

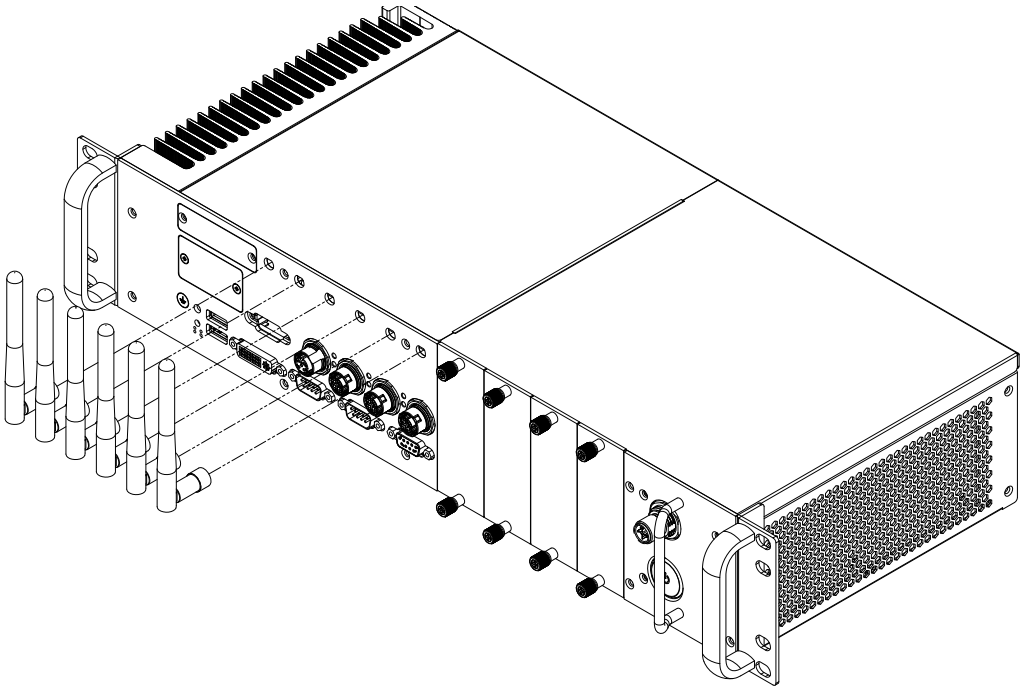


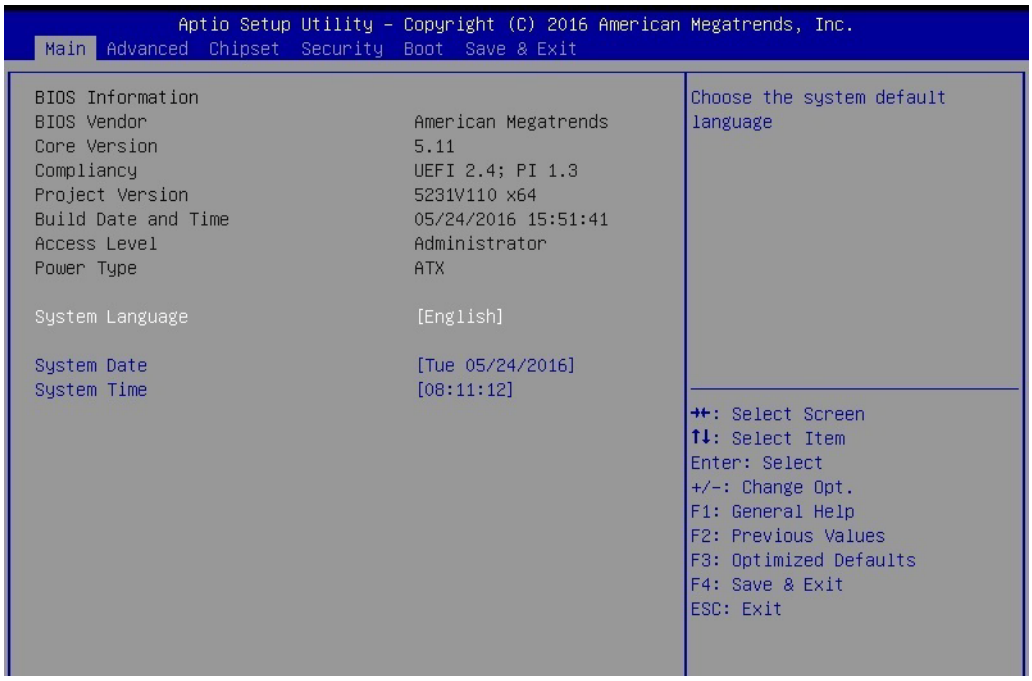
Figure 3.13 Antenna Installation

Chapter 4

BIOS Settings

4.1 Introduction

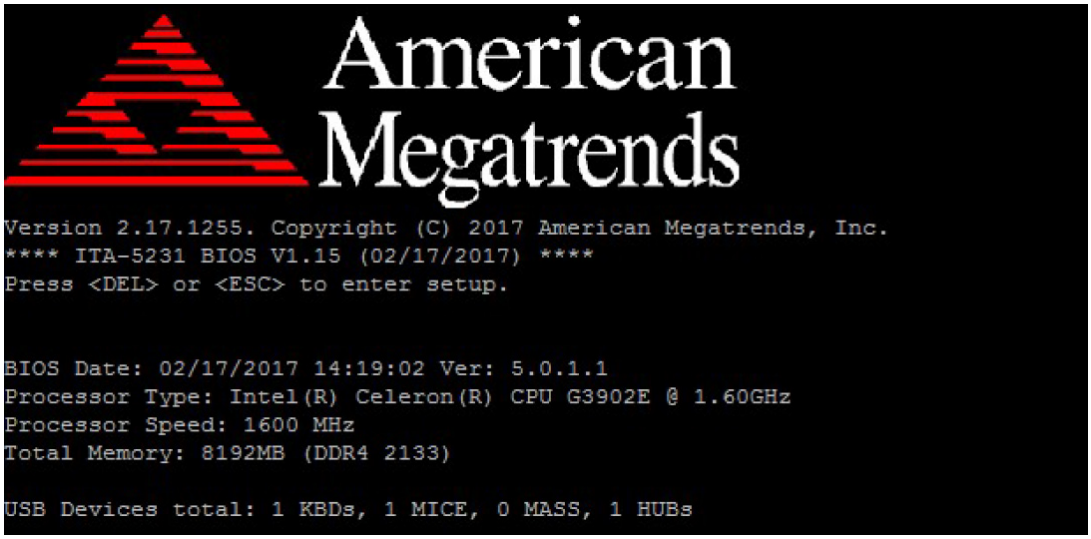
This chapter explains the basic navigation of the BIOS Setup menus and how to configure the BIOS settings for the ITA-5231 series. With the AMI BIOS Setup program, users can modify the BIOS settings and control the device features. The Setup program features several menus with multiple items that for enabling/disabling functions and implementing changes.



AMI's BIOS ROM has a built-in setup program that allows users to modify the basic system configuration. The configuration information is stored in CMOS, which ensures that the information is retained when the power is turned off.

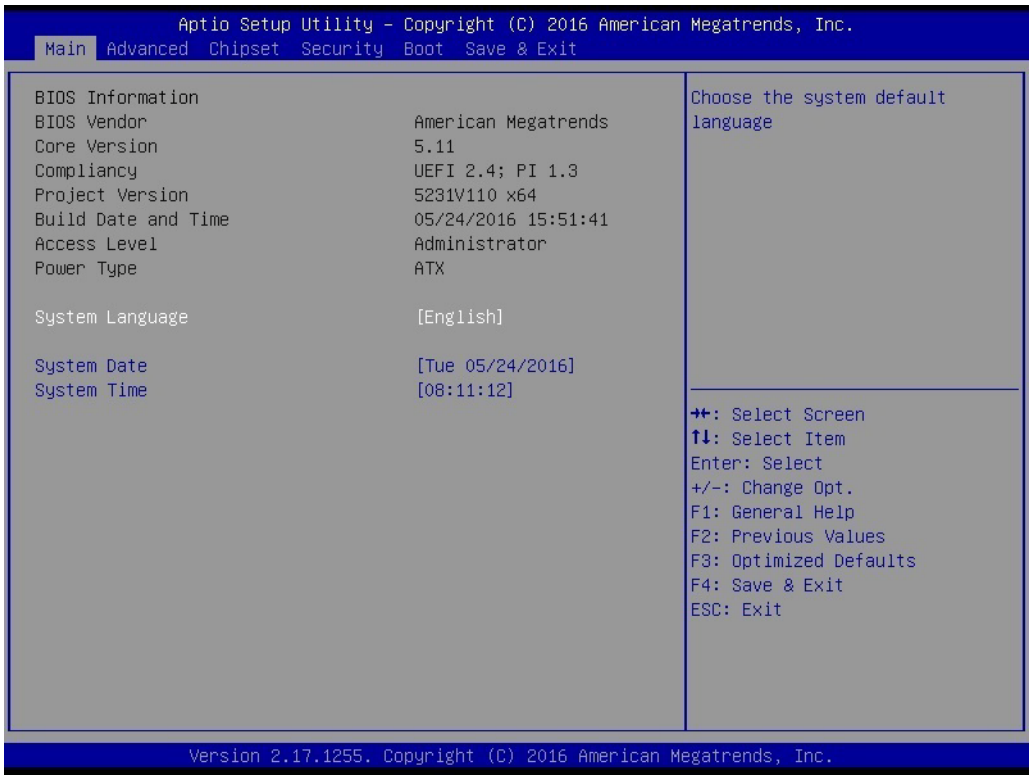
4.2 Entering BIOS Setup

Power on the computer to enter the POST screen. The BIOS and CPU information will be displayed on screen. Press <DEL> to enter the BIOS Setup utility.



4.3 Main Setup

Upon entering the BIOS Setup utility, users are presented with the Main setup page. Users can always return to the Main setup page by selecting the Main tab. The Main BIOS Setup page is shown below.



The Main BIOS setup page has two main frames. The left frame displays all the items accessible on the Main page. Items that are grayed out cannot be configured, whereas items presented in blue text can be configured. The right frame displays the key legend.

Located above the key legend is an area reserved for a text message. When an item is selected in the left frame, the item is presented in white text and often accompanied by a text message.

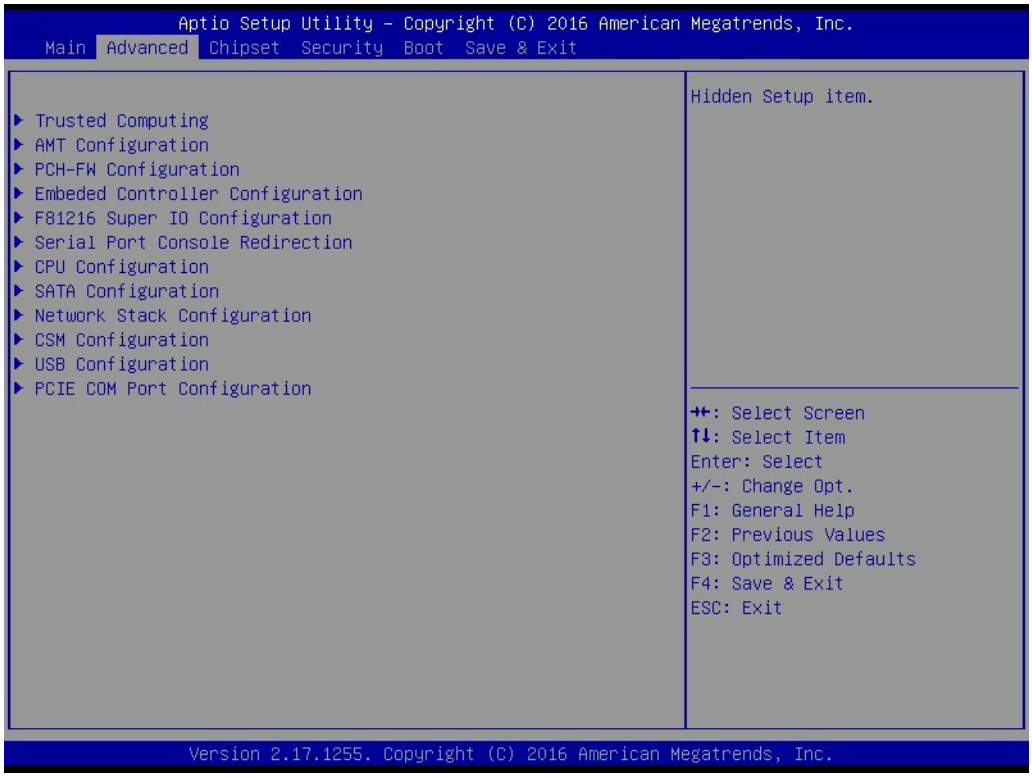
- **System Time/System Date**

  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values via the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format, and the time must be entered in HH:MM:SS format.

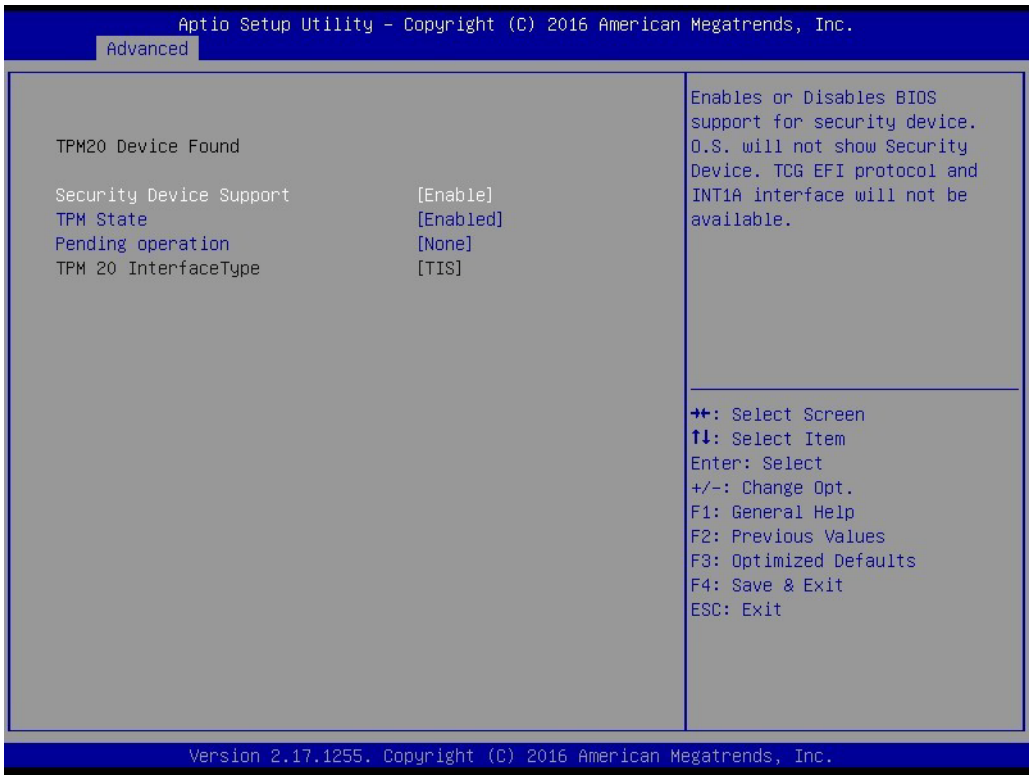
4.3.1 Advanced BIOS Setup

Select the Advanced tab from the BIOS Setup Utility to enter the Advanced BIOS Setup page. Select any of the items in the left frame of the screen, such as CPU Configuration, to access the sub menu for that item. The options for any of the Advanced BIOS Setup items can be displayed by highlighting the item using the <Arrow> keys.

The Advanced BIOS Setup page is shown below.



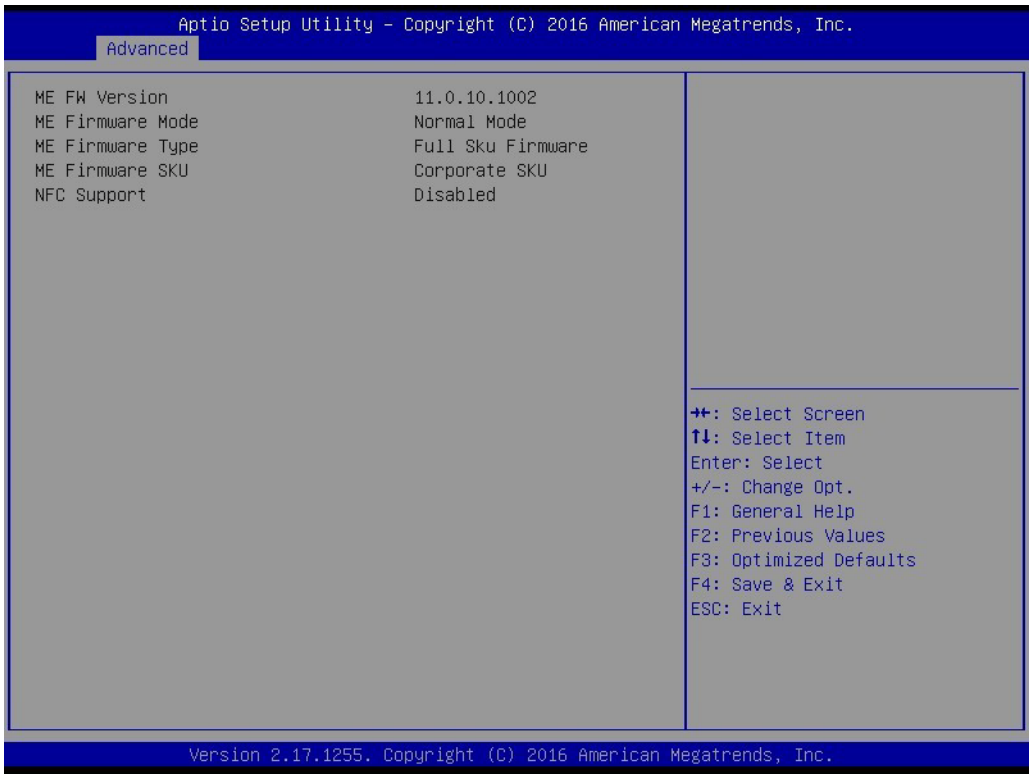
4.3.1.1 Trusted Computing



- **Security Device Support**
  This item allows users to enable/disable BIOS support for the security device. The default setting is “enabled”.
- **TPM State**
  This item allows users to enable/disable security device. The default setting is “enabled”.
- **Pending Operation**
  This item allows users to schedule an operation for the security device. The TPM setting can be “clear” or “none”. The default setting is “none”.

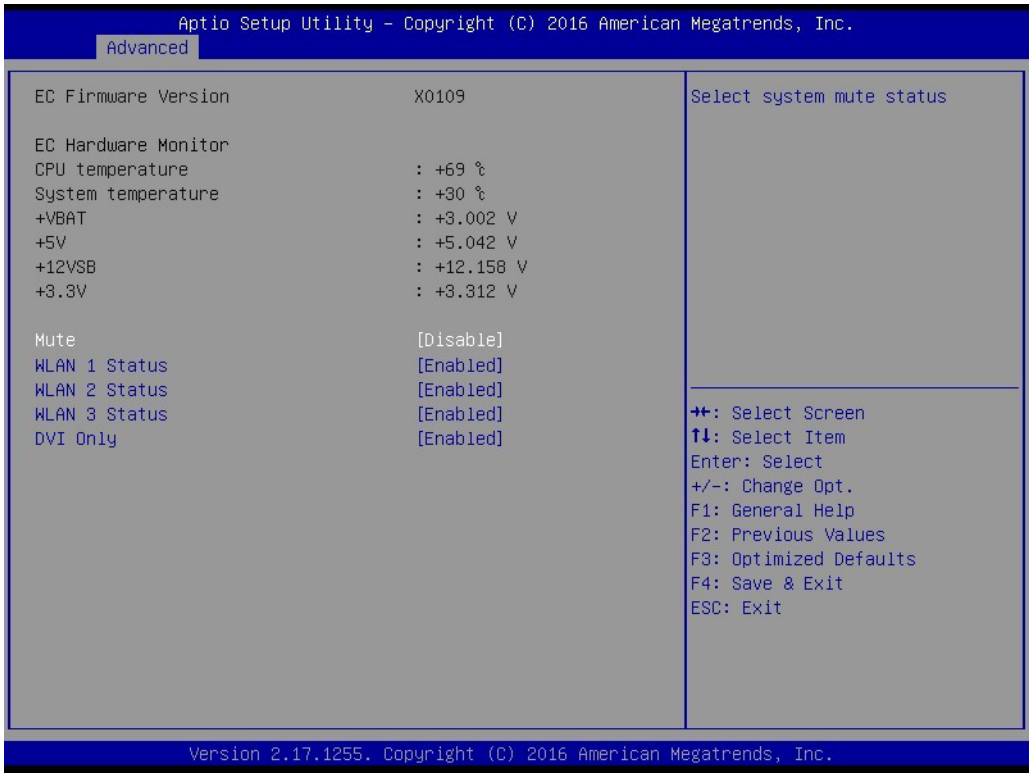
4.3.1.2 PCH-FW Configuration

This page shows the version, mode, type, and SKU of the ME firmware built-in BIOS.



4.3.1.3 Embedded Controller Configuration

This page shows the hardware data accessed by the embedded controller. Users can access this page to obtain the system temperature, voltage, or status information.



- **Mute**

  This item allows users to enable/disable the system audio. The default setting is “disabled”.

- **WLAN 1/2/3 Status**

  This item allows users to enable/disable WLAN status. The default setting is “enabled”.

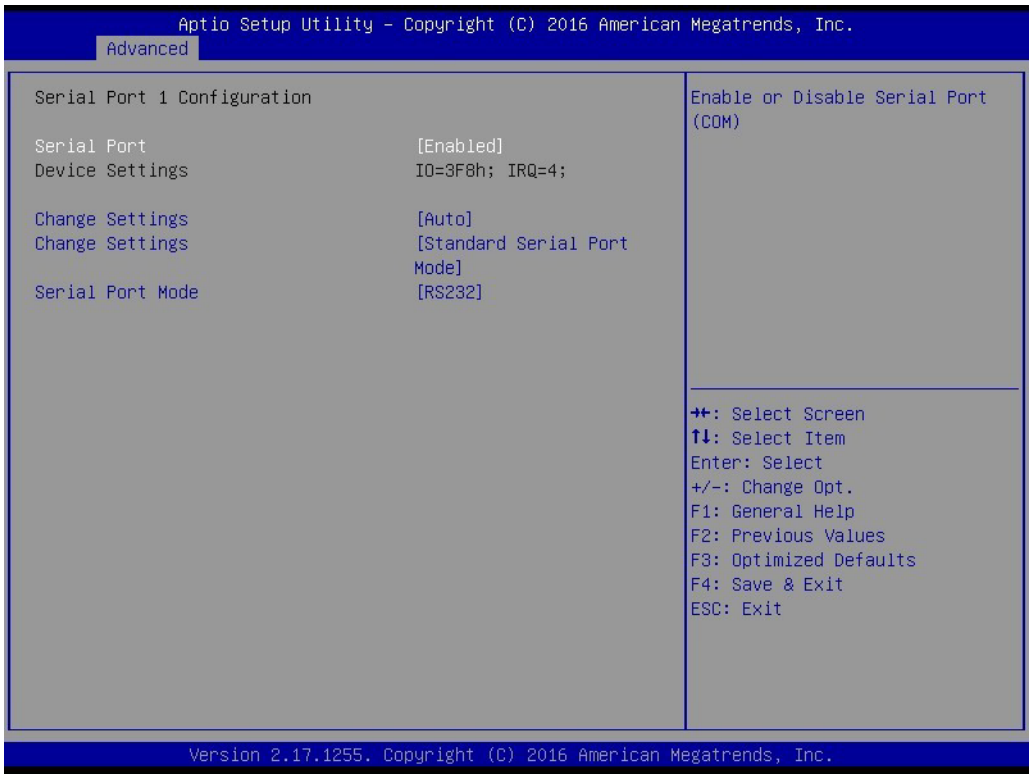
- **DVI Only**

  This item allows users to enable/disable DVI Only mode. The default setting is “disabled”.

4.3.1.4 F81216 Controller Configuration

ITA-5231 supports two serial ports. Users can configure the serial port in the BIOS Setup utility. Serial port 60 has a hardware reserved function. The default setting is “disabled”.

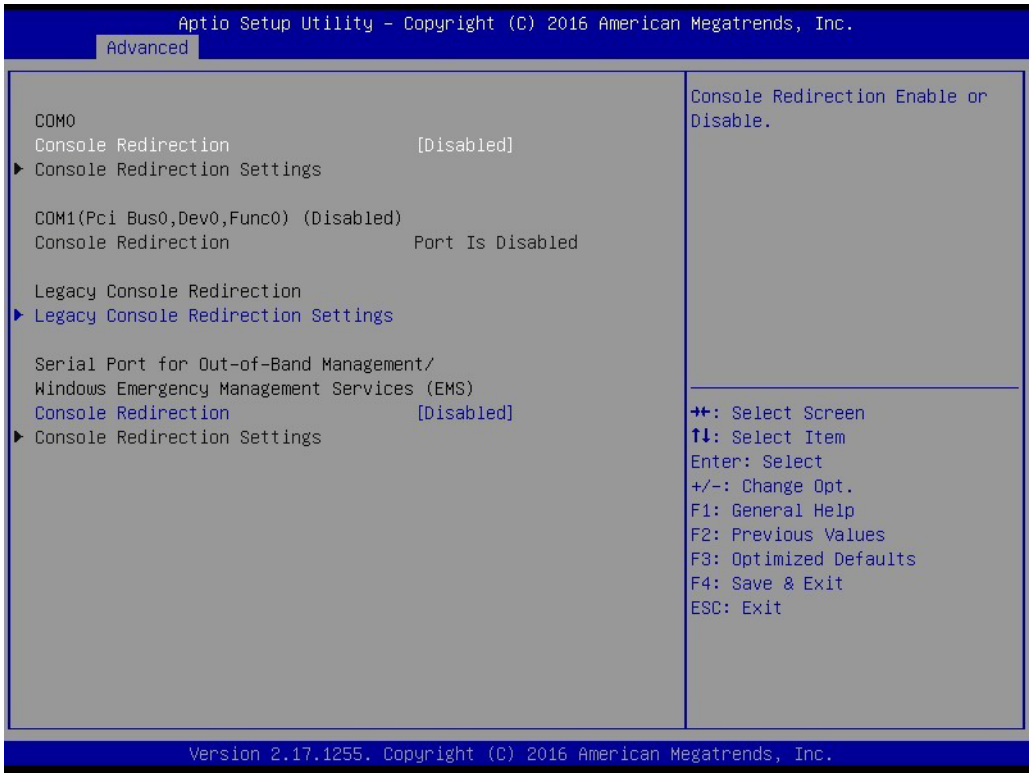
Serial Port 1/2 Configuration



- **Serial Port**
  This item allows users to enable/disable the serial port. The default setting is “enabled”.
- **Device Settings**
  This item allows users to view the I/O ports in operation and the IRQ number.
- **Change Settings [1]**
  This item allows users to optimize the serial port settings (I/O port and IRQ). The default setting is “auto”.
- **Change Settings [2]**
  This item allows users to optimize the serial port settings (full/half duplex). The default setting is “standard serial port mode”.
- **Serial Port Mode**
  This item allows users to select the serial port mode (RS-232 or RS-485). The default setting is “RS-232”.

4.3.1.5 Serial Port Console Redirection

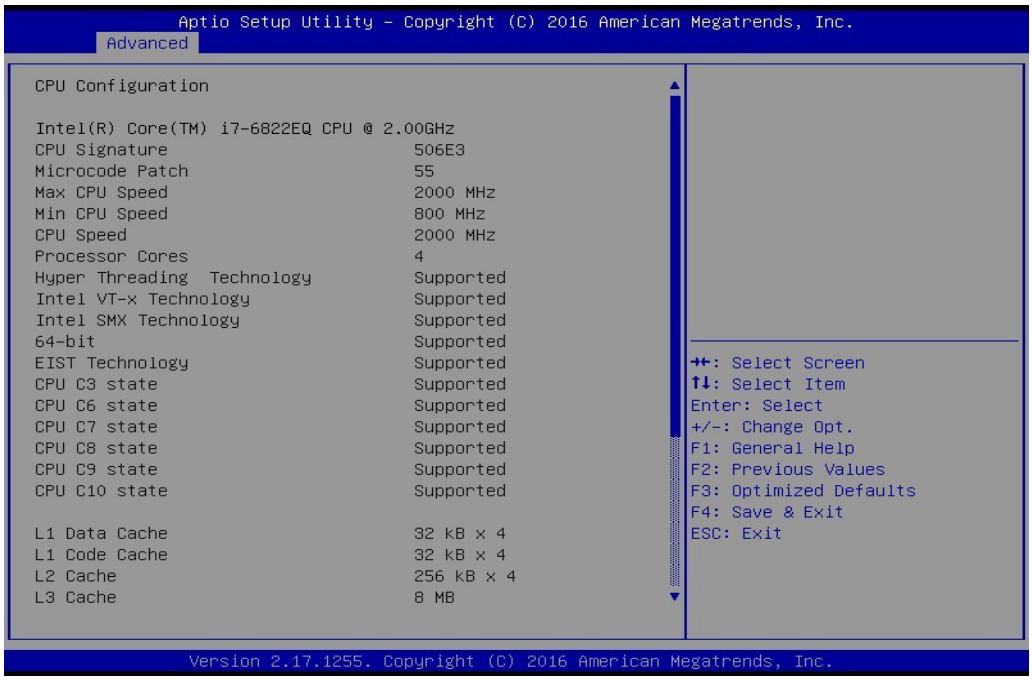
This page shows the console status. Users can configure the console settings in the Console Redirection Settings item.

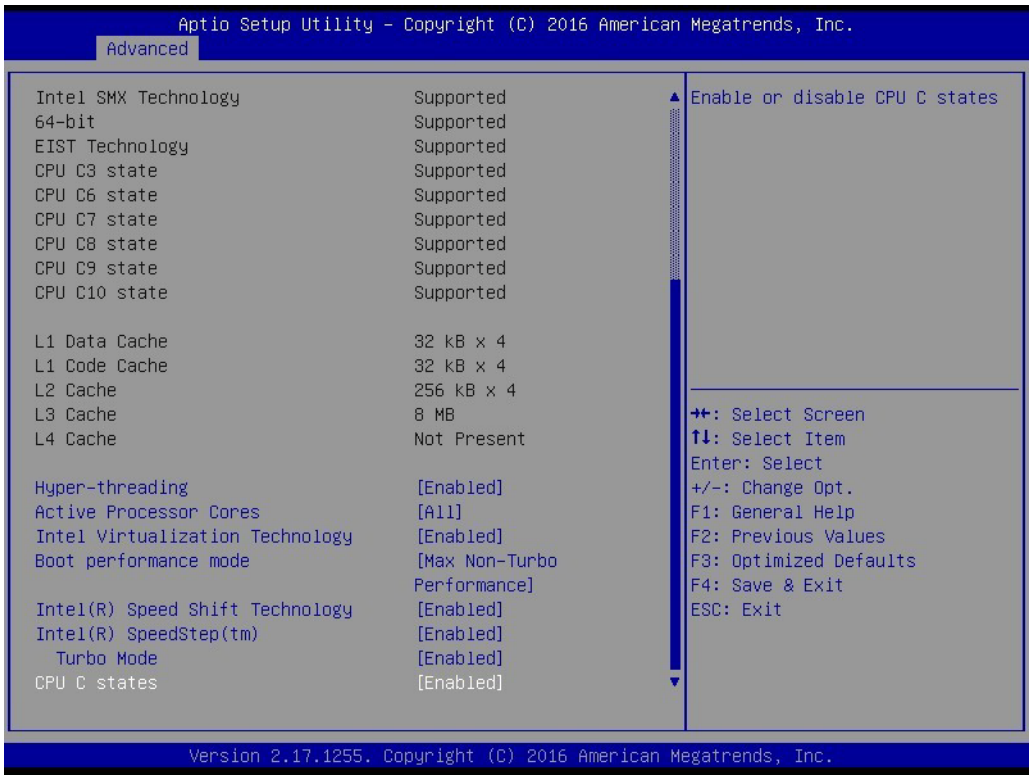


- **Console Redirection**
  This item allows users to enable/disable the console redirection function. The default setting is “disabled”.
- **Console Redirection Settings**
  When the console redirection function is enabled, this item becomes available. The settings specify how the host computer and remote computer exchange data. Both computers should have the same or compatible settings.
- **Legacy Console Redirection Settings**
  This item shows the legacy serial port number.

4.3.1.6 CPU Configuration

This page shows the system CPU information.





- **Hyper-Threading**

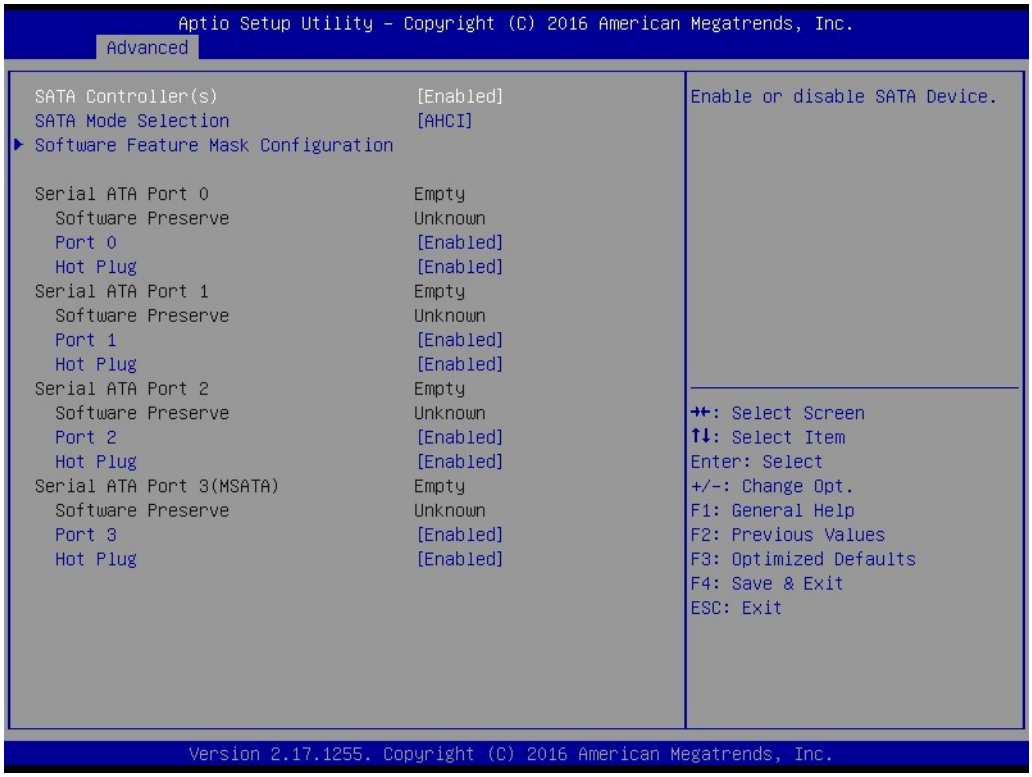
  This item allows users to enable/disable the CPU hyper-threading function. The default setting is “enabled”.

- **Active Processor Cores**

  This item allows users to select the number of cores to enable for each processor package. The default setting is “all”.

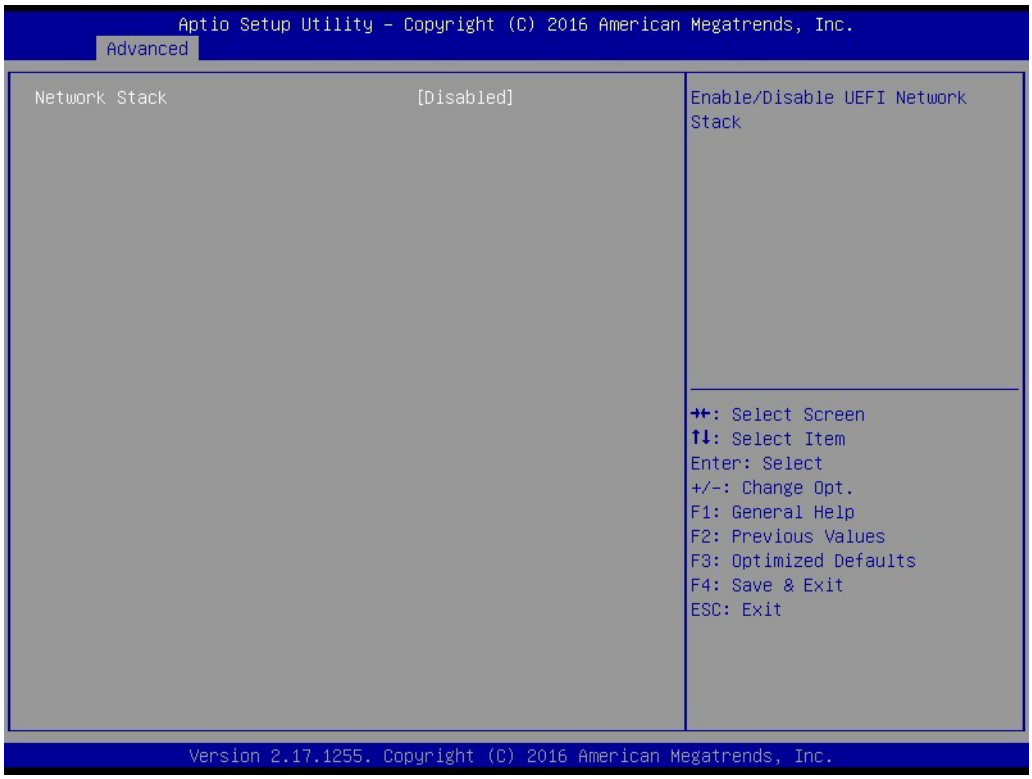
- **Intel Virtualization Technology**
  This item allows users to enable/disable Intel Virtualization Technology. When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. The default setting is “enabled”.
- **Boot Performance Mode**
  This item allows users to select the performance state that the BIOS will set before OS handoff. The default setting is “max. non-turbo performance”.
- **Intel® Speed Shift Technology/Intel® SpeedStep™**
  This item allows users to enable/disable support for more than two frequency ranges. The default setting is “enabled”.
- **CPU C States**
  This item allows users to enable/disable CPU C states. The default setting is “enabled”.

4.3.1.7 SATA Configuration



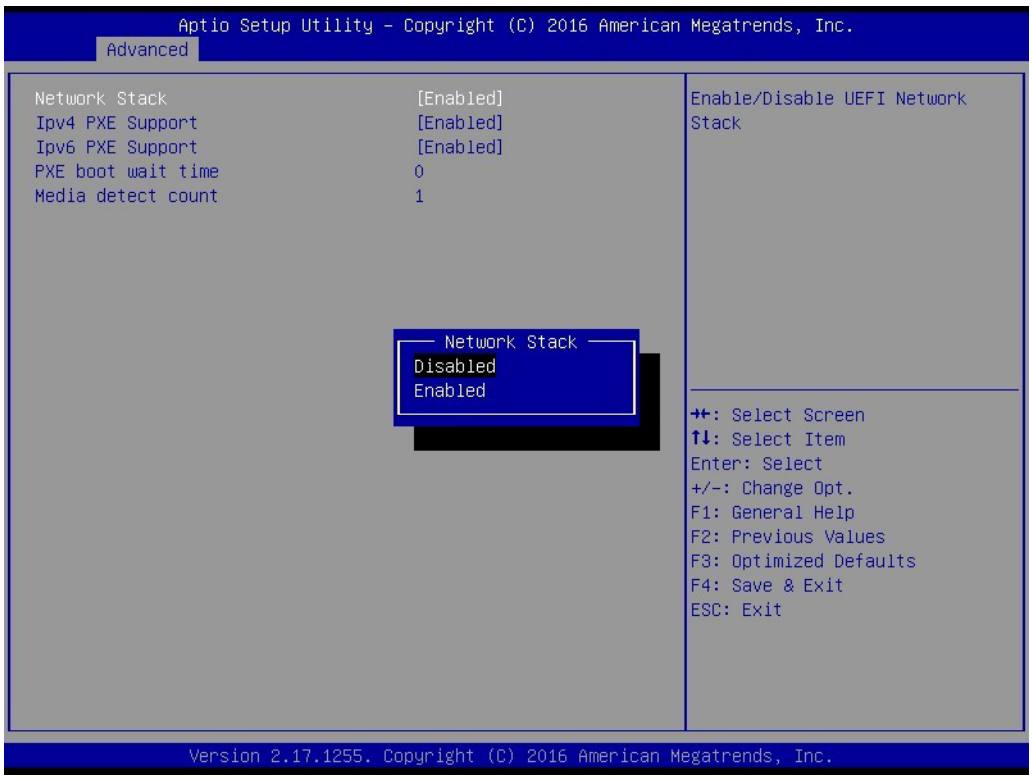
- **SATA Controller(s)**
  This item allows users to enable/disable SATA controllers. The default setting is “enabled”.
- **SATA Mode Selection**
  This item allows users to set the SATA mode as AHCI or RAID. The default setting is “AHCI”.
- **SATA Port 0/1/2/MSATA**
  This item allows users to enable/disable the SATA ports. The default setting is “enabled”.
- **Hot Plug**
  This item allows users to enable/disable hot plugging. The default setting is “enabled”.

4.3.1.8 Network Stack Configuration



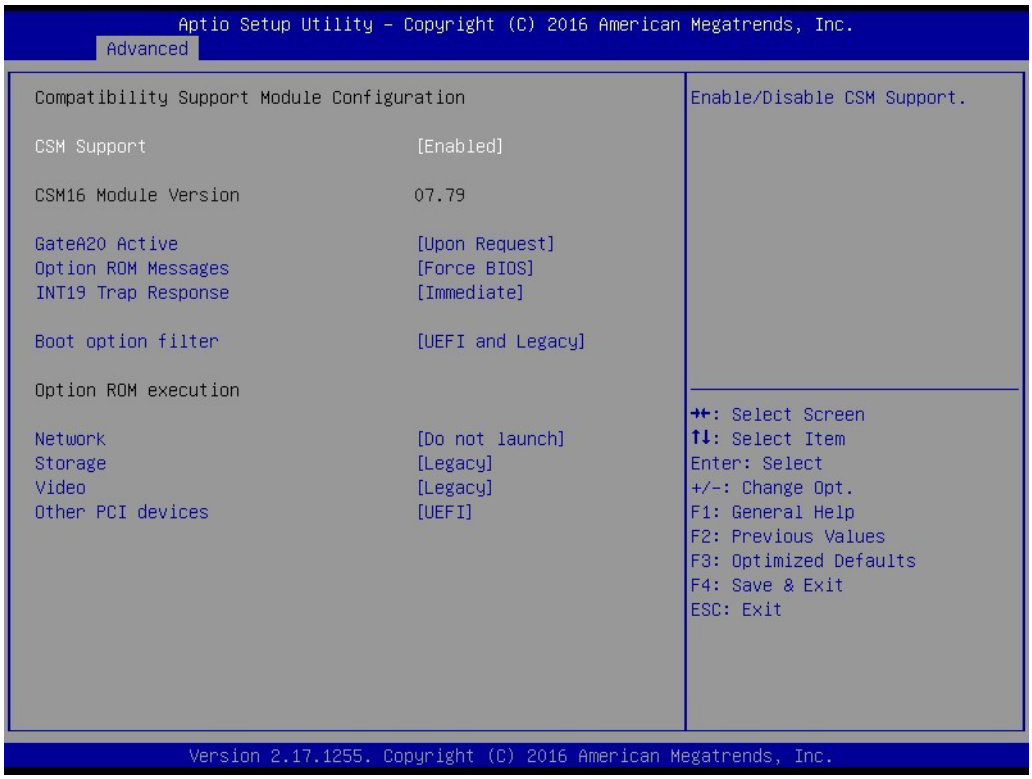
- **Network Stack**
  This item allows users to enable/disable the UEFI network stack. The default setting is “disabled”.

When the network stack is enabled, the followed page will be accessible:



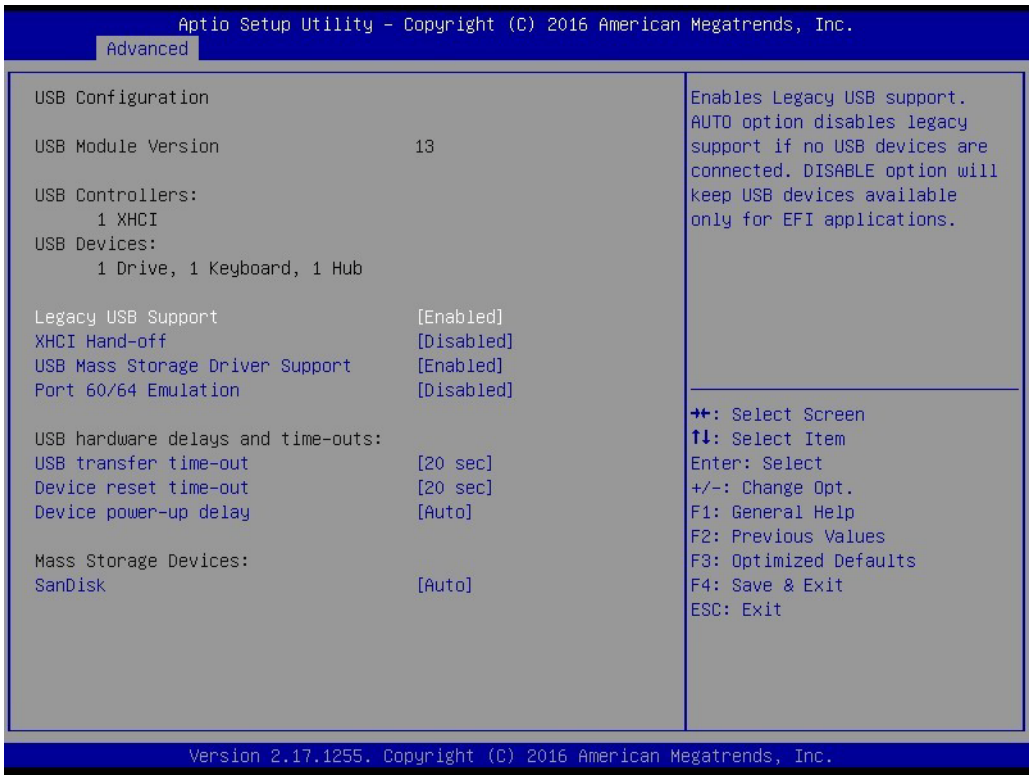
- **Ipv4 PXE Support**
  This item allows users to enable/disable IPV4 PXE support. If disabled, the IPV4 PXE boot option will not be created.
- **Ipv6 PXE Support**
  This item allows users to enable/disable IPV6 PXE support. If disabled, the IPV6 PXE boot option will not be created.
- **PXE Boot Wait Time**
  This item allows users to set the wait time for pressing <ESC> to abort PXE boot.
- **Media Detect Count**
  This item allows users to set the number of times that the presence of media is checked.

4.3.1.9 CSM Configuration



- **CSM Support**
  This item allows users to enable/disable CSM support. The default setting is "enabled".
- **GateA20 Active**
  This item is useful when the RT code is executed above 1 MB. When this is set as "upon request", GA20 can be disabled in the BIOS utility. When set as "always", GA20 cannot be disabled.
- **Option ROM Messages**
  This item allows users to set the display mode for the option ROM.
- **INT19 Trap Response**
  This item allows users to set the BIOS reaction to INT19 trapping by the option ROM. With the "Immediate" option, the trap is executed immediately; with "postponed," the trap is executed during legacy boot.
- **Boot Option Filter**
  This item allows users to set the legacy/UEFI ROM priority.
- **Network**
  This item allows users to control the execution of UEFI and legacy PXE OpRom.
- **Storage**
  This item allows users to control the execution of UEFI and legacy storage OpRom.
- **Video**
  This item allows users to control the execution of UEFI and legacy video OpRom.
- **Other PCI Devices**
  This item allows users to determine the OpRom execution policy for other devices.

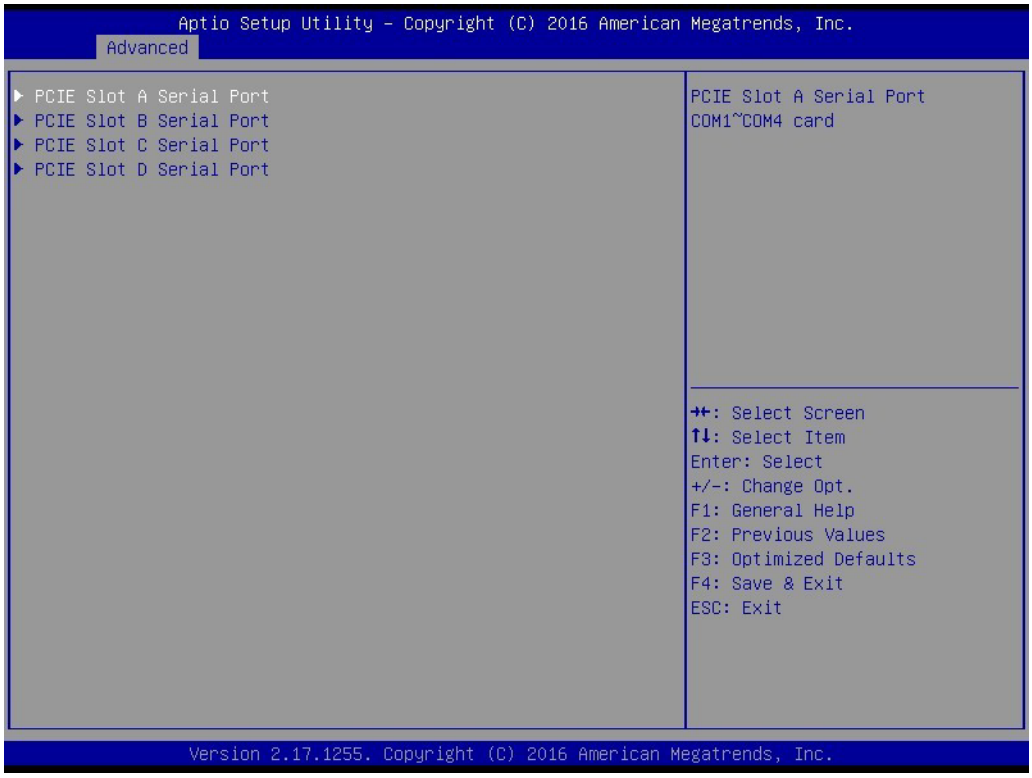
4.3.1.10 USB Configuration

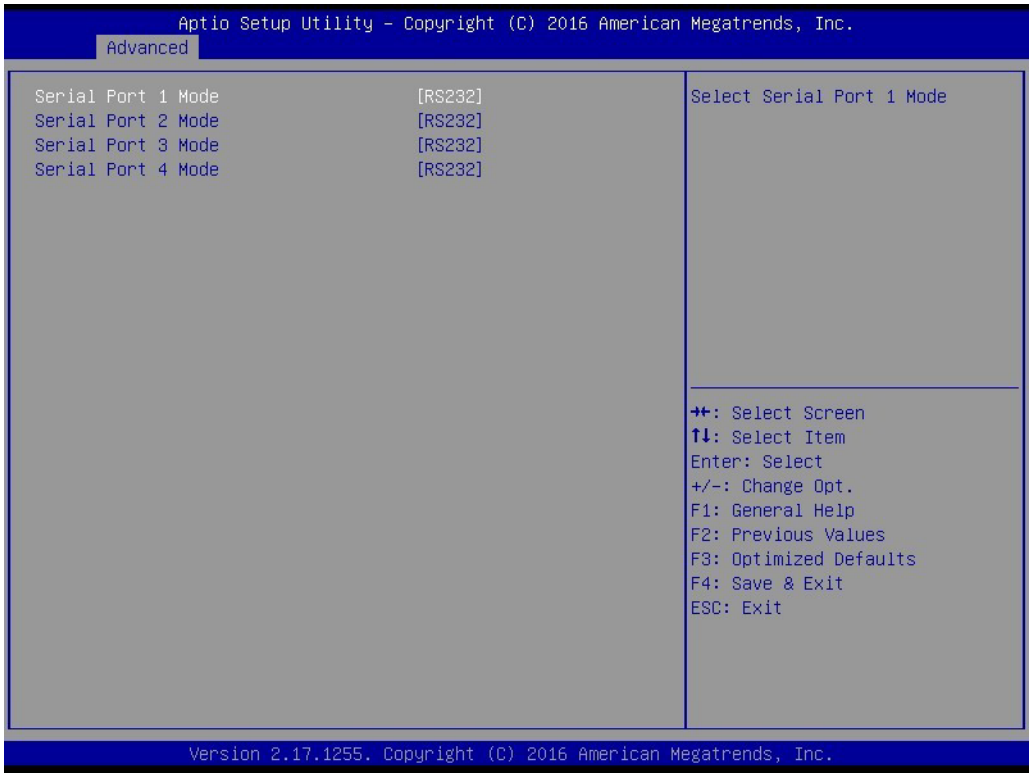


- **Legacy USB Support**
  This item allows users to enable/disable legacy USB support. The default settings is “enabled”.
- **XHCI Hand-off**
  This item is a workaround for OS without XHCI hand-off support. The XHCI ownership changes should be conducted by the XHCI driver.
- **USB Mass Storage Driver Support**
  This item allows users to enable/disable USB mass storage driver support.
- **Port 60/64 Emulation**
  This item allows users to enable/disable support for I/O port 60h/64h emulation. This should be enabled for complete USB keyboard legacy support for non-USB aware OS.
- **USB Transfer Timeout**
  This item allows users to set the timeout value for control, bulk, and interrupt transfers.
- **Device Power-Up Delay**
  This item allows users to set the timeout value for the USB device start unit command.

4.3.1.11 PCIE COM Port Configuration

ITA-5231 supports four PCIE serial ports. Users can configure the serial ports with the following settings:



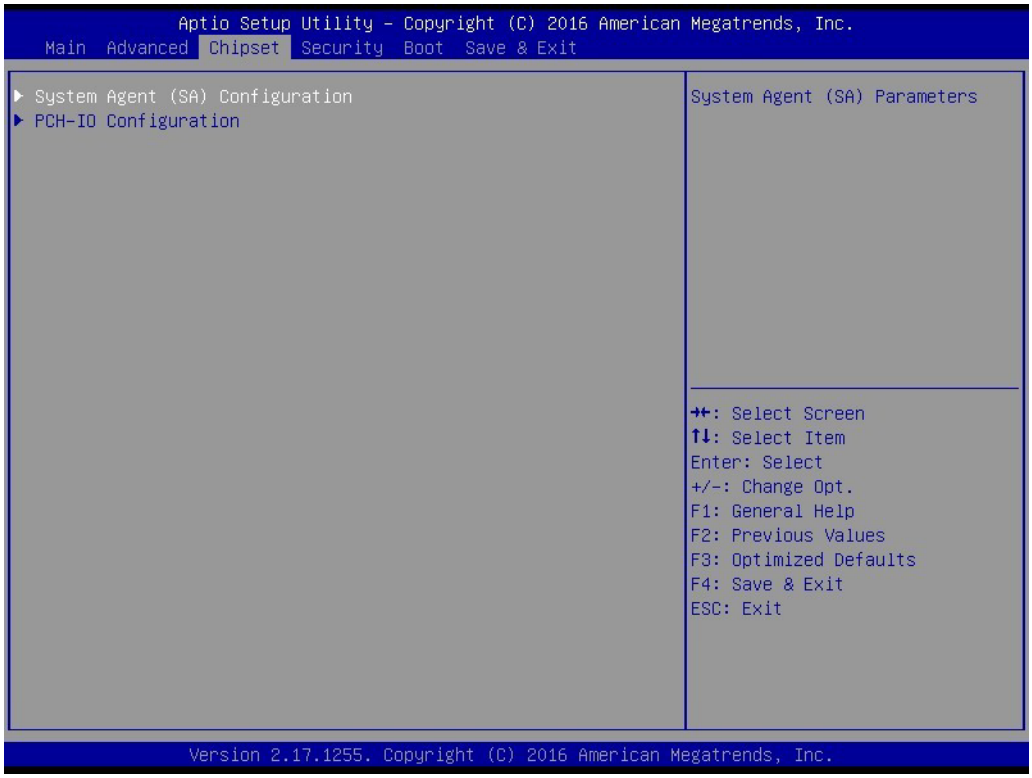


- **Serial Port 1/2/3/4 Mode**

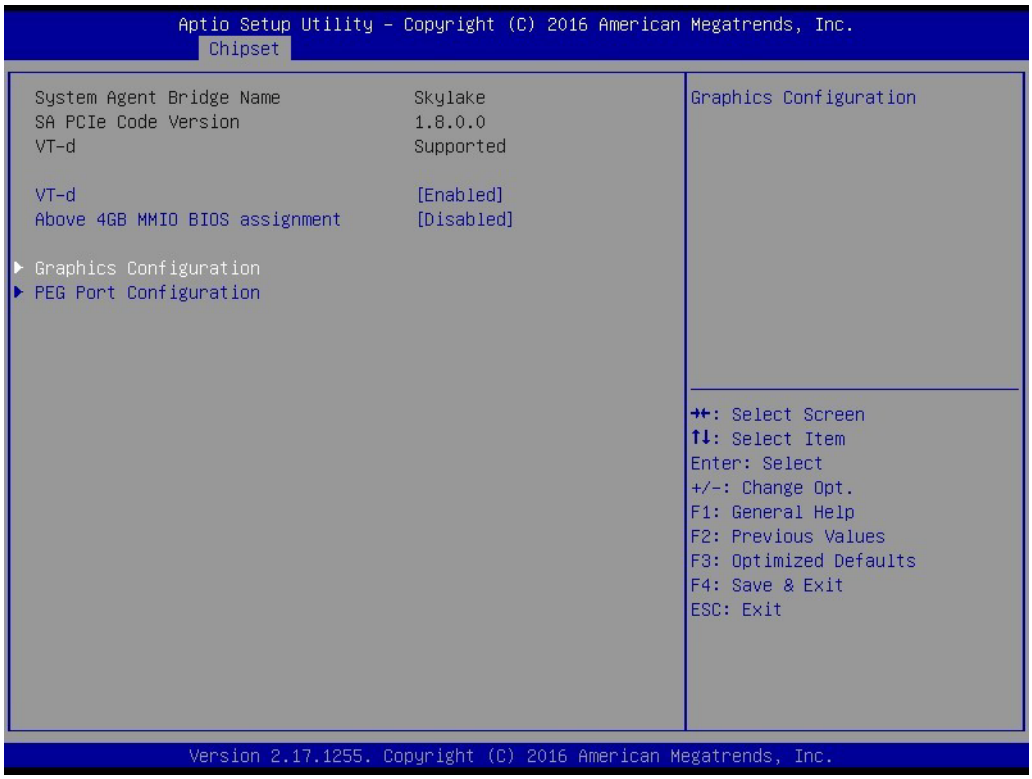
  This item allows users to set the serial port mode as RS-232, RS-422, or RS-485. The default setting is “RS-232”.

4.3.2 Chipset Configuration

The PCH and SA setting can be configured via the Chipset Configuration sub-page.

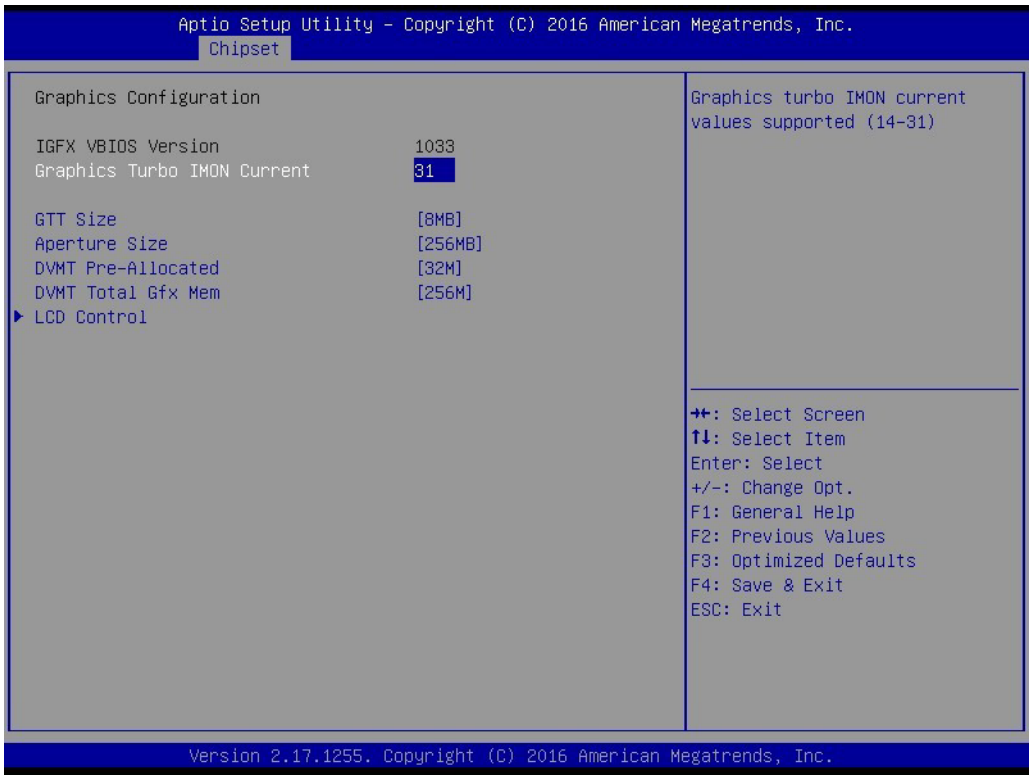


4.3.2.1 System Agent Configuration



- **VT-d**
  This item allows users to enable/disable VT-d function.
- **Above 4GB MMIO BIOS assignment**
  This item allows users to enable/disable above 4 GB MMIO BIOS assignment. When the aperture size is 2048 MB, this function is automatically disabled.
- **Graphics Configuration**
  This item allows users to configure the graphics settings.
- **PEG Port Configuration**
  This item allows users to configure PEG ports settings.

4.3.2.2 Graphics Configuration



- **IGFX VBIOS Version**
  This item allows users to view the current VBIOS version.
- **Graphics Turbo IMON Current**
  This item allows users to set the graphics turbo IMON current values (14 ~ 31).
- **GTT Size**
  This item allows users to select the GTT size.
- **Aperture Size**
  This item allows users to select the aperture size. If 2048 MB aperture is selected, CSM support must be disabled.
- **DVMT Pre-Allocated**
  This item allows users to select the DVMT 5.0 pre-allocated (fixed) graphics memory size used by the internal graphics device.
- **DVMT Total GFX Mem**
  This item allows users to select the DVMT 5.0 total graphics memory size used by the internal graphics device.
- **LCD Control**
  Refer to the next page.

- **Primary IGFX Boot Display**

  This item allows users to select the primary video device to be activated during POST. The options are HDMI, DVI, eDP panel, and VGA. The secondary boot display options will depend on the initial selection.

- **eDP LVDS Panel Type**

  This item allows users to select the eDP LVDS panel type.

- **Panel Scaling**

  This item allows users to configure the panel scaling function for the internal graphics device.

- **Backlight Control**

  This item allows users to control the backlight type.

- **Spread Spectrum Clock Chip**

  This item allows users to set the type of spread spectrum clock type. With the “hardware” option, spread is controlled by the chip; with the “software” option, spread is controlled by the BIOS settings.

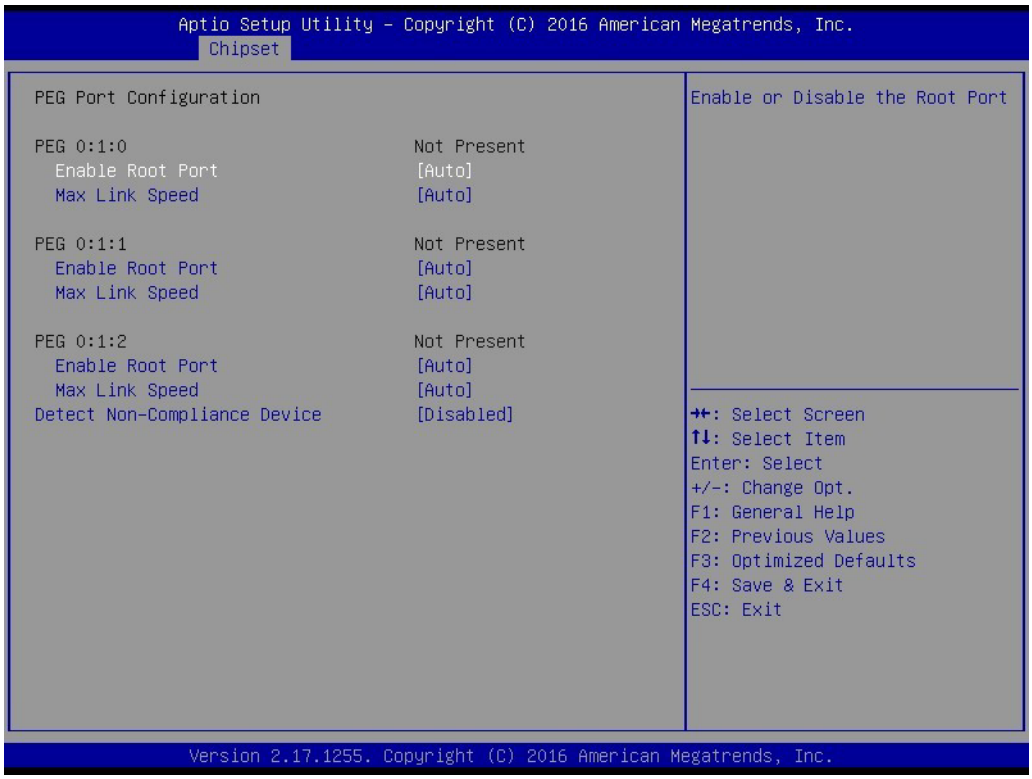
- **Active LFP**

  This item allows users to configure LFP usage.

- **Panel Color Depth**

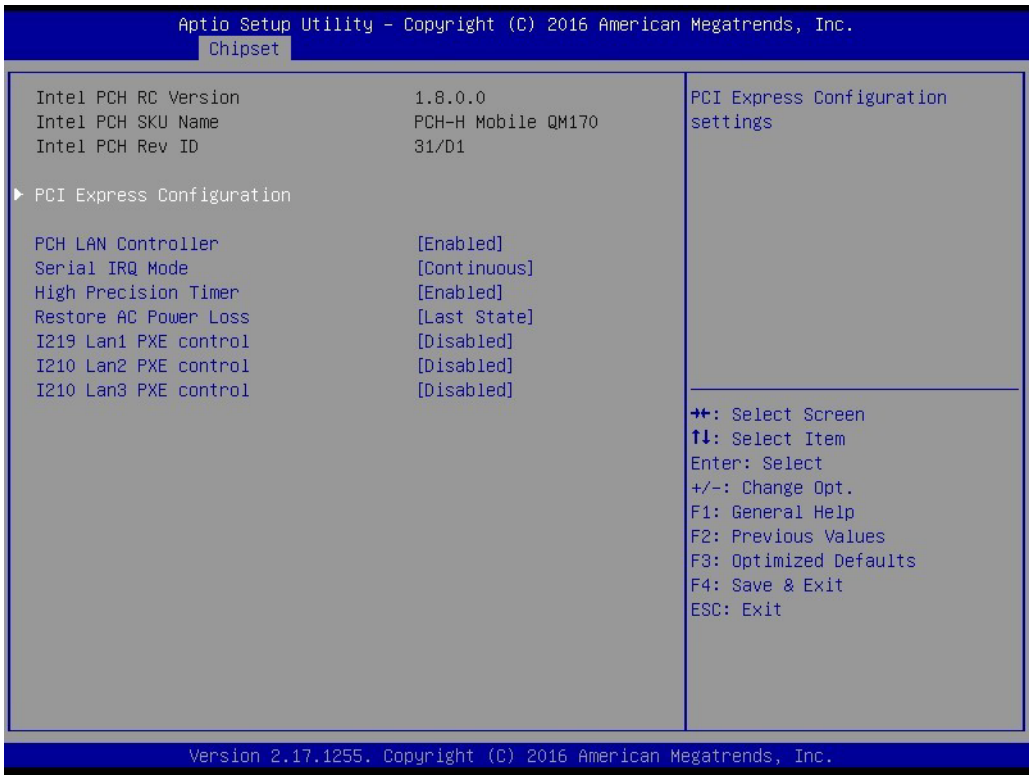
  This item allows users to set the LFP color depth.

4.3.2.3 PEG Port Configuration



- **Enable Root Port**
  This item allows users to enable/disable the root port.
- **Max Link Speed**
  This item allows users to configure the PEG port's max. link speed.
- **Detect Non-Compliant Device**
  This item allows users to enable/disable the detect non-compliant PCIE device function.

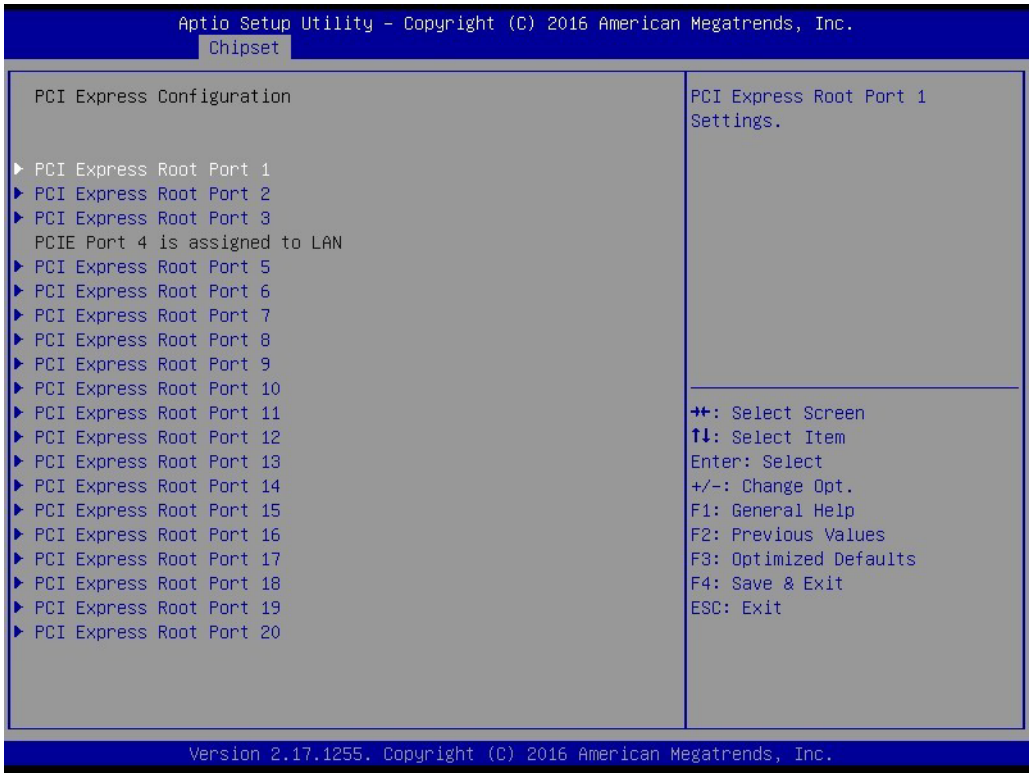
4.3.2.4 PCH-IO Configuration

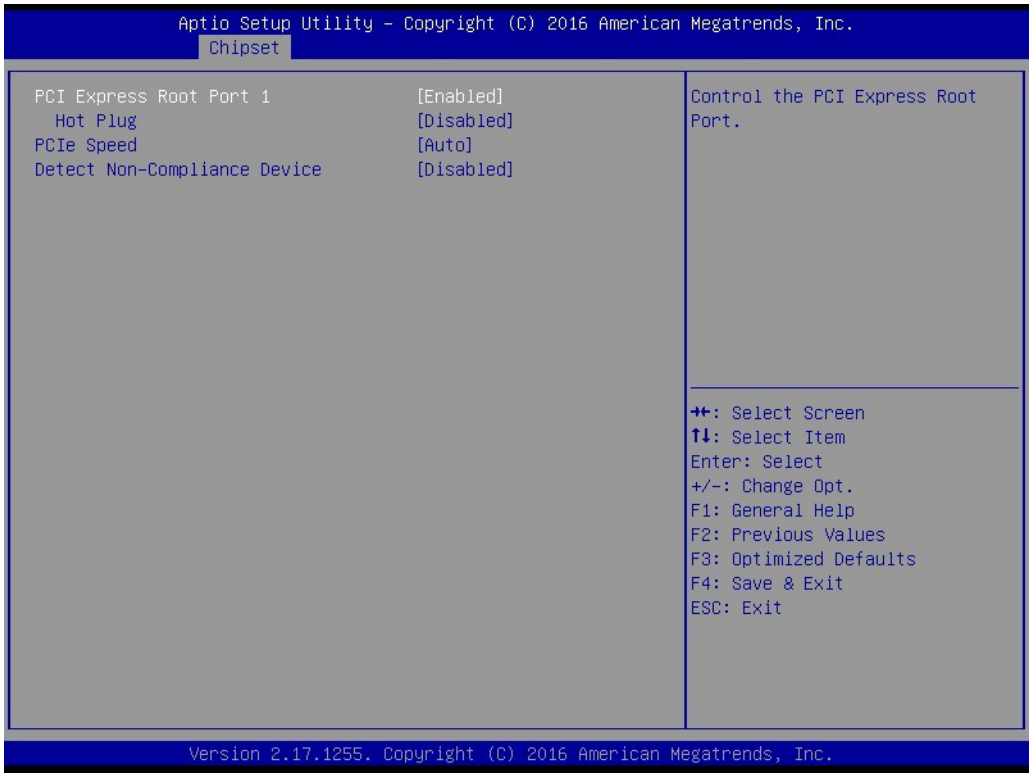


- **Intel PCH RC Version**
  This item allows users to view the current Intel PCH RC version.
- **Intel PCH SKU Name**
  This item allows users to view the current Intel PCH SKU name.
- **Intel PCH Rev ID**
  This item allows users to view the current Intel PCH reversion ID.
- **PCI Express Configuration**
  This item allows users to configure the PCI Express port.
- **PCH LAN Controller**
  This item allows users to enable/disable onboard NIC.
- **Serial IRQ Mode**
  This item allows users to select the serial IRQ mode.
- **High-Precision Timer**
  This item allows users to enable/disable the high-precision event timer.
- **Restore AC Power Loss**
  This item allows users to set the AC power state when power is restored after a power failure.
- **I219/I210 LAN PXE Control**
  This item allows users to enable/disable LAN PXE function.

4.3.2.5 PCI Express Configuration

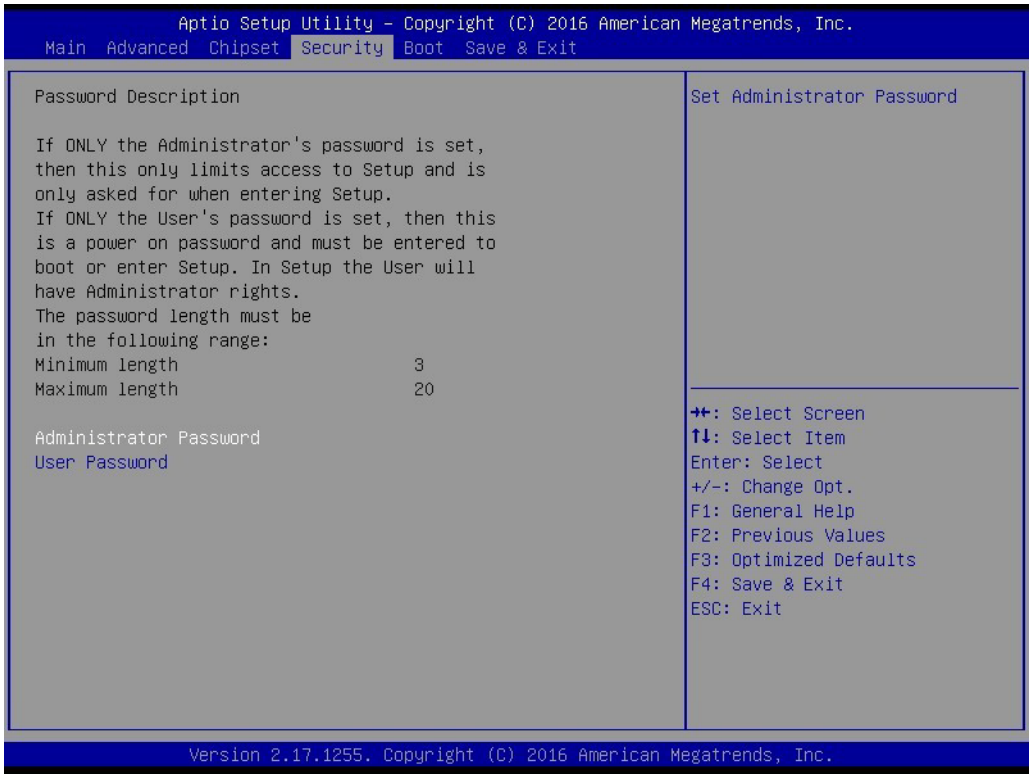
This page shows that the PCH supports the PCIE root ports. PCIE port 4 is assigned to i219 LAN. The items for configuration are show below.





- **PCI Express Root Port**
  This item allows users to configure the PCI Express root port.
- **Hot Plug**
  This item allows users to enable/disable PCI Express hot plugging.
- **PCIe Speed**
  This item allows users to set the PCI Express port speed.
- **Detect Non-Compliant Device**
  This item allows users to enable/disable the detect non-compliant PCI Express device function. If enabled, the system will take longer to complete POST.

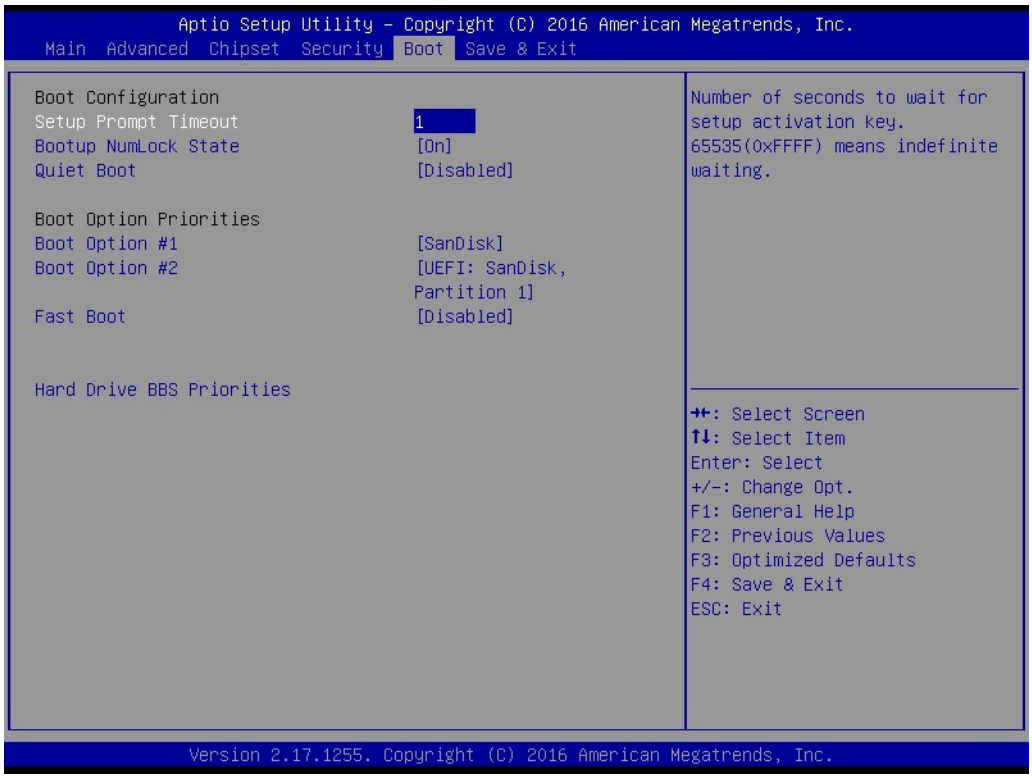
4.3.3 Security Configuration



In the BIOS Setup utility, select the Security tab. To access the submenu for any of the items, select the item and press <Enter>.

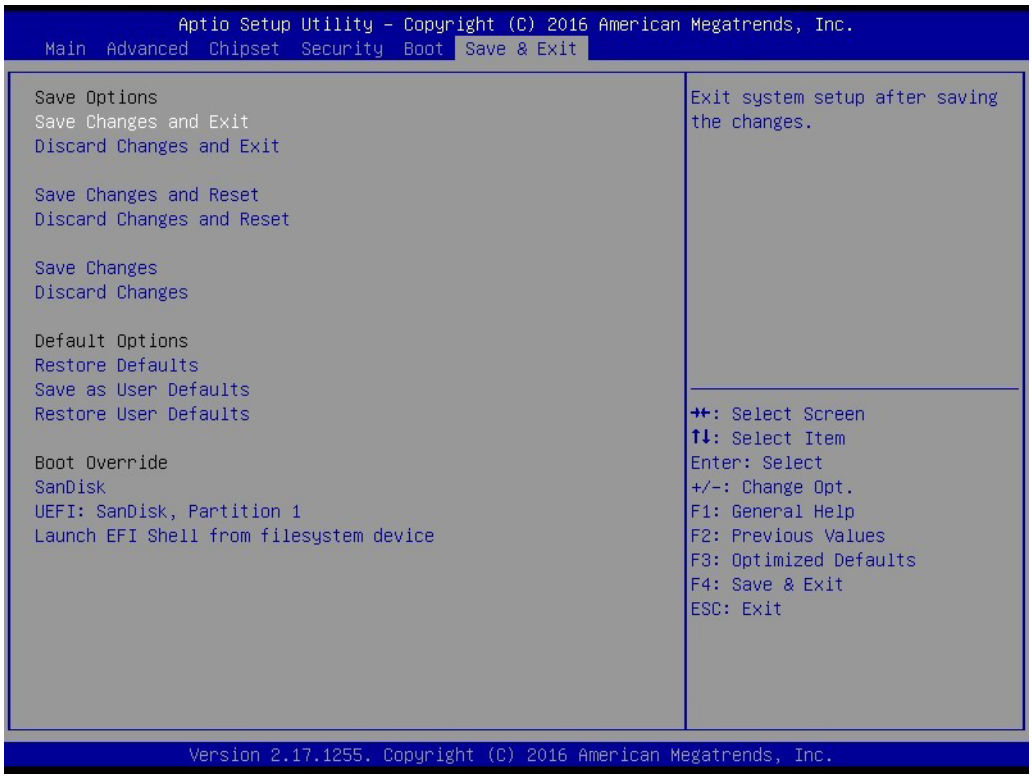
- **Administrator Password**
  This item allows users to set the administrator password. The ideal password length is between 3 and 20 characters.
- **User Password**
  This item allows users to set user passwords. The ideal password length is between 3 and 20 characters.

4.3.4 Boot Configuration



- **Setup Prompt Timeout**
  This item allows users to set the number of seconds to wait for the setup activation key. The default setting is “1”.
- **Bootup NumLock State**
  This item allows users to set the <NumLock> state during bootup. The default setting is “on”.
- **Quiet Boot**
  This item allows users to enable/disable quiet bootup. The default setting is “disabled”.
- **Boot Option Priorities**
  This item allows users to view the system boot order.
- **Fast Boot**
  This item allows users to enable/disable fast boot by initializing the minimum number of devices.
- **Hard Drive BBS Priorities**
  This item allows users to set the priority of legacy devices in this group.

4.3.5 Save & Exit



- **Save Changes and Exit**
  This item allows users to exit the BIOS utility after saving all changes.
- **Discard Changes and Exit**
  This item allows users to exit the BIOS utility without saving any changes.
- **Save Changes and Reset**
  This item allows users to reset the system after saving all changes.
- **Discard Changes and Reset**
  This item allows users to reset the system without saving any changes.
- **Save Changes**
  This item allows users to save all changes to any of the setup options.
- **Discard Changes**
  This item allows users to discard any changes to any of the setup options.
- **Restore Defaults**
  This item allows users to restore the default values for the setup options.
- **Save as User Defaults**
  This item allows users to save all current settings as user defaults.
- **Restore User Defaults**
  This item allows users to restore all settings to the user defaults.

Chapter 5

Driver Installation

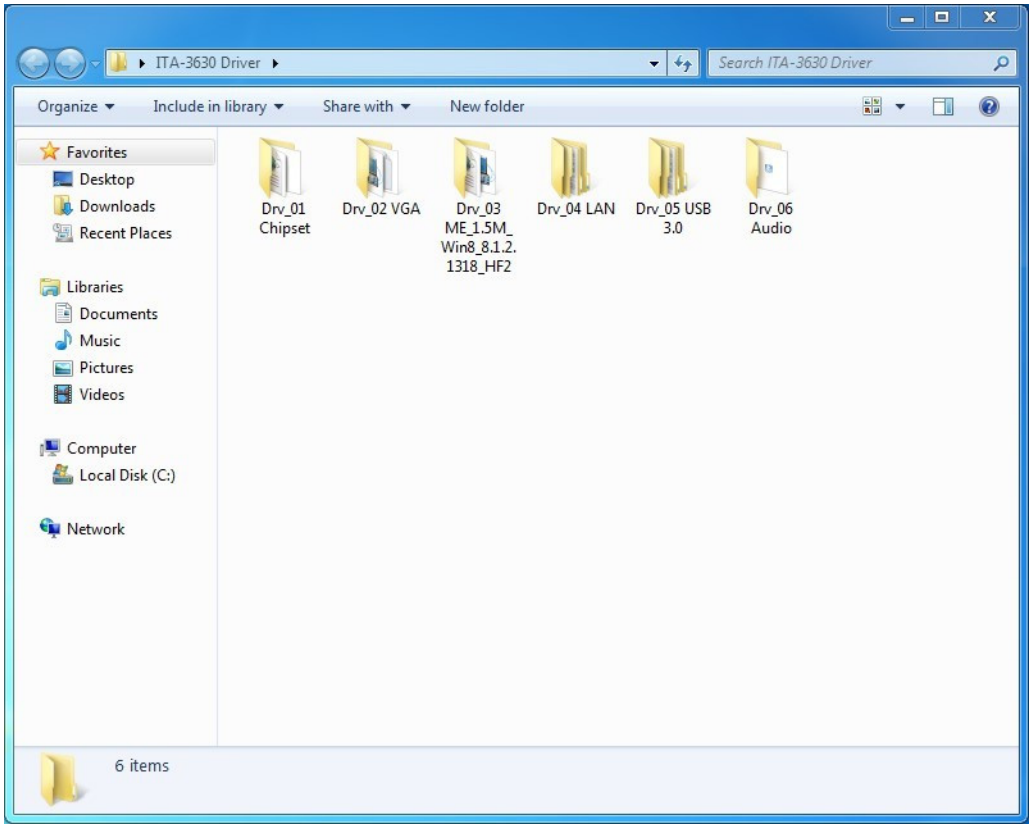
- Chipset Windows Driver Setup
- VGA Windows Driver Setup
- ME Windows Driver Setup
- LAN Windows Driver Setup
- USB 3.0 Windows Driver Setup

5.1 Introduction

Advantech offers a complete range of device drivers and software supports for Windows program developers. Windows device drivers can be applied to the most popular Windows programming tools, such as Visual C++, Visual Basic, Borland C++ Builder, and Borland Delphi. In this Chapter, Windows 7 is used as the example.

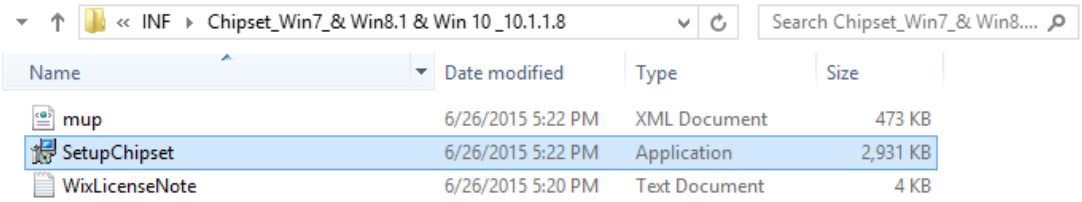
5.2 Driver Installation

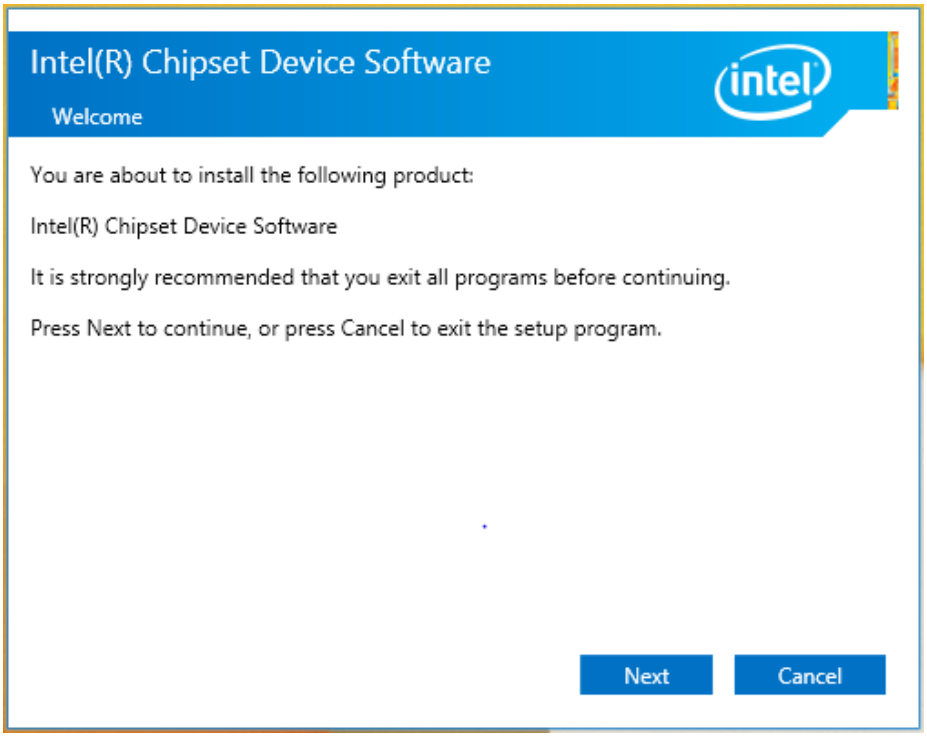
Insert the driver CD into the system's CD-ROM drive. The ITA-5231 driver folder items should appear as shown in the image below.

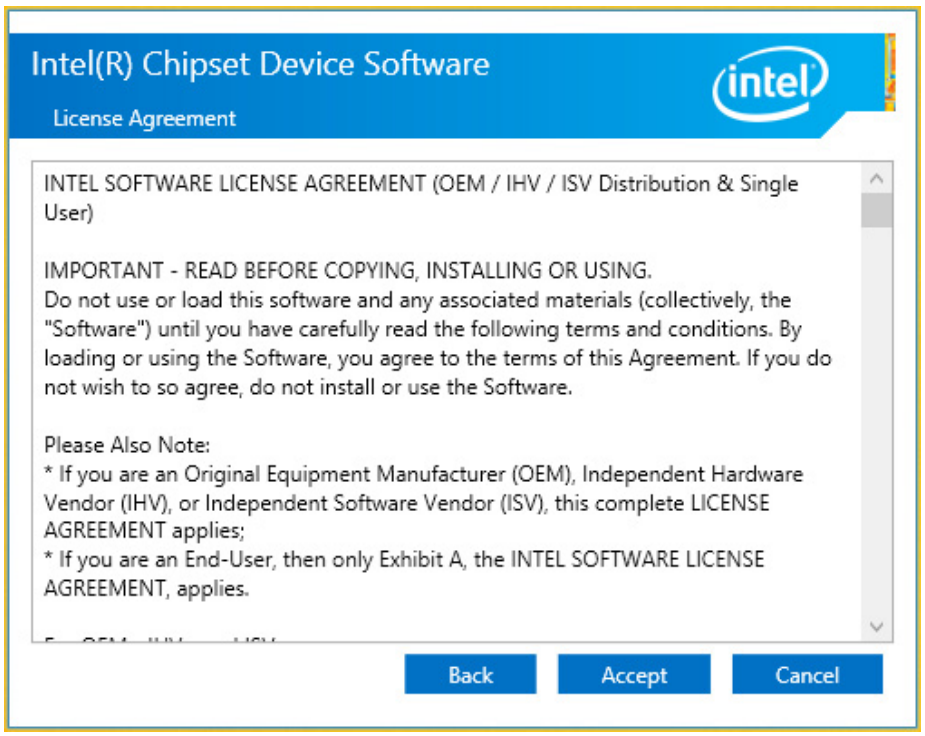


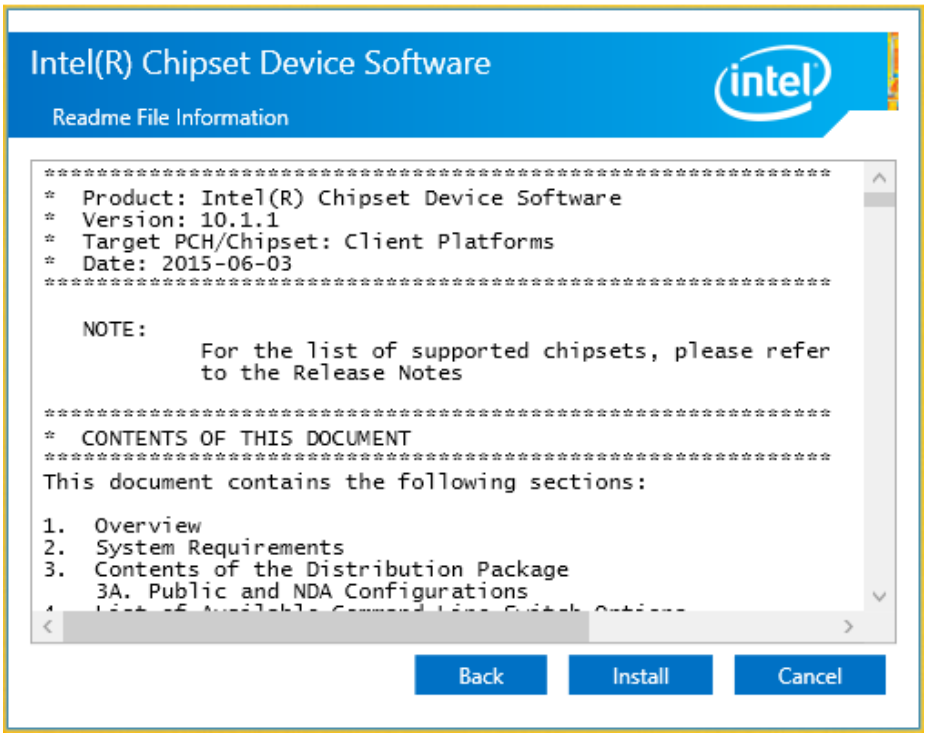
5.2.1 Chipset Windows Driver Setup

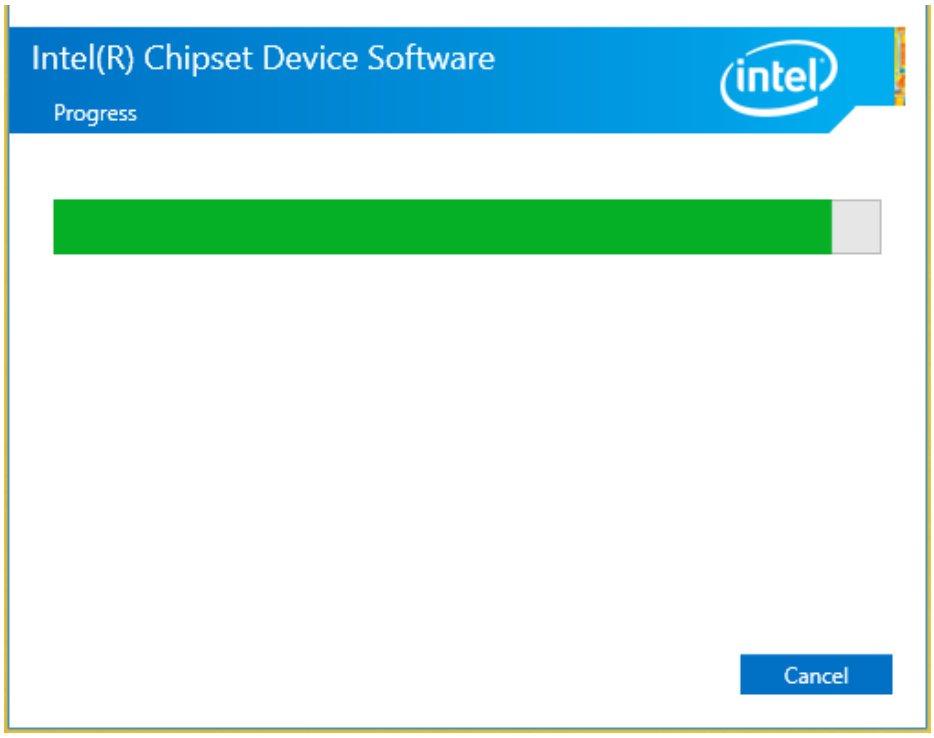
Insert the driver CD into the system's CD-ROM drive. The driver folder items should appear as shown in the image below. Navigate to the "INF" folder and click "Setup" to complete the installation.

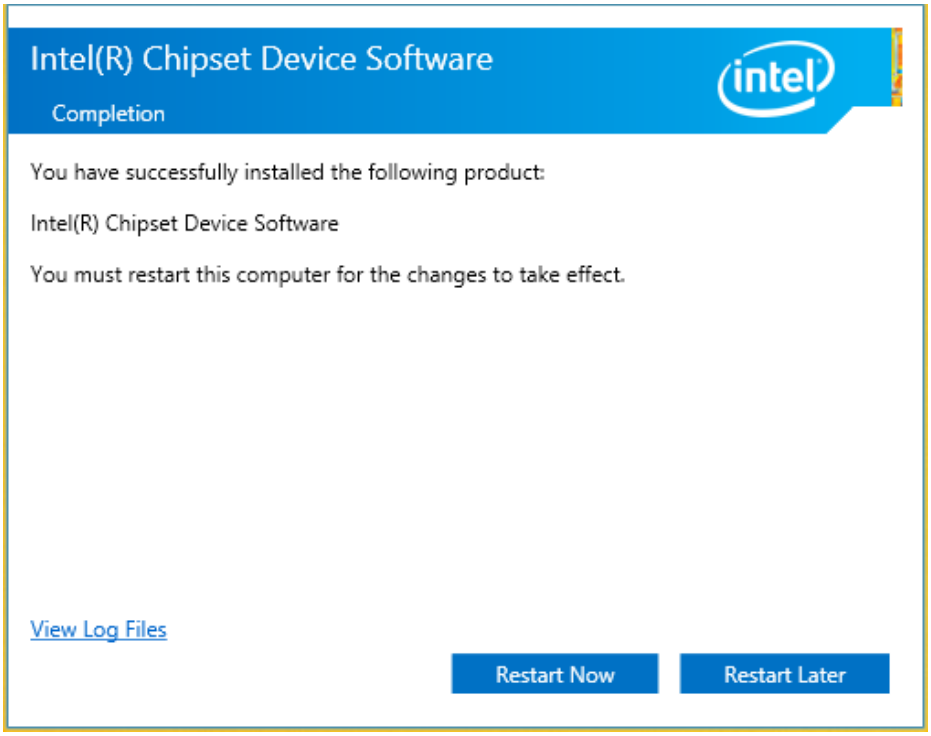





Intel(R) Chipset Device Software
License Agreement
INTEL SOFTWARE LICENSE AGREEMENT (OEM / IHV / ISV Distribution & Single User)
IMPORTANT - READ BEFORE COPYING, INSTALLING OR USING.
Do not use or load this software and any associated materials (collectively, the "Software") until you have carefully read the following terms and conditions. By loading or using the Software, you agree to the terms of this Agreement. If you do not wish to so agree, do not install or use the Software.
Please Also Note:
* If you are an Original Equipment Manufacturer (OEM), Independent Hardware Vendor (IHV), or Independent Software Vendor (ISV), this complete LICENSE AGREEMENT applies;
* If you are an End-User, then only Exhibit A, the INTEL SOFTWARE LICENSE AGREEMENT, applies.
Back
Accept
Cancel

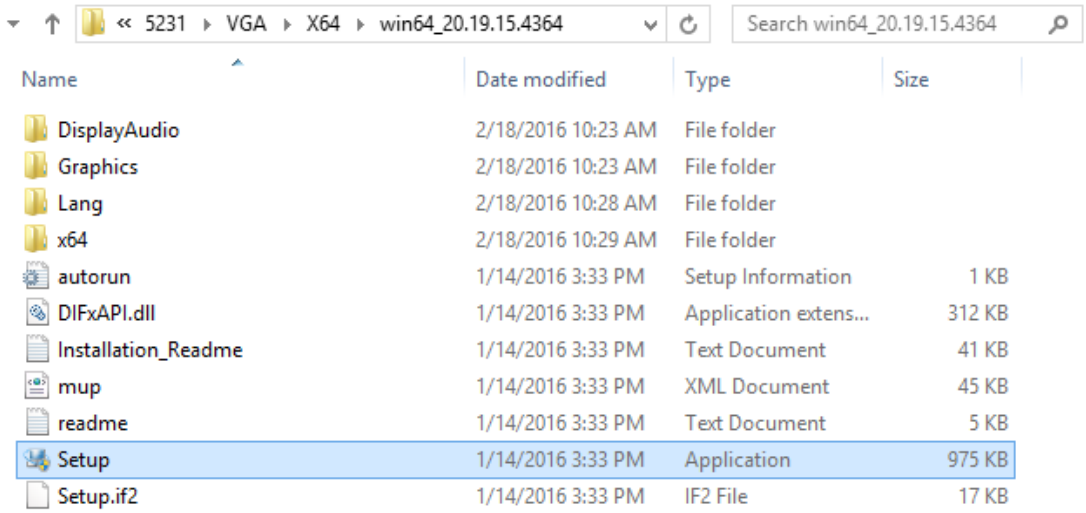

Intel(R) Chipset Device Software
Readme File Information
* Product: Intel(R) Chipset Device Software
* Version: 10.1.1
* Target PCH/Chipset: Client Platforms
* Date: 2015-06-03
NOTE:
For the list of supported chipsets, please refer to the Release Notes
* CONTENTS OF THIS DOCUMENT
This document contains the following sections:
1. Overview
2. System Requirements
3. Contents of the Distribution Package
3A. Public and NDA Configurations
Back
Install
Cancel


Intel(R) Chipset Device Software
Progress
Cancel


Intel(R) Chipset Device Software
Completion
You have successfully installed the following product:
Intel(R) Chipset Device Software
You must restart this computer for the changes to take effect.
View Log Files
Restart Now
Restart Later

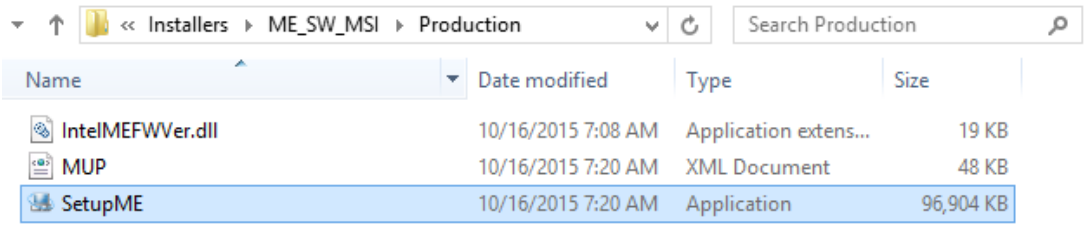
5.2.2 VGA Windows Driver Setup

Insert the driver CD into the system's CD-ROM drive. The driver folder items should appear as shown in the image below. Navigate to the "ME" folder and click "Setup" to complete the driver installation.



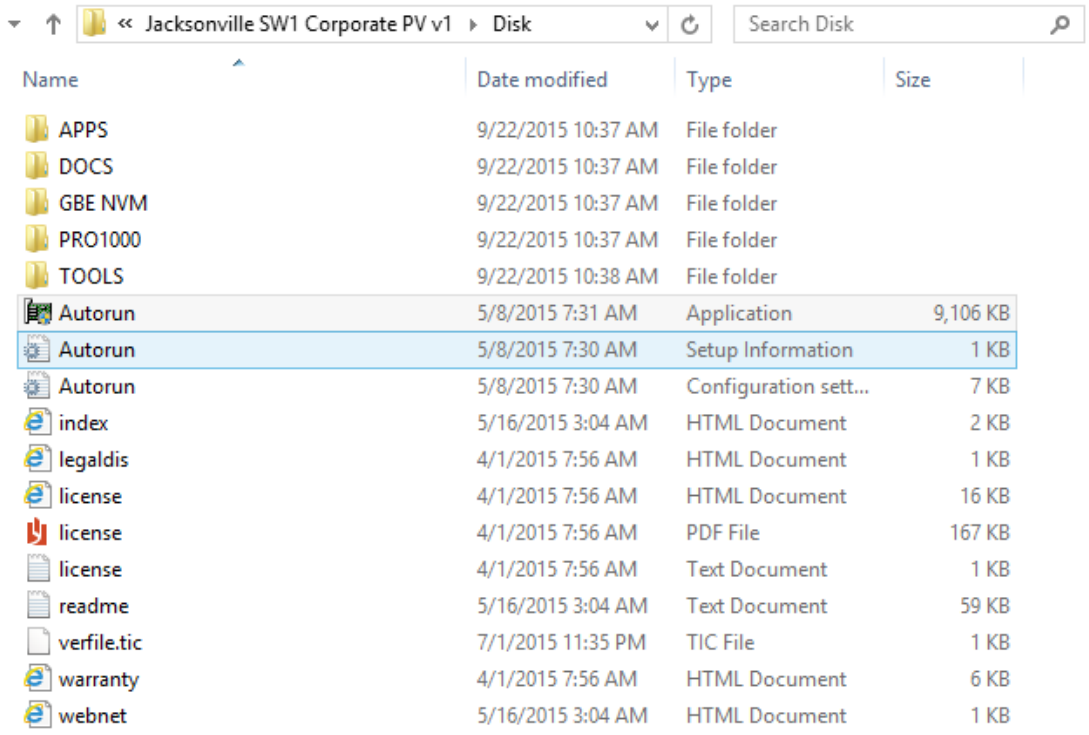
5.2.3 ME Windows Driver Setup

Insert the driver CD into the system's CD-ROM drive. The driver folder items should appear as shown in the image below. Navigate to the "VGA" folder and click "Setup" to complete the driver installation.



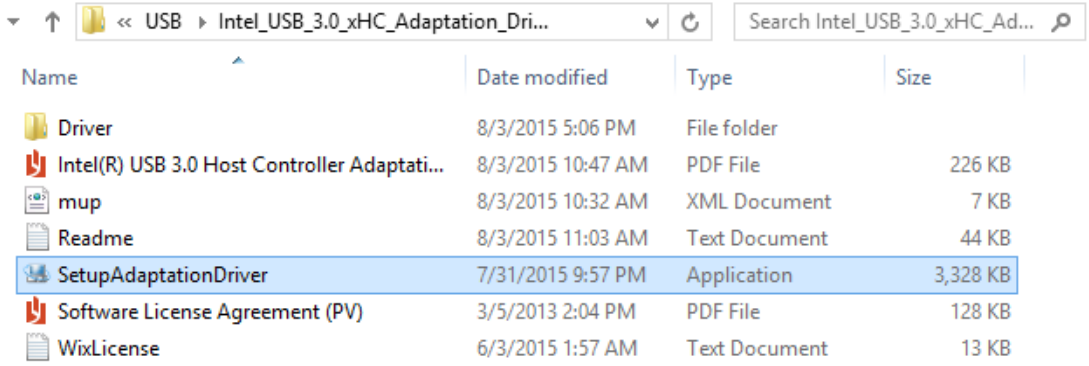
5.2.4 LAN Windows Driver Setup

Insert the driver CD into the system's CD-ROM drive. The driver folder items should appear as shown in the image below. Navigate to the "LAN" folder and click "Setup" to complete the driver installation.



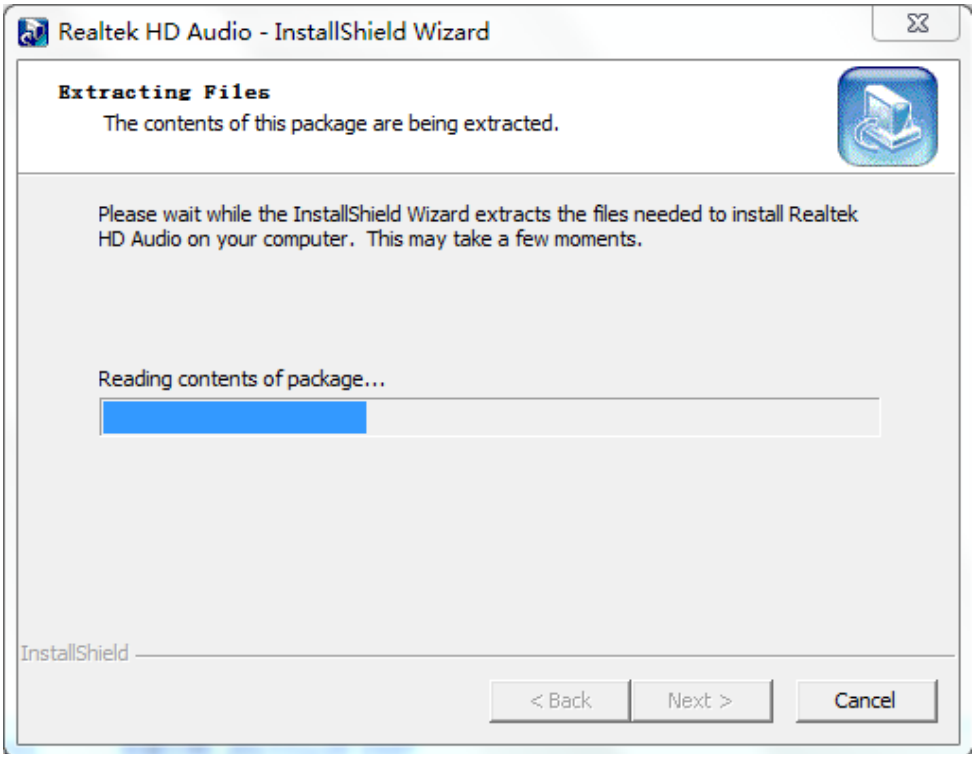
5.2.5 USB 3.0 Windows Driver Setup

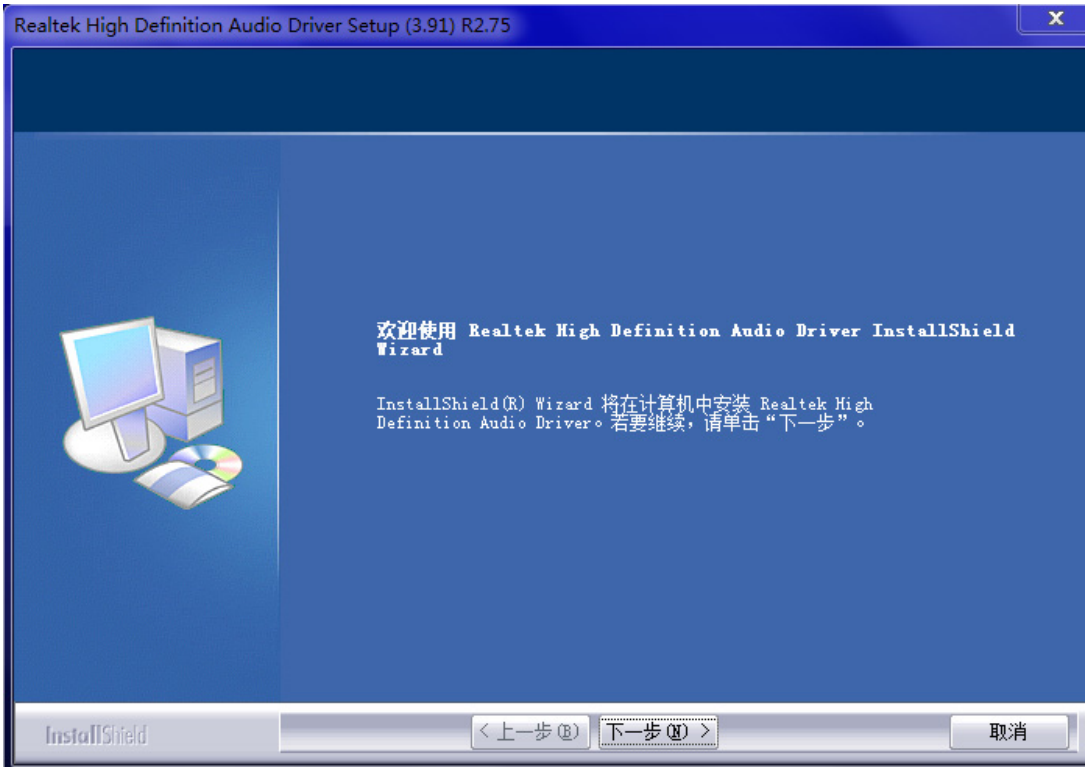
Insert the driver CD into the system's CD-ROM driver. The driver folder items should appear as shown in the image below. Navigate to the "USB" folder and click "Setup" to complete the driver installation.

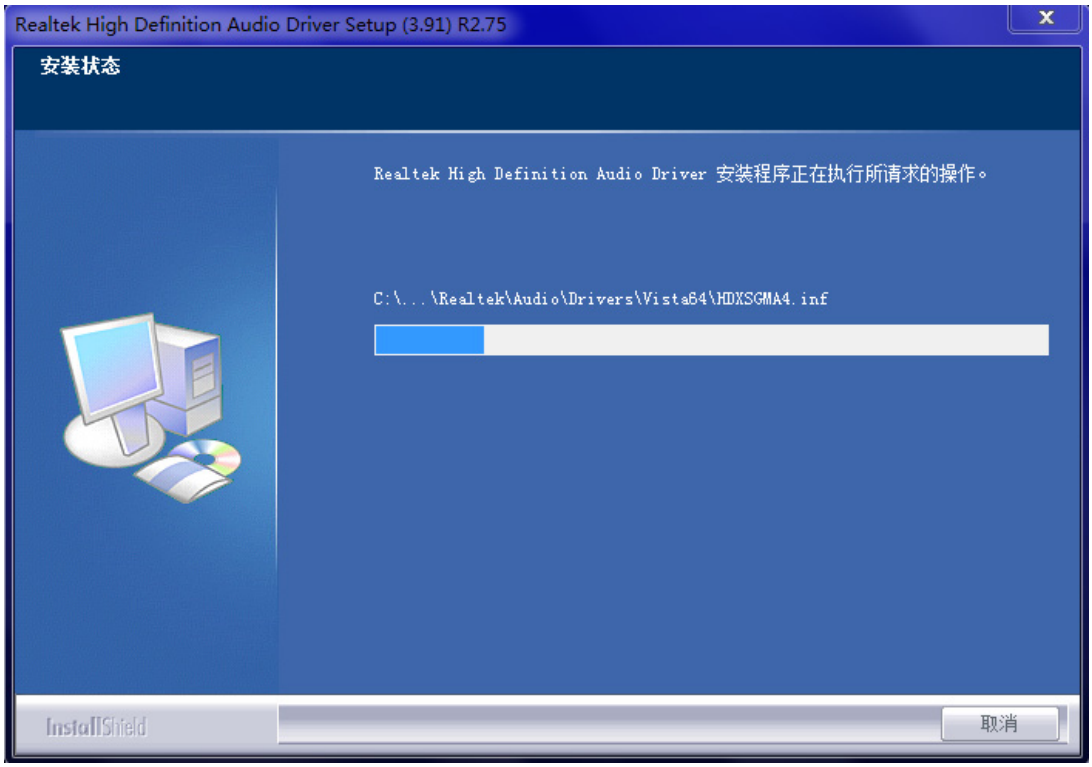


5.2.6 Audio Windows Driver Setup

Insert the driver CD into the system's CD-ROM driver. The driver folder items should appear as shown in the image below. Navigate to the "Audio" folder and click "Setup" to complete the driver installation.


Realtek HD Audio - InstallShield Wizard
Extracting Files
The contents of this package are being extracted.
Please wait while the InstallShield Wizard extracts the files needed to install Realtek HD Audio on your computer. This may take a few moments.
Reading contents of package...
InstallShield
< Back
Next >
Cancel


Realtek High Definition Audio Driver Setup (3.91) R2.75
欢迎使用 Realtek High Definition Audio Driver InstallShield Wizard
InstallShield(R) Wizard 将在计算机中安装 Realtek High Definition Audio Driver。若要继续，请单击“下一步”。
InstallShield
< 上一步(B)
下一步(N) >
取消


Realtek High Definition Audio Driver Setup (3.91) R2.75
安装状态
Realtek High Definition Audio Driver 安装程序正在执行所请求的操作。
C:\...\Realtek\Audio\Drivers\Vista64\HDXSGMA4.inf
InstallShield
取消

Chapter 6

GPIO Programming Guide

Note!

Download the specifications for programming the NXP Semiconductors' PCA9554 GPIO IC from the NXP website.

https://www.nxp.com/docs/en/data-sheet/PCA9554_9554A.pdf?fsrch=1&sr=1&pageNum=1

6.1 Digital DI/O Definition

See Section 2.3.3.

6.2 Configuration Sequence

ITA-5231's GPIO is realized through the PCA9554 GPIO IC connected to ICH SMBUS. Therefore, the GPIO IC is configured and accessed through I/O space via the ICH SMBUS controller.

Table 6.1: ICH SMBUS I/O Space

SMB_BASE+ Offset	Mnemonic	Registration Name	Default	Type
00h	HST_STS	Host status	00h	R/WC, RO, R/WC (special)
02h	HST_CNT	Host control	00h	R/W, W O
03h	HST_CMD	Host command	00h	R/W
04h	XMIT_SLVA	Transmit slave address	00h	R/W
05h	HST_D0	Host data 0	00h	R/W
06h	HST_D1	Host data 1	00h	R/W

For ITA-5231, the I/O address of the above SMB_BASE is 0xF040. The corresponding SMBUS slave address of PCA9554 for GPIO 00 ~ GPIO 07 on ITA-5231 is 0x40 (8bit address): GPIO 00 ~ GPIO 07: PCA9554 0x40 (IO0 ~ IO7)

Table 6.2: Pin Definitions

Symbol	Pin DIP16, SO16, SSOP16, TSSOP16	HVQFN16	SSOP20	Description
A0	1	15	6	Address input 0
A1	2	16	7	Address input 1
A2	3	1	9	Address input 2
IO0	4	2	10	Input/output 0
IO1	5	3	11	Input/output 1
IO2	6	4	12	Input/output 2
IO3	7	5	14	Input/output 3
VSS	8	6	15	Supply ground
IO4	9	7	16	Input/output 4
IO5	10	8	17	Input/output 5
IO6	11	9	19	Input/output 6
IO7	12	10	20	Input/output 7
INT	13	11	1	Interrupt output (open-drain)
SCL	14	12	2	Serial clock line
SDA	15	13	4	Serial data line
VDD	16	14	5	Supply voltage
n.c.	-	-	3,8,13,18	Not connected

6.2.1 Command Byte

Table 6.3: Command Byte

Command	Protocol	Function
0	Read byte	Input port register
1	Read/write byte	Output port register
2	Read/write byte	Polarity inversion register
3	Read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read. PCA9554 has a total of four registers to control GPIO.

6.2.2 PCA9554 Register 0

This register is read-only and reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writing to the register has no effect. The default “X” is determined by the externally applied logic level, which is normal “1” when no external signal is applied because of the internal pull-up resistors.

Table 6.4: Register 0 – Input Port Register Bit Description

Bit	Symbol	Access	Value	Description
7	I7	Read only	X	Determined by externally applied logic level
6	I6	Read only	X	
5	I5	Read only	X	
4	I4	Read only	X	
3	I3	Read only	X	
2	I2	Read only	X	
1	I1	Read only	X	
0	I0	Read only	X	

If one GPIO pin is set to input, the input value can be read from the bit that corresponds to Register 0.

6.2.3 PCA9554 Register 1 – Output Port Register

This register reflects the outgoing logic levels of the pins defined as outputs by Registers 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 6.5: Register 1 – Output Port Register Bit Description

Bit	Symbol	Access	Value	Description
7	O7	R	1*	Determined by externally applied logic level
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	
3	O3	R	1*	
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

If one GPIO pin is set to output, the input value can be read from the bit that corresponds to Register 1.

6.2.4 PCA9554 Register 2 – Polarity Inversion Register

This register allows users to invert the polarity of the input port register data. If a bit in this register is set (write with “1”), the corresponding input port data is inverted. If a bit in this register is cleared (write with “0”), the input port data polarity is retained.

Table 6.6: Register 2 – Polarity Inversion Register Bit Description

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	Invert polarity of the input port register data
6	N6	R/W	0*	
5	N5	R/W	0*	0= Input port register data retained (default)
4	N4	R/W	0*	
3	N3	R/W	0*	1= Input port register data inverted
2	N2	R/W	0*	
1	N1	R/W	0*	
0	N0	R/W	0*	

If one GPIO pin is set to input, you can control the polarity of input pin from the bit that corresponds to Register 2.

6.2.5 PCA9554 Register 3 – Configuration Register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. Upon reset, the I/Os are configured as inputs with a weak pull-up to VDD.

Table 6.7: Register 2 – Polarity Inversion Register Bit Description

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	Configures the directions of the I/O pins
6	C6	R/W	1*	
5	C5	R/W	1*	0= Corresponding port pin is enabled as an output
4	C4	R/W	1*	
3	C3	R/W	1*	1= Corresponding port pin is enabled as an input (default)
2	C2	R/W	1*	
1	C1	R/W	1*	
0	C0	R/W	1*	

Register 3 is used to set each GPIO as input or output:

If the bit is “0”, the corresponding GPIO pin is set as output;

If the bit is “1”, the corresponding GPIO pin is set as input.

6.3 Example

Below is an example based on ITA-5231. Assuming that GPIO 00 is set as output and GPIO 7 is set as input, with two pins interconnected, how is the corresponding register set?

GPIO 00 corresponds to PCA9554 0x40 IO0, while GPIO 07 corresponds to PCA9554 0x40 IO7.

Set GPIO 00 as Output

1. Read the SMBUS slave 0x40 Register 3 byte value.
2. Set bit 0 of the value read in Step 1 as 0 and write it to the SMBUS slave 0x40 Register 3.
3. Read the SMBUS slave 0x40 Register 1 byte value.
4. Set bit 0 of the value read in Step 3 as 0 or 1 according to how low or high the output value is. Then write it back to SMBUS slave 0x40 Register 1.

Set GPIO 07 as Input

1. Read the SMBUS slave 0x40 Register 3 byte value.
2. Set bit 7 of the value read in Step 1 as 1 and write it to the SMBUS slave 0x40 Register 3.
3. Read the SMBUS slave 0x40 Register 0 byte value.
4. Decide the low or high of the input value through the bit 7 value read in Step 3.

Function Call for Reference

```
ICH SMBUS Access Code
(The following code is realized by simulating the access of BIOS to SMBUS. It uses Borand C++.
3.1 for compiling and is successfully tested under DOS (But it is not tested under other OSs).

#define SMBUS_PORT 0xF040 //SMB_BASE is 0xF040
typedefunsigned char BYTE;

////////////////////////////////////////////////////////////////////

BYTE   smbus_read_byte(BYTE addr, BYTE offset)
//Read SMBUS Register byte value. Read one byte value each time. ddr is slave
address (such as 0x40), and offset is register offset.
{
       int  i;
       BYTE data;

       outportb(SMBUS_PORT + 4, (addr | 1)); //Write slave address to SMB_BASE + 4 (When reading, bit 0 of slave address should be set as 1, so here addr|1 is available)
       newiodelay();      //delay
       newiodelay();      //delay

       chk_smbus_ready(); //Whether SMBUS is ready

       outportb(SMBUS_PORT + 3, offset);//Write register offset to SMB_BASE  +3.
```

```
        newiodelay();       //delay
        newiodelay();       //delay

        outportb(SMBUS_PORT + 2, 0x48); //Write   SMBUS   command   to
SMB_BASE + 2. 0x48 means starting byte data transmission
        newiodelay();       //delay
        newiodelay();       //delay

        for (i = 0; i <= 0x100;  i++)
        {
             newiodelay();      //longerdelay
        }



        chk_smbus_ready(); //wheater SMBUS is ready return
(inportb(SMBUS_PORT + 5)); // Byte value read from SMB_BASE + 5
}

//////////////////////////////////////////////////////////////////

void smbus_write_byte(BYTE addr, BYTE offset, BYTE value)
// Write SMBUS Register byte value. Write one byte value each time.
addr is slave address (such as 0x40), and offset is register offset
{
        int  i;

        outportb(SMBUS_PORT + 4, addr); //  Write  slave  address  to
SMB_BASE + 4 (When writing, slave address bit 0 should be set as 0)
        moredelay();        //longerdelay
        moredelay();        //longerdelay

        chk_smbus_ready(); //wheater SMBUS is ready

        outportb(SMBUS_PORT + 3, offset);// write register offset to
SMB_BASE  +3.
        moredelay();        //longerdelay
        moredelay();        //longerdelay

        outportb(SMBUS_PORT + 5, value);//   Write   data   value   to
SMB_BASE + 5
        moredelay();        //longerdelay
        moredelay();        //longerdelay

        outportb(SMBUS_PORT + 2, 0x48); //  Write  SMBUS  command  to
SMB_BASE + 2.. 0x48 means starting byte data transmission.
        moredelay();        //longerdelay
```

```
        moredelay();        //longerdelay

        for (i = 0; i <= 0x100; i++)
        {
             newiodelay();//longerdelay
        }
        chk_smbus_ready(); //wheater SMBUS is ready
}
```

```
////////////////////////////////////////////////////////////////////////
```

```
int     chk_smbus_ready()
// To decide whether SMBUS is ready or has completed the action, you
should wait for a long time to check whether SMBUS has successfully
transmitted the command.
Since error may rarely occurs, BIOS code does not make judgement on
the return value of this function in read and write of SUMBUS byte.
{
        int  i, result = 1;
        BYTE data;

        for (i = 0; i <= 0x800; i++)
        {
             //SMB_BASE + 0 is the value of SMBUS status
             data = inportb(SMBUS_PORT);//Read SMBUS status value once
             data = check_data(SMBUS_PORT);//Read  SMBUS  status  value
several time
             outportb(SMBUS_PORT, data); //  Write  back  SMBUS  status
value which will clear status value (Write 1 to the corresponding bit
means clearing status
             if (data & 0x02)
             {    // If bit 1 is set (which means the command is
completed), SMBUS is ready
                  result = 0;//SMBUS ready
                  break;
             }

             if (!(data & 0xBF))
             {    // If all bits are 0 except bit 2 (which means error
occurs on SMBUS), SMBUS is ready
             result = 0;         //SMBUS ready
             break;
```

```
            }

            if (data & 0x04)
            {    // If bit 2 is set (which means error occurs on
SMBUS), error occurs on SMBUS which is rarely the case
            result = 1;        //SMBUS error
            break;
            }
       }

       return result;
}


//////////////////////////////////////////////////////////////////////

BYTE   check_data (W ORD addr)
{
       int  i;
       BYTE data;

       for(i = 0; i <= 6; i++)
       {
            data = inportb(addr);
            if (data!= 0)
                 break;
       }
       return data;
}

//////////////////////////////////////////////////////////////////////

void newiodelay()
//Shorter delay
{
       outportb(0xeb, 0); // IO port 0xeb No real device occupies.
Write a value to this port can realize delay function. You can also
choose other method according to the real situation.
}

//////////////////////////////////////////////////////////////////////

void  moredelay()
//longerdelay
{
       int  i;
```

```
        for (i = 0; i < 20; i++)
        {
             outportb(0xeb, 0); // IO port 0xeb No real device occupies. Write a value to this port can realize delay function. You can also choose other method according to the real situation.
        }
}
```

```
**********************************************************************
GPIO Simcodes
(take GPIO 00 and GPIO 07 as an example)

Output High to GPIO 00:
        data = smbus_read_byte(0x40, 0x03); //Read slave 0x40 register 3 byte
        data &= 0xfe;//Set bit 0 as 0
        smbus_write_byte(0x40, 0x03, data)//write, set GPIO 00 as Output
        data = smbus_read_byte(0x40, 0x01) //Read slave 0x40 register 1
        data |= 0x01; //Set bit 0 as 1, High
        smbus_write_byte(0x40, 0x01, data) //Write, Output High value


Read Input Value from GPIO 07:
        data = smbus_read_byte(0x40, 0x03); //Read slave 0x40 register 3 byte
        data |= 0x80; //Set bit 7 as 1
        smbus_write_byte(0x40, 0x03,data) //Write, set GPIO 07 as Input
        data = smbus_read_byte(0x40, 0x00) //Read slave 0x40 register 0. Then, the response value of bit 7 should know whether the input is low or high.
```

Appendix A

Programming the Watchdog Timer

A.1 Introduction

The ITA-5231's watchdog timer can be used to monitor the software operations and take corrective action if the software fails to function within the programmed period. This section describes the operation of the watchdog timer and procedures for programming it.

A.1.1 Watchdog Timer Overview

The watchdog timer is built into the embedded controller and provides the following user-programmable functions:

- Can be enabled/disabled via software
- Timebase is 100 ms
- Each time limit is a word long
- The event time can be set from 0 to 0xFFFE
- Writing 0xFFFF to time limit ram will disable events
- The timer can be set from 100 ms to 109.22 minutes
- Generates and resets signal if the software fails to reset the timer before timeout

A.1.2 Programming the Watchdog Timer

The watchdog timer logic can be accessed through the EC PM2 (power management channel 2). PM2 is a LPC I/O port channel. The PM2 channel includes one command/status port and one data port. The system can use the command port to send a command to the EC or obtain the current port status. The system can send command parameters or obtain the EC return data through the data port. Typically, 0x29A is the command/status port and 0x299 is the data port.

Command/Status port: Port 0x29A

Action	Description
Write	Send command to EC
Read	Get EC 299/29A port status

The status that was read from 0x29A is described below.

Status from the command/status port

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	IBF (input buffer full)	OBF (output buffer full)

Note!

1. *BIT 0 (OBF) - When the EC returns data to the 0x299 port, the OBF is set as "1". The OBF is cleared to zero after the system reads data from the 0x299 port.*
2. *BIT 1 (IBF) - When the system writes data or commands to 0x299 or 0x29A, the IBF is set as "1". The IBF is cleared to zero after the EC obtains data/command from the 299/29A port.*

Data Port: Port 0x299

Action	Description Send
Write	data to EC Get
Read	data from EC

Note!

1. *After writing data/commands to the 299/29A port, the IBF will be set as "1". Users must wait for the IBF to clear to zero, before writing the next data/commands to the 299/29A port.*
2. *If the EC command returns data, users can read the data from the 68 port when the OBF is set as "1".*

Watchdog Command

0x28	Start watchdog
0x29	Stop watchdog
0x2A	Reset watchdog
0x88	Read EC HW RAM
0x89	Write EC HW RAM

Watchdog HW RAM Address

Watchdog HW RAM is used to set the time limit and retain the event status.

Address	**Function**	**Description**							
0x57	Watchdog event flag	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		X	X	X	Pwr Btn	WD Pin	Reset	SCI	NMI
0x5E-0x5F	Watchdog reset delay time	0 ~ 0xFFFE, setup reset time							

Note!

NMI – 1: NMI event sent; 0: NMI event not sent.
SCI – 1: SCI event sent; 0: SCI event not sent.
RESET – 1: Reset event sent; 0: Reset event not sent.
WDPin – 1: WDPin event sent; 0: WDPin event not sent.
PwrBtn – 1: PwrBtn event sent; 0: PwrBtn event not sent.

Example Program

```
//Wait IBF Empty
unsigned char ECWaitIBFEmpty()
{
	unsigned char Status;

	do{
	     Status = inportb(0x29A);    //Read back Status
	} while (Status & 0x02); //If IBF Set?

	return Status;
}

//Write non-data command (no data) to EC
void EcWriteCmd (unsigned char cmd)
{
	ECWaitIBFEmpty();//Wait IBF Empty outpor tb(0x29A, (unsigned
char)cmd);   //Write command
}

//Write standard command (include data) to EC
void IT8528ECSetData (
	unsigned char	Cmd, //command
	unsigned char	Addr,//write address
	unsigned char	Value,//data
)
{
	ECWaitIBFEmpty();                          //Wait IBF Empty
	outportb (IT8528E_HWM_CMD_PORT, Cmd);      //Write command
	ECWaitIBFEmpty();                          //Wait IBF Empty
	outportb (IT8528E_HWM_DATA_PORT, Addr); //Write address
	ECWaitIBFEmpty();                          //Wait IBF Empty
	outportb (IT8528E_HWM_DATA_PORT, Value);   //Write data
}

//Stop watchdog
void disable_wdt()
{
	EcWriteCmd(0x29);       //Write command 0x29 to stop watch dog
}
```

```
//Start watchdog
void enable_wdt( i
       nt time,       //Time
       int timebase   //Time base: 0: second 1: minute
)
{
       unsigned int time_word;

       EcWriteCmd(0x29);  //Write command 0x29 to stop watch dog

       if (timebase == 0) //Second base = 100ms * 10
            time_word = time * 10;
       else               //Minute base = 100ms * 600
            time_word = time * 600;

       IT8528ECSetData (0x89,0x5E, (unsigned char)(time_word>>8));//Use
command 0x89 to write time data hibyte to hw ram address 0x5E
       IT8528ECSetData (0x89, 0x5F,(unsigned char)(time_word&0x00ff)); //Use
command 0x89 to write time data lowbyte to hw ram address 0x5f
       IT8528ECSetData (0x89, 0x57, 0x04);                    //Use
command 0x89 to write watchdog time event to hw ram address
0x57
                                                              //0x04:
Bit2 =1 , watchdog output as RESET

       EcWriteCmd(0x28);///Write command 0x28 to stop watch dog
}
```

Appendix B

Declaration of the Presence Condition of the Restricted Substances Marking

BSMI RoHS 限用物質含有情況標示確認表

Declaration of the Presence Condition of the Restricted Substances Marking

設備名稱：電腦 Equipment name	型號 （型式）：ITA-5231 Type designation (Type)					
單元 Unit	限用物質及其化學符號 Restricted substances and its chemical symbols					
	鉛 Lead (Pb)	汞 Mercury (Hg)	鎘 Cadmium (Cd)	六價鉻 Hexavalent chromium (Cr^{+6})	多溴聯苯 Polybrominated biphenyls (PBB)	多溴二苯醚 Polybrominated diphenyl ethers (PBDE)
電路板	－	○	○	○	○	○
固定组件 （螺絲、螺柱）	－	○	○	○	○	○
內外殼	－	○	○	○	○	○
散熱模組	－	○	○	○	○	○
線材	－	○	○	○	○	○

備考 1.“ 超出 0.1 wt %” 及 “ 超出 0.01 wt %” 係指限用物質之百分比含量超出百分比含量基準值。

Note 1: “Exceeding 0.1 wt %” and “exceeding 0.01 wt %” indicate that the percentage content of the restricted substance exceeds the reference percentage value of presence condition.

備考 2.“ ○ ” 係指該項限用物質之百分比含量未超出百分比含量基準值。

Note 2: “○” indicates that the percentage content of the restricted substance does not exceed the percentage of reference value of presence.

備考 3.“ － ” 係指該項限用物質為排除項目。

Note 3” The “-” indicates that the restricted substance corresponds to the exemption.

Appendix C

Chinese Language Safety Instructions and Battery Information

C.1 安全指示

1. 請仔細閱讀此安全操作說明。
2. 請妥善保存此用戶手冊供日後參考。
3. 用濕抹布清洗設備前，請從插座拔下電源線。請不要使用液體或去汙噴霧劑清洗設備。
4. 對於使用電源線的設備，設備周圍必須有容易接觸到的電源插座。
5. 請不要在潮濕環境中使用設備。
6. 請在安裝前確保設備放置在可靠的平面上，意外跌落可能會導致設備損壞。
7. 設備外殼的開口是用於空氣對流，從而防止設備過熱。**請不要覆蓋這些開口。**
8. 當您連接設備到電源插座上前，請確認電源插座的電壓是否符合要求。
9. 請將電源線佈置在人們不易絆到的位置，並不要在電源線上覆蓋任何雜物。
10. 請注意設備上的所有警告標識。
11. 如果長時間不使用設備，請將其同電源插座斷開，避免設備被超標的電壓波動損壞。
12. 請不要讓任何液體流入通風口，以免引起火災或者短路。
13. 請不要自行打開設備。為了確保您的安全，請由經過認證的工程師來打開設備。如遇下列情況，請由專業人員來維修：
    - 電源線或者插頭損壞；
    - 設備內部有液體流入；
    - 設備曾暴露在過於潮濕的環境中使用；
    - 設備無法正常工作，或您無法通過用戶手冊來使其正常工作；
    - 設備跌落或者損壞；
    - 設備有明顯的外觀破損。
14. 請不要把設備放置在超出我們建議的溫度範圍的環境，即不要低於 -25° C（-13 ° F）或高於 60° C （140° F），否則可能會損壞設備。
15. 此為 A 級產品，在生活環境中，該產品可能會造成無線電干擾。在這種情況下，可能需要使用者對干擾採取切實可行的措施。
16. 本產品不帶電線元件銷售，應購買已通過 CCC 認證的電線元件。

注意：電腦配置了由電池供電的即時時鐘電路，如果電池放置不正確，將有爆炸的危險。因此，只可以使用製造商推薦的同一種或者同等型號的電池進行替換。請按照製造商的指示處理舊電池。

根據 IEC 704-1:1982 的規定，操作員所在位置的聲壓級不可高於 70dB(A)。

免責聲明：該安全指示符合 IEC 704-1 的要求。研華公司對其內容的準確性不承擔任何法律責任。

C.2 電池信息

電池、電池組和蓄電池不應作為未分類的生活垃圾處理，請使用公共收集系統返回和回收，或哪找當地法規要求進行處理。

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Please verify specifications before quoting. This guide is intended for reference purposes only.

All product specifications are subject to change without notice.