

User Manual

AFE-R360

Intel® Core™ Ultra U/H-series 3.5" SBC



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This manual is for the AFE-R360.

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Product Warranty (2 years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

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- 1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
- 2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
- If your product is diagnosed as defective, obtain a return merchandize authorization (RMA) number from your dealer. This allows us to process your return more quickly.
- 4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
- 5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

Declaration of Conformity

CE

This product has passed the CE test for environmental specifications. Test conditions for passing include the equipment being operated within an industrial enclosure. In order to protect the product from damage caused by electrostatic discharge (ESD) or EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

Technical Support and Assistance

- 1. Visit the Advantech website at www.advantech.com/support to obtain the latest product information.
- 2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
 - Product name and serial number
 - Description of your peripheral attachments
 - Description of your software (operating system, version, application software, etc.)
 - A complete description of the problem
 - The exact wording of any error messages

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- 1 x AFE-R360 SBC
- 1 x USB 2.0 Cable 20cm (p/n: 1700030406-01)
- 1 x Audio Cable 20cm (p/n: 1700019584-01)
- 4 x COM RS-232 Cable 20cm (p/n: 1700031582-01)
- 1x Cooler 1970005512T001 or Heatsink (1970005973T001)
- 1 x Screw Kit (4sets screws for M.2 device)
- 1 x DeviceOn Package

Optional Accessories

- 1x Heat spreader of AFE-R360 (p/n: 1970005998T001)
- MIOe-MIPI
- MIOe-GMSL
- 2P Phoenix to DC jack power cable (p/n: 1700009001)
- 4 wires COM RS-422/485 cables (p/n: 1700035016-01)

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General Information

1.1 Introduction

AFER-R360 is powered by Intel® Core[™] Ultra H/ U series processors. AFER-R360 offers embedded iManager 3.0, SUSI 4.0 and WISE-PaaS/DeviceOn created by Advantech to monitor and control system operation effectively and remotely.

AFE-R360 adopts the latest hybrid core design processor, for improvements in CPU processing, graphics, security and I/O flexibility

1.2 Specifications

Table 1.1:	Specificati	ons					
	Processor	Core Ultra 7, 155H	Core Ultra 5, 125H	Core Ultra 7, 155U	Core Ultra 5, 125U		
	Max. Frequency	4.8GHz	4.5GHz	4.8GHz	4.3GHz		
	Base Frequency (P-Core)	1.4GHz	1.2GHz	1.7GHz	1.3GHz		
Platform	Core/Thread	16, 6P+8E+2LE/ 22	14, 4P+8E+2LPE/ 18	12, 2P+8E+2LE / 14	12, 2P+8E+2LE / 14		
	LLC	24MB	18MB	12MB	12MB		
	CPU TDP	28W	28W	15W	15W		
	Chipset	On-package Intel 600) Series Chipset				
	BIOS	AMI EFI 256Mbit					
	Technology	DDR5 5600					
Memory	Max. Capacity	Up to 96GB					
,	Channel/ Socket	Dual Channels/ 2 Sockets					
	Controller	Intel® ARC® Graph- ics	Intel® Arc™ graph- ics	Intel® Graphics	Intel® Graphics		
Graphics	Max. Frequency	2.25GHz	2.2GHz	1.95GHz	1.85GHz		
•	Execution Unit	128	112	128	112		
	3D/ HW Acceleration	DX12.1, OGL4.6, OCL3.0, HW Encode/ Decode: H.265 (HEVC), H.264, AV1					
Display I/F	DisplayPort	1 x DP1.4a, up to 409	96 x 2160x 36bpp @60)Hz			
Ethornot	Controller	LAN1~3: Intel i226LM					
Ethemet	Speed	LAN1~3: 2.5GbE					
	M.2 E-Key	1 x E-Key 2230 (PClex2, USB2.0)					
Expansion	M.2 B-Key	1 x B-Key 3042/ 3052	2* (PCIe x2/ SATA, US	B2.0) w' Nano SIM			
Expansion	M.2 M-Key	2 x M-Key 2280 (PCI	ex4 Gen.4 NVMe)				
	120Pin B2B	8 lanes MIPI-CSI, I20	C, 3.3V, 1.8V				

Table 1.1: Specifications								
	Ethernet	3 x RJ-45						
	DP	1						
External I/O	USB Type-C	2 x USB3.2 Gen2x1 10Gbps, support DisplayPort1.4 Alt. Mode						
	USB Type-A	2 x USB3.2 Gen2x	1 10Gbps					
	Power Connector	2-pin phoenix conr	pin phoenix connector, optional 4-pin ATX connector					
	USB4	1 USB4 with USB ⁻ PCle	Type-C, Bandwidth mir	ו. 20Gbps, max. 40G	bps, with USB4/ Display/			
	USB2.0	2						
	COM Port	4 x RS-232/422/48	5, max. 1Mbps					
	CANBus	2 x CAN-FD						
	Serial Bus	1x I2C/ SMBUS						
Internal I/O	Audio	Realtek ALC888s,	Line-in/Line-out/MIC					
	GPIO	8-bit general purpo	ose input output I/O					
	Fan	12V, 1A (4-wire)						
	Front Panel Control	Power-on, Reset, I	Power-on, Reset, Buzzer, CaseOpen					
	MIPI-CSI	Jp to 4x 22pin FPC, or option to 2x 30pin I-PEX MIPI-CSI ports, expanded through /IPI-CSI interfaced card, MIOe-MIPI						
	GMSL	Up to 4x FAKRA, expanded through GMSL interfaced card, MIOe-GMSL.						
Board	Watchdog Timer	65536 level, 0~655	535 sec					
Feature	ТРМ	Discrete TPM2.0, fTPM* support by request						
	SUSI	SW API for Hardwa	are Monitor, Smart Far	Control, I2C, GPIO,	WDT			
	Supply Voltage	Vin: DC 12V~24V	+/- 10%; RTC Battery:	Lithium 3V/210mAH				
	Connector	2P Phoenix, option	al to ATX 2x2 pin 90D					
Power	Power Management	AT, ATX						
	Max. Consumption	116.04 (12V)/ 128.4 (24V)	129.96W (12V)/ 134.4W (24V)	81.10 (12V)/ 74.3W (24V)	115.26W (12V)/ 123.40W (24V)			
	Idle Consumption	13.06 (12V)/ 15.19 (24V)	15.36W (12V)/ 17.69W (24V)	14.6W (12V)/ 15.84W (24V)	12.74W (12V)/ 15.12W (24V)			
	Temperature	Operating: 0 ~ 60 ° Storage: -40 ~ 85 °	°C (32 ~ 140 °F) °C (-40 ~ 185 °F)					
Environment	Humidity	Operating: 40 °C @ Storage: 60 °C @	95% relative humidit 95%relative humidity, r	y, non-condensing non-condensing				
	Vibration Resistance	3.5 Grms						
Certification	EMC	CE, FCC Class B						
Machanical	Dimensions	146 x 102 mm (5.7	" x 4")					
mechanica	Net Weight	170g						
*NIa	to: Support by ro	au oct						

*Note: Support by request.

1.3 Block Diagram





Mechanical Specifications

2.1 Introduction

The compact form factor SBC is a new-generation SBC designed with a variety of mechanical improvements. This chapter includes board dimension and assembly instructions for the standard thermal solution.

2.2 Board Layout: Dimensions



Figure 2.1 AFE-R360 Mechanical Diagram (Top Side)



Figure 2.2 AFE-R360 Mechanical Diagram (Bottom Side)



Figure 2.3 AFE-R360 Mechanical Diagram (with Cooler)



Figure 2.4 AFE-R360 Mechanical Diagram (with Cooler)



Figure 2.5 AFE-R360 Mechanical Diagram (with Heatsink)

2.3 Quick Installation Guide

This section introduces installation of the MIOe-MIPI, which is the camera IO extension card designed for AFE-R360. Please assemble it by following diagram.



Figure 2.6 AFE-R360 & MIOe-MIPI Installation



Figure 2.7 AFE-R360 & MIOe-MIPI Complete Installation



Jumpers and Connectors

3.1 Jumper & Switches

The AFE-R360 has a number of jumpers that allow you to configure your system to suit your application. The table below lists the functions of the various jumpers.

3.1.1 Miscellaneous Selection Jumper: SW1

Table 3.1: Miscellaneous Selection Jumper: SW1			
Jumper Short	Panel Functional		
1	ATX_DET (Default)		
2	LOAD_BIOS_DEFAULT (Default_off)		
3	GPI (no function)		
4	Topswap (no function, default on)		
5	Topswap (no function, default on)		
6	GPI (no function)		
7	LOAD_BIOS_DEFAULT (On)		
8	AT_DET#		



3.2 Connectors

Table 3.2	: Connectors	
1	AUDIO1	Audio Internal Connector
2	BAT1	RTC battery Connector
3	CANBUS1	CAN Bus Port 0
4	CANBUS2	CAN Bus Port 1
5	CN1	Front Panel Internal Connector
6	COM1	COM Port Internal Connector 1
7	COM2	COM Port Internal Connector 2
8	COM3	COM Port Internal Connector 3
9	COM4	COM Port Internal Connector 4
10	DCIN1	DC Power Input Connector
11	DP1	Display Port Connector
12	FAN1	Smart FAN
13	GPIO1	GPIO Internal Connector
14	I2C_1	I2C/ SMBus Internal Connector
15	LAN1	I226 RJ45 LAN Ports
16	LAN2	I226 RJ45 LAN Ports
17	LAN3	I226 RJ45 LAN Ports
19	MIPI1	MIPI Internal Connector
20	M2_B1	M.2 Key-B Connector
21	M2_1	M.2 Key-E Connector
22	M2_2	M.2 Key-M Connector
23	M2_3	M.2 Key-M Connector
24	SW1	Miscellaneous Selection Jumper
25	TYPEC1	TypeC Port (USB3.2/DP)
26	TYPEC2	TypeC Port (USB3.2/DP)
27	TYPEC3	TypeC Port (TBT4)
28	USB1	USB3.2 Connector
29	USB2	USB2.0 Internal Connector
30	U4	DDR5 SO-DIMM 5.2mm
31	U5	DDR5 SO-DIMM 9.2mm

3.3 Locating Connectors





(for MIOe-MIPI or MIOe-GMSL connection)

Chapter 3 Jumpers and Connectors

3.4 Connector Pin Define

Table 3.3: CANBus Internal Connector: CANBUS1			
Pin	Signal Pin Definition		
PN	1654903500		
Vendor MPN	ACES/ 85205-03001		
Pin	Signal Definition		
1	CAN0_D+		
2	CAN0_D-		
3	GND		



Table 3.4: CANBus Internal Connector: CANBUS2			
Pin	Signal Pin Definition		
PN	1654903500		
Vendor MPN	ACES/ 85205-03001		
Pin	Signal Definition		
1	CAN2_D+		
2	CAN2_D-		
3	GND		



Table 3.5: I2C Internal Connector: I2C_1			
Pin	Signal Pin Definition		
PN	1655904020		
Vendor MPN	ACES/ 85205-04001		
Pin	Signal Definition		
1	GND		
2	EC_I2C0_z_DAT		
3	EC 12C0 z CLK		



Table 3.6: Smart FAN Internal Connector: FAN1			
Pin	Signal Pin Definition		
PN	1653008788-01		
Vendor MPN	ACES/ 50273-00401-001		
Pin	Signal Definition		
1	GND		
2	+V12		
3	FAN_SPEED		
4	FAN_V5_PWM		



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Table 3.7: USB2.0 Dual-Ports Internal Connector: USB2

Pin	Signal Pin Definition
PN	1653008214-01
Vendor MPN	Pinrex/ 52C-90-10GBE0
Pin	Signal Definition
1	+V5SB_USB2
2	+V5SB_USB2
3	USB9_z_P-
4	USB10_z_P-
5	USB9_z_P+
6	USB10_z_P+
7	GND
8	GND
9	GND
10	NC



Table 3.8: Audio Internal Connector: AUDIO1		
Pin	Signal Pin Definition	
PN	1653008214-01	
Vendor MPN	Pinrex/ 52C-90-10GBE0	
Pin	Signal Definition	
1	LOUTR	
2	LINR	
3	GND_AUD	
4	GND_AUD	
5	LOUTL	
6	LINL	
7	GND_AUD	
8	FRONT_JD	
9	MIC1R	
10	MIC1L	



Table 3.9: MIPI Power Connector: MIPI_P1		
Pin	Signal Pin Definition	
PN	1653007538-01	
Vendor MPN	Pinrex/ 721-81-02TW00	
Pin	Signal Definition	
1	+VDCIN	
2	GND	



Table 3.10: COM-Port Internal Connector 1: COM1		
Pin	Signal Pin Definition	
PN	1655004032	
Vendor MPN	ACES/ 85205-05701	
Pin	Signal Definition	
1	COM1_TXD	
2	COM1_RTS#	
3	COM1_RXD	
4	COM1_CTS#	
5	GND	



Table 3.11: COM-Port Internal Connector 2: COM2	
Pin	Signal Pin Definition
PN	1655004032
Vendor MPN	ACES/ 85205-05701
Pin	Signal Definition
1	COM2_TXD
2	COM2_RTS#
3	COM2_RXD
9	COM2_CTS#
10	GND



Table 3.12: COM-Port Internal Connector 3: COM3	
Pin	Signal Pin Definition
PN	1655004032
Vendor MPN	ACES/ 85205-05701
Pin	Signal Definition
1	COM3_TXD
2	COM3_RTS#
3	COM3_RXD
4	COM3_CTS#
5	GND



Table 3.13: COM-Port Internal Connector 4: COM4		
Pin	Signal Pin Definition	
PN	1655004032	
Vendor MPN	ACES/ 85205-05701	
Pin	Signal Definition	
1	COM4_TXD	
2	COM4_RTS#	
3	COM4_RXD	
4	COM4_CTS#	
5	GND	



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Table 3.14: Front Panel Internal Connector: CN1		
Pin	Signal Pin Definition	
PN	1653007728-02	
Vendor MPN	ACES/ 50273-0107N-002	
Pin	Signal Definition	
1	GND	
2	BUZZER-	
3	BUZZER+	
4	CASEOPEN#	
5	NC	
6	FP_a_PSIN#	
7	FP_a_RST#	
8	+V3.3	
9	NC	
10	+V5	



Table 3.15: GPIO Internal Connector: GPIO1		
Pin	Signal Pin Definition	
PN	1653007728-02	
Vendor MPN	ACES/ 50273-0107N-002	
Pin	Signal Definition	
1	GND	
2	EC_P1_GPIO7	
3	EC_P1_GPIO2	
4	EC_P1_GPIO6	
5	EC_P1_GPIO1	
6	EC_P1_GPIO5	
7	EC_P1_GPIO0	
8	EC_P1_GPIO4	
9	+V5_P1_GPIO	
10	EC P1 GPIO3	



Table 3.16: RTC battery Connector: BAT1		
Pin	Signal Pin Definition	
1	+VBAT	
2	GND	



Table 3.17: M.2 Key-E Connector: M2_1		
Pin	Signal Pin Definition	
1	GND	
2	+V3.3SB_M.2_E	
3	USB6_z_P+	
4	+V3.3SB_M.2_E	
5	USB6_z_P-	
6	NC	
7	GND	
8	NC	
9	NC	
10	NC	
11	NC	
12	NC	
13	NC	
14	NC	
15	NC	
16	NC	
17	NC	
18	GND	
19	NC	
20	NC	
21	NC	
22	UART2_RXD	
23	NC	
32	UART2_TXD	
33	GND	
34	NC	
35	PCIE_M2_z_TX3+	
36	NC	
37	PCIE_M2_z_TX3-	

Table 3.17: M.2 Key	r-E Connector: M2_1
38	CLINK_RST#
39	GND
40	CLINK_DATA
41	PCIE_M2_RX3+
42	CLINK_CLK
43	PCIE_M2_RX3-
44	CNV_PA_BLANKING
45	GND
46	NC
47	CLK0_M2E_z_PCIE+
48	NC
49	CLK0_M2E_z_PCIE-
50	SUSCLK_z_EKEY
51	GND
52	PLTRST_BUFFER#
53	PCIE_a_CLKREQ0#
54	BT_DISABLE#
55	PCIE_WAKE#_3.3
56	WIFI_DISABLE#
57	GND
58	NC
59	PCIE_M2_z_TX4+
60	NC
61	PCIE_M2_z_TX4-
62	NC
63	GND
64	NC
65	PCIE_M2_RX4+
66	NC
67	PCIE_M2_RX4-
68	PCIE_a_CLKREQ1#
69	GND
70	NC
71	CLK1_M2E_z_PCIE+
72	+V3.3SB_M.2_E
73	CLK1_M2E_z_PCIE-
74	+V3.3SB_M.2_E
75	GND
H1	NC
H2	NC
H3	GND
H4	GND

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Table 3.18: M.2 Key-M Connector: M2_2

Pin	Signal Pin Definition	
1	GND	
2	+V3.3_M.2_1	
3	GND	
4	+V3.3_M.2_1	
5	PCIE3_KEY-M_RX3-	
6	NC	
7	PCIE3_KEY-M_RX3+	
8	M.2_PLN#	
9	GND	
10	NC	
11	PCIE3_KEY-M_a_TX3-	
12	+V3.3_M.2_1	
13	PCIE3_KEY-M_a_TX3+	
14	+V3.3_M.2_1	

Table 3.18: M.2 Key	r-M Connector: M2_2
15	GND
16	+V3.3_M.2_1
17	PCIE3_KEY-M_RX2-
18	+V3.3_M.2_1
19	PCIE3_KEY-M_RX2+
20	NC
21	GND
22	NC
23	PCIE3_KEY-M_a_TX2-
24	NC
25	PCIE3_KEY-M_a_TX2+
26	NC
27	GND
28	NC
29	PCIE3_KEY-M_RX1-
30	NC
31	PCIE3_KEY-M_RX1+
32	GND
33	GND
34	USB8_z_P+
35	PCIE3_KEY-M_a_TX1-
36	USB8_z_P-
37	PCIE3_KEY-M_a_TX1+
38	GND
39	GND
40	NC
41	PCIE3_KEY-M_RX0-
42	NC
43	PCIE3_KEY-M_RX0+
44	NC
45	GND
46	NC
47	PCIE3_KEY-M_a_TX0-
48	NC
49	PCIE3_KEY-M_a_TX0+
50	PLTRST_M2M1_BUFFER#
51	GND
52	CLK0_M2MB_a_PCIE_REQ#
53	CK0_100M_a_MKEY_N
54	M2M1_PCIE_WAKE#
55	CK0_100M_a_MKEY_P
56	NC
57	GND
58	NC
67	NC
68	PCH_SUSCLK_R_M2M1
69	NC

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Table 3.18: M.2 Ke	y-M Connector: M2_2
70	+V3.3_M.2_1
71	GND
72	+V3.3_M.2_1
73	GND
74	+V3.3_M.2_1
75	GND
H1	NC
H2	NC
H3	NC
H4	NC



Table 3.19: M.2 Key	r-M Connector: M2_3
Pin	Signal Pin Definition
1	GND
2	+V3.3_M.2_2
3	GND
4	+V3.3_M.2_2
5	PCIE4_KEY-M_RX3-
6	NC
7	PCIE4_KEY-M_RX3+
8	M2M1_PLN#
9	GND
10	NC
11	PCIE4_KEY-M_a_TX3-
12	+V3.3_M.2_2
13	PCIE4_KEY-M_a_TX3+
14	+V3.3_M.2_2
15	GND
16	+V3.3_M.2_2
17	PCIE4_KEY-M_RX2-
18	+V3.3_M.2_2
19	PCIE4_KEY-M_RX2+
20	NC
21	GND
22	NC
23	PCIE4_KEY-M_a_TX2-
24	NC
25	PCIE4_KEY-M_a_TX2+
26	NC
27	GND
28	NC
29	PCIE4_KEY-M_RX1-
30	NC
31	PCIE4_KEY-M_RX1+
32	NC
33	GND
34	NC
35	PCIE4_KEY-M_a_TX1-
36	NC
37	PCIE4_KEY-M_a_TX1+
38	NC
39	GND
40	NC
41	PCIE4_KEY-M_RX0-
42	NC
43	PCIE4_KEY-M_RX0+
44	NC
45	GND

Table 3.19: M.2 Key	r-M Connector: M2_3
46	NC
47	PCIE4_KEY-M_a_TX0-
48	NC
49	PCIE4_KEY-M_a_TX0+
50	PLTRST_M2M2_BUFFER#
51	GND
52	CLK1_M2MB_a_PCIE_REQ#
53	CK1_100M_a_MKEY_N
54	M2M2_PCIE_WAKE#
55	CK1_100M_a_MKEY_P
56	NC
57	GND
58	NC
67	NC
68	PCH_SUSCLK_R_M2M2
69	NC
70	+V3.3_M.2_2
71	GND
72	+V3.3_M.2_2
73	GND
74	+V3.3_M.2_2
75	GND
H1	NC
H2	NC
H3	NC
H4	NC

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34		- 33
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4 6		45
48		4/
50		49
52		51
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70		- %
72		- 73
74		75
		UH2
		<u>~</u> H4
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Table 3.20: M.2 Key-B Connector: M2_B1	
Pin	Signal Pin Definition
1	M2B1_CFG3
2	+V3.3A_M.2_B
3	GND
4	+V3.3A_M.2_B
5	GND
6	M2B1_FULL_CARD_OFF#
7	USB_M2B1_P
8	M2B1_W_DISABLE1#
9	USB_M2B1_N
10	CAM1_SYNCOUT
11	GND
20	M2B1_PCIE_DIS
21	M2B1_CFG0
22	M2B1_ANT_CFG
Table 3.20: M.2 Key-	B Connector: M2_B1
----------------------	--------------------
23 M	M2B1_WAKE_ON_WWAN#
24 M	M2B1_ANT_TUNER
25 N	M2B1_DPR
26 M	M2B1_W_DISABLE2#
27 (GND
28 N	NC
29 M	M2B1_PCIE_RX1-
<u>30</u>	M2B1_UIM_RESET
<u>31</u>	M2B1_PCIE_RX1+
<u>32</u>	M2B1_UIM_CLK
33 (GND
<u>34</u>	M2B1_UIM_DATA
35 N	M2B1_PCIE_TX1-
<u>36</u>	M2B1_UIM_PWR
37 N	M2B1_PCIE_TX1+
<u>38</u>	NC
39 (GND
40 N	NC
41 M	M2B1_PCIE_RX-
42 N	NC
43 M	M2B1_PCIE_RX+
44 N	NC
45 0	GND
46 N	NC
47 N	M2B1_PCIE_TX-
48 N	NC
49 M	M2B1_PCIE_TX+
<u>50</u>	M2B1_a_PERST#
51 (GND
52 N	M2B1_a_CLKREQ#
53 (CLK100M_a_M2B1-
54 N	M2B1_PCIEWAKE#
55 0	CLK100M_a_M2B1+
56 N	NC
57 (GND
<u>58</u>	NC
59 N	NC
<u>60</u>	NC
<u>61</u>	NC
<u>62</u>	NC
<u>63</u>	NC
<u>64</u>	NC
65 N	NC
<u>66</u>	NC
67 N	M2B1_a_RESET#
68 N	M2B1_SUSCLK
69 N	M2_DET

Table 3.20: M.2 Key	r-B Connector: M2_B1
70	+V3.3A_M.2_B
71	GND
72	+V3.3A_M.2_B
73	GND
74	+V3.3A_M.2_B
75	M2B1_CFG2
H1	NC
H2	NC
H3	GND
H4	GND



Table 3.21: MIPI Co	onnector: MIPI1
Pin	Signal Pin Definition
1	CSI_A_D0+
2	CSI_B_D0+
3	CSI_A_D0-
4	CSI_B_D0-
5	GND
6	GND
7	CSI_A_CLK+
8	CSI_B_CLK+
9	CSI_A_CLK-
10	CSI_B_CLK-
11	GND
12	GND
13	CSI_A_D1+
14	CSI_B_D1+
15	CSI_A_D1-
16	CSI_B_D1-
17	GND
18	GND
19	CSI_E_D0+
20	CSI_F_D0+
21	CSI_E_D0-
22	CSI_F_D0-
23	GND
24	GND
25	CSI_E_CLK+
26	CSI_F_CLK+
27	CSI_E_CLK-
28	CSI_F_CLK-
29	GND
30	GND
31	CSI_E_D1+
32	CSI_F_D1+
33	CSI_E_D1-
34	CSI_F_D1-
35	GND
36	GND
37	NC
38	NC
39	NC
40	NC
41	GND
42	GND
43	NC
44	NC
45	NC

Table 3.21: MIPI Co	nnector: MIPI1
46	NC
47	GND
48	GND
49	NC
50	NC
51	NC
52	NC
53	GND
54	GND
55	NC
56	NC
57	NC
58	NC
59	NC
60	NC
61	NC
62	NC
63	GND
64	GND
65	NC
66	NC
67	NC
68	NC
69	GND
70	GND
71	NC
72	NC
73	NC
74	NC
75	CAM2_SCL
76	CAM3_SCL
77	CAM2_SDA
78	CAM3_SDA
79	GND
80	GND
81	NC
82	NC
83	NC
84	Camera Error#1
85	CAM1_SYNCIN_R
86	IMGCLKOUT3
87	CAM1_SCL
88	IMGCLKOUT1
89	CAM1_SDA
90	PWDN2
91	IMGCLKOUT0
92	CAM2_RST_R_N

Table 3.21: MIPI Co	nnector: MIPI1
93	PWDN1
94	IMGCLKOUT2
95	CAM1_RST_R_N
96	SCL1B
97	CAM2_SYNCIN_R
98	SDA1B
99	GND
100	GND
101	STROBE_CAM1
102	1.8V
103	EE_+V3.3_A_PG
104	CRD2_A1
105	CAM4_SCL
106	CRD2_A0
107	CAM4_SDA
108	3.3V
109	CAM1_CLK_EN
110	3.3V
111	PRIVACY_CAM1
112	CAM2_CLK_EN
113	STROBE_CAM2
114	XMASTER_CAM1_R
115	GND
116	GND
117	XMASTER_CAM2_R
118	3.3V
119	CRD1_PWREN
120	3.3V





AMI BIOS Setup

AMIBIOS has been integrated into a plethora of motherboards for decades. With the AMIBIOS Setup program, you can modify BIOS settings and control the various system features. This chapter describes the basic navigation of the AFE-R360 BIOS setup screens.

Main Advanced Chipset Security	Aptio Setup – AMI Boot Save & Exit MEBx	
BIOS Vendor Core Version Compliancy Project Version Build Date and Time Access Level Power Type	American Megatrends 5.0.3.2 1.00 x64 UEFI 2.9.0; PI 1.7 AFE R360000H060X019 05/31/2024 12:44:04 Administrator AT	Set the Date. Use Tab to switch between Date elements. Default Ranges: Year: 1998–9999 Months: 1–12 Days: Dependent on month Range of Years may vary.
Memory Information		
Total Memory	32768 MB	
Memory Frequency	4800 MT/s	
System Date System Time	[Fri 06/27/2025] [10:52:24]	<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2.22.1293 Copyright (C) 2024 AMI		

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in battery-backed CMOS so it retains the Setup information when the power is turned off.

4.1 Entering Setup

Turn on the computer and check for the patch code. If there is a number assigned to the patch code, it means that the BIOS supports your CPU. If there is no number assigned to the patch code, please contact an Advantech application engineer to obtain an up-to-date patch code file. This will ensure that your CPU's system status is valid. After ensuring that you have a number assigned to the patch code, press and you will immediately be allowed to enter Setup.

4.1.1 Main Setup

When you first enter the BIOS Setup Utility, you will encounter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.

Main Advanced Chipset Security	Aptio Setup – AMI Boot Save & Exit MEBx	
BIOS Vendor Core Version Compliancy Project Version Build Date and Time Access Level Power Type	American Megatrends 5.0.3.2 1.00 x64 UEFI 2.9.0; PI 1.7 AFE R360000H060X019 05/31/2024 12:44:04 Administrator AT	Set the Date. Use Tab to switch between Date elements. Default Ranges: Year: 1998–9999 Months: 1–12 Days: Dependent on month Range of Years may vary.
Memory Information Total Memory	32768 MB	
Memory Frequency	4800 MT/s	
System Date System Time	[Fri 06/27/2025] [10:52:24]	<pre>++: Select Screen f↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>



The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

System time/System date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

Chapter 4 AMI BIOS Setup

4.1.2 Advanced BIOS Features Setup

Select the Advanced tab from the AFE-R360 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screens is shown below. The sub menus are described on the following pages.

Main Advanced Chipset Securit	Aptio Setup – AMI Boot Save & Exit MEBx	
 RC ACPI Settings WMAN Configuration CPU Configuration Power & Performance PCH-FW Configuration Trusted Computing ACPI Settings iManager Configuration S5 RTC Wake Settings Serial Port Console Redirection Intel TXT Information PCI Subsystem Settings USB Configuration Network Stack Configuration NVMe Configuration 	System ACPI Parame **: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Value F3: Optimized Defa F4: Save & Exit ESC: Exit	ters. s ults
Versio	12.22.1293 Copyright (C) 2024 AMI	

4.1.2.1 RC ACPI Settings



- Native PCIE Enable Enable/Disable PCIE Native Control reported in ACPI Table.
- Native ASPM Choose ASPM feature is controlled by OS or BIOS.
- Low Power S0 Idle Capability This item determines to Enable/Disable ACPI Low Power S0 Idle Capability under OS.

4.1.2.2 WWAN Configuration

Advanced	Aptio Setup — AMI	
WWAN Device Firmware Flash Device	[5G Enabled] [Disabled]	Select the M.2 WWAN Device options to enable 5G – M80 (MediaTek) Modems
		<pre> ++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2	.22.1293 Copyright (C) 2024	AMI

WWAN Device

Select the M.2 WWAN Device option to enable 5G Modems.

Firmware Flash Device Enable or Disable WWAN Firmware Flash Device.

4.1.2.3 CPU Configuration

Advanced	Aptio Setup – AMI	
CPU Configuration		Enable/Disable CPU Flex Ratio
Brand String ID Microcode Revision VMX	Intel(R) Core(TM) Ultra 7 165H 0xA06A4 1C Supported	
SMX/TXT TXT Crash Code TXT SPAD Boot Guard Status Boot Guard ACM Policy Status	Supported 0x00000000 0x904000000000000 0xC0008000 0x00000000000000	
Boot Guard SACM Information CPU Flex Ratio Override CPU Flex Ratio Settings Intel (VMX) Virtualization Technology	0x00000010000000 [Disabled] 31 [Enabled]	<pre>++: Select Screen f↓: Select Item Enter: Select +/-: Change Opt. F1: General Help</pre>
AVX Active Performance-cores Active Efficient-cores Active SOC-North Efficient-cores Hyper-Threading AES MachineCheck	[Enabled] [All] [All] [All] [Enabled] [Enabled] [Enabled]	F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Uses is a) 22 4222 Comunicate (C) 2024	

Brand String	Intel(R) Core(TM) Ultra	Enables utilization of additional bacdware
TD	0va06a4	canabilities provided by Inte
Microcode Revision	10	(R) Trusted Execution
VMX	Supported	Technology.
SMX/TXT	Supported	Changes require a full power
TXT Crash Code	0x00000000	cycle to take effect.
TXT SPAD	0×904000000000000	
Boot Guard Status	0×C0008000	
Boot Guard ACM Policy Status	0x000000000000000	
Boot Guard SACM Information	0x00000010000000	
CPU Flex Ratio Override	[Disabled]	
CPU Flex Ratio Settings	31	++: Select Screen
Intel (VMX) Virtualization	[Enabled]	↑↓: Select Item
Technology		Enter: Select
AVX	[Enabled]	+/-: Change Opt.
Active Performance-cores	[A11]	F1: General Help
Active Efficient-cores	[A11]	F2: Previous Values
Active SOC–North Efficient–cores	[A11]	F3: Optimized Defaults
Hyper-Threading	[Enabled]	F4: Save & Exit
AES	[Enabled]	ESC: Exit
MachineCheck	[Enabled]	
MonitorMWait	[Enabled]	
Intel Trusted Execution Technology	[Disabled]	*

CPU Flex Ratio Override Ency Data CPU Flex Ratio Program

Enable/Disable CPU Flex Ratio Programming.

Intel (VMX) Virtualization Technology When Enabled, a VMM can utilize the additional hardware capability provided by Vanderpool Technology.

AVX

Enable/Disable the AVX 2/3 Instructions.

Active Performance-cores Number of P-cores to enable in each processor package.

Active Efficient-cores

Number of E-cores to enable in each processor package.

Active SOC-North Efficient-Core Number of SOC-North Efficient-cores to enable in SOC North

Hyper-Threading

This item allows users to Enable/Disable Hyper-Threading Technology.

AES Enable/Disable AES (Advanced Encryption Standard).

MachineCheck

Enable/Disable Machine Check.

MonitorMWait

Enable/Disable MonitorMWait.

Intel Trusted Execution Technology Enables utilization of additional hardware capability provided by Intel® Trusted Execution Technology.

4.1.2.4 Power & Performance

Aptio Setup – AMI Advanced	
Power & Performance > CPU – Power Management Control > GT/Media – Power Management Control	CPU – Power Management Control Options
	<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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- CPU Power Management Control
 CPU Power Management Control Options.
- GT Power Management Control
 GT Power Management Control Options.

4.1.2.4.1CPU - Power Management Control

Advanced	Aptio Setup – AMI	
Huvanceu		
CPU – Power Management Control		Enable/Disable Boot Maximum Frequency in CPU strap.
Boot Max Frequency	[Enabled]	
Boot performance mode	[Max Non-Turbo Performance]	
Intel(R) SpeedStep(tm)	[Enabled]	
Intel(R) Speed Shift Technology	[Enabled]	
Turbo Mode	[Enabled]	
 View/Configure Turbo Options Configure ToP Configurations 		
Platform Pli Enable	[Disabled]	
Platform PL2 Enable	[Disabled]	
Power Limit 4 Override	[Disabled]	
C states	[Disabled]	↔+: Select Screen
Power Limit 3 Settings		†↓: Select Item
		Enter: Select
		+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Uptimized Defaults
		F90. Evit
		Loos Entr
- Version 1	2 22 1293 Conuright (C) 2024	L AMT
Version 2		

- Boot Max Frequency Enable/Disable Boot Maximum Frequency in CPU strap.
 Boot performance mode Select the performance state that the BIOS will set before OS handoff.
 Intel® SpeedStep™ Allows more than two frequency ranges to be supported.
 Intel® Speed Shift Technology Enable/Disable Intel® Speed Shift Technology support.
- Turbo Mode Enable/Disable processor turbo mode.
- View/Configure Turbo Options
 View and Configure Turbo Options.
- **Config TDP Configuration** Config TDP Configurations.
- Platform PL1 Enable Enable/Disable Platform Power Limit 1 programming.
- Platform PL2 Enable Enable/Disable Platform Power Limit 1 programming.
- Power Limit 4 Override

Enable/Disable Power Limit 4 override.

- C states Enable/Disable CPU Power Management.
- PowerLimit 3 Settings Power Limit 3 Settings.

■ View/Configure Turbo Options

Advanced	Aptio Setup — AMI	
Current Turbo Settings		View/Configure Turbo Ratio
Max Turbo Power Limit Min Turbo Power Limit Package TDP Limit Power Limit 1 Power Limit 2	4095.875 0.0 28.0 28.0 64.0	Limit options
▶ Turbo Ratio Limit Options Energy Efficient P-state Package Power Limit MSR Lock Energy Efficient Turbo	[Enabled] [Disabled] [Enabled]	
		<pre>++: Select Screen f↓: Select Item Enter: Select</pre>
		+/-: Change Opt. F1: General Help E2: Previous Values
		F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version	2.22.1293 Copyright (C) 2024	4 AMI

- Turbo Ratio Limit Option
 View/Configure Turbo Ratio Limit Options.
- Energy Efficient P-state
 Enable/Disable Energy Efficient P-state feature.
- Package Power Limit MSR Lock
 Enable/Disable locking of Package Power Limit settings.
- Energy Efficient Turbo
 Enable/Disable Energy Efficient Turbo feature.

Advanced	Aptio Setup — AMI	
Current Turbo Ratio Limit Settings	1	Performance-core Turbo Ratio
P–core Turbo Ratio Limit CoreO (TRLC)	1	range, the turbo ratio is defined in Turbo Ratio Limit
P-core Turbo Ratio Limit Core1 (TRLC)	2	RatioO. If value is zero, this entry is ignored.
P–core Turbo Ratio Limit Core2 (TRLC)	3	
P–core Turbo Ratio Limit Core3 (TRLC)	4	
P–core Turbo Ratio Limit Core4 (TRLC)	5	
P–core Turbo Ratio Limit Core5 (TRLC)	6	++: Select Screen
P–core Turbo Ratio Limit Core6 (TRLC)	7	†∔: Select Item Enter: Select
P–core Turbo Ratio Limit Core7 (TRLC)	8	+/−: Change Opt. F1: General Help
P–core Turbo Ratio Limit RatioO (TRLR)	50	F2: Previous Values F3: Optimized Defaults
P–core Turbo Ratio Limit Ratio1 (TRLR)	50	F4: Save & Exit ESC: Exit
P-core Turbo Ratio Limit Ratio2 (TRLR)	50	
Version 2	.22.1293 Copyright (C) 2024	AMI

Chapter 4 AMI BIOS Setup

Config TDP Configurations

Advanced	Aptio Setup – AMI	
Config TDP Configurations Enable Configurable TDP Configurable TDP Boot Mode Configurable TDP Lock	[Applies to cTDP] [Nominal] [Disabled]	Applies cTDP (Assured Power) initialization settings based on non-cTDP (Assured Power) or cTDP (Assured Power). Default is 1: Applies to cTDP (Assured
CTDP BIOS control ConfigTDP Levels ConfigTDP Turbo Activation Ratio Power Limit 1 Power Limit 2	[Disabled] 3 13 (Unlocked) 28.0W (MSR:28.0) 64.0W (MSR:64.0)	Power); if 0 then applies non-cTDP (Assured Power) and BIOS will bypass cTDP (Assured Power) initialzation flow
Custom Settings Nominal ConfigTDP Nominal	Ratio:14 TAR:13	
Power Limit 1 Power Limit 2 Power Limit 1 Time Window ConfigTDP Turbo Activation Ratio	PL1:28.0W 0 [0] 0	++: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help E2: Browlears Values
Custom Settings Level1 ConfigTDP Level1 Power Limit 1 Power Limit 2 Power Limit 1 Time Window ConfigTDP Turbo Activation Ratio	Ratio:10 TAR:9 PL1:20.0W 0 0 [0] 0	F2: Previous values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version	2.22.1293 Conuright (C) 2024	L AMT

- Enable Configurable TDP Applies TDP initialization settings based on non-cTDP or cTDP.
- Configurable TDP Boot Mode Configurable TDP Mode as Nominal/Up/Down/Deactivate TDP selection.
- Configurable TDP Lock
 Configurable TDP Mode Lock sets the Lock bit.
- CTDP BIOS control Enables CTDP control via runtime ACPI BIOS method.
- Power Limit 1
 Power Limit 1 in Milli Watts.
- Power Limit 2
 Power Limit 2 in Milli Watts.
- Power Limit 1 Time Window
 Power Limit 1 Time Window value in seconds.
- ConfigTDP Turbo Activation Ration
 Custom value for Turbo Activation Ratio.

Power Limit 3 Settings



- Power Limit 3 Override

Enable/Disable Power Limit 3 override.

4.1.2.4.2GT - Power Management Control

Advanced	Aptio Setup – AMI	
GT/Media – Power Management Control RC6(Render Standby) MC6(Media Standby) Maximum GT frequency Disable Turbo GT frequency	[Enabled] [Enabled] [Default Max Frequency] [Disabled]	Check to enable render standby support.
		<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2	.22.1293 Copyright (C) 2024	AMI

- RC6 (Render Standby) Check to enable render standby support.
- Maximum GT frequency Maximum GT frequency limited by user.
- Disable Turbo GT frequency Enabled/Disabled Turbo GT frequency.
- MC6 (Media Standby) Check to enable Media standby support.

4.1.2.5 PCH-FW Configuration

Advanced	Aptio Setup – AMI	
ME Firmware Version ME Firmware Mode ME Firmware SKU ME Firmware Status 1 ME Firmware Status 2 ME State	18.0.5.2107 Normal Mode Corporate SKU 0x90000255 0x6B008300 [Enabled]	Configure Intel(R) Active Management Technology Parameters
Manageability Features State AMT BIOS Features > AMT Configuration ME Unconfig on RTC Clear Core Bios Done Message	[Enabled] [Enabled] [Enabled] [Enabled]	
▶ Firmware Update Configuration		<pre>++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version	2.22.1293 Copyright (C) 202	4 AMI

- ME State When Disabled ME will be put ME into Temporarily Disabled Mode.
- Manageability Feature State When Disabled, ME will not be unconfigured on RTC Clear.
- AMT BIOS Features
 When Disabled, ME will not be unconfigured on RTC Clear.
- AMT Configuration
 Configure Intel® Active Management Technology Parameters.
- ME Unconfig on RTC Clear When Disabled, ME will not be unconfigured on RTC Clear.
- Core BIOS Done Message Enable/Disable Core BIOS Done message sent to ME.
 Firmware Update Configuration
- Firmware Update Configuration
 Configure Management Engine Technology Parameters.

4.1.2.5.1AMT Configuration

Advanced	Aptio Setup – AMI	
USB Provisioning of AMT Activate Remote Assistance Process Unconfigure ME	[Disabled] [Disabled] [Disabled]	Enable/Disable of AMT USB Provisioning. ++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help
		F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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- USB Provision of AMT Enable/Disable of AMT BIOS Provisioning.
- Active Remote Assistance Process Trigger CIRA boot.
- Unconfigure ME Unconfigure ME with resetting MEBx password to default on next boot.

4.1.2.5.2AMT Configuration

Me FW Image Re-Flash [Disabled] Enable/Disable Me FW Image Re-Flash function. FW Update [Enabled] ++: Select Screen ++: Select Screen ++: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit F4: Save & Exit	Advanced	Aptio Setup — AMI	
++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit F4: Save & Exit	Me FW Image Re-Flash FW Update	[Disabled] [Enabled]	Enable/Disable Me FW Image Re-Flash function.
			<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>

4.1.2.6 Trusted Computing

Advanced	Aptio Setup – AMI	
TPM Device Selection	[dTPM]	Selects TPM device: fTPM or
TPM 2.0 Device Found Firmware Version:	7.2	dTPM - Disables fTPM and
Vendor:	NTC	fTPM/dTPM will be disabled and all data saved on it will be
Security Device Support Active PCR banks	[Enable] SHA256	lost.
Available PCR banks	SHA256,SHA384	
SHA256 PCR Bank SHA384 PCR Bank	[Enabled] [Disabled]	
Pending operation	[None]	++: Select Screen
Plat†orm Hierarchy Storage Hierarchy	[Enabled] [Enabled]	T∔: Select Item Enter: Select
Endorsement Hierarchy Physical Presence Spec Version	[Enabled] [1.3]	+/−: Change Opt. F1: General Help
TPM 2.0 InterfaceType Device Select	[TIS] [Auto]	F2: Previous Values F3: Optimized Defaults
		F4: Save & Exit ESC: Exit
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- Security Device Support Enable or disable BIOS support for security device.
- SHA256 PCR Bank Enable or Disable SHA256 PCR Bank.
- Pending operation
 Schedule an Operation for the Security Device.
- Platform Hierarchy Enable or Disable Platform Hierarchy.
- Storage Hierarchy Enable or Disable Storage Hierarchy.
- Endorsement Hierarchy
 Enable or Disable Endorsement Hierarchy.
- Physical Presence Spec Version Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3.
- Device Select TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices.

4.1.2.7 ACPI Settings



- Enable ACPI Auto Configuration Enable or disable BIOS ACPI auto configuration.
 Enable Hibernation Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
- ACPI Sleep State
 Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
- PCIE Wake Enable or disable PCIE to wake the system from S5.

Chapter 4 AMI BIOS Setup

4.1.2.8 iManager Configuration

Advanced	Aptio Setup — AMI	
iManager Configuration		Select the Critical
iManager Chipset Firmware Version	EIO-300 X01044494	must shutdown the system.
ACPI Shutdown Temperature Power Saving Mode Backlight Enable Polarity Backlight Control Mode Brightness PWM Polarity Brightness Control Enable	[By EC] [Normal] [By EC] [By EC] [By EC] [By EC]	
 Serial Port 1 Configuration Serial Port 2 Configuration Serial Port 3 Configuration Serial Port 4 Configuration Hardware Monitor Watch Dog Timer Configuration Case Open Detection GPIO Configuration 	[Disabled]	++: Select Screen †1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults
USB Power Enable Control 1 USB Power Enable Control 2	[Enabled] [Enabled]	F4: Save & Exit ESC: Exit

ACPI Shutdown Temperature
Enable/Disable CPU Shutdown Temperature.
Power Saving Mode
Enable/Disable power saving mode.
Backlight Enable Polarity
Switch Backlight Enable Polarity for Native or Invert.
Backlight Control Mode
Switch Backlight Control to PWM or DC mode.
Brightness PWM Polarity
Backlight Control Brightness PWM Polarity for Native or Invert.
Brightness Control Enable
Choose to control LVDS brightness value by EC or User overrid
stage.
Serial Port 1 Configuration
Set Parameters of Serial Port 1.
Serial Port 2 Configuration

- Serial Port 2 Configuration Set Parameters of Serial Port 2.
 Serial Port 3 Configuration
- Set Parameters of Serial Port 3.
- Serial Port 4 Configuration Set Parameters of Serial Port 4.
- Hardware Monitor Monitor hardware Status.
- Watch Dog Timer Configuration Watch Dog Timer Configuration Page.
- Case Open Detection
 Enable or Disable Case Open Detect Function.

override during POST

GPIO Configuration GPIO Configuration Settings.

4.1.2.8.1Serial Port 1 Configuration



- Serial Port Enable or Disable Serial Port (COM).
- Change Settings Select an optimal settings for Super IO device.
- COM Port Mode COM Port Mode Select.

4.1.2.8.2Serial Port 2 Configuration



- Serial Port Enable or Disable Serial Port (COM).
- Change Settings
 Select an optimal settings for Super IO device.
- COM Port Mode COM Port Mode Select.

4.1.2.8.3Serial Port 3 Configuration



- Serial Port Enable or Disable Serial Port (COM).
- Change Settings Select an optimal settings for Super IO device.
- COM Port Mode COM Port Mode Select.

4.1.2.8.4Serial Port 4 Configuration



- Serial Port Enable or Disable Serial Port (COM).
- Change Settings
 Select an optimal settings for Super IO device.
- COM Port Mode COM Port Mode Select.

4.1.2.8.5Hardware Monitor



4.1.2.8.6Watch Dog Timer Configuration

Advanced	Aptio Setup – AMI	
Watch Dog Timer Configuration		Enabled or Disabled Watch Dog
Watch Dog Timer	[Disabled]	<pre>Timer function (Start before boot to OS and must stop by self) ++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. Fl: General Help F2: Previous Values F3: Optimized Defaults</pre>
		F4: Save & Exit ESC: Exit
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Watch Dog Timer

Enable or Disable Watch Dog Timer Function.

4.1.2.8.7GPIO Configuration

Advanced	Aptio Setup – AMI	
GPIO Configuration		Choose to control GPIO by EC
GPIO Control Enable		stage.
		<pre>++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. Fl: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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 GPIO Control Enable Choose to control GPIO by EC or user override during POST stage.
 GPIO0/1/2/3/4/5/6/7

Configure GPIO0/1/2/3/4/5/6/7.

4.1.2.9 S5 RTC Wake Settings



Wake system from S5

Enable or disable System wake on alarm event. Select FixedTime, system will wake on the hr::min::sec specified.

4.1.2.10 Serial Port Console Redirection

Advanced	Aptio Setup – AMI	
COM1 Console Redirection ▶ Console Redirection Settings	[Disabled]	Console Redirection Enable or Disable.
COMMI(PC1 Bus0,Dev0,FuncO) (Disabled) Console Redirection	Port Is Disabled	
Serial Port for Out-of-Band Manageme Windows Emergency Management Service Console Redirection EMS ▶ Console Redirection Settings	nt/ s (EMS) [Disabled]	
		<pre> ++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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Console Redirection
 This item allows users to configuration console redirection deta

This item allows users to configuration console redirection detail settings.

Console Redirection EMS

This item allows users to enable or disable console redirection for Microsoft Windows Emergency Management Services (EMS).

4.1.2.11 Intel TXT Information

Advanced	Aptio Setup – AMI	
Intel TXT Information Chipset BiosAcm Chipset Txt Cpu Txt Error Code	Production Fused Production Fused Supported Supported None	
Class Code Major Code Minor Code	None None None	++: Select Screen
		<pre>11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit</pre>
Vers	ion 2.22.1293 Copyright (C) 202	4 AMI

Intel TXT Information Display Intel TXT information.
4.1.2.12 PCI Subsystem Settings



Above 4G Decoding

Globally Enables or Disables 64bit capable Devices to be Decoded in Above 4G Address Space. (Only if System Supports 64 bit PCI Decoding).

Re-size BAR Support

If system has Resizable BAR capable PCIe Devices, this option Enables or Disables Resizable BAR Support.

SR-IOV Support

If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.

4.1.2.13 USB Configuration

Advanced	Aptio Setup – AMI	
USB Configuration		This is a workaround for OSes
USB Module Version	35	WITHOUT XHCI HAND-OTT SUPPORT. The XHCI ownership change should be claimed by XHCI
USB Controllers: 2 XHCIs		driver.
USB Devices: 1 Drive, 2 Keyboards, 1 Mouse,	1 Hub	
XHCI Hand–off USB Mass Storage Driver Support	[Enabled] [Enabled]	
USB hardware delays and time-outs:		
USB transfer time-out Device reset time-out	[20 sec] [20 sec]	↔: Select Screen t∔: Select Item
Device power-up delay	[Auto]	Enter: Select +/-: Change Opt.
Mass Storage Devices: TOSHIBA TransMemory PMAP	[Auto]	F1: General Help F2: Previous Values
	[hato]	F3: Optimized Defaults
		ESC: Exit
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Legacy USB Support

Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

XHCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

- USB Mass Storage Driver Support Enable/Disable USB Mass Storage Driver Support.
- USB transfer time-out
 Time-out value for control, Bulk, and interrupt transfers.
- Device reset time-out

USB mass storage device start unit command time-out.

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

4.1.2.14 Network Stack Configuration

Advanced	Aptio Setup – AMI	
Network Stack	[Disabled]	Enable/Disable UEFI Network Stack **: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Versi	on 2.22.1293 Copyright (C) 202	24 AMI

Network Stack Enable/Disable UEFI Network Stack.

4.1.2.15 NVMe Configuration



4.1.3 Chipset Configuration

Select the Chipset tab from the AFE-R360 setup screen to enter the Chipset BIOS Setup screen. You can display a Chipset BIOS Setup option by highlighting it using the <Arrow> keys. All Plug and Play BIOS Setup options are described in this section. The Plug and Play BIOS Setup screen is shown below.

Main Adva	anced Chipset	Apt Security Boot	io Setup – AMI Save & Exit MEBx	
 System Ager PCIE Config PCH-IO Config 	nt (SA) Configu guration figuration	ration		System Agent (SA) Parameters
				<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
		Version 2.22.1	293 Copyright (C) 2024	AMI

4.1.3.1 System Agent (SA) Configuration

Chipset	Aptio Setup — AMI	
System Agent (SA) Configuration		Memory Configuration Parameters
 Memory Configuration TCSS setup menu VMD setup menu VT-d setup menu 		
Above 4GB MMIO BIOS assignment IPU Device (B0:D5:F0) NPU Device (B0:D11:F0)	[Enabled] [Disabled] [Enabled]	
		<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2	.22.1293 Copyright (C) 2024	AMI

- Memory Configuration Memory Configuration Parameters.
- TCSS setup menu TCSS Configuration settings.
- VMD setup menu VMD setup
- VT-d VT-D capability.

4.1.3.1.1Memory Configuration

Chipset	Aptio Setup – AMI	
Memory Configuration Memory RC Version Memory Frequency tCL-tRCD-tRP-tRAS SO-DIMM 1 SO-DIMM 2 Size Number of Ranks Manufacturer	1.2.4.9 4800 MT/s 40-39-39-77 Not Populated / Disabled Populated & Enabled 32768 MB (DDR5) 2 Advantech Co Ltd	Enable Or Disable Base Memory Test Run on Warm Boot
Memory Test on Warm Boot Max TOLUD SAGV Memory Scrambler Force ColdReset Memory Remap	[Enabled] [Dynamic] [Disabled] [Enabled] [Disabled] [Enabled]	++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Ve	ersion 2.22.1293 Copyright (C) 2024	4 AMI

- Memory Test on Warm Boot Enable/Disable Base Memory Test Run on Warm Boot.
 Max TOLUD
 - Maximum Value of TOLUD.
- SA GV System Agent Geysetville.
- Memory Scrambler
 Enable/Disable Memory Scrambler support.
- Force ColdReset Force ColdReset OR Choose MrcColdBoot mode.
- Memory Remap Enable/Disable Memory Remap above 4GB.

4.1.3.1.2TCSS Setup Menu

Chipset	Aptio Setup – AMI	
TCSS Configuration		Enable/Disable TCSS xHCI
IOM FW version: 30001A00		
PHY FW version: 1865		
TBT FW IMR Status: COOOO385 TBT FW version: 0901 Deepest TC state: 000A		
TCSS xHCI Support ITBT PCIE1 Root Port ITBT DMA0	[Enabled] [Enabled] [Enabled]	
		↑↓: Select Item
		+/-: Change Opt.
		F2: Previous Values
		F3: Uptimized Defaults F4: Save & Exit
		ESC: Exit
Version 2	.22.1293 Copyright (C) 2024	AMI

- TCSS xHCl Support Enable/Disable TCSS xHCl.
- ITBT PECI1 Root Port Enable/Disable ITBT PCIE Root.
- ITBT DMA0 Enable/Disable ITBT DMA0.

4.1.3.1.3VMD Setup Menu



4.1.3.1.4VT-d Setup Menu

	Antin Onturn ANT	
Chipset	Hptio Setup – HMi	
VT–d Configuration		Enable DMA Protection in
VT-d	Supported	table is installed in DXE and If VTD_INFO_PPI is installed
VT-d Pre-boot DMA Protection X2APIC Opt Out DMA Control Guarantee	[Enabled] [Disabled] [Disabled] [Enabled]	in PEI.)
		++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
	aian 2 22 1222 Parunisht de	THA LCC

Chapter 4 AMI BIOS Setup

4.1.3.1.5IPU Device Enable (for MIPI-CSI sensor enabling)

Chipset	Aptio Setup – AMI	
System Agent (SA) Configuration		MIPI Camera Configuration
 Memory Configuration TCSS setup menu VMD setup menu VT-d setup menu 		
Above 4GB MMIO BIOS assignment IPU Device (B0:D5:F0) NPU Device (B0:D11:F0) ▶ MIPI Camera Configuration	[Enabled] [Enabled] [Enabled]	
		<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2	.22.1293 Copyright (C) 2024	AMI

IPU Device

IPU Enabled to allow CPU process video streaming from MIPI-CSI inputs.



- Camera 1 Option Camera input from CN1, 5 on MIOe-MIPI.
- Camera2 Option Camera input from CN2, 6 on MIOe-MIPI.
- Camera3 Option Camera input from CN3 on MIOe-MIPI.
- Camera4 Option Camera input from CN4 on MIOe-MIPI.

Chipset	Aptio Setup – AMI	
Camera1 Sensor Model	[e-CAM25_CUR360] Sensor Model EV2M-GOM1 EV2M-OOM1 e-CAM25_CUR360	Sensor Model
	e-CAMB1_CUR360 User Custom	++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

- Link Options-Camera1 MIPI-CSI sensor selection, select by camera model name.
- Link Options-Camera2 MIPI-CSI sensor selection, select by camera model name.
- Link Options-Camera3 MIPI-CSI sensor selection, select by camera model name.
- Link Options-Camera4 MIPI-CSI sensor selection, select by camera model name.

Chipset	Aptio Setup — AMI	
Camera1 Sensor Model Custom HID PPR Value PPR Unit Camera module name MIPI port LaneUsed I2C Channel Device 0 I2C Address	[User Custom] 10 A 0 [x2] [I2C3] 8	Sensor Model
		<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version	2.22.1293 Copyright (C) 2024	AMI

Table 4.1: Link Options-User Custom

MIOe-MIPI	Sensor Model	Custom HID	LaneUsed	MIPI port	I2C Channel	I2C Address
CN1	By Sensor	By Sensor	X2	0	I2C3	By Sensor
CN2	By Sensor	By Sensor	X2	1	I2C4	By Sensor
CN3	By Sensor	By Sensor	X2	4	I2C1	By Sensor
CN4	By Sensor	By Sensor	X2	5	I2C2	By Sensor
CN5	By Sensor	By Sensor	X4	4	I2C1	By Sensor
CN6	By Sensor	By Sensor	X4	0	I2C2	By Sensor

4.1.3.2 PCI Express Configuration

Chinset	Aptio Setup – AMI	
SOC Configuration > PCI Express Root Port PXPA1 PCI Express Root Port PXPA2 > PCI Express Root Port PXPA3 PCI Express Root Port PXPA4 IOE Configuration > PCI Express Root Port PXPD	Shadowed by x2/x4 port Shadowed by x2/x4 port	PCI Express Root Port Settings.
 PCI Express Root Port PXPE 		<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Versi	on 2.22.1293 Copyright (C) 202	24 AMI

PCI Express Root Port PXPA1/PXPA2/PXPA3/PXPA4/PXPD/PXPE PCI Express Root Port Settings.

4.1.3.3 PCH-IO Configuration

Chipset	Aptio Setup - AMI		
PCH-IO Configuration		SATA Device Options Settings	
 SATA Configuration USB Configuration Security Configuration HD Audio Configuration 			
Windows SMI	[Enable SMI and Enable SMI Lock]		
Onboard LAN1 Controller LAN1 PXE OpROM Onboard LAN2 Controller LAN2 PXE OpROM Onboard LAN3 Controller LAN3 PXE OpROM Restore AC Power Loss SPD Write Disable	[Enabled] [Disabled] [Enabled] [Disabled] [Disabled] [Power Off] [TRUE]	<pre>++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>	
Version 2.22.1293 Copyright (C) 2024 AMI			

- SATA Configuration SATA Device Options Settings.
- USB Configuration USB Configuration Settings.
- Security Configuration Security Configuration Settings.
- HD Audio Configuration HD Audio Subsystem Configuration Settings.
- PCH LAN Controller Enable or Disable onboard NIC.
- Wake on LAN Enable Enable or Disable Integrated LAN to wake the system.
- LAN1 PXE ROM Enable or disable boot option for LAN1 Controller.
- Onboard LAN2 Controller Select to Enable or Disable onboard LAN2 Controller.
- LAN2 PXE ROM Enable or disable boot option for LAN2 Controller.
- Restore AC Power Loss
 Specify what state to go to when power is re-applied after a power failure (G3 state).
- SPD Write Disable Enable/Disable setting SPD Write Disable.

4.1.3.3.1SATA Configuration

Chipset	Aptio Setup – AMI	
SATA Configuration		Enable/Disable SATA Device.
SATA Controller(s) SATA Mode Selection SATA Controller Speed Limit Aggressive LPM Support M.2 SATA Port Software Preserve Port 1 SATA Port 1 DevSlp	[Enabled] [AHCI] [Default] [Disabled] Empty Unknown [Enabled] [Disabled]	<pre>++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values</pre>
Vansian	2 22 1292 Comunicat (P) 2024	F3: Optimized Defaults F4: Save & Exit ESC: Exit

- SATA Controller Enable or Disable SATA Device.
- SATA Mode Selection
 Determines how SATA controllers operate.
- SATA Controller Speed Limit Indicates the maximum speed the SATA controller can support.
- Aggressive LPM Support Enable PCH to aggressively enter link power state.

M.2 SATA Port

- Port 1 Enable or Disable SATA Port.
- SATA Port 1 DevSlp Enable/Disable SATA Port 1 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen.

4.1.3.3.2USB Configuration



USB Port Disable Override

Selectively Enable/Disable the corresponding USB Port from reporting a Device Connection to the Controller.

Chapter 4 AMI BIOS Setup

4.1.3.3.3Security Configuration

Chipset	Aptio Setup – AMI		
Security Configuration		Enable will lock bytes 38h–3Fh	
RTC Memory Lock BIOS Lock Force unlock on all GPIO pads	[Enabled] [Disabled] [Disabled]	bank of RTC RAM	
		<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>	
Version 2.22.1293 Copyright (C) 2024 AMI			

RTC Memory Lock

Enable will lock bytes 38h-3Fh in the lower/upper 128-byte bank of RTC RAM.

- BIOS Lock Enable or Disable the PCH BIOS Lock Enable feature.
- Force unlock on all GPIO pads If Enabled BIOS will force all GPIO pads to be in unlock state.

4.1.3.3.4HD Audio Configuration



HD Audio

Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled. Enabled = HDA will be unconditionally Enabled.

4.1.3.3.5SerialIO Configuration

Chipset	Aptio Setup – AMI			
SerialIo Configuration		Enables/DisablesSerialIo		
I2CO Controller	[Enabled]	Controller		
1201 Controller	[Enabled]	If given device is Function O PSE disabling is skinned PSE		
▶ Serial IO I2CO Settings		default will remain and device		
▶ Serial IO I2C1 Settings		PCI CFG Space will still be		
SerialIO timing parameters	[Disabled]	visible. This is needed to		
		allow PCI enumerator access		
		multifunction device		
		The following devices depend 🔻		
		++: Select Screen		
		Fnter: Select		
		+/-: Change Opt.		
		F1: General Help		
		F2: Previous Values		
		F3: Optimized Defaults		
		F4: Save & Exit		
		ESC. EXIT		
Version 2.22.1284 Copyright (C) 2022 AMI				

- I2C0/I2C1 Controller Enable/Disable SerialIO Controller.
- Serial IO I2C0/I2C1 Settings Configure Seriallo Controller.
- SerialIO timing parameters
 Enable additional timing parameters for all SerialIO controllers.

4.1.4 Security



Select Security Setup from the AFE-R360 Setup main BIOS setup menu. All Security Setup options, such as password protection and virus protection are described in this section. To access the sub menu for the following items, select the item and press <Enter>:

Change Administrator/User Password

Select this option and press <ENTER> to access the sub menu, and then type in the password.

Secure Boot

Secure Boot Configurations.

4.1.5 Boot



Setup Prompt Timeout

Number of seconds that the firmware will wait before initiating the original default boot selection. A value of 0 indicates that the default boot selection is to be initiated immediately on boot. A value of 65535(0xFFFF) indicates that firmware will wait for user input before booting. This means the default boot selection is not automatically started by the firmware.

 Bootup NumLock State Select the keyboard NumLock state.

Quiet Boot

Enables or disables Quiet Boot option.

Boot Option #1

Sets the system boot order.

Fast Boot

Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

4.1.6 Save & Exit



Save Changes and Exit This item allows you to exit system setup after saving the changes.

- Discard Changes and Exit This item allows you to exit system setup without saving any changes.
- Save Changes and Reset This item allows you to reset the system after saving the changes.
- Discard Changes and Reset This item allows you to rest system setup without saving any changes.
- Save Changes This item allows you to save changes done so far to any of the options.
- Discard Changes
 This item allows you to discard changes done so far to any of the options.
- Restore Defaults This item allows you to restore/load default values for all the options.
- Save as User Defaults This item allows you to save the changes done so far as user defaults.
- Restore User Defaults This item allows you to restore the user defaults to all the options.
- Boot Override Boot device select can override your boot priority.



System Assignments

A.1 System I/O Ports

Addr. Range (Hex) Device 00h-1Fh DMA Controller 20h-2Dh Interrupt Controller 2Eh–2Fh Motherboard resources 30h-3Dh Interrupt Controller 40h-43h Timer/Counter 4Eh–4Fh Motherboard resources 50h-53h Timer/Counter 60h-6Fh 8042 (keyboard controller)/NMI Controller/Microcontroller 70h-7Fh Real-time Controller 80h-8Fh Debug Port/Reserved 90h-9Fh Debug Port/Reset Generator A0h-ADh Interrupt Controller **B0h-B1h Interrupt Controller B4h-BDh Power Management** 200h-27Fh CANBus Controller 280h-28Fh I2C Controller 290h-29Fh EC Index port and Data port 2A0h-2BFh GPIO Controller 2C0h-2DFh SMBus Controller 2E8h-2EFh Communications Port (COM4) 2F0h-2F7h EC/PMC Controller 2F8h-2FFh Communications Port (COM2) 300h-37Fh CANBus Controller 3E8h-3EFh Communications Port (COM3) 3F8h-3FFh Communications Port (COM1) 480h-4CFh Motherboard resources 4D0h-4D1h Interrupt Controller 680h-69Fh Motherboard resources A00h-AFFh Motherboard resources 164Eh-164Fh Motherboard resources 1800h-18FFh Motherboard resources CF9h-CF9h Reset Generator

A.2 DMA Channel Assignments

Channel Function

0 Available 1 Available 2 Available 3 Available 4 Direct memory access controller 5 Available 6 Available 7 Available

A.3 1st MB Memory Map

Addr. Range (Hex) Device

E0000h - FFFFh System board D0000h - DFFFFh PCI Bus C0000h - CFFFFh System board A0000h - BFFFFh PCI Bus A0000h - BFFFFh Intel® HD Graphic 00000h - 9FFFFh System board

A.4 Interrupt Assignments

Interrupt# Interrupt source

NMI Parity error detected **IRQ0** System timer IRQ1 Using SERIRQ, Keyboard Emulation IRQ2 Interrupt from controller 2 (cascade) IRQ3 Communications Port (COM2) IRQ4 Communications Port (COM1) IRQ5 EC Watch Dog **IRQ6 CANBus Controller** IRQ7 Communications Port (COM3) IRQ8 System CMOS/real time clock IRQ9 Microsoft ACPI-Compliant System IRQ10 Communications Port (COM4) **IRQ11** Display Controller **IRQ12** Available IRQ13 Numeric data processor **IRQ14 GPIO Controller IRQ15** Reserved



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