PhanTAM-9XXC Series

15.6”, 21.5” Fanless Stainless Steel Display

User Manual

Release Date	Revision
OCT. 2024	V1.2

Aplex Technology, Inc.

15F-1, No.186, Jian Yi Road, Zhonghe District, New Taipei City 235, Taiwan

Tel: 886-2-82262881 Fax: 886-2-82262883 URL: https://www.aplex.com/

Revision History

Reversion	Date	Description
1.0	2023/05/05	Official Version
1.1	2023/06/15	1.2 delete 2.5” SSD for option
1.2	2024/10/14	Page 3 1. Delete logistics statement 2. Add Safety Precauion

Warning!

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, it may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

Electric Shock Hazard – Do not operate the machine with its back cover removed. There are dangerous high voltages inside.

Caution

Risk of explosion if the battery is replaced with an incorrect type.

Batteries should be recycled where possible. Disposal of used batteries must be in accordance with local environmental regulations.

Disclaimer

This information in this document is subject to change without notice. In no event shall Aplex Technology Inc. be liable for damages of any kind, whether incidental or consequential, arising from either the use or misuse of information in this document or in any related materials.

Safety Precautions

Follow the messages below to prevent your systems from damage:

◆ Avoid your system from static electricity on all occasions.

◆ Prevent electric shock. Don‘t touch any components of this card when the card is power-on. Always disconnect power when the system is not in use.

◆ Disconnect power when you change any hardware devices. For instance, when you connect a jumper or install any cards, a surge of power may damage the electronic components or the whole system.

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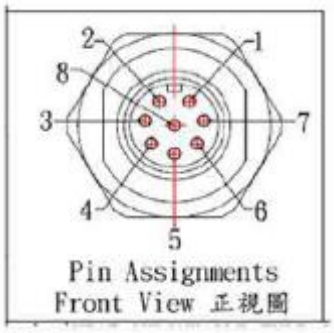
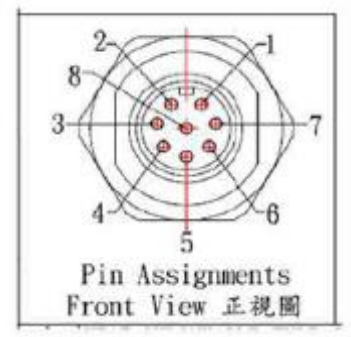
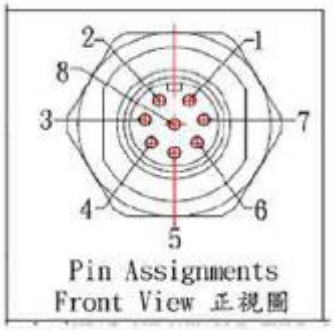
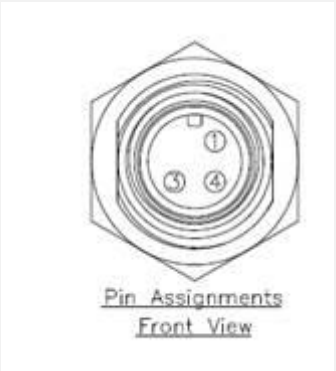
Chapter 1 Getting Started

1.1 Features

- 15.6”/21.5” Intel® 11th Gen. Fanless Stainless Steel display
- Gap-free sealing and Slim Front Frame architecture at front bezel
- IP66/IP69K Full sealed with Anti-Corrosion Enclosure
- Special Hygienic Screws on I/O Cover
- Optional Robust Waterproof Wireless Antenna Cover and Air Pressure Balance Screw
- M12 Connectors with waterproof cover and chain
- DC 9~36V wide range power input

1.2 Specifications

<table>
<tr><th></th><th>PhanTAM-916CP/R(H)</th><th>PhanTAM-921CP/R(H)</th></tr>
<tr><td colspan="3">System</td></tr>
<tr><td>CPU</td><td colspan="2">Onboard Intel® 11th Gen (Tiger Lake-UP3) Processors:
Core™ i5-1145G7E (4C, 1.5 GHz, up to 4.1GHz, 28W TDP)
Core™ i3-1115G4E (2C, 2.2 GHz, up to 3.9GHz, 28W TDP)</td></tr>
<tr><td>Memory</td><td colspan="2">2 x SO-DIMM up to 64GB DDR4 3200MHz(Dual Channel, Non-ECC)</td></tr>
<tr><td>Graphics</td><td colspan="2">Intel®Iris®Xe Graphics
Intel UHD Graphics for 11th Gen Processors</td></tr>
<tr><td>LVDS</td><td colspan="2">1 x 18/24 bit Dual Channel</td></tr>
<tr><td colspan="3">Outside IO Port – Standard M12 I/O Connector on the Rear Side</td></tr>
<tr><td>USB</td><td>1 x M12 8-pin for 2x USB2.0 with waterproof cover and chain
USB1/2:
<table>
<tr><th>CN1</th><th>Pin Define</th></tr>
<tr><td>1</td><td>USB1 5V</td></tr>
<tr><td>3</td><td>D1-</td></tr>
<tr><td>4</td><td>D1+</td></tr>
<tr><td>7</td><td>GND</td></tr>
<tr><td>2</td><td>USB2 5V</td></tr>
<tr><td>5</td><td>D2-</td></tr>
<tr><td>6</td><td>D2+</td></tr>
</table></td><td> 
</td></tr>
</table>

<table>
<tr><td></td><td><table><tr><td>8</td><td>GND</td></tr></table></td><td></td></tr>
<tr><td>Serial/Parallel</td><td>1 x M12 8-pin COM1, RS-232/422/485, Default RS-232, with waterproof cover and chain<table><tr><td></td><td>Pin Define</td></tr><tr><td>1</td><td>DCD</td></tr><tr><td>2</td><td>RXD</td></tr><tr><td>3</td><td>TXD</td></tr><tr><td>4</td><td>DTR</td></tr><tr><td>5</td><td>GND</td></tr><tr><td>6</td><td>DSR</td></tr><tr><td>7</td><td>RTS</td></tr><tr><td>8</td><td>CTS</td></tr></table></td><td> 
</td></tr>
<tr><td>LAN</td><td>1 x M12 8-pin for LAN with waterproof cover and chain
LAN:<table><tr><td></td><td>Pin Define</td></tr><tr><td>1</td><td>LAN1_0+</td></tr><tr><td>2</td><td>LAN1_0-</td></tr><tr><td>3</td><td>LAN1_1+</td></tr><tr><td>4</td><td>LAN1_1-</td></tr><tr><td>5</td><td>LAN1_2+</td></tr><tr><td>6</td><td>LAN1_2-</td></tr><tr><td>7</td><td>LAN1_3+</td></tr><tr><td>8</td><td>LAN1_3-</td></tr></table></td><td> 
</td></tr>
<tr><td>Power</td><td>1 x M12 3-pin for DC power with waterproof cover and chain<table><tr><td></td><td>Pin Define</td></tr><tr><td>1</td><td>NC</td></tr><tr><td>3</td><td>VCC</td></tr><tr><td>4</td><td>GND</td></tr></table></td><td> 
</td></tr>
<tr><td colspan="3">Option I/O Port (Either two)</td></tr>
<tr><td></td><td colspan="2">2 x optional blank M12 connectors with waterproof cap for selecting two from the following options:</td></tr>
</table>

Option	2 x USB 2.0 1 x USB 3.2 Gen1 1 x COM		
Storage Space			
Storage	1 x M.2 M-Key 2280 (PCIex4 as default)		
Expansion			
Expansion Slot	1 x M.2 2230 E-Key (PCIex2+USB2.0) socket for WIFI/BT and Antenna at rear side (option) 1 x Full-size mPCIe/mSATA with NANO-SIM (mPCIe as default, select by BIOS)		
RFID module	RFID module design on the front side (option)		
Display – Standard LCD			
Display Type	15.6” TFT LCD		21.5” TFT LCD
Max. Resolution	1366 x 768	1920 x 1080	1920 x 1080
Max. Color	16.7M	16.2M	16.7M
Luminance (cd/m^2)	400	450	250
Contrast Ratio	500:1	800:1	1000:1
Viewing Angle(H/V)	170/160	170/170	178/178
Backlight Lifetime	50,000hrs	50,000hrs	50,000hrs
Option	Optical bonding		
Display – High Brightness LCD (option)			
Display Type	15.6” TFT LCD		21.5” TFT LCD
Max. Resolution	1366 x 768	1920 x 1080	1920 x 1080
Max. Color	16.7M	16.2M	16.7M
Luminance (cd/m^2)	1000	1000	1000
Contrast Ratio	1000:1	1000:1	1000:1
Viewing Angle(H/V)	160/160	170/170	178/178
Backlight Lifetime	50,000hrs	50,000hrs	50,000hrs
Option	Optical bonding		
Touch Screen			
Type	Resistive touch window (for R model) Projected capacitive touch screen (for P model)		
Interface	USB		
Light Transmission	Resistive touch window: over 80% Projected capacitive touch screen: over 90%		
Power			
Power Input	DC 9~36V		

Power Consumption	MAX:31.8W (916CP)	MAX:34.05W (921CP)
Mechanical		
Color	304 Stainless steel enclosure (default) 316 Stainless steel enclosure (option)	
Construction	Stainless steel enclosure	
Mounting	VESA mount 100 x 100 or SWING ARM	
IP Rating	IP66/IP69K	
Dimension (mm)	403.4 x 254.4 x 64.9	539.4 x 331.4 x 61.9
Net Weight(Kg)	5.1	7.9
Environmental		
Operating temperature	0~50°C (-20~60°C for option)	
Storage temperature	-30~70°C	
Storage humidity	10 to 90% @ 40°C, non- condensing	
Certification	Meet CE / FCC Class A	
Operating System Support	Windows 10 IoT ENT LTSC	

1.3 Dimensions

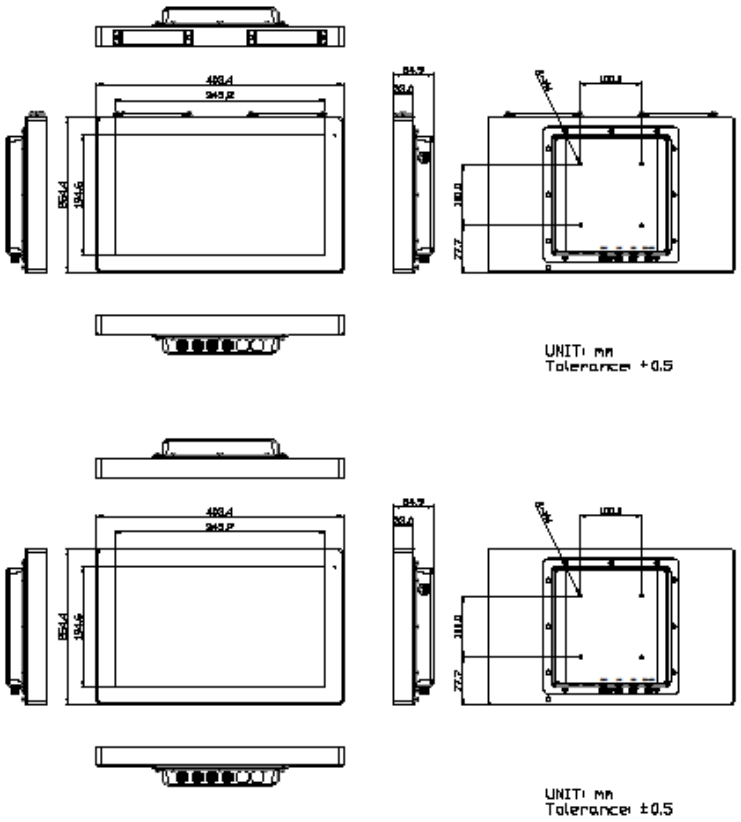


Figure 1.1: Dimensions of PHANTAM-916CP/R(H)

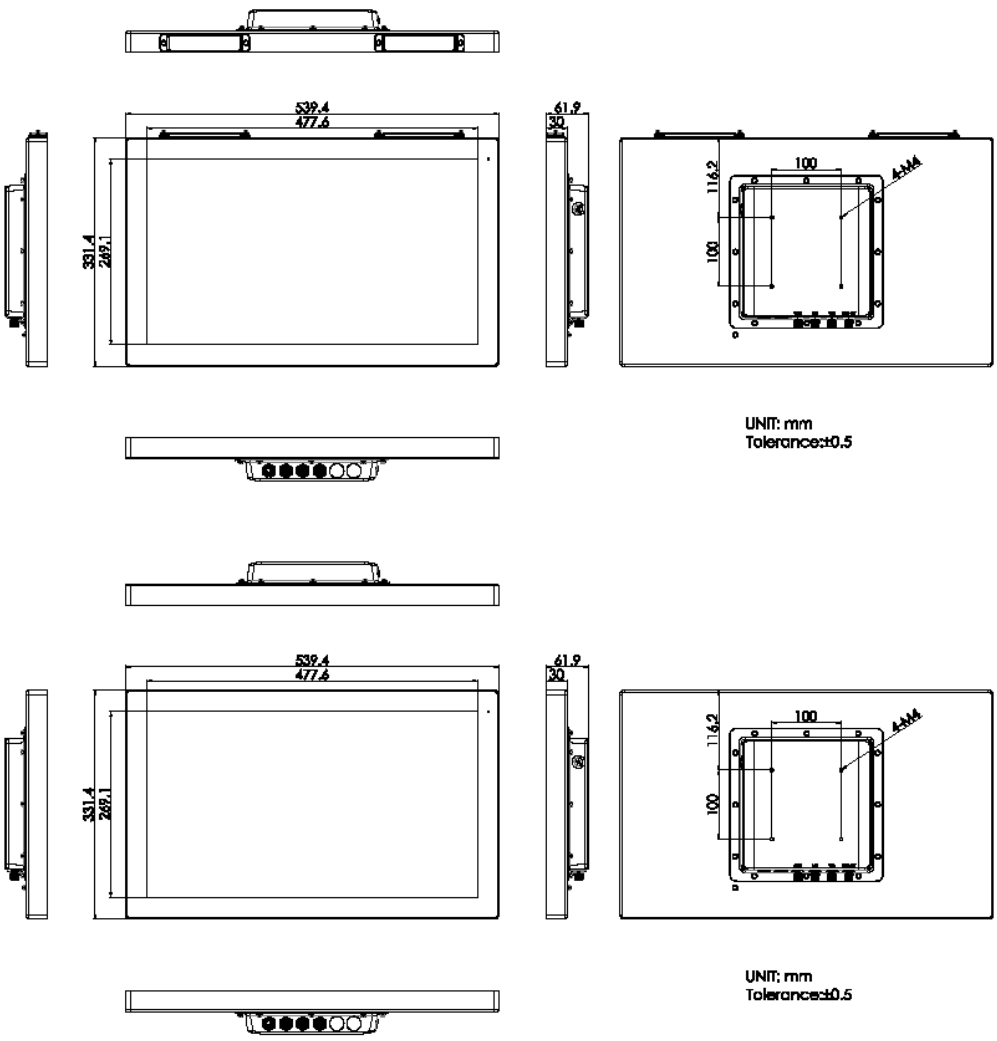


Figure 1.2: Dimensions of PHANTAM-921CP/R(H)

1.4 Brief Description of PhanTAM-9XXC Series

PhanTAM-9XXC series with MOTHERBOARD Aaeon GENE-TGU6 is an IP66/IP69K rated with M12 connectors new generation stainless steel panel pc, which comes with 15.6” and 21.5” color TFT LCD. PhanTAM-9XXC series are wide range DC 9~36V power input and true flat front bezel designed with grade 304 stainless steel enclosure (grade 316 is for option). Futhermore, the models support resistive touch, and projected capacitive touch for option, and can be high brightness LCD and optical bonding designed for option. It supports touch on/off button on the side edge for hygienic cleaning nad ergonomic versatile mounting: SWING ARM or space-saving VESA mounting.

Figure 1.3: Front View PhanTAM-9XXC

Figure 1.4: Rear View of PhanTAM-9XXC

Chapter 2 Hardware

2.1 Motherboard Introduction

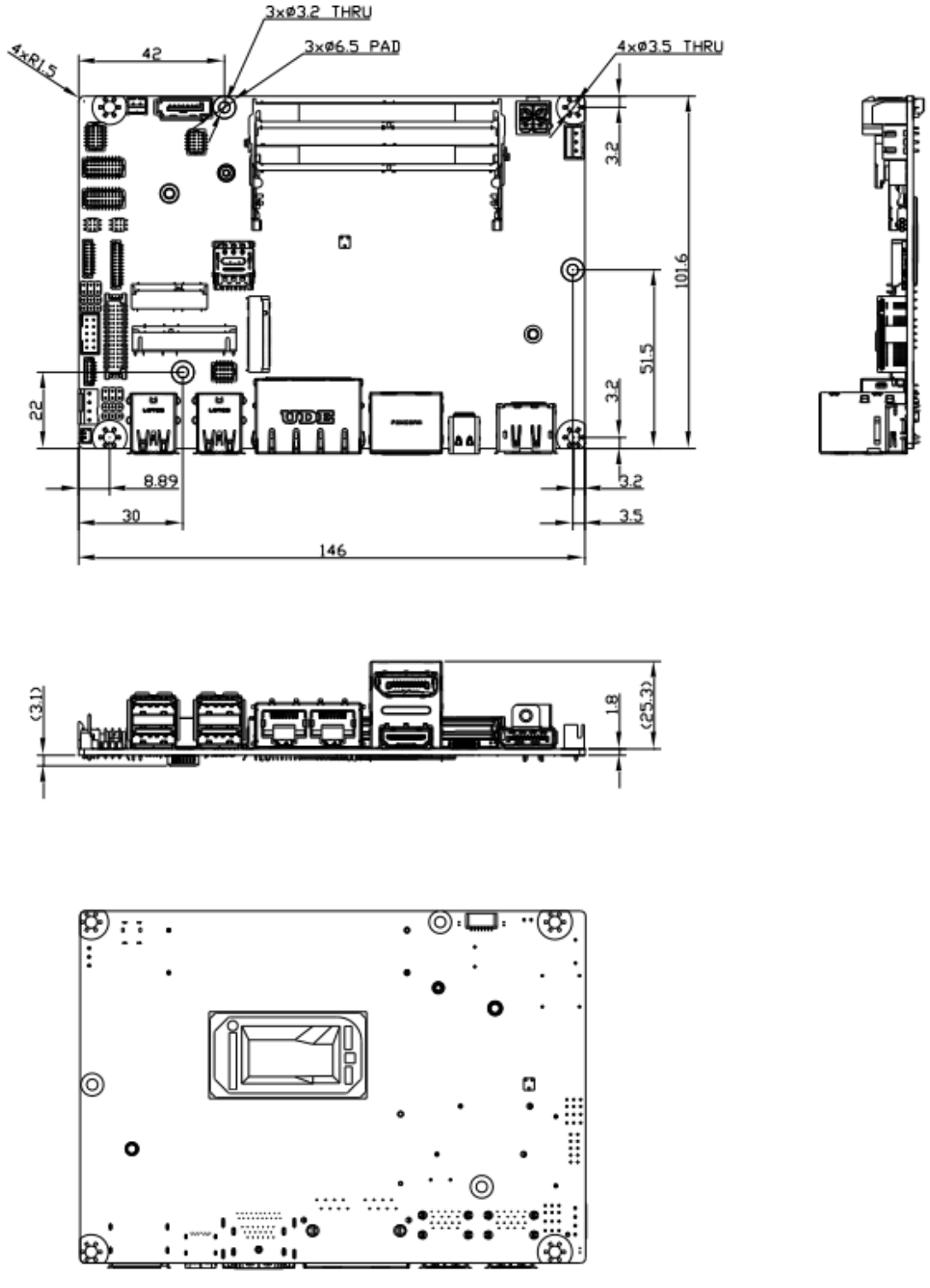
Standard 3.5" subcompact board developed on the basis of Intel 11th Generation Core™/Celeron Processor, which provides abundant peripheral interfaces to meet the needs of different customers. Also, it features one mPCIe/mSATA, dual GbE ports, 2-COM and 4 x USB3.2 Gen 2 Ports; one HDMI, one VGA and one LVDS interface.

2.2 Specifications & Dimensions

Specifications	
Board Size	146mm x 107.7mm
CPU Support	Intel® Core™ i3-1115G4E(2C/4T, 2.20GHz, up to 3.90GHz, 15W, up to 28W) Intel® Core™ i5-1145G7E(4C/8T, 1.50GHz, up to 4.10GHz, 15W, up to 28W) Intel® Core™ i7-1185G7E(4C/8T, 1.80GHz, up to 4.40GHz, 15W, up to 28W) Celeron® 6305E(2C/2T, 1.80GHz, 15W only)
Chipset	SOC
Memory Support	DDR4 up to 2400MHz, Dual Channel SODIMM x2, up to 64GB, IBECC
Graphics	Intel® UHD Graphics Intel® Iris® Xe Graphics
Display Mode	1 x HDMI 2.0b 1 x LVDS (18/24-bit dual LVDS) (optional: eDP1.4b) 2 x DP 1.4a 1 x DP 1.4 (Type C)
Multi Display	Up to 4 Simultaneous Displays
Wake on LAN	Yes
BIOS	UEFI
SATA	1 x SATAIII (6.0Gbps) 1 x +5V SATA Power Connector

Video	LVDS/ eDP x 1 (default: LVDS) eDP: up to 1080P@60Hz
USB	2 x USB 2.0
Serial	3 x RS232/RS422/RS485 port, (COM1, COM3, COM4) 1 x RS232/RS422/RS485 port, support 5V/12V/RI(COM2)
Digital I/O	8-bit digital I/O 4-bit digital Input 4-bit digital Output
Battery	Lithium Battery 3V/240mAh
SMBus/I2C	I2C/SMBus x 1 (Default: SMBus)
SIM	Nano-SIM x 1
Audio	Support Audio via Realtek ALC897/892 audio codec Audio Interface: Line-in/Line-out/MIC 1x Audio Header
Expansion Bus	1 x Full-size mPCIe/mSATA slot (mSATA as default, , select by BIOS) M.2 M-Key 2280 x 1 (PCIe [x4]) M.2 E-Key 2230 x 1 (PCIe, USB2.0)
FAN	Smart Fan x 1
Touch Ctrl	4/5/8-wire touch controller(option)
Power Management	Wide Range DC+9V~36V (+12V option) 1 x 2-pin Phoenix connector Power supply type: AT/ATX
Switches and LED Indicators	1 x Power on/off switch 1 x Reset 1 x HDD LED status 1 x Power LED status 1 x Buzzer
External I/O port	4 x USB 3.2 Gen 2 Ports 1 x USB 3.2 Gen 2 Type C (PD5V/3A) 2 x RJ45 GbE LAN Ports 1 x HDMI 2.0b 2 x DP 1.4a 1 x DP 1.4 (Type C)

Temperature	Operating: 0℃ to 60℃ Storage: -40℃ to 80℃
Humidity	0% - 90% relatively, non-condensing, operating
Power Consumption	Typical: 4.96A at +12V, Intel® i7-1185G7E, DDR4 3200MHz 32GB x 2 Maximum: 7.32A at +12V, Intel® i7-1185G7E, DDR4 3200MHz 32GB x 2
Watchdog Timer	255 Level
MTBF (Hrs)	329,884
EMI/EMS	CE/FCC class A



(Unit: mm)

Figure 2.1: Motherboard Dimensions

2.3 Jumpers and Connectors Location

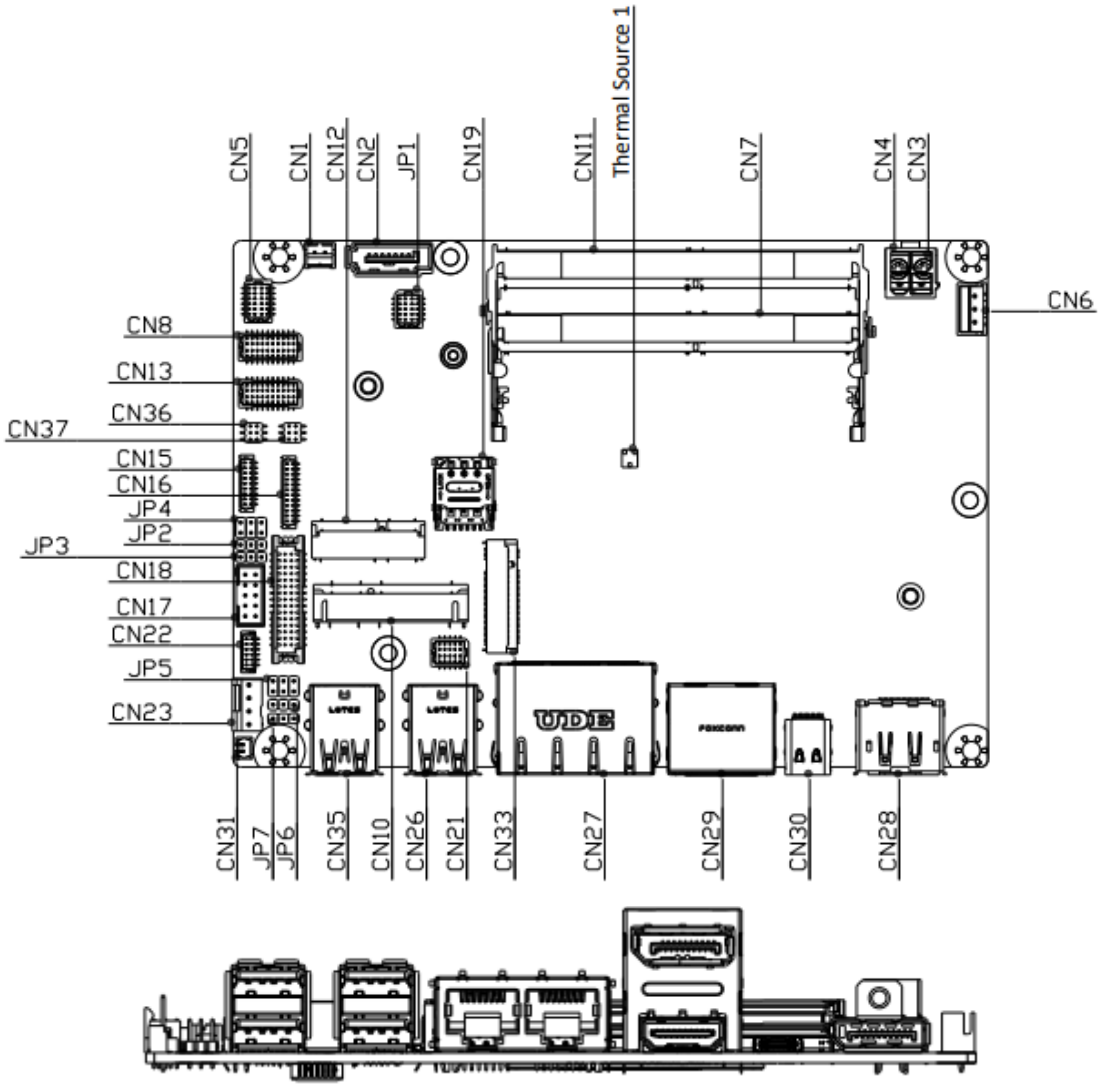


Figure 2.2: Jumpers and Connectors Location- Board Top

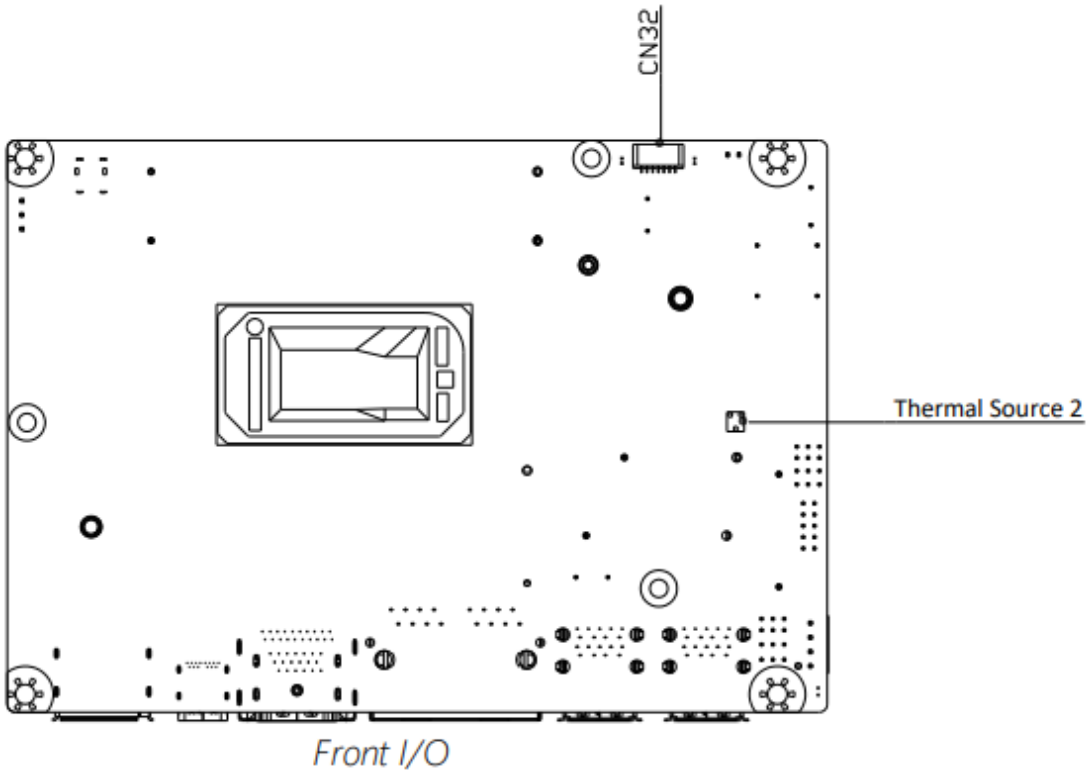


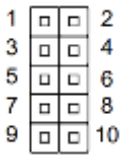
Figure 2.3: Jumpers and Connectors Location- Board Bottom

2.4 Jumpers Setting and Connectors

Please refer to the table below for all of the board's jumpers that you can configure for your application

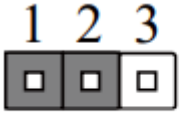
Label	Function
JP1	Front Panel Connector
JP2	Touch Screen 4/5/8-wire Mode Selection
JP3	Auto Power Button Enable/ Disable Selection
JP4	COM2 Pin 8 Function Selection
JP5	LVDS/eDP Port Backlight Inverter VCC Selection and Operating VDD Selection
JP6	LVDS/eDP Port Backlight Lightness Control Mode Selection
JP7	Clear CMOS Jumper

1. Front Panel Connector (JP1):

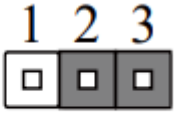


Pin	Function	Pin	Function
Pin 1	PWR_BTN-	Pin 2	PWR_BTN+
Pin 3	HDD_LED-	Pin 4	HDD_LED+
Pin 5	SPEAKER-	Pin 6	SPEAKER+
Pin 7	PWR_LED-	Pin 8	PWR_LED+
Pin 9	H/W RESET-	Pin 10	H/W RESET+

2. Touch Screen 4,5,8-Wire Selection (JP2):

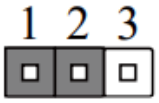


4/8-Wire Mode

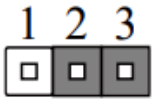


5-Wire Mode (**Default**)

3. Auto Power Button Enable/Disable Selection (JP3):

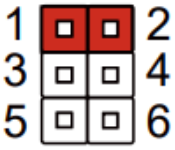


Disable/
ATX Power Mode

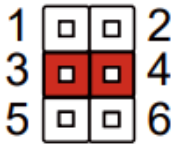


Enable/
AT Power Mode (**Default**)

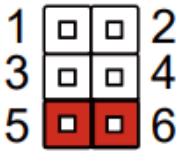
4. COM2 Pin8 Function Selection (JP4):



+12V

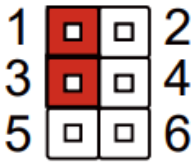
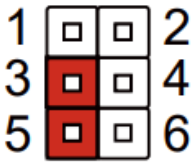
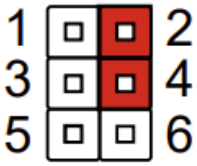
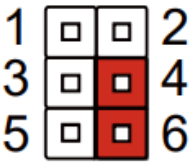


Ring (**Default**)



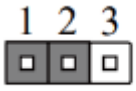
+5V

5. LVDS/eDP Port Backlight Inverter VCC and LVDS VDD Selection (JP5):

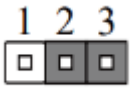
Backlight VCC Selection		LVDS VDD Selection	
			
+12V	+5V (**Default**)	+3.3V (**Default**)	+5V

Note: JP5 Default is two (2) jumpers placed on pins 3-5 and pins 2-4.

6. LVDS/eDP Port Backlight Lightness Control Mode (JP6):

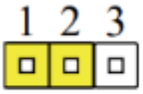


VR Mode

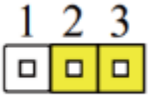


PWM Mode (**Default**)

7. Clear CMOS Jumper (JP9):



Normal (**Default**)



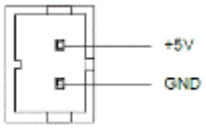
Clear CMOS

8. List of Connectors :

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN1	+5V Output for SATA HDD
CN2	SATA Port
CN3	External Power Input
CN5	Audio I/O Port
CN6	External +5VSB Input
CN7	DDR4 SO-DIMM Slot
CN8	COM Port 3, Port 4; RS232/422/485 Dual Port Header
CN10	Mini Card Slot (Full-Size)
CN11	DDR4 SO-DIMM Slot
CN12	M.2 E Key 2230
CN13	COM Port 1, Port 2; RS232/422/485 Dual Port Header
CN15	Touch Screen Connector (Optional)
CN16	eSPI Debug Port
CN17	Digital I/O Port
CN18	LVDS/eDP Port
CN19	Nano SIM Card Socket
CN21	USB2.0 Port 5, Port 6; Dual Port Header
CN22	LVDS/eDP Port Inverter/ Backlight Connector
CN23	CPU Fan
CN26	USB3.2 Gen 2 Port 1, Port 2, Dual Port Connector
CN27	LAN (RJ-45) Dual Port Connector; i225 (left), i219 (right)
CN28	DP Connector
CN29	DP and HDMI Connector
CN30	Type C Connector (USB3.2 Gen 2 Only)
CN31	Battery Connector
CN32	SPI BIOS Debug Port
CN33	M.2 M Key 2280
CN35	USB3.2 Gen 2 Port 3, Port 4, Dual Port Connector
CN36	i219 LED Connector
CN37	i225 LED Connector

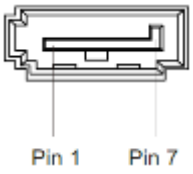
9. +5V Output for SATA HDD (CN1):



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V at 1A
2	GND	GND	

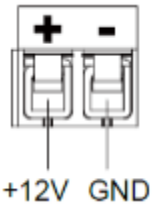
Note: Max current for Pin 1 is 1 Amp.

10. SATA Port (CN2):



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX	DIFF	
4	GND	GND	
5	SATA_RX	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

10. External Power Input (CN3):

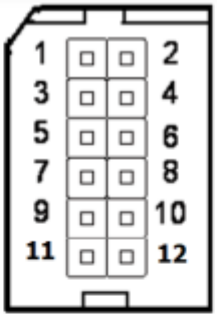


Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+9~+36V (or +12V) at 8A
2	GND	GND	

Note:

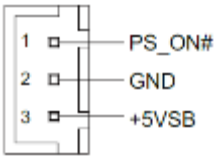
There are two types of power input, 9~36V or 12V (by BOM option).

11. Audio I/O Port (CN5)：



Pin	Pin Name	Signal Type
1	LOUT_R	OUT
2	MIC_R	IN
3	LOUT_L	OUT
4	MIC_L	IN
5	JD_LOUT	IN
6	JD_MIC	IN
7	AUD_GND	GND
8	AUD_GND	GND
9	JD_LIN	IN
10	LIN_R	IN
11	+VDD_AUD	PWR
12	LIN_L	IN

12. External +5VSB Input (CN6):

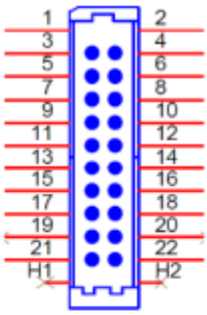


Pin	Pin Name	Signal Type	Signal Level
1	PS_ON#	OUT	+5V
2	GND	GND	
3	+5VSB	PWR	+5V at 2A

13. DDR SO-DIMM Slot (CN7):

Standard Specifications

14. COM Port3, Port 4 Dual Header (CN8):



RS-232

Pin	Pin	Pin Name	Signal Type	Signal Level
1	2	DCD	IN	
3	4	RX	IN	
5	6	TX	OUT	±5V
7	8	DTR	OUT	±5V
9	10	GND	GND	
11	12	DSR	IN	
13	14	RTS	OUT	±5V
15	16	CTS	IN	
17	18	RI	IN	
19	20	NC		

RS-485

Pin	Pin	Pin Name	Signal Type	Signal Level
1	2	RS485_D-	I/O	±5V
3	4	RS485_D+	I/O	±5V
5	6	NC		
7	8	NC		
9	10	GND	GND	
11	12	NC		
13	14	NC		
15	16	NC		
17	18	NC		
19	20	NC		

RS-422

Pin	Pin	Pin Name	Signal Type	Signal Level
1	2	RS422_TX-	OUT	+5V
3	4	RS422_TX+	OUT	±5V
5	6	RS422_RX+	IN	
7	8	RS422_RX-	IN	
9	10	GND	GND	
11	12	NC		
13	14	NC		
15	16	NC		
17	18	NC		
19	20	NC		

15. Mini Card Slot (Full-Size) (CN10):

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	UIM_PWR	PWR	
9	GND	GND	
10	UIM_DATA	I/O	
11	PCIE_REF_CLK-	DIFF	
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	
14	UIM_RST	IN	
15	GND	GND	
16	UIM_VPP	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V

25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

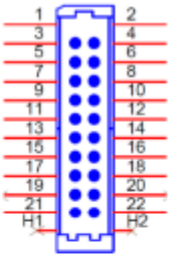
16. DDR SO-DIMM Slot (CN11):

Standard Specification

17. M.2 E-Key 2230 (CN12):

Standard Specification

18. COM Port1, Port 2 Dual Header (CN13):



RS-232

Pin	Pin	Pin Name	Signal Type	Signal Level
1	2	DCD	IN	
3	4	RX	IN	
5	6	TX	OUT	±5V
7	8	DTR	OUT	±5V
9	10	GND	GND	
11	12	DSR	IN	

Pin	Pin	Pin Name	Signal Type	Signal Level
13	14	RTS	OUT	±5V
15	16	CTS	IN	
17	18	RI/+5V/+12V	IN	
19	20	NC		

Note: RI/+5V/+12V for COM2 only.

RS-485

Pin	Pin	Pin Name	Signal Type	Signal Level
1	2	RS485_D-	I/O	±5V
3	4	RS485_D+	I/O	±5V
5	6	NC		
7	8	NC		
9	10	GND	GND	
11	12	NC		
13	14	NC		
15	16	NC		
17	18	NC		
19	20	NC		

RS-422

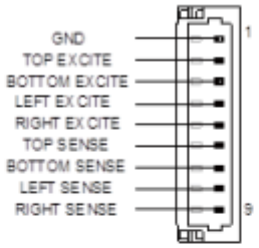
Pin	Pin	Pin Name	Signal Type	Signal Level
1	2	RS422_TX-	OUT	+5V
3	4	RS422_TX+	OUT	±5V
5	6	RS422_RX+	IN	
7	8	RS422_RX-	IN	
9	10	GND	GND	
11	12	NC		
13	14	NC		
15	16	NC		
17	18	NC		
19	20	NC		

Note 1: COM2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

Note 2: Pin 8 function can be set by JP4 (See Ch 2.3.4).

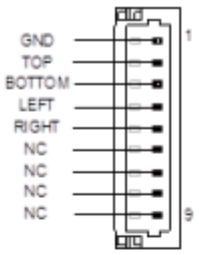
19. Touchscreen Connector (option) (CN15):

Note: Touch mode can be set by BIOS.



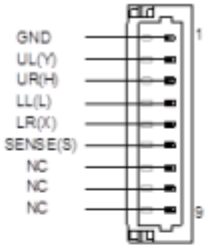
8-Wire Mode

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	TOP EXCITE	IN	
3	BOTTOM EXCITE	IN	
4	LEFT EXCITE	IN	
5	RIGHT EXCITE	IN	
6	TOP SENSE	IN	
7	BOTTOM SENSE	IN	
8	LEFT SENSE	IN	
9	RIGHT SENSE	IN	



4-Wire Mode

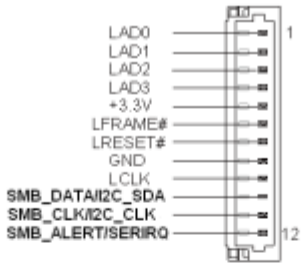
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	TOP	IN	
3	BOTTOM	IN	
4	LEFT	IN	
5	RIGHT	IN	
6	NC		
7	NC		
8	NC		
9	NC		



5-Wire Mode

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	UL(Y)	IN	
3	UR(H)	IN	
4	LL(L)	IN	
5	LR(X)	IN	
6	SENSE(S)	IN	
7	NC		
8	NC		
9	NC		

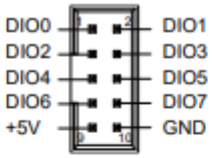
20. eSPI Debug Port (CN16):



Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	SMB_DATA/I2C_SDA	I/O	
11	SMB_CLK/I2C_CLK	OUT	
12	SMB_ALERT/SERIRQ	IN	+3.3V

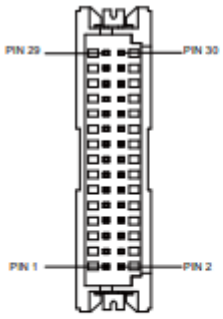
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V at 0.5A
2	USB5_D-	DIFF	
3	USB5_D+	DIFF	
4	GND	GND	
5	GND	GND	

21. Digital I/O Connector (CN17):



Pin	Signal Description	Pin	Signal Description
1	PD0	2	PD1
3	PD2	4	PD3
5	PD4	6	PD5
7	PD6	8	PD7
9	+V5S (0.5A)	10	GND

22. LVDS/eDP Port (CN18):



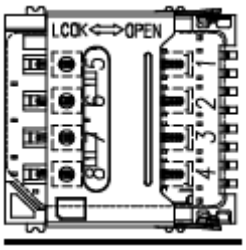
Note: LVDS LCD_PWR can be set to +3.3V or +5V by JP5. (See Ch 2.3.5)

Note: LVDS LCD_PWR supports current of 2A

Pin	LVDS	eDP	Signal Type	Signal Level
1	BKL_ENABLE	BKL_ENABLE	OUT	
2	BKL_CONTROL	BKL_CONTROL	OUT	
3	LCD_PWR	LCD_PWR	PWR	+3.3V/+5V
4	GND	GND	GND	
5	LVDS_A_CLK-	eDP_TXN3	DIFF	
6	LVDS_A_CLK+	eDP_TXP3	DIFF	
7	LCD_PWR	LCD_PWR	PWR	+3.3V/+5V
8	GND	GND	GND	
9	LVDS_DA0-	eDP_TXN2	DIFF	
10	LVDS_DA0+	eDP_TXP2	DIFF	
11	LVDS_DA1-	eDP_TXN1	DIFF	
12	LVDS_DA1+	eDP_TXP1	DIFF	
13	LVDS_DA2-	eDP_TXN0	DIFF	
14	LVDS_DA2+	eDP_TXP0	DIFF	
15	LVDS_DA3-	NC	DIFF	
16	LVDS_DA3+	eDP_HPD	DIFF	
17	DDC_DATA	eDP_AUX_N	I/O	+3.3V
18	DDC_CLK	eDP_AUX_P	I/O	+3.3V
19	LVDS_DB0-	NC	DIFF	
20	LVDS_DB0+	NC	DIFF	
21	LVDS_DB1-	NC	DIFF	
22	LVDS_DB1+	NC	DIFF	
23	LVDS_DB2-	NC	DIFF	
24	LVDS_DB2+	NC	DIFF	
25	LVDS_DB3-	NC	DIFF	
26	LVDS_DB3+	NC	DIFF	

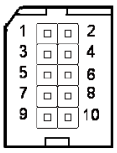
27	LCD_PWR	LCD_PWR	PWR	+3.3V/+5V
28	GND	GND	GND	
29	LVDS_B_CLK-	NC	DIFF	
30	LVDS_B_CLK+	NC	DIFF	

23. Nano SIM Card Socket (CN19):



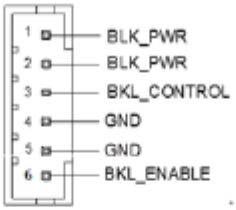
Pin	Pin Name	Signal Type	Signal Level
1	UIM_PWR	PWR	
2	UIM_RST	IN	
3	UIM_CLK	IN	
4	NC		
5	GND	GND	
6	UIM_VPP	PWR	
7	UIM_DATA	I/O	
8	NC		

24. USB 2.0 Port 5, Port6 Dual Header (CN21):



USB Port 5		USB Port 6	
Pin	Pin Name	Pin	Pin Name
1	+5VSB (0.5A)	2	+5VSB (0.5A)
3	USB5_D-	4	USB6_D-
5	USB5_D+	6	USB6_D+
7	GND	8	GND
9	GND	10	GND

25. LVDS/eDP Port Inverter/Backlight Connector (CN22):



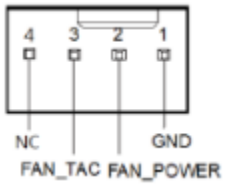
Pin	Pin Name	Signal Type	Signal level
1	BKL_PWR	PWR	+5V / +12V
2	BKL_PWR	PWR	+5V / +12V
3	BKL_CONTROL	OUT	
4	GND	GND	
5	GND	GND	
6	BKL_ENABLE	OUT	+3.3V

Note 1: LVDS BKL_PWR can be set to +5V or +12V by JP5. (See Ch 2.3.5)

Note 2: LVDS BKL_PWR supports current of 1.5A

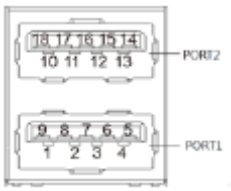
Note 3: LVDS BKL_CONTROL can be set by JP6. (See Ch 2.3.6)

26. CPU Fan (CN23):



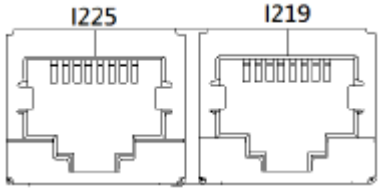
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	FAN_POWER	PWR	+12V at 1A
3	FAN_TAC	IN	
4	NC		

27. USB 3.2 Gen 2 Ports 1&2 Dual Connector (CN26):



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V at 0.9A
2	USB0_D-	DIFF	
3	USB0_D+	DIFF	
4	GND	GND	
5	USB0_SSRX–	DIFF	
6	USB0_SSRX+	DIFF	
7	GND	GND	
8	USB0_SSTX–	DIFF	
9	USB0_SSTX+	DIFF	
10	+5VSB	PWR	+5V at 0.9A
11	USB1_D-	DIFF	
12	USB1_D+	DIFF	
13	GND	GND	
14	USB1_SSRX–	DIFF	
15	USB1_SSRX+	DIFF	
16	GND	GND	
17	USB1_SSTX–	DIFF	
18	USB1_SSTX+	DIFF	

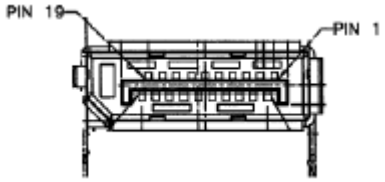
28. LAN (RJ-45) Dual Port i225 and i219 (CN27):



i225		i219	
Pin	Pin Name	Pin	Pin Name
1P1	LAN2_MDI0_P	2P1	LAN1_MDI0_P
1P2	LAN2_MDI0_N	2P2	LAN1_MDI0_N
1P3	LAN2_MDI1_P	2P3	LAN1_MDI1_P
1P4	LAN2_MDI1_N	2P4	LAN1_MDI1_N
1P7	LAN2_MDI2_P	2P7	LAN1_MDI2_P

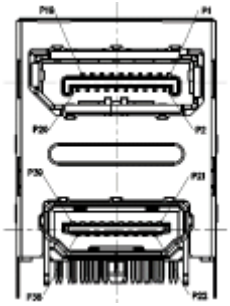
1P8	LAN2_MDI2_N	2P8	LAN1_MDI2_N
1P9	LAN2_MDI3_P	2P9	LAN1_MDI3_P
1P10	LAN2_MDI3_N	2P10	LAN1_MDI3_N

29. DP Connector (CN28):



Pin	Pin Name	Signal Type	Signal Level
1	DP1_TX0_DP	DIFF	
2	GND	GND	
3	DP1_TX0_DN	DIFF	
4	DP1_TX1_DP	DIFF	
5	GND	GND	
6	DP1_TX1_DN	DIFF	
7	DP1_TX2_DP	DIFF	
8	GND	GND	
9	DP1_TX2_DN	DIFF	
10	DP1_TX3_DP	DIFF	
11	GND	GND	
12	DP1_TX3_DN	DIFF	
13	GND	GND	
14	GND	GND	
15	DP1_AUX_DP	I/O	
16	GND	GND	
17	DP1_AUX_DN	I/O	
18	DP1_HPD	I/O	
19	GND	GND	
20	+V3P3S	PWR	+3.3V

30. DP + HDMI Connector (CN29):

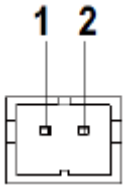


Pin	Pin Name	Signal Type	Signal Level
		DP Port	
1	DP2_TX0_DP	DIFF	
2	GND	GND	
3	DP2_TX0_DN	DIFF	
4	DP2_TX1_DP	DIFF	
5	GND	GND	
6	DP2_TX1_DN	DIFF	
7	DP2_TX2_DP	DIFF	

8	GND	GND	
9	DP2_TX2_DN	DIFF	
10	DP2_TX3_DP	DIFF	
11	GND	GND	
12	DP2_TX3_DN	DIFF	
13	GND	GND	
14	GND	GND	
15	DP2_AUX_DP	I/O	
16	GND	GND	
17	DP2_AUX_DN	I/O	
18	DP2_HPD	I/O	
19	GND	GND	
20	+V3P3S	PWR	+3.3V
		HDMI Port	
21	HDMI_TX2+	DIFF	
22	GND	GND	
23	HDMI_TX2-	DIFF	
24	HDMI_TX1+	DIFF	
25	GND	GND	
26	HDMI_TX1-	DIFF	
27	HDMI_TX0+	DIFF	
28	GND	GND	
29	HDMI_TX0-	DIFF	
30	HDMI_CLK+	DIFF	
31	GND	GND	
32	HDMI_CLK-	DIFF	

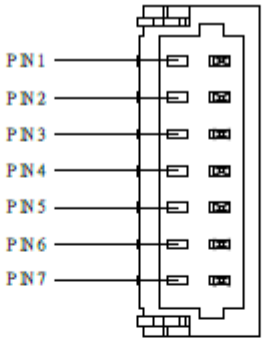
33	NC		
34	NC		
35	DDC_CLK	I/O	+5V
36	DDC_DATA	I/O	+5V
37	GND	GND	
38	+5V	PWR	+5V
39	HDMI_HPD		

31. Battery Connector (CN31):



Pin	Pin Name	Signal Type	Signal Level
1	+3.3V	PWR	3.3V
2	GND	GND	

32. SPI BIOS Debug Port (CN32):

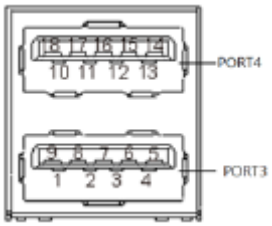


Pin	Pin Name	Signal Type	Signal Level
1	SPI_MISO	OUT	
2	GND	GND	
3	SPI_CLK	IN	
4	+3.3VSB	PWR	+3.3V
5	SPI_MOSI	IN	
6	SPI_CS	IN	
7	NC		

33. M.2 M-Key 2280 slot (CN33):

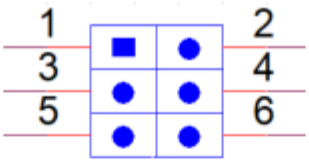
Standard Specification

34. USB 3.2 Gen 2 Ports 3&4 Dual Connector (CN35):



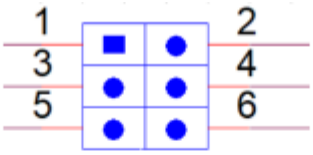
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V at 0.9A
2	USB2_D-	DIFF	
3	USB2_D+	DIFF	
4	GND	GND	
5	USB2_SSRX–	DIFF	
6	USB2_SSRX+	DIFF	
7	GND	GND	
8	USB2_SSTX–	DIFF	
9	USB2_SSTX+	DIFF	
10	+5VSB	PWR	+5V at 0.9A
11	USB3_D-	DIFF	
12	USB3_D+	DIFF	
13	GND	GND	
14	USB3_SSRX–	DIFF	
15	USB3_SSRX+	DIFF	
16	GND	GND	
17	USB3_SSTX–	DIFF	
18	USB3_SSTX+	DIFF	

35. i219 LED Connector (CN36):



Pin	Pin Name	Signal Type	Signal Level
1	LINK_ACT#	IO	
2	+V3P3A	PWR	+3.3V
3	LAN_1000#	IO	
4	LAN_100#	IO	
5	LAN_100#	IO	
6	LAN_1000#	IO	

36. i225 LED Connector (CN37):



Pin	Pin Name	Signal Type	Signal Level
1	LINK_ACT#	IO	
2	+V3P3A	PWR	+3.3V
3	LAN_2500#	IO	
4	LAN_1000#	IO	
5	LAN_1000#	IO	
6	LAN_2500#	IO	

Chapter 3 BIOS Setup

3.1 System Test and Initialization

The GENE-TGU6 board uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the module will output a few short beeps or display an error message. The module can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or an error is detected, the module will load the default configuration and reboot automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration was reset by the Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The system CMOS memory has an integral lithium battery backup for data retention. You will need to replace the battery unit when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <ESC> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Access advanced hardware settings and Hardware Monitor

Chipset – Chipset settings and options

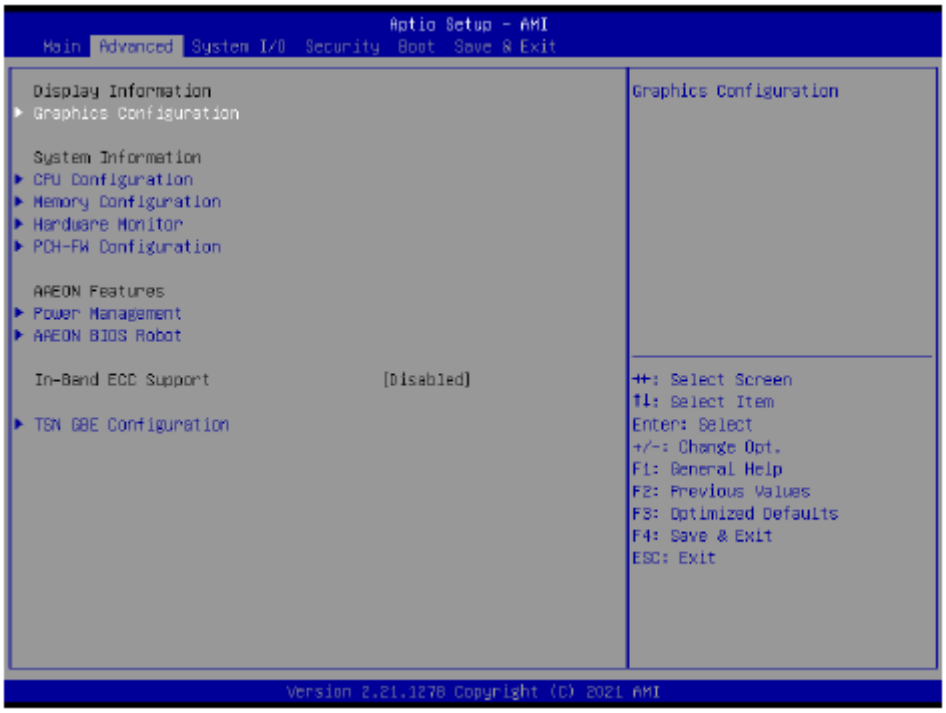
Security – Set admin and user passwords, access secure boot options

Boot – Boot options including BBS priority and Quiet Boot options

Save & Exit – Save your changes and exit the program

3.3 Setup Submenu:Main

3.4 Setup Submenu: Advanced

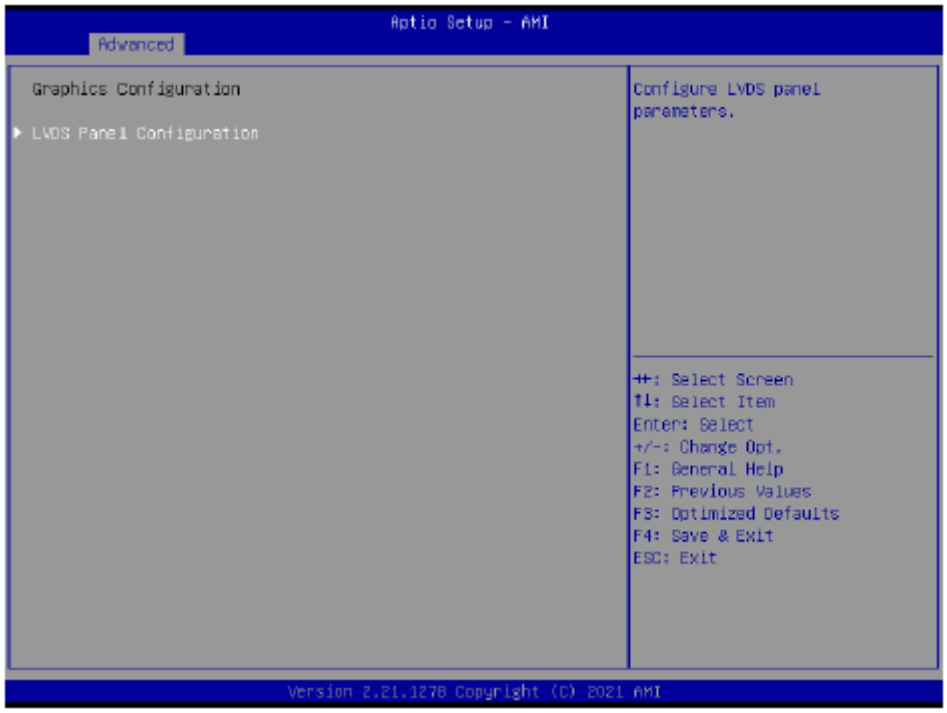


Options Summary		
In-Band ECC Support	Disabled	
	Enabled	Optimal Default; Failsafe Default
Enable/Disabled In-Band ECC Support		
In-Band ECC Error Injection	Enabled	
	Disabled	Optimal Default, Failsafe Default
By enabling this Error Injection feature, the user acknowledges the security risks. Enabling Error Injection allows attackers who have access to the Host Operating System to inject IBECC errors that can cause unintended memory corruption and enable the leak of security data in the BIOS stolen memory regions.		
In-Band ECC Operation Mode	0	
	1	
	2	Optimal Default, Failsafe Default
0: Functional Mode protects requests based on the address range, 1: Makes all requests non-protected and ignore range checks, 2: Makes all requests protected and ignore range checks		

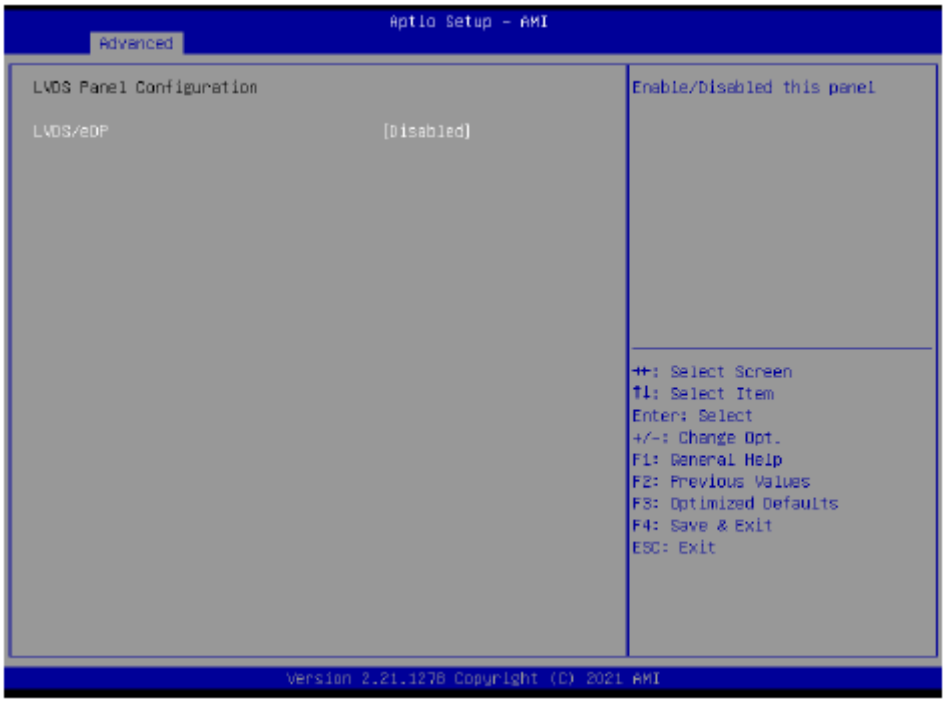
Options Summary		
IBECC Protect Region 0-7	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disabled In-Band ECC for Region 0-7		

Note: In-Band ECC Support availability depends on CPU.

3.4.1 Graphics Configuration



3.4.1.1 LVDS Panel Configuration



Options Summary		
LVDS/eDP	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disabled this panel.		
LVDS Panel Type	640X480@60HZ	
	800X480@60HZ	
	800X600@60HZ	
	1024X600@60HZ	
	1024X768@60HZ	Optimal Default, Failsafe Default
	1280X768@60HZ	
	1280X800@60HZ	
	1280X1024@60HZ	
	1366X768@60HZ	
	1440X900@60HZ	
	1600X1200@60HZ	
	1920X1080@60HZ	
	1920X1200@60HZ	

Options Summary		
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		
Color Depth	18-bit	Optimal Default, Failsafe Default
	24-bit	
	36-bit	
	48-bit	
Select panel type		
Backlight Mode	BIOS & Application	
	Windows Slider	Optimal Default, Failsafe Default
Select backlight control signal type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	Optimal Default, Failsafe Default
	90%	
	100%	
Select backlight control level		
Backlight PWM Freq	100Hz	
	200Hz	
	220Hz	Optimal Default, Failsafe Default
	500Hz	
	1.1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal		
Swing Level	150mV	
	200mV	
	250mV	
	300mV	Optimal Default, Failsafe Default
	350mV	
	400mV	

Options Summary		
Swing Level	450mV	
Select Swing Level		
Center Spreading Depth	no spreading	Optimal Default, Failsafe Default
	0.5%	
	1.0%	
	1.5%	
	2.0%	
	2.5%	
Select Center Spreading Depth		

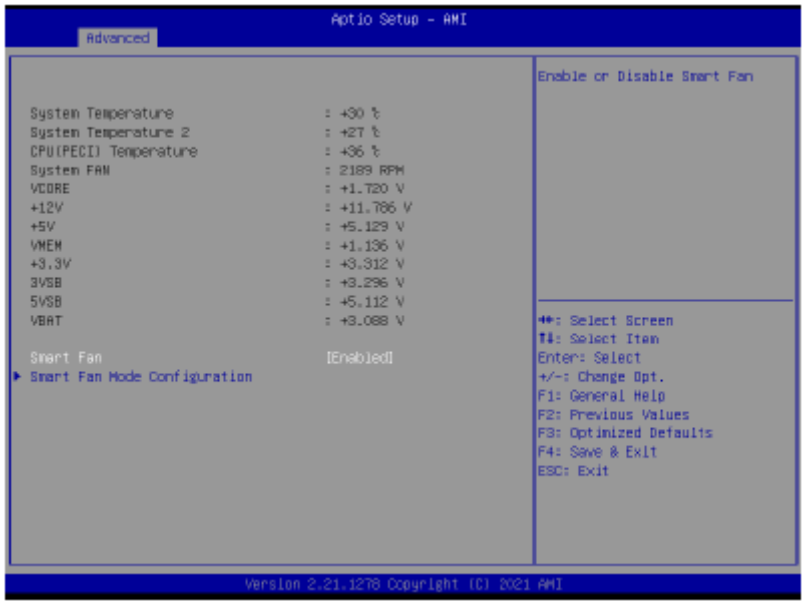
Options Summary		
Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable Platform Hierarchy		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2: Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		

3.4.2 CPU Configuration

Options Summary		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
Intel(R) SpeedStep(tm)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Allows more than two frequency ranges to be supported.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.		

3.4.3 Memory Configuration

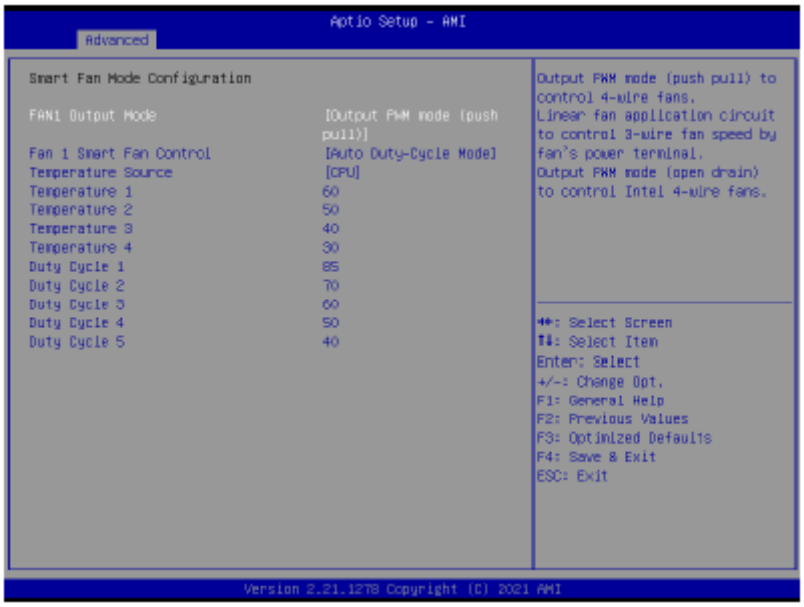
3.4.4 Hardware Monitor



Options Summary		
Smart Fan	Disabled	
	Enabled	Optimal Default; Failsafe Default
Enable or Disable Smart Fan		

3.4.4.1 Smart Fan Mode Configuration

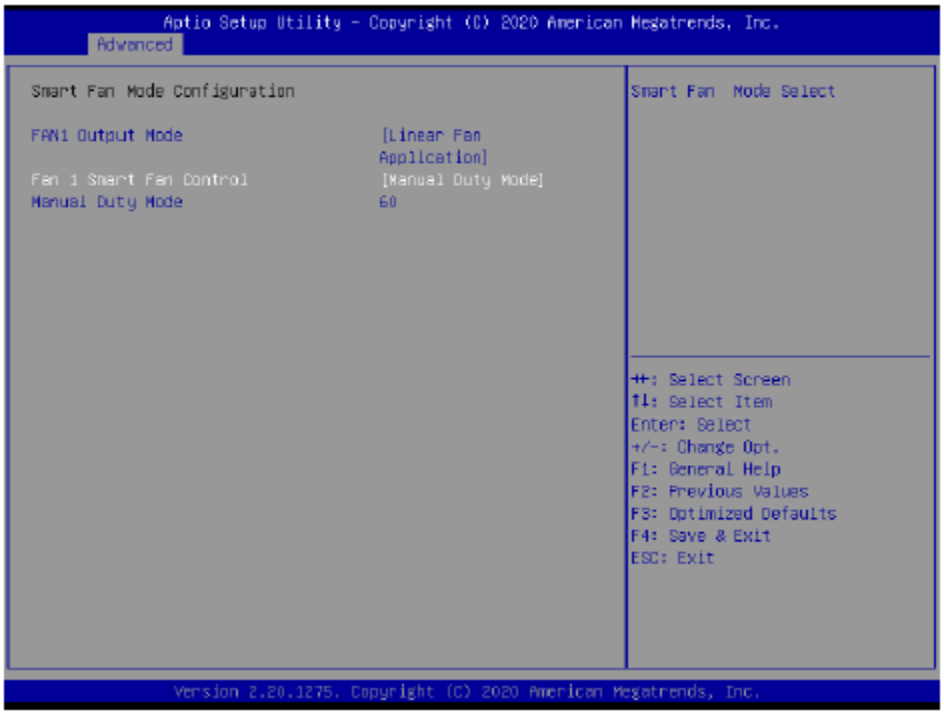
Auto Duty Cycle Mode



Options Summary		
FAN1 Output Mode	Output PWM mode (push pull)	
	Linear Fan Application	
	Output PWM mode (open drain)	Optimal Default, Failsafe Default
Output PWM mode (push pull) to control 4-wire fans.\nLinear fan application circuit to control 3-wire fan speed by fan's power terminal.\nOutput PWM mode (open drain) to control Intel 4-wire fans.		
Fan 1 Smart Fan Control	Manual Duty Mode	
	Auto Duty-Cycle Mode	Optimal Default, Failsafe Default
Smart Fan Mode Select		
Temperature Source	CPU	Optimal Default, Failsafe Default
	System Temperature 2	
	System Temperature	
Select the monitored temperature source for this fan.		

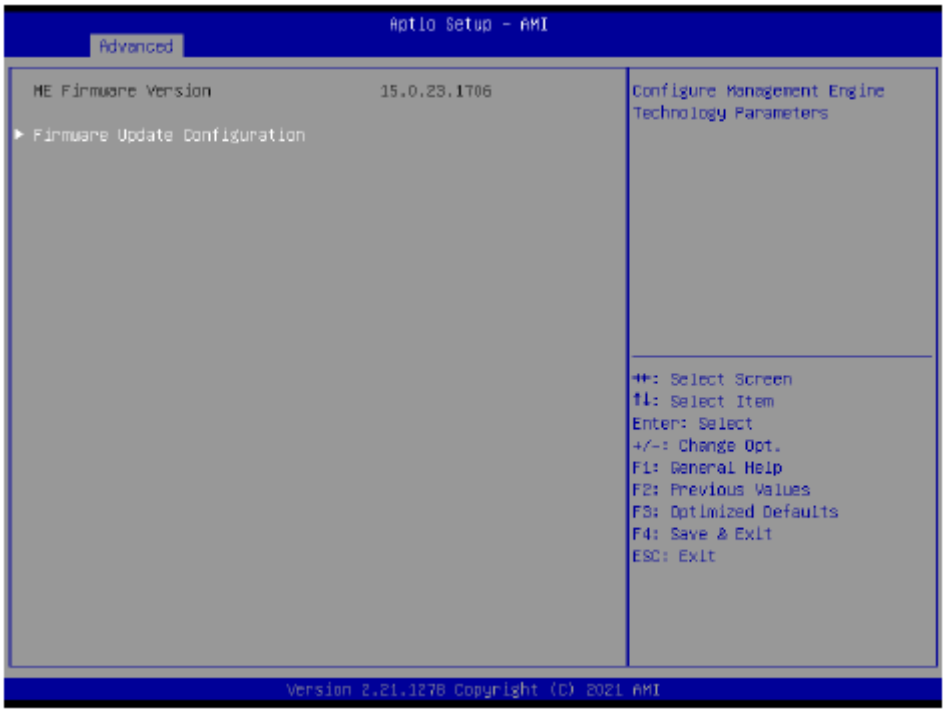
Options Summary	
Duty Cycle	Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100
Temperature	

Manual Duty Mode

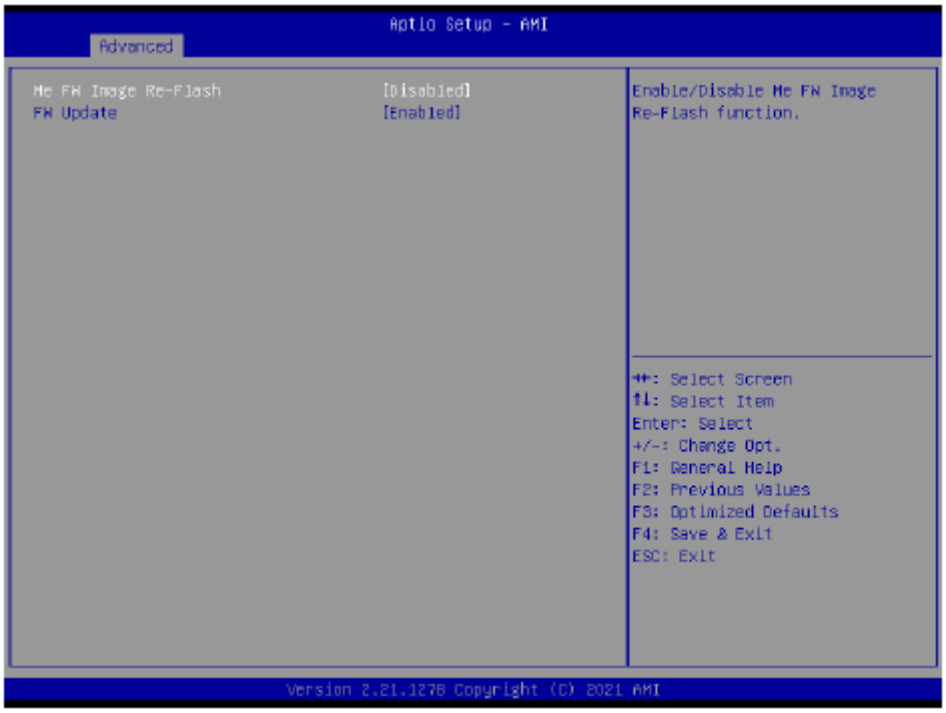


Options Summary		
Manual Duty Mode	60	Optimal Default, Failsafe Default
Manual mode fan control, user can write expected duty cycle (PWM fan type) 1-100		

3.4.5 PCH-FW Configuration



3.4.5.1 Firmware Update Configuration

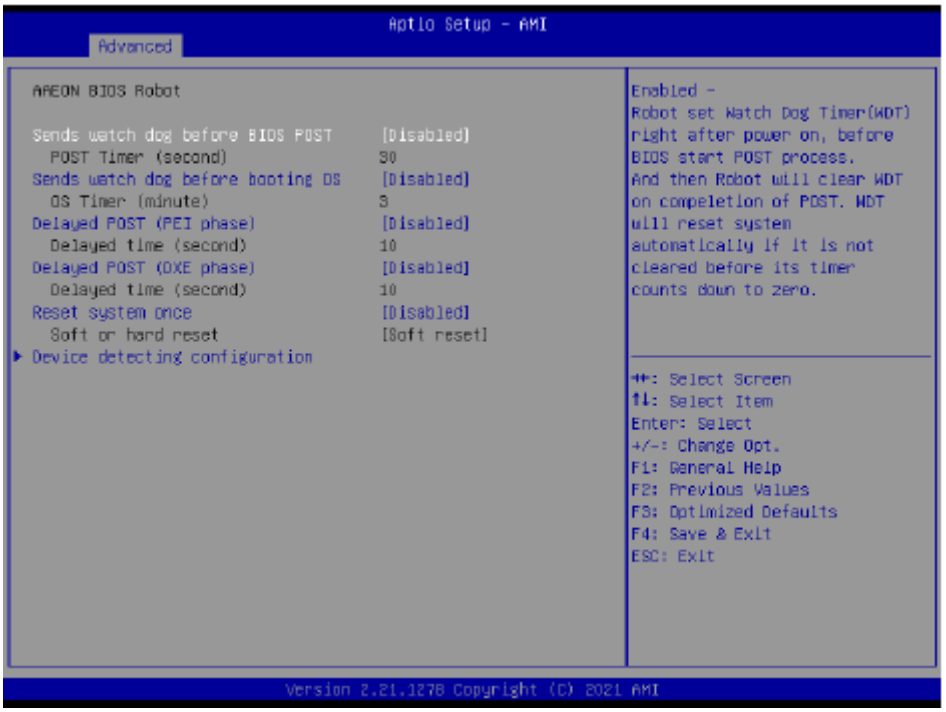


Options Summary		
Me FW Image Re-Flash	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Me FW Image Re-Flash function.		
FW Update	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable ME FW Update function.		

3.4.6 Power Management

Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
IO Restore AC power Loss		
RTC wake system from S5	Disable	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
	Bypass	
Fixed Time: System will wake on the hr::min::sec specified./n Dynamic Time: System will wake on the current time + Increase minute(s)./n Bypass: BIOS will not control RTC wake function during system shutdown		

3.4.7 BIOS Robot



Options Summary		
Sends watch dog before BIOS POST	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot set Watch Dog Time r(WDT) right after power on, before BIOS start POST process. Robot will clear WDT on completion of POST. WDT will reset system automatically if it is not cleared before its timer counts down to zero.		
POST Timer (second)	30	Optimal Default, Failsafe Default
Timer count set to Watch Dog Timer for POST. **WARNING**: Do not set to a value equal to or shorter than normal POST time, otherwise system may never complete POST unless clearing BIOS settings. More than twice the normal POST time is suggested.		
Sends watch dog before booting OS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot set Watch Dog Timer (WDT) after POST completion, before BIOS transfers control to OS. **WARNING**: Before enabling this function, a program in OS must be responsible for clearing WDT. Also, this function should be disabled if OS is going to update itself.		

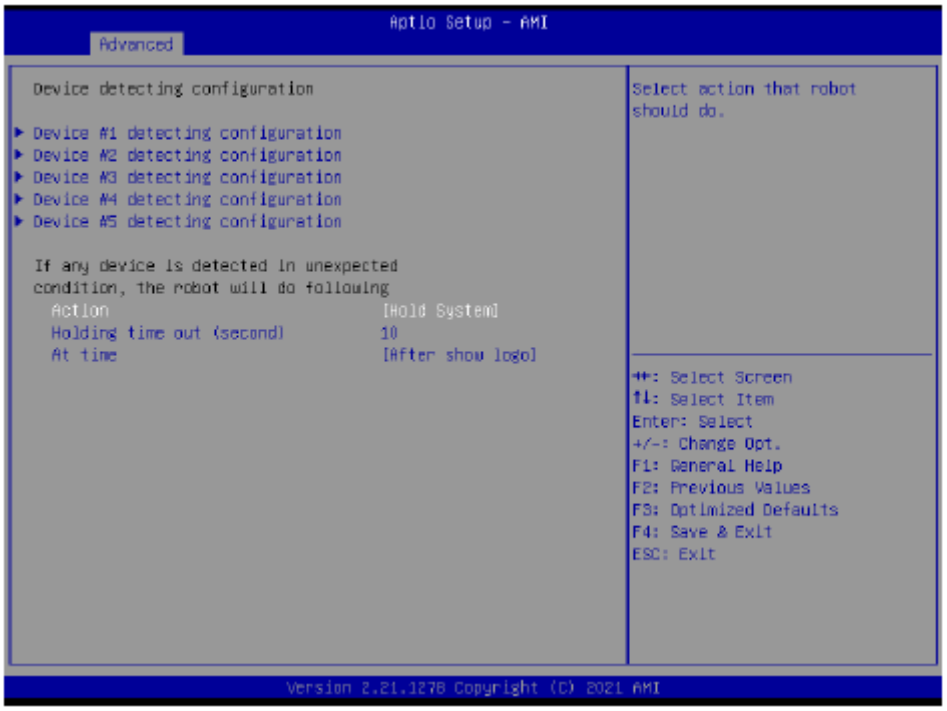
Options Summary		
OS Timer (minute)	3	Optimal Default, Failsafe Default
Timer count set to Watch Dog Timer for OS loading.		
Delayed POST (PEI phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot holds BIOS from starting POST, right after power on. This allows BIOS POST to start with stable power or start after system is physically warmed-up. **Note**: Robot does this before 'Sends watch dog'.		
Delayed time (second)	10	Optimal Default, Failsafe Default
Period of time for Robot to hold BIOS from POST.		
Delayed POST (DXE phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot holds BIOS before POST completion. This allows BIOS POST to start with stable power or start after system is physically warmed-up. **Note**: Robot does this after 'Sends watch dog before BIOS POST'.		
Delayed time (second)	10	Optimal Default, Failsafe Default
Period of time for Robot to hold BIOS from POST.		
Reset system once	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot resets system for one time on each boot. This will send a soft or hard reset to onboard devices, thus puts devices to more stable state.		
Soft or hard reset	Soft reset	Optimal Default, Failsafe Default
	Hard reset	
Select reset type robot should send on each boot.		

3.4.7.1 Device Detecting Configuration

Action: Rest System

Options Summary		
Action	Reset System	Optimal Default, Failsafe Default
	Hold System	
Select action that robot should do.		
Soft or hard reset	Soft	Optimal Default, Failsafe Default
	Hard	
Select reset type robot should send on each boot.		
Retry-Count	3	Optimal Default, Failsafe Default
Fill retry counter here. Robot will reset system at most counter times, and then let system continue its POST.		
At time	After show logo	Optimal Default, Failsafe Default
	Before show logo	
Select robot action time: After show logo – Robot will do action after logo is displayed. System devices are almost ready. Before show logo – Robot will do action earlier before logo, but some devices may not be ready.		

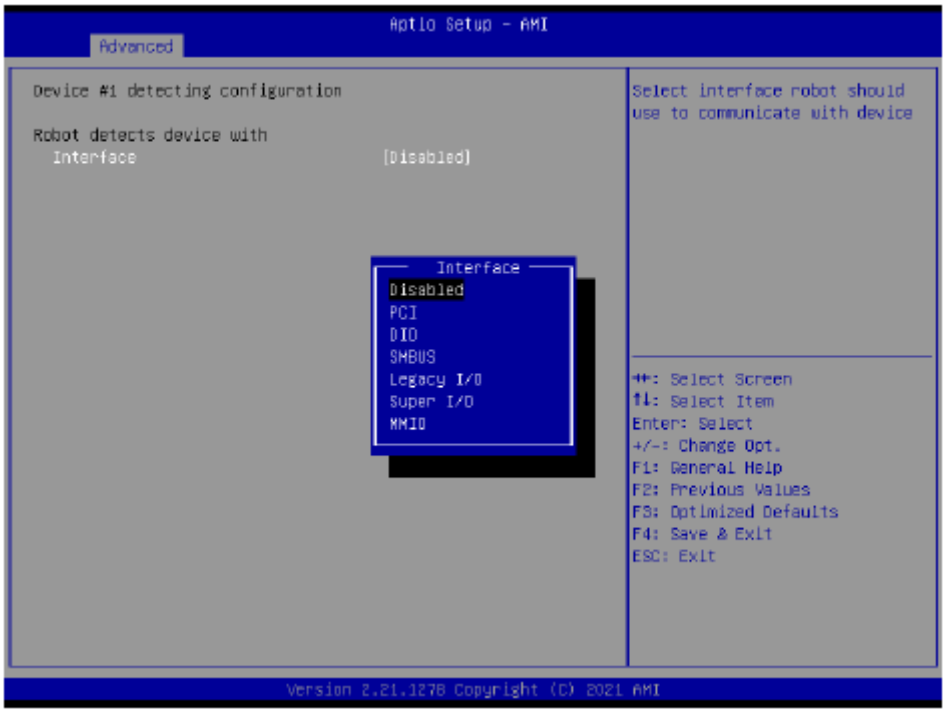
Action: Hold System



Options Summary		
Action	Reset System	Optimal Default, Failsafe Default
	Hold System	
Select action that robot should do.		
Holding time out (second)	10	Optimal Default, Failsafe Default
Fill hold time out here. Robot will hold system no longer then time-out value, and then let system continue its POST.		
At time	After show logo	Optimal Default, Failsafe Default
	Before show logo	
Select robot action time: After show logo - Robot will do actoin after logo is displayed. System devices are almost ready. Before show logo - Robot will do action earlier before logo, but some devices may not be ready.		

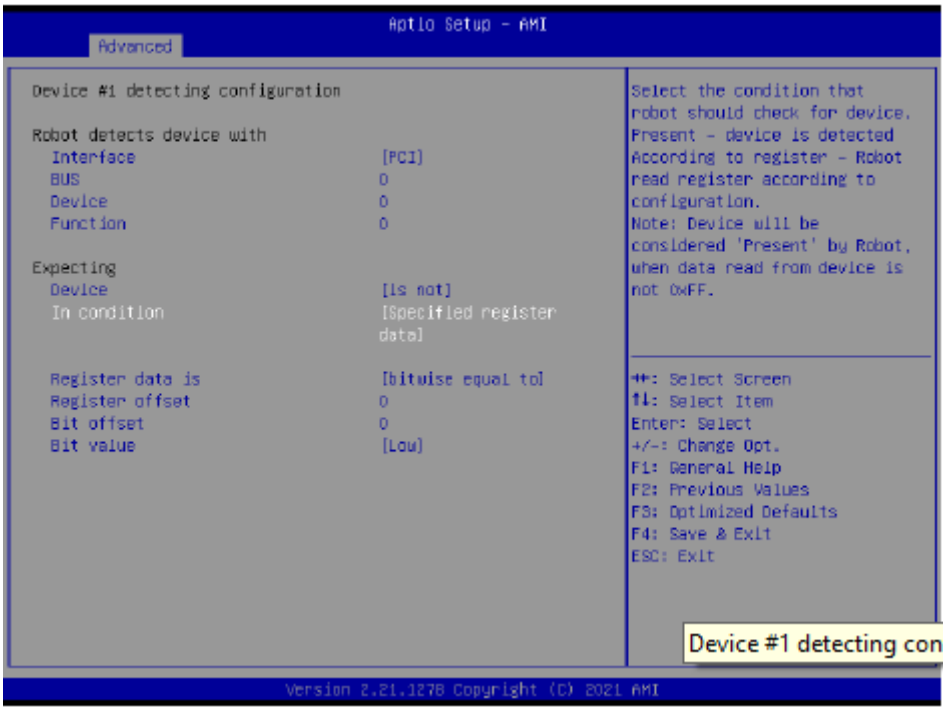
3.4.7.1.1 Device# Detecting Configuration

Interface: Disabled



Options Summary		
Interface	Disabled	Optimal Default, Failsafe Default
	PCI	
	DIO	
	SMBUS	
	Legacy I/O	
	Super I/O	
	MMIO	
Select interface robot should use to communicate with device.		

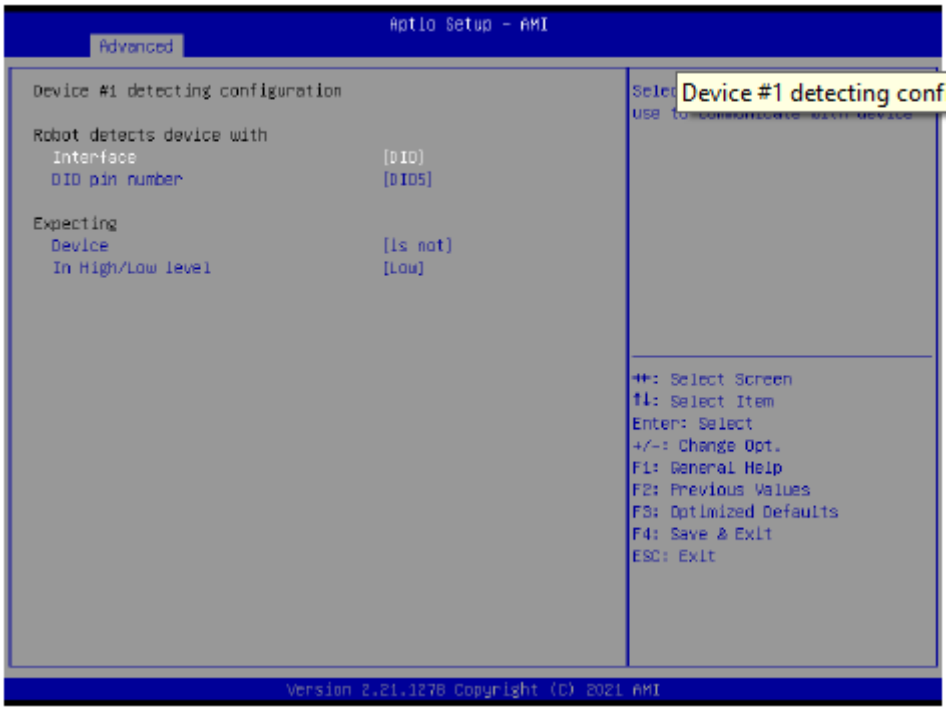
Interface: PCI



Options Summary		
BUS	0	Optimal Default, Failsafe Default
Fill BUS number to a PCI device, in hexadecimal. Range: 0 - FF		
Device	0	Optimal Default, Failsafe Default
Fill DEVICE number to a PCI device, in hexadecimal. Range: 0 - FF		
Function	0	Optimal Default, Failsafe Default
Fill FUNCTION number to a PCI device, in hexadecimal. Range: 0 - FF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		

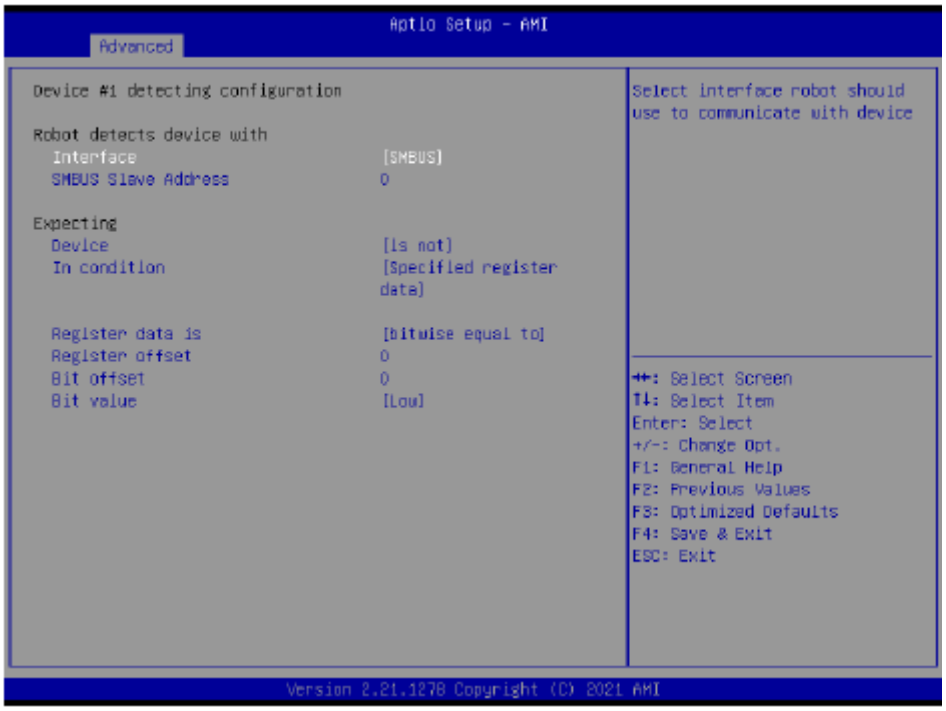
Options Summary		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		
Register offset	0	Optimal Default, Failsafe Default
Fill register offset (or index) for robot to read, in hexadecimal. Range: 0 - FF		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

Interface: DIO



Options Summary		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
DIO pin number	DIO1	Optimal Default, Failsafe Default
	DIO*	
Fill DIO pin number. 0 - DIO0, 1 - DIO1, and so on. For COM express product: 0-3 - GPI0-3, 4-7 - GPO0-3		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In High/Low level	Low	Optimal Default, Failsafe Default
	High	
Select High/Low level of the DIO pin that robot should do action.		

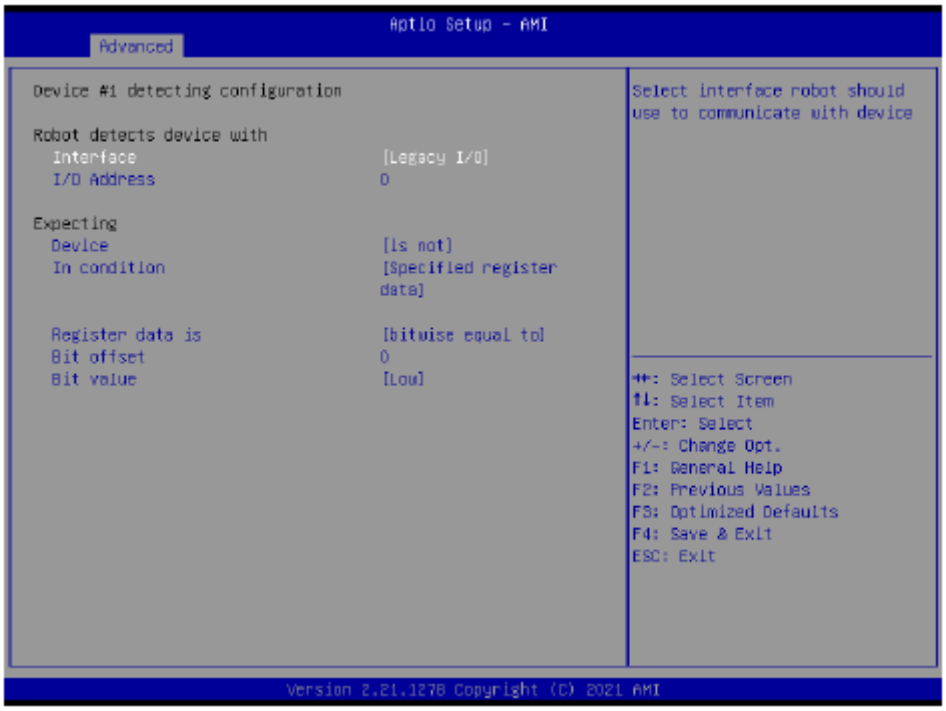
Interface: SMBUS



Options Summary		
SMBUS Slave Address	0	Optimal Default, Failsafe Default
Fill slave address to a SMBUS device, in hexadecimal. Range: 0 - FF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		

Options Summary		
Register offset	0	Optimal Default, Failsafe Default
Fill register offset (or index) for robot to read, in hexadecimal. Range: 0 - FF		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

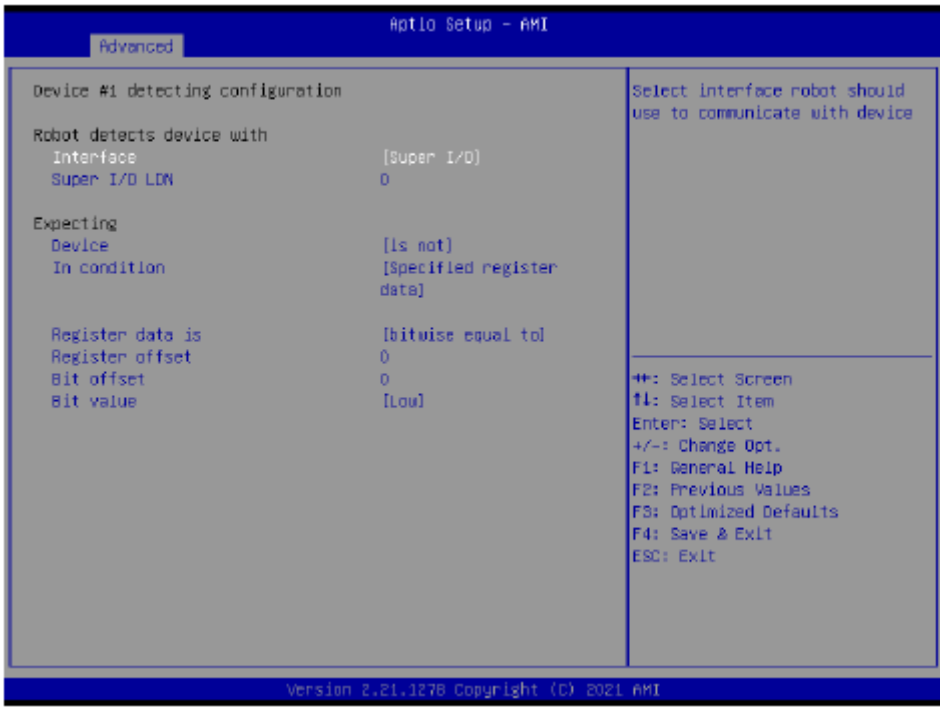
Interface: Legacy I/O



Options Summary		
I/O Address	0	Optimal Default, Failsafe Default
Fill I/O address device is responding to. Range: 0~FFFF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		

Options Summary		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

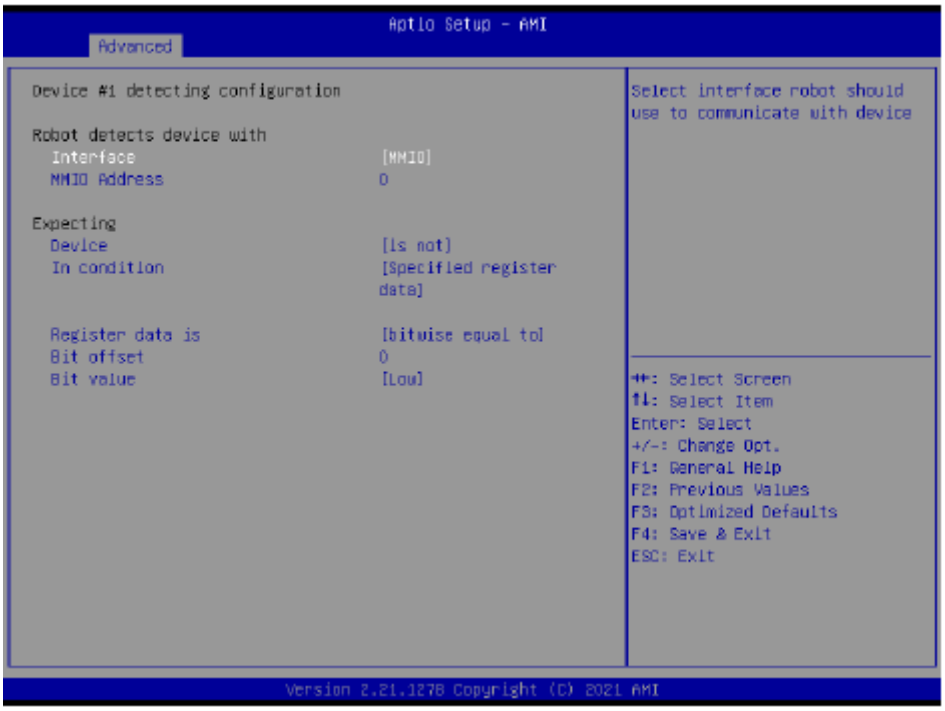
Interface: Super I/O



Options Summary		
Super I/O LDN	0	Optimal Default, Failsafe Default
Fill LDN number to a Super I/O device. Range: 0~FF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		

Options Summary		
Register offset	0	Optimal Default, Failsafe Default
Fill register offset (or index) for robot to read, in hexadecimal. Range: 0 - FF		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

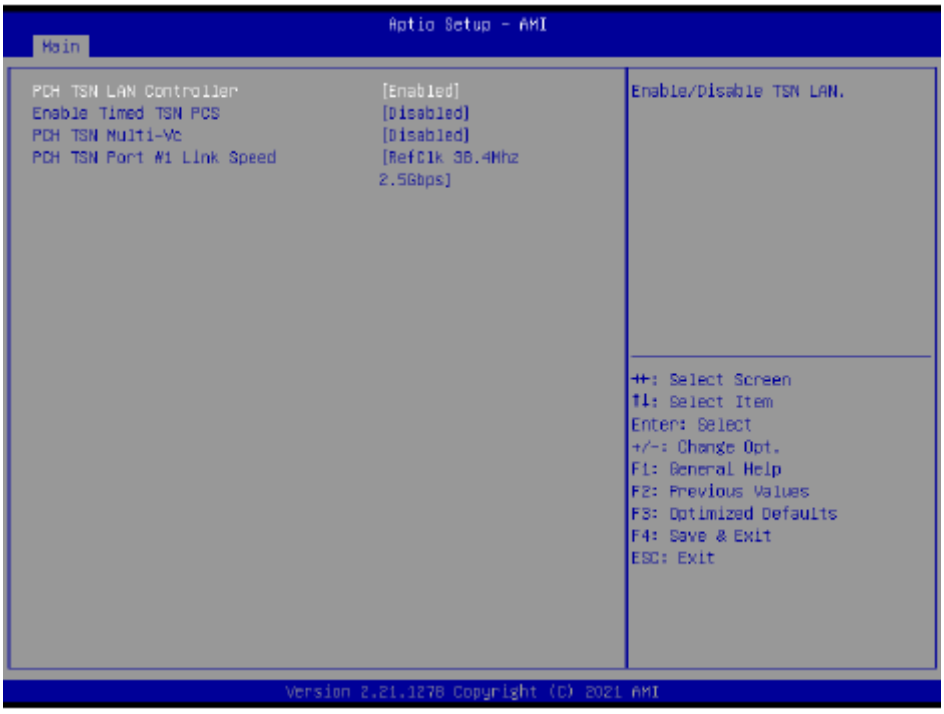
Interface: MMIO



Options Summary		
MMIO Address	0	Optimal Default, Failsafe Default
Fill Memory Mapped I/O address device is responding to. Range: 0~FFFFFFFF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		

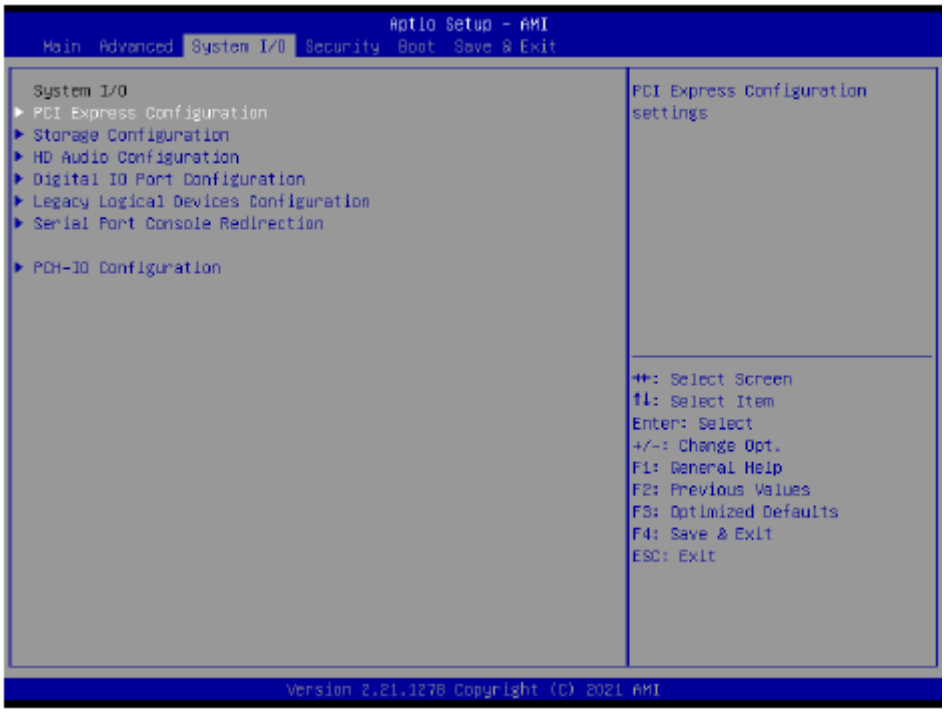
Options Summary		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

3.4.8 TSN GBE Configuration

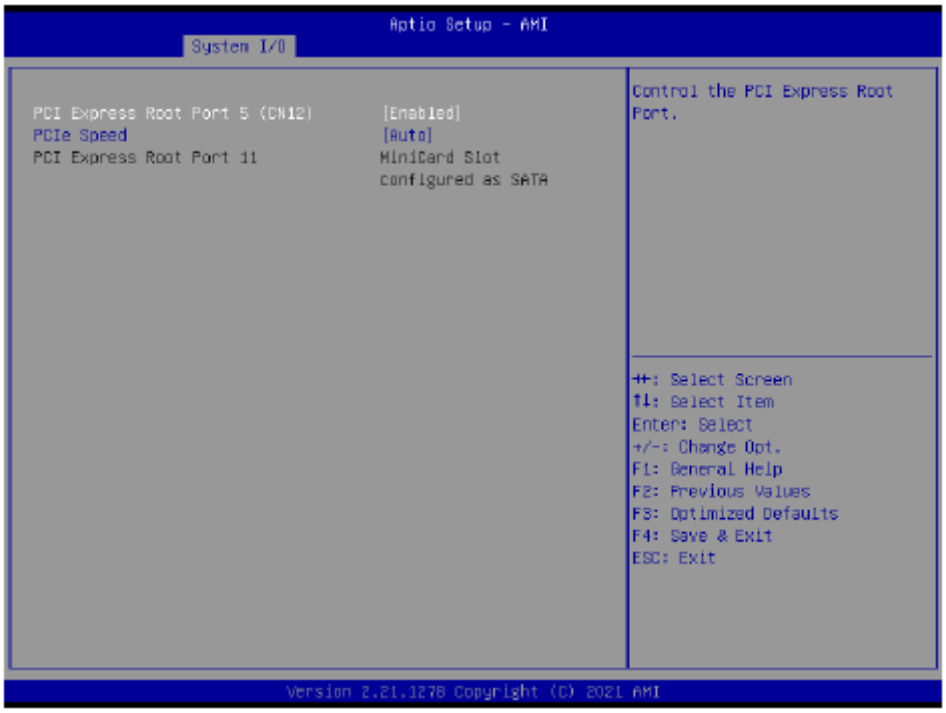


Options Summary		
PCH TSN LAN Controller	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable TSN LAN		
Enable Timed TSN PCS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable TSN PCS. When enabled, TSN PCS device will appear in ACPI table		
PCH TSN Multi-Vc	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable PCH TSN Multi Virtual Channels		
PCH TSN Port #1 Link Speed	RefClk 24Mhz 2.5Gbps	
	RefClk 24Mhz 1Gbps	Optimal Default, Failsafe Default
	RefClk 38.4Mhz 2.5Gbps	
	RefClk 38.4Mhz 1Gbps	
PCH TSN Link Speed config		

3.5 Setup Submenu: System I/O

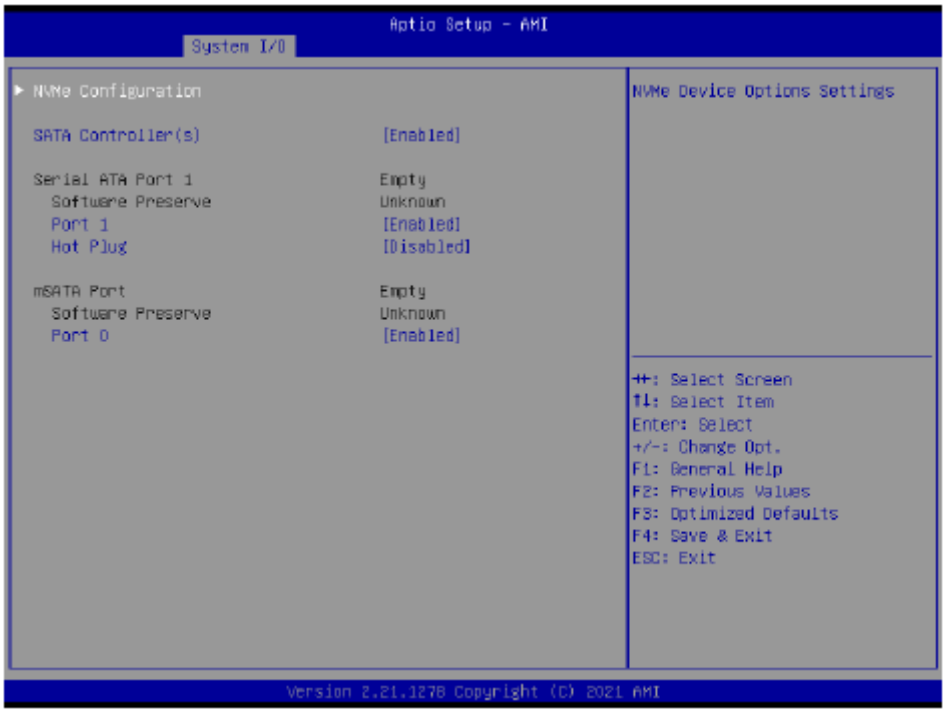


3.5.1 PCI Express Configuration



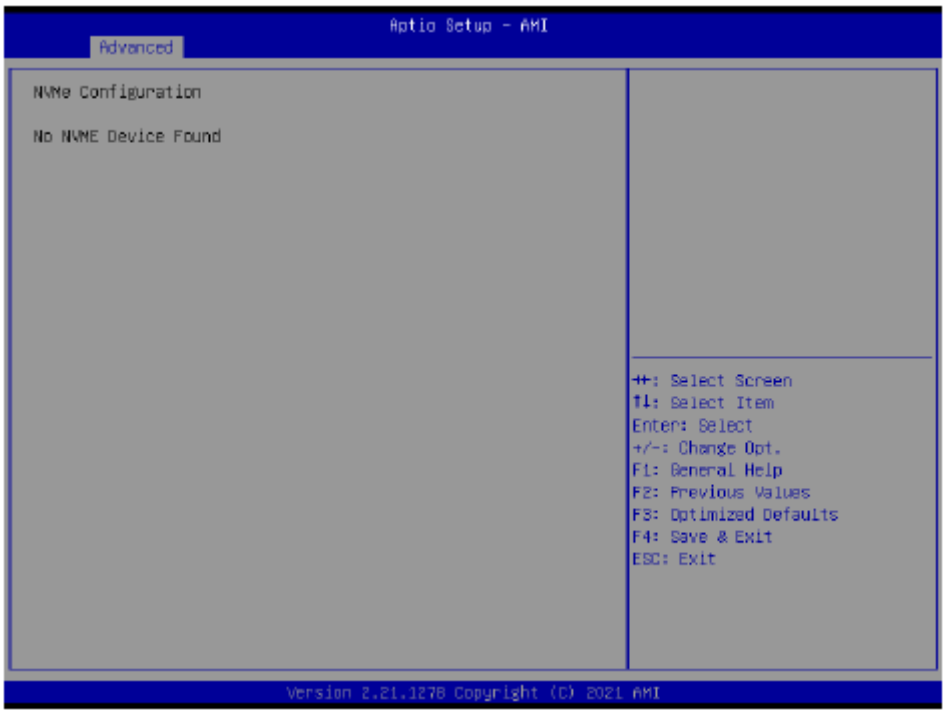
Options Summary		
PCI Express Root Port 5 (CN12) / Port11	Enabled	Optimal Default, Failsafe Default
	Disabled	
Control the PCI Express Root Port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Control the PCI Express Speed		

3.5.2 Storage Configuration

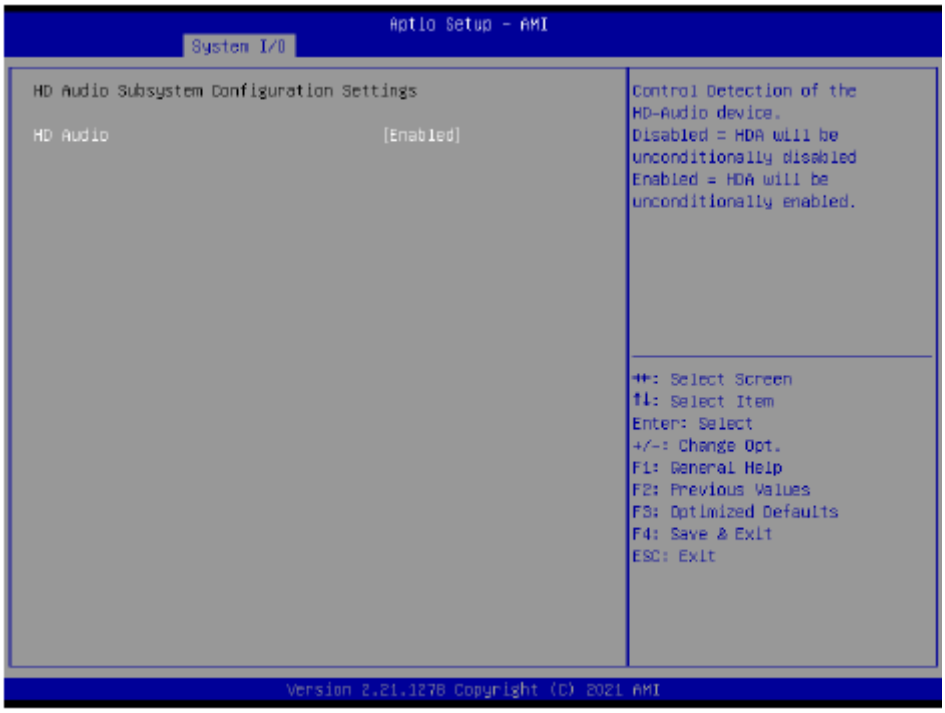


Options Summary		
SATA Controller(s)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable SATA Device.		
Port 0 / 1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		

3.5.2.1 NVME Configuration

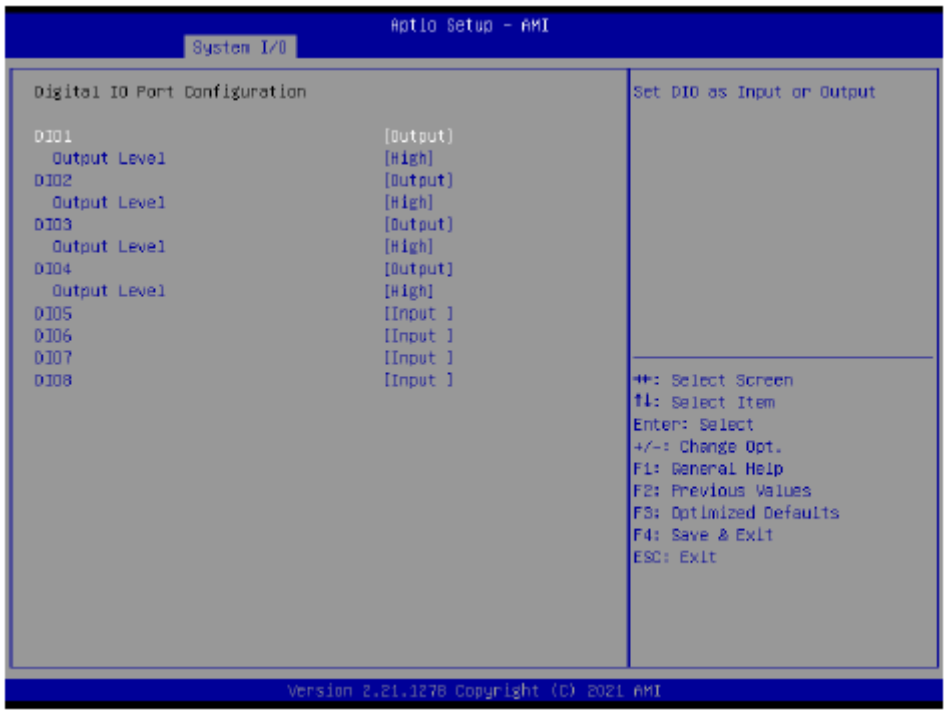


3.5.3 HD Audio Subsystem Configuration Settings



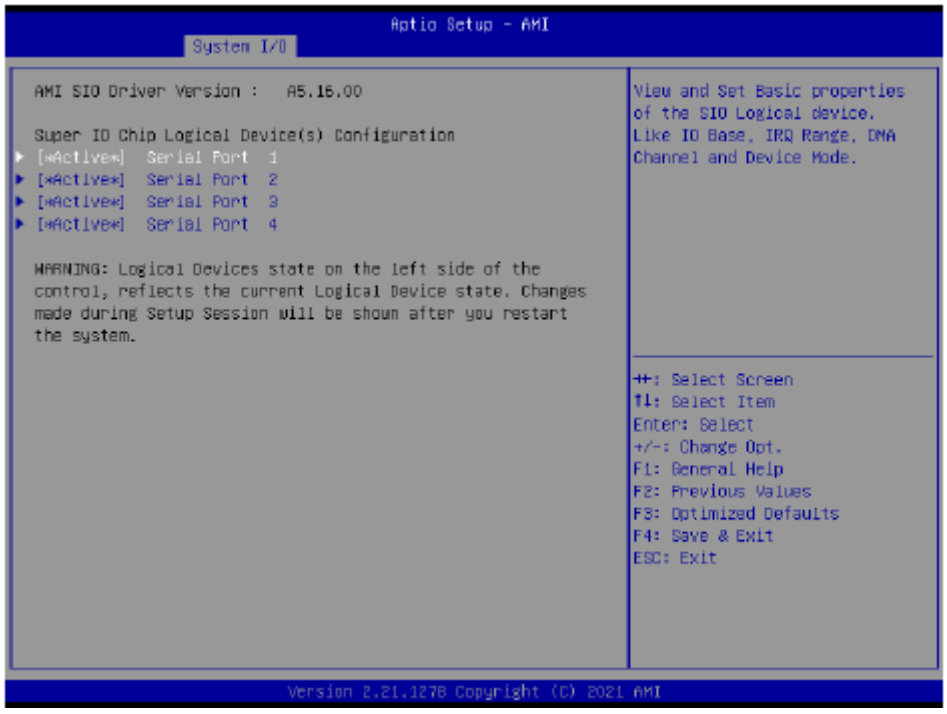
Options Summary		
HD Audio	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled.		

3.5.4 Digital IO Port Configuration

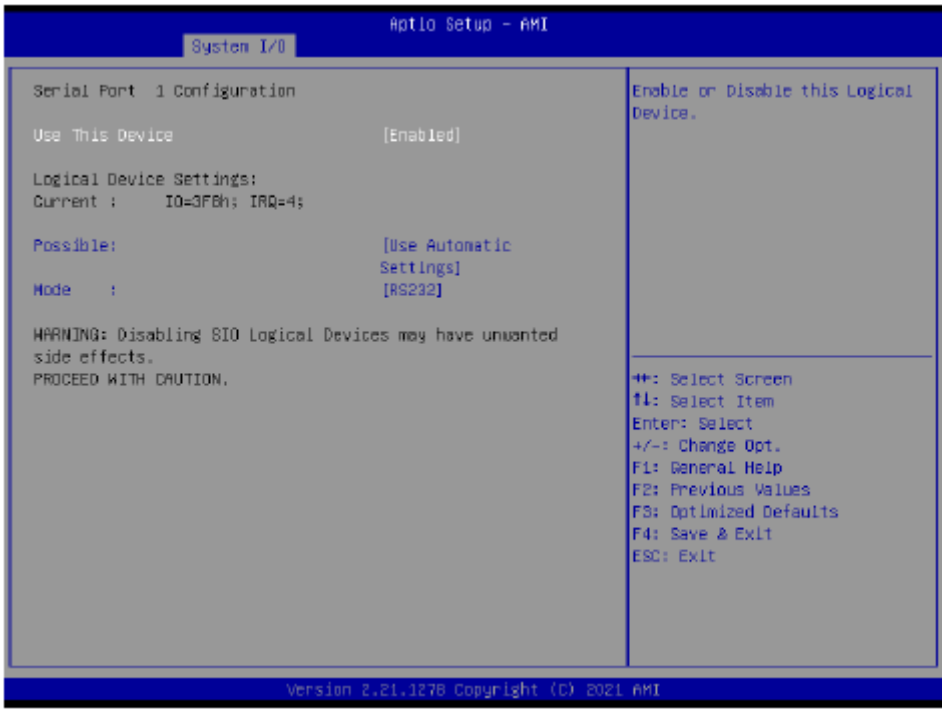


Options Summary		
DIO Port #	Output	
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		

3.5.5 Legacy Logical Devices Configuration

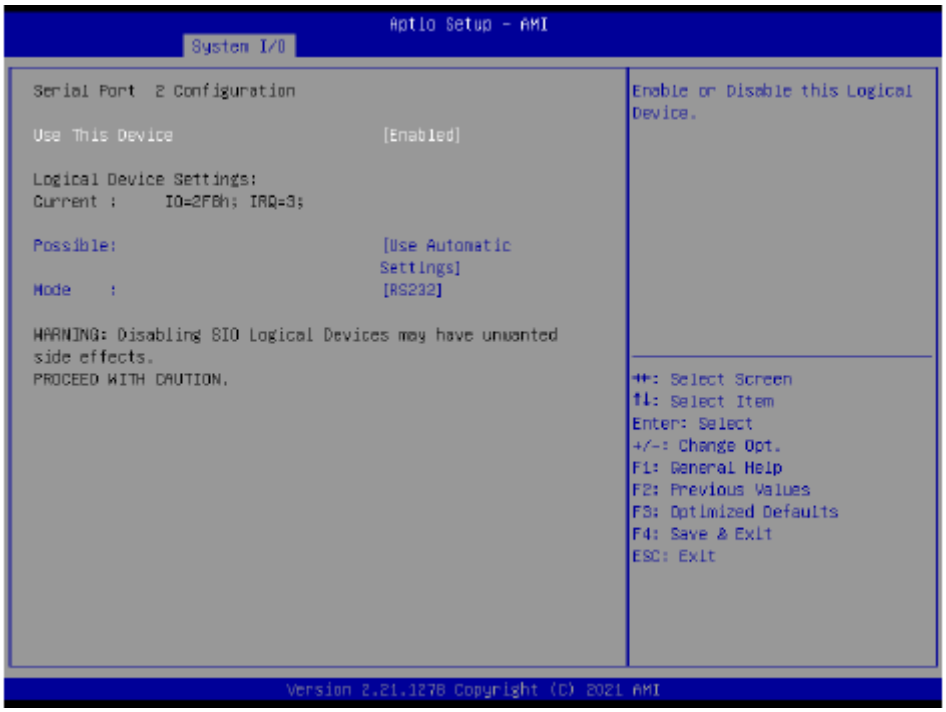


3.5.5.1 Serial Port1 Configuration



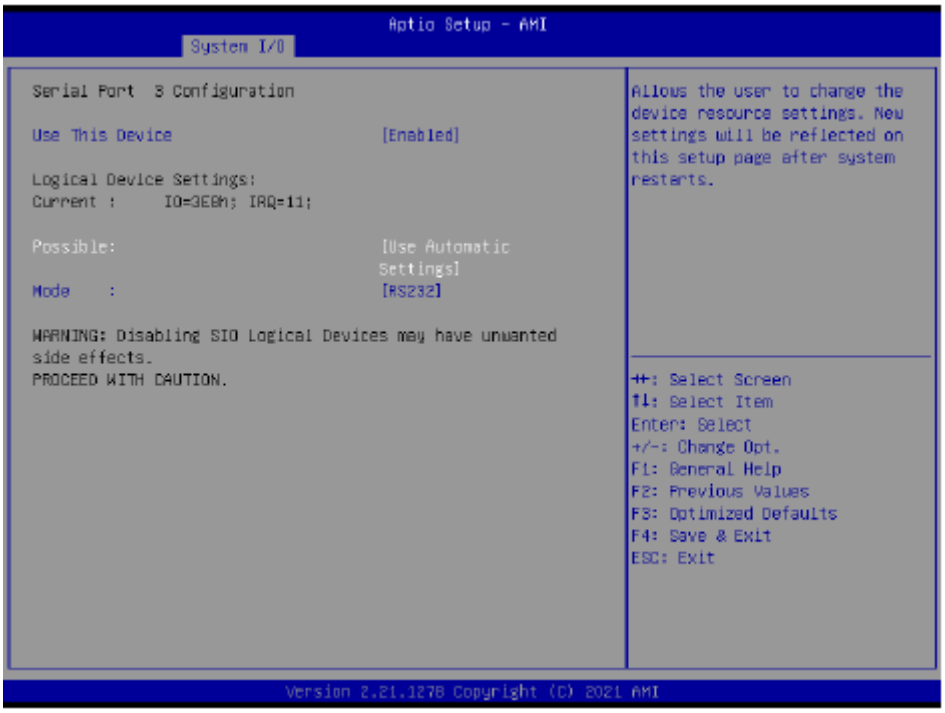
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4	
	IO=2F8h; IRQ=3	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

3.5.5.2 Serial Port2 Configuration



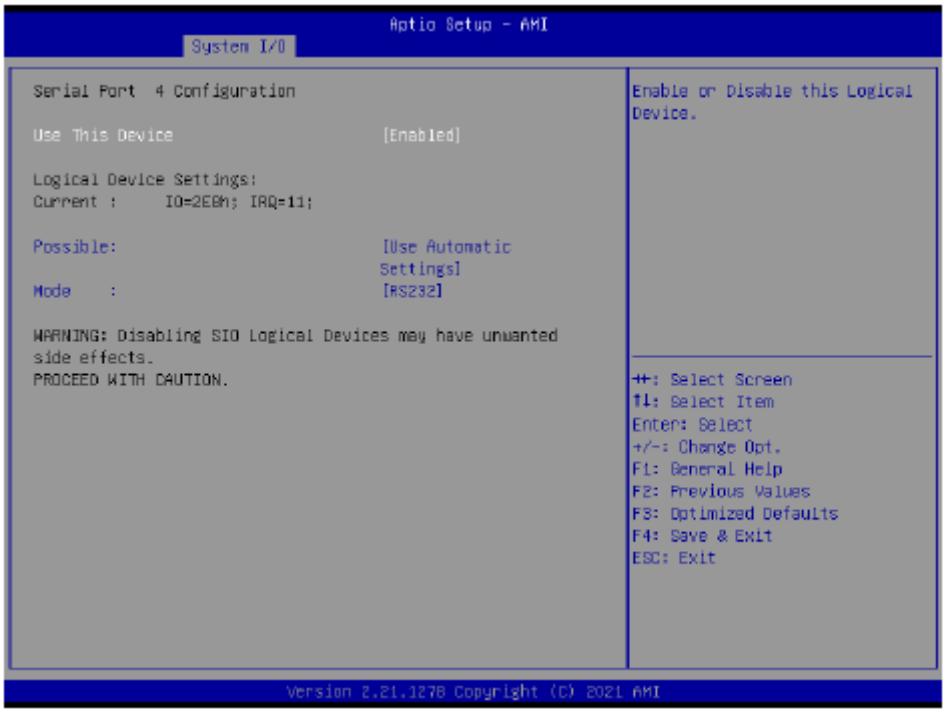
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3	
	IO=3F8h; IRQ=4	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

3.5.5.3 Serial Port3 Configuration



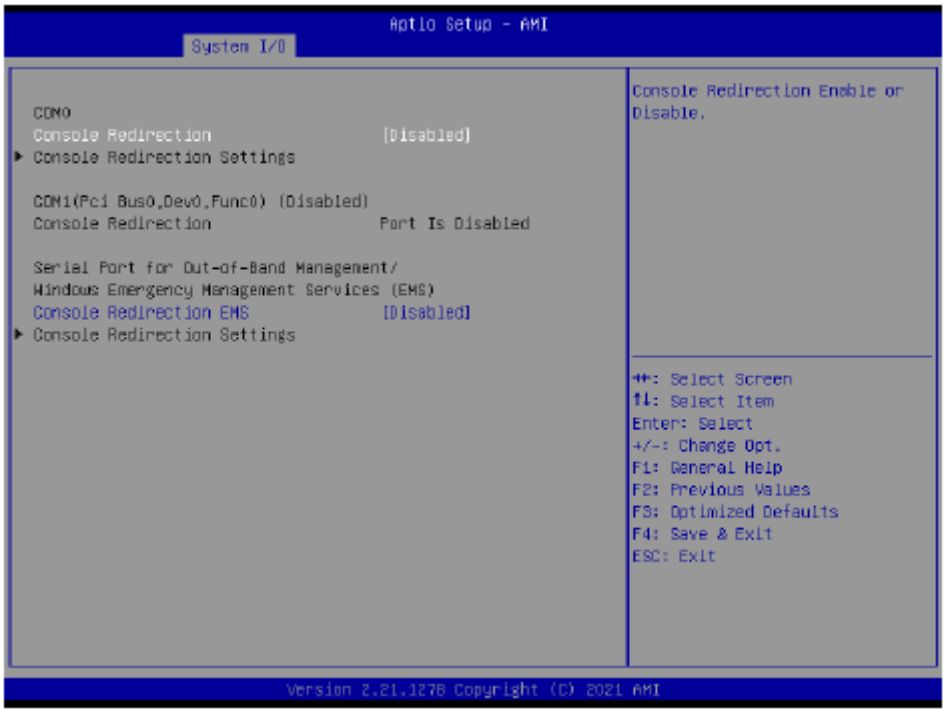
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3E8h; IRQ=11	
	IO=2E8h; IRQ=11	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

3.5.5.4 Serial Port4 Configuration



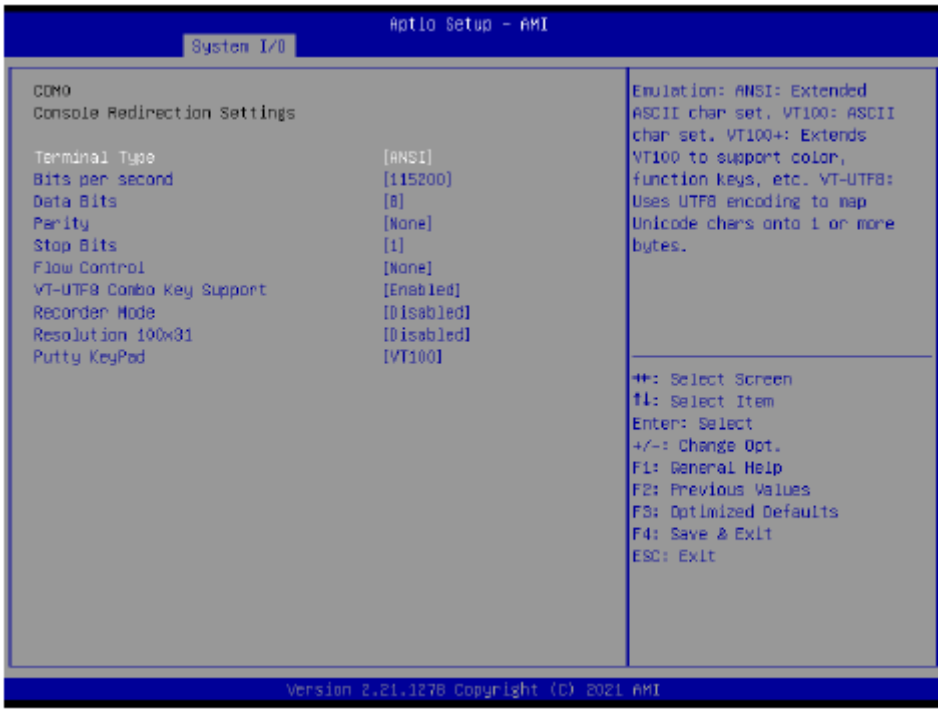
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2E8h; IRQ=11	
	IO=3E8h; IRQ=11	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

3.5.6 Legacy Logical Devices Configuration



Options Summary		
Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		
Console Redirection EMS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		

3.5.6.1 Console Redirection Settings



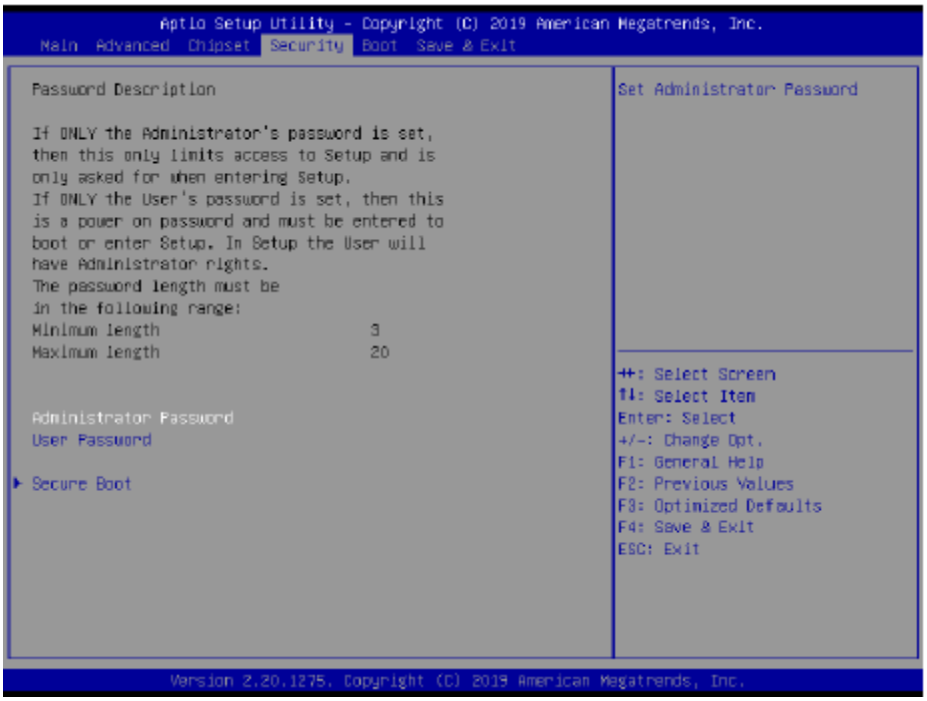
Options Summary		
Terminal Type	VT100	
	VT100+	
	VT-UTF8	
	ANSI	Optimal Default, Failsafe Default
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.		
Bits Per second	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		
Data Bits	7	
	8	Optimal Default, Failsafe Default
Data Bits		

Options Summary		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.		
Flow Control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		
VT-UTF8 Combo Key Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
With this mode enabled only text will be sent. This is to capture Terminal data.		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables extended terminal resolution		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select FunctionKey and KeyPad on Putty.		

3.5.7 PCH-IO Configuration

Options Summary		
MiniCard Slot Function	SATA	Optimal Default, Failsafe Default
	PCIe	
Select function enabled for Full size MiniCard Slot (CN10)		

3.6 Setup Submenu: Security



Change User/Administrator Password

You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.6.1 Trusted Computing

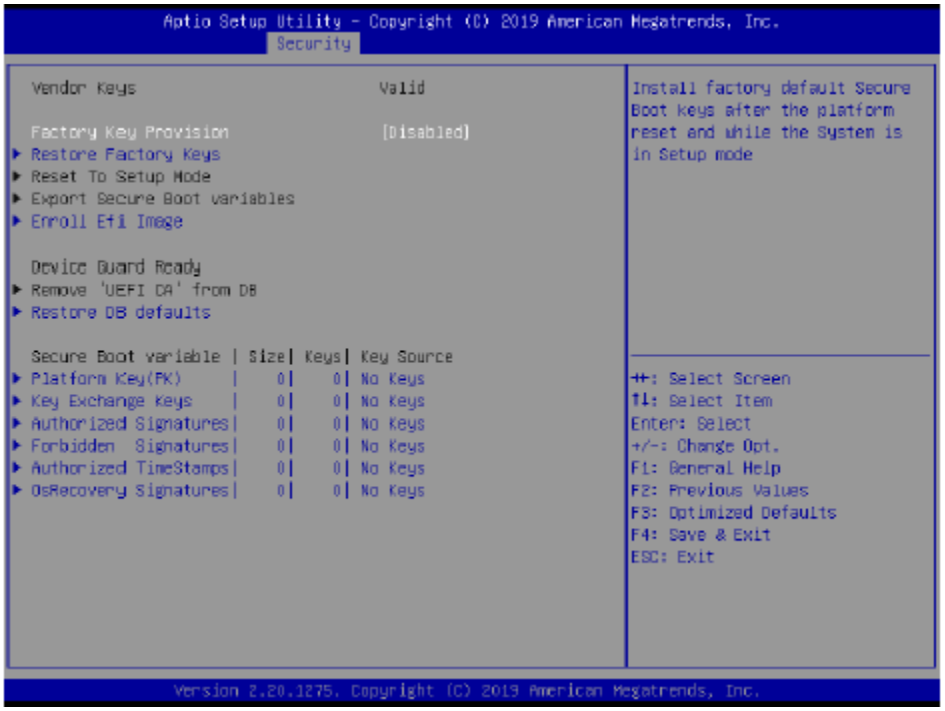
Options Summary		
Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA256 PCR Bank		
Pending Operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		

Options Summary		
Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable Platform Hierarchy		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		

3.6.2 Secure Boot

Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Secure Boot Mode	Custom	Optimal Default, Failsafe Default
	Standard	
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases		
Reset To Setup Mode		
Delete all Secure Boot key databases from NVRAM		

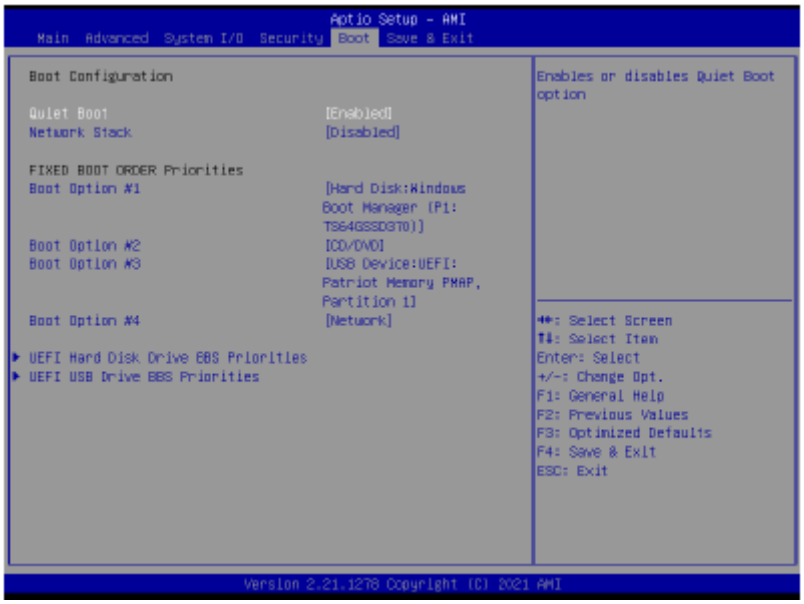
3.6.2.1 Key Management



Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases		
Reset To Setup Mode		
Delete all Secure Boot key databases from NVRAM		
Export Secure Boot variables		
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device		
Enroll Efi Image		
Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)		

Options Summary		
Remove 'UEFI CA' from DB		
Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db)		
Restore DB defaults		
Restore DB variable to factory defaults		
Platform Key(PK)	Details	
	Export	
	Update	
	Delete	
Key Exchange Keys	Details	
	Export	
	Update	
	Append	
	Delete	
Authorized Signatures	Details	
	Export	
	Update	
	Append	
	Delete	
Forbidden Signatures	Details	
	Export	
	Update	
	Append	
	Delete	
Authorized TimeStamps	Update	
	Append	
OsRecovery Signatures	Update	
	Append	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed		

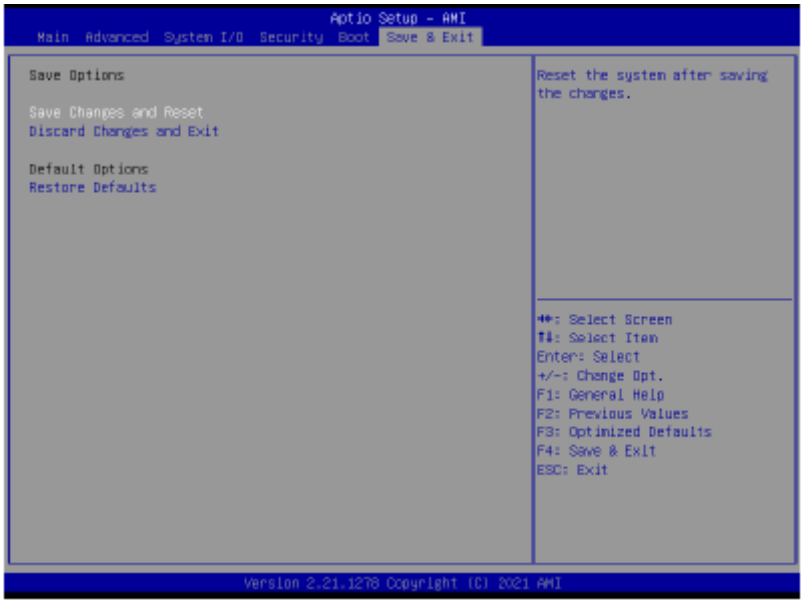
3.7 Setup Submenu: Boot



Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or disables showing boot logo.		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack		

3.7.1 BBS Priorities

3.8 Setup Submenu: Save & Exit

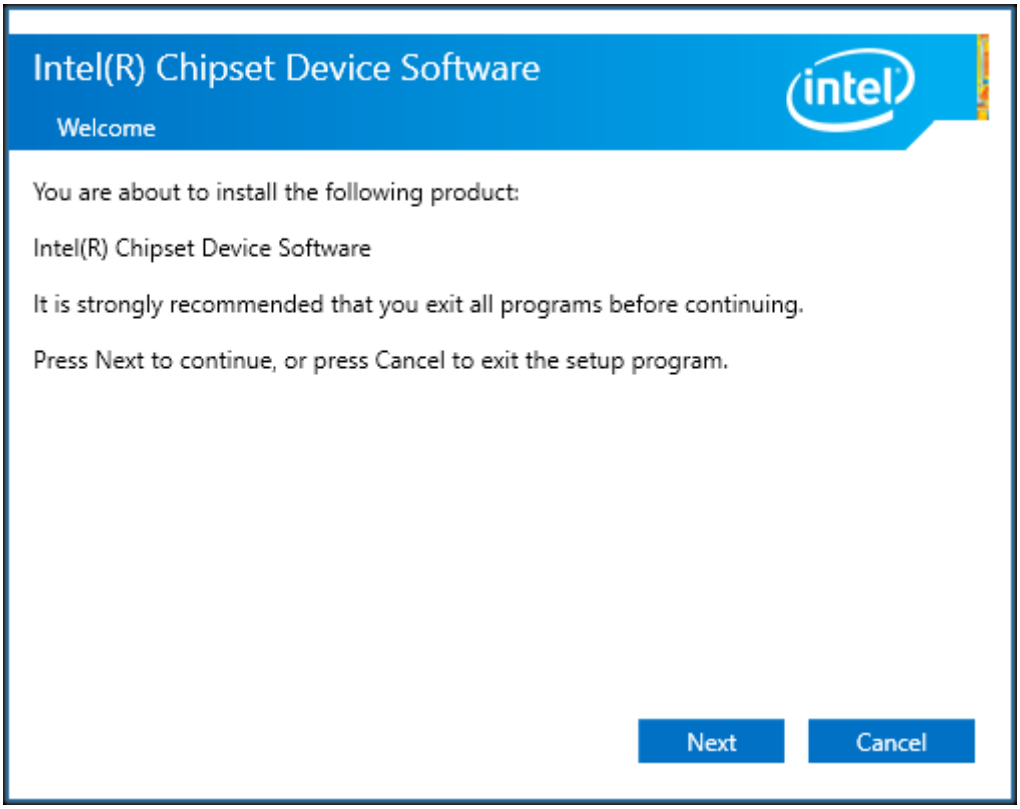


Chapter 4 Installation of Drivers

4.1 Intel® Chipset Device Software

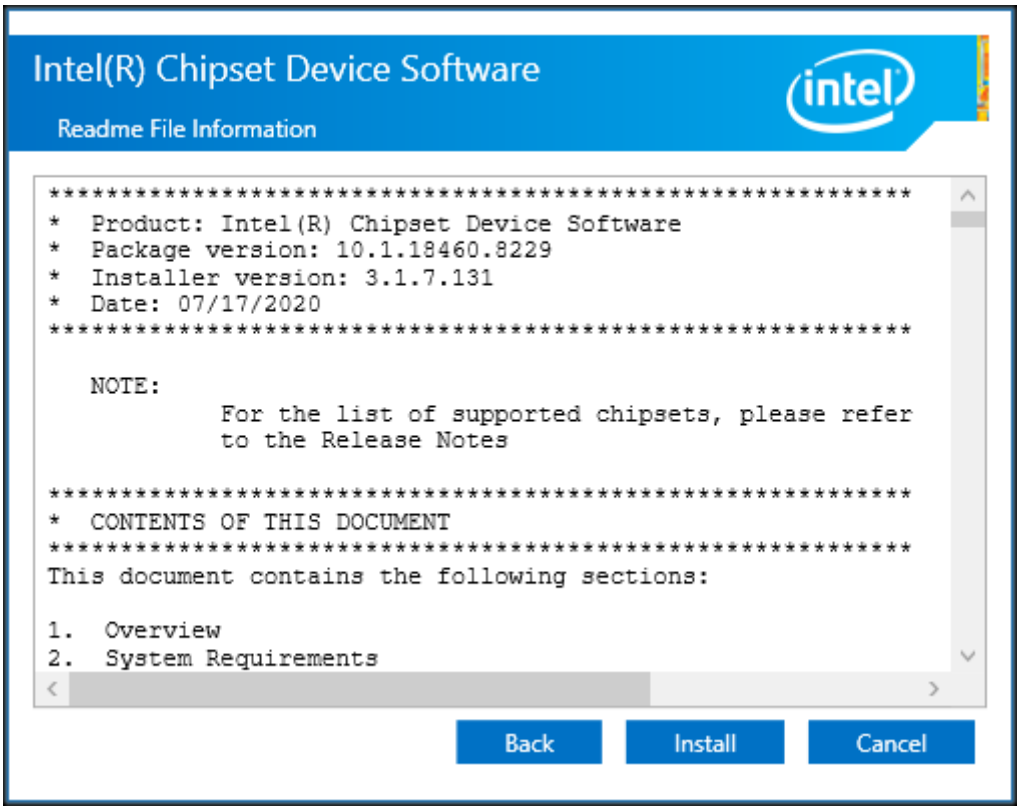
To install the Intel® Chipset Device Software, please follow the steps below.

Step 1. Here is welcome page. Please make sure you save and exit all programs before install**.** Click **Next.**



Step2. Read the license agreement. Click **Accept** to accept all of the terms of the license agreement.

Step3. Click **Install** to begin the installation.



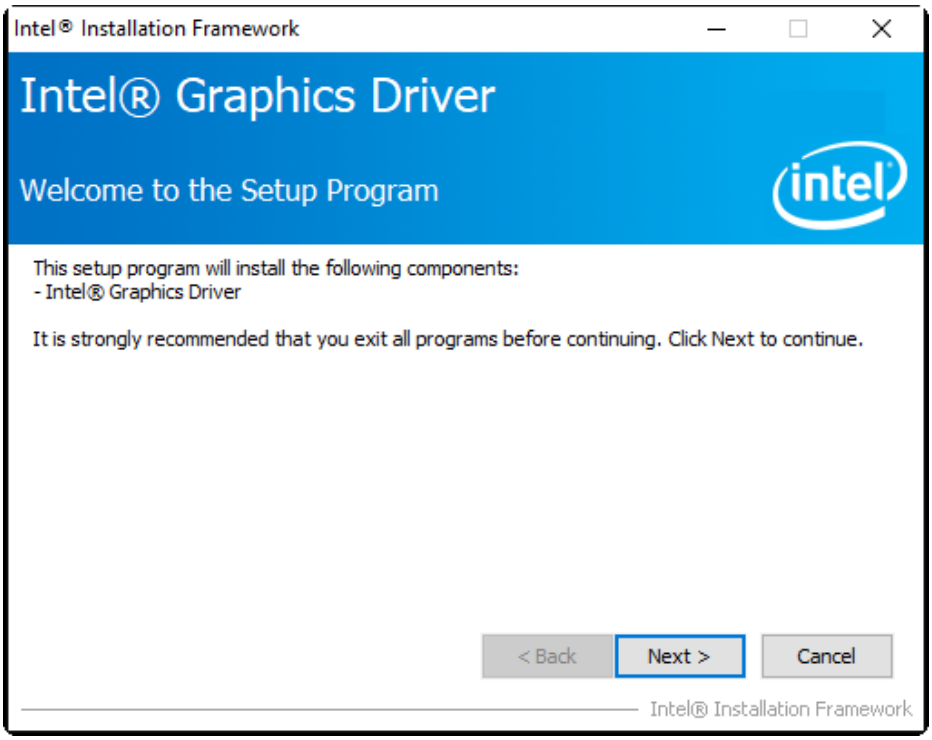
Step5. Click **Finish** to finish installation.


Intel(R) Chipset Device Software
Completion
You have successfully installed the following product:
Intel(R) Chipset Device Software
Press Finish to complete the setup process.
View Log Files
Finish

4.2 Intel® VGA Chipset

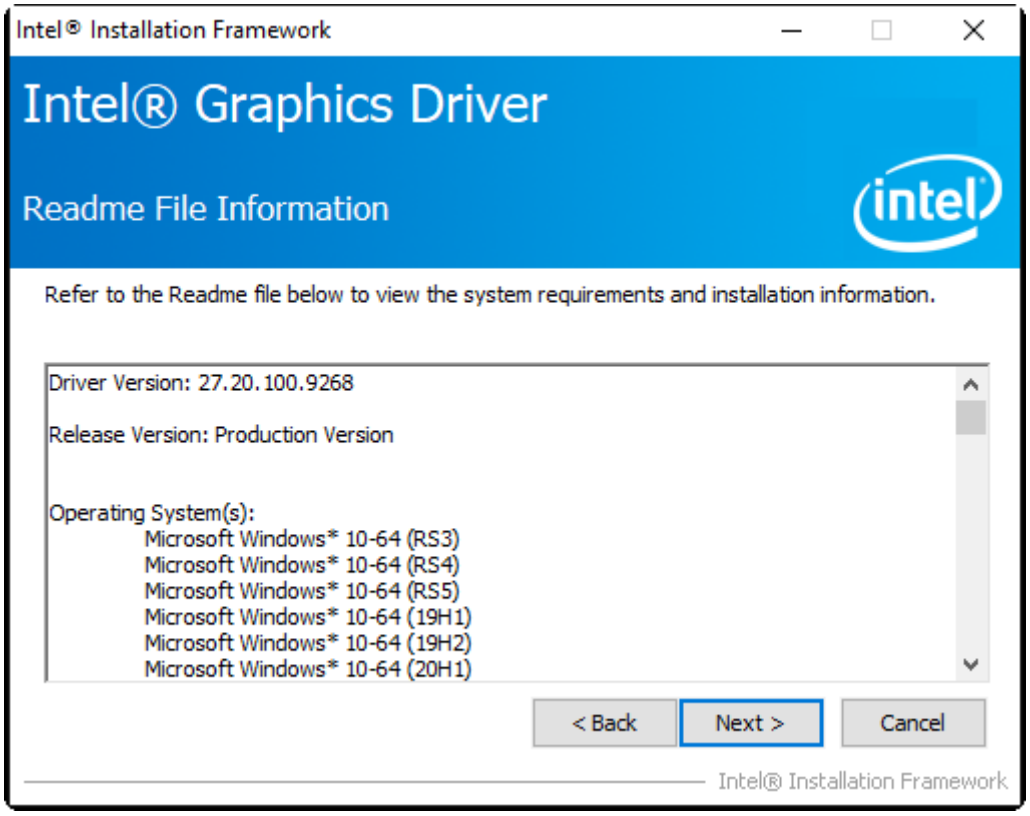
To install the Intel® VGA Chipset, please follow the steps below.

Step1. Click **Next.**

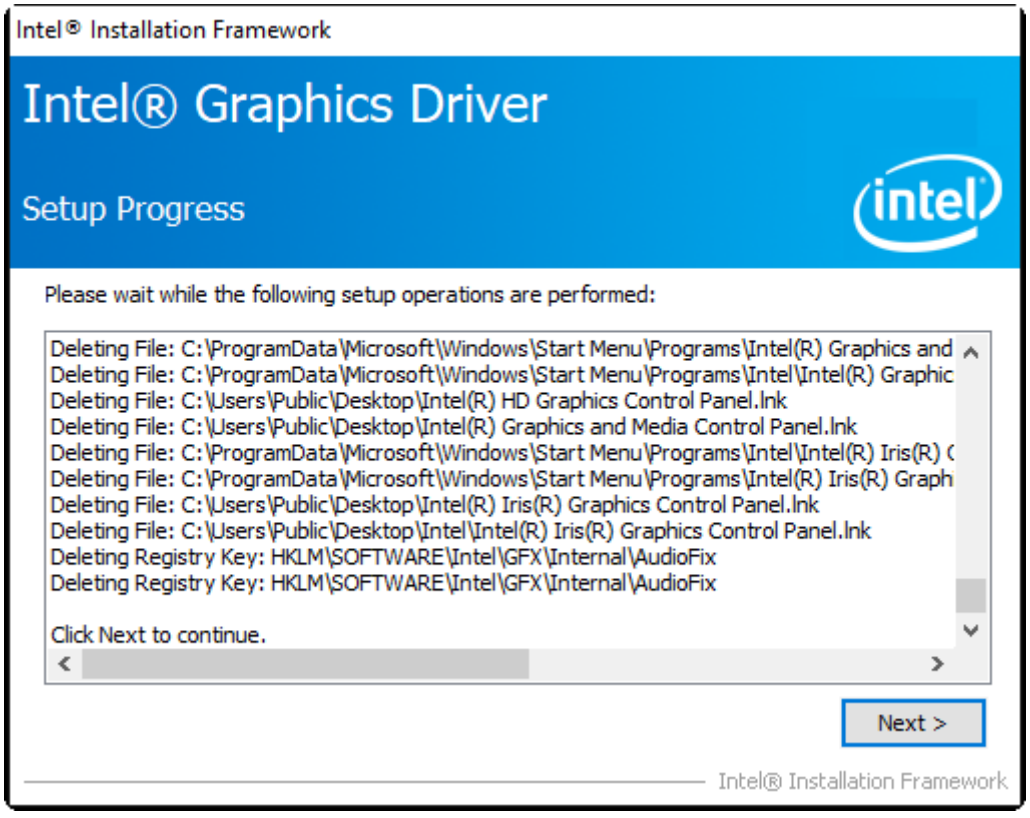


Step2. Read the license agreement. Click **Yes** to accept all of the terms of the license agreement.

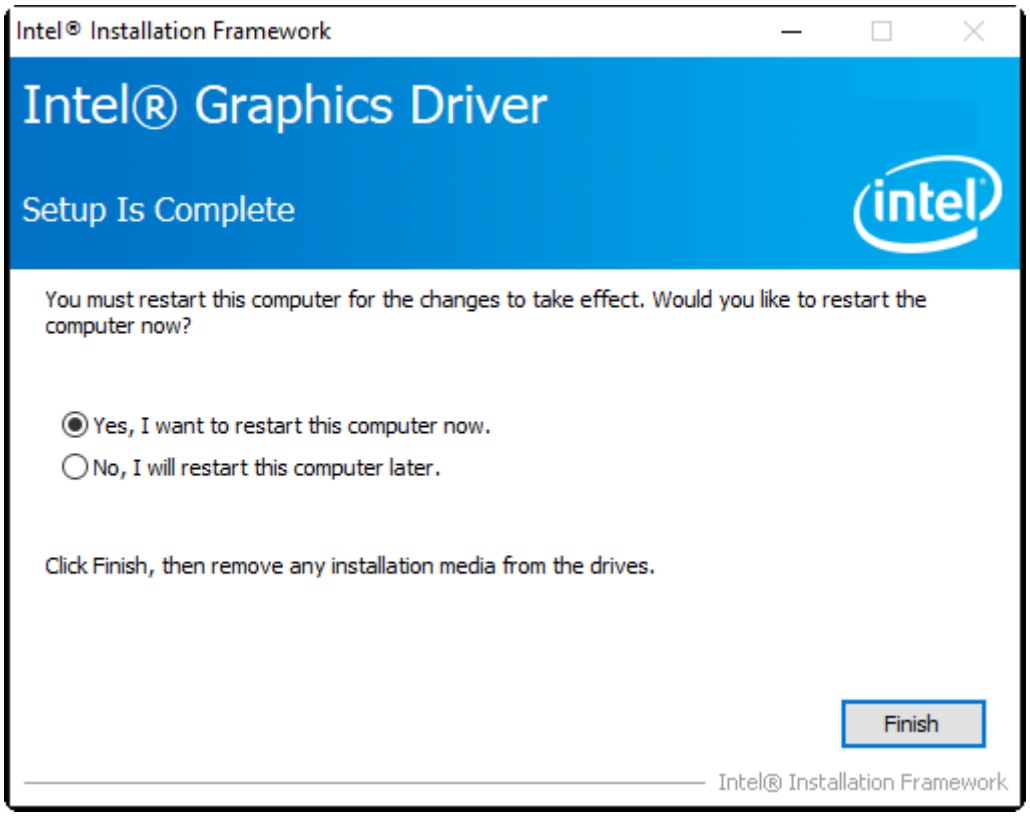
Step3. Click **Next** to continue.



Step4. Click **Next** to continue the program.



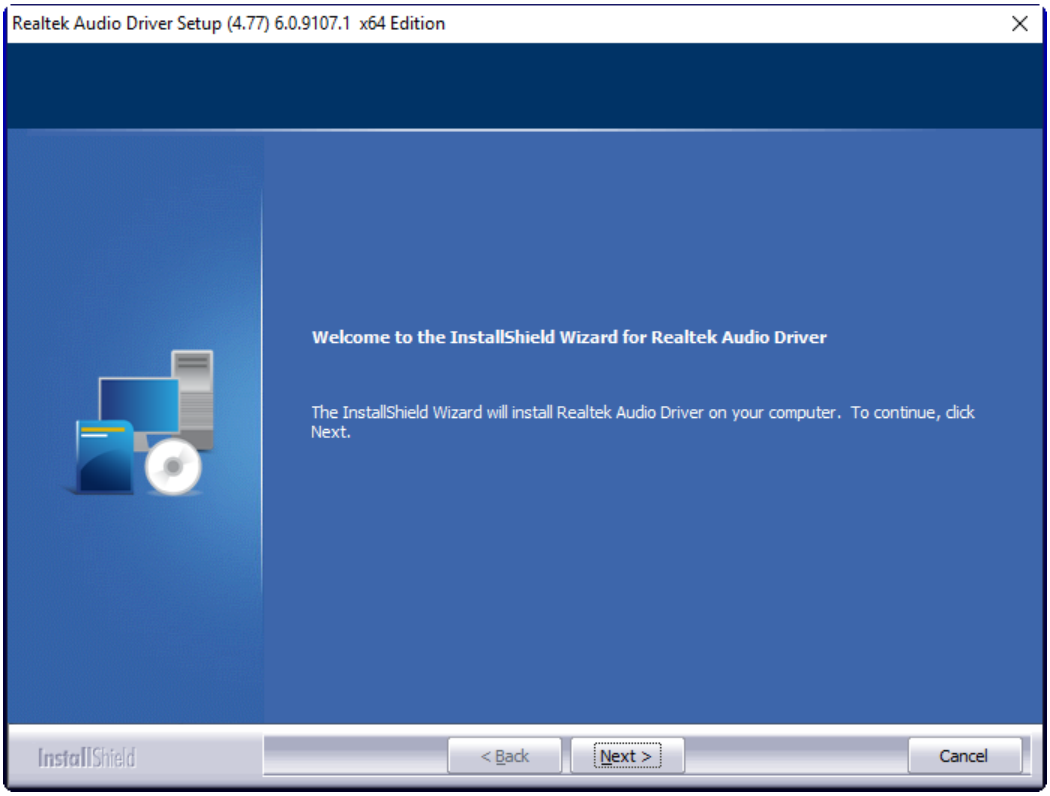
Step5. Select **Yes, I want to restart this computer now**. Click **Finish** to complete installation.



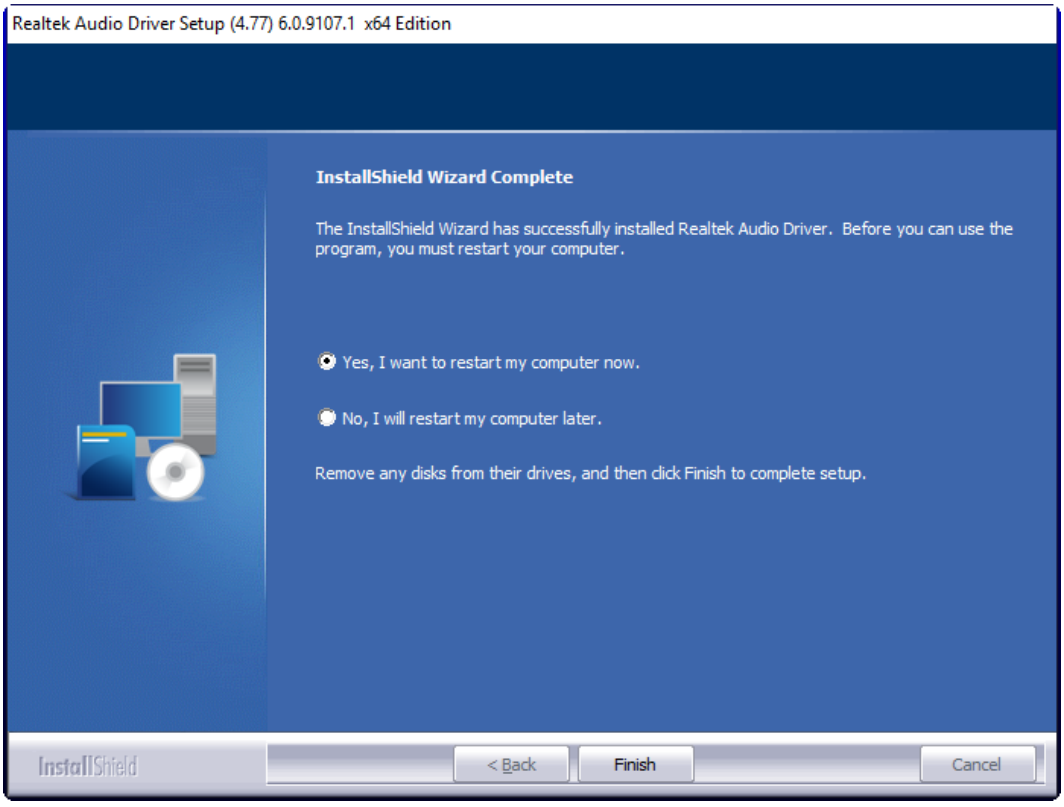
4.3 Realtek Audio Driver

To install the Realtek Audio Driver, please follow the steps below.

Step1. Select setup language you need. Click **Next** to continue.



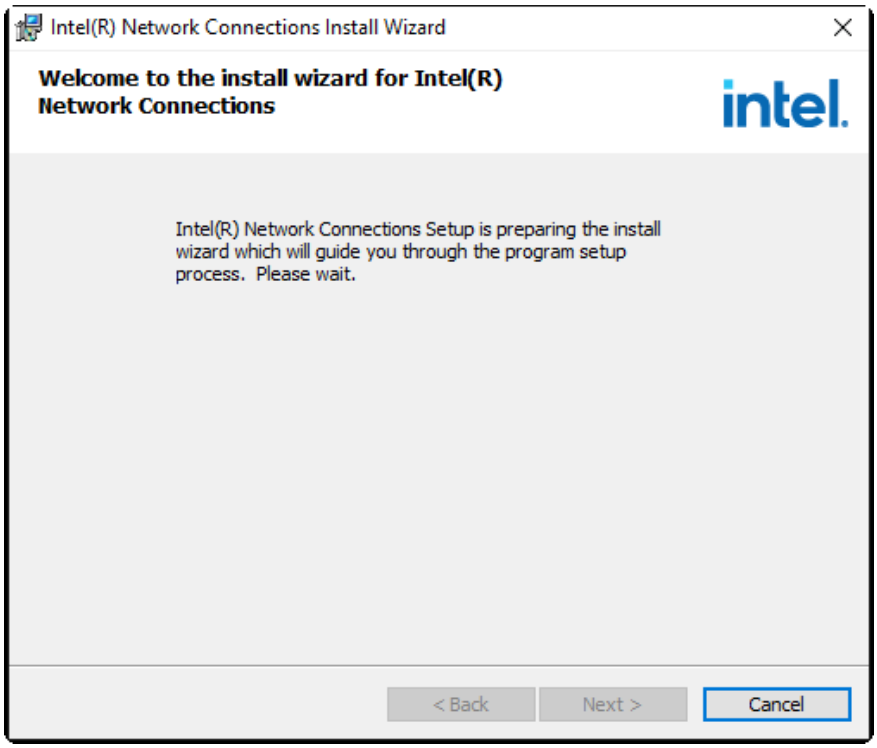
Step2. Click **Finish** to complete the installation.



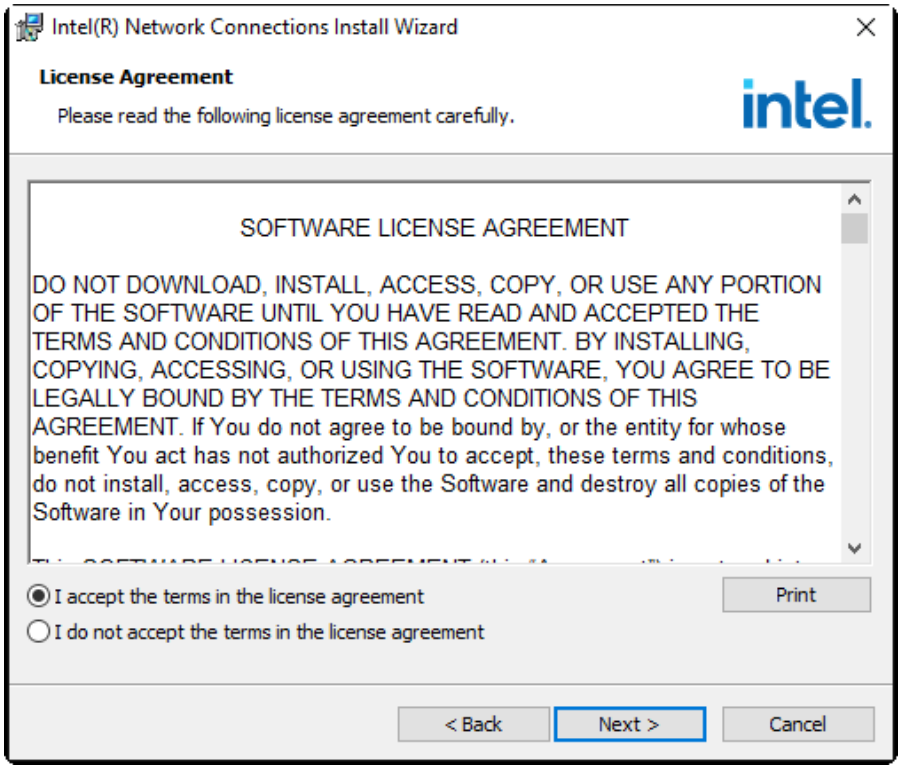
4.4 Intel® LAN Driver

To install the Intel® LAN Driver, please follow the steps below.

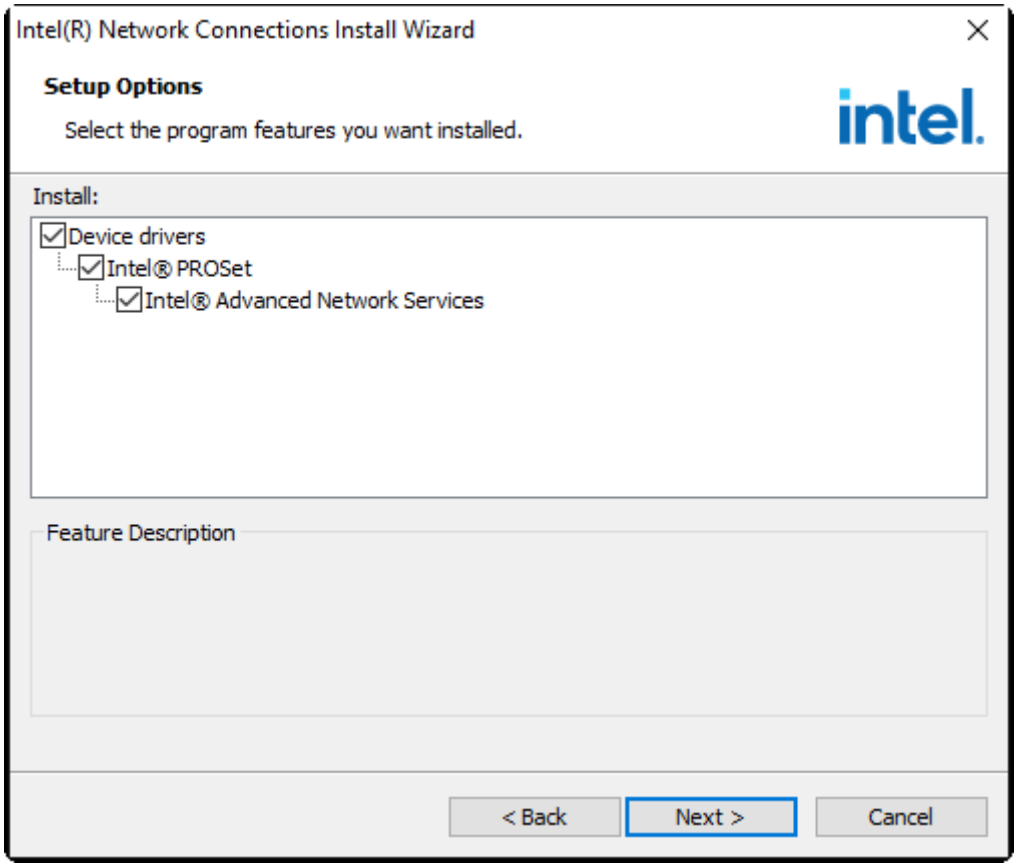
Step1. Here is welcome page. Please wait for program setup process.



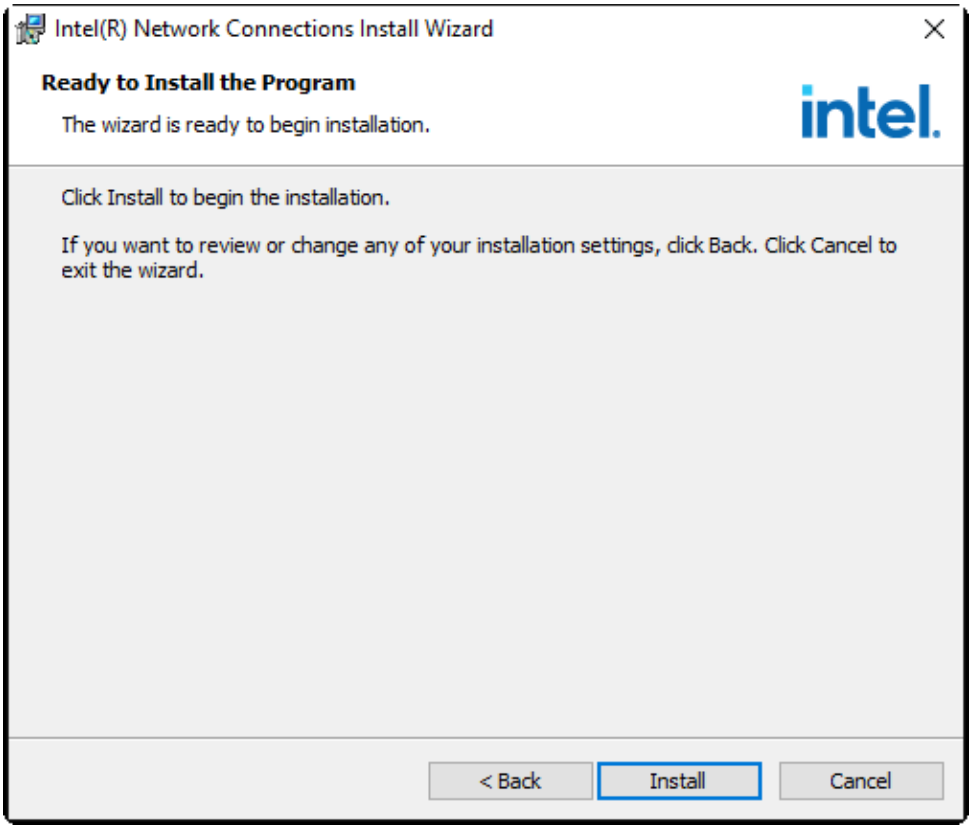
Step2. Read the license agreement. Select **I accept the terms in the license agreement** and click **Yes** to accept all of the terms of the license agreement.



Step3. Click **Next** to continue.



Step4. Click **Install** to begin the installation.



Step5. Click **Install** to begin the installation.