

User Manual

SOM-2532



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Product Warranty (2 years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced free of charge during the warranty period. For out-of-warranty repairs, customers will be billed according to the cost of replacement mate-rials, service time, and freight. Please consult your dealer for more details.

If you believe your product to be defective, follow the steps outlined below.

- 1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
- 2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
- 3. If your product is diagnosed as defective, obtain a return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
- 4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
- 5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

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Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This type of cable is available from Advantech. Please contact your local supplier for ordering information.

Test conditions for passing also include the equipment being operated within an industrial enclosure. In order to protect the product from damage caused by electrostatic discharge (ESD) and EMI leakage, we strongly recommend the use of CEcompliant industrial enclosure products.

FCC Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

FM

This equipment has passed FM certification. According to the National Fire Protection Association, work sites are categorized into different classes, divisions, and groups based on hazard considerations. This equipment is compliant with the specifications for Class I, Division 2, Groups A, B, C, and D indoor hazards.

Technical Support and Assistance

- 1. Visit the Advantech website at www.advantech.com/support to obtain the latest product information.
- 2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
 - Product name and serial number
 - Description of your peripheral attachments
 - Description of your software (operating system, version, application software, etc.)
 - A complete description of the problem
 - The exact wording of any error messages

Warnings, Cautions, and Notes



Warning! Warnings indicate conditions, which if not observed, can cause personal injury!





Caution! Cautions are included to help prevent hardware damage and data losses. For example,

"Batteries are at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions."



Notes provide optional additional information.

Document Feedback

To assist us with improving this manual, we welcome all comments and constructive criticism. Please send all feedback in writing to support@advantech.com.

Packing List

Before system installation, check that the items listed below are included and in good condition. If any item does not accord with the list, contact your dealer immediately.

- SOM-2532 module
- 1 x Heatspreader (1960093586N000)

Safety Instructions

- 1. Read these safety instructions carefully.
- 2. Retain this user manual for future reference.
- 3. Disconnect the equipment from all power outlets before cleaning. Use only a damp cloth for cleaning. Do not use liquid or spray detergents.
- 4. For pluggable equipment, the power outlet socket must be located near the equipment and easily accessible.
- 5. Protect the equipment from humidity.
- 6. Place the equipment on a reliable surface during installation. Dropping or letting the equipment fall may cause damage.
- 7. The openings on the enclosure are for air convection. Protect the equipment from overheating. Do not cover the openings.
- 8. Ensure that the voltage of the power source is correct before connecting the equipment to a power outlet.
- 9. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
- 10. All cautions and warnings on the equipment should be noted.
- 11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage from transient overvoltage.
- 12. Never pour liquid into an opening. This may cause fire or electrical shock.
- 13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
- 14. If any of the following occurs, have the equipment checked by service personnel:
 - The power cord or plug is damaged.
 - Liquid has penetrated the equipment.
 - The equipment has been exposed to moisture.
 - The equipment is malfunctioning, or does not operate according to the user manual.
 - The equipment has been dropped and damaged.
 - The equipment shows obvious signs of breakage.
- 15. Do not leave the equipment in an environment with a storage temperature of below -20°C (-4°F) or above 60°C (140°F) as this may damage the components. The equipment should be kept in a controlled environment.
- 16. CAUTION: Batteries are at risk of exploding if incorrectly replaced. Replace only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.
- 17. In accordance with IEC 704-1:1982 specifications, the sound pressure level at the operator's position does not exceed 70 dB (A).

DISCLAIMER: These instructions are provided according to IEC 704-1 standards. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from the PC chassis before manual handling. Do not touch any components on the CPU card or other cards while the PC is powered on.
- Disconnect the power before making any configuration changes. A sudden rush of power after connecting a jumper or installing a card may damage sensitive electronic components.

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General Information

This chapter details background information on the SOM-2532 CPU Computer-on-Module.

- Sections include:
- Introduction
- Functional Block Diagram
- Product Specification

1.1 Introduction

Advantech's SOM-2532 series features SMARC 2.1.1 specifications and is equipped with the newest generation of Intel® processors — including the Pentium®, Celeron®, and Atom® platforms. SOM-2532 is designed with up to 4 cores and yields 40% better CPU performance and improved graphics processing when compared with previous models. SOM-2532 supports onboard DDR4 3200MT/s, up to 16GB capacity, and IBECC on selected SKUs. It is equipped with onboard eMMC up to 64GB to ensure product stability. SOM-2532 supports multiple I/Os and display inputs — including dual GbE LAN with TSN PHY to improve device accuracy, 2 x CAN-FD, and 3 x independent displays up to 4K. Several I/Os are faster than those of its predecessors — these include 2 x USB 3.2 Gen2 (10GT/s), 4 x PCIe Gen3 (8.0GT/s), and 1 x SATA Gen3. CAN FD enables a maximum 8Mbps data transfer rate and is capable of reaching 10 x the payload transmission speed to empower data-intensive applications. Likewise, SOM-2532 uses an increased data payload size and the CAN FD protocol to enhance security.

Advantech iManager (SUSI 4) satisfies diverse embedded application requirements by providing a multi-level watchdog timer, voltage and temperature monitoring, thermal protection and mitigation through processor throttling, LCD backlight on/off and brightness control, and embedded storage for customized information. When combined with Advantech's WISE-PaaS/RMM, it can remotely monitor and control devices over the Internet. All Advantech SMARC modules integrate iManager and WISE-PaaS/RMM.

Acronyms

Term	Define					
AC'97	Audio CODEC (Coder-Decoder)					
ACPI	Advanced Configuration Power Interface – standard for implementing power- saving modes in PC-AT systems.					
BIOS	Basic Input Output System – firmware in a PC-AT system that is used to initial- ize system components before handing control over to the operating system.					
CAN	Controller-area network (CAN or CAN-bus) is a vehicle bus standard designed to allow micro-controllers to communicate with each other within a vehicle without a host computer.					
DDI	Digital Display Interface – including Display Port, HDMI/DVI, and SDVO.					
EAPI	 Embedded Application Programmable Interface. Software interface for COM Express[®] specific industrial functionality: System information Watchdog timer I2C Bus Flat Panel brightness control User storage area GPIO 					
GbE	Gigabit Ethernet					
GPIO	General purpose input output					
HDA	Intel® High Definition Audio (HD Audio) refers to the specification released by Intel in 2004 for delivering high definition audio that is capable of playing back more channels at higher quality than AC'97.					
I2C	Inter-Integrated Circuit – 2 wire (clock and data) signaling scheme allowing communication between integrated circuits, primarily used to read and load register values.					
ME	Management Engine					
PC-AT	"Personal Computer – Advanced Technology" – an IBM trademark term used to refer to Intel-based personal computers in the 1990s.					

PEG	PCI Express Graphics
RTC	Real-Time Clock – battery-backed circuit in PC-AT systems that keeps the system time and date as well as certain system setup parameters.
SPD	Serial Presence Detect – refers to serial EEPROM on DRAMs that has DRAM Module configuration information.
ТРМ	Trusted Platform Module – a chip to enhance the security features of a com- puter system.
UEFI	Unified Extensible Firmware Interface
WDT	Watchdog Timer

1.2 Functional Block Diagram

LPDDR4 max. 16GB 3200MT/s IBECC for Specific SKUs eMMC Storage Onboard		eDP/MIPL-DSI(Optional) eDP0,1 eDP to LVDS ↓ LVDS (NXP PTN3460) DDI2 Level Shifter (NXP PTN3363) DDI1 (DP++) DP++0	
		PCle0,1 PClex1 IA, B	
		PCIe2 SERDES1(Optional) BIOS Mapping C	
		SERDESO(Optional) BIOS Mapping BIOS Mapping	
		RGMII0 Ethernet0	
		RGMII1 Giga LAN Ethernet1	
		CAN FD CAN PHY CANO	tor Iger)
	Intel Atom® x6000, Pentium® and	CAN FD CAN PHY CAN1	Conne [.] Iden Fir
	Celeron [®] x6000 Series Processor	1250 125	5.9
		I252 HDA(I2S optional)	MAR 4-pir
		SATAO 1 SATA	3.6
		6 USB2.0 (1 OTG)	
		2 USB3.1 Gen2 (1 OTG)	
		SER0,2 2 UART (4 Lanes)	
		SDIO SD Card	
		SPI0 SPI	
		SPI BIOS TPM	
		Embedded Controller (ITE5121)	
		GPIO Port 0-4	
		I2C(Optional)	

1.3 Product Specifications

1.3.1 Compliance

- SMARC (Smart Mobility Architecture) 2.1
- Basic Size 82 x 50 mm (3.22 x 1.96 in)

1.3.2 Feature List

Feature	Min/Max in SMARC 2.1	SOM-2532
Memory	1	LPDDR4
eMMC (on module)	0/(N/A)	1
LVDS LCD/eDP/MIPI-DSI	1/1/1	1/1/1
HDMI/DP++	0/1	1/1
DP++	0/1	1
MIPI-CSI	0/2	0
SDIO	0/1	1
SPI	0/2	1
12S	0/1	1
Audio HDA/I2S2	0/1	1
SMBus	0/1	1
12C	2/6	2
Serial Port	2/4	4
CAN Bus	0/2	2
USB 2.0	2/6	6
USB 3.2	0/2	2
USB (OTG)	0/2	0
PCIe (Gen3)	0/4	4
SATA	0/1	1
GbE	0/2	2
Watchdog	0/1	1
GPIO	14/14	14
Management	1/1	1
Boot Select	1/1	1
JTAG (on board)	0/1	0
Wi-Fi Module	0/1	0
ТРМ	0/(N/A)	1
RTC	0/1	1
Force Recov	0/1	1

1.3.3 Processor System

CPU	Std. Freq.	Max. Turbo Freq.	Cores	Cache (MB)	TDP (W)
Pentium® N6415	1.2 GHz	3.0 GHz	4	1.5	6.5
Atom® x6211E	1.3 GHz	3.0 GHz	2	1.5	6
Atom® x6413E	1.5 GHz	3.0 GHz	4	1.5	9
Atom® x6425E	2.0 GHz	3.0 GHz	4	1.5	12
Atom® x6425RE	1.9 GHz	NA	4	1.5	12

1.3.4 Memory

Dual channels on board, LPDDR4 3200MT/s up to 16GB, up to 4267MT/s by specific SPU SKUs (non-ECC).

1.3.5 Graphics/Audio

Graphics Core: Intel® Gen10 UHD/P630 Graphics supports DX12, OGL5.0, OCL2.1, and MPEG2, HEVC/H265, VC1/WMV9 HW decode/encode/transcode acceleration.

CPU	Graphics Core	Base Freq.	Max Freq.
Pentium® N6415	Gen10 UHD Graphics	350 MHz	800 MHz
Atom® x6211E	Gen10 UHD Graphics	350 MHz	750 MHz
Atom® x6413E	Gen10 UHD Graphics	500 MHz	750 MHz
Atom® x6425E	Gen10 UHD Graphics	500 MHz	750 MHz
Atom® x6425RE	Gen10 UHD Graphics	400 MHz	NA

1.3.6 Expansion Interface

1.3.6.1 PCle x1

PCI Express x1: Supports default 4 x PCIe x1 ports that are compliant with PCIe Gen3 (8.0 GT/s) specifications, and configurable to PCIe x4 or PCIe x2 upon request. Several configurable combinations may need BIOS modifications. Please contact Advantech sales or FAE for more details.

1.3.7 ESPI

2 x eSPI to Carrier Board (ESPI_CS0#, ESPI_CS1#), 1 x eSPI to EC.

1.3.8 Serial Bus

1.3.8.1 SMBus

Supports SMBus 2.0 specifications.

1.3.8.2 I2C Bus

Supports I2C bus 7-bit and 10-bit address modes, up to 400 kHz.

1.3.9 I/O

1.3.9.1 Gigabit Ethernet

Ethernet: Marvell 88E1512 Gigabit LAN supports 10/100/1000 Mbps speed; supports TSN via specific SKUs.

1.3.9.2 SATA

Supports 1 x SATA 3.0 (6.0 Gb/s).

1.3.9.3 USB 3.2 / USB 2.0

2 x USB 3.2 (10.0 Gbps) and 6 x USB 2.0 (480 Mbps, including 1 client port) which are backward compatible with USB 1.

1.3.9.4 USB 3.2

SMARC	P0	P1		
SoC	P0	P1		
SMARC		USB_0_1_OC		
SoC USB_OC#	OC_0#			

1.3.9.5 USB 2.0

SMARC	P0	P1	P2	P3	P4	P5
SoC	P0	P1	P2	P3	P4	P5
SMARC		USB0_EN_OC USB1_EN_OC	l l	JSB2_EN_OC JSB3_EN_OC		USB4_EN_OC USB5_EN_OC
SoC USB_OC#		OC_0#		OC_2#		OC_3#

1.3.9.6 HDA

Supports HD-Audio and LPE Audio for DDI[1:0] (DisplayPort and HDMI), 1.8V signal level, up to 24 MHz serial data clock.

1.3.9.7 Audio I2S

From EHL SOC I2S port 2 (follows CRB, Supports Linux only). Only supports the ALC5660 codec.

1.3.9.8 SPI Bus

Supports Master SPI operation only. SPI clock can be 50 MHz, 33 MHz, or 20 MHz, with capacity up to 16MB.

1.3.9.9 CAN Bus

Supports 2 x CAN-FD bus interfaces.

1.3.9.10 eMMC v5.1

HS400 DDR Mode. Supports transfer of data in 8-bit modes. Maximum HS400 Dual Rate 400 MB/s (200 MHz).

1.3.9.11 GPIO

14 x programmable general purpose Input or output (GPIO).

1.3.9.12 SDIO

Supports 1 x SDIO 3.0 interface.

1.3.9.13 TXE

Trusted Execution Engine 3.0 (TXE 3.0).

1.3.9.14 SMBus

SMBus 2.0 specifications. Supports SMBALERT# signal. Signal level 3.3V or 1.8V selectable.

1.3.9.15 TPM

Supports the TPM 2.0 module by default.

1.3.9.16 Watchdog

Supports multi-level watchdog time-out output. Provides 1-65535 levels, from 100ms- to 109.22-minute intervals.

1.3.9.17 Serial Ports

2 x 4-wire and 2 x 2-wire ports for the HSUART signal interface using RTS/CTS control only

- Programmable FIFO enable/disable
- 64B iDMA FIFO per channel with up to 32b burst capability
- Even, odd, or no parity bit selectable
- 1, 1.5, or 2 stop bit selectable

1.3.9.18 **BIOS**

The BIOS chip is on the module by default. This allows the user to place the BIOS chip on the carrier board with an appropriate design and a pull-down to GND on the BIOS_DISABLE# pin.

Notice: If the system CMOS is cleared, we strongly suggest going to the BIOS setup menu and loading the default settings during the first boot-up.

The standard module has no jumper at SCN1, so BIOS settings are kept without an RTC coin battery. If you need to restore to default BIOS settings, follow the steps below:



- 1. Remove the coin battery.
- 2. Put a jumper on SCN1 pins 1-2.
- 3. Turn on the power supply.
- 4. The system will boot up a few times.
- 5. BIOS will be loaded with the default settings.

1.3.10 Power Management

1.3.10.1 Power Supply

Supports both ATX and AT power modes. VSB is for suspending power and is optional if not required by standby (suspend-to-RAM) support. The RTC battery may be optional if keeping the time/date is not required.

- VCC: 5V +/- 5%
- VSB: 5V +/- 5% (suspend power)
- RTC Battery Power: 2.0V 3.3V

1.3.10.2 PWROK

Power OK monitors the main power supply. A high value indicates that the power is good. This signal can be used to hold off module startup and to allow carrier-based FPGAs or other configurable devices time to be programmed.

1.3.10.3 Power Sequence

According to SMARC 2.1 specifications.

1.3.10.4 Wake Events

Support for various wake-up events allows users to adapt to different scenarios.

- Wake-on-LAN (WOL): Wake to S0 from S3/S4
- **USB Wake:** Wake to S0 from S3/S4
- **PCIe Device Wake:** Depends on user inquiry and may need customized BIOS.

1.3.10.5 Advantech S5 ECO Mode (Deep Sleep Mode)

Advantech iManager provides additional features that allow the system to enter a very low suspended power mode – S5 ECO mode. In this mode, the module will cut all power, including suspend and active power, into the chipset and keep an on-module controller active. As such, less than 50mW of power will be consumed to extend the battery pack's lifespan. While this mode is enabled in BIOS, the system (or module) only supports power button boot and no other methods like WOL.

1.3.11 Environment

1.3.11.1 Temperature

Operating: 0 ~ 60°C (32 ~ 140°F) **Storage:** -40 ~ 85°C (-40 ~ 185°F) **Extended temperature:** -40 ~ 85°C (-40 ~ 185°F)

1.3.11.2 Humidity

Operating: 40°C (104°F) @ 95% relative humidity, non-condensing **Storage:** 60°C (140°F) @ 95% relative humidity, non-condensing

1.3.11.3 Vibrations

3.5G, 5~500Hz X/Y/Z Axis

1.3.11.4 Drop Test (Shock)

Federal Standard 101 Method 5007 test procedure with standard packing

1.3.11.5 EMC

CE EN55022 Class B and FCC Certifications: Validate with standard development boards in the Advantech chassis.

1.3.12 MTBF

Please refer to the Advantech SOM-2532 Series Reliability Prediction Report No: TBD. (Estimated date: 2021 Q4).

1.3.13 OS Support (Duplicated from the SW Chapter)

To install the drivers, please connect to the Internet and go to the following website: http://support.advantech.com.tw to download the setup file.

1.3.14 Advantech iManager

Supports APIs for GPIO, smart fan control, multi-stage watchdog timer, and output, temperature sensor, hardware monitor, etc. It follows PICMG EAPI 1.0 specifications to provide backward compatibility.

1.3.15 Power Consumption

Power Consumption Table (Watts)						
VSB=5V	Active	Power Domai	n	Mechanical Off		
Power State	S0 Max. Load	S0 Burn-in	S0 Idle	S5/G3RTC (uA)		
SOM-2532DCBC-U0A1	24.107 W	15.723 W	4.013 W	1.44/5.09		

Hardware Configurations:

- 1. MB: SOM-2532DCBC-U0A1
- 2. DRAM: 16GB DDR4 3200MHz
- 3. Carrier board: SOM-DB2500-00A1

Test Condition:

- 1. **Test temperature:** room temperature (about 25°C / 77°F)
- 2. **Test voltage:** rated voltage DC +5.0V
- 3. Test loading:
 - Maximum load mode: Running programs
 - Idle mode: DUT power management off and not running any programs
- 4. **OS:** Windows 10 Pro

1.3.16 Performance

For reference performance or benchmark data for comparison with other modules, please refer to the "Advantech COM Performance & Power Consumption Table".

1.3.17 Selection Guide with P/N

Part No.	CPU	Core	Graphics	Base Freq.	Max. Boost Freq.	GFX HFM	GFX Burst Mode	CPU TDP	Onboard Memory	ЕММС	IBECC	Thermal solution	Operating Temp.
SOM-2532CCBC- S9A1	Atom® x6425RE	4	32EU	1.9GHz	N/A	400MHz	N/A	12W	8GB	32GB	Yes	Passive	0~60°C
SOM-2532DCBC- U0A1	Atom® x6425E	4	32EU	2.0GHz	3.0GHz	500MHz	750MHz	12W	16GB	N/A	Yes	Passive	0~60°C
SOM-2532CCBC- U0A1	Atom® x6425E	4	32EU	2.0GHz	3.0GHz	500MHz	750MHz	12W	8GB	32GB	Yes	Passive	0~60°C
SOM-2532CCBC- S3A1	Atom® X6211E	2	16EU	1.3GHz	3.0GHz	350MHz	750MHz	6W	8GB	32GB	Yes	Passive	0~60°C
SOM-2532CCBX- S9A1	Atom® x6425RE	4	32EU	1.9GHz	N/A	400MHz	N/A	12W	8GB	32GB	Yes	Passive	-40 ~ 85°C
SOM-2532DCBX- U0A1	Atom® x6425E	4	32EU	2.0GHz	3.0GHz	500MHz	750MHz	12W	16GB	N/A	Yes	Passive	-40 ~ 85°C
SOM-2532CCBX- S3A1	Atom® X6211E	2	16EU	1.3GHz	3.0GHz	350MHz	750MHz	6W	8GB	32GB	Yes	Passive	-40 ~ 85°C

1.3.18 Packing list

Part No.	Description	Quantity
-	SOM-2532 COM module	1
1970005009N001/1970005010N001	Heatspreader IHS / Heatspreader NON-I	1

1.3.19 Development Board

Part No.	Description
SOM-DB2500	SMARC Development Board, SMARC 2.0 & 2.1 compliance

1.3.20 Optional Accessory

Part No.	Description
1970005111T001	Semi-heatsink

1.3.21 Pin Descriptions

Advantech provides useful checklists for schematic design and layout routing. The schematic checklist will specify details about each pin's electrical properties and how to connect them for different user scenes. The layout checklist will specify the layout constraints and recommendations for trace length, impedance, and other necessary information during design.

Please contact the nearest Advantech branch office to acquire the design documents and/or advanced support.



Mechanical Information

This chapter details mechanical information for the SOM-2532 CPU Computer-on-Module.

- Sections include:
- Board Information
- Mechanical Drawing
- Assembly Drawing

2.1 Board Information

The figures below show the main chips located on the SOM-2532 Computer-on-Module. Please be aware of their positions when designing carrier boards to avoid mechanical issues. It is advisable to select thermal solutions that optimize heat dissipation for optimal performance.



Figure 2.1 Board Chips ID — Front



Figure 2.2 Board Chips ID — Rear

2.2 Mechanical Drawing

For more details on 2D/3D models, please consult Advantech's COM support service website at <u>http://com.advantech.com</u>.



Figure 2.3 Atom® Series Board Mechanical Drawing - Front



Figure 2.4 Atom® Series Board Mechanical Drawing - Rear



Figure 2.5 Atom® Series Board Mechanical Drawing - Side



Figure 2.6 Celeron® Pentium® (J and N Series) Board Mechanical Drawing -Front



Figure 2.7 Celeron® Pentium® (J and N Series) Board Mechanical Drawing - Rear



Figure 2.8 Celeron® Pentium® (J and N Series) Board Mechanical Drawing - Side

2.3 Assembly Drawing

These figures demonstrate the assembly order of the thermal module — in particular the COM module and the carrier board.



Figure 2.9 Atom® Series Assembly Drawing



Figure 2.10 Celeron® Pentium® (J and N Series) Board Assembly Drawing There are 4 x reserved screw holes for SOM-2532. These are used to attach the heat spreader. Please consider the CPU and chip height tolerance when designing your thermal solution.



Intel® Atom® Series Processor Figure 2.11 Main Chip Height and Tolerance



Intel® Celeron® and Pentium® (N and J Series) Processors Figure 2.12 Main Chip Height and Tolerance



AMI BIOS

This chapter details BIOS setup information for the SOM-2532 CPU Computer-on Module.

- Sections include:
- Introduction
- Entering Setup
- Hot/Operation Key
- Exit BIOS Setup Utility

3.1 Introduction

AMI BIOS has been integrated into many motherboards for over a decade. With the AMI BIOS Setup Utility, users can modify BIOS settings and control various system features. This chapter describes the basic navigation of the BIOS Setup Utility.

Advanced	Aptio Setup – AMI	
CPU Configuration		When enabled, a VMM can
Type ID Speed L1 Data Cache L1 Instruction Cache L2 Cache L3 Cache	Intel(R) Pentium(R) J6425 @ 1.80GHz 0x90661 1800 MHz 32 KB x 4 32 KB x 4 1536 KB x 4 4 MB	hardware capabilities provided by Vanderpool Technology.
VMX	Supported	
Intel (VMX) Virtualization Technology Active Processor Cores	[Enabled]	<pre>++: Select Screen f↓: Select Item</pre>
AES MonitorMWait	[Enabled] [Enabled]	Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2	2.22.1282 Copyright (C) 2021	AMI

Figure 3.1 Setup Program Initial Screen

AMI's BIOS ROM has a built-in setup program that allows users to modify the basic system configuration. This information is stored in flash ROM to retain the setup information when power is turned off.

3.2 Entering Setup

Turn on the computer and then press or <ESC> to enter the setup menu.

3.2.1 Main Setup

When users enter the BIOS Setup Utility, they will enter the Main setup screen. Users can always return to the Main setup screen by selecting the Main tab. There are two Main setup options. They are described in this section. The Main BIOS setup screen is shown below.

Advanced	Aptio Setup – AMI	
CPU Configuration		When enabled, a VMM can
Type ID Speed L1 Data Cache L1 Instruction Cache L2 Cache L3 Cache VMX	Intel(R) Pentium(R) J6425 @ 1.80GHz 0x90661 1800 MHz 32 KB x 4 32 KB x 4 1536 KB x 4 4 MB Supported	hardware capabilities provided by Vanderpool Technology.
Intel (VMX) Virtualization Technology Active Processor Cores AES MonitorMWait	[Enabled] [All] [Enabled] [Enabled]	<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>

Figure 3.2 Main Setup Screen

The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

3.2.1.1 System Time / System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

3.2.2 Advanced BIOS Features Setup

Select the Advanced tab from the SOM-2532 setup screen to enter the Advanced BIOS Setup screen. Users can select any item in the left frame of the screen, such as CPU Configuration, to go to the sub-menu for that item. Users can display an Advanced BIOS setup option by highlighting it using the <Arrow> keys. All Advanced BIOS setup options are described in this section. The Advanced BIOS setup screens are shown below. The sub-menus are described on the following pages.



Figure 3.3 Advanced BIOS Features Setup Screen

- CPU Configuration
 CPU configuration parameters
- PCH-FW Configuration
 Intel® Time Coordinated Computing
- Trusted Computing
 Trusted computing settings
- ACPI Settings
 System ACPI parameters
- Embedded Controller Embedded controller parameters
- Serial Port Console Redirection Serial port console redirection
- USB Configuration
 USB configuration parameters
- Network Stack Configuration Network stack settings
- NVME Configuration
- SDIO Configuration
 SDIO configuration parameters
- SMARC GPIO Configuration

Chapter 3 AMI BIOS

3.2.2.1 CPU Configuration

CPU Configuration When enabled, a VMM can utilize the additional hardware capabilities provide by Vanderpool Technology. ID 0x90661 Speed 1800 MHz L1 Data Cache 32 KB × 4 L2 Cache 1536 KB × 4 L3 Cache 4 MB VMX Supported Intel (VMX) Virtualization [Enabled] rechnology Free Select Item Active Processor Cores [All] MonitorMWait [Enabled] HoritorMWait [Enabled] File General Help File General Help File General Help File Save & Exit	Advanced	Aptio Setup – AMI	
TypeIntel(R) Pentium(R) J6425 @ 1.80GHzhardware capabilities provide by Vanderpool Technology.ID0x90661Speed1800 MHzL1 Data Cache32 KB x 4L1 Instruction Cache32 KB x 4L2 Cache1536 KB x 4L3 Cache4 MBVMXSupportedIntel (VMX) Virtualization[Enabled]Technology(A11)Active Processor Cores[A11]AES[Enabled]MonitorMWait[Enabled]F1: General HelpF2: Previous ValuesF3: Optimized DefaultsF4: Save & Exit	CPU Configuration		When enabled, a VMM can
Intel (VMX) Virtualization [Enabled] Technology ++: Select Screen Active Processor Cores [All] AES [Enabled] MonitorMWait [Enabled] Enter: Select Item F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit	Type ID Speed L1 Data Cache L1 Instruction Cache L2 Cache L3 Cache VMX	Intel(R) Pentium(R) J6425 @ 1.80GHz 0x90661 1800 MHz 32 KB x 4 32 KB x 4 1536 KB x 4 4 MB Supported	hardware capabilities provided by Vanderpool Technology.
ESC: Exit	Intel (VMX) Virtualization Technology Active Processor Cores AES MonitorMWait	[Enabled] [A11] [Enabled] [Enabled]	<pre> ++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2.21.1278 Copyright (C) 2021 AMI Figure 3 4 CPU Configuration			

Speed

Displays the processor speed

Intel (VMX) Virtualization Technology When enabled, a VMM can utilize additional hardware capabilities provided by Vanderpool Technology.

Active Processor Cores

Number of cores to enable in each processor package.

AES

Enable/Disable AES (Advanced Encryption Standard).

MonitorMwait

Enable/Disable Monitor Mwait.

3.2.2.2 PCH-FW Configuration



Figure 3.5 PCH-FW Configuration

- ME State When Disabled, ME will be put into ME Temporarily Disabled Mode.
 ME Unconfig on RTC Clear
 - When Disabled, ME will not be unconfigured on RTC clear.
- Firmware Update Configuration Configure management engine technology parameters.
- OEM Key Revocation Configuration Configure OEM key revocation.

3.2.2.3 Firmware Update Configuration

Me FW Image Re-Flash [Disabled] Enable/Disable Me FW Image FW Update [Enabled] Re-Flash function. ++: Select Screen 11: Select Item Enter: Select tem Flash enter: Select tem FI: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit	Advanced	Aptio Setup — AMI	
++: Select Screen ++: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit	Me FW Image Re-Flash FW Update	[Disabled] [Enabled]	Enable/Disable Me FW Image Re-Flash function.
ESU: EXIT			<pre>++: Select Screen f↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>

Figure 3.6 Firmware Update Configuration

ME FW Image Re-Flash

Enable/Disable the Me FW Image Re-Flash function.

FW Update

Enable/Disable the Me FW Update function.

3.2.2.4 Intel® Time Coordinated Computing

Advanced	Aptio Setup — AMI	
Advanced Intel(R) Time Coordinated Computing Intel(R) TCC Mode Affected Settings ID Fabric Low Latency GT CLOS C states Intel(R) Speed Shift Technology Intel(R) SpeedStep(tm) ACPI D3Cold Support Low Power SO Idle Capability SA GV Page Close Idle Timeout RAPL PL 1 enable RAPL PL 2 enable Power Down Mode RC6(Render Standby) Legacy ID Low Latency PCH TSN GBE Multi-Vc PSE TSN GBE 0 Multi-Vc PSE TSN GBE 1 Multi-Vc PCI Express Root Port 1 ASPM	[Disabled] [Disabled]	Enable or Disable ID Fabric Low Latency. This will turn off some power management in the PCH ID fabrics. This option provides the most aggressive ID Fabric performance setting. S3 state is NOT supported. ++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Figure 3.7 Intel® Time Coordinated Computing

IO Fabric Low Latency

Enable or Disable IO Fabric Low Latency. This will turn off some power management in the PCH IO fabrics. This option provides the most aggressive IO Fabric performance setting. S3 state is NOT supported.

GT CLOS

Enable or Disable Graphics Technology (GT) Class of Service. Enable will reduce Gfx LLC allocation to minimize impact of Gfx workload on LLC.

C states

Enable/Disable CPU power management. Allows the CPU to go to C states when it's not 100% utilized.

Inte® Speed Shift Technology

Enable/Disable Intel® speed shift technology support. Enabling will expose the CPPC v2 interface to allow for hardware-controlled P-states

Intel® Speedstep®

Allows more than two frequency ranges to be supported.

ACPI D3Cold Support

Enable/Disable ACPI D3Cold (RTD3) support.

Low Power SO Idle Capability

This variable determines if we enable ACPI lower power S0 idle capability (mutually exclusive with smart connect). While this is enabled, it also disables the 8254 timer for SLP_S0 support.

SA GV

System agent geyserville. It can be disabled, fixed to a specific point, or enabled for frequency switching.

Page Close Idle Timeout

Page Close Idle Timeout Control
RAPL PL1 enable	
Enable=enable, Disable (Disable=Def)	

- RAPL PL2 enable
 Enable=enable, Disable (Disable=Def)
- Power Down Mode
 CKE power down mode control.
- RC6 (Render standby)
 Check to enable render standby support.

Legacy IO Low Latency

Set to enable low latency of legacy IO. Some systems require lower IO latency irrespective of power. This is a tradeoff between power and IO latency.

PCH TSN GBE Multi-Vc Enable/Disable TSN Multi Virtual Channels.

PSE TSN GBE 0 Multi-Vc

Enable/Disable TSN Multi Virtual Channels. TSN GBE must not be host owned.

PSE TSN GBE 1 Multi-Vc

Enable/Disable TSN multi virtual channels. TSN GBE must not be host owned.

DMI Link ASPM Control

The control of Active State Power Management of the DMI Link.

Aptio Setu Advanced	D - AMI
▶ L1 Substates ▶ PTM	▲ Enable/Disable Multi Virtual Channel.
PCI Express Root Port 2 > ASPM > L1 Substates > PTM	
PCI Express Root Port 3 > ASPM > L1 Substates > PTM	
PCI Express Root Port 4 ▶ ASPM ▶ L1 Substates ▶ PTM	<pre>++: Select Screen 1↓: Select Item Enter: Select +/-: Change Opt. E1: Ceneral Help</pre>
PCI Express Root Port 5 ASPM L1 Substates PTM Multi-VC	F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
۲ Version 2.22.1282 Cop	yright (C) 2021 AMI

Figure 3.8 Intel® Time Coordinated Computing

ASPM

Set the ASPM Level

- Force L0s Force all links to the L0s State
- AUTO BIOS auto-configure
- DISABLE Disable ASPM

L1 Substates

PCI Express L1 Substates settings.

PTM

Enable/Disable Precision Time Measurement

Multi-VC

Enable/Disable Multi Virtual Channel.

3.2.2.5 Trusted Computing

Advanced	Aptio Setup — AMI		
TPM 2.0 Device Found Firmware Version: Vendor:	7.62 IFX	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and	
Security Device Support Active PCR banks Available PCR banks	[Enable] SHA256 SHA-1,SHA256	INT1A interface will not be available.	
SHA-1 PCR Bank SHA256 PCR Bank Pending operation	(Disabled) (Enabled) (None)		
Platform Hierarchy Storage Hierarchy Endorsement Hierarchy TPM 2.0 UEFI Spec Version Physical Presence Spec Version TPM 2.0 InterfaceType Device Select	[Enabled] [Enabled] [Enabled] [TCG_2] [1.3] [TIS] [Auto]	<pre>++: Select Screen tl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>	
Version 2.21.1278 Copyright (C) 2021 AMI			
Figure 2.0 Tructed Computing			

Figure 3.9 Trusted Computing

Security Device Support

Enables or disables BIOS support for a security device. The OS will not show the security device. TCG EFI protocol and INT1A interface will not be available

SHA-1 PCR Bank

Enable or disable SHA-1 PCR Bank.

SHA256 PCR Bank

Enable or disable SHA256 PCR Bank.

Pending Operation

Schedules an operation for the security device. Note: Your computer will reboot during restart in order to change the state of the security device.

Platform Hierarchy

Enable or disable platform hierarchy.

Storage Hierarchy

Enable or disable storage hierarchy.

Endorsement Hierarchy

Enable or disable endorsement hierarchy.

TPM 2.0 UEFI Spec version

Select the TCG2 spec version support, TCG_1_2: the compatible mode for Win8/Win10, TCG_2: Supports new TCG2 protocol and event format for Win10 or later.

Physical Presence Spec Version

Select to tell the OS to support PPI Spec Version 1.2 or 1.3. Note: some HCK tests might not support 1.3.

TPM 2.0 Interface Type

Select the communication interface for a TPM 2.0 device.

Device Select

TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices. If not found, TPM 1.2 devices will be enumerated.

3.2.2.6 ACPI Settings



Figure 3.10 ACPI Settings

Enable ACPI Auto Configuration

Enables or disables BIOS ACPI Auto Configuration.

Enable Hibernation

Enables or disables the system ability to hibernate (OS/S4 sleep state). This option may not be effective with some OS.

ACPI Sleep State

Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.

3.2.2.7 Embedded Controller



Figure 3.11 Embedded Controller

- CPU Shutdown Temperature
 CPU Shutdown Temperature.
- Smart Fan Carrier Board Control Carrier Board Smart FAN function. It gets the value from EC and only sets the value when saving changes.
- Backlight Enable Polarity
 Switch Backlight Enable Polarity to native or invert.
- Brightness PWM Polarity
 Backlight Control Brightness PWM Polarity for native or invert.
- Serial Port 1 Configuration
 Set Parameters of Serial Port 1 (COMA).
- Serial Port 2 Configuration Set Parameters of Serial Port 2 (COMB).
- Hardware Monitor
 Monitor hardware status.

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3.2.2.8 Serial Port 1 Configuration



Figure 3.12 Serial Port 1 Configuration

Serial Port

Enable or disable Serial Port (COM).

- Device Settings Set Parameters of Serial Port 1 (COMA).
- Change Settings
 Select optimal settings for a Super IO Device.
- Device Mode
 Change the serial port mode.

3.2.2.9 Serial Port 2 Configuration



Figure 3.13 Serial Port 2 Configuration

- Serial Port Enable or disable Serial Port (COM).
- Device Settings Set parameters of Serial Port 2 (COMB).
- Change Settings
 Select optimal settings for a Super IO Device.
- Device Mode
 Change the serial port mode.

3.2.2.10 Hardware Monitor

Advanced	Aptio Setup – AMI	
PC Health Status		
CPU temperature	: +32°C	
Carrier Board FAN	: N/A	
+VBAT +Vin	: +2.868 V : +4.938 V	
		<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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Figure 3.14 Hardware Monitor

3.2.2.11 Serial Port Console Redirection

	Advanced	Aptio Setup – AMI	
►	COMO Console Redirection Console Redirection Settings	[Disabled]	Console Redirection Enable or Disable.
•	COM1 Console Redirection Console Redirection Settings	[Disabled]	
Þ	COM2(Pci Bus0,Dev30,Func0,Port0) Console Redirection Console Redirection Settings	[Disabled]	
Þ	COM3(Pci Bus0,Dev25,Func2,Port0) Console Redirection Console Redirection Settings	[Disabled]	++: Select Screen †↓: Select Item Enter: Select +/-: Change Opt.
Þ	Serial Port for Out-of-Band Managemen Windows Emergency Management Services Console Redirection EMS Console Redirection Settings	t∕ : (EMS) [Disabled]	F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit
			ESC: EXIT
	Version 2.	21.1278 Copyright (C) 2021	AMI

Figure 3.15 Serial Port Console Redirection

COM0

Console Redirection

Enable or disable Console Redirection.

Console Redirection Settings

The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

COM1

Console Redirection

Enable or disable Console Redirection.

Console Redirection Settings

The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

COM2

Console Redirection

Enable or disable Console Redirection.

Console Redirection Settings

The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

COM3

Console Redirection

Enable or disable Console Redirection.

Console Redirection Settings

The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

Serial Port for Out-of-Band Management / Windows Emergency Management Services (EMS)

Console Redirection EMS

Enable or disable Console Redirection.

Console Redirection Settings

The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

3.2.2.12 USB Configuration

USB Configuration		Enables Legacy USB support.
USB Module Version 25	5	AUTU option disables legacy support if no USB devices are connected. DISABLE option will
USB Controllers: 1 XHCI		keep USB devices available only for EFI applications.
USB Devices: 1 Drive, 1 Keyboard, 1 Mouse, 1 H	łub	
Legacy USB Support [E XHCI Hand-off [E	Enabled] Enabled]	
USB Mass Storage Driver Support [E	Enabled]	
USB hardware delays and time-outs:		++: Select Screen
USB transfer time-out [2 Dewice paget time out	20 sec] 20 sec]	T↓: Select Item
Device nower-up delau [4	Autol	+/-: Change Ont.
		F1: General Help
Mass Storage Devices:		F2: Previous Values
SKYMEDI USB Drive [f	Auto]	F3: Optimized Defaults
		F4: Save & Exit
		ESU: EXIT
Version 2.21	1.1278 Conuright (C) 2021	AMT

Figure 3.16 USB Configuration

Legacy USB Support

Enables Legacy USB support. The AUTO option disables legacy support if no USB devices are connected. The DISABLE option will keep USB devices available only for EFI applications.

XHCI Hand-off

This is a workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI driver.

 USB Mass Storage Driver Support Enable/Disable USB Mass Storage Driver Support.

USB transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers.

Device reset time-out

USB mass storage device Start Unit command time-out.

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller.

'Auto' uses the default value: for a Root port it is 100 ms, for a Hub port the delay is taken from the Hub descriptor.

Device power-up delay in seconds

The delay range is 1~40 seconds, in one-second increments.

3.2.2.13 Network Stack Configuration



Figure 3.17 Network Stack Configuration

Network Stack

Enable/Disable UEFI Network Stack.

IPv4 PXE support

Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

IPv4 HTTP Support

Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.

IPv6 PXE Support

Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

IPv6 HTTP Support

Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.

PXE boor wait time

Wait time in seconds to press the ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

Media detect count

Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

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3.2.2.14 SDIO Configuration

Advanced	Aptio Setup –	AMI
SDIO Configuration		Auto Option: Access SD device
SDIO Access Mode	[Auto]	supports it,otherwise in PIO
Mass Storage Devices:		device in DMA mode.PIO Option: Access SD device in PIO mode.
Bus 0 Dev 1A Func 0 eMMC S0J57X(31.8GB)	[Auto]	
		++: Select Screen ↑↓: Select Item
		Enter: Select +/-: Change Opt.
		F1: General Help F2: Previous Values F3: Optimized Defaults
		F4: Save & Exit ESC: Exit
Version 2.21.1278 Copyright (C) 2021 AMI		
Figure 3.18 SDIO Configuration		

SDIO Access Mode

Auto Option: Access an SD device in DMA mode if the controller supports it, otherwise it will be in PIO mode. DMA Option: Access an SD device in DMA mode. PIO Option: Access SD device in PIO mode. eMMC S0J57X

3.2.2.15 SMARC GPIO Configuration

Advanced	Aptio Setup – AMI	
SMARC GPIO Configuration		SMARC GPIOO
GPI00 GPI01 GPI02 GPI03 GPI04 GPI05 GPI06	[GPO LOW] [GPO LOW] [GPO LOW] [GPO LOW] [HDA_RST#] [Disabled] [Disabled]	<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Versio	n 2.21.1278 Copyright (C) 2021	L AMI

Figure 3.19 Network Stack Configuration

GPIO0

SMARC GPIO0

- GPIO1 SMARC GPIO1
- GPIO2
 SMARC GPIO2
- GPIO3
 SMARC GPIO3
- GPIO4 SMARC GPIO4
- GPIO5SMARC GPIO5
- GPIO6
 SMARC GPIO6

3.2.3 Chipset Setup

Select the chipset tab from the SOM-2532 setup screen to enter the chipset BIOS setup screen. You can display a chipset BIOS setup option by highlighting it using the <Arrow> keys. All Plug and Play BIOS setup options are described in this section. The Plug and Play BIOS Setup screen is shown below.

Aptio Setup – AMI Main Advanced <mark>Chipset</mark> Security Boot Save & Exit	
▶ System Agent (SA) Configuration ▶ PCH-IO Configuration	System Agent (SA) Parameters
	<pre>++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2.21.1278 Copyright (C) 2021	AMI

Figure 3.20 Chipset Setup

- System Agent (SA) Configuration System Agent Parameters
- PCH-IO Configuration PCH parameters

3.2.3.1 System Agent (SA) Configuration



Figure 3.21 System Agent (SA) Configuration

Memory Configuration

Memory configuration Parameters

VT-d

VT-d capability

Above 4GB MMIO BIOS assignment

Enable/Disable above-4GB memory mapped IO BIOS assignment. This is enabled automatically when the aperture size is set to 2048MB.

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Memory Configuration

Chipset	Aptio Setup – AMI	
Memory Configuration		Maximum Value of TOLUD.
Memory RC Version Memory Frequency	0.0.4.104 3200 MTPS	adjust TOLUD automatically based on largest MMIO length of installed graphic controller
Channel O Slot O Size Number of Ranks Manufacturer Channel 1 Slot O Size Number of Ranks Manufacturer	Populated & Enabled 8192 MB 2 2C00 Populated & Enabled 8192 MB 2 2C00	
Max TOLUD		<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2.21.1278 Copyright (C) 2021 AMI		
Figure 3.22 Memory Configuration		

- Max TOLUD

Maximum value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on the largest MMIO length of the installed graphics controller.

Graphics Configuration

Chipset	Aptio Setup – AMI	
Graphics Configuration		Keep IGFX enabled based on the setup options.
Internal Graphics GTT Size	(Auto) [8MB]	
Aperture Size DVMT Pre-Allocated	[256MB] [60M]	
DVMT Total Gfx Mem ▶ LCD Control	[256M]	
		++: Select Screen
		I∔: Select Item Enter: Select
		+/-: Change opt. F1: General Help
		F3: Optimized Defaults
		ESC: Exit
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Figure 3.23 Graphics Configuration

Internal Graphics

Keep IGFX enabled based on the setup options.

- GTT Size Select the GTT size.
- Aperture Size

Select the aperture size. Note: Above 4GB, MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM support.

- DVMT Pre-Allocated Select DVMT5.0 pre-allocated (fixed) graphics memory size as used by the internal graphics device.
- DVMT Total Gfx Mem

```
Select DVMT5.0 total graphics memory size as used by the internal graphics device.
```

LCD Control



Figure 3.24 LCD Control

- NXP non-EDID Support
 NXP PTN3460 Support. Enable: Use internal EDID setting; Disable: Get EDID from the DDC bus
- Color depth and packing format
- Dual LVDS mode
- LCD panel type Select the LCD panel used by the internal graphics device by selecting the appropriate setup item.
- LVDS clock spreading
- LVDS swing level
- Primary IGFX Boot Display
 Select the video device which will be activated during POST. This has no

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effect if external graphics are present. The secondary boot display selection will appear based on your selection. VGA modes will be supported only on the primary display.

- Panel Scaling
 Select the LCD panel scaling option used by the internal graphics device.
- Panel color depth Select the LFP panel color depth.

3.2.3.2 PCH-IO Configuration

Chipset	Aptio Setup – AMI	
PCH-IO Configuration > PCI Express Configuration > SATA Configuration > USB Configuration > Security Configuration > HD Audio Configuration > SerialIo Configuration > SCS Configuration > PSE Configuration > TSN GBE Configuration		PCI Express Configuration settings
State After G3 Enable VNN Voltage Raise Pcie Pll SSC Flash Protection Range Registers (FPRR) SPD Write Disable	[S5 State] [Disabled] [Auto] [Enabled] [TRUE]	<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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Figure 3.25 PCH-IO Configuration		

- PCI Express Configuration PCI Express Configuration settings
- SATA Configuration
 SATA device option settings
- USB Configuration
 USB Configuration settings
- Security Configuration Security Configuration settings
- HD Audio Configuration
 HD audio subsystem configuration settings
- Serial I/O Configuration Serial I/O configuration settings
- SCS Configuration
 Storage and communication subsystem configuration
- PSE Configuration
 Programmable service engine configuration
- TSN GBE Configuration
 Time sensitive network GBE configuration

PCI Express Configuration

Chipset	Aptio Setup – AMI	
PCI Express Configuration		The control of Active State
DMI Link ASPM Control PCIE Port assigned to LAN Compliance Test Mode	[Disabled] Disabled [Disabled]	Fower Management of the DMI Link.
 PCI Express Root Port 1 PCI Express Root Port 2 PCI Express Root Port 3 PCI Express Root Port 4 		
		<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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Figure 3.26 PCI Express Configuration

- DMI Link ASPM Control
 - The control of Active State Power Management of the DMI Link.
- Compliance Test Mode
 Compliance Mode Enable/Disable.
- PCI Express Root Port 1 Controls the PCI Express Root Port. AUTO: To disable unused root port auto
 - matically for optimal power savings. Enable: Enable PCIe root port; Disable: Disable PCIe root port.
- PCI Express Root Port 2 Control the PCI Express Root Port. AUTO: To disable unused root port automatically for optimal power savings. Enable: Enable PCIe root port; Disable: Disable PCIe root port.
- PCI Express Root Port 3 Control the PCI Express Root Port. AUTO: To disable unused root port automatically for optimal power savings. Enable: Enable PCIe root port; Disable: Disable PCIe root port.
- PCI Express Root Port 4 Control the PCI Express Root Port. AUTO: To disable unused root port automatically for optimal power savings. Enable: Enable PCIe root port; Disable: Disable PCIe root port.

Chipset	Aptio Setup — AMI	
PCI Express Root Port 1 ASPM Hot Plug PCIe Speed	[Enabled] [Disabled] [Disabled] [Gen3]	Control the PCI Express Root Port.
		<pre>++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Figure 2.27 DOL Express Doct Dort 1		
Figure 3.27 PGI Express Root Port 1		

- PCI Express Root Port 1 Control the PCI Express Root Port. AUTO: To disable unused root port automatically for optimal power savings. Enable: Enable PCIe root port; Disable: Disable PCIe root port.
- ASPM
 - PCI Express Active State Power Management settings.
- PCle Speed Configure PCle Speed.

Chipset	Aptio Setup – AMI	
PCI Express Root Port 2 ASPM Hot Plug PCIe Speed	[Enabled] [Disabled] [Disabled] [Gen3]	Control the PCI Express Root Port. ++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Vers	100 2.21.1278 Cupgright (C)	

Figure 3.28 PCI Express Root Port 2

- PCI Express Root Port 2 Control the PCI Express Root Port. AUTO: To disable unused root port automatically for optimal power savings. Enable: Enable PCIe root port; Disable: Disable PCIe root port.
- ASPM
 - PCI Express Active State Power Management settings.
- Hot Plug
 PCI Express hot plug enable/disable.
- PCIe Speed Configure PCIe Speed.

Chipset	Aptio Setup – AMI	
PCI Express Root Port 3 ASPM Hot Plug PCIe Speed	[Enabled] [Disabled] [Disabled] [Gen3]	Control the PCI Express Root Port.
		++: Select Screen f4: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Figure 3.29 PCI Express Root Port 3

- PCI Express Root Port 3 Control the PCI Express Root Port. AUTO: To disable an unused root port automatically for optimal power savings. Enable: Enable PCIe root port; Disable: Disable PCIe root port.
- ASPM.
 - PCI Express Active State Power Management settings.
- Hot Plug

PCI Express hot plug enable/disable.

 PCIe Speed Configure PCIe speed.

Chipset	Aptio Setup – AMI	
PCI Express Root Port 4 ASPM Hot Plug PCIe Speed	[Enabled] [Disabled] [Disabled] [Gen3]	Control the PCI Express Root Port. ++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults
		F4: Save & Exit ESC: Exit
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Figure 3.30 PCI Express Root Port 4

- PCI Express Root Port 4 Control the PCI Express Root Port. AUTO: To disable an unused root port automatically for optimal power savings. Enable: Enable PCIe root port; Disable: Disable PCIe root port
- ASPM.
 - PCI Express Active State Power Management settings.
- Hot Plug PCI Express hot plug enable/disable.
- PCIe Speed Configure PCIe Speed.

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SATA Configuration

Chipset	Aptio Setup – AMI	
SATA Configuration		Enable/Disable SATA Device.
SATA Controller(s) SATA Controller Speed	[Enabled] [Default]	
Serial ATA Port 1 Software Preserve Port 1 Hot Plug	Empty Unknown [Enabled] [Disabled]	
		<pre> ++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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- SATA Controller(s) Enable/Disable SATA Device.
- SATA Controller Speed Indicates the maximum speed the SATA controller can support.
- SATA Port 1
- Port 1

Enable or disable SATA Port.

 Hot plug PCI Express hot plug enable/disable.

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USB Configuration



Figure 3.32 USB Configuration

- XHCI Disable Compliance Mode
 Options to disable Compliance Mode. Default is False which does not disable compliance Mode. Set to TRUE to disable compliance Mode.
- XDCI Support Enable/Disable XDCI.

Security Configuration

Chipset	Aptio Setup – AMI	
Security Configuration		Enable will lock bytes 38h-3Fh
RTC Memory Lock BIOS Lock	[Enabled] [Enabled]	bank of RTC RAM
		<pre> ++: Select Screen 1↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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Figure 3.33 Security Configuration

RTC Memory Lock

Enable will lock bytes 38h-3Fh in the lower/upper 126–byte bank of RTC RAM.

BIOS Lock

Enable/Disable the PCH BIOS lock enable feature. Required to be enabled to ensure SMM protection of flash.

HD Audio Subsystem Configuration Settings Aptio Setup - AMI Chipset HD Audio Subsystem Configuration Settings Control Detection of the HD-Audio device. Disabled = HDA will be Audio DSP [Disabled] unconditionally disabled Enabled = HDA will be unconditionally enabled. ++: Select Screen †↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit



- HD Audio

Control Detection of the HD-Audio device. Disabled=HDA will be unconditionally disabled. Enabled=HAD will be unconditionally enabled.

- Audio DSP Enable/Disable Audio DSP.

Serial I/O Configuration

Chipset	Aptio Setup – AMI	
SerialIo Configuration I2CO Controller I2C2 Controller I2C3 Controller I2C4 Controller UARTO Controller UART2 Controller UART2 Controller Serial IO I2C0 Settings Serial IO I2C3 Settings Serial IO I2C4 Settings Serial IO SPI1 Settings Serial IO UART0 Settings Serial IO UART0 Settings	[Enabled] [Enabled] [Enabled] [Enabled] [Enabled] [Enabled]	Enables/Disables SerialIo Controller If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PGI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device. The following devices depend **: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Figure 3.35 Serial I/O Configuration

I2C0 controller

Enables/Disables serial I/O controller. If a given device is function0, PSF disabling is skipped. PSF default will remain and device PCI CFG space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device.

I2C2 controller

Enables/Disables serial I/O controller. If a given device is function0, PSF disabling is skipped. PSF default will remain and device PCI CFG space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device.

I2C3 controller

Enables/Disables serial I/O controller. If a given device is function0, PSF disabling is skipped. PSF default will remain and device PCI CFG space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device.

I2C4 controller

Enables/Disables serial I/O controller. If a given device is function0, PSF disabling is skipped. PSF default will remain and device PCI CFG space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device.

- UART0 controller

Enables/Disables serial I/O controller. If a given device is function0, PSF disabling is skipped. PSF default will remain and device PCI CFG space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device.

UART2 controller

Enables/Disables serial I/O controller. If a given device is function0, PSF disabling is skipped. PSF default will remain and device PCI CFG space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device.

- Serial I/O I2C0 Settings

Chipset	Aptio Setup — AMI	
Serial IO I2CO Settings		Select Serial IO I2C #O Speed
Set Serial IO I2C #0 Speed Timing parameters StandardSpeed SCL High StandardSpeed SCL Low StandardSpeed SDA Hold FastSpeed SCL Low FastSpeed SDA Hold FastSpeedPlus SCL High FastSpeedPlus SCL Low FastSpeedPlus SDA Hold HighSpeed SCL High HighSpeed SCL Low HighSpeed SCL Low HighSpeed SCL Low HighSpeed SCL Low HighSpeed SCL Low HighSpeed SCL Low HighSpeed SCL and HighSpeed SCL High HighSpeed SCL High HighSpeed SCL I SC HighSpeed SCL I SC HighSpeed SC I SC HighSpeed SC I SC SC I SC HighSpeed SC I SC	[Fast Mode] 429 495 30 81 153 30 9 16 11 8 200 2000	<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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Figure 3.36 Serial I/O I2C0 Settings

 Set Serial I/O I2C #0 Speed Select serial I/O I2C#0 speed.

Chapter 3 AMI BIOS

- Serial I/O I2C2 Settings

Chipset	Aptio Setup – AMI	
Serial IO I2C2 Settings		Indicates what type of I2C Touch Panel is connected to
▶ Serial IO Touch Panel Settings		this SerialIo controller
Set Serial IO I2C #2 Speed	[Fast Mode]	
StandardSneed SCL High	429	
StandardSpeed SCL Low	495	
StandardSpeed SDA Hold	30	
FastSpeed SCL High	81	
FastSpeed SCL Low	153	
FastSpeed SDA Hold	30	
FastSpeedPlus SCL High	9	
FastSpeedPlus SCL Low	16	++: Select Screen
FastSpeedPlus SDA Hold	11	↑↓: Select Item
HighSpeed SCL High	8	Enter: Select
HighSpeed SCL Low	16	+/-: Change Opt.
HighSpeed SDA Hold	8	F1: General Help
DO->D3 idle timeout (screen off)	200	F2: Previous Values
DO–>D3 idle timeout (screen on)	2000	F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
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VEI S1011	E.EI.IETO COPYLIGHT (C) 200	- 1 1111

Figure 3.37 Serial I/O I2C2 Settings

 Set Serial I/O I2C #2 Speed Select serial I/O I2C#2 speed.

- Serial I/O I2C3 Settings

Chipset	Aptio Setup — AMI	
Serial IO I2C3 Settings		Select Serial IO I2C #3 Speed
Set Serial IO I2C #3 Speed Timing parameters StandardSpeed SCL High StandardSpeed SCL Low StandardSpeed SDA Hold FastSpeed SCL Low FastSpeed SDA Hold FastSpeed SDA Hold FastSpeedPlus SCL Low FastSpeedPlus SCL Low FastSpeedPlus SDA Hold HighSpeed SCL High HighSpeed SCL Low HighSpeed SDA Hold DO->D3 idle timeout (screen off) DO->D3 idle timeout (screen on)	[Fast Mode] 429 495 30 81 153 30 9 16 11 8 16 8 200 2000	<pre>++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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 Set Serial I/O I2C #3 Speed Select serial I/O I2C#3 speed.

- Serial I/O I2C4 Settings

Chipset	Aptio Setup — AMI	
Serial IO I2C4 Settings Set Serial IO I2C #4 Speed Timing parameters StandardSpeed SCL High StandardSpeed SCL Low StandardSpeed SCL Low FastSpeed SCL High FastSpeed SCL Low FastSpeed Plus SCL High FastSpeedPlus SCL Low FastSpeedPlus SCL Low FastSpeedPlus SCL Low FastSpeedPlus SCL Low HighSpeed SCL High HighSpeed SCL Low HighSpeed SCL High D0->D3 idle timeout (screen off) D0->D3 idle timeout (screen on)	[Fast Mode] 429 495 30 81 153 30 9 16 11 8 16 8 200 2000 2000	Select Serial IO I2C #4 Speed ++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Figure 3.39 Serial I/O I2C4 Settings

 Set Serial I/O I2C #4 Speed Select serial I/O I2C#4 speed.

Chapter 3 AMI BIOS

- Serial I/O SPI1 Settings

Chipset	Aptio Setup – AMI	
Serial IO SPI1 Settings ChipSelect O polarity ChipSelect 1 polarity Delayed Rx Clock Chip Select O Chip Select 1	[Active High] [Active High] [As Is] [Enabled] [Enabled]	Sets initial polarity for ChipSelect signal
Timing parameters DO→D3 idle timeout (screen off) DO→D3 idle timeout (screen on)	200 2000	
		<pre>++: Select Screen f↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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Figure 3.40 Serial I/O SPI1 Settings

- Chipselect 0 polarity
 Sets the initial polarity for chipselect signal.
- Chipselect 1 polarity
 Sets the initial polarity for chipselect signal.
- Delayed Rx Clock
 Configure the SPI delayed Rx clock option: As is –Default internal-Internally delayed Tx Clock-Negative edge of Tx clock Rx Clock-Negative edge of the delayed Ex clock.
- Chip Select0

This enables the SPI device for testing purposes. This option has dependency on the WITT device. If the WITT device is enabled with SPI, this option will be grayed out.

Chip Select1

This enables the SPI device for testing purposes. This option has dependency on the WITT device. If the WITT device is enabled with SPI, this option will be grayed out.

- SCS Configuration

Chipset	Aptio Setup — AMI	
eMMC 5.1 Controller eMMC 5.1 HS400 Mode Enable HS400 software tuning Driver Strength eMMC 5.1 DDR50 Mode SDCard 3.0 Controller	(Enabled) [Enabled] [Disabled] [40 Ohm] [Disabled] [Enabled]	Enable or Disable SCS eMMC 5.1 Controller
		<pre>++: Select Screen f↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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- eMMC 5.1 Controller
 Enable/Disable SCS eMMC 5.1 Controller.
- eMMC 5.1 HS400 Mode
 Enable/Disable SCS eMMC 5.1 HS400 Mode.
- Enable HS400 software tuning Software tuning should improve eMMC HS400 stability at the expense of boot time.
- Driver Strength
 Sets I/O driver strength.
- eMMC 5.1 DDR50 Mode
 Enable/Disable SCS eMMC 5.1 DDR50 Mode.
- SDCard 3.0 Controller
 Enable/Disable SCS SDHC 3.0 Controller.

- Serial I/O UART0 Settings

Chipset	Aptio Setup – AMI	
Serial IO UARTO Settings Hardware Flow Control DMA Enable	[Enabled] [Enabled]	When enabled configures additional 2 GPIO pads for use as RTS/CTS signals for UART
Timing parameters DO->D3 idle timeout (screen off) DO->D3 idle timeout (screen on)	200 200	
		<pre> ++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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Figure 3.41 Serial I/O UART0 Settings

- Hardware flow control When enabled, it configures 2 additional GPIO pads for use as RTS/CTS signals for UART.
- DMA enable
 Enabled: UART OS driver will use DMA when possible. Disabled: OS driver will enforce PIO mode.

- Serial I/O UART2 Settings

Chipset	Aptio Setup — AMI	
Serial IO UART2 Settings Hardware Flow Control DMA Enable	[Disabled] [Enabled]	When enabled configures additional 2 GPIO pads for use as RTS/CTS signals for UART
Timing parameters DO->D3 idle timeout (screen off) DO->D3 idle timeout (screen on)	200 200	
		<pre>++: Select Screen f↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version	2.21.1278 Copyright (C) 2021	L AMI

Figure 3.42 Serial I/O UART2 Settings

- Hardware flow control When enabled, it configures 2 additional GPIO pads for use as RTS/CTS signals for UART.
- DMA enable
 Enabled: UART OS driver will use DMA when possible. Disabled: OS driver will enforce PIO mode.

PSE Controller

Chipset	Aptio Setup – AMI	
PSE Controller PSE DashBoard Configuration LOG OUTPUT CHANNEL LOG OUTPUT OFFSET LOG OUTPUT SIZE Shell Eclite CPU Temp Read OOB WoL PSE Debug (JTAG/SWD) Enable PSE JTAG/SWD PIN MUX PSE Add-In-Card PSE IP Ownership and GPIO Mux Assignment Configuration I2S0 PSE I2S0 PIN Assignment I2S1 PWM PMM Pin Mux Selection UARTO HSUARTO/RS485 UART1 HSUART1/RS485	[Enabled] 3 0 0 0 [Disabled] [Enabled] [Enabled] [Enabled] [Enabled] [Disabled] [Disabled] [Disabled] [Disabled] [Disabled] [Disabled] [Disabled] [None] [PSE owned with pin muxed] [None] [Non	 Enables/Disables Programmable Service Engine (PSE) Device **: Select Screen **: Select Item Enter: Select */-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Figure 3.43 PSE Controller

- PSE controller
 Enable/Disable programmable service engine device.
- Shell
 Enable/Disable shell.
- Eclite

Enable/Disable PSE Eclite service.

– OOB

Enable/Disable OOB service.

– WOL

Enable/Disable PSE GBE WoL.

- PSE Debug(JTAG/SWD)Enable
 PSE JTAG/SWD Debug enable.
- PSE Add-In-Card Enable/Disable PSE Add-In-Card.
- I2S0

I2S0 has pin conflict with CAN0, CAN1, TGPIO 14-17. I2S1 does not have conflict. If it is grayed out, check the above options. The same pin cannot be assigned to multiple IP.

- PSE I2S0 Pin assignment
 PSE I2S0 pin assignment. Choose I2S0 pin out to GPIO group E or group R.
- I2S1

I2S0 has pin conflict with CAN0, CAN1, TGPIO 14-17. I2S1 does not have conflict. If it is grayed out, check the above options. The same pin cannot be assigned to multiple IP.

- PWM

PWM has pin conflicts with UART3, SPI0, SPI1, I2C5 and TGPIO. If it is

grayed out, check the above options. The same pin cannot be assigned to multiple IP. I2S1 does not have a conflict.

- UART0

If UART0 is disabled, UART1-5 will be disabled also due to sharing the same function.

- HSUART0/RS485

Select this to enable UART to support HSUART/RS485. Each HSUART pin conflict dependency is similar to UART.

– UART1

To assign this device as host-owned, you must enable PSE UART0 to be host-owned because UART0 is the function0 of this device. UART0 has no pin conflict. UART1 has a pin conflict with TGPIO. UART2 is enabled by default for PSE logging purposes. UART3 has a conflict with GBE0-1, PWM, and TGPIO.

– HSUART1/RS485

Select this to enable UART to support HSUART/RS485. Each HSUART pin conflict dependency is similar to UART.

Chipset	Aptio Setup – AMI	
UART2	[PSE owned with pin	To assign this device to host
HSUART2/RS485	muxed) [PSE owned with pin muxed]	IZCO to host owned because
UART3	[None]	device.
HSUART3/RS485	[None]	I2C1 has pin conflict with
UART4	[None]	TGPI08-9
UART5	[None]	I2C2 has no pin conflict.
QEP0	[None]	1203 has pin conflict with
	[None]	16P1018-19.
	[None]	
12C0	[Host owned with nin	
1200	muxed]	++: Select Screen
T2C1	[Host owned with nin	14: Select Item
	muxed]	Enter: Select
12C2	[PSE owned with pin	+/-: Change Opt.
	muxed]	F1: General Help
12C3	I2C3 is not	F2: Previous Values
	configurable as it is	F3: Optimized Defaults
	shared with SMBUS	F4: Save & Exit
I2C4	[None]	ESC: Exit
1205	[None]	
12C6	[Host owned with pin	
	muxed]	•
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Figure 3.44 PSE Controller

UART2

To assign this device as host-owned, you must enable PSE UART0 to be hostowned because UART0 is the function0 of this device. UART0 has no pin conflict. UART1 has a pin conflict with TGPIO. UART2 is enabled by default for PSE logging purposes. UART3 has a conflict with GBE0-1, PWM, and TGPIO.

HSUART2/RS485

Select this to enable UART to support HSUART/RS485. Each HSUART pin conflict dependency is similar to UART.
UART3

UART3 has pin conflicts with GBE0-1, PWM, TGPIO, and the serial I/O controller. If it is grayed out, check the above options. The same pin cannot be assigned to multiple IP.

HSUART3/RS485

Select this to enable UART to support HSUART/RS485. Each HSUART pin conflict dependency is similar to UART.

UART4

To assign this device as host-owned, you must enable PSE UART0 to be hostowned because UART0 is the function0 of this device. UART0 has no pin conflict. UART1 has a pin conflict with TGPIO. UART2 is enabled by default for the purposes of PSE logging. UART3 has a conflict with GBE0-1, PWM, and TGPIO.

UART5

To assign this device as host-owned, you must enable PSE UART0 to be hostowned because UART0 is the function0 of this device. UART0 has no pin conflict. UART1 has a pin conflict with TGPIO. UART2 is enabled by default for PSE logging purposes. UART3 has conflicts with GBE0-1, PWM, and TGPIO.

QEP0

To assign this device as host-owned, you must enable PSE I2C7 to be hostowned because I2C7 is the function0 of this device. If it is grayed out, check the above options. The same pin cannot be assigned to multiple IP.

QEP1

To assign this device as host-owned, you must enable PSE I2C7 to be hostowned because I2C7 is the function0 of this device. If it is grayed out, check the above options. The same pin cannot be assigned to multiple IP.

QEP2

To assign this device as host-owned, you must enable PSE I2C7 to be hostowned because I2C7 is the function0 of this device. If it is grayed out, check the above options. The same pin cannot be assigned to multiple IP.

QEP3

To assign this device as host-owned, you must enable PSE I2C7 to be hostowned because I2C7 is the function0 of this device. If it is grayed out, check the above options. The same pin cannot be assigned to multiple IP.

12C0

If I2C0 is not set as host-owned, I2C 1-6 cannot be set as host-owned either due to sharing the same function.

I2C1

To assign this device as host-owned, you must enable PSE I2C0 to be hostowned because I2C0 is the function0 of this device. I2C1 has a pin conflict with TGPI08-9 and I2C2 has no pin conflict. I2C3 has a pin conflict with TGPI018-19. I2C4 has no pin conflict. I2C5 has a pin conflict with PWM. I2C6 has no pin conflict.

I2C2

Grayed out to be reserved for ECLite.

12C3

To assign this device as host-owned, you must enable PSE I2C0 to be hostowned because I2C0 is the function0 of this device. I2C1 has a pin conflict with TGPI08-9. I2C2 has no pin conflict. I2C3 has a pin conflict with TGPI018-19. I2C4 has no pin conflict. I2C5 has a pin conflict with PWM. I2C6 has no pin conflict.

I2C4

To assign this device as host-owned, you must enable PSE I2C0 to be hostowned because I2C0 is the function0 of this device. I2C1 has a pin conflict with TGPIO8-9. I2C2 has no pin conflict. I2C3 has a pin conflict with TGPIO18-19. I2C4 has no pin conflict. I2C5 has a pin conflict with PWM. I2C6 has no pin conflict.

I2C5

To assign this device as host-owned, you must enable PSE I2C0 to be hostowned because I2C0 is the function0 of this device. I2C1 has a pin conflict with TGPIO8-9. I2C2 has no pin conflict. I2C3 has a pin conflict with TGPIO18-19. I2C4 has no pin conflict. I2C5 has a pin conflict with PWM. I2C6 has no pin conflict.

I2C6

To assign this device as host-owned, you must enable PSE I2C0 to be hostowned because I2C0 is the function0 of this device. I2C1 has a pin conflict with TGPIO8-9. I2C2 has no pin conflict. I2C3 has a pin conflict with TGPIO18-19. I2C4 has no pin conflict. I2C5 has a pin conflict with PWM. I2C6 has no pin conflict.

Chipset	Aptio Setup — AMI	
1207	[PSE owned with pin muxed]	▲ Enable individual GPIO/TGPIO
SPIO	[None]	
SPI1	[None]	
SPI2	[None]	
SPI3	[None]	
CANO	[None]	
CAN1	[None]	
DMAO	[PSE owned with pin muxed]	
DMA1	[PSE owned with pin muxed]	
DMA2	[PSE owned with pin muxed]	
GBE0	[Host owned with pin muxed]	↑↓: Select Item Enter: Select
PSE GBEO DLL Override	[Disabled]	+/-: Change Opt.
GBE1	[Host owned with pin	F1: General Help
	muxed]	F2: Previous Values
PSE GBE1 DLL Override	[Disabled]	F3: Optimized Defaults
GPIO/TGPIO O	[PSE owned with pin muxed]	F4: Save & Exit ESC: Exit
GPIO/TGPIO O MUX SELECTION	[All pins are GPIO]	
▶ GPIO/TGPIO O Pin Selection		
		T
Uppelor	2 21 1270 Conunight (C) 202	21 ANT
VENSION	гелет.тело соругтупс (с) 202	

Figure 3.45 PSE Controller

I2C7

If I2C7 is not set as host-owned, all PSE CAN and QEP devices cannot be set as host-owned too due to sharing the same function. I2C7 cannot be assigned as host-owned if UCSI ACPI devices are enabled.

SPI0

SPI0 has a pin conflict with PWM pin3, TGPIO pin10-13 and 39, serial SPI2. If it is grayed out, check the above options. The same pin cannot be assigned to

multiple OP. If SPI0 is not set as host-owned, SPI1-3 cannot be set as host-owned either, due to sharing the same function.

SPI1

To assign this device as host-owned, you must enable PSE SPI0 to be hostowned because SPI0 is the function0 of this device. SPI0 has a pin conflict with PWM, TGPI010-13, 39, and Serial I/O SPI2. SPI1 has a pin conflict with PWM and TGPIO 32-35. SPI2 has a pin conflict with Serial I/O SPI0.

SPI2

SPI2 has a pin conflict with WWAN WAKE GPIO. If it is grayed out, check the WWAN Wake GPIO configuration or Serial I/O SPI0. The same pin cannot be assigned to multiple IP.

SPI3

To assign this device as host-owned, you must enable PSE SPI0 to be hostowned because SPI0 is the function0 of this device. SPI0 has a pin conflict with PWM, TGPI010-13, 39, and Serial I/O SPI2. SPI1 has a pin conflict with PWM and TGPI0 32-35. SPI2 has a pin conflict with Serial I/O SPI0.

CAN0

To assign this device as host-owned, you must enable PSE I2C7 to be hostowned because I2C7 is the function0 of this device. CAN0 has a pin conflict with I2S0 and TGPIO 16-17. CAN1 has a pin conflict with I2S0 and TGPIO 14-15. If it is grayed out, check the above options.

CAN1

To assign this device as host-owned, you must enable PSE I2C7 to be hostowned because I2C7 is the function 0 of this device. CAN0 has pin conflict with I2S0 and TGPIO 16-17. CAN1 has a pin conflict with I2S0 and TGPIO 14-15. If it is grayed out, check the above options.

DMA0

This DMA device is reserved for PSE firmware loading, thus it is always grayed out.

DMA1

Select ownership for DMA.

DMA2

Select ownership for DMA.

GBE0

Select ownership for GBE.

PSE GBE0 DLL Override

Enable/Disable PSE GBE0 DLL. To enable this, GBE0 must be enabled.

PSE GBE1 DLL Override

Enable/Disable PSE GBE1 DLL. To enable this, GBE1 must be enabled.

GPIO/TGPIO 0 MUX SELECTION

Choose top, mid, lower, or all mux for GPIO/TGPIO 0 controller instance. Lower: TGPIo(0-19), GPIO(20-29) Mid: TGPIO(0-9, 20-29), GPIO(10-19) Top:TGPIO(10-29) GPIO(0-9) All:GPIO(0-29)

Chipset	Aptio Setup – AMI	
GPIO/TGPIO 1	[PSE owned with pin muxed]	Checked = Interrupt set to SB mode. Default unchecked is MSI
GPI0/IGPI0 1 MOX SELECTION	(AII pins are GPIU)	mode.
PSE Interrupt Assignment		
Configuration		
1280	[Disabled]	
I2S1	[Disabled]	
	[Disabled]	
UART1	[Disabled]	
UART2	[Disabled]	
UART3	[Disabled]	
UART4	[Disabled]	++: Select Screen
UART5	[Disabled]	T∔: Select Item
HSUARTU HSUART1	[Disabled]	Enter: Select
HSUART2	[Disabled]	F1: General Help
HSUART3	[Disabled]	F2: Previous Values
QEPO	[Disabled]	F3: Optimized Defaults
QEP1	[Disabled]	F4: Save & Exit
QEP2	[Disabled]	ESC: Exit
QEP3	[Disabled]	
1200	[Disabled]	
	[D13db1cd]	

Figure 3.46 PSE Controller

GPIO/TGPIO1

Owner of GPIO/TGPIO 1 controller(PSE or HOST owned)

GPIO/TGPIO 1 Mux selection

Choose Top, Mid, Lower, or all mux for GPIO/TGPIO 1 controller instance. Lower: TGPIO(30-49) GPIO(50-59) Mid: TGPIO(30-39, 50-59)GPIO(40-49) Top: TGPIO(40-59) GPIO(30-39) All:GPIO(30-59)

GPIO/TGPIO 1 Pin selection

Enable individual GPIO/TGPIO pin.

PSE Interrupt assignment configuration

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **I2S0**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **I2S1**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **PWM**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **UART0**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **UART1**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **UART2**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **UART3**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode.

UART4

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **UART5**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **HSUART0**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **HSUART1**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **HSUART2**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **HSUART3**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **QEP0**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **QEP1**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **QEP2**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **QEP3**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **I2C0**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **I2C1**

Checked=Interrupt set to SB mode. Default unchecked is MSI mode.

Chipset	Aptio Setup – AMI	
Chipset QEP3 I200 I201 I202 I203 I204 I205 I206 I207 SPI0 SPI1 SPI2 SPI3 DMA0 DMA1 DMA2 LH2PSE CAN0 CAN1 Delaued Ry Clock SPI0	Aptio Setup - AMI [Disabled]	 Enable/Disable DMA test Device ++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Evit
Delayed Rx Clock SPI0	3	ESC: Exit
Delayed Rx Clock SPI2	3	
Delayed Rx Clock SPI3 DMA Test	3 [Disabled]	•
	Version 2.22.1282 Copyright (C)	2021 AMI

Figure 3.47 PSE Controller

QEP2

Checked=Interrupt set to SB mode. Default unchecked is MSI mode. QEP3 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. 12C0 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. 12C1 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. 12C2 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. 12C3 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. 12C4 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. 12C5 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **I2C6** Checked=Interrupt set to SB mode. Default unchecked is MSI mode. 12C7 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. SPI0 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. SPI1 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. SPI2 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. SPI3 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. DMA0 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. DMA1 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. DMA2 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. LH2PSE Checked=Interrupt set to SB mode. Default unchecked is MSI mode. CAN0 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. CAN1 Checked=Interrupt set to SB mode. Default unchecked is MSI mode. **DMA** test Enable/Disable DMA test device. **PSE I2C Test Device** Enable PSE I2C WITT device and select which controllers use it. **PSE SPI Test Device** Enable PSE SPI WITT device and select which controllers use it.

PSE UARTT Test Device

Enable the PSE UARTT test device and select which controllers use it.

TSN GBE configuration

Chipset	Aptio Setup — AMI	
PCH TSN LAN Controller PCH TSN GBE Multi-Vc PCH TSN GBE SGMII Support PCH TSN Link Speed Flex IO Lane Assignment: PSE TSN GBE 0 Multi-Vc	[Disabled] [Disabled] [Enabled] [RefClk 38.4Mhz 1Gbps] None [Disabled]	Enable∕Disable TSN LAN.
PSE ISN GBE O SGMII Support. PSE TSN GBE O Link Speed PSE TSN GBE 1 Multi-Vc PSE TSN GBE 1 SGMII Support	[Disabled] [RefClk 38.4Mhz 1Gbps] [Disabled] [Disabled]	
PSE TSN GBE 1 Link Speed	[RefClk 38.4Mhz 1Gbps]	<pre>++: Select Screen fl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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Figure 3.48 TSN GBE configuration

- PCH TSN LAN Controller Enable/Disable TSN LAN.
- PCH TSN GBE Multi-Vc Enable/Disable TSN Multi Virtual Channels.
- PCH TSN GBE SGMII Support Enable/Disable SGMII mode for PCH TSN GBE. Ports in SGMII mode with the same PLL common lane must use the same link speed. SATA or UFS may need to be disabled if the TSN port is using the same PLL common lane. Please make sure IFWI has proper straps set for SGMII. Make sure Flex IO Lane Assignment is not NONE.
- PCH TSN Link Speed
 PCH TSN Link Speed configuration.
- PCH TSN GBE 0 Multi-Vc Enable/Disable TSN Multi Virtual Channels. TSN GBE must be host owned.
- PSE TSN GBE 0 SGMII Support Enable/Disable Modphy support for SGMII mode for PSE TSN GBE 0. Ports in SGMII mode with the same PLL common lane must use the same link speed. UFS will need to be disabled as this TSN port uses the same PLL common lane. Please make sure IFWI has proper straps set for SGMII. Make sure Flex IO Lane Assignment is not NONE.
- PSE TSN GBE 0 Link Speed
 PSE TSN GBE 0 Link Speed configuration.
- PSE TSN GBE 1 Multi-Vc Enable/Disable TSN Multi Virtual Channels. TSN GBE must be host owned.

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- PSE TSN GBE 1 SGMII Support

Enable/Disable Modphy support for SGMII mode for PSE TSN GBE 1. Ports in SGMII mode with the same PLL common lane must use the same link Speed. SATA or UFS may need to be disabled if TSN port is using the same PLL common lane. Please make sure IFWI has proper straps set for SGMII. Make sure Flex IO Lane Assignment is not NONE.

PSE TSN GBE 1 Link Speed
 PSE TSN GBE 1 Link Speed configuration.

3.2.4 Security Chipset



- Administrator Password
 Set the administrator password.
- User Password Set the user password.
- Secure Boot Secure boot configuration.

Boot Setup

Main Advanced Chipset Se	Aptio Setup – AMI ecurity <mark>Boot</mark> Save & Exit	
Boot Configuration Setup Prompt Timeout Bootup NumLock State Quiet Boot	<mark>1</mark> [Off] [Disabled]	Number of seconds to wait for setup activation key. 65535(OxFFFF) means indefinite waiting.
Boot Option Priorities Boot Option #1 Fast Boot	[UEFI: SKYMEDI USB Drive, Partition 1 (SKYMEDI USB Drive)] [Disabled]	
		<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
1	/ersion 2.21.1278 Copyright (C) 202	21 AMI

Figure 3.50 Boot Setup

Boot Configuration

- Setup Prompt Timeout Number of seconds to wait for the setup activation key. 65535(0xFFFF) means indefinite waiting.
- Bootup NumLock State
 Select the keyboard NumLock state.
- Quiet Boot Enables or disables the Quiet Boot option.
- Boot Option Priorities
 Boot Option #1
 Sets the system boot order.
- Fast Boot

Enable or Disable FastBoot features. Most probes are skipped to reduce time spent during boot.

3.2.5 Save & Exit

Aptio Setup – AMI Main Advanced Chipset Security Boot <mark>Save & Exit</mark>	
Save Options Save Changes and Exit Discard Changes and Reset Discard Changes and Reset Save Changes Discard Changes Default Options Restore Defaults Save as User Defaults Restore User Defaults Boot Override UEFI: SKYMEDI USB Drive, Partition 1 (SKYMEDI USB Drive)	Exit system setup after saving the changes. ++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Figure 3.51 Save & Exit

- Save Options
- Save Changes and Exit
 Exit system setup after saving the changes.
- Discard Changes and Exit
 Exit system setup without saving any changes.
- Save Changes and Reset Reset the system after saving the changes.
- Discard Changes and Reset Reset system setup without saving any changes.
- Default Options
- Restore Defaults Restore/Load default values for all the setup options.
- Save as User Defaults
 Save the changes done so far as User Defaults.
- Restore User Defaults
 Restore the User Defaults to all the setup options.
- Boot Override



S/W Introduction and Installation

- S/W Introduction
- Driver Installation
- Advantech iManager (SUSI 4)

4.1 S/W Introduction

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft Windows embedded technology". We enable Windows Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows Embedded Software solutions easily and widely available to the embedded computing community.

*Elkhart Lake doesn't support AFU Windows flash.

4.2 Driver Installation

The Intel® Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured.

4.2.1 Windows Driver Setup (TBD)

To install the drivers on a windows-based operating system, please connect to the Internet and go to the website http://support.advantech.com.tw to download the drivers that you want to install and follow the Driver Setup instructions to complete the installation.

4.2.2 Other OS

Linux Ubuntu 18.04.1 Windows 10 IoT Core Linux Wind River 64-bit VxWorks (7.0) *If you need the CAN bus function, please enter Linux-intel-iot-Its-5.15-kernel.

4.3 Advantech iManager (SUSI 4.0)

Advantech's platforms come equipped with iManager, a micro controller that provides embedded features for system integrators. Embedded features have been moved from the OS/BIOS level to the board level, to increase reliability and simplify integration.

iManager runs whether the operating system is running or not; it can count the boot times and running hours of the device, monitor device health, and provide an advanced watchdog to handle errors just as they happen. iManager also comes with a secure & encrypted EEPROM for storing important security key or other customerdefined information. All the embedded functions are configured through API and provide corresponding utilities to demonstrate. These APIs comply with PICMG EAPI (Embedded Application Programmable Interface) specifications and are unified in the same structures. It makes these embedded features easier to integrate, speeds up development schedules, and provides customers with software continuity while upgrading hardware. For more details of how to use the APIs and utilities, please refer to the Advantech iManager 2.0 Software API User Manual.

Control



General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch on/off a device. Our API also provides Programmable GPIO, which allows developers to dynamically set the GPIO input or output status.



SMBus is the System Management Bus defined by Intel® Corporation in 1995. It is used in personal computers and servers for low-speed system management communications The SMBus API allows a developer to interface a embedded system environment and transfer serial messages using the SMBus protocols, allowing multiple simultaneous device control



^{IP}C is a bi-directional two wire bus that was developed by Philips for use in their televisions in the 1980s. The ^{IP}C API allows a developer to interface with an embedded system environment and transfer serial messages using the ^{IP}C protocols, allowing multiple simultaneous device control.

Display

Brightness

The Brightness Control API allows a developer to interface with an embedded device to easily control brightness.



The Backlight API allows a developer to control the backlight (screen) on/off in an embedded device.

Monitor



A watchdog timer (WDT) is a device that performs a specific operation after a certain period of time if something goes wrong and the system does not recover on its own. A watchdog timer can be programmed to perform a warm boot (restarting the system) after a certain number of seconds.



The Hardware Monitor (HWM) API is a system health supervision API that inspects certain condition indexes, such as fan speed, temperature and voltage.



The Hardware Control API allows developers to set the PVMM (Pulse Width Modulation) value to adjust fan speed or other devices; it can also be used to adjust the LCD brightness.

Power Saving



Make use of Intel SpeedStep technology to reduce power power consumption. The system will automatically adjust the CPU Speed depending on system loading.



Refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. These APIs allow the user to lower the clock from 87.5% to 12.5%.

Throttling



Pin Assignments

This appendix provides you with information about the hardware pin assignments for the SOM-2532 CPU System-on-Module.

Sections include: ■ SOM-2532 Pin Assignments

A.1 SOM-2532 Pin Assignments

This section shows the SOM-2532 pin assignments on the SMARC connector which is compliant with SMARC 2.0 definitions. Please contact Advantech for a design guide, checklist, reference schematic, hardware/software, and/or detailed information.

SMARC Function	Pin	Pin Name	SOM-2532
	S125	LVDS0_0+ / eDP0_TX0+ /DSI0_D0+	v /v/v
	S126	LVDS0_0- / eDP0_TX0- /DSI0_D0-	v /v/v
	S128	LVDS0_1+ / eDP0_TX1+ /DSI0_D1+	v /v/v
	S129	LVDS0_1- / eDP0_TX1- /DSI0_D1-	v /v/v
	S131	LVDS0_2+ / eDP0_TX2+ /DSI0_D2+	v /v/v
	S132	LVDS0_2- / eDP0_TX2- /DSI0_D2-	v /v/v
	S137	LVDS0_3+ / eDP0_TX3+ /DSI0_D3+	v /v/v
	S138	LVDS0_3- / eDP0_TX3- /DSI0_D3-	v /v/v
	S134	LVDS0_CK+ / eDP0_AUX+ /DSI0_CLK+	v /v/v
	S135	LVDS0_CK- / eDP0_AUX- /DSI0_CLK-	v /v/v
	S111	LVDS1_0+ / eDP1_TX0+ /DSI1_D0+	v / -/-
	S112	LVDS1_0- / eDP1_TX0- /DSI1_D0-	v / -/-
	S114	LVDS1_1+ / eDP1_TX1+ /DSI1_D1+	v / -/-
	S115	LVDS1_1- / eDP1_TX1- /DSI1_D1-	v / -/-
	S117	LVDS1_2+ / eDP1_TX2+ /DSI1_D2+	v / -/-
	S118	LVDS1_2- / eDP1_TX2- /DSI1_D2-	v / -/-
	S120	LVDS1_3+ / eDP1_TX3+ /DSI1_D3+	v / -/-
	S121	LVDS1_3- / eDP1_TX3- /DSI1_D3-	v / -/-
	S108	LVDS1_CK+ / eDP1_AUX+ /DSI1_CLK+	v / -/-
	S109	LVDS1_CK- / eDP1_AUX- /DSI1_CLK-	v / -/-
	S139	I2C_LCD_CK	v
	S140	I2C_LCD_DAT	v
	S133	LCD0_VDD_EN	v
	S116	LCD1_VDD_EN	v
	S127	LCD0_BKLT_EN	v
	S107	LCD1_BKLT_EN	v
	S141	LCD0_BKLT_PWM	v
	S122	LCD1_BKLT_PWM	v
	S144	EDP0_HPD / DSI0_TE	v/v
	S113	EDP1_HPD	v

	P92	DP1_LANE0+ / HDMI_D2+	v/v
	P93	DP1_LANE0- / HDMI_D2-	v/v
	P95	DP1_LANE1+ / HDMI_D1+	v/v
	P96	DP1_LANE1- / HDMI_D1-	v/v
	P98	DP1_LANE2+ / HDMI_D0+	v/v
	P99	DP1_LANE2- / HDMI_D0-	v/v
	P101	DP1_LANE3+ / HDMI_CK+	v/v
	P102	DP1_LANE3- / HDMI_CK-	v/v
	P104	DP1_HPD / HDMI_HPD	v/v
	P105	DP1_AUX+/HDMI_CTRL_CK	v/v
	P106	DP1_AUX-/HDMI_CTRL_DAT	v/v
	P107	DP1_AUX_SEL	v
	S102	DP0_LANE3+	v
	S103	DP0_LANE3-	v
	S99	DP0_LANE2+	v
	S100	DP0_LANE2-	v
	S96	DP0_LANE1+	v
	S97	DP0_LANE1-	v
DFTT	S93	DP0_LANE0+	v
	S94	DP0_LANE0-	v
	S105	DP0_AUX+	v
	S106	DP0_AUX -	v
	S98	DP0_HPD	v
	S95	DP0_AUX_SEL	v

	P108	GPIO0 / CAM0_PWR#	v/-
	P109	GPIO1 / CAM1_PWR#	v/-
	P110	GPIO2 / CAM0_RST#	v/-
	P111	GPIO3 / CAM1_RST#	v/-
	S7	I2C_CAM0_DAT	-
	S5	I2C_CAM0_CK	-
	S2	I2C_CAM1_DAT	-
	S1	I2C_CAM1_CK	-
	S11	CSI0_RX0+	-
	S12	CSI0_RX0-	-
	S14	CSI0_RX1+	-
	S15	CSI0_RX1-	-
CSI	P7	CSI1_RX0+	-
	P8	CSI1_RX0-	-
	P10	CSI1_RX1+	-
	P11	CSI1_RX1-	-
	P13	CSI1_RX2+	-
	P14	CSI1_RX2-	-
	P16	CSI1_RX3+	-
	P17	CSI1_RX3-	-
	S8	CSI0_CK+	-
	S9	CSI0_CK-	-
	P3	CSI1_CK+	-
	P4	CSI1_CK-	-
	S6	CAM_MCK	-
	P39	SDIO_D0	v
	P40	SDIO_D1	v
	P41	SDIO_D2	v
	P42	SDIO_D3	v
SDIO Card	P33	SDIO WP	v
	P36	SDIO_CK	v
	P34	SDIO CMD	v
	P35	SDIO_CD#	v
	P37	SDIO_PWR_EN	v
	P43	SPI0_CS0#	v
	P31	SPI0_CS1#	v
SPI0	P44	SPI0_CK	v
	P45	SPI0_DIN	v
	P46	SPI0_DO	V

	P56	ESPI_CK / SPI1_ CK / QSPI_CK	v / -/-
	P54	ESPI_CS0# / SPI1_CS0# / QSPI_CS0#	v / -/-
	P55	ESPI_CS1# / SPI1_CS1# / QSPI_CS1#	v / -/-
	P57	ESPI_IO_1 / SPI1_DIN / QSPI_IO_1	v / -/-
	P58	ESPI_IO_0 / SPI1_DO /QSPI_IO_0	v / -/-
6371/3711	S56	ESPI_IO_2 / QSPI_IO_2	v / -
	S57	ESPI_IO_3 / QSPI_IO_3	v / -
	S58	ESPI_RESET#	v
	S43	ESPI_ALERT0#	v
	S44	ESPI_ALERT1#	v
	S39	I2S0_LRCK	v
	S40	I2S0_SDOUT	v
12S	S41	I2S0_SDIN	v
	S42	I2S0_CK	v
	S38	AUDIO_MCK	v
	S50	HDA_SYNC / I2S2_LRCK	v / -
	S51	HDA_SDO / 12S2_SDOUT	v / -
HDA / I2S	S52	HDA_SDI / I2S2_SDIN	v / -
	S53	HDA_CK / I2S2_CK	v / -
	P112	HDA_RST#	v
12C Interfaces	S48	I2C_GP_CK	v
12C Interfaces	S49	I2C_GP_DAT	v
	P129	SER0_TX	v
	P130	SER0_RX	v
	P134	SER1_TX	v
	P135	SER1_RX	v
	P136	SER2_TX	v
Sorial Ports	P137	SER2_RX	v
	P140	SER3_TX	v
	P141	SER3_RX	v
	P131	SER0_RTS#	v
	P132	SER0_CTS#	v
	P138	SER2_RTS#	v
	P139	SER2_CTS#	v
	P143	CAN0_TX	v
CAN BUS	P145	CAN1_TX	v
CAN Bus	P144	CAN0_RX	v
	P146	CAN1_RX	v
-			

	1		
	P60	USB0+	v
	P61	USB0-	v
	P65	USB1+	v
	P66	USB1-	v
	P69	USB2+	v
	P70	USB2-	v
	S68	USB3+	v
	S69	USB3-	v
	S35	USB4+	v
	S36	USB4-	v
	S59	USB5+	v
	S60	USB5-	v
	P62	USB0_EN_OC#	v
	P67	USB1_EN_OC#	v
	P71	USB2_EN_OC#	v
036	P74	USB3_EN_OC#	v
	P76	USB4_EN_OC#	v
	S55	USB5_EN_OC#	v
	P63	USB0_VBUS_DET	v
	S37	USB3_VBUS_DET	v
	P64	USB0_OTG_ID	v
	S104	USB3_OTG_ID	v
	S75	USB2SSRX-	v
	S74	USB2SSRX+	v
	S66	USB3SSRX-	v
	S65	USB3SSRX+	v
	S72	USB2SSTX-	v
	S71	USB2SSTX+	v
	S63	USB3SSTX-	v
	S62	USB3SSTX+	v

	P89	PCIE_A_TX+	v
	P90	PCIE_A_TX-	v
	S90	PCIE_B_TX+	v
	S91	PCIE_B_TX-	v
	S81	PCIE_C_TX+ / SERDES_1_TX+	v / v
	S82	PCIE_C_TX- / SERDES_1_TX-	v / v
	S29	PCIE_D_TX+ / SERDES_0_TX+	v / v
	S30	PCIE_D_TX- / SERDES_0_TX-	v / v
	P86	PCIE_A_RX+	v
	P87	PCIE_A_RX-	v
	S87	PCIE_B_RX+	v
	S88	PCIE_B_RX-	v
DCIa	S78	PCIE_C_RX+ / SERDES_1_RX+	v / v
PCIE	S79	PCIE_C_RX- / SERDES_1_RX	v / v
	S32	PCIE_D_RX+ / SERDES_0_RX+	v / v
	S33	PCIE_D_RX- / SERDES_0_RX-	v / v
	P83	PCIE_A_REFCK+	v
	P84	PCIE_A_REFCK-	v
	S84	PCIE_B_REFCK+	v
	S85	PCIE_B_REFCK-	v
	P80	PCIE_C_REFCK+	v
	P81	PCIE_C_REFCK-	v
	P75	PCIE_A_RST#	v
	S76	PCIE_B_RST#	v
	S77	PCIE_C_RST#	v
	S146	PCIE_WAKE#	v
	P48	SATA_TX+	v
	P49	SATA_TX-	v
SATA	P51	SATA_RX+	v
	P52	SATA_RX-	v
	S54	SATA_ACT#	v

	P30	GBE0_MDI0+	v
	P29	GBE0 MDI0-	v
	P27	GBE0 MDI1+	v
	P26	GBE0_MDI1-	v
	P24	GBE0_MDI2+	v
	P23	GBE0_MDI2-	v
	P20	GBE0_MDI3+	v
	P19	GBE0_MDI3-	v
	S17	GBE1_MDI0+	v
	S18	GBE1_MDI0-	v
	S20	GBE1_MDI1+	v
	S21	GBE1_MDI1-	v
Ethorpot	S23	GBE1_MDI2+	v
	S24	GBE1_MDI2-	v
	S26	GBE1_MDI3+	v
	S27	GBE1_MDI3-	v
	P21	GBE0_LINK100#	v
	S19	GBE1 LINK100#	v
	P22	GBE0_LINK1000#	v
	S22	GBE1_LINK1000#	v
	P25	GBE0_LINK_ACT#	v
	s31	GBE1_LINK_ACT#	v
	P28	GBE0_CTREF	v
	S28	GBE1_CTREF	-
	P6	GBE0_SDP	-
	P5	GBE1_SDP	-
Watchdog	S145	WDT_TIME_OUT#	v
	P108	GPIO0 / CAM0_PWR#	v / -
	P109	GPIO1 / CAM1_PWR#	v / -
	P110	GPIO2 / CAM0_RST#	v / -
	P111	GPIO3 / CAM1_RST#	v / -
	P112	GPIO4 / HDA_RST#	v / v
	P113	GPIO5 / PWM_OUT	v / v
GPIO	P114	GPIO6 / TACHIN	v / v
	P115	GPIO7	v
	P116	GPIO8	v
	P117	GPIO9	v
	P118	GPIO10	v
	P119	GPIO11	v
	S142	GPIO12	v
	S123	GPIO13	v

	S150	VIN PWR BAD#	v
	S154	CARRIER PWR ON	v
	S153	CARRIER STBY#	v
	P126	RESET OUT#	v
	P127	RESET IN#	v
	P128	POWER BTN#	v
	S149	SLEEP#	v
Management Pins	S148	LID#	v
······································	S156	BATLOW#	v
	P122	I2C PM DAT	v
	P121	12C PM CK	v
	S151	CHARGING#	v
	S152	CHARGER PRSNT#	v
	S157	TEST#	v
	P1	SMB ALERT	v
	P123	BOOT SEL0#	-
	P124	BOOT SEL1#	-
Boot Select	P125	BOOT SEL2#	v
	S155	FORCE RECOV#	v
	S147		v
	P147		v
	P148		v
	P149		v
	P150		v
	P151		v
	P152		v
	P153		v
	P154		v
	P155		v
	P156		v
	P2	GND	v
	P9	GND	v
	P12	GND	v
Power / GND /RSVD	P12	GND	v
	P15	GND	v
	P18	GND	v
	P32	GND	v
	P38	GND	v
	P47	GND	v
	P50	GND	v
	P53	GND	v
	P59	GND	v
	P68	GND	v
	P79	GND	v
	P82	GND	v
	P85	GND	v
	P88	GND	v
L	i		

	P91	GND	v
	P94	GND	v
	P97	GND	v
	P100	GND	v
	P103	GND	v
	P120	GND	v
	P133	GND	v
	P142	GND	v
	S3	GND	v
	S10	GND	v
	S13	GND	v
	S16	GND	v
	S25	GND	v
	S34	GND	v
	S47	GND	v
	S61	GND	v
	S64	GND	v
	S67	GND	v
	S70	GND	v
	S73	GND	v
	S80	GND	V
Power / GND /RSVD	S83	GND	V
	S86	GND	V
	S89	GND	v
	S92	GND	v
	S101	GND	v
	S110	GND	v
	S119	GND	v
	S124	GND	v
	S130	GND	v
	S136	GND	v
	S143	GND	v
	S158	GND	v
	P72	RSVD	NC
	P73	RSVD	NC
	P77	RSVD	NC
	P78	RSVD	NC
	S4	RSVD	NC
	S45	RSVD	NC
	S46	RSVD	NC
	S123	RSVD	NC
	S142	RSVD	NC
	-	VDD_JTAG_IO	NC
	-	JTAG_TRST#	NC
	-	JTAG_TMS	NC
JIAG	-	JTAG_TDO	NC
	-	JTAG_TDI	NC
	-	JTAG_TCK	NC



Watchdog Timer

This appendix details information about programming the watchdog timer on the SOM-2532 CPU System-on-Module.

Sections include:

■ Watchdog Timer Programming

B.1 Programming the Watchdog Timer

Trigger Event Note		
IRQ	(BIOS setting default disable)**	
NMI	N/A	
SCI	Power button event	
Power Off	Support	
H/W Restart	Support	
WDT Pin Activate	Support	

** WDT new driver support automatically selects an available IRQ number from BIOS, and then sets to EC. Only Win10 supports it.

In other OS, it will still use an IRQ number from BIOS as usual.

For details, please refer to the iManager & Software API User Manual.



System Assignments

This appendix details information on the system resource allocation on the SOM-2532 CPU System-on-Module.

- Sections include:
- System I/O Ports
- DMA Channel Assignments
- Interrupt Assignments
- 1st MB Memory Map

C.1 System I/O Ports

Table C.1: System I/O Ports

Resource	Device		
0x0000000-0x00000CF7	PCI Express Root Complex		
0x0000020-0x00000021	Programmable interrupt controller		
0x0000024-0x0000025	Programmable interrupt controller		
0x0000028-0x0000029	Programmable interrupt controller		
0x0000002C-0x0000002D	Programmable interrupt controller		
0x0000002E-0x0000002F	Motherboard resources		
0x0000030-0x0000031	Programmable interrupt controller		
0x0000034-0x0000035	Programmable interrupt controller		
0x0000038-0x0000039	Programmable interrupt controller		
0x000003C-0x000003D	Programmable interrupt controller		
0x00000040-0x00000043	System timer		
0x0000004E-0x0000004F	Motherboard resources		
0x0000050-0x00000053	System timer		
0x0000061-0x0000061	Motherboard resources		
0x0000062-0x0000062	Microsoft ACPI-Compliant Embedded Controller		
0x0000063-0x0000063	Motherboard resources		
0x0000065-0x0000065	Motherboard resources		
0x0000066-0x0000066	Microsoft ACPI-Compliant Embedded Controller		
0x0000067-0x0000067	Motherboard resources		
0x0000070-0x00000070	Motherboard resources		
0x0000080-0x0000080	Motherboard resources		
0x0000092-0x0000092	Motherboard resources		
0x000000A0-0x000000A1	Programmable interrupt controller		
0x000000A4-0x000000A5	Programmable interrupt controller		
0x000000A8-0x000000A9	Programmable interrupt controller		
0x00000AC-0x00000AD	Programmable interrupt controller		
0x000000B0-0x000000B1	Programmable interrupt controller		
0x000000B2-0x000000B3	Motherboard resources		
0x000000B4-0x000000B5	Programmable interrupt controller		
0x000000B8-0x000000B9	Programmable interrupt controller		
0x000000BC-0x000000BD	Programmable interrupt controller		
0x0000029C-0x0000029D	Motherboard resources		
0x000002F8-0x000002FF	Communications Port (COM2)		
0x000003F8-0x000003FF	Communications Port (COM1)		
0x000004D0-0x000004D1	Programmable interrupt controller		
0x00000680-0x0000069F	Motherboard resources		
0x00000D00-0x0000FFFF	PCI Express Root Complex		
0x0000164E-0x0000164F	Motherboard resources		
0x00001800-0x000018FE	Motherboard resources		
0x00001854-0x00001857	Motherboard resources		
0x00002000-0x000020FE	Motherboard resources		
0x00003000-0x0000303F	Intel® UHD Graphics		
0x00003060-0x0000307F	Standard SATA AHCI Controller		

0x00003080-0x00003083	Standard SATA AHCI Controller
0x00003090-0x00003097	Standard SATA AHCI Controller
0x0000EFA0-0x0000EFBF	Intel® SMBus Controller - 4B23

C.2 Interrupt Assignments

Table C.2: Interrupt Assignments		
Resource	Device	
IRQ 0	System timer	
IRQ 3	Communications Port (COM2)	
IRQ 7	Communications Port (COM1)	
IRQ 14	Intel® Serial IO GPIO Host Controller - INTC1020	
IRQ 16	SDA Standard Compliant SD Host Controller	
IRQ 17	SDA Standard Compliant SD Host Controller	
IRQ 54-IRQ 60	Microsoft ACPI-Compliant System	
IRQ 61-IRQ 70	Microsoft ACPI-Compliant System	
IRQ 71-IRQ 80	Microsoft ACPI-Compliant System	
IRQ 81-IRQ 90	Microsoft ACPI-Compliant System	
IRQ 91-IRQ 100	Microsoft ACPI-Compliant System	
IRQ 101-IRQ 110	Microsoft ACPI-Compliant System	
IRQ 111-IRQ 120	Microsoft ACPI-Compliant System	
IRQ 121-IRQ 130	Microsoft ACPI-Compliant System	
IRQ 131-IRQ 140	Microsoft ACPI-Compliant System	
IRQ 141-IRQ 150	Microsoft ACPI-Compliant System	
IRQ 151-IRQ 160	Microsoft ACPI-Compliant System	
IRQ 161-IRQ 170	Microsoft ACPI-Compliant System	
IRQ 171-IRQ 180	Microsoft ACPI-Compliant System	
IRQ 181-IRQ 190	Microsoft ACPI-Compliant System	
IRQ 191-IRQ 200	Microsoft ACPI-Compliant System	
IRQ 201-IRQ 204	Microsoft ACPI-Compliant System	
IRQ 256-IRQ 260	Microsoft ACPI-Compliant System	
IRQ 261-IRQ 270	Microsoft ACPI-Compliant System	
IRQ 271-IRQ 280	Microsoft ACPI-Compliant System	
IRQ 281-IRQ 290	Microsoft ACPI-Compliant System	
IRQ 291-IRQ 300	Microsoft ACPI-Compliant System	
IRQ 301-IRQ 310	Microsoft ACPI-Compliant System	
IRQ 311-IRQ 320	Microsoft ACPI-Compliant System	
IRQ 321-IRQ 330	Microsoft ACPI-Compliant System	
IRQ 331-IRQ 340	Microsoft ACPI-Compliant System	
IRQ 341-IRQ 350	Microsoft ACPI-Compliant System	
IRQ 351-IRQ 360	Microsoft ACPI-Compliant System	
IRQ 361-IRQ 370	Microsoft ACPI-Compliant System	
IRQ 371-IRQ 380	Microsoft ACPI-Compliant System	
IRQ 381-IRQ 390	Microsoft ACPI-Compliant System	
IRQ 391-IRQ 400	Microsoft ACPI-Compliant System	
IRQ 401-IRQ 410	Microsoft ACPI-Compliant System	

Table C.2: Interrupt Assig	nments
IRQ 411-IRQ 420	Microsoft ACPI-Compliant System
IRQ 421-IRQ 430	Microsoft ACPI-Compliant System
IRQ 431-IRQ 440	Microsoft ACPI-Compliant System
IRQ 441-IRQ 450	Microsoft ACPI-Compliant System
IRQ 451-IRQ 460	Microsoft ACPI-Compliant System
IRQ 461-IRQ 470	Microsoft ACPI-Compliant System
IRQ 471-IRQ 480	Microsoft ACPI-Compliant System
IRQ 481-IRQ 490	Microsoft ACPI-Compliant System
IRQ 491-IRQ 500	Microsoft ACPI-Compliant System
IRQ 501-IRQ 510	Microsoft ACPI-Compliant System
IRQ 511	Microsoft ACPI-Compliant System
IRQ 1024	SDA Standard Compliant SD Host Controller
IRQ 4294967284	Intel® Integrated Sensor Solution
IRQ 4294967285	Intel® Serial IO I2C Host Controller - 4BBF
IRQ 4294967286	Intel® Serial IO I2C Host Controller - 4BBA
IRQ 4294967287	Intel® Serial IO I2C Host Controller - 4BB9
IRQ 4294967288	Intel® Smart Sound Technology (Intel® SST) Audio Con- troller
IRQ 4294967289	Intel® Management Engine Interface #1
IRQ 4294967290	Intel® USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967291	Intel® UHD Graphics
IRQ 4294967292	Intel® EC1000R 1.0GbE Connection
IRQ 4294967293	Intel® EC1000R 1.0GbE Connection #2
IRQ 4294967294	Standard SATA AHCI Controller

C.3 1st MB Memory Map

Table C.3: 1st MB Memory Map		
Resource	Device	
0x1340000-0x137FFFF	Intel® EC1000R 1.0GbE Connection	
0xFEC80000-0xFECFFFFF	Motherboard resources	
0xFEDA0000-0xFEDA0FFF	Motherboard resources	
0xFEDA1000-0xFEDA1FFF	Motherboard resources	
0xC0000000-0xCFFFFFF	Motherboard resources	
0xFED20000-0xFED7FFFF	Motherboard resources	
0xFED90000-0xFED93FFF	Motherboard resources	
0xFED45000-0xFED8FFFF	Motherboard resources	
0xFEE00000-0xFEEFFFFF	Motherboard resources	
0x13A1000-0x13A1FFF	SDA Standard Compliant SD Host Controller	
0xFFCFA000-0xFFCFBFFF	Intel® Serial IO I2C Host Controller - 4BB9	
0xFFCFC000-0xFFCFFFFF	Intel® Smart Sound Technology (Intel® SST) Audio Con- troller	
0xFFD00000-0xFFDFFFFF	Intel® Smart Sound Technology (Intel® SST) Audio Con- troller	
0xFFCF8000-0xFFCF9FFF	Intel® Serial IO I2C Host Controller - 4BBA	

Table	C.3:	1st M	IB Me	emory	Map

0xFED00000-0xFED003FF	High precision event timer
0x0000-0xFFFFF	Intel® UHD Graphics
0x0000-0xFFFFFF	Intel® UHD Graphics
0xFFCF6000-0xFFCF7FFF	Intel® Serial IO I2C Host Controller - 4BBF
0xFFE00000-0xFFFFFFF	Intel® Integrated Sensor Solution
0xFE010000-0xFE010FFF	Intel® SPI (flash) Controller - 4B24
0xFD000000-0xFD68FFFF	Motherboard resources
0xFD6F0000-0xFDFFFFFF	Motherboard resources
0xFE000000-0xFE01FFFF	Motherboard resources
0xFE200000-0xFE7FFFFF	Motherboard resources
0xFF000000-0xFFFFFFFF	Motherboard resources
0xFD6B0000-0xFD6CFFFF	Motherboard resources
0xFD6B0000-0xFD6CFFFF	Intel® Serial I/O GPIO Host Controller - INTC1020
0x1300000-0x133FFFF	Intel® EC1000R 1.0GbE Connection #2
0x1380000-0x138FFFF	Intel® USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
0xFE032000-0xFE032FFF	Motherboard resources
0xFE033000-0xFE033FFF	Motherboard resources
0xFED40000-0xFED44FFF	Trusted Platform Module 2.0
0x13A0000-0x13A0FFF	SDA Standard Compliant SD Host Controller
0x139E000-0x139E0FF	Intel® SMBus Controller - 4B23
0xFD6E0000-0xFD6EFFFF	Intel® Serial IO GPIO Host Controller - INTC1020
0xFD6D0000-0xFD6DFFFF	Intel® Serial IO GPIO Host Controller - INTC1020
0xFD6C0000-0xFD6CFFFF	Intel® Serial IO GPIO Host Controller - INTC1020
0xFD6A0000-0xFD6AFFFF	Intel® Serial IO GPIO Host Controller - INTC1020
0xFD690000-0xFD69FFFF	Intel® Serial IO GPIO Host Controller - INTC1020
0xFFCF5000-0xFFCF5FFF	Intel® Management Engine Interface #1
0xA0000-0xBFFFF	PCI Express Root Complex
0xE0000-0xE3FFF	PCI Express Root Complex
0xE4000-0xE7FFF	PCI Express Root Complex
0xE8000-0xEBFFF	PCI Express Root Complex
0xEC000-0xEFFFF	PCI Express Root Complex
0xF0000-0xFFFFF	PCI Express Root Complex
0x1300200-0x1300203	Intel® Ethernet PCS - 1033
0x1300204-0x1300207	Intel® Ethernet PCS - 1033
0x1340200-0x1340203	Intel® Ethernet PCS - 1033
0x1340204-0x1340207	Intel® Ethernet PCS - 1033
0x7FC00000-0x7FC01FFF	Standard SATA AHCI Controller
0x7FC00000-0x7FC01FFF	PCI Express Root Complex
0x7FC02000-0x7FC027FF	Standard SATA AHCI Controller
0x7FC03000-0x7FC030FF	Standard SATA AHCI Controller



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