innodisk

The Total Solution For Industrial Flash Storage

Approval Sheet

Customer	
Product Number	**M3DW-8GSS6C0C-D**
Module speed	**PC3-12800**
Pin	**204pin**
Cl-tRCD-tRP	**11-11-11**
SDRAM Operating Temp	**0℃~85℃**
Date	**23rd March 2015**

Approval by Customer

P/N:

Signature:

Date:

Sales: **Sr. Technical Manager: John Hsieh**

Rev 1.0

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)
		CL=7	CL=9	CL=11			
PC3-12800	**P**	1066	1333	1600	13.125	13.125	13.125

- JEDEC Standard 204-pin Dual In-Line Memory Module
- Intend for PC3-12800 applications
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.5 Volt (±0.1V)
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- On-Board Thermal Sensor (Optional)
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8μs ($T_A \leq +85°C$)
- 16/10/2 Addressing (row/column/rank)-8GB
- SDRAM operating temperature range

$0°C \leq T_A \leq +85°C$

- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 7, 9 ,11
  - Burst Length: switch on-the-fly: BL=8 or BC 4
- RoHS Compliant *(Section 13)*

2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +65	°C	1
T_{STG}	Storage Temperature	-50 to +100	°C	
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.
2. Up to 9850 ft.

3. SDRAM Parameters by device density

RTT_Nom Setting	Parameter		4Gb	Units
tRFC	REF command ACT or REF command time		260	ns
tREFI	Average periodic refresh interval	0°C≦ T_{CASE}≦ **85**°C	7.8	µs
		85°C≦ T_{CASE}≦ **95**°C	3.9	µs

4. Ordering Information

DDR3 ECCSODIMM							
Part Number	Density	Speed	Bandwidth	Number of DRAM	Number of rank	ECC	Thermal Sensor
M3DW-8GSS6C0C-D	8GB	PC3-12800	1024Mx72	18	2	Y	N
M3DW-8GSS6C0C-DT							Y

5. Pin Configurations (Front side/Back side)

X72 SODIMM

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	VREFDQ	2	VSS	53	VSS	54	DQ28	103	A3	104	A4	155	VSS	156	DQS5_t
3	VSS	4	DQ4	55	DQ24	56	DQ29	105	A1	106	A2	157	DM5	158	VSS
5	DQ0	6	DQ5	57	DQ25	58	VSS	107	A0	108	BA1	159	DQ42	160	DQ46
7	DQ1	8	VSS	59	DM3	60	DQS3_c	109	VDD	110	VDD	161	DQ43	162	DQ47
9	VSS	10	DQS0_c	61	VSS	62	DQS3_t	111	CK0_t	112	Par_In, NC, CK1_t	163	VSS	164	VSS
11	DM0	12	DQS0_t	63	DQ26	64	VSS	113	CK0_c	114	Err_Out_n, NC, CK1_c	165	DQ48	166	DQ52
13	DQ2	14	VSS	65	DQ27	66	DQ30	115	VDD	116	VDD	167	DQ49	168	DQ53
15	DQ3	16	DQ6	67	VSS	68	DQ31	117	A10/AP	118	S3_n	169	VSS	170	VSS
17	VSS	18	DQ7	69	CB0	70	VSS	119	BA0	120	S2_n	171	DQS6_c	172	DM6
19	DQ8	20	VSS	71	CB1	72	CB4	121	WE_n	122	RAS_n	173	DQS6_t	174	DQ54
21	DQ9	22	DQ12	Key				123	VDD	124	VDD	175	VSS	176	DQ55
23	VSS	24	DQ13	73	VSS	74	CB5	125	CAS_n	126	ODT0	177	DQ50	178	VSS
25	DQS1_c	26	VSS	75	DQS8_c	76	DM8	127	S0_n	128	ODT1	179	DQ51	180	DQ60
27	DQS1_t	28	DM1	77	DQS8_t	78	VSS	129	S1_n	130	A13	181	VSS	182	DQ61
29	VSS	30	RESET_n	79	VSS	80	CB6	131	VDD	132	VDD	183	DQ56	184	VSS
31	DQ10	32	VSS	81	CB2	82	CB7	133	DQ32	134	DQ36	185	DQ57	186	DQS7_c
33	DQ11	34	DQ14	83	CB3	84	VREFCA	135	DQ33	136	DQ37	187	VSS	188	DQS7_t
35	VSS	36	DQ15	85	VDD	86	VDD	137	VSS	138	VSS	189	DM7	190	VSS
37	DQ16	38	VSS	87	CKE0	88	A15	139	DQS4_c	140	DM4	191	DQ58	192	DQ62
39	DQ17	40	DQ20	89	CKE1	90	A14	141	DQS4_t	142	DQ38	193	DQ59	194	DQ63
41	VSS	42	DQ21	91	BA2	92	A9	143	VSS	144	DQ39	195	VSS	196	VSS
43	DQS2_c	44	DM2	93	VDD	94	VDD	145	DQ34	146	VSS	197	SA0	198	EVENT_n
45	DQS2_t	46	VSS	95	A12/BC_n	96	A11	147	DQ35	148	DQ44	199	VDDSPD	200	SDA
47	VSS	48	DQ22	97	A8	98	A7	149	VSS	150	DQ45	201	SA1	202	SCL
49	DQ18	50	DQ23	99	A5	100	A6	151	DQ40	152	VSS	203	VTT	204	VTT
51	DQ19	52	VSS	101	VDD	102	VDD	153	DQ41	154	DQS5_c				

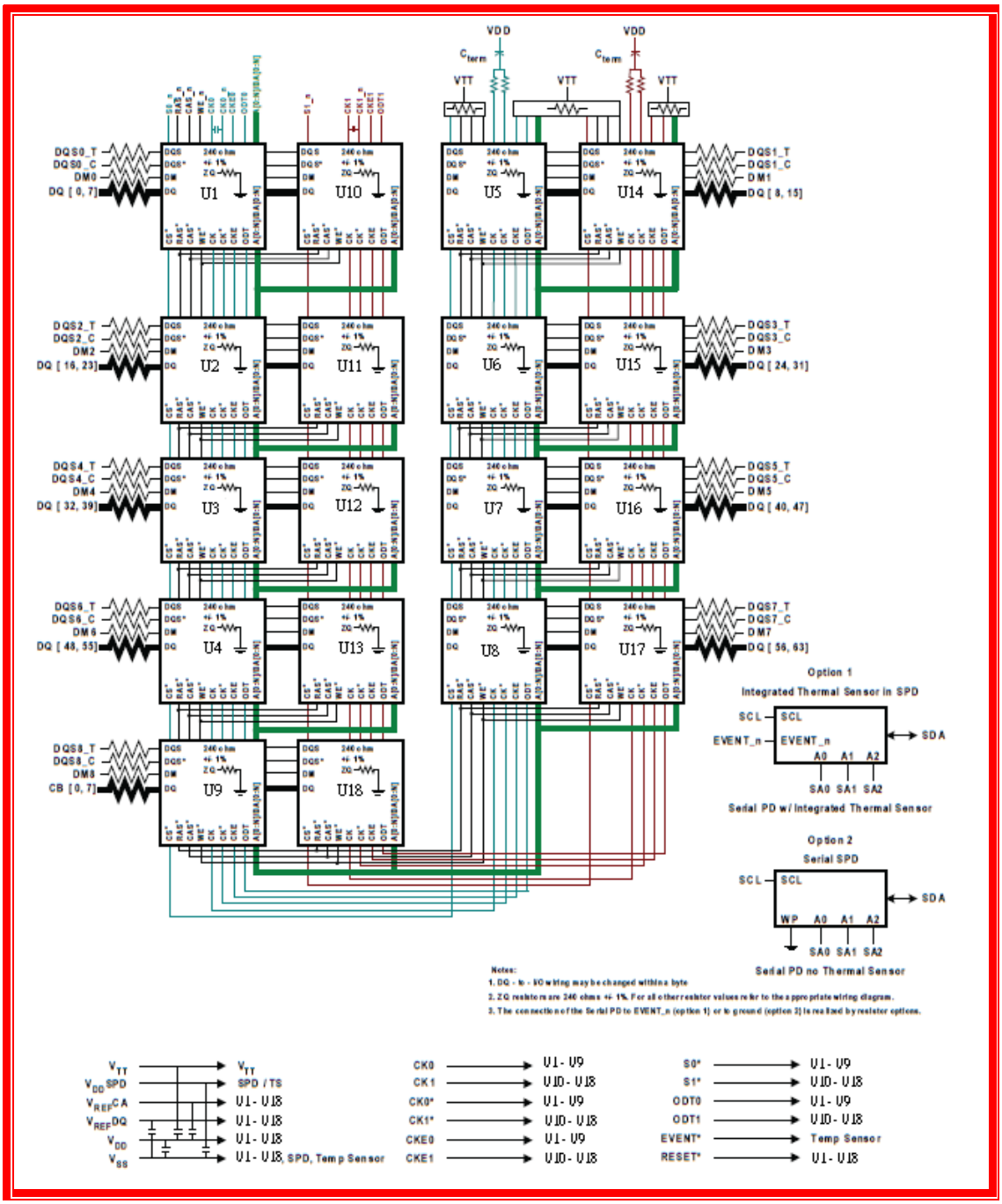
6. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
/RAS	SDRAM row address strobe	SA0 – SA1	Serial Presence Detect Address Inputs
/CAS	SDRAM column address strobe	V_{DD}	Power Supply
/WE	SDRAM write enable	V_{DDID}	V_{DD} Identification Flag
/S0 - /S1	DIMM Rank Select Lines	V_{DDQ}	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	V_{REFDQ}	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	V_{REFCA}	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	V_{SS}	Ground
DQS0 – DQS8 /DQS0-/DQS8	SDRAM data strobes	V_{DDSPD}	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	/Reset	Reset enable
CK0 – CK1 /CK0 - /CK1	Differential SDRAM Clocks	Event#	Reserved for optional temperature-sensing hardware
RSVD	Reserved for future use.	V_{TT}	SDRAM I/O termination supply.

7. Function Block Diagram:

- (8GB, 2 Ranks 512Mx8 DDR3 SDRAMs)



Note: Temperature sensor accuracy (max):

– ± 1 °C from +75 °C to +95 °C

– ± 2 °C from +40 °C to +125 °C

– ± 3 °C from –40 °C to +125 °C

8. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.4 to +1.975	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.4 to +1.975	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.4 to +1.975	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.
For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under
all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional
conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.
4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

9. SDRAM AC & DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply Voltage	1.425	1.5	1.575	V	1,2
Single Ended AC/DC Input Levels						
$V_{IH\ (DC)}$	DC Input High (Logic1) Voltage	V_{REF} + 0.1	-	V_{DD}	V	3
$V_{IL\ (DC)}$	DC Input Low (Logic 0) Voltage	V_{SS}	-	V_{REF} - 0.1	V	3
$V_{IH\ (AC)}$	AC Input High (Logic1) Voltage	V_{REF}+ 0.175	-	-	V	3
$V_{IL\ (AC)}$	AC Input Low (Logic 0) Voltage	-	-	V_{REF} - 0.175	V	3
$V_{REFDQ\ (DC)}$	Reference Voltage for DQ, DM inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
$V_{REFCA\ (DC)}$	Reference Voltage for ADD,CMD inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
Single Ended AC/DC output Levels						
$V_{OH\ (DC)}$	DC output high measurement level (for IV curve linearity)	-	0.8 x VDDQ	-	V	
$V_{OM\ (DC)}$	DC output mid measurement level (for IV curve linearity)	-	0.5 x VDDQ	-	V	
$V_{OL\ (DC)}$	DC output low measurement level (for IV curve linearity)	-	0.2 x VDDQ	-	V	
$V_{OH\ (AC)}$	AC output high measurement level (for output SR)	-	VTT + 0.1 x VDDQ	-	V	6
$V_{OL\ (AC)}$	AC output low measurement level (for output SR)		VTT - 0.1 x VDDQ	-	V	6

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Differential AC/DC Input Levels						
V_{IHdiff}	Differential Input high	+0.2	-	Note 9	V	7
V_{ILdiff}	Differential Input logic Low	Note 9	-	-0.2	V	7
$V_{IHdiff(ac)}$	Differential Input high ac	2* ($V_{IH\ (AC)}$-V_{REF})	-	Note 9	V	8
$V_{ILdiff(ac)}$	Differential Input logic Low ac	Note 9	-	2* (V_{REF}-$V_{IL\ (AC)}$)	V	8
Differential AC and DC Output Levels						
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	-	+ 0.2 x VDDQ	-	V	10
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	-	- 0.2 x VDDQ	-	V	10

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
4. The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
5. For reference: approx. VDD/2 +/- 15 mV.
6. The swing of ± 0.1 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2
7. Used to define a differential signal slew-rate.
8. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
9. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot.
10. The swing of ± 0.2 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

10. Operating, Standby, and Refresh Currents

- 8GB ECCSODIMM (2 Rank, 512Mx8 DDR3 SDRAMs T_{CASE} = 0 °C ~ 70 °C)

Symbol	Parameter/Condition		PC3-12800	Unit
I DD0	One bank; Active - Precharge		540	mA
I DD1	One bank; Active - Read - Precharge		630	mA
I DD2N	Precharge Standby Current		340	mA
I DD2P	Precharge Power Down Current	Fast Mode	250	mA
	Precharge Power Down Current	Slow Mode	250	mA
I DD2Q	Pecharge Quiet Standby Current		340	mA
I DD3N	Active Standby Current		430	mA
I DD3P	Active Power-Down Current		340	mA
I DD4R	Operating Current Burst Read		1020	mA
I DD4W	Operating Current Burst Write		1100	mA
I DD5B	Burst Refresh Current		140	mA
I DD6	Self-Refresh Current: Normal Temperature Range		250	mA
I DD7	Operating Bank Interleave Read Current		1600	mA
I DD8	Low precharge current		255	mA

11. SPD

Serial Presence Detect – (8GB)

2 RANK UNBUFFERED DDR SDRAM DIMM based on 512Mx8, 8Banks, 8K Refresh, DDR3 SDRAMs with SPD

Byte	Description	Serial PD Data Entry (Hexadecimal)	Note
0	Number of Serial PD Bytes Written during Production	92	
1	SPD Revision	11	
2	Key Byte/DRAM Device Type	0B	
3	Key Byte/Module type	08	
4	SDRAM Density and Banks	04	
5	SDRAM Address	21	
6	Reserve	00	
7	Module Organization	09	
8	Module Memory Bus Width	0B	
9	Fine Timebase (FTB) Dividend/Divisor	52	
10	Medium Timebase (MTB) Dividend	01	
11	Medium Timebase (MTB) Divisor	08	
12	SDRAM Minimum Cycle Time (tCKmin)	0A	
13	Reserve	00	
14	CAS latency, least Significant Byte	FE	
15	CAS latency, most Significant Byte	00	
16	Minimum CAS Latency Time (tAAmin)	69	
17	Minimum Write Recovery Time (tWRmin)	78	

Byte	Description	Serial PD Data Entry (Hexadecimal)	Note
18	Minimum RAS# to CAS# Delay Time (tRCDmin)	69	
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	30	
20	Minimum Row Precharge Delay Time (tRPmin)	69	
21	Upper Nibbles for tRAS and tRC	11	
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	18	
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	81	
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte	20	
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte	08	
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	3C	
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	3C	
28	Upper Nibble for tFAW	00	
29	Minimum Four Activate Window Delay Time (tFAWmin)	F0	
30	SDRAM Optional Features	83	
31	SDRAM Thermal and Refresh Options	0D	
32	Module Thermal Sensor	00	
33	SDRAM Device Type	00	

34-59	Reserve	00	
60-63	Module Type Specific Section,	0F 11 23 00	
64-117	Reserve	00	
117-118	Module ID: Module Manufacturer's JEDEC ID Code	86 F1	
119	Module ID: Module Manufacturing Location	02	
120-121	Module ID: Module Manufacturing Date	0A 03	
122-125	**Module Serial Number**	00	
126-127	**SPD Cyclical Redundancy Code**	B2 2A	
128-255	reserve	-	

12. Timing Parameters

(T_{CASE} = 0 °C ~ 70 °C; V_{DDQ} = V_{DD} , See AC Characteristics)

Symbol	Parameter	PC3-12800		Unit
		Min.	Max.	
Clock Timing				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.5	3.3	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-70	70	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-60	60	Ps
JIT (CC)	Cycle to Cycle Period Jitter	140		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	120		Ps
TJIT (duty)		-	-	Ps
TERR (2per)	Cumulative error across 2 cycle	-103	103	Ps
TERR (3per)	Cumulative error across 3 cycle	-122	122	Ps
TERR (4per)	Cumulative error across 4 cycle	-136	136	Ps
TERR (5per)	Cumulative error across 5 cycle	-147	147	Ps
TERR (6per)	Cumulative error across 6 cycle	-155	155	Ps
TERR (7per)	Cumulative error across 7 cycle	-163	163	Ps
TERR (8per)	Cumulative error across 3 cycle	-169	169	Ps
TERR (9per)	Cumulative error across 4 cycle	-175	175	Ps
TERR (10per)	Cumulative error across 5 cycle	-180	180	Ps

TERR (11per)	Cumulative error across 6 cycle	-184	184	Ps
TERR (12per)	Cumulative error across 7 cycle	-188	188	Ps
TERR (nper)	Cumulative error across 13~50 cycle	$_{t}$ERR(nper)min = (1 + 0.68ln(n)) * $_{t}$JIT(per)min $_{t}$ERR(nper)max = (1 + 0.68ln(n)) * $_{t}$JIT(per)max		Ps
Data Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDSQ	DQS, DQS# to DQ skew, per group, per access	-	100	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-450	225	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	225	Ps
tDS(base) AC150	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	10	-	Ps
tDH(base) DC 100	Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	45	-	Ps
Data Strobe Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tRPRE	DQS,DQS# differential READ Preamble	0.9		tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)
tQSH	DQS, DQS# differential output high time	0.4		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.4		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)
tDQSCK	DQS, DQS# rising edge output access time from rising CK, CK#	-225	225	Ps

tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-450	225	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	225	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.27	0.27	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.18	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.18	-	tCK(avg)
Command and Address Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to Internal read command	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			
tRC	Refer to Section 1 Feature			
tCCD		4	-	nCK

tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup(tRP / tCK(avg))		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	35	9 tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4nCK, 6ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4nCK, 7.5ns)	-	
tFAW	Four activate window for 1KB page size	30	-	ns
tFAW	Four activate window for 2KB page size	40	-	ns
tIS (base)	Command and Address setup time to CK, CK#, referenced to Vih(ac) / Vil(ac) levels.	45		ns
tIH(base)	Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	170		ps
tIS(base) AC150	Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	120		ps
Calibration Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tZQinit	Power-up and RESET calibration time	Max. (512nCK, 640ns)	-	nCK
tZQoper	Normal operation Full calibration time	Max. (256nCK, 320ns)	-	nCK
tZQCS	Normal operation Short calibration time	Max. (64nCK, 80ns)	-	nCK

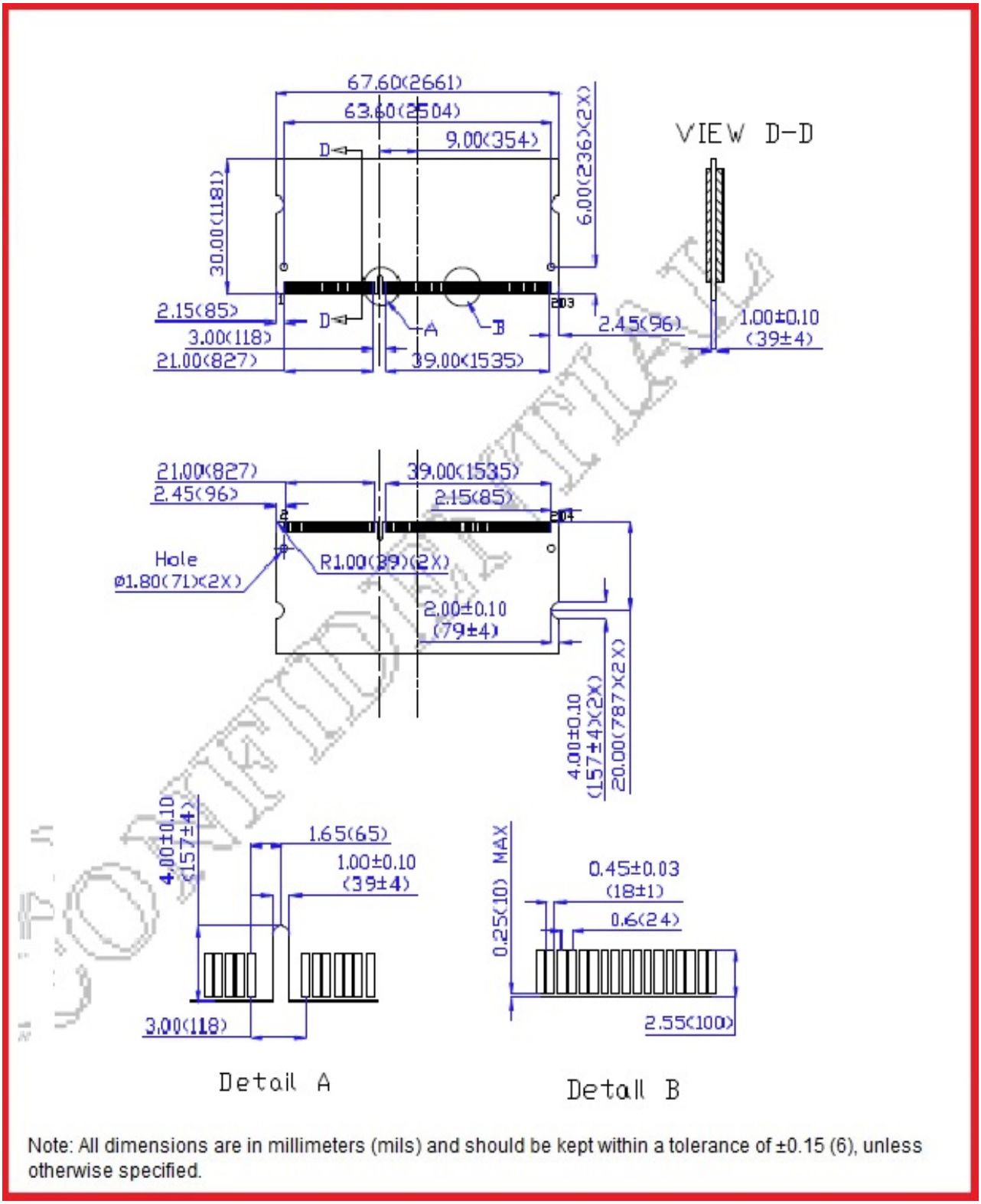
Reset Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK,tRFC(min) +10ns)	-	
Self Refresh Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXS	Exit Self Refresh to commands not requiring a locked DLL	Max(5nCK), tRFC(min) +10ns)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE9min) +1nCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5nCK,10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5nCK,10ns)	-	
Power Down Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK CK, 24ns)	-	

tCKE	CKE minimum pulse width	max(3nCK,5ns)	-	
tCPDED	Command pass disable delay	1	-	nCK
tPD	Power Down Entry to Exit Timing	tCK(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	nCK
ODT Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK

tAONPD	Asynchronous RTT turn-on delay (Powe-Down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns
tAON	RTT-turn-on	-225	225	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	tCK(avg)

13. PACKAGE DIMENSION

- (8GB, 2 Ranks, 512Mx8 DDR3 base ECCSODIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

14. RoHS Declaration

Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product M3DW-8GSS6C0C/-(X) complies with the requirement of RoHS directives 2011/65/EU and 2006/12/EC.

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3rd party test reports of the component/ raw materials used in the manufacture of products.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI（Cr+6）	< 1000 ppm
Polybromodiphenyl ether（PBDE）	< 1000 ppm
Polybrominated Biphenyls（PBB）	< 1000 ppm
Perfluorooctane Sulfonate (PFOS)	Not Contained

Date issued: 2013/01/22

Manufacturer: ：InnoDisk Co., Ltd.
Address：9F, No. 100, Sec.1 Xintai 5th Rd., Xizhi City, Taipei 221, Taiwan

Authorized Signature：

QA Dept. Director – Ryan Tsai

Revision Log

Rev	Date	Modification
0.1	23rd March 2015	Preliminary Edition
1.0	23rd March 2015	Official released.