innodisk

Approval Sheet

Customer	
Product Number	**M4UE-4GNX1C0M-H**
Module speed	**PC4-3200**
Pin	**288 pin**
Cl-tRCD-tRP	**22-22-22**
Operating Temp (Tc)	**0℃~95℃**
Date	**28th July 2025**

The Total Solution For
Industrial Flash Storage

Rev 1.0

1. Features

Key Parameter

Industry Nomenclature	**Speed Grade**	**Data Rate MT/s**			**CL**	**tRCD**	**tRP**
		CL=19	**CL=21**	**CL=22**			
PC4-3200	**E**	2666	2933	3200	22	22	22

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- JEDEC Standard 288-pin Dual In-Line Memory Module
- Intend for PC4-3200 applications
- Inputs and Outputs are SSTL-12 compatible
- $V_{DD}=V_{DDQ}$= 1.2 Volt (1.14V~1.26V)
- V_{PP}=2.5 Volt (2.375V~2.75V)
- V_{DDSPD}=2.2-3.6V
- Low-Power auto self-refresh (LPASR)
- 8 Banks (2 Bank Groups)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals.
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Golden Connector
- Fly-By topology
- Terminated control, command and address bus
- Programmable /CAS Latency: 10,11,12,13,14,15,16,17,18,19,20,21,22,24
- On-die V_{REFDQ} generation and Calibration
- On-Board EEPROM
- RoHS and Halogen free *(Section 11)*

2. Ordering Information

DDR4 UDIMM

Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M4UE-4GNX1C0M-H	4GB	PC4-3200	512Mx64	4	1	N

3. Pin Configurations (Front side/Back side)

DDR4 UDIMM

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	NC	145	NC	37	VSS	181	DQ29	73	VDD	217	VDD	109	VSS	253	DQ41
2	VSS	146	VREFCA	38	DQ24	182	VSS	74	CK0_t	218	CK1_t	110	DM5_n/ DBI5_n,NC	254	VSS
3	DQ4	147	VSS	39	VSS	183	DQ25	75	CK0_c	219	CK1_c	111	NC	255	DQS5_c
4	VSS	148	DQ5	40	DM3_n/ DBI3_n,NC	184	VSS	76	VDD	220	VDD	112	VSS	256	DQS5_t
5	DQ0	149	VSS	41	NC	185	DQS3_c	77	VTT	221	VTT	113	DQ46	257	VSS
6	VSS	150	DQ1	42	VSS	186	DQS3_t	78	EVENT_n,NF	222	PARITY	114	VSS	258	DQ47
7	DM0_n/ DBI0_n	151	VSS	43	DQ30	187	VSS	79	A0	223	VDD	115	DQ42	259	VSS
8	NC	152	DQS0_c	44	VSS	188	DQ31	80	VDD	224	BA1	116	VSS	260	DQ43
9	VSS	153	DQS0_t	45	DQ26	189	VSS	81	BA0	225	A10/AP	117	DQ52	261	VSS
10	DQ6	154	VSS	46	VSS	190	DQ27	82	RAS_n /A16	226	VDD	118	VSS	262	DQ53
11	VSS	155	DQ7	47	CB4/NC	191	VSS	83	VDD	227	NC	119	DQ48	263	VSS
12	DQ2	156	VSS	48	VSS	192	CB5,NC	84	CS0_n	228	WE_n/ A14	120	VSS	264	DQ49
13	VSS	157	DQ3	49	CB0/NC	193	VSS	85	VDD	229	VDD	121	DM6_n/ DBI6_n	265	VSS
14	DQ12	158	VSS	50	VSS	194	CB1,NC	86	CAS_n/ A15	230	NC	122	NC	266	DQS6_c
15	VSS	159	DQ13	51	DM8_n/ DBI8_n.NC	195	VSS	87	ODT0	231	VDD	123	VSS	267	DQS6_t
16	DQ8	160	VSS	52	NC	196	DQS8_c	88	VDD	232	A13	124	DQ54	268	VSS
17	VSS	161	DQ9	53	VSS	197	DQS8_t	89	CS1_n	233	VDD	125	VSS	269	DQ55
18	DM1_n/ DBI1_n,NC	162	VSS	54	CB6 DBI8_n,NC	198	VSS	90	VDD	234	NC	126	DQ50	270	VSS
19	NC	163	DQS1_c	55	VSS	199	CB7,NC	91	ODT1	235	NC	127	VSS	271	DQ51
20	VSS	164	DQS1_t	56	CB2/NC	200	VSS	92	VDD	236	VDD	128	DQ60	272	VSS
21	DQ14	165	VSS	57	VSS	201	CB3,NC	93	NC	237	NC	129	VSS	273	DQ61
22	VSS	166	DQ15	58	RESET_n	202	VSS	94	VSS	238	SA2	130	DQ56	274	VSS
23	DQ10	167	VSS	59	VDD	203	CKE1	95	DQ36	239	VSS	131	VSS	275	DQ57
24	VSS	168	DQ11	60	CKE0	204	VDD	96	VSS	240	DQ37	132	DM7_n/ DBI7_n,NC	276	VSS
25	DQ20	169	VSS	61	VDD	205	NC	97	DQ32	241	VSS	133	NC	277	DQS7_c
26	VSS	170	DQ21	62	ACT_n	206	VDD	98	VSS	242	DQ33	134	VSS	278	DQS7_t
27	DQ16	171	VSS	63	BG0	207	BG1	99	DM4_n/ DBI4_n,NC	243	VSS	135	DQ62	279	VSS
28	VSS	172	DQ17	64	VDD	208	ALERT_n	100	NC	244	DQS4_c	136	VSS	280	DQ63
29	DM2_n/ DBI2_n,NC	173	VSS	65	A12/BC_n	209	VDD	101	VSS	245	DQS4_t	137	DQ58	281	VSS
30	NC	174	DQS2_c	66	A9	210	A11	102	DQ38	246	VSS	138	VSS	282	DQ59
31	VSS	175	DQS2_t	67	VDD	211	A7	103	VSS	247	DQ39	139	SA0	283	VSS
32	DQ22	176	VSS	68	A8	212	VDD	104	DQ34	248	VSS	140	SA1	284	VSSSPD
33	VSS	177	DQ23	69	A6	213	A5	105	VSS	249	DQ35	141	SCL	285	SDA
34	DQ18	178	VSS	70	VDD	214	A4	106	DQ44	250	VSS	142	VPP	286	VPP
35	VSS	179	DQ19	71	A3	215	VDD	107	VSS	251	DQ45	143	VPP	287	VPP
36	DQ28	180	VSS	72	A1	216	A2	108	DQ40	252	VSS	144	NC	288	VPP

Note:
1. NC = No Connect, RFU = Reserved for Future Use
2. Address A17 is only valid for 16 Gb x4 based SDRAMs.
3. RAS_n is a multiplexed function with A16.
4. CAS_n is a multiplexed function with A15.
5. WE_n is a multiplexed function with A14.

4. Architecture

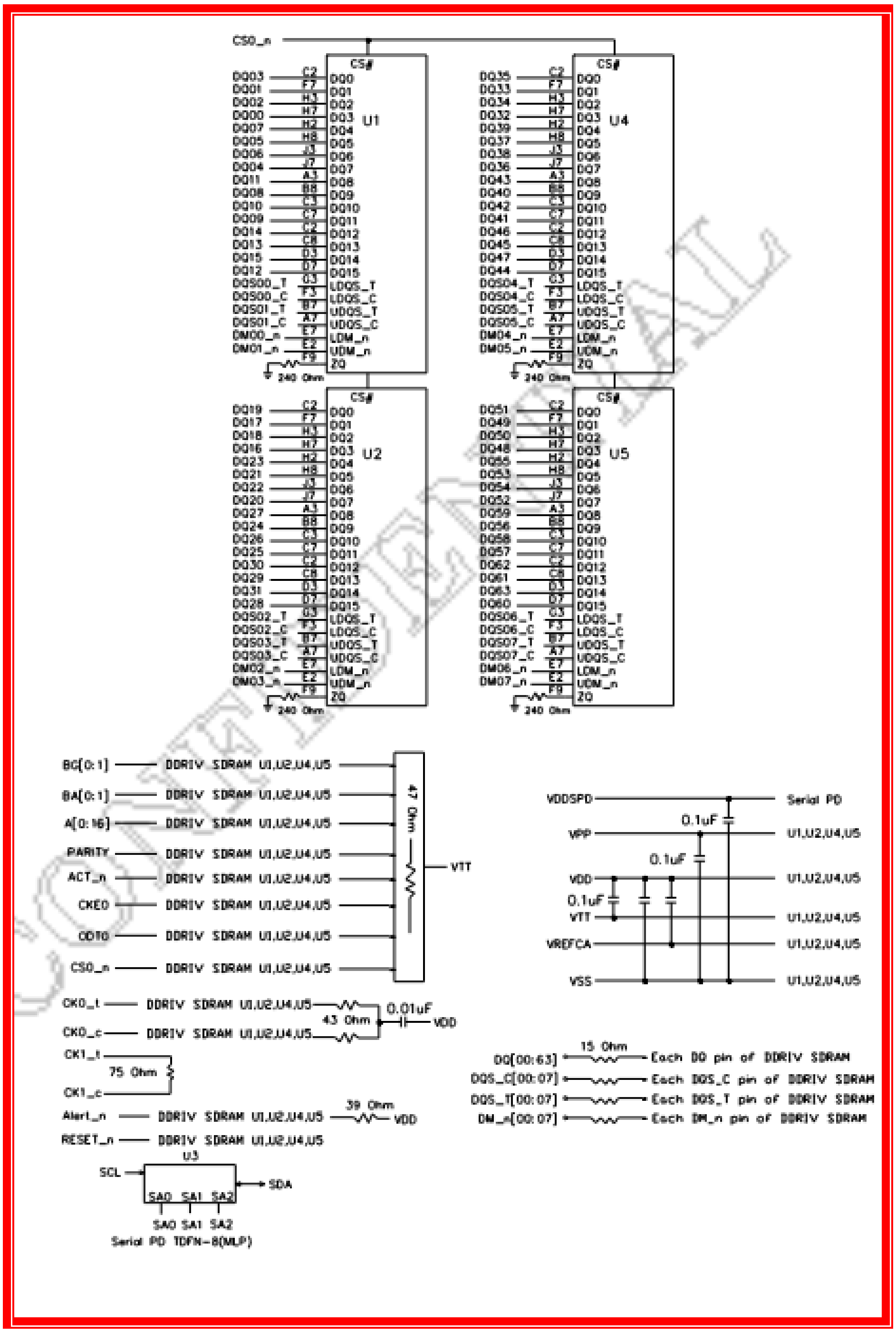
Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	SDRAM address bus	SCL	I^{2}C serial bus clock for SPD/TSE
BA0, BA1	SDRAM bank select	SDA	I^{2}C serial bus data line for SPD/TSE
BG0, BG1	SDRAM bank group select	SA0–SA2	I^{2}C slave address select for SPD/TSE
RAS_n[2]	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n[3]	SDRAM column address strobe	VDD	SDRAM I/O & core power supply
WE_n[4]	SDRAM write enable	C0, C1,C2	Chip ID lines
CS0_n, CS1_n	DIMM Rank Select Lines	12 V	Optional power Supply on socket but not used on UDIMM
CKE0, CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0–CB7	DIMM ECC check bits (for x72 module)	VPP	SDRAM Supply
TDQS0_t-TDQS8_t TDQS0_c-TDQS8_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs.		
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)		
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	RESET_n	Set DRAMs to a Known State
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)	EVENT_n	SPD signals a thermal event has occurred.
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)	RFU	Reserved for future use

Note 1 Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs this connection pin is NC.
Note 2 RAS_n is a multiplexed function with A16.
Note 3 CAS_n is a multiplexed function with A15.
Note 4 WE_n is a multiplexed function with A14.

5. Function Block Diagram:

- (4GB, 1 Rank 512Mx16 DDR4 SDRAMs)



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component’s ODT and output driver.

6. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.3 to +1.5	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.3 to +1.5	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.3 to +1.5	V	4,6

Note:

1) Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM.

2) The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions.

3) Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

7. Operating Condition

Symbol	Parameter	Min	Nom	Max	Units	Notes
VDD	Supply Voltage	1.14	1.2	1.26	V	1
VPP	DRAM activating power supply	2.375	2.5	2.75	V	2
VREFCA(DC)	Input reference voltage command/ address bus	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	3
VTT	Termination Voltage	0.49 × VDD	0.5 × VDD	0.51 × VDD	V	4

Note:

1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
4. VTT termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.

8. Operating, Standby, and Refresh Currents

- 4GB UDIMM (1 Rank 512Mx16 DDR4 SDRAMs)

Symbol	Proposed Conditions	Value		Units
		IDD Max.	IPP Max.	
IDD0	Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n:stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2;ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	420	24	mA
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0	420	-	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stableat 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	456	26	mA
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1	460	-	mA
IDD2N	Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banksclosed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	352	6	mA
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N	352	-	mA

IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern	380	-	mA
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled3	276	-	mA
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled3	308	-	mA
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled3	308	-	mA
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled3	276	-	mA
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	240	6	mA
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	288	-	mA
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern	408	9	mA

IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N	408	-	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	324	9	mA
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	948	56	mA
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R	980	-	mA
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled3, Other conditions: see IDD4R	964	-	mA
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	984	9	mA
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W	996	-	mA
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions: see IDD4W	996	-	mA

IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled3, Other conditions: see IDD4W	936	-	mA
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled3, Other conditions: see IDD4W	940	-	mA
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	956	136	mA
IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B	832	112	mA
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B	700	108	mA
IDD6N	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	172	10	mA
IDD6E	Self-Refresh Current: Extended Temperature Range) TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	236	20	mA

IDD6R	Self-Refresh Current: Reduced Temperature Range TCASE: 0 - 45 °C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: see Table 34 on p age 37; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	156	8	mA
IDD6A	Auto Self-Refresh Current TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: see Table 34 on p age 37; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	192	12	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1000	144	mA
IDD8	Maximum Power Down Current TBD	144	6	mA

9. Timing Parameters

Clock Timing				
Parameter	Symbol	MIN	MAX	Units
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	ns
Average Clock Period	tCK(avg)	0.625	<0.682	ns
Average high pulse width	tCH(avg)	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_to t	tCK(avg)max + tJIT(per)max_tot	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.45	-	tCK(avg)
Clock Period Jitter- total	JIT(per)_tot	-32	32	ps
Clock Period Jitter- deterministic	JIT(per)_dj	-16	16	ps
Clock Period Jitter during DLL lock-ing period	tJIT(per, lck)	-25	25	ps
Cycle to Cycle Period Jitter	tJIT(cc)_to-tal	62		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	50		ps
Cumulative error across 2 cycles	tERR(2per)	-46	46	ps
Cumulative error across 3 cycles	tERR(3per)	-55	55	ps
Cumulative error across 4 cycles	tERR(4per)	-61	61	ps
Cumulative error across 5 cycles	tERR(5per)	-65	65	ps
Cumulative error across 6 cycles	tERR(6per)	-69	69	ps
Cumulative error across 7 cycles	tERR(7per)	-73	73	ps

Cumulative error across 8 cycles	tERR(8per)	-76	76	ps
Cumulative error across 9 cycles	tERR(9per)	-78	78	ps
Cumulative error across 10 cycles	tERR(10per)	-80	80	ps
Cumulative error across 11 cycles	tERR(11per)	-83	83	ps
Cumulative error across 12 cycles	tERR(12per)	-84	84	ps
Cumulative error across 13 cycles	tERR(13per)	-86	86	ps
Cumulative error across 14 cycles	tERR(14per)	-87	87	ps
Cumulative error across 15 cycles	tERR(15per)	-89	89	ps
Cumulative error across 16 cycles	tERR(16per)	-90	90	ps
Cumulative error across 17 cycles	tERR(17per)	-92	92	ps
Cumulative error across 18 cycles	tERR(18per)	-93	93	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)		ps
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	40	-	ps
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	130	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	65	-	ps
Command and Address hold time to CK_t, CK_c referenced	tIH(Vref)	130	-	ps

to Vref levels				
Control and Address Input pulse width for each input	tIPW	340	-	ps
Command and Address Timing				
Parameter	Symbol	MIN	MAX	Units
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 5 ns)	-	nCK
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,2.5ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S(1/ 2K)	Max(4nCK,2.5ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,4.9ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/ 2K)	Max(4nCK,4.9ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,21ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,10ns)	-	ns
Delay from start of internal write transaction to internal	tWTR_S	max(2nCK,2.5ns)	-	

read com-mand for different bank group				
Delay from start of internal write transaction to internal read com-mand for same bank group	tWTR_L	max(4nCK,7.5ns)	-	
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (5nCK,3.75ns)	-	ns
delay from start of internal write transaction to internal read com-mand for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max (5nCK,3.75ns)	-	ns
delay from start of internal write transaction to internal read com-mand for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+max (5nCK,3.75ns)	-	ns
DLL locking time	tDLLK	1024	-	nCK
Mode Register Set command cycle time	tMRD	8	-	nCK
Mode Register Set command up-date delay	tMOD	max(24nCK,15ns)	-	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
Multi Purpose Register Write Re-covery Time	tWR_MPR	tMOD (min) + AL + PL	-	-
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))		nCK
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	UI
DQ0 or DQL0 driven to 0 hold	tPDA_H	0.5	-	UI

time from last DQS fall-ing edge				
CS_n to Command Address Latency				
CS_n to Command Address Laten-cy	tCAL	max(3 nCK, 3.748 ns)	-	nCK
DRAM Data Timing				
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.20	tCK(avg) /2
DQ output hold time from DQS_t,DQS_c	tQH	0.70	-	tCK(avg) /2
Data Valid Window per device: tQH - tDQSQ for a device	tDVWd	0.64	-	UI
Data Valid Window per device, per pin: tQH - tDQSQ each device’s out-put	tDVWp	0.72	-	UI
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-250	160	Ps
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	160	ps
Data Strobe Timing				
DQS_t, DQS_c differential READ Preamble	tRPRE	0.9		tCK
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	TBD	tCK
DQS_t,DQS_c differential output high time	tQSH	0.4	-	tCK
DQS_t,DQS_c differential output low time	tQSL	0.4	-	tCK
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	tCK
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	TBD	tCK
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-250	160	ps

DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	160	ps
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	tCK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	tCK
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	tCK
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	tCK
DQS_t, DQS_c rising edge output timing locatino from rising	tDQSCK (DLL On)	-160	160	ps
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)		260	ps
MPSM Timing				
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)		
Exit MPSM to commands not requiring a locked DLL	tXMP	txs(imin)		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)		
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	
Calibration Timing				
Power-up and RESET calibration time	tZQinit	1024	-	nCK

Normal operation Full calibration time	tZQoper	512	-	nCK
Normal operation Short calibration time	tZQCS	128	-	nCK
Reset/Self Refresh Timing				
Exit Reset from CKE HIGH to a valid command	command tXPR	max (5nCK,tRFC(min)+ 10ns)	-	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT(min)	tRFC4(min)+ 10ns	-	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	
Exit Self Refresh to commands re-quiring a locked DLL	tXSDLL	tDLLK(min)	-	
Minimum CKE low width for Self re-fresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	
Minimum CKE low width for Self re-fresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power- Down Entry (PDE)	tCKSRE	max(5nCK,10 ns)	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power- Down when CA Parity is enabled	tCKS-RE_PAR	max (5nCK,10ns) +PL	-	
Valid Clock Requirement before Self Refresh Exit (SRX)	tCKSRX	max(5nCK,10 ns)	-	

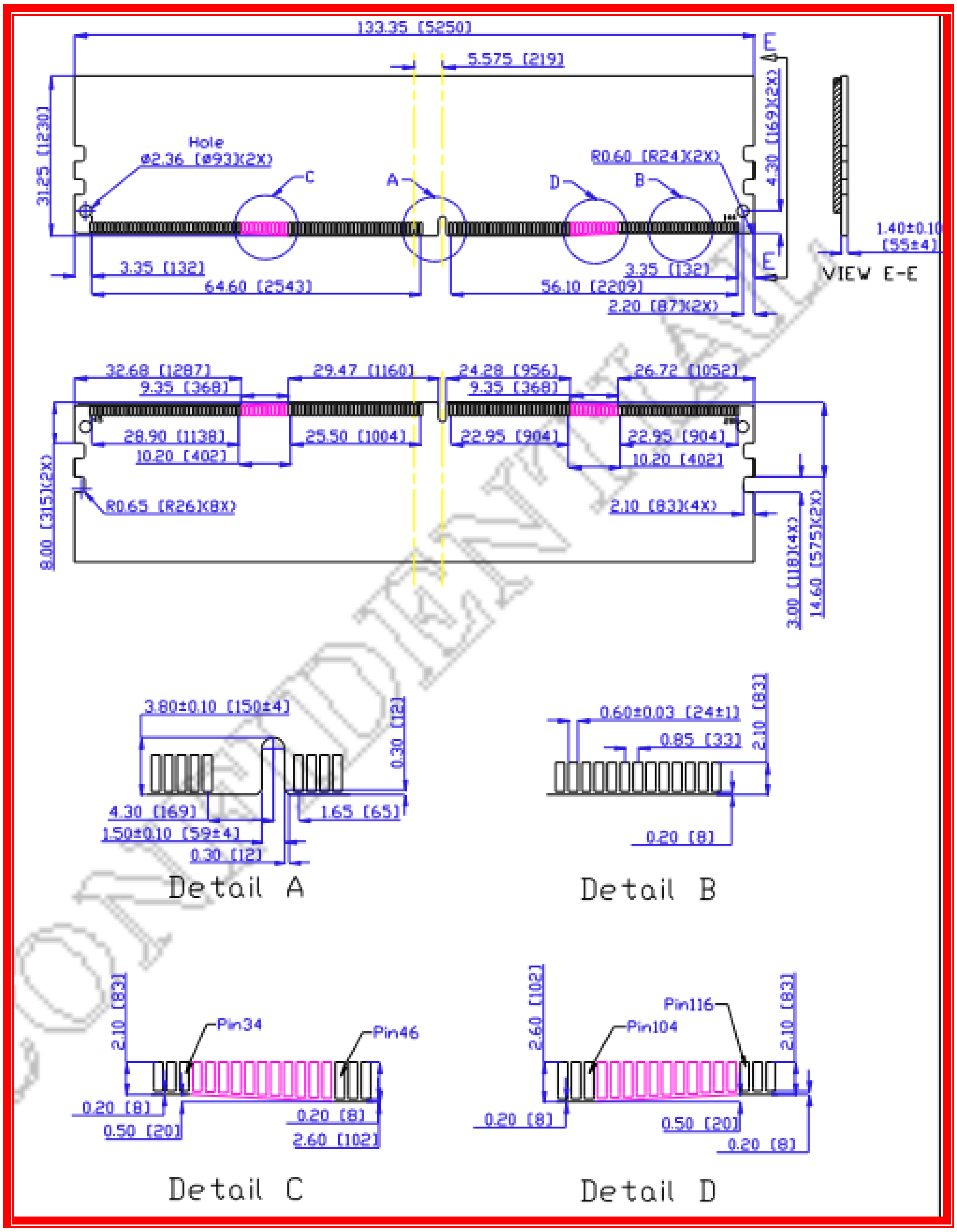
or Power-Down Exit (PDX) or Reset Exit				
Power Down Timing				
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	(4nCK,6ns)	-	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	
Command pass disable delay	tCPDED	4	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	2	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	2	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	
PDA Timing				
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)		

Mode Register Set command up-date delay in PDA mode	tMOD_PDA	tMOD		
ODT Timing				
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	ns
RTT dynamic change skew	tADC	0.26	0.74	tCK(avg)
Write Leveling Timing				
First DQS_t/DQS_n rising edge af-ter write leveling mode is pro-grammed	tWLMRD	40	-	nCK
DQS_t/DQS_n delay after write lev-eling mode is programmed	tWLDQSEN	25	-	nCK
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	tCK(avg)
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	tCK(avg)
Write leveling output delay	tWLO	0	9.5	ns
Write leveling output error	tWLOE		2	ns
CA Parity Timing				
Commands not guaranteed to be executed during this time	tPAR_UN-KNOWN	-	PL	
Delay from errant command to ALERT_n assertion	tPAR_ALER T_ON	-	PL+6ns	
Pulse width of ALERT_n signal when asserted	tPAR_ALER T_PW	96	192	nCK
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA	tPAR_ALER T_RSP	-	85	nCK

parity mode				
Parity Latency	PL	6		nCK
CRC Error Reporting				
CRC error to ALERT_n latency	tCRC_ALER T	3	13	ns
CRC ALERT_n pulse width	CRC_ALER T_PW	6	10	nCK
tREFI				
tRFC1 (min)	2Gb	160	-	ns
	4Gb	260	-	ns
	8Gb	350	-	ns
	16Gb	550	-	ns
tRFC2 (min)	2Gb	110	-	ns
	4Gb	160	-	ns
	8Gb	260	-	ns
	16Gb	350	-	ns
tRFC3 (min)	2Gb	90	-	ns
	4Gb	110	-	ns
	8Gb	160	-	ns
	16Gb	260	-	ns

10. PACKAGE DIMENSION

- (4GB, 1 Rank 512Mx16 DDR4 base UDIMM)



Note1: Device position is only for reference.

Note2: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

11. RoHS Declaration

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宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Internet: https://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Products: All Innodisk EM FLASH, DRAM and EP products

一、宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及(EU) 2015/863 關於 RoHS 之規範要求。
Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。
Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

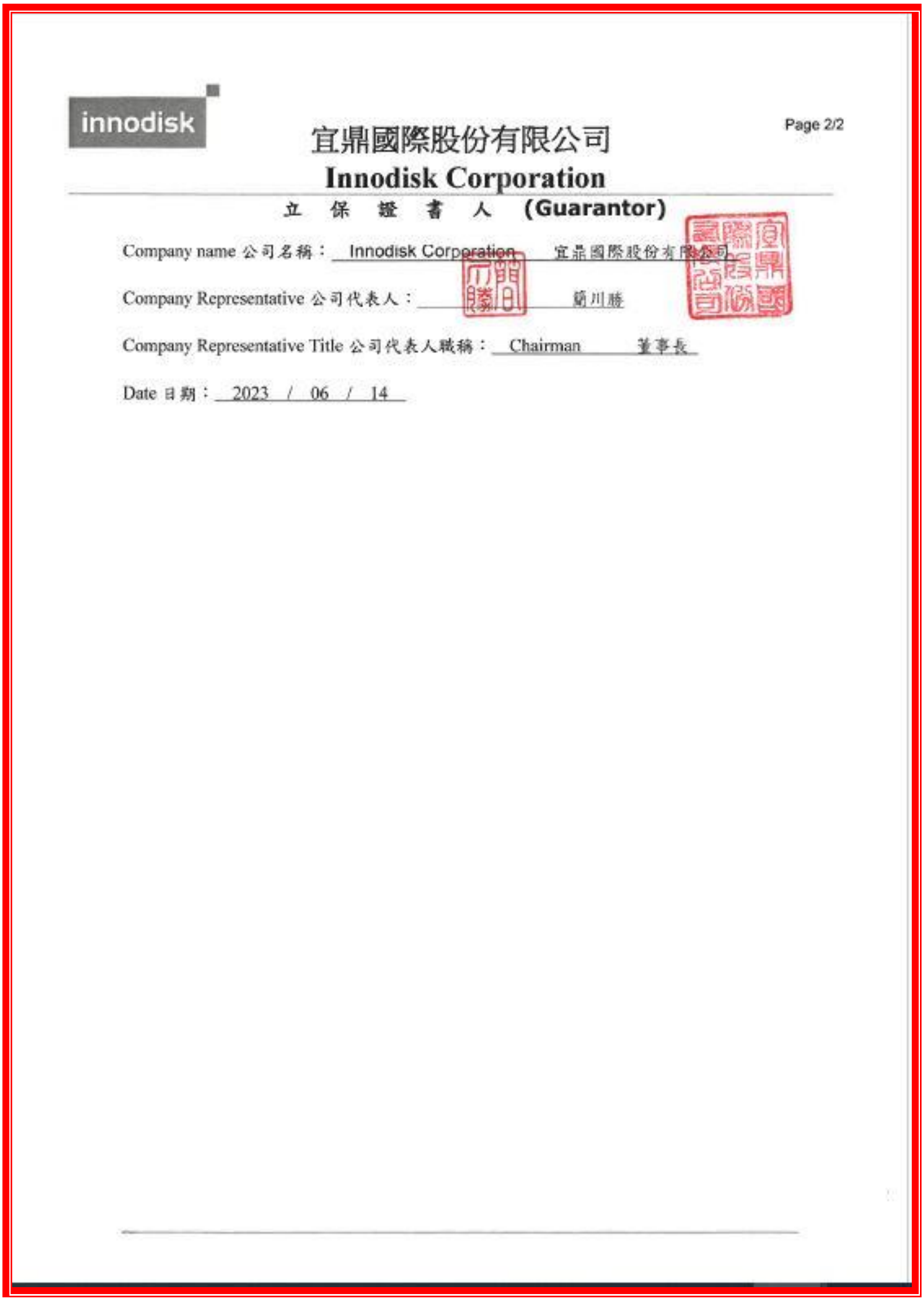
三、本公司聲明我們的產品符合 RoHS 指令的附件中 7(a)、7(c)-I、6(c)允許豁免。
We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.

※ 7(a) Lead in high melting temperature type solders(i.e. lead-based alloys containing 85% by weight or more lead).

※ 7(c)-I Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.

※ 6(c) Copper alloy containing up to 4% lead by weight. (This exemption applies to products that use antennas)

Name of hazardous substance	**Limited of RoHS ppm（mg/kg）**
鉛（Pb）	< 1000 ppm
汞（Hg）	< 1000 ppm
鎘（Cd）	< 100 ppm
六價鉻（Cr 6+）	< 1000 ppm
多溴聯苯（PBBs）	< 1000 ppm
多溴二苯醚（PBDEs）	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯（DEHP）	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯（BBP）	< 1000 ppm
鄰苯二甲酸二丁酯（DBP）	< 1000 ppm
鄰苯二甲酸二異丁酯（DIBP）	< 1000 ppm



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宜鼎國際股份有限公司

Innodisk Corporation

立保證書人 (Guarantor)

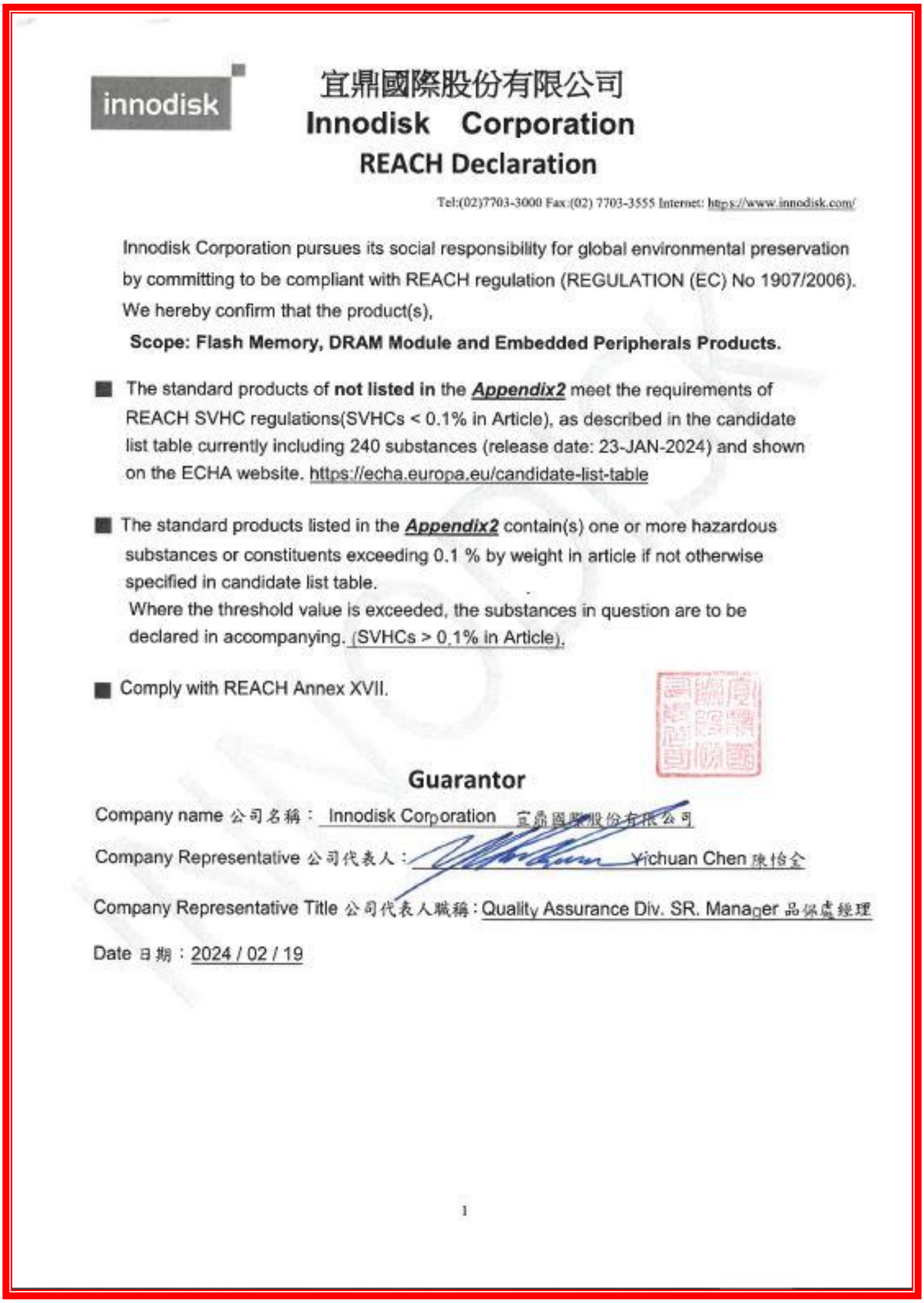
Company name 公司名稱：Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人：簡川勝

Company Representative Title 公司代表人職稱：Chairman 董事長

Date 日期：2023 / 06 / 14

12. REACH Declaration



宜鼎國際股份有限公司

Innodisk Corporation

REACH Declaration

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: https://www.innodisk.com/

Innodisk Corporation pursues its social responsibility for global environmental preservation by committing to be compliant with REACH regulation (REGULATION (EC) No 1907/2006). We hereby confirm that the product(s),

Scope: Flash Memory, DRAM Module and Embedded Peripherals Products.

- The standard products of **not listed** in the ***Appendix2*** meet the requirements of REACH SVHC regulations(SVHCs < 0.1% in Article), as described in the candidate list table currently including 240 substances (release date: 23-JAN-2024) and shown on the ECHA website. https://echa.europa.eu/candidate-list-table
- The standard products listed in the ***Appendix2*** contain(s) one or more hazardous substances or constituents exceeding 0.1 % by weight in article if not otherwise specified in candidate list table.
  Where the threshold value is exceeded, the substances in question are to be declared in accompanying. (SVHCs > 0.1% in Article).
- Comply with REACH Annex XVII.

Guarantor

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Yichuan Chen 陳怡全

Company Representative Title 公司代表人職稱：Quality Assurance Div. SR. Manager 品保處經理

Date 日期：2024 / 02 / 19

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Revision Log

Rev	Date	Modification
0.1	28th July 2025	Preliminary Edition
1.0	28th July 2025	Official Released