

User Manual

AIMB-292

Thin Al Motherboard with 12th/13th/14th Gen Intel® Core™ Processor and MXM GPU Integration



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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

CPU Compatibility

Processor Number	Max TDP	Code Name	Cores/Threads
i9-14900	65W	Raptor Lake-S Refresh	8P+16E/32T
i9-14900T	35W	Raptor Lake-S Refresh	8P+16E/32T
i7-14700	65W	Raptor Lake-S Refresh	8P+12E/28T
i7-14700T	35W	Raptor Lake-S Refresh	8P+12E/28T
i5-14500	65W	Raptor Lake-S Refresh	6P+8E/20T
i5-14500T	35W	Raptor Lake-S Refresh	6P+8E/20T
i5-14400	65W	Raptor Lake-S Refresh	6P+4E/16T
i5-14400T	35W	Raptor Lake-S Refresh	6P+4E/16T
i3-14100	60W	Raptor Lake-S Refresh	4P+0E/8T
i3-14100T	35W	Raptor Lake-S Refresh	4P+0E/8T
Intel® Processor 300	46W	Raptor Lake-S Refresh	2P+0E/4T
Intel® Processor 300T	35W	Raptor Lake-S Refresh	2P+0E/4T
i9-13900	65W	Raptor Lake-S	8P+16E/32T
i9-13900E	65W	Raptor Lake-S	8P+16E/32T
i9-13900TE	35W	Raptor Lake-S	8P+16E/32T
i7-13700	65W	Raptor Lake-S	8P+8E/24T
i7-13700E	65W	Raptor Lake-S	8P+8E/24T
i7-13700TE	35W	Raptor Lake-S	8P+8E/24T
i5-13500	65W	Raptor Lake-S	6P+8E/20T
i5-13500E	65W	Raptor Lake-S	6P+8E/20T
i5-13500TE	35W	Raptor Lake-S	6P+8E/20T
i5-13400	65W	Raptor Lake-S	6P+4E/16T
i5-13400E	65W	Raptor Lake-S	6P+4E/16T
i3-13100	60W	Raptor Lake-S	4P+0E/8T
i3-13100E	60W	Raptor Lake-S	4P+0E/8T
i3-13100TE	35W	Raptor Lake-S	4P+0E/8T
i9-12900	65W	Alder Lake-S	8P+8E/24T
i9-12900E	65W	Alder Lake-S	8P+8E/24T
i9-12900TE	35W	Alder Lake-S	8P+8E/24T
i7-12700	65W	Alder Lake-S	4P+8E/20T
i7-12700E	65W	Alder Lake-S	8P+8E/24T
i7-12700TE	35W	Alder Lake-S	8P+8E/24T
i5-12500	65W	Alder Lake-S	6P+6E/12T
i5-12500E	65W	Alder Lake-S	6P+6E/12T
i5-12500TE	35W	Alder Lake-S	6P+6E/12T
i5-12400	65W	Alder Lake-S	6P+6E/12T
i3-12100	60W	Alder Lake-S	4P+4E/8T
i3-12100E	60W	Alder Lake-S	4P+4E/8T
i3-12100TE	35W	Alder Lake-S	4P+4E/8T
G7400E	46W	Alder Lake-S	2P+2E/4T
G7400TE	35W	Alder Lake-S	2P+2E/4T
G6900E	46W	Alder Lake-S	2P+2E/4T
G6900TE	35W	Alder Lake-S	2P+2E/2T

Memory Compatibility

Category	Speed	Capacity	Vendor	ADVANTECH P/N	ECC
DDR5	5600	48GB	ADVANTECH	SQR-SD5N48G5K6M	N
DDR5	5600	32GB	ADVANTECH	SQR-SD5N32G5K6SNPB	N

Initial Inspection

Before you begin installing your motherboard, please make sure that the following materials have been shipped:

- 1 x AIMB-292 Thin AI Motherboard
- 1 x SATA HDD cable
- 1 x SATA power cable
- 1 x Serial port cable
- 1 x I/O port bracket
- 1 x Startup Manual
- 1 x Warranty Card
- 2 x screws (M3x4.5L)

If any of these items are missing or damaged, contact your distributor or sales representative immediately. We have carefully inspected the AIMB-292 mechanically and electrically before shipment. It should be free of marks and scratches and in perfect working order upon receipt. As you unpack the AIMB-292, check it for signs of shipping damage. (For example, damaged box, scratches, dents, etc.) If it is damaged or it fails to meet the specifications, notify our service department or your local sales representative immediately. Also notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After inspection, we will make arrangements to repair or replace the unit.

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Chapter

General Introduction

1.1 Introduction

The AIMB-292 is engineered with the Intel® Q670E chipset, providing high performance and power efficiency for industrial applications. This motherboard supports Intel® Core™ i9/i7/i5/i3 LGA1700 CPUs up to 65W and dual-channel DDR5 5600MT/s SDRAM, with a maximum capacity of 96GB. It features a diverse range of I/O connectivity, including 2 serial ports, 4 USB 3.2 Gen2x1, 2 USB 2.0, 1 SATA III, and dual 2.5 GbE LAN ports along with 1 GbE LAN port. The AIMB-292 also offers flexible storage options with support for SATA HDDs, M.2 NVMe SSDs, and additional M.2 slots for Wi-Fi, Bluetooth, or LTE by option. This industrial motherboard is designed to accommodate NVIDIA RTX/Quadro GPUs, leveraging an ultra-slender design to deliver exceptional computing power and advanced graphics performance for visual computing and edge intelligence. It features both native Intel® UHD Graphics 770 and discrete NVIDIA Quadro® A4500 GPUs, with support for multiple display outputs including LVDS or eDP, and DP, offering maximum resolutions up to 4K.

1.2 Features

- I/O expansion: 2 serial ports, 4 USB 3.2 Gen2x1 and 2 USB 2.0, 1 SATA III, 1 M.2 M-Key & 1 M.2 E-Key (or 1 M.2 B-key by option), 2.5 GbE LAN and 1 GbE I AN
- Industrial motherboard featuring NVIDIA RTX/Quadro MXM GPU: The AIMB-292 leverages an ultra-slender design to deliver outstanding computing power and superior graphics performance for visual computing and edge intelligence.
- Wide selection of storage devices: SATA HDD, M.2 (M-Key and E-Key or B-Key by option). Customers benefit from the flexibility of using the most suitable storage device for the capacity needed.

1.3 Specifications

1.3.1 System

- **CPU**: Intel® Core™ i9/i7/i5/i3 LGA1700 CPU (up to 65W)
- BIOS: AMI EFI 256 Mbit SPI BIOS.
- System chipset: Intel® Q670E.
- SATA hard disk drive interface:
 - One on-board SATA connector with a data transmission rate up to 6 GB/s
 - One M.2 M-Key slot (2280), supporting NVMe SSD
 - One M.2 E-Key slot (2230), supporting Wi-Fi/BT or One B-Key slot (3042), supporting LTE and storage by option

1.3.2 Memory

■ RAM: 2 x 262-pin SODIMM sockets support dual-channel DDR5 5600MT/s SDRAM, up to 96GB Max.

1.3.3 Input/Output

- **Serial ports:** 2 serial ports support RS-232/422/485 with auto flow control.
- USB port: Supports up to 4 USB 3.2 Gen2x1 and 2 USB 2.0
- **GPIO connector:** 8-bit general purpose Input/Output.

1.3.4 Graphics

- Native GPU: Intel® UHD Graphics 770
- Discrete GPU: NVIDIA Quadro® A4500
- LVDS or eDP: 1 LVDS with maximum resolution up to 1920x1200 @ 60Hz or 1 eDP with maximum resolution up to 1920x1080 @ 60Hz by pass mode.
- **DP:** 2 DP 1.4a from MXM Type-A/B/B+ module, maximum resolution up to 4K at 120Hz and 1 x DP ++ from CPU maximum resolution up to 4096 x 2160 @ 60 Hz

1.3.5 Ethernet LAN

- Supports three 10/100/1000/2500 Mbps Ethernet ports
- Controller:

GbE LAN1: Intel i226-VGbE LAN2: Intel i226-VGbE LAN3: Intel i210-AT

1.3.6 Industrial Features

■ Watchdog timer: The watchdog timer can generate a system reset. It is programmable, with each unit equal to one second or one minute (255 levels).

1.3.7 Mechanical and Environmental Specifications

- Operating temperature: 0 ~ 55°C (32 ~ 131°F), depends on CPU speed and cooler solution
- Storage temperature: -40 ~ 85°C (-40 ~ 185°F).
- **Humidity:** 5 ~ 95% non-condensing.
- Power supply voltage: 24V
- Power consumption: Boost 100.2W; Typical 62.5W (configuration: Intel® Core™ i9-14900 5.4 GHz, 2pcs 48 GB DDR5 5600MHz SODIMM)
- Board size: 170 x 230 mm (6.69" x 9.06").
- Board weight: 1.5 kg

1.4 Jumpers and Connectors

Connectors on the AIMB-292 motherboard link it to devices such as hard disk drives and a keyboard. In addition, the board has a number of jumpers used to configure the system for your application.

The tables below list the function of each of the board jumpers and connectors. Later sections in this chapter give instructions on setting jumpers. Chapter 2 gives instructions for connecting external devices to your motherboard.

Table 1.1: I/O Connector			
	Description	Part Reference	
1	DC IN Connector	DCIN1	
2	RJ-45 Dual LAN ports	LAN1_LAN2	
3	RJ-45 Signal LAN port	LAN3	
4	SATA	SATA1	
5	SIM CARD	SIM1	
6	M.2 E-Key	M2_E1	
7	M.2 M-Key	M2_M1	
8	MXM	MXM16-1	
9	Audio	AUDIO1	
10	DisplayPort	DP1	
11	Dual DisplayPort	DP2_DP3	
12	USB Port 1234	USB1234	

Table 1.2: Box Header			
	Description	Part Reference	
1	COM1 Connector	COM1	
2	COM2 Connector	COM2	
3	EDP/LVDS Connector	EDP1_LVDS1	
4	ATX 5V/PSON Connector	ATX_5VSB1	
5	EDP/LVDS Backlight Inverter Power Connector	INV1	
6	USB 56	USB56	
7	SATA Power	SATA_PWR1	

Part Reference
JFP2
GPIO1
CPUFAN1
SYSFAN1
SYSFAN2
AMP1
VR_PMB1
MXMFAN1

Table 1.4: Jumper Settings			
	Description	Part Reference	
1	Front Panel Header	JFP1	
2	CMOS Reset Header	JCMOS1	
3	AT/ATX Mode Selection	PSON1	
4	EDP Panel/LVDS Panel Voltage Selection	JLVDS1	
5	Program EC Header	JEC1	

1.5 Board Layout: Jumper and Connector Locations

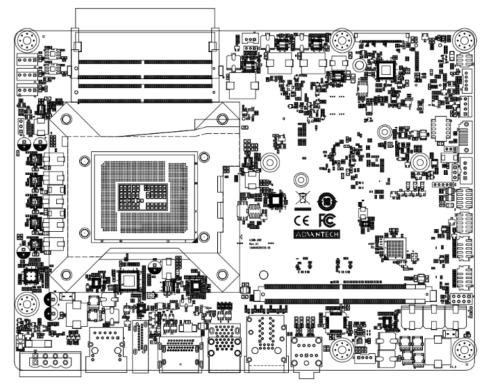


Figure 1.1 Jumper and Connector Locations (Top Side)

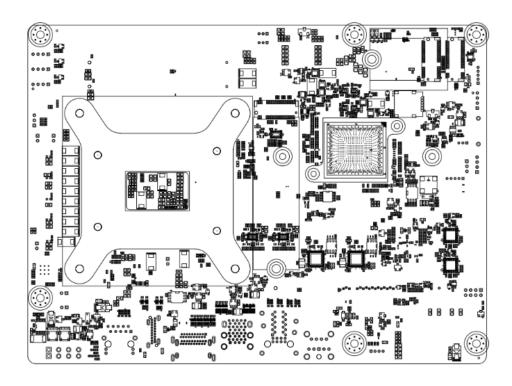


Figure 1.2 Jumper and Connector Locations (Bottom Side)

1.6 AIMB-292 Board Diagram

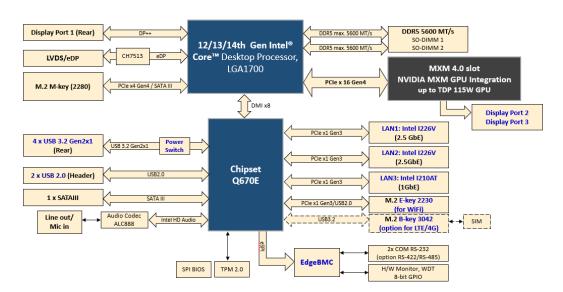


Figure 1.3 AIMB-292 Board Diagram

1.7 Safety Precautions



Warning! Always completely disconnect the power cord from the chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.



Caution! Always ground yourself to remove any static charge before touching the motherboard. Modern electronic devices are very sensitive to electrostatic discharges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis.



Caution! The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.



Caution! There is danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

1.8 **Jumper Settings**

This section provides instructions on how to configure your motherboard by setting the jumpers. It also includes the motherboard's default settings and your options for each jumper.

1.8.1 How to Set Jumpers

You can configure your motherboard to match the needs of your application by setting the jumpers. A jumper is a metal bridge that closes an electrical circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" (or turn ON) a jumper, you connect the pins with the clip. To "open" (or turn OFF) a jumper, you remove the clip. Sometimes a jumper consists of a set of three pins, labeled 1, 2, and 3. In this case you connect either pins 1 and 2, or 2 and 3. A pair of needle-nose pliers may be useful when setting jumpers.

1.8.2 Front Panel Header (JFP1)

Table 1.5: JFP1



Pin	Signal	Pin	Signal
1	3.3V	2	FP_PANSWIN#
3	FP_HDD_LED#	4	GND
5	SMB_DAT_RESUME	6	FP_SYS_RESET#
7	SMB_CLK_RESUME	8	GND

1.8.3 CMOS Reset Header (JCMOS1)

Table 1.6: JCMOS1	
Function	Jumper Settings
1-2 (Default) Keep CMOS data*	1 2 3
2~3 Clear CMOS data	1 2 3

1.8.4 AT/ATX Mode Selection (PSON1)

Table 1.7: PSON1		
Function	Jumper Settings	
1-2 AT Mode	1 2 3	
2-3 (Default) ATX Mode	1 2 3	

1.8.5 EDP Panel/LVDS Panel Voltage Selection (JLVDS1)

Table 1.8: PSON1+JCMOS	
Function	Jumper Setting
Jumper position for 3.3V (Default)	2 4 6
Jumper position for 5V	2 4 6
Jumper position for 12V	2 4 6

1.9 System Memory

The AIMB-292 has two sockets for a 262-pin DDR5 SODIMM. These sockets use a 1.2 V unbuffered double data rate synchronous DRAM (DDR SDRAM). DRAM is available in capacities of 8GB, 16GB, 32GB and 48GB. The sockets can take any combination with SODIMMs of any size, giving a total memory size between 8GB, 16GB, 64GB, up to max 96GB. The AIMB-292 does NOT support error checking and correction (ECC).

1.10 Memory Installation Procedures

To install SODIMMs, first make sure the two handles of the SODIMM socket are in the "open" position, i.e., the handles lean outward. Slowly slide the SODIMM module along the plastic guides on both ends of the socket. Then firmly but gently (avoid pushing down too hard) press the SODIMM module well down into the socket, until you hear a click when the two handles have automatically locked the memory module into the correct position of the SODIMM socket. To remove the memory module, just push both handles outward, and the memory module will be ejected by the mechanism.

1.11 Cache Memory

The AIMB-292 supports a CPU with one of the following built-in full-speed last-level caches:

36MB for Intel® Core™-i9-14900/i9-14900T/i9-13900E/i9-13900TE

33MB for Intel® Core™-i7-14700/i7-14700T

30MB for Intel® Core™ i9-12900E/i9-12900TE

25MB for Intel® Core™ i7-12700E/i7-12700TE

24MB for Intel® Core™ i5-14500/ i5-14500T

20MB for Intel® Core™ i5-14400/ i5-14400T

18MB for Intel® Core™ i5-12500E/i7-12500TE

12MB for Intel® Core™ i3-14100/ i3-14100T/i3-12100E/i7-12100TE

6MB Intel® Pentium® Processor 300/ Intel® Processor 300T/G7400E/G7400TE

4MB Intel® Pentium® G6900E/G6900TE

The built-in second-level cache in the processor yields much higher performance than conventional external cache memory.

1.12 Processor Installation

The AIMB-292 is designed to support 14th Gen Intel® Core™ i9/i7/i5/i3, Pentium®, and Celeron® LGA 1700 processors.

Chapter

Connecting Peripherals

2.1 Introduction

You can access most of the connectors from the top of the board as it is being installed in the chassis. If you have a number of cards installed or have a packed chassis, you may need to partially remove the card to make all the connections.

2.2 I/O Connector

2.2.1 DC-In Connector (DCIN1)

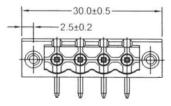


Table 2.1: [DC-In Connector (DCIN1	
Pin	Signal	
1	GND	
2	POWER	
3	POWER	
4	GND	

2.2.2 RJ-45 Dual LAN Ports (LAN1_LAN2)

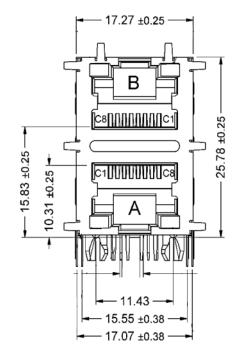


Table 2	2.2: RJ-45 Dual LAN Ports (L	AN1_LA	N2)
Pin	Signal	Pin	Signal
AL1	LAN1_LED2_ACT#	BL1	LAN2_LED2_ACT#
AL2	+V3.3LAN1	BL2	+V3.3LAN1
AL3	LAN1_LED1_2.5G#	BL3	LAN2_LED1_2.5G#
AL4	LAN1_LED1_1G#	BL4	LAN2_LED1_1G#
RA9	GND	RB9	GND
RA1	LAN1_MDI0+	RB1	LAN2_MDI0+
RA2	LAN1_MDI0-	RB2	LAN2_MDI0-
RA3	LAN1_MDI1+	RB3	LAN2_MDI1+
RA4	LAN1_MDI1-	RB4	LAN2_MDI1-
RA5	LAN1_MDI2+	RB5	LAN2_MDI2+
RA6	LAN1_MDI2-	RB6	LAN2_MDI2-
RA7	LAN1_MDI3+	RB7	LAN2_MDI3+
RA8	LAN1_MDI3-	RB8	LAN2_MDI3-
RA10	GND	RB10	GND

2.2.3 RJ-45 Signal LAN Port (LAN3)

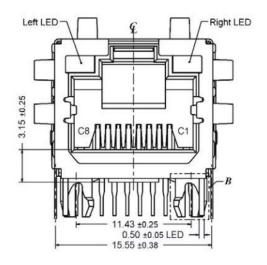


Table	2.3: RJ-45 Signal LAN Port (LAN3)	
Pin	Signal	Pin	Signal
L1	LAN3_LED1	L2	+V3.3_LAN3
L3	LAN3_LED2	L4	LAN3_LED0
R5	GND	R4	LAN3_MDI1-
R1	LAN3_MDI0+	R7	LAN3_MDI2+
R2	LAN3_MDI0-	R8	LAN3_MDI2-
R3	LAN3_MDI1+	R9	LAN3_MDI3+
R10	LAN3_MDI3-	R6	GND

2.2.4 **SATA (SATA1)**



Table 2.4: S	ATA (SATA1)	
Pin	Signal	
1	GND	
2	TX+	
3	TX-	
4	GND	
5	RX-	
6	RX+	
7	GND	

2.2.5 **SIM CARD (SIM1)**

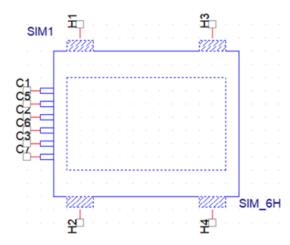


Table 2	2.5: SIM CARD (SIM1)		
Pin	Signal	Pin	Signal
C1	VCC	C5	GND
C2	RST	C6	VPP
C3	CLK	C7	IO

2.2.6 M.2 E-Key (M2_E1)

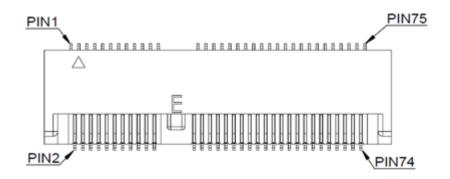


Table	2.6: M.2 E-Key (M2_E1)		
Pin	Signal	Pin	Signal
1	GND	2	+3.3V
3	USB_D+	4	+3.3V
5	USB_D-	6	WLAN_LED1#
7	GND	8	BT_PCMCLK
9	CNV_WR_D1-	10	BT_PCMFRM
11	CNV_WR_D1+	12	BT_PCMIN
13	GND	14	BT_PCMOUT
15	CNV_WR_D0-	16	BT_LED#
17	CNV_WR_D0+	18	GND
19	GND	20	UART WAKE#
21	CNV_WR_CLK-	22	CNV_BRI_RSP
23	CNV_WR_CLK+	24	Connector Key
25	Connector Key	26	Connector Key
27	Connector Key	28	Connector Key
29	Connector Key	30	Connector Key
31	Connector Key	32	CNV_RGI_DT_R
33	GND	34	CNV_RGI_RSP
35	PETp0	36	CNV_BRI_DT_R
37	PETn0	38	CL_RST#
39	GND	40	CL_DAT
41	PERp0	42	CL_CLK
43	PERn0	44	CNV_GNSS_PA_BLANKING
45	GND	46	CNV_MFUART2_TXD
47	REFCLKp0	48	CNV_MFUART2_RXD
49	REFCLKn0	50	SUSCLK
51	GND	52	WLAN_RST#
53	CLKREQ0#	54	BT_RF_KILL#
55	PEWAKE0#	56	WIFI_RF_KILL#
57	GND	58	NC
59	CNV_WT_D1-	60	NC
61	CNV_WT_D1+	62	NC
63	GND	64	NC
65	CNV_WT_D0-	66	NC
67	CNV_WT_D0+	68	NC

Table 2	2.6: M.2 E-Key (M2_E1)		
69	GND	70	NC
71	CNV_WT_CLK-	72	+3.3V
73	CNV_WT_CLK+	74	+3.3V
75	GND		

2.2.7 M.2 M-Key (M2_M1)

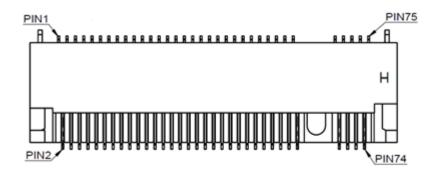
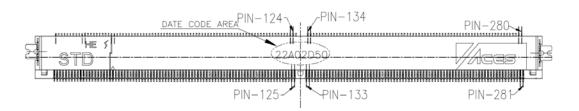


Table	2.7: M.2 E-Key (M2_M1)		
Pin	Signal	Pin	Signal
1	GND	2	3.3V
3	GND	4	3.3V
5	PERn3	6	N/C
7	PERp3	8	N/C
9	GND	10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)
11	PETn3	12	3.3V
13	PETp3	14	3.3V
15	GND	16	3.3V
17	PERn2	18	3.3V
19	PERp2	20	N/C
21	GND	22	N/C
23	PETn2	24	N/C
25	PETp2	26	N/C
27	GND	28	N/C
29	PERn1	30	N/C
31	PERp1	32	N/C
33	GND	34	N/C
35	PETn1	36	N/C
37	PETp1	38	DEVSLP (O)
39	GND	40	N/C
41	PERn0/SATA-B+	42	N/C
43	PERp0/SATA-B-	44	N/C
45	GND	46	N/C
47	PETn0/SATA-A-	48	N/C
49	PETp0/SATA-A+	50	PERST# (O)(0/3.3V) or N/C
51	GND	52	CLKREQ# (I/O)(0/3.3V) or N/C
53	REFCLKn	54	PEWAKE# (I/O)(0/3.3V) or N/C
55	REFCLKp	56	N/C

Table	e 2.7: M.2 E-Key (M2_M1)		
57	GND	58	N/C
59	Connector Key	60	Connector Key
61	Connector Key	62	Connector Key
63	Connector Key	64	Connector Key
65	Connector Key	66	Connector Key
67	N/C	68	SUSCLK(32kHz) (O)(0/3.3V)
69	PEDET (NC-PCIe/GND-SATA)	70	3.3V
71	GND	72	3.3V
73	GND	74	3.3V
75	GND		

2.2.8 MXM (MXM16-1)



2.2.9 Audio (AUDIO1)

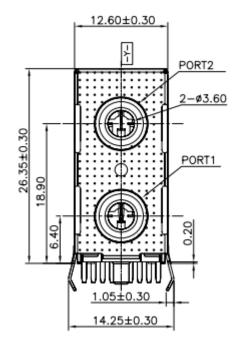


Table 2.8: Audio (A	AUDIO1)
Pin	Signal
1	MIC IN
2	LINE OUT

2.2.10 DisplayPort (DP1)

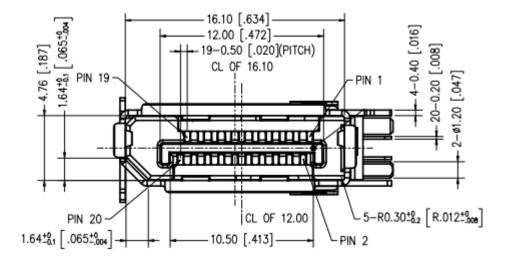


Table	2.9: DisplayPort (DP1)		
Pin	Signal	Pin	Signal
1	DP1_0+	2	GND
3	DP1_0-	4	DP1_1+
5	GND	6	DP1_1-
7	DP1_2+	8	GND
9	DP1_2-	10	DP1_3+
11	GND	12	DP1_3-
13	DP1_HDMI_DNG_DET	14	GND
15	DP1_AUX+	16	GND
17	DP1_AUX-	18	HPD
19	GND	20	POWER

2.2.11 Dual DisplayPort (DP2_DP3)

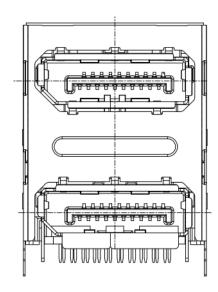


Table 2	10: Dual DisplayPort (DP2_I	OP3)	
Pin	Signal	Pin	Signal
P1	DP3_0+	P21	DP2_0+
P2	GND	P22	GND
P3	DP3_0-	P23	DP2_0-
P4	DP3_1+	P24	DP2_1+
P5	GND	P25	GND
P6	DP3_1-	P26	DP2_1-
P7	DP3_2+	P27	DP2_2+
P8	GND	P28	GND
P9	DP3_2-	P29	DP2_2-
P10	DP3_3+	P30	DP2_3+
P11	GND	P31	GND
P12	DP3_3-	P32	DP2_3-
P13	DP3_HDMI_DNG_DET	P33	DP2_HDMI_DNG_DET
P14	GND	P34	GND
P15	DP3_AUX+	P35	DP2_AUX+
P16	GND	P36	GND
P17	DP3_AUX-	P37	DP2_AUX-
P18	DP3_HPD	P38	DP2_HPD
P19	GND	P39	GND
P20	+3.3V_DP3	P40	+3.3V_DP

2.2.12 USB Port 1234 (USB1234)

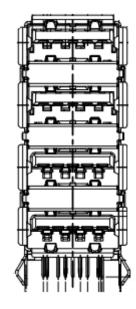


Table 2.11: USB Port 1234 (USB1234)			
Pin	Signal	Pin	Signal
11	+USBV1	12	D1-
13	D1+	14	GND
15	USB31_P1_z_RX-	16	USB31_P1_z_RX+
17	GND	18	USB31_P1_z_TX-
19	USB31_P1_z_TX+		
21	USBV2	22	D2-
23	D2+	24	GND
25	USB31_P2_z_RX-	26	USB31_P2_z_RX+
27	GND	28	USB31_P2_z_TX-
29	USB31_P2_z_TX+		
31	USBV3	32	D3-
33	D3+	34	GND
35	USB31_P3_z_RX-	36	USB31_P3_z_RX+
37	GND	38	USB31_P3_z_TX-
39	USB31_P3_z_TX+	40	
41	USBV4	42	D4-
43	D4+	44	GND
45	USB31_P4_z_RX-	46	USB31_P4_z_RX+
47	GND	48	USB31_P4_z_TX-
49	USB31_P4_z_TX+		

2.3 Box Header

2.3.1 COM1 Connector (COM1)

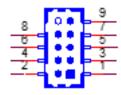


Table 2.12: COM1 Connector (COM1)			
Pin	Signal	Pin	Signal
1	COM1_422_485_TX-	2	COM1_422_485_TX+
3	COM1_422_RX+	4	COM1_422_RX-
5	GND	6	COM1_DSR#
7	COM1_RTS#	8	COM1_CTS#
9	COM1_RI#	10	NC

2.3.2 COM2 Connector (COM2)

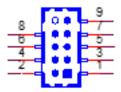


Table 2.13: COM2 Connector (COM2)			
Pin	Signal	Pin	Signal
1	COM2_422_485_TX-	2	COM2_422_485_TX+
3	COM2_422_RX+	4	COM2_422_RX-
5	GND	6	COM2_DSR#
7	COM2_RTS#	8	COM2_CTS#
9	COM2_RI#	10	NC

2.3.3 EDP/LVDS Connector (EDP1_LVDS1)

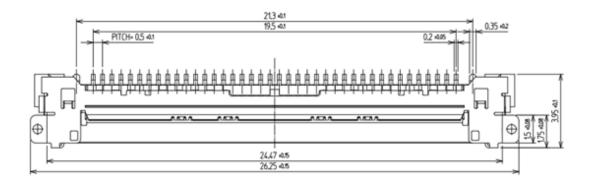


Table 2.14: LVDS P	Pin Definitions
Pin	Signal
1	LVDS1_CTRL
2	GND
3	CH7511_CLK1N
4	CH7511_CLK1P
5	GND
6	CH7511_A0N_C
7	CH7511_A0P_C
8	GND
9	CH7511_A1N_C
10	CH7511_A1P_C
11	GND
12	CH7511_A2N_C
13	CH7511_A2P_C
14	GND
15	NC
16	NC
17	GND
18	LVDS1_A3N_C
19	LVDS1_A3P_C
20	GND
21	LVDS1_CLK2N
22	LVDS1_CLK2P
23	GND
24	LVDS1_A7N_C
25	LVDS1_A7P_C
26	GND
27	LVDS1_A6N_C
28	LVDS1_A6P_C
29	GND
30	LVDS1_A5N_C
31	LVDS1_A5P_C
32	GND
33	LVDS1_A4N_C

Table 2.14: LVDS Pin Definitions		
34	LVDS1_A4P_C	
35	NC	
36	GND	
37	VDD_LVDS1	
38	VDD_LVDS1	
39	VDD_LVDS1	
40	VDD_LVDS1	

Table 2.15: eDP Pi	n Definitions
Pin	Signal
1	LVDS1_CTRL
2	GND
3	AUX_CH_N
4	AUX_CH_P
5	GND
6	NC
7	HPD
8	GND
9	Lane1_N
10	Lane1_P
11	GND
12	Lane0_N
13	Lane0_P
14	GND
17	GND
20	GND
23	GND
26	GND
29	GND
32	GND
35	NC
36	NC
37	VDD_LVDS1
38	VDD_LVDS1
39	VDD_LVDS1
40	VDD_LVDS1

2.3.4 ATX 5V/PSON Connector (ATX_5VSB1)

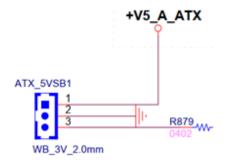


Table 2.16: ATX 5V/PSON Connector (ATX_5VSB1)		
Pin	Signal	
1	+5V_A_ATX	
2	GND	
3	SPS_PS_ON#	

2.3.5 EDP/LVDS Backlight Inverter Power Connector (INV1)

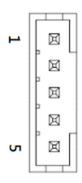


Table 2.17: EDP/LVDS Backlight Inverter Power Connector (INV1)		
Pin	Signal	
1	+12V	
2	GND	
3	BKL EN	
4	BKL CTRL	
5	+5V	

2.3.6 USB 56 (USB56)

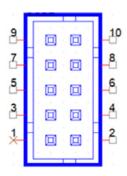


Table	2.18: USB 56 (USB56)		
Pin	Signal	Pin	Signal
1	N.C	2	GND
3	GND	4	GND
5	D+	6	D+
7	D-	8	D-
9	VBUS	10	VBUS

2.3.7 SATA Power (SATA_PWR1)

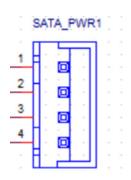


Table 2.19: SATA Power (SATA_PWR1)		
Pin	Signal	
1	+V5	
2	GND	
3	GND	
4	+V12	

2.4 Pin Header

2.4.1 Power LED Pin Header (JFP2)



Table 2.20: Power LED Pin Header (JFP2)		
Pin	Signal	
1	Power LED+	
2	NC	
3	Power LED-	

2.4.2 General Purpose I/O Pin Header (GPIO1)

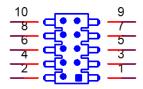


Table 2.21: General Purpose I/O Pin Header (GPIO1)			
Pin	Signal	Pin	Signal
1	GPIO0	2	GPIO4
3	GPIO1	4	GPIO5
5	GPIO2	6	GPIO6
7	GPIO3	8	GPI07
9	VCC_GPIO	10	GND

2.4.3 CPUFAN (CPUFAN1)

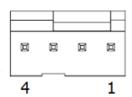


Table 2.22: CPUFAN (CPUFAN1)		
Pin	Signal	
1	GND	
2	CPU FAN VCC	
3	CPU FAN SPEED	
4	CPU FAN PWM	

2.4.4 SYSFAN (SYSFAN1)

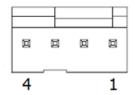


Table 2.23: SYSFAN (SYSFAN1)		
Pin	Signal	
1	GND	
2	SYSTEM FAN VCC	
3	SYSTEM FAN SPEED	
4	SYSTEM FAN PWM	

2.4.5 SYSFAN (SYSFAN2)



Table 2.24: SYSFAN (SYSFAN2)		
Pin	Signal	
1	GND	
2	SYSTEM FAN VCC	
3	SYSTEM FAN SPEED	
4	SYSTEM FAN PWM	

2.4.6 AMP (AMP 1)

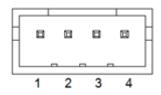


Table 2.25: AMP (AMP 1)		
Pin	Signal	
1	AMP OUT – R+	
2	AMP OUT – R-	
3	AMP OUT – L-	
4	AMP OUT – L+	

2.4.7 Program VCORE Header (VR_PMB1)



Table 2.26: Program VCORE Header (VR_PMB1)		
Pin	Signal	
1	DATA	
2	GND	
3	CLK	

2.4.8 MXM FAN (MXMFAN1)

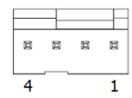


Table 2.27: MXM FAN (MXMFAN1)		
Pin	Signal	
1	GND	
2	MXM FAN VCC	
3	MXM FAN SPEED	
4	MXM FAN PWM	

2.5 Jumper Settings

2.5.1 Front Panel Header (JFP1)

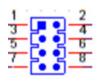


Table 2.28: Front Panel Header (JFP1)			
Pin	Signal	Pin	Signal
1	3.3V	2	FP_PANSWIN#
3	FP_HDD_LED#	4	GND
5	SMB_DAT_RESUME	6	FP_SYS_RESET#
7	SMB_CLK_RESUME	8	GND

2.5.2 CMOS Reset Header (JCMOS1)



Table 2.29: CMOS Reset Header (JCMOS1)		
Pin	Signal	
1	NC	
2	RTCRST#	
3	RTCRST#_PD	

2.5.3 AT/ATX Mode Selection (PSON1)



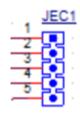
Table 2.30: AT/ATX Mode Selection (PSON1)		
Pin	Signal	
1	VCCAT	
2	+V3_Pull High	
3	VCCATX	

2.5.4 EDP Panel / LVDS Panel Voltage Selection (JEDP1_LVDS1)



Table 2.31: EDP Panel / LVDS Panel Voltage Selection (JEDP1_LVDS1)			
Pin	Signal	Pin	Signal
1	NC	2	+5V
3	+12V	4	VDD
5	NC	6	+3.3V

2.5.5 Program EC Header (JEC1)



Chapter

BIOS Operation

3.1 Introduction

With the AMI BIOS Setup program, you can modify BIOS settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning special features on or off. This chapter describes the basic navigation of the AIMB-292 setup screens.

3.2 BIOS Setup

The AIMB-292 Series system has AMI BIOS built in, with a CMOS SETUP utility that allows users to configure required settings or to activate certain system features. The CMOS SETUP saves the configuration in the CMOS RAM of the motherboard. When the power is turned off, the battery on the board supplies the necessary power to preserve the CMOS RAM.

When the power is turned on, press the button during the BIOS POST (Power-On Self-Test) to access the CMOS SETUP screen.

Table 3.1: Control Keys		
< ↑ >< ↓ >< ← >< → >	Move to select item	
<enter></enter>	Select Item	
<esc></esc>	Main Menu - Quit and not save changes into CMOS Sub-menu - Exit current page and return to Main Menu	
<page +="" up=""></page>	Increase the numeric value or make changes	
<page .="" down=""></page>	Decrease the numeric value or make changes	
<f1></f1>	General help, for Setup Sub-menu	
<f2></f2>	Item Help	
<f5></f5>	Load Previous Values	
<f7></f7>	Load Setup Defaults	
<f10></f10>	Save all CMOS changes	

3.2.1 Main Menu

Press to enter the AMI BIOS CMOS Setup Utility. The Main Menu will appear on the screen. Use the arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.



The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the legend. Above the legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

System Time / System Date

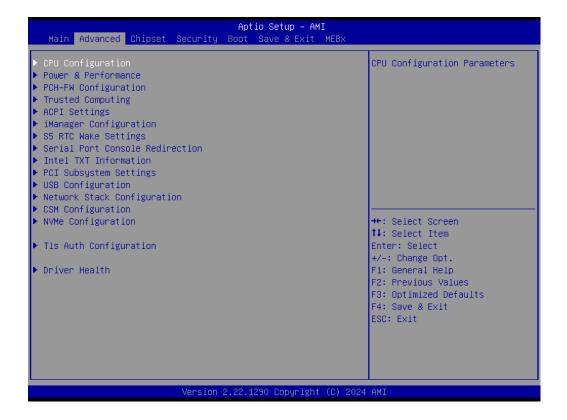
Use this option to change the system time and date. Highlight the System Time or System Date using the <Arrow> keys. Enter new values via the keyboard. Press the <Tab> or <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

3.2.2 Advanced BIOS Features

Select the Advanced tab from the AIMB-292 setup menu to enter the Advanced BIOS setup page. Users can select any item in the left frame of the screen, such as CPU configuration. Select an Advanced BIOS setup option by highlighting the text using the <Arrow> keys. All Advanced BIOS setup options are described in this section. The Advanced BIOS setup menu screen is shown below. The sub-menus are described in the following pages.

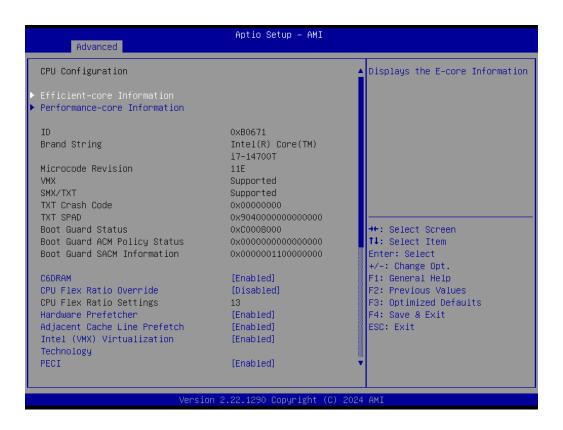
3.2.2.1 CPU Configuration

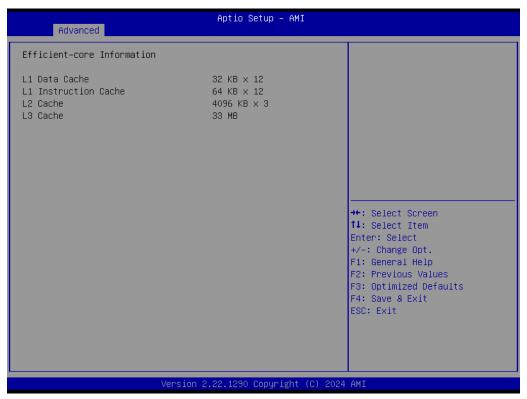
Advanced → CPU Configuration



Efficient-core Information

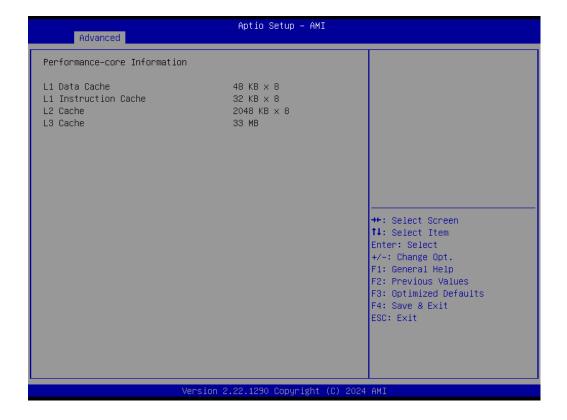
Advanced → CPU Configuration → Efficient-core Information





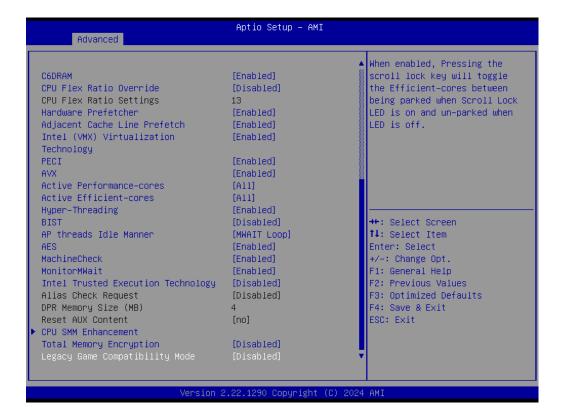
Performance-core Information

Advanced → CPU Configuration → Performance-core Information



CPU SMM Enhancement

Advanced → CPU SMM Enhancement



- SMM Use Delay Indication [Enable]
 Enable/Disable usage of SMM DELAYED MSR for MP sync in SMI.
- SMM Use Block Indication [Enable]
- SMM Use SMM en-US Indication [Enable]

3.2.2.2 Power & Performance

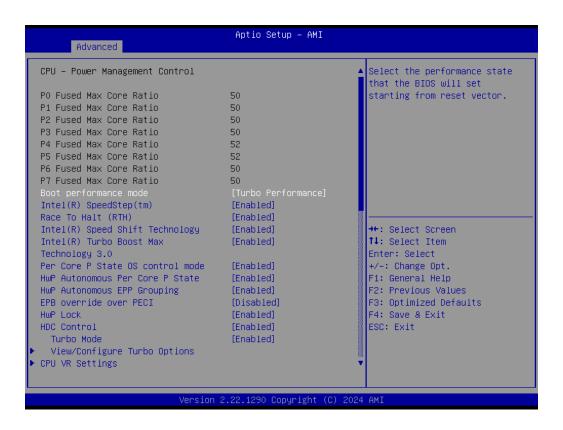
Advanced → Power & Performance



- CPU Power Management Control CPU Power Management Control Options.
- GT Power Management Control

CPU – Power Management Control

Advanced → Power & Performance → CPU – Power Management Control



■ Boot performance mode [Turbo Performance]

Select the performance state that the BIOS will set starting from the reset vector.

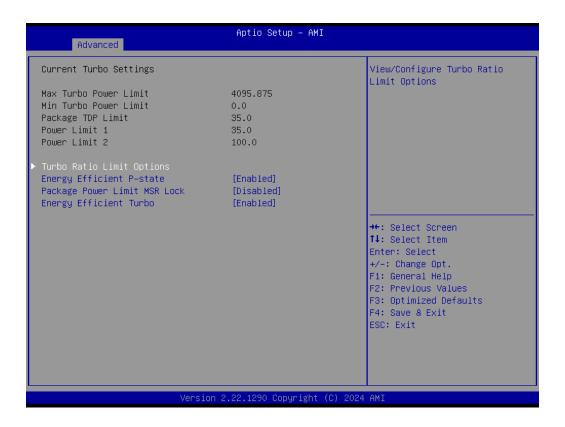
Current Turbo Settings

Advanced \rightarrow Power & Performance \rightarrow CPU – Power Management Control \rightarrow View/ Configure Turbo Ratio



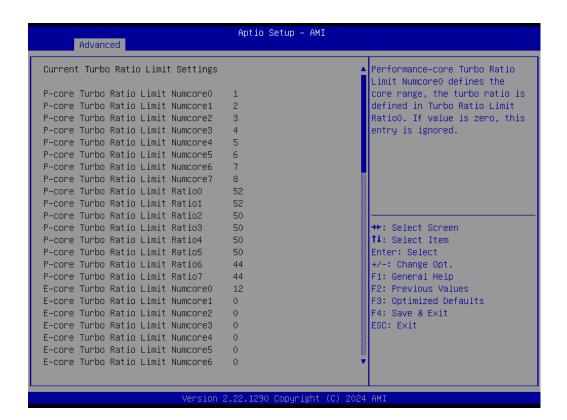
Turbo Ratio Limit Options

Advanced → Power & Performance → CPU – Power Management Control → View/ Configure Turbo Ratio → Turbo Ratio Limit Options



Turbo Ratio Limit Options View/Configure Turbo Ratio Limit Options.

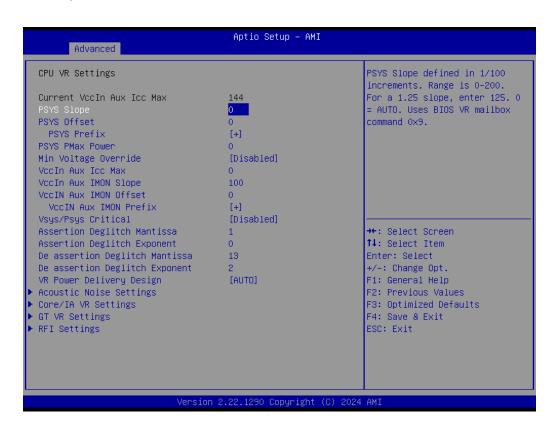
- Energy Efficient P-state [Enable]
- Package Power Limit MSR Lock [Disabled]
- Power Limit 1 Override [Disabled]
- Power Limit 2 Override [Enabled]
- Power Limit 2 0
- Energy Efficient P-state [Disable]



Aptio Setup – AMI Advanced E-core Turbo Ratio Limit Numcore7 Performance–core Turbo Ratio E-core Turbo Ratio Limit Ratio0 Limit Ratio6 defines the turbo 37 E-core Turbo Ratio Limit Ratio1 0 ratio (max is 85 in normal E-core Turbo Ratio Limit Ratio2 0 mode and 120 in core extension E-core Turbo Ratio Limit Ratio3 mode), the core range is E-core Turbo Ratio Limit Ratio4 defined in Turbo Ratio Limit 0 E-core Turbo Ratio Limit Ratio5 Numcore6 Λ E-core Turbo Ratio Limit Ratio6 E-core Turbo Ratio Limit Ratio7 P-core Turbo Ratio Limit NumcoreO P-core Turbo Ratio Limit Numcore1 P-core Turbo Ratio Limit Numcore2 P-core Turbo Ratio Limit Numcore3 →+: Select Screen P-core Turbo Ratio Limit Numcore4 ↑↓: Select Item P-core Turbo Ratio Limit Numcore5 Enter: Select P-core Turbo Ratio Limit Numcore6 +/-: Change Opt. F1: General Help P-core Turbo Ratio Limit Numcore7 P-core Turbo Ratio Limit RatioO 52 F2: Previous Values P-core Turbo Ratio Limit Ratio1 F3: Optimized Defaults P-core Turbo Ratio Limit Ratio2 F4: Save & Exit P-core Turbo Ratio Limit Ratio3 50 ESC: Exit P-core Turbo Ratio Limit Ratio4 50 P-core Turbo Ratio Limit Ratio5

CPU VR Settings

Advanced \rightarrow Power & Performance \rightarrow CPU – Power Management Control \rightarrow CPU VR Settings

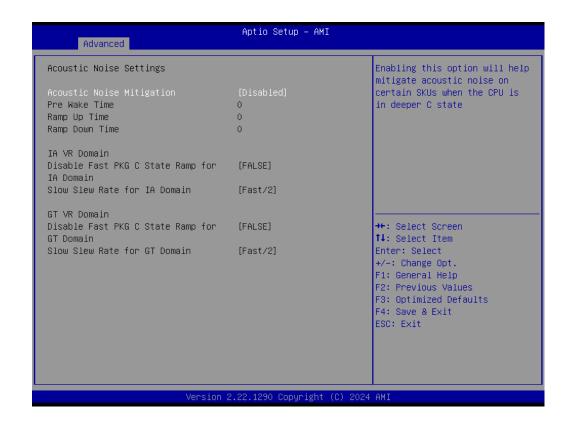


PSYS Slope

PSYS Slope is defined in 1/100 increments. The range is 0-200. For a 1.25 slope, enter 125. 0=Auto. Users BIOS VR mailbox command 0x9.

Acoustic Noise Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → Acoustic Noise Settings



■ Acoustic Noise Mitigation [Disabled]

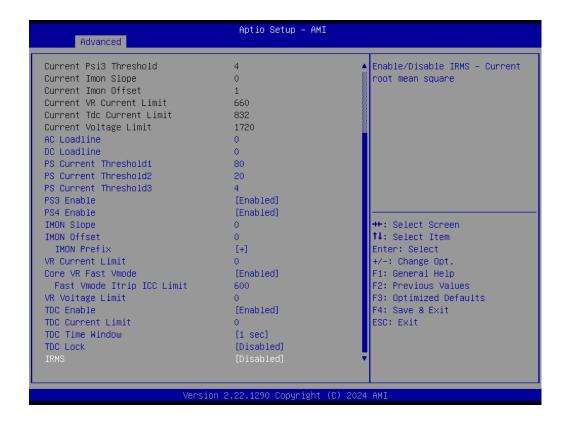
Enabling this option will help mitigate acoustic noise on certain SKUs when the CPU is in a deeper C state.

Core/IA VR Settings

Advanced \rightarrow Power & Performance \rightarrow CPU – Power Management Control \rightarrow CPU VR Settings \rightarrow Core/IA Settings



VR Config Enable [Enabled] VR Config Enable.

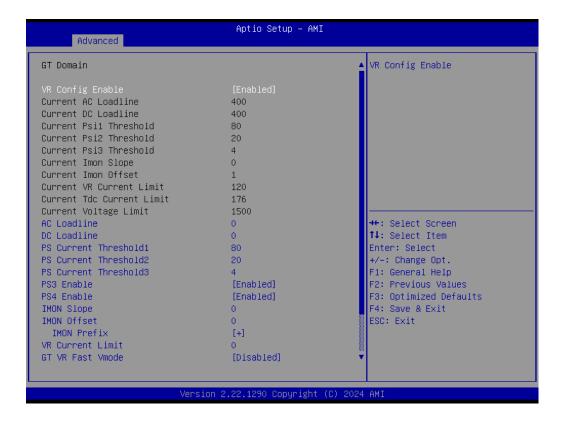


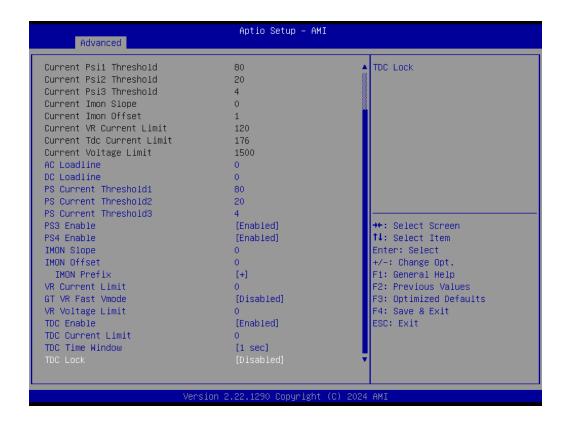
IRMS [Disabled]

Enable/Disable IRMS - Current root mean square.

GT Domain

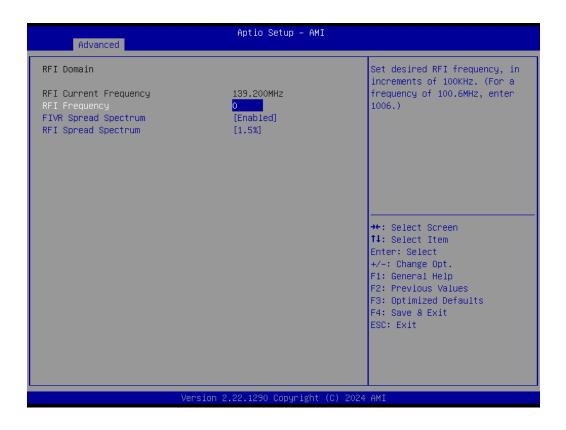
Advanced \to Power & Performance \to CPU – Power Management Control \to CPU VR Settings \to GT Domain





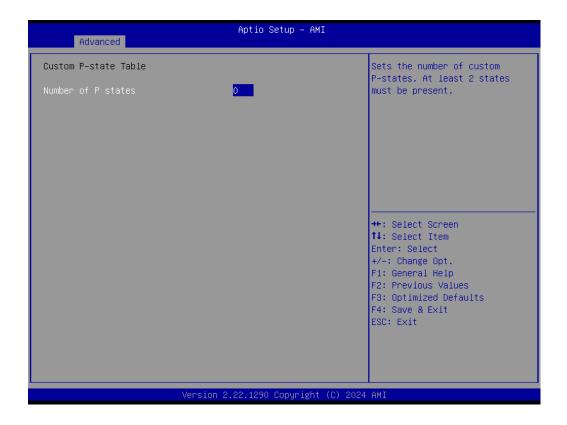
RFI Domain

Advanced \rightarrow Power & Performance \rightarrow CPU – Power Management Control \rightarrow CPU VR Settings \rightarrow RFI Domain



Custom P-state Table

Advanced \rightarrow Power & Performance \rightarrow CPU – Power Management Control \rightarrow Custom P-state Table



Number of P states 0

Sets the number of custom P-states. At least 2 states must be present.

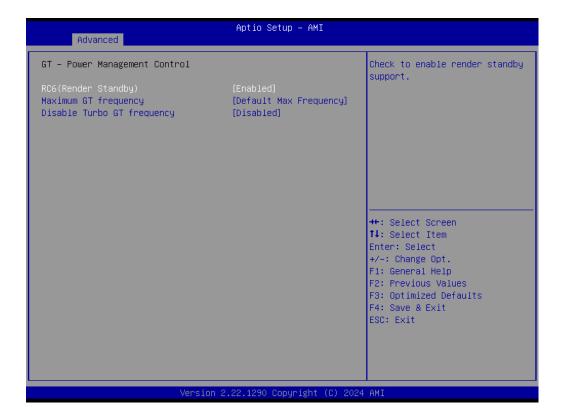
CFG Lock

 $\mathsf{Advanced} \to \mathsf{Power} \ \& \ \mathsf{Performance} \to \mathsf{CPU} - \mathsf{Power} \ \mathsf{Management} \ \mathsf{Control} \to \mathsf{CFG} \ \mathsf{Lock}$



GT – Power Management Control

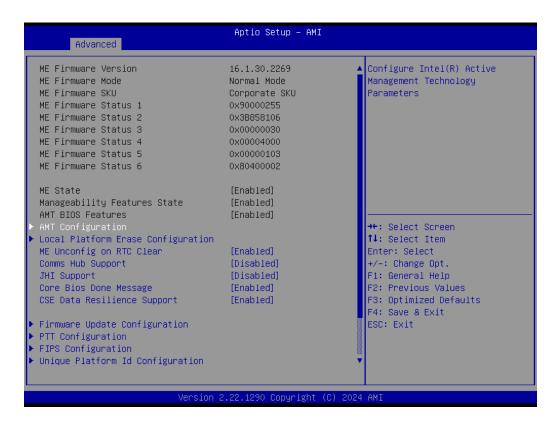
Advanced → Power & Performance → GT – Power Management Control

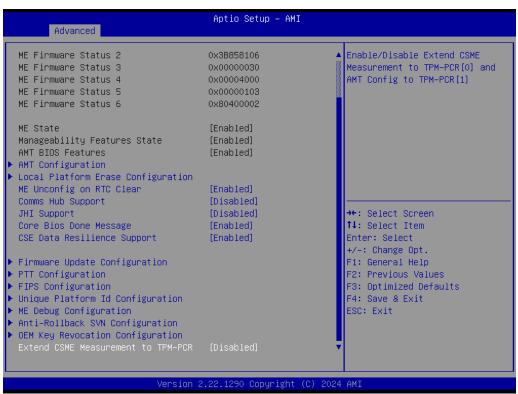


- RC6 (Render Standby) [Enabled]
 Check to enable render standby support.
- Maximum GT frequency [Default Max Frequency]
- Disable Turbo GT frequency [Disabled]

3.2.2.3 PCH-FW Configuration

Advanced → PCH-FW Configuration





AMT Configuration

Advanced → PCH-FW Configuration → AMT Configuration



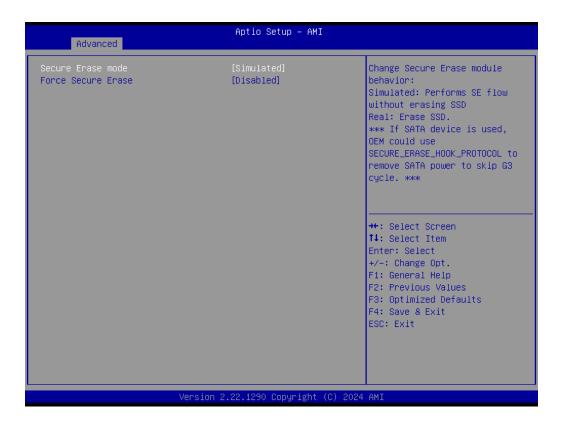
AMT Configuration

Advanced→ PCH-FW Configuration → AMT Configuration → ASF Configuration



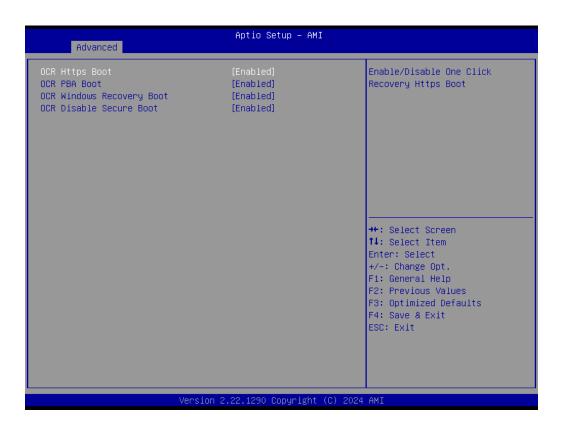
Secure Erase Configuration

Advanced \rightarrow PCH-FW Configuration \rightarrow AMT Configuration \rightarrow Secure Erase Configuration



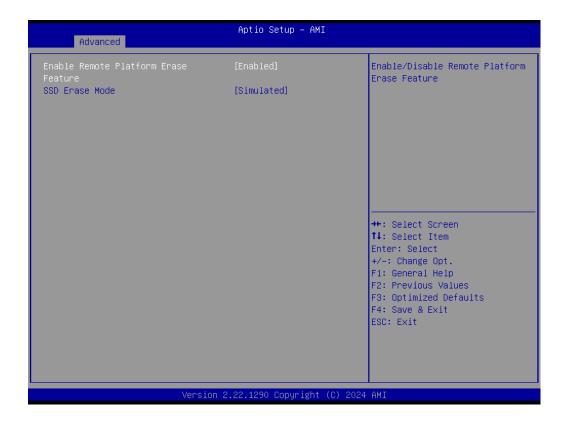
One Click Recovery (OCR) Configuration

Advanced \to PCH-FW Configuration \to AMT Configuration \to One Click Recovery (OCR) Configuration



Enable Remote Platform Erase Feature

Advanced \to PCH-FW Configuration \to AMT Configuration \to Enable Remote Platform Erase Feature



Performance Platform Erase Operations



Firmware Update Configuration

Advanced → PCH-FW Configuration → Firmware Update Configuration



PTT Configuration

Advanced → PCH-FW Configuration → PTT Configuration



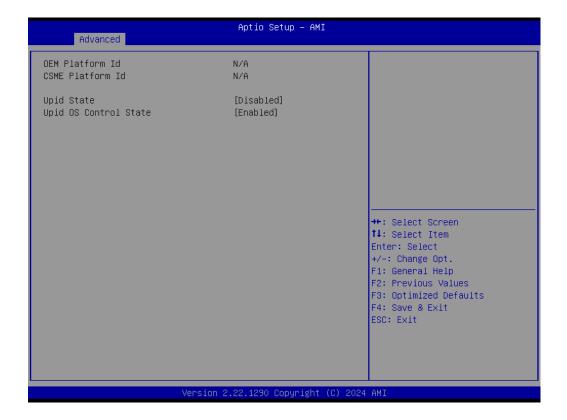
FIPS Configuration

 $Advanced \rightarrow PCH\text{-}FW\ Configuration \rightarrow FIPS\ Configuration$



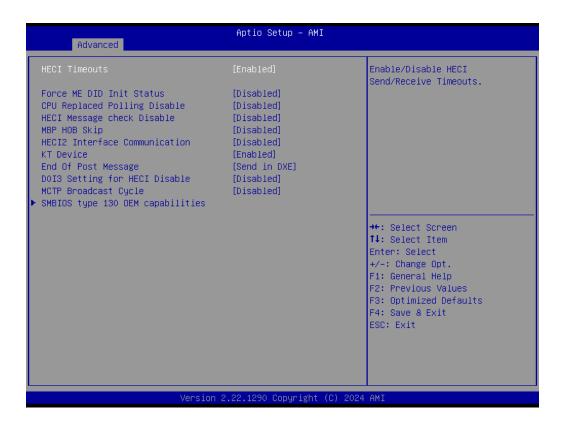
Unique Platform Id Configuration

Advanced → PCH-FW Configuration → Unique Platform Id Configuration



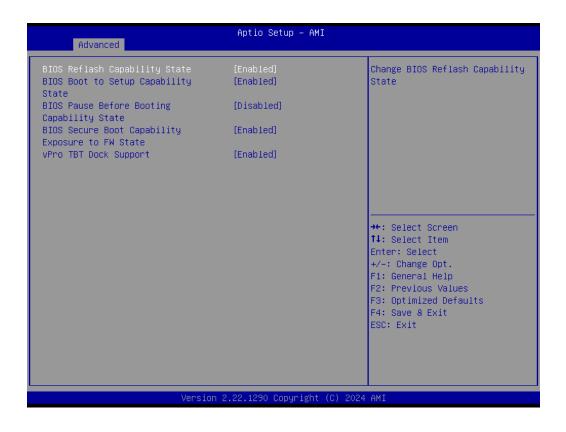
ME Debug Configuration

Advanced → PCH-FW Configuration → ME Debug Configuration



SMBIOS Type 130 OEM Capabilities

Advanced → PCH-FW Configuration → ME Debug Configuration → SMBIOS Type 130 OEM Capabilities



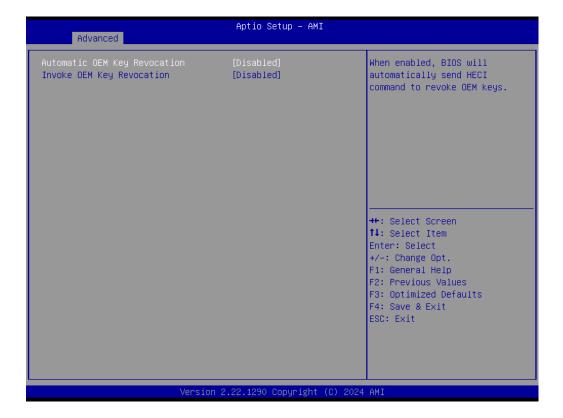
Anti-Rollback SVN Configuration

Advanced → PCH-FW Configuration → Anti-Rollback SVN Configuration



OEM Key Revocation Configuration

Advanced → PCH-FW Configuration → OEM Key Revocation Configuration



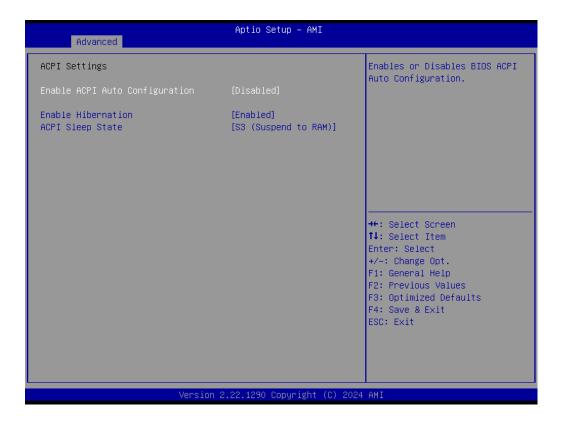
3.2.2.4 Trusted Computing Settings

 $Advanced \rightarrow Trusted \ Computing \\$

Advanced	Aptio Setup – AMI	
TPM 2.0 Device Found Firmware Version: Vendor: Security Device Support Active PCR banks Available PCR banks SHA256 PCR Bank SHA384 PCR Bank Pending operation Platform Hierarchy Storage Hierarchy Endorsement Hierarchy Physical Presence Spec Version TPM 2.0 InterfaceType Device Select	15.23 IFX [Enable] SHA256 SHA256,SHA384 [Enabled] [Disabled] [None] [Enabled]	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
	[Enabled] [Enabled] [1.3] [TIS] [Auto]	++: Select Screen †1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

3.2.2.5 ACPI Settings

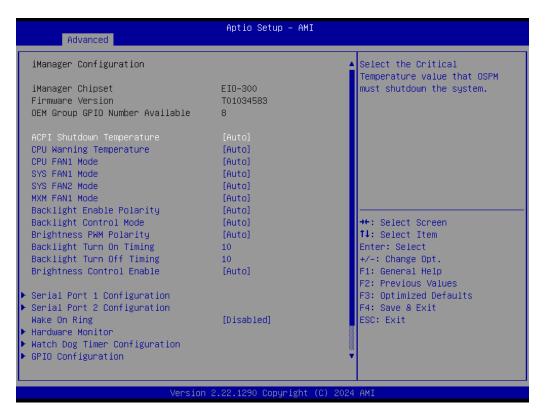
Advanced → ACPI Settings



- Enable ACPI Auto Configuration [Disabled] Enable/Disable BIOS ACPI auto configuration.
- Enable Hibernation [Enabled]
 Enable/Disable the system's ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
- ACPI Sleep State [S3 (Suspend to RAM)]
 Select the ACPI sleep state the system will enter when the SUSPEND button is pressed.

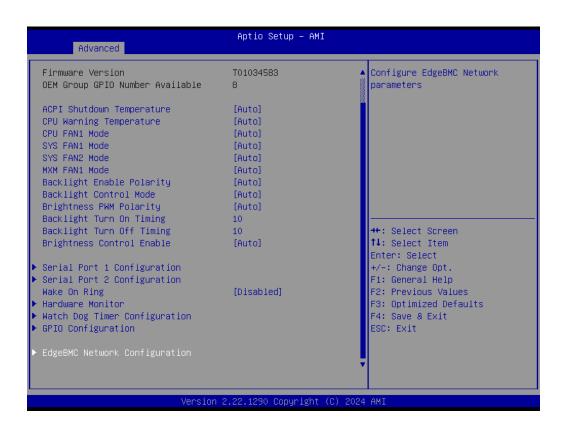
ACPI Shutdown Temperature

Advanced → iManager Configuration → ACPI Shutdown Temperature



3.2.2.6 EdgeBMC Network Configuration

Advanced → iManager Configuration → EdgeBMC Network Configuration





Serial Port 1 Configuration

Advanced → iManager Configuration → Serial Port 1 Configuration



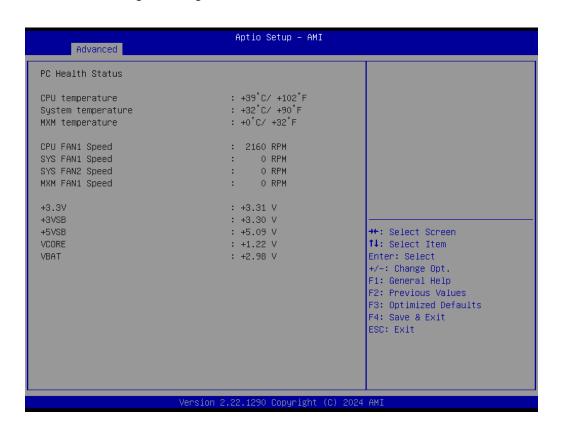
Serial Port 2 Configuration

Advanced → iManager Configuration → Serial Port 2 Configuration



3.2.2.7 **HW Monitor**

Advanced → iManager Configuration → HW Monitor



3.2.2.8 Watch Dog Timer Configuration

Advanced → iManager Configuration → Watch Dog Timer Configuration



3.2.2.9 **GPIO Configuration**

Advanced → iManager Configuration → GPIO Configuration



3.2.2.10 S5 RTC Wake Settings

Advanced → S5 RTC Wake Settings



Wake system from S5 [Disabled]

This item allows you to enable or disable a system wake-on-alarm event.

3.2.2.11 Serial Port Console Redirection

Advanced → Serial Port Console Redirection

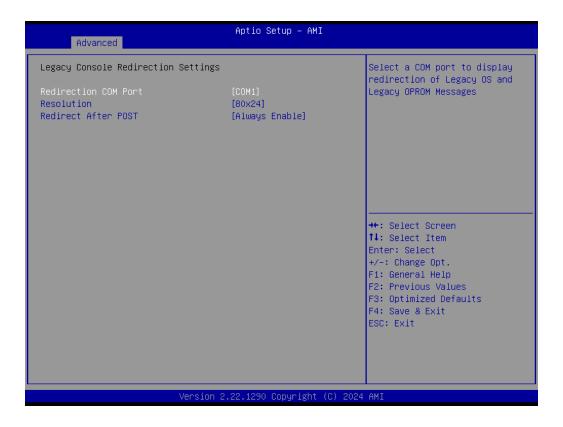


■ Console Redirection [Disabled]

Enable/Disable the console redirection feature.

3.2.2.12 Legacy Console Redirection Settings

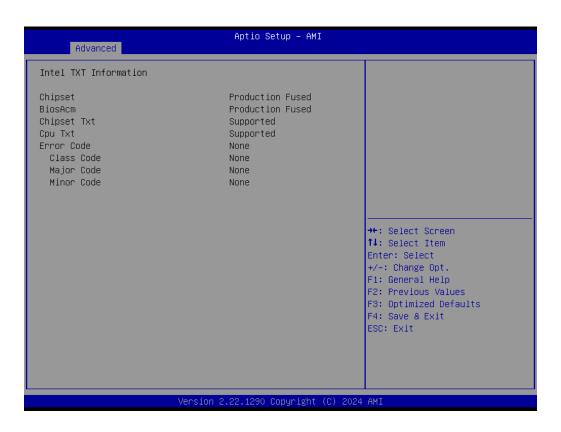
Advanced → Serial Port Console Redirection → Legacy Console Redirection Settings



Redirection COM Port [COM1]

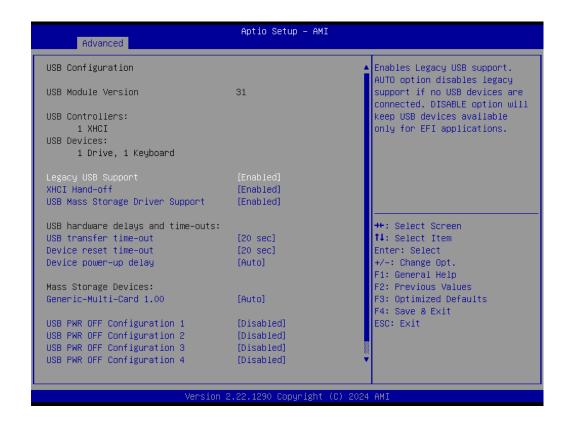
3.2.2.13 Intel TXT Information

Advanced → Intel TXT Information



3.2.2.14 USB Configuration

Advanced → USB Configuration



- Legacy USB Support [Enabled]
- XHCI Hand-off [Enabled]
- USB Mass Storage Driver Support [Enabled]
- USB hardware delays and time-outs
 USB Device transfer & reset time-out and delay setting.
- Mass Storage Devices [Auto] Shows USB mass storage device information.
- USB PWR OFF Configuration 1-6 [Disabled]
 Power off USB Port 1-6 via BIOS setting.

3.2.2.15 Network Stack Configuration

Advanced → Network Stack Configuration



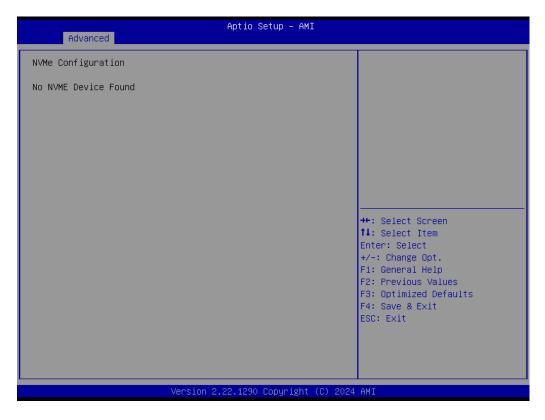
3.2.2.16 CSM Configuration

Advanced → CSM Configuration



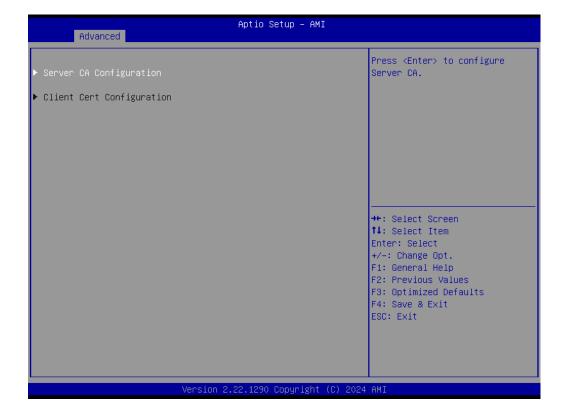
3.2.2.17 NVMe Configuration

Advanced → NVMe Configuration



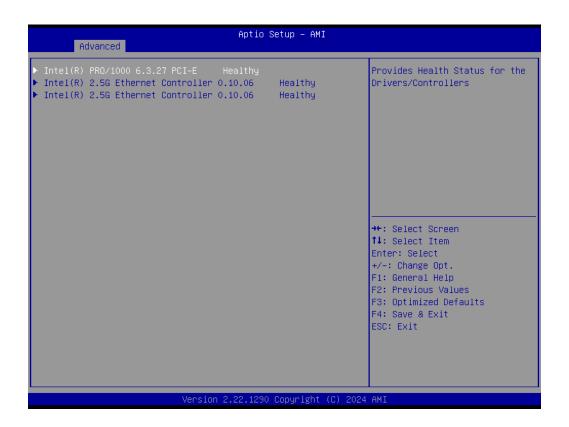
3.2.2.18 TIs Auth Configuration

Advanced → TIs Auth Configuration



3.2.2.19 Driver Health

Advanced → Driver Health



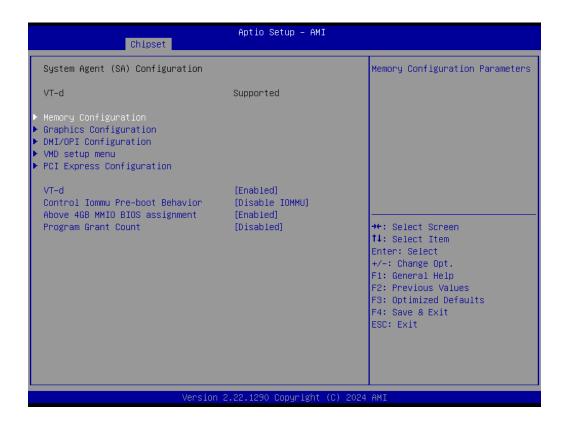
3.2.3 Chipset Configuration Setting

Select the chipset tab from the BIOS setup screen to enter the Chipset Setup screen. Users can select any item in the left frame of the screen, such as PCI Express Configuration, to go to the sub-menu for that item. Users can display a Chipset Setup option by highlighting it using the <Arrow> keys. All Chipset Setup options are described in this section. The Chipset Setup screens are shown below. The submenus are described on the following pages.



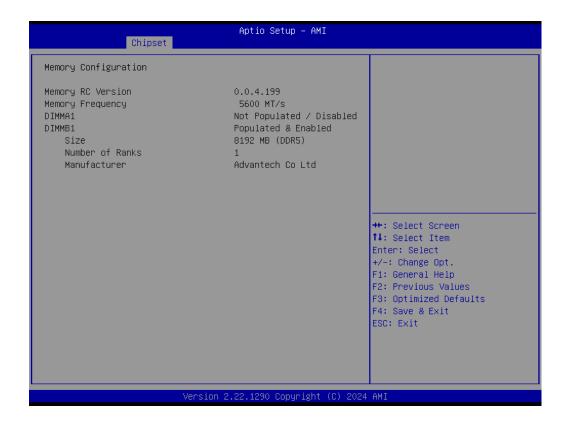
3.2.3.1 System Agent (SA) Configuration

Chipset → System Agent (SA) Configuration



Memory Configuration

Chipset → System Agent (SA) Configuration → Memory Configuration



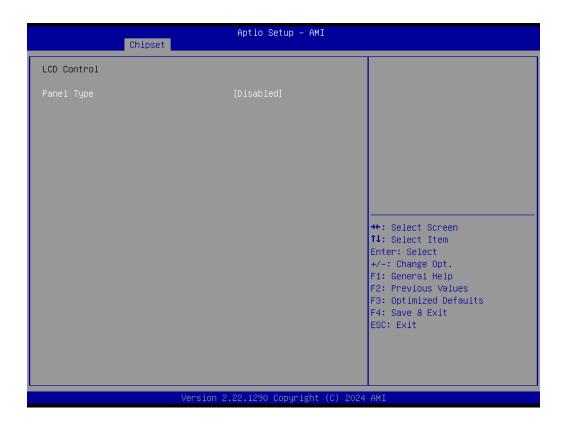
Graphics Configuration

Chipset → System Agent (SA) Configuration → Graphics Configuration



LCD Control

 $\hbox{Chipset} \to \hbox{System Agent (SA) Configuration} \to \hbox{Graphics Configuration} \to \hbox{LCD Control}$



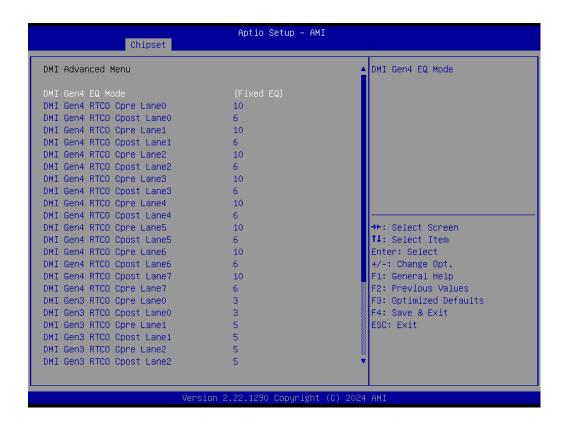
DMI/OPI Configuration

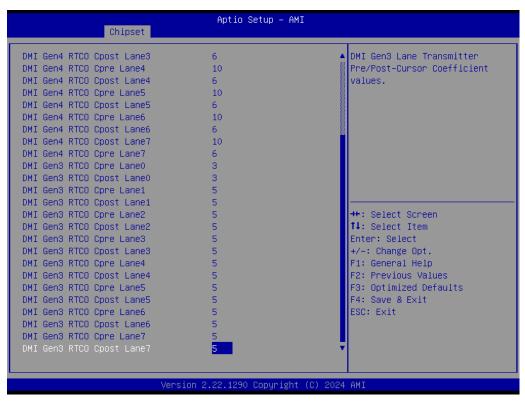
Chipset → System Agent (SA) Configuration → DMI/OPI Configuration



DMI Advanced Menu

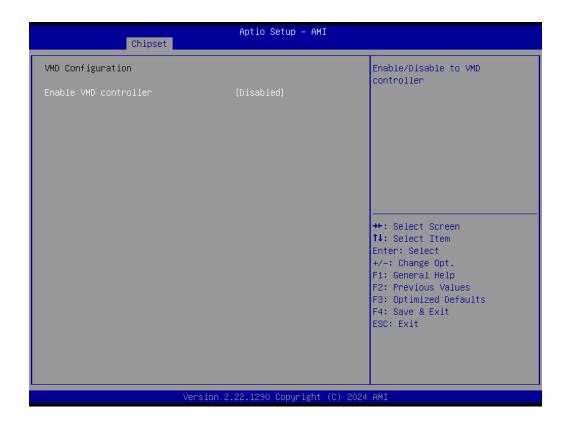
Chipset \to System Agent (SA) Configuration \to DMI/OPI Configuration \to DMI Advanced Menu





VMD Configuration

 $Chipset \to System\ Agent\ (SA)\ Configuration \to VMD\ Configuration$



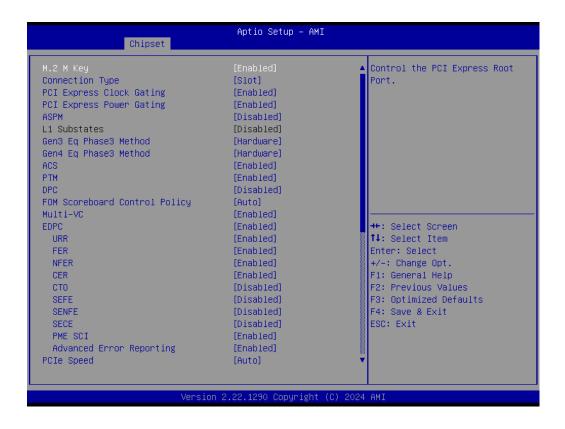
PCI Express Configuration

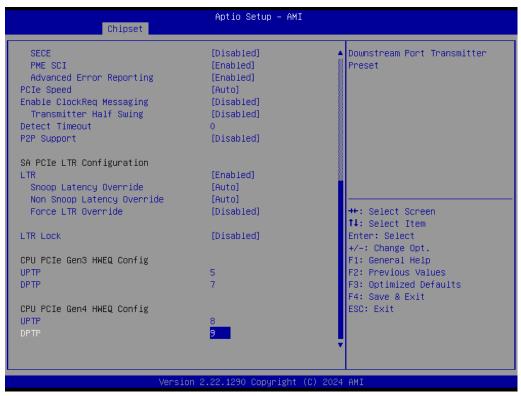
Chipset →System Agent (SA) Configuration → PCI Express Configuration



M.2 M-Key

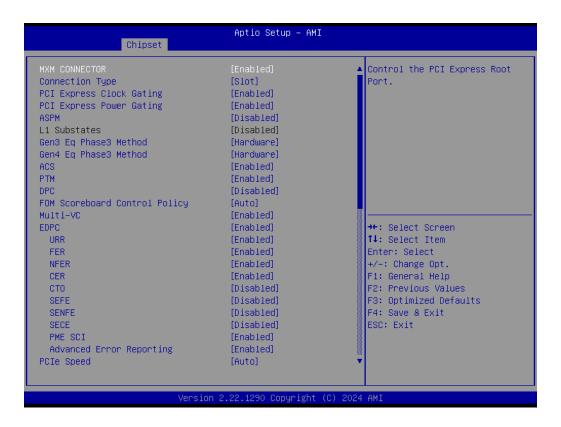
Chipset \rightarrow System Agent (SA) Configuration \rightarrow PCI Express Configuration \rightarrow M.2 M-Key

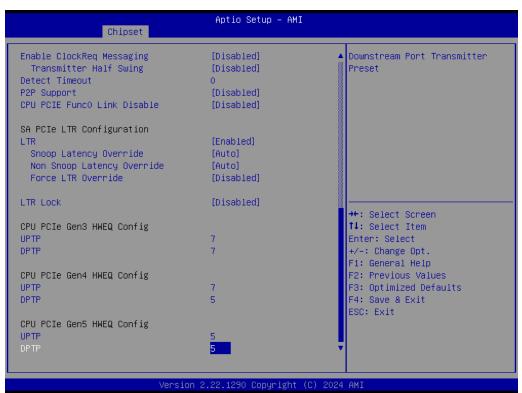




MXM Connector

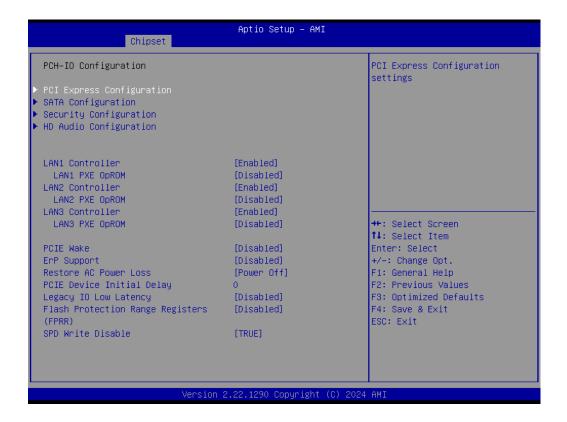
Chipset \rightarrow System Agent (SA) Configuration \rightarrow PCI Express Configuration \rightarrow MXM Connector





3.2.3.2 PCH-I/O Configuration

Chipset → PCH-IO Configuration



- PCI Express Configuration
- SATA Configuration
- Security Configuration
- HD Audio Configuration

PCI Express Configuration

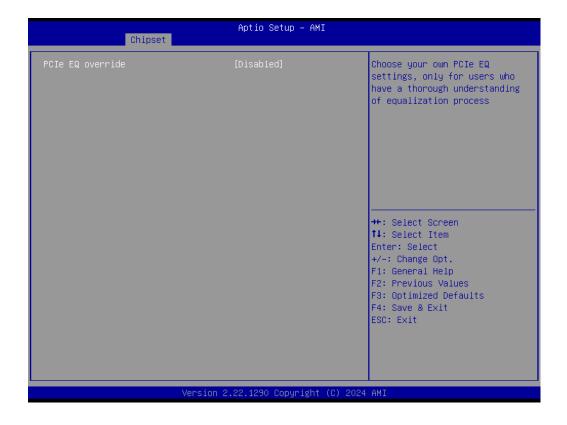
Chipset → PCH-IO Configuration → PCI Express Configuration



- **DMI Link ASPM Control [L1]**
- PCIe function swap [Enabled]
- **PCIe EQ settings**

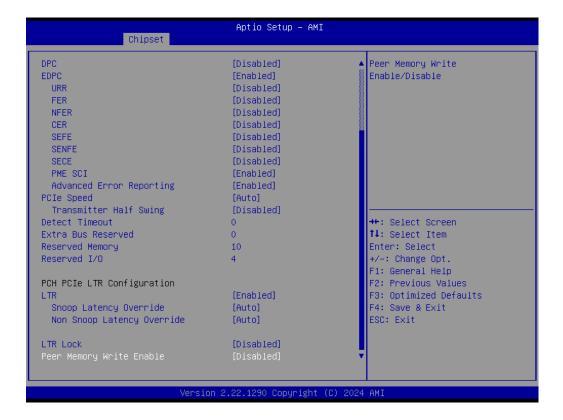
PCIe EQ Settings

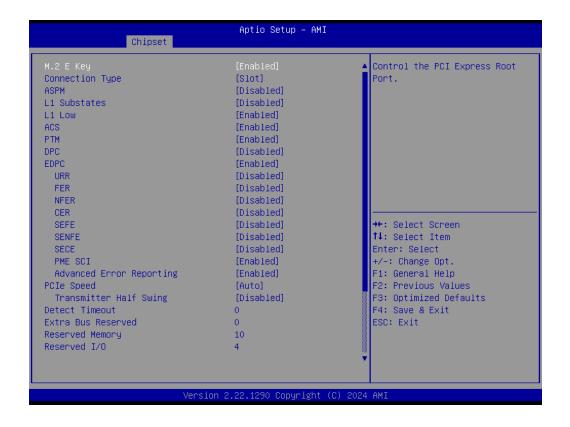
Chipset → PCH-IO Configuration → PCI Express Configuration → PCIe EQ Settings



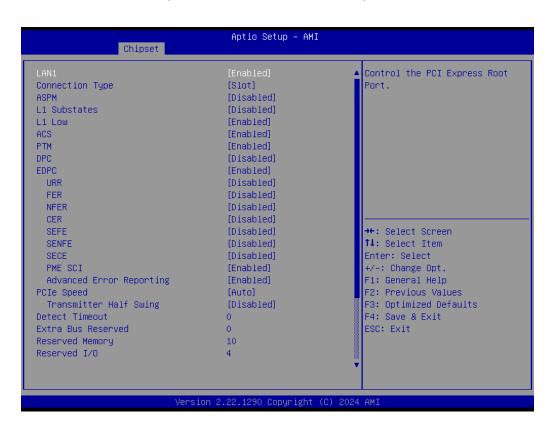
M.2 E-Key

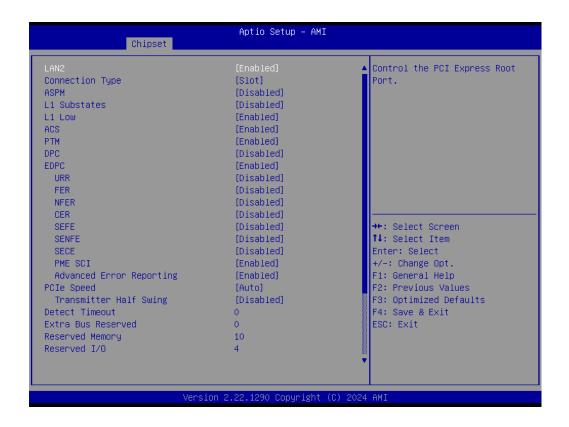
Chipset → PCH-IO Configuration → PCI Express Configuration → M.2 E-Key



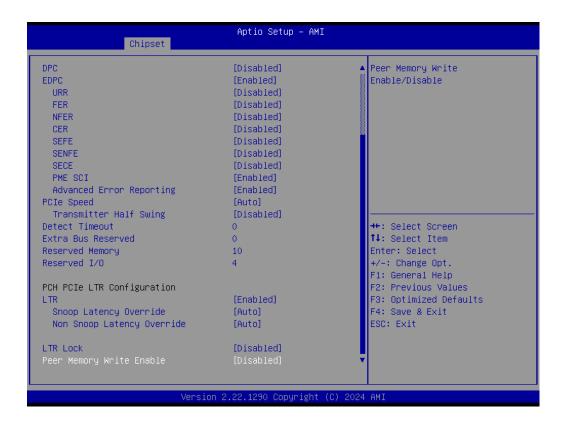


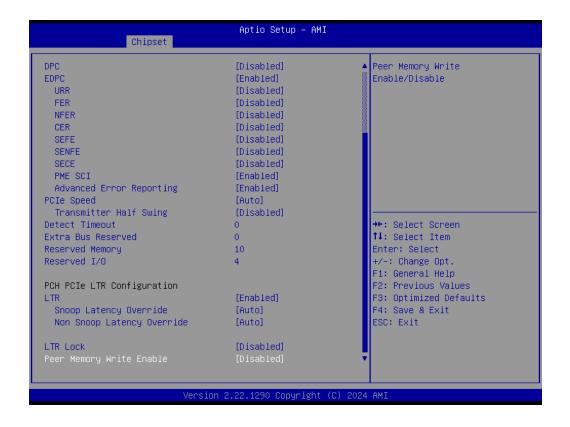
LAN 1Chipset → PCH-IO Configuration → PCI Express Configuration → LAN1



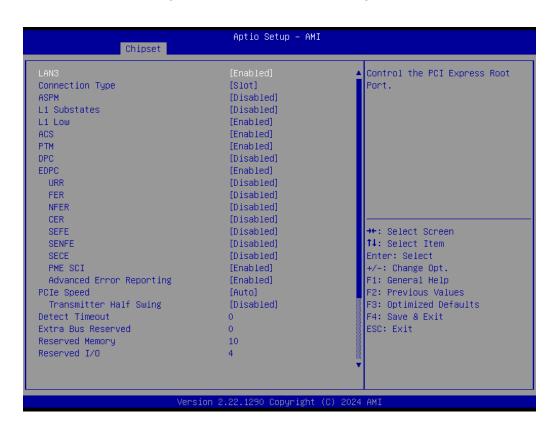


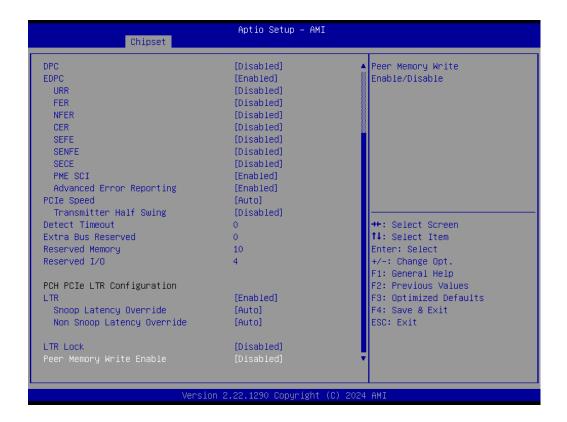
LAN 2 Chipset \rightarrow PCH-IO Configuration \rightarrow PCI Express Configuration \rightarrow LAN2





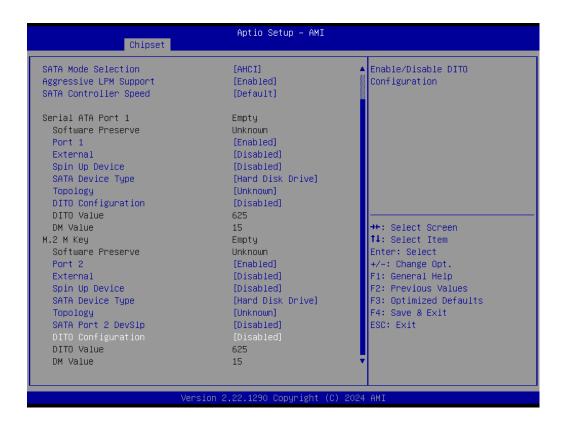
LAN 3 Chipset \rightarrow PCH-IO Configuration \rightarrow PCI Express Configuration \rightarrow LAN3





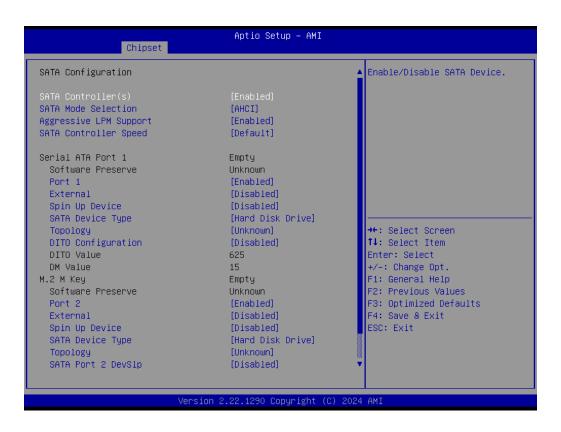
M.2 M-Key

Chipset → PCH-IO Configuration → PCI Express Configuration → M.2 M-Key



SATA Configuration

Chipset → PCH-IO Configuration → SATA Configuration



Security Configuration

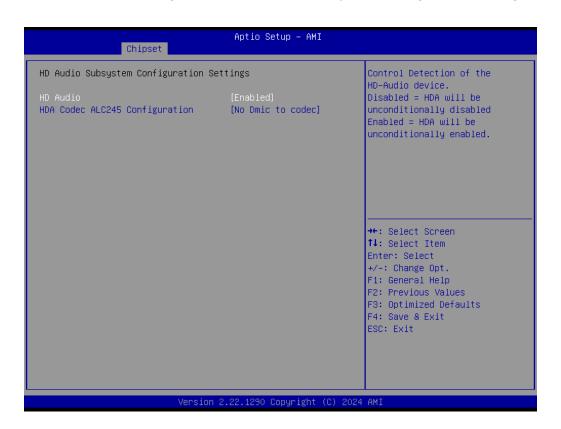
 $\textbf{Chipset} \rightarrow \textbf{PCH-IO Configuration} \rightarrow \textbf{Security Configuration}$



- RTC Memory Lock [Enabled]
- BIOS Lock [Enabled]
- Force unlock on all GPIO pads [Disabled]

HD Audio Subsystem Configuration Settings

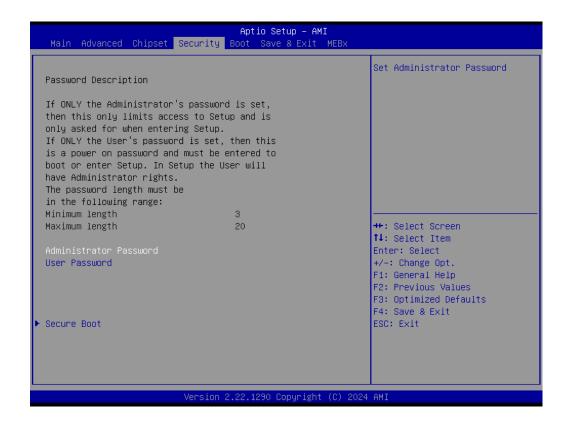
Chipset → PCH-IO Configuration → HD Audio Subsystem Configuration Settings



3.2.4 Security

Secure Boot

Security → Secure Boot



Administrator Password

Select this option and press to access the sub-menu, and then type in the password.

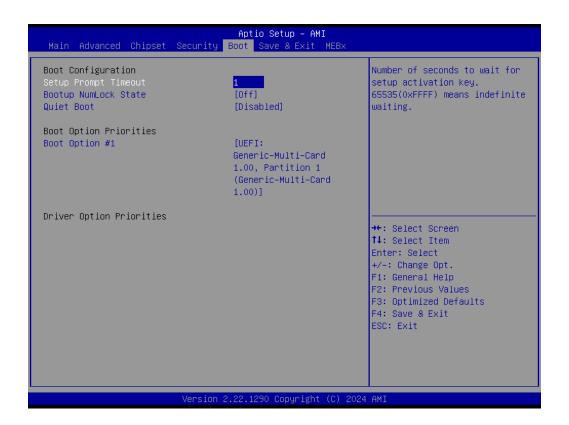
Set the Administrator password.

User Password

Select this option and press to access the sub-menu, and then type in the password.

Set the User Password.

3.2.5 Boot Settings



Setup Prompt Timeout

User the <-> keys to adjust the number of seconds to wait for the setup activation key.

Bootup NumLock State [Off]

On or Off power on state for the NumLock.

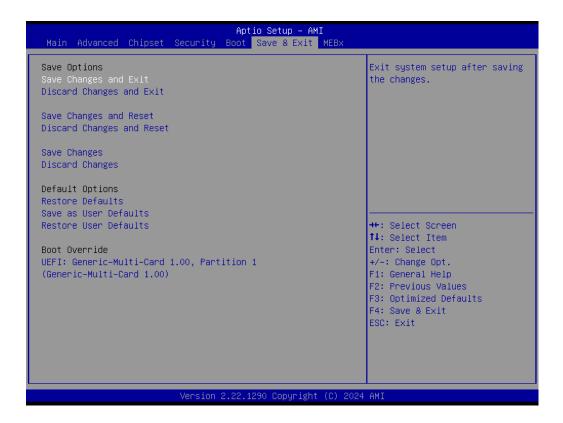
■ Quiet Boot [Disabled]

If this option is set to disabled, the BIOS displays normal POST messages. If enabled, an OEM logo is shown instead of POST messages.

■ Boot Option #1

Choose boot priority from the boot devices.

3.2.6 Save & Exit Configuration



Save Changes and Exit

When users have completed system configuration, select this option to save changes, exit the BIOS setup menu and reboot the computer to take effect of all system configuration parameters.

1.Select Exit Saving Changes from the Exit menu and press <Enter>. The following message appears: Save Configuration Changes and Exit Now? [Ok] [Cancel] 2. Select Ok or Cancel.

Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration.

- 1.Select Exit Discarding Changes from the Exit menu and press <Enter>. The following message appears: Discard Changes and Exit Setup Now? [Ok] [Cancel]
- 2. Select Ok to discard changes and exit. Select Discard Changes from the Exit menu and press <Enter>.

Save Changes and Reset

When users have completed system configuration, select this option to save changes, exit the BIOS setup menu, and reboot the computer to take effect of all system configuration parameters.

- 1.Select Exit Saving Changes from the Exit menu and press <Enter>. The Following message appears: Save Configuration Changes and Exit Now? [Ok] [Cancel]
- 2. Select Ok or Cancel.

Discard Changes and Reset

Select this option to quit Setup without making any permanent changes to the system configuration.

1.Select Reset Discarding Changes from the Exit menu and press <Enter>. The following message appears: Discard Changes and Exit Setup Now? [Ok] [Cancel]

2.Select Ok to discard changes and reset. Discard Changes Select Discard Changes from the Exit menu and press <Enter>.

Restore Defaults

The BIOS automatically configures all setup items to optimal settings when users select this option. Defaults are designed for maximum system performance but may not work best for all computer applications. In particular, do not use the Defaults if the user's computer is experiencing system configuration problems. Select Restore Defaults from the Exit menu and press <Enter>.

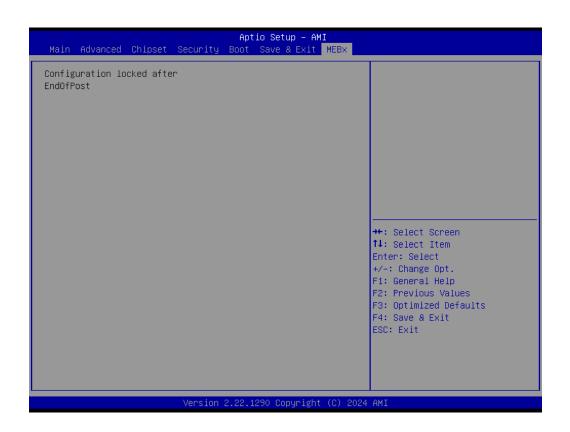
Save as User Default

Save the all current settings as a user default.

■ Restore User Default

Restore all settings to user default values.

3.2.7 **MEB**x



Chapter

Software Introduction & Services

4.1 Introduction

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft® Windows® embedded technology" We enable Windows® Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows® Embedded Software solutions easily and widely available to the embedded computing community.

4.2 Value-Added Software Services

Software API: An interface that defines the ways by which an application program may request services from libraries and/or operating systems. It provides not only the underlying drivers required but also a rich set of user-friendly, intelligent, and integrated interfaces, which speeds development, enhances security, and offers add-on value for Advantech platforms. It plays the role of catalyst between developer and solution, and makes Advantech embedded platforms easier and simpler to adopt and operate with customer applications.

4.2.1 Software API

4.2.1.1 Control

GP I/O



SMBus



General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch the device on/off. Our API also provides Programmable GPIO, which allows developers to dynamically set the GPIO input or output status.

SMBus is the System Management Bus defined by Intel Corporation in 1995. It is used in personal computers and servers for low-speed system management communications. The SMBus API allows a developer to interface with an embedded system environment and transfer serial messages using the SMBus protocols, allowing multiple simultaneous device control.

4.2.1.2 **Display**

Brightness Control



The Brightness Control API allows a developer to access embedded devices and easily control brightness.

Backlight



The Backlight API allows a developer to control the backlight (screen) on/off in embedded devices.

4.2.1.3 **Monitor**

Watchdog



A watchdog timer (WDT) is a device that performs a specific operation after a certain period of time if something goes wrong and the system does not recover on its own. A watchdog timer can be programmed to perform a warm boot (restarting the system) after a certain number of seconds.

Hardware Monitor



The Hardware Monitor (HWM) API is a system health supervision API that inspects certain condition indexes, such as fan speed, temperature, and voltage.

4.2.1.4 Power Saving

CPU Speed



This makes use of Intel® SpeedStep® BIOS technology to save power consumption. The system will automatically adjust the CPU speed depending on the system loading.

System Throttling



This refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. This API allows the user to adjust the clock from 87.5% to 12.5%.

4.2.2 Software Utility

BIOS Flash



The BIOS Flash utility allows customers to update the flash ROM BIOS version, or use it to back up the current BIOS by copying it from the flash chip to a file on a customer's disk. The BIOS Flash utility also provides a command line version and an API for fast implementation into customized applications.

Embedded Security ID



The embedded application is the most important property of a system integrator. It contains valuable intellectual property, design knowledge and innovation, but this makes it vulnerable! Embedded Security ID utility provides reliable security functions for customers to secure their application data within the embedded BIOS.

Monitoring



Monitoring is a utility for a customer to monitor the system health, like voltage, CPU and system temperature and fan speed. These items are important to a device; if critical errors occur and are not solved immediately, permanent damage may be caused.

Chapter

Chipset Software Installation Utility

5.1 Before You Begin

To facilitate the installation of the enhanced display drivers and utility software, read the instructions in this chapter carefully. The drivers for the AIMB-292 are located on the Advantech support website: http://support.advantech.com/Support/. The drivers on the support website will guide and link you to the utilities and drivers under a Windows system. Updates are provided via Service Packs from Microsoft*.

Note!



The driver files on the website are compressed. Do not attempt to install the drivers by copying the files manually. You must download the files and decompress them first. Also, please use the supplied SETUP program to install the drivers.

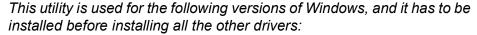
Before you begin, it is important to note that most display drivers need to have the relevant software application already installed in the system prior to installing the enhanced display drivers. In addition, many of the installation procedures assume that you are familiar with both the relevant software applications and operating system commands. Review the relevant operating system commands and the pertinent sections of your application software's user manual before performing the installation.

5.2 Introduction

The Intel® Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured. This is needed for the proper functioning of the following features:

- Core PCI PnP services
- Serial ATA interface support
- USB support
- Identification of Intel® chipset components in the Device Manager

Note!





Windows 10 (64-bit)

Chapter

LAN Configuration

6.1 Introduction

The AIMB-292 system features three Gigabit Ethernet LANs via dedicated PCI Express x1 lanes (Intel® I226-V (LAN1 and LAN2) and Intel® I210-AT (LAN3)) that offer bandwidth of up to 500 MB/sec, eliminating bottlenecks in the flow of network data by incorporating Gigabit Ethernet at 2500 Mbps.

6.2 Features

- Integrated 10/100/1000/2500 Mbps transceiver
- 10/100/1000/2500 Mbps triple-speed MAC
- High-speed RISC core with 24-KB cache
- On-chip voltage regulation
- Wake-on-LAN (WOL) support
- PCI Express x1 host interface

6.3 Installation

Note!



Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.

The Intel® I226-V (LAN1 and LAN2) and Intel® I210-AT (LAN3) Gigabit integrated controllers support all major network operating systems. However, the installation procedure varies between systems. Please follow the driver setup procedure instructions specific to the operating system installed.

6.4 Windows® 10 Driver Setup (Intel® I226-V and Intel® I210-AT)

Download the driver from the support website to your computer and decompress the file. Select "Autorun", then navigate to the directory for your OS.

Note!



Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.



www.advantech.com

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