

AIMB-2710

Mini-ITX motherboard
15th Gen Intel® Core™ Ultra
Processor, LGA1851

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- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

Initial Inspection

Before you begin installing your motherboard, please make sure that the following materials have been shipped:

- 1 x AIMB-2710 motherboard
- 1 x SATA HDD cable
- 1 x SATA power cable
- 1 x Serial port cable
- 1 x I/O port bracket
- 1 x Startup manual
- 1 x Warranty card
- 2 x Screw (M3x4L)
- 1 x SATA PWR cable
- 1 x ATX cable

If any of these items are missing or damaged, contact your distributor or sales representative immediately. We have carefully inspected the AIMB-2710 mechanically and electrically before shipment. It should be free of marks and scratches and in perfect working order upon receipt. As you unpack the AIMB-2710, check it for signs of shipping damage. (For example, damaged box, scratches, dents, etc.) If it is damaged or it fails to meet the specifications, notify our service department or your local sales representative immediately. Also notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After inspection, we will make arrangements to repair or replace the unit.

Contents

Chapter 1 General Information1

1.1	Introduction	2
1.2	Features	2
1.3	Specifications	2
1.3.1	System	2
1.3.2	Memory	2
1.3.3	Input/Output	2
1.3.4	Graphics	2
1.3.5	Ethernet LAN	3
1.3.6	Industrial Features	3
1.3.7	Mechanical and Environmental Specifications	3
1.4	Jumpers and Connectors	3
	Table 1.1: I/O Connector	3
	Table 1.2: Box header	4
	Table 1.3: Pin Header	4
	Table 1.4: Jumper Settings	4
1.5	Board layout: Jumper and Connector Locations	5
	Figure 1.1 Jumper and Connector Location (Top Side)	5
	Figure 1.2 Jumper and Connector Location (Bottom Side)	6
1.6	AIMB-2710 Board Diagram	6
	Figure 1.3 AIMB-2710 Block Diagram	6
1.7	Safety Precautions	7
1.8	Jumper Settings	7
1.8.1	How to Set Jumpers	7
1.8.2	EDP Panel / LVDS Panel Voltage Selection (JEDP1_LVDS1)	8
	Table 1.5: JEDP1_LVDS1	8
1.8.3	CMOS Clear (JCOMS1)	8
	Table 1.6: JCOMS1	8
1.8.4	AT/ATX Mode Selection (PSON1)	8
	Table 1.7: PSON1	8
1.8.5	PCI Express x16 Bifurcation (SW_PEGSEL1)	9
	Table 1.8: SW_PEGSEL1	9
1.8.6	COM1_RI# Pin RI# / 5V / 12V Selection (JSETCOM1_V1)	9
	Table 1.9: JSETCOM1_V1	9
1.8.7	Flash Descriptor Security Override Pin Header (JME1)	10
	Table 1.10: JME1	10
1.9	System Memory	10
1.10	Memory Installation Procedures	10

Chapter 2 Pin Assignments11

2.1	Introduction	12
2.2	I/O Connector	12
2.2.1	Direct Current Input Connector (DCIN1)	12
	Table 2.1: DCIN1	12
2.2.2	Display Port / HDMI Connector (DP1+HDMI1)	12
	Table 2.2: DP1+HDMI1	12
2.2.3	TBT4 / USB4 Type Connector (USBC1)	13
	Table 2.3: USBC1	13
2.2.4	RJ45 + USB3.2 Stack Connector (LAN1_USB12)	14
	Table 2.4: LAN1_USB12	14
2.2.5	RJ45 + USB3.2 Stack Connector (LAN2_USB78)	14
	Table 2.5: LAN2_USB78	14
2.2.6	HD Audio Interface (Analog) (AUDIO1)	15

	Table 2.6: AUDIO1	15
2.2.7	PCI Express x16 Slot (PCIEX16_1).....	15
	Table 2.7: PCIEX16_1	15
2.2.8	M.2 E-KEY Connector (M2_E1).....	17
	Table 2.8: M2E1	17
2.2.9	M.2 M-KEY Connector (M2_M1)	18
	Table 2.9: M2M1	18
2.2.10	Serial ATA Interface Connector (SATA1)	19
	Table 2.10: SATA1	19
2.2.11	Serial ATA Interface Connector (SATA2)	20
	Table 2.11: SATA2	20
2.2.12	DDR5 SO-DIMM Socket A1 (DIMMA1)	20
2.2.13	DDR5 SO-DIMM Socket B1 (DIMMB1)	20
2.3	Box Header	20
2.3.1	ATX Supported 3-Pin Header on Board (ATX_5VSB1).....	20
	Table 2.12: ATX_5VSB1	20
2.3.2	USB2.0 Front Panel Header (USB2_56)	21
	Table 2.13: USB2_56	21
2.3.3	Universal Serial Bus 3.2 (USB3_34).....	21
	Table 2.14: USB3_34	21
2.3.4	CMOS Battery Connector (BAT1).....	22
	Table 2.15: BAT1	22
2.3.5	COM1 Connector (COM1).....	22
	Table 2.16: COM1	22
2.3.6	COM2 Connector (COM2).....	22
	Table 2.17: COM2	22
2.3.7	EDP / LVDS Backlight Inverter Power Connector (INV1)	23
	Table 2.18: INV1	23
2.3.8	EDP Connector / LVDS Connector (EDP1_LVDS1).....	23
	Table 2.19: LVDS1:	23
	Table 2.20: EDP1	24
2.3.9	SATA Power Connector (SATA_PWR1)	24
	Table 2.21: SATA_PWR1	24
2.4	Pin Header	25
2.4.1	Audio Amplifier Output Pin Header (AMP1).....	25
	Table 2.22: AMP1	25
2.4.2	Flash Descriptor Security Override Pin Header (JME1)	25
	Table 2.23: JME1	25
2.4.3	Case Open Connector (JCASE1).....	25
	Table 2.24: JCASE1	25
2.4.4	8-bits General Purpose I/O Pin header (GPIO1)	26
	Table 2.25: GPIO1	26
2.4.5	CPU FAN Connector (CPUFAN1)	26
	Table 2.26: CPUFAN1	26
2.4.6	System FAN Connector (SYSFAN1)	26
	Table 2.27: SYSFAN1	26
2.4.7	IT5782VG Programming Header (JSMBUS1).....	27
	Table 2.28: JSMBUS1	27
2.4.8	Power LED Pin Header (JFP2).....	27
	Table 2.29: JFP2	27
2.4.9	LED Port 80 Connector (LED_P80).....	27
	Table 2.30: LED_P80	27
2.4.10	VR Programming Header (VR_PMB1)	28
	Table 2.31: VR_PMB1	28
2.4.11	SPI BIOS Flash Socket (SPI1)	28
	Table 2.32: SPI1	28
2.5	Jumper Setting.....	29
2.5.1	COMS Mode Selection (JCMOS1)	29
	Table 2.33: JCMOS1	29
2.5.2	AT / ATX Mode Selection (PSON1).....	29

	Table 2.34: PSON1	29
2.5.3	COM1 RI# Selection Pin Header (JSETCOM1_V1)	29
	Table 2.35: JSETCOM1_V1	29
2.5.4	PWRBTN#/ RESET#/HDD LED/ Serial Bus From HW Monitor IC (JFP1)	30
	Table 2.36: JFP1	30
2.5.5	EDP Panel / LVDS Panel Voltage Selection (JEDP1_LVDS1)...	30
	Table 2.37: JEDP1_LVDS1	30
2.5.6	PCI Express x16 Bifurcation (SW_PEGSEL1).....	30
	Table 2.38: SW_PEGSEL1	30

Chapter 3 BIOS Operation31

3.1	Introduction	32
3.2	BIOS Setup	32
3.2.1	Main Menu	33
3.2.2	Advanced BIOS Features	34
3.2.3	Security	75
3.2.4	Boot Settings.....	76
3.2.5	Save & Exit Configuration	77
3.2.6	MEBx	77

Chapter 4 Software Introduction & Service79

4.1	Introduction	80
4.2	Value-Added Software Services	80
4.2.1	Software API	80
4.2.2	Software Utility	82

Chapter 5 Chipset Software Installation Utility 83

5.1	Before You Begin	84
5.2	Introduction	84

Chapter 6 LAN Configuration.....85

6.1	Introduction	86
6.2	Features	86
6.3	Installation	86
6.4	Windows® 11 Driver Setup	86

Chapter 1

General Information

1.1 Introduction

The AIMB-2710 is powered by 15th Gen Intel® Core™ Ultra 9/7/5 processors (LGA1851, up to 65W TDP), delivering robust performance and power efficiency for a wide range of industrial applications. This Mini-ITX motherboard adopts the Intel® Q870 or H810 chipset and supports up to 96GB of dual-channel DDR5 6400 MT/s memory across two 262-pin CSODIMM slots. It features extensive I/O connectivity, including 2 COM ports, 1 x USB Type-C, 4 x USB3.2 Gen2x1 and 2 x USB3.2 Gen1x1, and dual Ethernet ports supporting 2.5 GbE. For storage and expansion, the AIMB-2710 offers 2 SATA III ports and 2 M.2 slots, including one M-key slots for NVMe SSDs and an E-Key slot for wireless connectivity such as WiFi or Bluetooth. The motherboard supports high-performance graphics with Intel Enhanced Intel® Xe LPG architecture, providing up to one HDMI 2.1 TMDS, two DP 1.4 (1 via USB Type-C) and one LVDS (or one eDP by option)

1.2 Features

- **I/O Expansion:** 2 x serial ports, 1 x USB Type-C, 4 x USB3.2, 1 x Gen2 USB, 2 x USB3.2, 1 x USB Gen1, 2 SATA III, 1 x M.2 M-Key, 2 x M.2 E-Key, and 2 x 2.5 GbE LAN.
- **Mini-ITX Form Factor:** AIMB-2710 is a mini-ITX motherboard.
- **Wide Selection of Storage Devices:** SATA HDD, M.2 (M-Key and E-Key). Customers benefit from the flexibility of using the most suitable storage device for the capacity needed.
- **Optimized Integrated Graphics:** Intel Enhanced Intel® Xe LPG architecture

1.3 Specifications

1.3.1 System

- **CPU:** Supports 15th Gen Intel® Core™ Ultra 9/7/5 LGA1851 CPU (up to 65W)
- **BIOS:** AMI EFI 256 Mbit SPI BIOS.
- **System Chipset:** Intel® Q870 / H810
- **Storage Interface:**
 - 2 x on-board SATA connector with a data transmission rate up to 6 GB/s
 - 1 x M.2 M-Key slot (2280), supporting NVMe SSD

1.3.2 Memory

- **RAM:** 2 x 262-pins CSODIMM socket support dual channel DDR5 6400 MT/s CSODIMM, up to 96GB Max.

1.3.3 Input/Output

- **Serial Ports:** 2 serial ports (COM1 RS232, COM2 RS232/422/485).
- **USB Port:** Supports up to 1 x USB Type-C, 4 x USB3.2 Gen2x1 and 2 x USB3.2 Gen1x1
- **GPIO Connector:** 8-bit general purpose Input/Output.

1.3.4 Graphics

- **Controller:** Intel Enhanced Intel® Xe LPG architecture
- **LVDS or eDP:** Supports 1 LVDS up to 1920 x 1080 @60Hz, colay with 1 eDP up to 4096 x 2160 @ 60Hz.

- **DP:** Supports 2 DP (1 via USB Type-C) up to 4096 x 2160 @120Hz.
- **HDMI:** Supports 1 HDMI 2.1 TMDS up to 4096 x 2160 @60Hz.

1.3.5 Ethernet LAN

- Supports dual 10/100/1000/2500 Mbps Ethernet port (s)
- **Controller:**
 - LAN1: Intel I226 2.5 GbE (I226-LM, V-PRO)
 - LAN2: Intel I226 2.5 GbE (I226-V)

1.3.6 Industrial Features

- **Watchdog Timer:** Can generate a system reset. The watchdog timer is programmable, with each unit equal to one second or one minute (255 levels).

1.3.7 Mechanical and Environmental Specifications

- **Operating Temperature:** 0 ~ 60°C (32 ~ 140°F)
- **Storage Temperature:** -40 ~ 85°C (-40 ~ 185°F).
- **Humidity:** 5 ~ 95% non-condensing.
- **Power Supply Voltage:** 12-24V
- **Power Consumption:** Boost 218.96W; Typical 148.98W
(configuration: Intel® Core™ Ultra 9 285, 2pcs 48 GB DDR5 5600 MT/s)
- **Board Size:** 170 x 170 mm (6.69 x 6.69").
- **Board Weight:** 1.0 kg

1.4 Jumpers and Connectors

Connectors on the AIMB-2710 motherboard link it to devices such as hard disk drives and a keyboard. In addition, the board has a number of jumpers used to configure the system for your application.

The tables below list the function of each of the board jumpers and connectors. Later sections in this chapter give instructions on setting jumpers. Chapter 2 gives instructions for connecting external devices to your motherboard.

Table 1.1: I/O Connector

	Description	Part Reference
1	Direct Current input connector	DCIN1
2	Display Port / HDMI connector	DP1+HDMI1
3	TBT4 / USB4 Type C connector	USBC1
4	RJ-45 + USB3.2 stack connector	LAN1_USB12
5	RJ-45 + USB3.2 stack connector	LAN2_USB78
6	HD Audio Interface (Analog)	AUDIO1
7	PCI Express x16 slot	PCIEX16_1
8	M.2 E-Key Connector	M2_E1
9	M.2 M-Key Connector	M2_M1
10	Serial ATA interface Connector	SATA1
11	Serial ATA interface Connector	SATA2
12	DDR5 SO-DIMM Socket A1	DIMMA1
13	DDR5 SO-DIMM Socket B1	DIMMB1

Table 1.2: Box header

	Description	Part Reference
1	ATX supported 3-pin header on board	ATX_5VSB1
2	USB2.0 Front panel Header	USB2_56
3	Universal Serial Bus 3.2	USB3_34
4	CMOS battery Connector	BAT1
5	COM1 Connector	COM1
6	COM2 Connector	COM2
7	EDP / LVDS Backlight Inverter Power Connector	INV1
8	EDP Connector / LVDS Connector	EDP1_LVDS1
9	SATA Power connector	SATA_PWR1

Table 1.3: Pin Header

	Description	Part Reference
1	Audio amplifier output pin header	AMP1
2	Flash Descriptor Security Override Pin Header	JME1
3	Case Open Connector	JCASE1
4	8-bits General Purpose I/O pin header	GPIO1
5	CPU FAN Connector	CPUFAN1
6	System FAN Connector	SYSFAN1
7	IT5782VG Programming Header	JSMBUS1
8	Power LED pin header	JFP2
9	LED port 80 connector	LED_P80
10	VR Programming Header	VR_PMB1
11	SPI BIOS flash socket	SPI1

Table 1.4: Jumper Settings

	Description	Part Reference
1	COMS Mode selection	JCMOS1
2	AT / ATX Mode selection	PSON1
3	COM1 RI# selection pin header	JSETCOM1_V1
4	PWRBTN#/ RESET#/HDD LED/ Serial bus from HW monitor IC	JFP1
5	EDP Panel / LVDS Panel Voltage Selection	JEDP1_LVDS1
6	PCI Express x16 Bifurcation	SW_PEGSEL1

1.5 Board layout: Jumper and Connector Locations

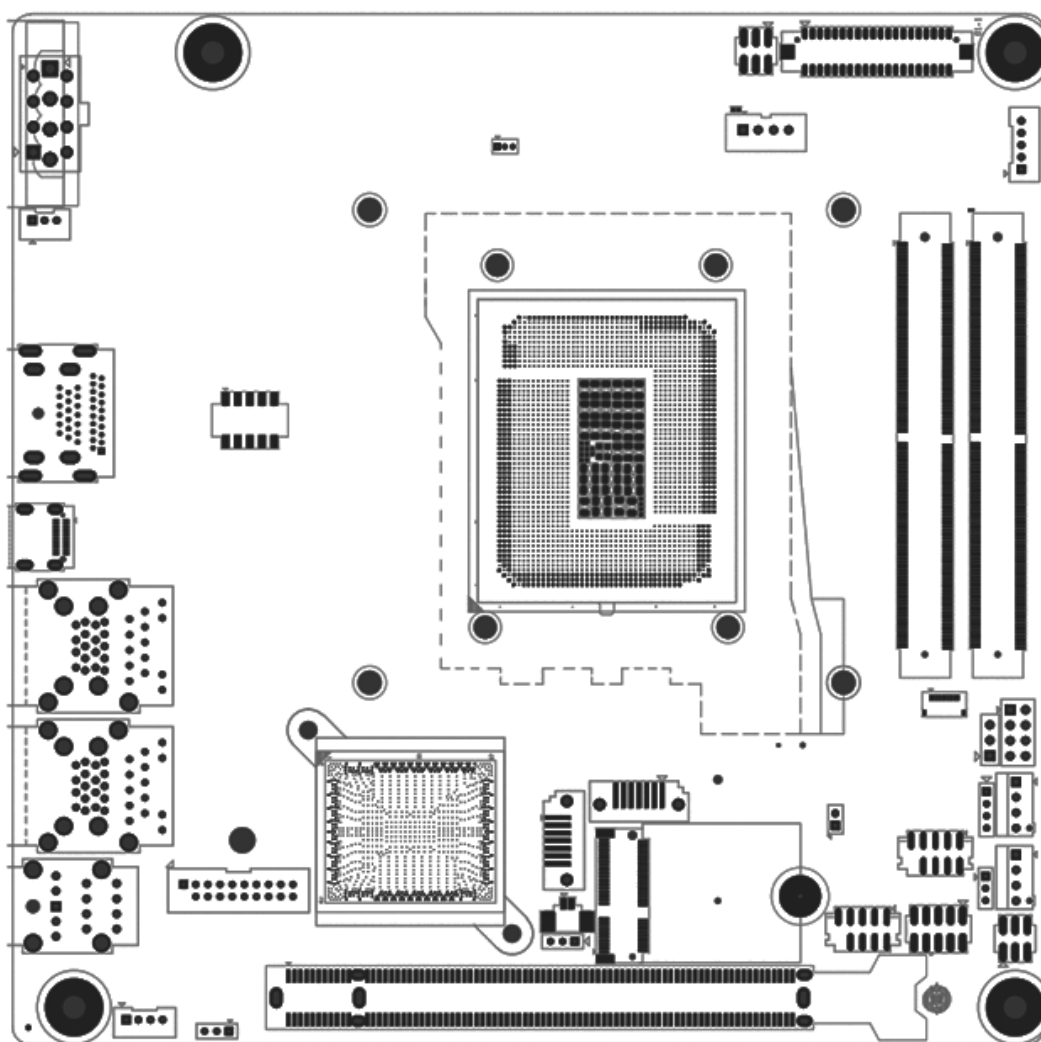


Figure 1.1 Jumper and Connector Location (Top Side)

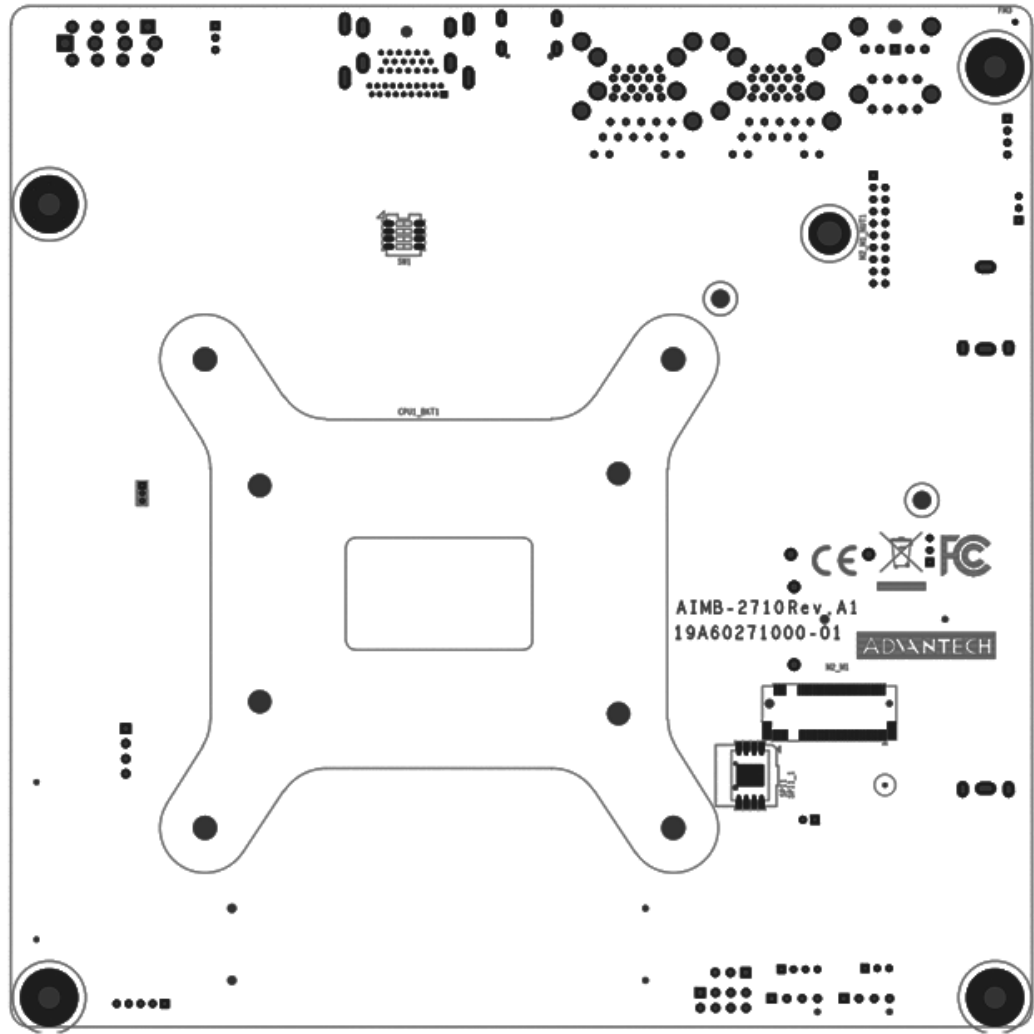


Figure 1.2 Jumper and Connector Location (Bottom Side)

1.6 AIMB-2710 Board Diagram

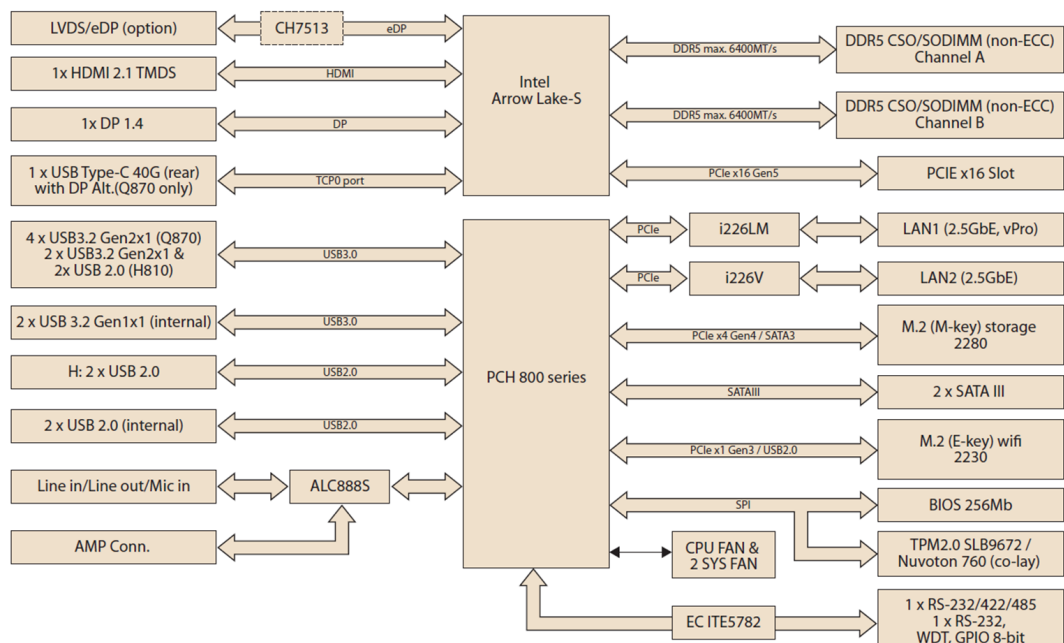


Figure 1.3 AIMB-2710 Block Diagram

1.7 Safety Precautions

Warning! Always completely disconnect the power cord from chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.



Caution! Always ground yourself to remove any static charge before touching the motherboard. Modern electronic devices are very sensitive to electrostatic discharges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis.



Caution! The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by the manufacturer. Discard used batteries according to manufacturer's instructions.



Caution! There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.



1.8 Jumper Settings

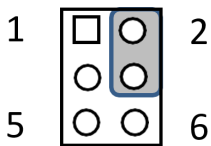
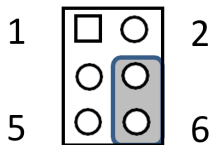
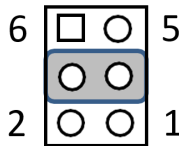
This section provides instructions on how to configure your motherboard by setting the jumpers. It also includes the motherboard's default settings and your options for each jumper.

1.8.1 How to Set Jumpers

Users can configure your motherboard to match the needs of your application by setting the jumpers. A jumper is a metal bridge that closes an electrical circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” (or turn ON) a jumper, you connect the pins with the clip. To “open” (or turn OFF) a jumper, you remove the clip. Sometimes a jumper consists of a set of three pins, labeled 1, 2, and 3. In this case you connect either pins 1 and 2, or 2 and 3. A pair of needle-nose pliers may be useful when setting jumpers.

1.8.2 EDP Panel / LVDS Panel Voltage Selection (JEDP1_LVDS1)

Table 1.5: JEDP1_LVDS1

Function	Jumper Setting
Jumper position for 5V	
Jumper position for 3.3V (Default)	
Jumper position for 12V	

1.8.3 CMOS Clear (JCOMS1)

Table 1.6: JCOMS1

Function	Jumper Setting
Keep CMOS Data (Default)	
Clear CMOS Data	

1.8.4 AT/ATX Mode Selection (PSON1)

Table 1.7: PSON1

Function	Jumper Setting
ATX Mode (Default)	
AT Mode	

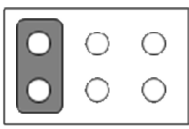
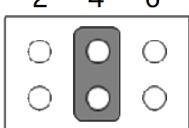
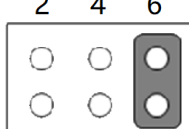
1.8.5 PCI Express x16 Bifurcation (SW_PEGSEL1)

Table 1.8: SW_PEGSEL1

Function	Jumper Setting
1 X16 (Default)	
2 X8	
1 X8 + 2 X4	

1.8.6 COM1_RI# Pin RI# / 5V / 12V Selection (JSETCOM1_V1)

Table 1.9: JSETCOM1_V1

Function	Jumper Setting
Jumper position for RI# (Default)	
Jumper position for +5V	
Jumper position for +12V	

1.8.7 Flash Descriptor Security Override Pin Header (JME1)

Table 1.10: JME1

Function	Jumper Setting		
	1	2	3
Disable Flash Descriptor Security (Default)			
Enable Flash Descriptor Security			

1.9 System Memory

AIMB-2710 has two sockets for a 262-pin DDR5 CSODIMM. These sockets use a 1.2 V unbuffered double data rate synchronous DRAM (DDR SDRAM). DRAM is available in capacities of 8GB, 16GB, 32GB and 48GB. The sockets can take any combination with CSODIMMs of any size, giving a total memory size between 8GB, 16GB, 32GB, 64GB, up to max 96GB. AIMB-2710 does NOT support error checking and correction (ECC).

1.10 Memory Installation Procedures

To install DIMMs, first make sure the two handles of the DIMM socket are in the “open” position, i.e., the handles lean outward. Slowly slide the DIMM module along the plastic guides on both ends of the socket. Then firmly but gently (avoid pushing down too hard) press the DIMM module well down into the socket, until you hear a click when the two handles have automatically locked the memory module into the correct position of the DIMM socket. To remove the memory module, just push both handles outward, and the memory module will be ejected by the mechanism.

Chapter 2

Pin Assignments

2.1 Introduction

You can access most of the connectors from the top of the board as it is being installed in the chassis. If you have a number of cards installed or have a packed chassis, you may need to partially remove the card to make all the connections.

2.2 I/O Connector

2.2.1 Direct Current Input Connector (DCIN1)

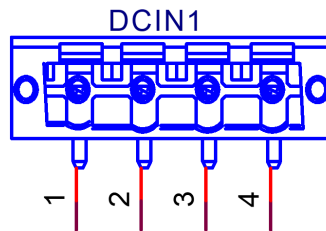


Table 2.1: DCIN1

Pin	Signal
1	GND
2	12V ~ 24V
3	12V ~ 24V
4	GND

2.2.2 DisplayPort / HDMI Connector (DP1 + HDMI1)

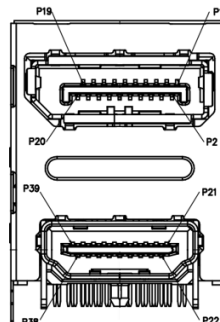


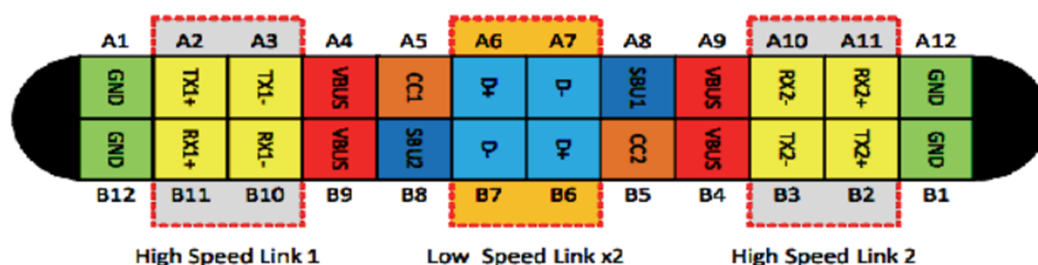
Table 2.2: DP1 + HDMI1

Pin	Signal	Pin	Signal
P1	ML_Lane 0+	P21	TMDS Data2+
P2	GND	P22	GND
P3	ML_Lane 0-	P23	TMDS Data2-
P4	ML_Lane 1+	P24	TMDS Data1+
P5	GND	P25	GND
P6	ML_Lane 1-	P26	TMDS Data1-
P7	ML_Lane 2+	P27	TMDS Data0+
P8	GND	P28	GND
P9	ML_Lane 2-	P29	TMDS Data0-

Table 2.2: DP1 + HDMI1

P10	ML_Lane 3+	P30	TMDS Clock+
P11	GND	P31	GND
P12	ML_Lane 3-	P32	TMDS Clock-
P13	AUX_EN#	P33	NC
P14	GND	P34	NC
P15	AUX+	P35	SCL
P16	GND	P36	SDA
P17	AUX-	P37	GND
P18	HPD	P38	HDMI_PWR
P19	GND	P39	HPD
P20	DP_PWR		

2.2.3 TBT4 / USB4 Type Connector (USBC1)

**Table 2.3: USBC1**

Pin	Signal	Pin	Signal
A1	GND1	B1	GND3
A2	SSTXP1_1	B2	SSTXP2_2
A3	SSTXN1_1	B3	SSTXN2_2
A4	VUSB_1	B4	VUSB_3
A5	CC1	B5	CC2
A6	DP1	B6	DP2
A7	DN1	B7	DN2
A8	SBU1	B8	SBU2
A9	VUSB_2	B9	VUSB_4
A10	SSRXN2_1	B10	SSRXN1_2
A11	SSRXP2_1	B11	SSRXP1_2
A12	GND2	B12	GND4

2.2.4 RJ-45 + USB3.2 Stack Connector (LAN1_USB12)

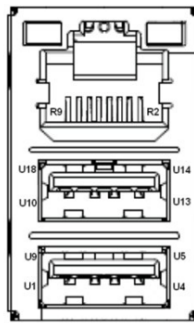


Table 2.4: LAN1_USB12

Pin	Signal	Pin	Signal
U1	VBUS (*)	U10	VBUS (*)
U2	D_1-	U11	D_2-
U3	D_1+	U12	D_2+
U4	GND	U13	GND
U5	RX_1-	U14	RX_2-
U6	RX_1+	U15	RX_2+
U7	GND	U16	GND
U8	TX_1-	U17	TX_2-
U9	TX_1+	U18	TX_2+
R2	MDI_0+	R6	MDI_2+
R3	MDI_0-	R7	MDI_2-
R4	MDI_1+	R8	MDI_3+
R5	MDI_1-	R9	MDI_3-

2.2.5 RJ-45 + USB3.2 Stack Connector (LAN2_USB78)

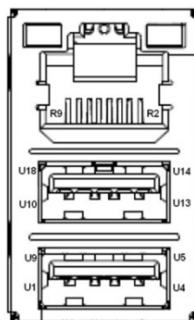


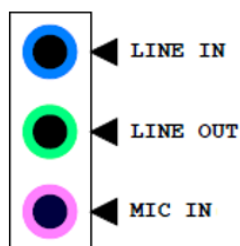
Table 2.5: LAN2_USB78

Pin	Signal	Pin	Signal
U1	VBUS	U10	VBUS
U2	D_7-	U11	D_8-
U3	D_7+	U12	D_8+
U4	GND	U13	GND
U5	RX_7-	U14	RX_8-
U6	RX_7+	U15	RX_8+

Table 2.5: LAN2_USB78

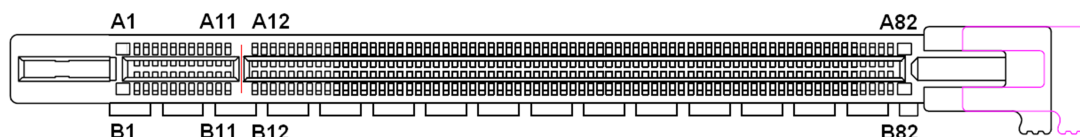
U7	GND	U16	GND
U8	TX_7-	U17	TX_8-
U9	TX_7+	U18	TX_8+
R2	MDI_0+	R6	MDI_2+
R3	MDI_0-	R7	MDI_2-
R4	MDI_1+	R8	MDI_3+
R5	MDI_1-	R9	MDI_3-

2.2.6 HD Audio Interface (Analog) (AUDIO1)

**Table 2.6: AUDIO1**

Pin	Signal
1	MIC IN
2	LINE OUT
3	LINE IN

2.2.7 PCI Express x16 Slot (PCIEX16_1)

**Table 2.7: PCIEX16_1**

Pin	Signal	Pin	Signal
B1	+12V	A1	PRSNT1#
B2	+12V	A2	+12V
B3	+12V	A3	+12V
B4	GND	A4	GND
B5	SMB_CLK	A5	Reserved
B6	SMB_DATA	A6	Reserved
B7	GND	A7	Reserved
B8	+3.3V	A8	Reserved
B9	Reserved	A9	+3.3V
B10	+3.3VAUX	A10	+3.3V
B11	WAKE#	A11	PWRGD
B12	Reserved	A12	GND
B13	GND	A13	REFCLK+

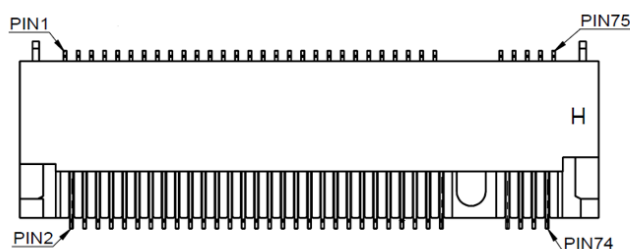
Table 2.7: PCIEX16_1

B14	TX0+	A14	REFCLK-
B15	TX0-	A15	GND
B16	GND	A16	RX0+
B17	Reserved	A17	RX0-
B18	DETECT#	A18	GND
B19	TX1+	A19	Advantech define
B20	TX1-	A20	GND
B21	GND	A21	RX1+
B22	GND	A22	RX1-
B23	TX2+	A23	GND
B24	TX2-	A24	GND
B25	GND	A25	RX2+
B26	GND	A26	RX2-
B27	TX3+	A27	GND
B28	TX3-	A28	GND
B29	GND	A29	RX3+
B30	Reserved	A30	RX3-
B31	Reserved	A31	GND
B32	GND	A32	Advantech define
B33	TX4+	A33	Reserved
B34	TX4-	A34	GND
B35	GND	A35	RX4+
B36	GND	A36	RX4-
B37	TX5+	A37	GND
B38	TX5-	A38	GND
B39	GND	A39	RX5+
B40	GND	A40	RX5-
B41	TX6+	A41	GND
B42	TX6-	A42	GND
B43	GND	A43	RX6+
B44	GND	A44	RX6-
B45	TX7+	A45	GND
B46	TX7-	A46	GND
B47	GND	A47	RX7+
B48	Reserved	A48	RX7-
B49	GND	A49	GND
B50	TX8+	A50	Reserved
B59	TX10-	A59	GND
B60	GND	A60	RX10+
B61	GND	A61	RX10-
B62	TX11+	A62	GND
B63	TX11-	A63	GND
B64	GND	A64	RX11+
B65	GND	A65	RX11-
B66	TX12+	A66	GND
B67	TX12-	A67	GND
B68	GND	A68	RX12+

Table 2.7: PCIE16_1

B69	GND	A69	RX12-
B70	TX13+	A70	GND
B71	TX13-	A71	GND
B72	GND	A72	RX13+
B73	GND	A73	RX13-
B74	TX14+	A74	GND
B75	TX14-	A75	GND
B76	GND	A76	RX14+
B77	GND	A77	RX14-
B78	TX15+	A78	GND
B79	TX15-	A79	GND
B80	GND	A80	RX15+
B81	Reserved	A81	RX15-
B82	Reserved	A82	GND

2.2.8 M.2 E-Key Connector (M2_E1)

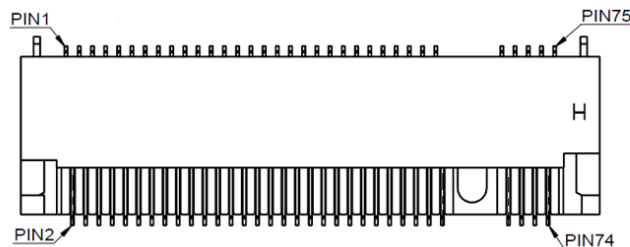
**Table 2.8: M2E1**

Pin	Signal	Pin	Signal
1	GND	2	+3.3V
3	USB_D+	4	+3.3V
5	USB_D-	6	WLAN_LED1#
7	GND	8	BT_PCMCLK
11	CNV_WR_D1+	12	BT_PCMIN
13	GND	14	BT_PCMOUT
15	CNV_WR_D0-	16	BT_LED#
17	CNV_WR_D0+	18	GND
19	GND	20	UART WAKE#
21	CNV_WR_CLK-	22	CNV_BRI_RSP
23	CNV_WR_CLK+	24	Connector Key
25	Connector Key	26	Connector Key
27	Connector Key	28	Connector Key
29	Connector Key	30	Connector Key
31	Connector Key	32	CNV_RGI_DT_R
33	GND	34	CNV_RGI_RSP
35	PETp0	36	CNV_BRI_DT_R
37	PETn0	38	CL_RST#
39	GND	40	CL_DAT
41	PERp0	42	CL_CLK

Table 2.8: M2E1

43	PERn0	44	CNV_GNSS_PA_BLANKING
45	GND	46	CNV_MFUART2_TXD
47	REFCLKp0	48	CNV_MFUART2_RXD
49	REFCLKn0	50	SUSCLK
51	GND	52	WLAN_RST#
53	CLKREQ0#	54	BT_RF_KILL#
55	PEWAKE0#	56	WIFI_RF_KILL#
57	GND	58	NC
59	CNV_WT_D1-	60	NC
47	REFCLKp0	48	CNV_MFUART2_RXD
49	REFCLKn0	50	SUSCLK
51	GND	52	WLAN_RST#
53	CLKREQ0#	54	BT_RF_KILL#
55	PEWAKE0#	56	WIFI_RF_KILL#
57	GND	58	NC
59	CNV_WT_D1-	60	NC
67	CNV_WT_D0+	68	NC
69	GND	70	NC
71	CNV_WT_CLK-	72	+3.3V
73	CNV_WT_CLK+	74	+3.3V
75	GND		

2.2.9 M.2 M-Key Connector (M2_M1)

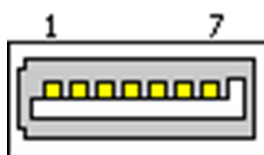
**Table 2.9: M2M1**

Pin	Signal	Pin	Signal
1	GND	2	3.3V
3	GND	4	3.3V
5	PERn3	6	N/C
7	PERp3	8	N/C
9	GND	10	DAS/DSS# (I/O)/LED1# (I)(O/3.3V)
11	PETn3	12	3.3V
13	PETp3	14	3.3V
15	GND	16	3.3V
17	PERn2	18	3.3V
19	PERp2	20	N/C
21	GND	22	N/C
23	PETn2	24	N/C

Table 2.9: M2M1

25	PETp2	26	N/C
27	GND	28	N/C
29	PERn1	30	N/C
31	PERp1	32	N/C
33	GND	34	N/C
35	PETn1	36	N/C
37	PETp1	38	DEVSLP (O)
39	GND	40	N/C
41	PERn0/SATA-B+	42	N/C
43	PERp0/SATA-B-	44	N/C
45	GND	46	N/C
47	PETn0/SATA-A-	48	N/C
49	PETp0/SATA-A+	50	PERST# (O)(0/3.3V) or N/C
51	GND	52	CLKREQ# (I/O)(0/3.3V) or N/C
53	REFCLKn	54	PEWAKE# (I/O)(0/3.3V) or N/C
55	REFCLKp	56	N/C
57	GND	58	N/C
59	Connector Key	60	Connector Key
61	Connector Key	62	Connector Key
63	Connector Key	64	Connector Key
65	Connector Key	66	Connector Key
67	N/C	68	SUSCLK(32kHz) (O)(0/3.3V)
69	PEDET (NC-PCIe/GND-SATA)	70	3.3V
71	GND	72	3.3V
73	GND	74	3.3V
75	GND		

2.2.10 Serial ATA Interface Connector (SATA1)

**Table 2.10: SATA1**

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

2.2.11 Serial ATA Interface Connector (SATA2)

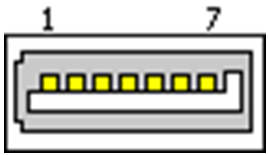


Table 2.11: SATA2

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

2.2.12 DDR5 SO-DIMM Socket A1 (DIMMA1)

Please refer to JEDEC STANDARD.

2.2.13 DDR5 SO-DIMM Socket B1 (DIMMB1)

Please refer to JEDEC STANDARD.

2.3 Box Header

2.3.1 ATX Supported 3-Pin Header on Board (ATX_5VSB1)

ATX_5VSB1

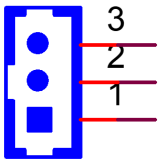


Table 2.12: ATX_5VSB1

Pin	Signal
1	+V5_A_ATX
2	GND
3	SPS_PS_ON#

2.3.2 USB2.0 Front Panel Header (USB2_56)

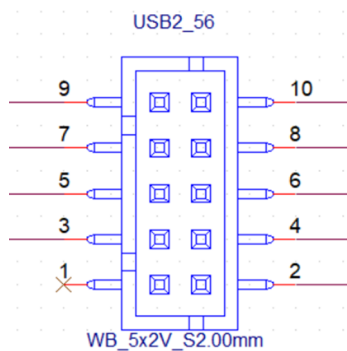


Table 2.13: USB2_56

Pin	Signal	Pin	Signal
1	N.C	2	N.C
3	GND	4	GND
5	D5+	6	D6+
7	D5-	8	D6-
9	VBUS	10	VBUS

2.3.3 Universal Serial Bus 3.2 (USB3_34)

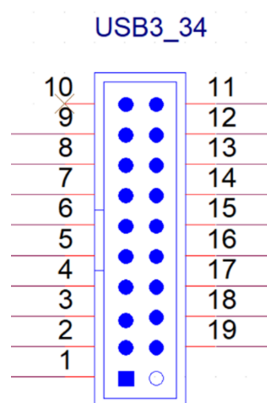


Table 2.14: USB3_34

Pin	Signal	Pin	Signal
1	VBUS	11	D4+
2	RX3-	12	D4-
3	RX3+	13	GND
4	GND	14	TX4+
5	TX3-	15	TX4-
6	TX3+	16	GND
7	GND	17	RX4+
8	D3-	18	RX4-
9	D3+	19	VBUS
10	NC		

2.3.4 CMOS Battery Connector (BAT1)

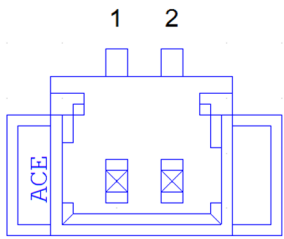


Table 2.15: BAT1

Pin	Signal
1	+VBAT
2	GND

2.3.5 COM1 Connector (COM1)

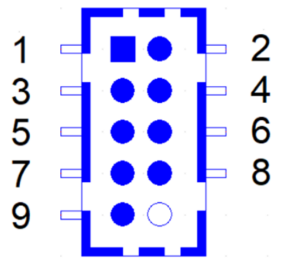


Table 2.16: COM1

Pin	Signal	Pin	Signal
1	COM1_DCD#	2	COM1_SIN
3	COM1_SOUT	4	COM1_DTR#
5	GND	6	COM1_DSR#
7	COM1_RTS#	8	COM1_CTS#
9	COM1_RI_V#		

2.3.6 COM2 Connector (COM2)

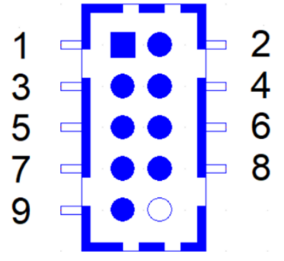


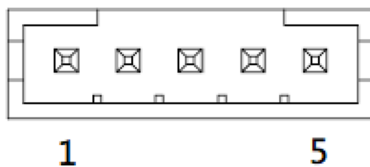
Table 2.17: COM2

Pin	Signal	Pin	Signal
1	COM2_422_485_TX-	2	COM2_422_485_TX+
3	COM2_422_RX+	4	COM2_422_RX-
5	GND	6	COM2_DSR#

Table 2.17: COM2

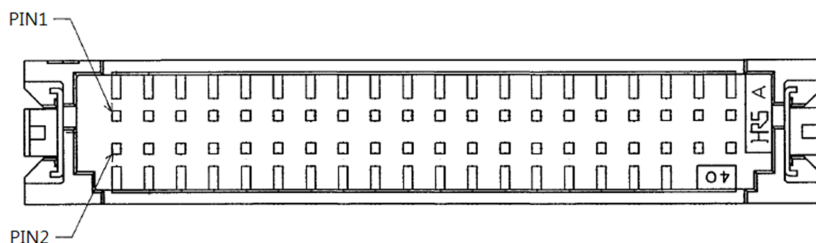
7	COM2_RTS#	8	COM2_CTS#
9	COM2_RI#		

2.3.7 EDP / LVDS Backlight Inverter Power Connector (INV1)

**Table 2.18: INV1**

Pin	Signal
1	+12V
2	GND
3	BKL EN
4	BKL CTRL
5	+5V

2.3.8 EDP Connector / LVDS Connector (EDP1_LVDS1)

**Table 2.19: LVDS1:**

Pin	Signal	Pin	Signal
1	VDD	2	VDD
3	LVDS_DETECT#	4	GND
5	VDD	6	VDD
7	LVDS_OD0-	8	LVDS_ED0-
9	LVDS_OD0+	10	LVDS_ED0+
11	GND	12	GND
13	LVDS_OD1-	14	LVDS_ED1-
15	LVDS_OD1+	16	LVDS_ED1+
17	GND	18	GND
19	LVDS_OD2-	20	LVDS_ED2-
21	LVDS_OD2+	22	LVDS_ED2+
23	GND	24	GND
25	LVDS_OCK-	26	LVDS_ECK-
27	LVDS_OCK+	28	LVDS_ECK+
29	GND	30	GND

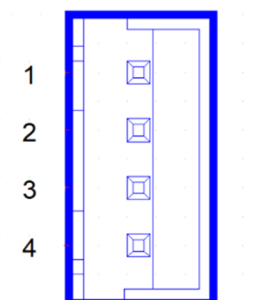
Table 2.19: LVDS1:

31	N.C	32	N.C
33	GND	34	GND
35	LVDS_OD3-	36	LVDS_ED3-
37	LVDS_OD3+	38	LVDS_ED3+
39	LVDS ENBKL	40	LVDS VCON

Table 2.20: EDP1

Pin	Signal	Pin	Signal
1	VDD	2	VDD
3	LVDS DETECT#	4	GND
5	VDD	6	VDD
7	EDP_TX2-	8	N.C
9	EDP_TX2+	10	N.C
11	GND	12	GND
13	EDP_TX1-	14	N.C
15	EDP_TX1+	16	N.C
17	GND	18	GND
19	EDP_TX0-	20	N.C
21	EDP_TX0+	22	N.C
23	GND	24	GND
25	EDP_TX3-	26	N.C
27	EDP_TX3+	28	N.C
29	GND	30	GND
31	EDP_AUX+	32	EDP_AUX-
33	GND	34	EDP_HPD
35	N.C	36	N.C
37	N.C	38	N.C
39	N.C	40	GND

2.3.9 SATA Power Connector (SATA_PWR1)

**Table 2.21: SATA_PWR1**

Pin	Signal
1	+V5
2	GND
3	GND
4	+V12

2.4 Pin Header

2.4.1 Audio Amplifier Output Pin Header (AMP1)

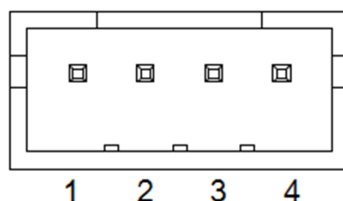


Table 2.22: AMP1

Pin	Signal
1	AMP OUT - R+
2	AMP OUT - R-
3	AMP OUT - L-
4	AMP OUT - L+

2.4.2 Flash Descriptor Security Override Pin Header (JME1)

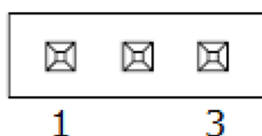


Table 2.23: JME1

Pin	Signal
1	Advantech Define
2	Advantech Define
3	NC

2.4.3 Case Open Connector (JCASE1)

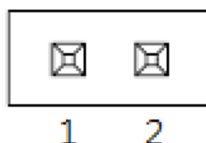


Table 2.24: JCASE1

Pin	Signal
1	Case Open
2	GND

2.4.4 8-bits General Purpose I/O Pin header (GPIO1)

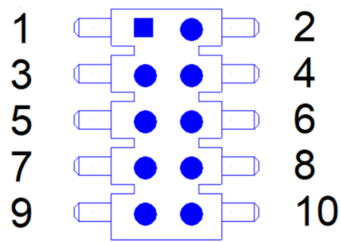


Table 2.25: GPIO1

Pin	Signal	Pin	Signal
1	GPIO0	2	GPIO4
3	GPIO1	4	GPIO5
5	GPIO2	6	GPIO6
7	GPIO3	8	GPIO7
9	VCC_GPIO	10	GND

2.4.5 CPU FAN Connector (CPUFAN1)



Table 2.26: CPUFAN1

Pin	Signal
1	GND
2	CPU FAN VCC
3	CPU FAN SPEED
4	CPU FAN PWM

2.4.6 System FAN Connector (SYSFAN1)



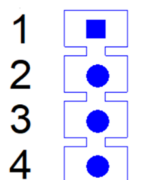
Table 2.27: SYSFAN1

Pin	Signal
1	GND
2	SYSTEM FAN VCC

Table 2.27: SYSFAN1

3	SYSTEM FAN SPEED
4	SYSTEM FAN PWM

2.4.7 IT5782VG Programming Header (JSMBUS1)

**Table 2.28: JSMBUS1**

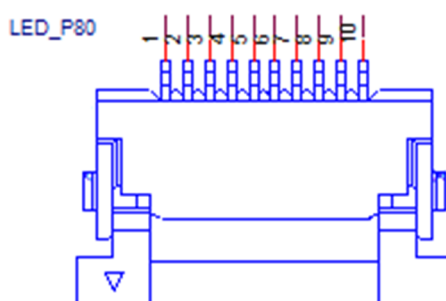
Pin	Signal
1	+V3.3_A_SIO
2	SMB_CLK_EC
3	SMB_DAT_EC
4	GND

2.4.8 Power LED Pin Header (JFP2)

**Table 2.29: JFP2**

Pin	Signal
1	Power LED+
2	NC
3	Power LED-

2.4.9 LED Port 80 Connector (LED_P80)

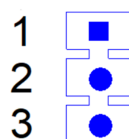
**Table 2.30: LED_P80**

Pin	Signal
1	GND
2	LED_A

Table 2.30: LED_P80

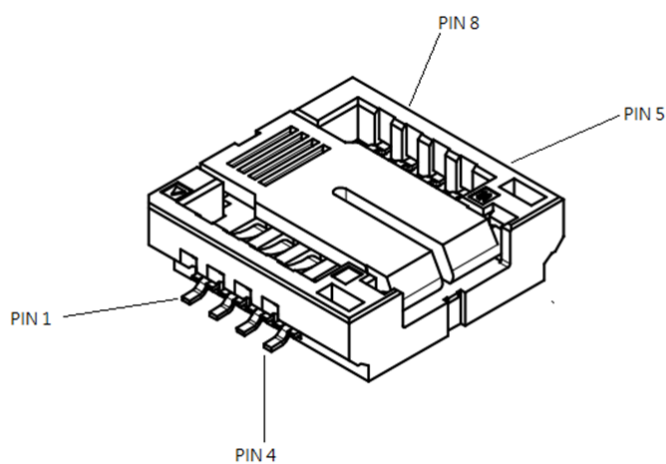
3	LED_B
4	LED_C
5	LED_D
6	LED_E
7	LED_F
8	LED_G
9	DGH0#
10	DGL0#

2.4.10 VR Programming Header (VR_PMB1)

**Table 2.31: VR_PMB1**

Pin	Signal
1	VR_+VCORE_SCLK
2	GND
3	VR_+VCORE_SDATA

2.4.11 SPI BIOS Flash Socket (SPI1)

**Table 2.32: SPI1**

Pin	Signal	Pin	Signal
1	CS#	5	MOSI
2	MISO	6	SCLK
3	WP# / IO2	7	HOLD# / IO3
4	GND	8	+V3.3_SPI

2.5 Jumper Setting

2.5.1 COMS Mode Selection (JCMOS1)



Table 2.33: JCMOS1

Pin	Signal
1	NC
2	RTC_RESET#
3	GND

2.5.2 AT / ATX Mode Selection (PSON1)

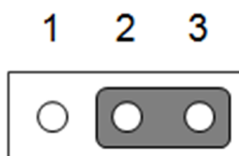


Table 2.34: PSON1

Pin	Signal
1	AT
2	+3.3V
3	ATX

2.5.3 COM1 RI# Selection Pin Header (JSETCOM1_V1)

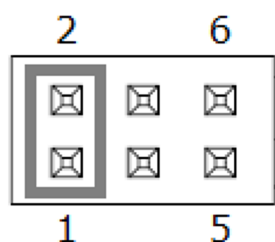


Table 2.35: JSETCOM1_V1

Pin	Signal	Pin	Signal
1	RI# [1]	2	Advantech define
3	Advantech define	4	+5V
5	+12V	6	Advantech define

2.5.4 PWRBTN#/ RESET#/HDD LED/ Serial Bus From HW Monitor IC (JFP1)

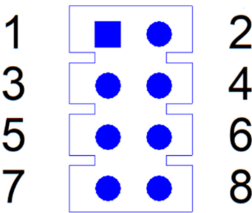


Table 2.36: JFP1			
Pin	Signal	Pin	Signal
1	HDD_LED+	2	PWRBTN#
3	HDD_LED-	4	GND
5	SMB_DAT	6	SYS_RESET#
7	SMB_CLK	8	GND

2.5.5 EDP Panel / LVDS Panel Voltage Selection (JEDP1_LVDS1)

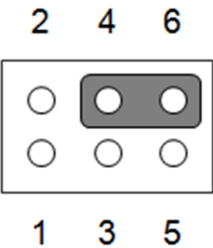


Table 2.37: JEDP1_LVDS1			
Pin	Signal	Pin	Signal
1	NC	2	+5V
3	+12V	4	VDD
5	NC	6	+3.3V

2.5.6 PCI Express x16 Bifurcation (SW_PEGSEL1)

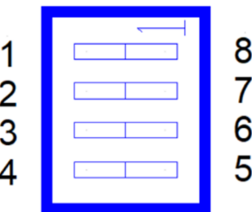


Table 2.38: SW_PEGSEL1	
Pin	Signal
1	PEG0CFGSEL [1]
2	PEG0CFGSEL [0]
3	Advantech define
4	NC

Chapter 3

BIOS Operation

3.1 Introduction

With the AMI BIOS Setup program, you can modify BIOS settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning special features on or off. This chapter describes the basic navigation of the AIMB-292 setup screens.

3.2 BIOS Setup

The AIMB-2710 Series system has AMI BIOS built in, with a CMOS SETUP utility that allows users to configure required settings or to activate certain system features. The CMOS SETUP saves the configuration in the CMOS RAM of the motherboard. When the power is turned off, the battery on the board supplies the necessary power to preserve the CMOS RAM.

When the power is turned on, press the button during the BIOS POST (Power-On Self-Test) to access the CMOS SETUP screen.

Control Keys	
< ↑ >< ↓ >< ← >< → >	Move to select item
<Enter>	Select Item
<Esc>	Main Menu - Quit and not save changes into CMOS Sub Menu - Exit current page and return to Main Menu
<Page Up/+>	Increase the numeric value or make changes
<Page Down/->	Decrease the numeric value or make changes
<F1>	General help, for Setup Sub Menu
<F2>	Item Help
<F5>	Load Previous Values
<F7>	Load Setup Defaults
<F10>	Save all CMOS changes

3.2.1 Main Menu

Press to enter the AMI BIOS CMOS Setup Utility. The Main Menu will appear on the screen. Use the arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.



The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the legend. Above the legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

■ System time / System date

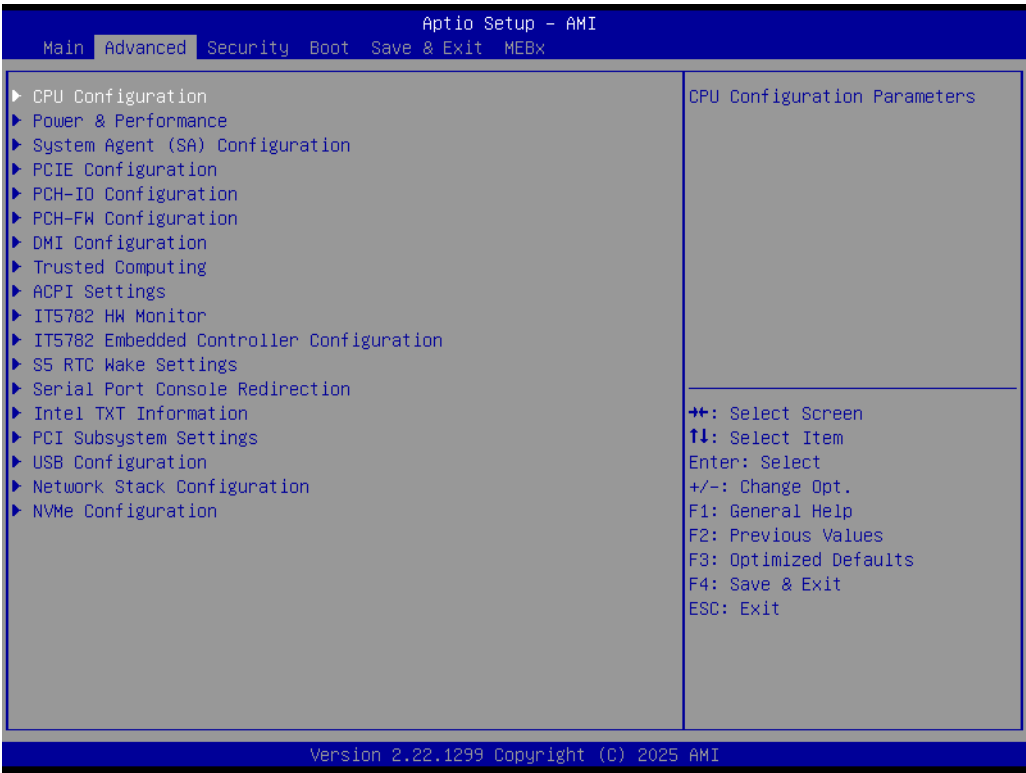
Use this option to change the system time and date. Highlight the System Time or System Date using the keys. Enter new values via the keyboard. Press the or keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

3.2.2 Advanced BIOS Features

Select the Advanced tab from the AIMB-2710 setup menu to enter the Advanced BIOS setup page. Users can select any item in the left frame of the screen, such as CPU configuration. Select an Advanced BIOS setup option by highlighting the text using the keys. All Advanced BIOS setup options are described in this section. The Advanced BIOS setup menu screen is shown below. The sub-menus are described in the following pages.

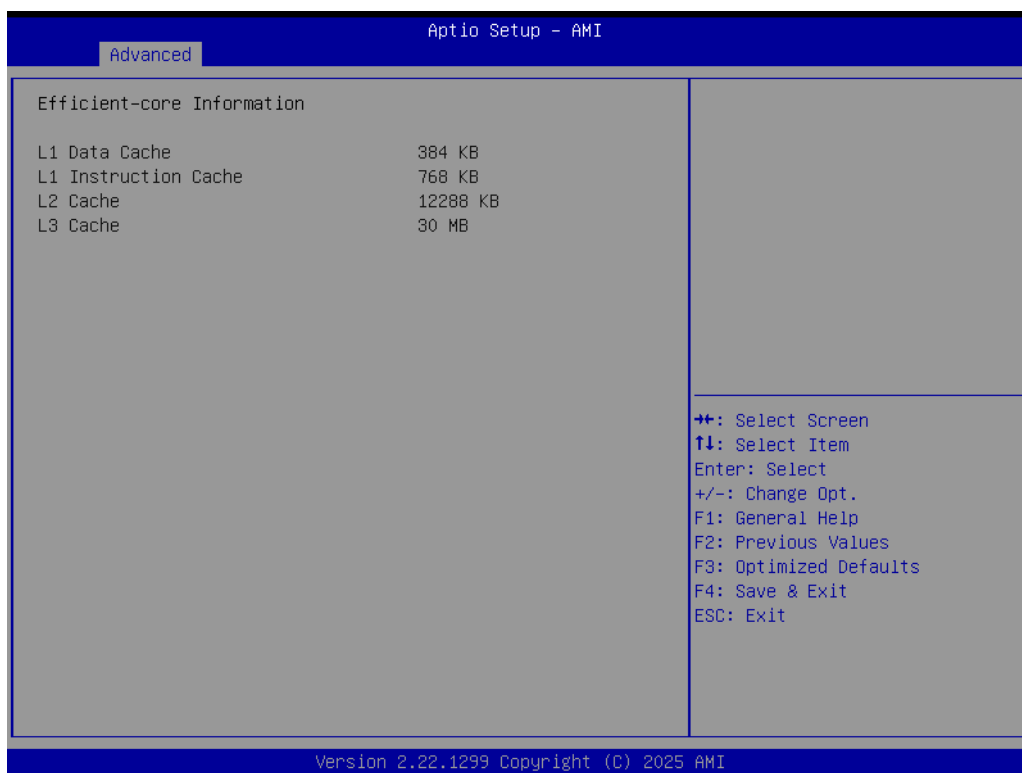
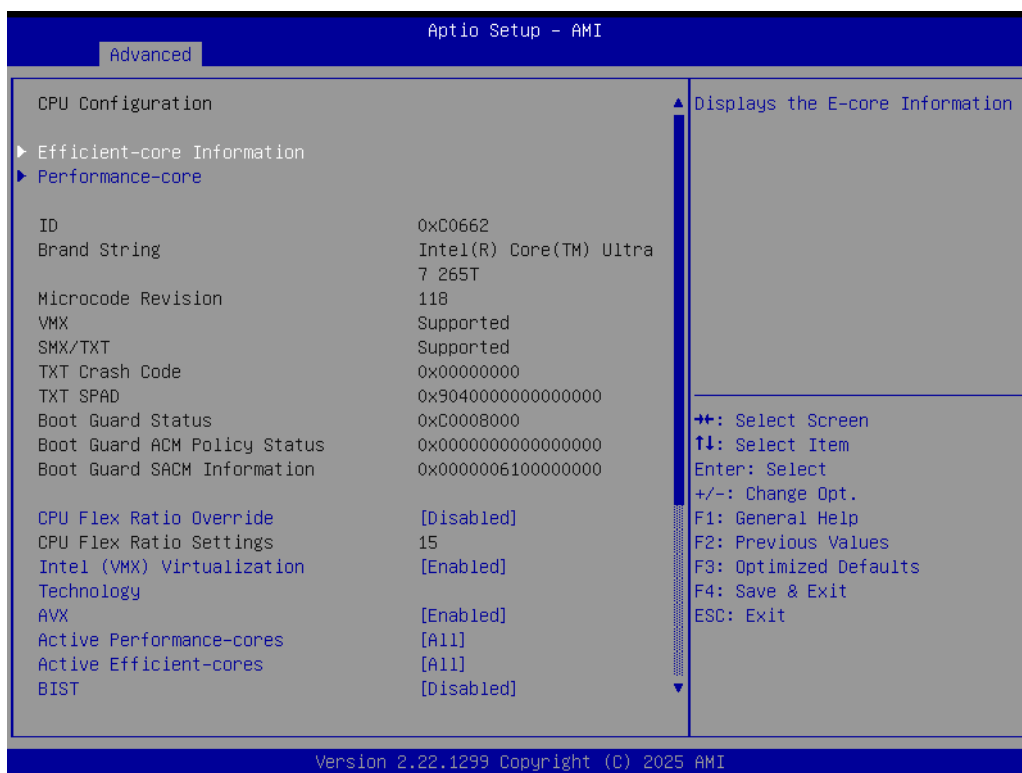
3.2.2.1 CPU Configuration

Advanced → CPU Configuration



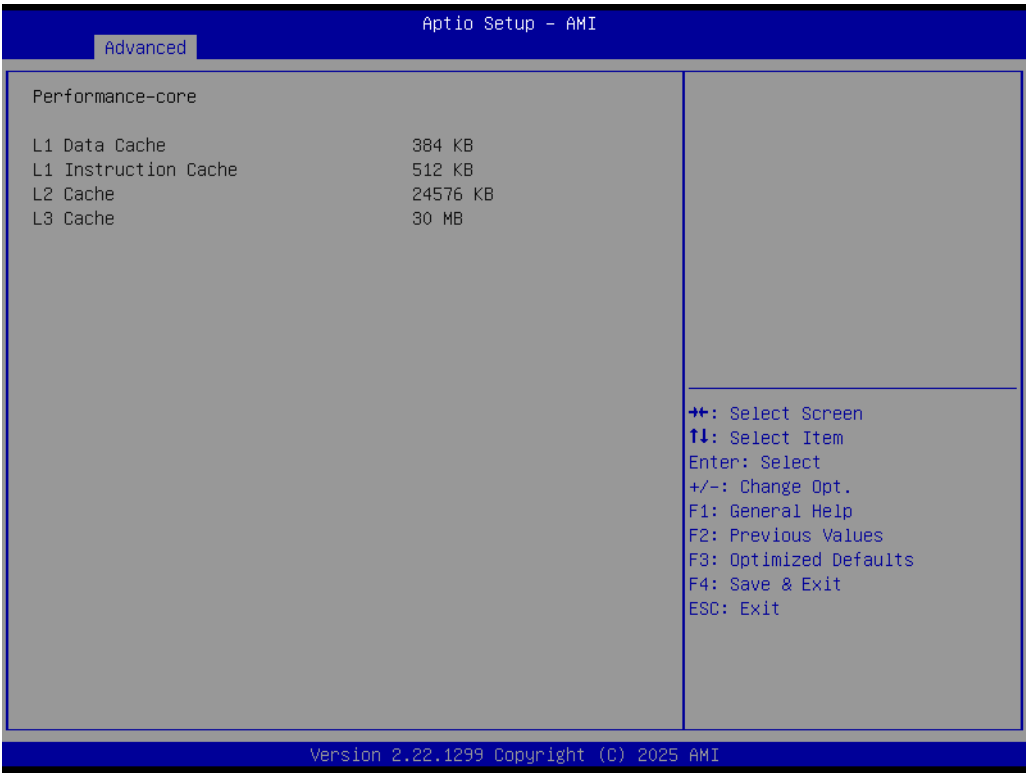
Efficient-core Information

Advanced → CPU Configuration → Efficient-core Information



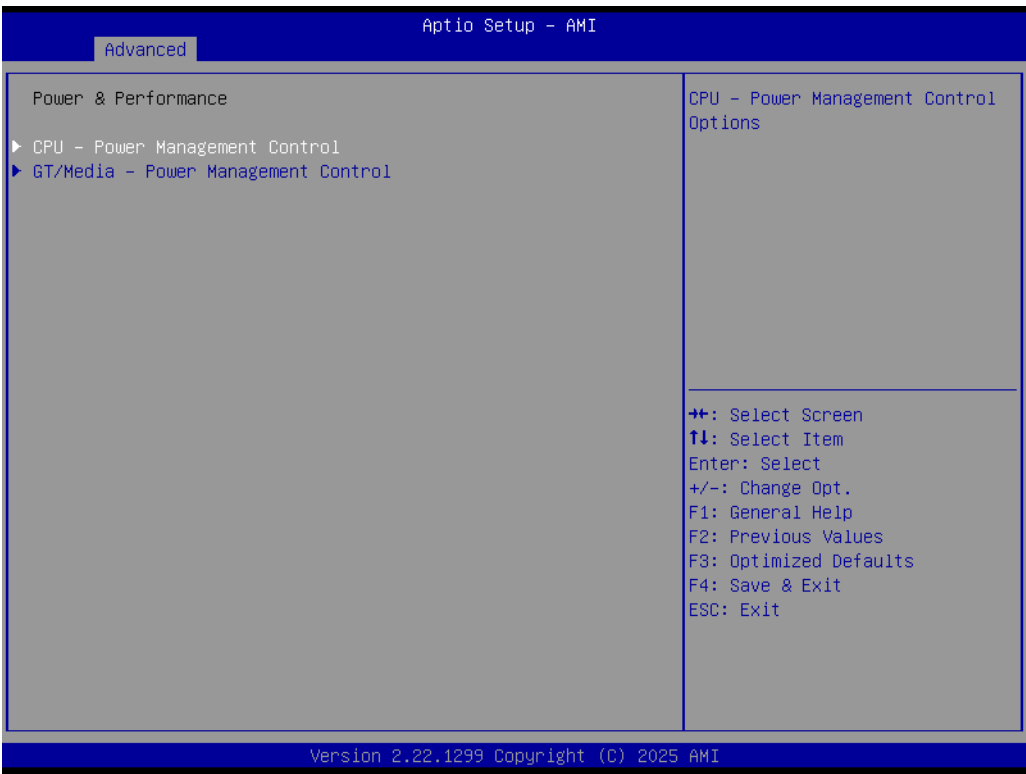
Performance-core Information

Advanced → CPU Configuration → Performance-core Information



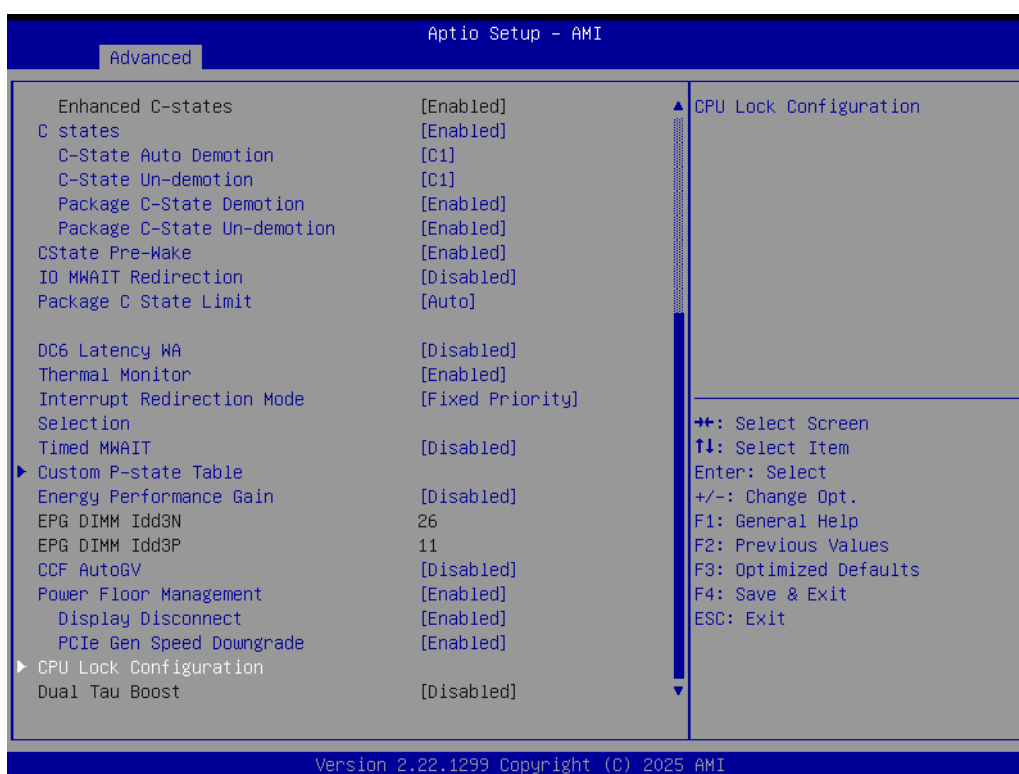
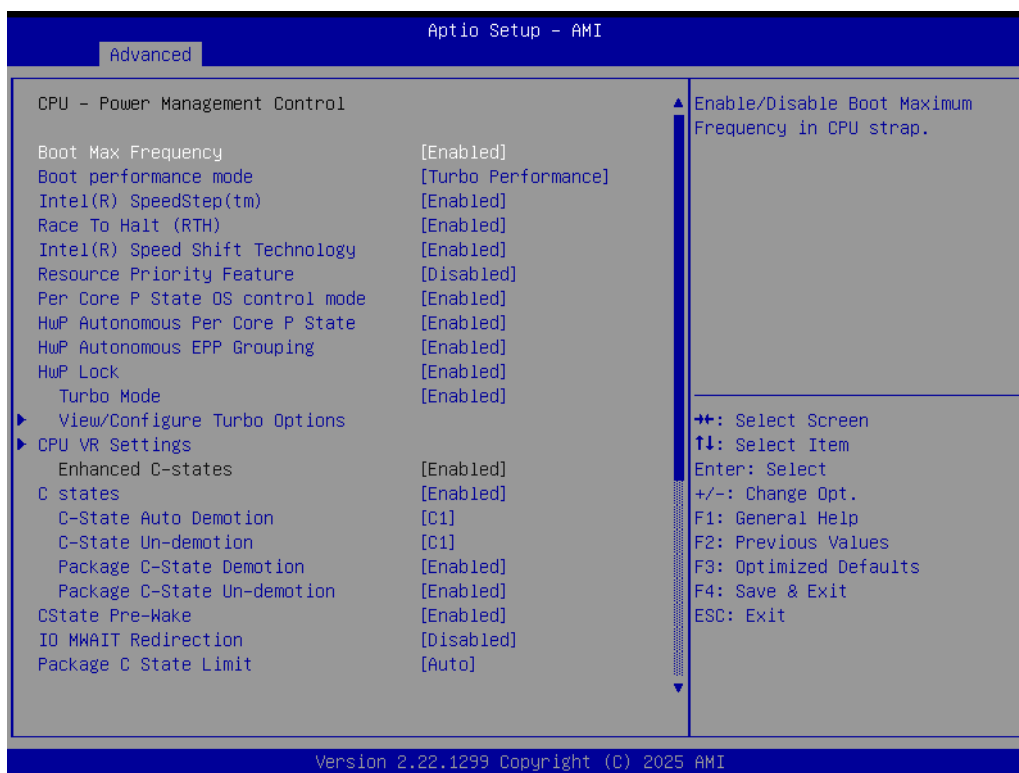
3.2.2.2 Power & Performance

Advanced → Power & Performance



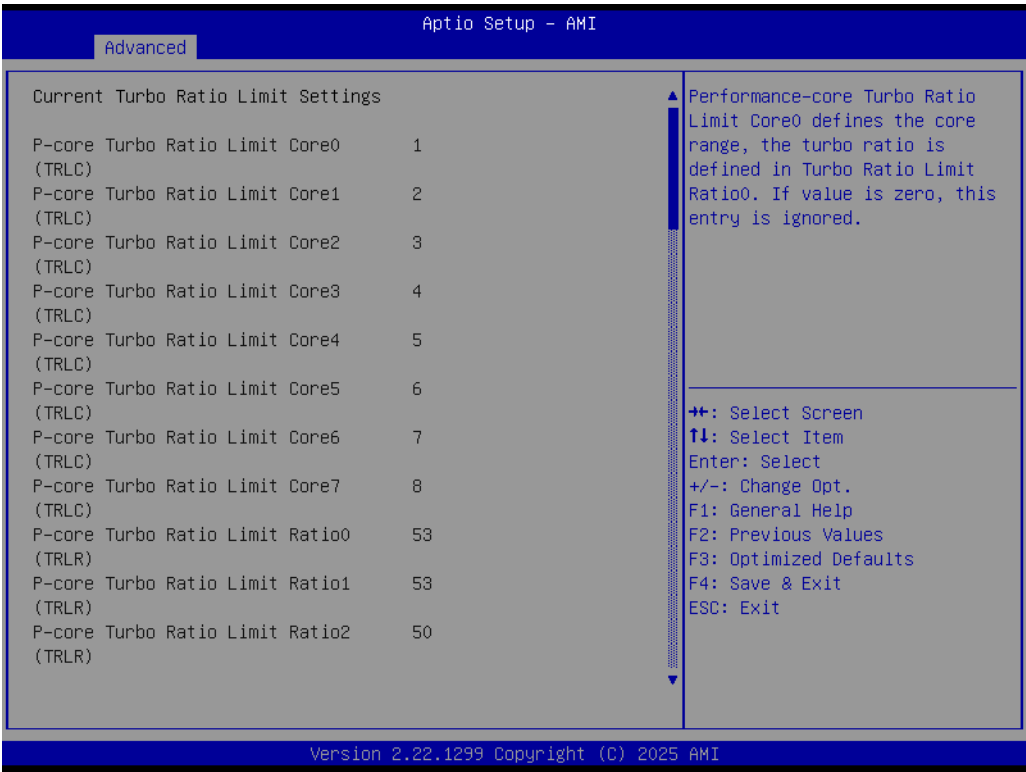
CPU – Power Management Control

Advanced → Power & Performance → CPU – Power Management Control



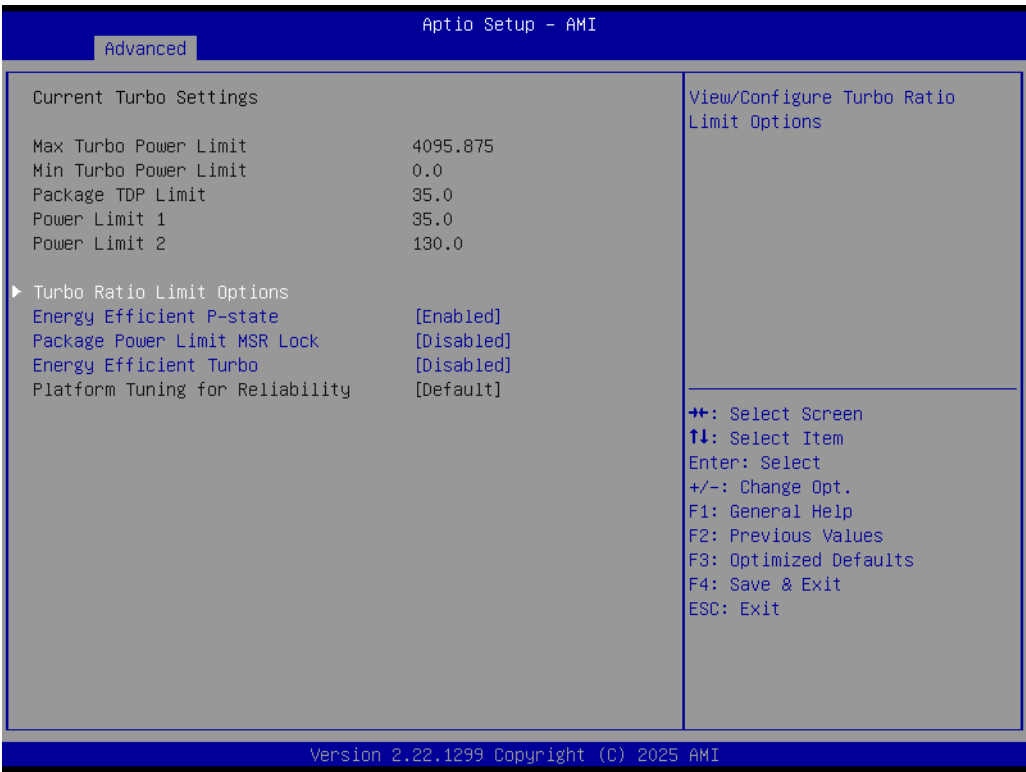
Current Turbo Settings

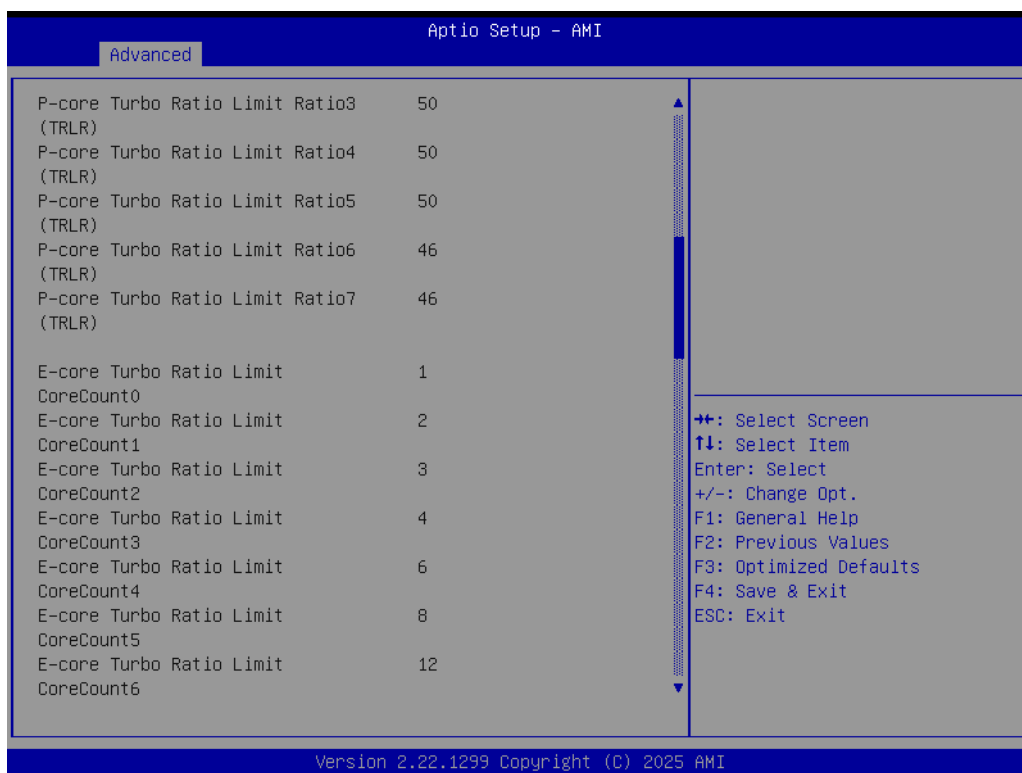
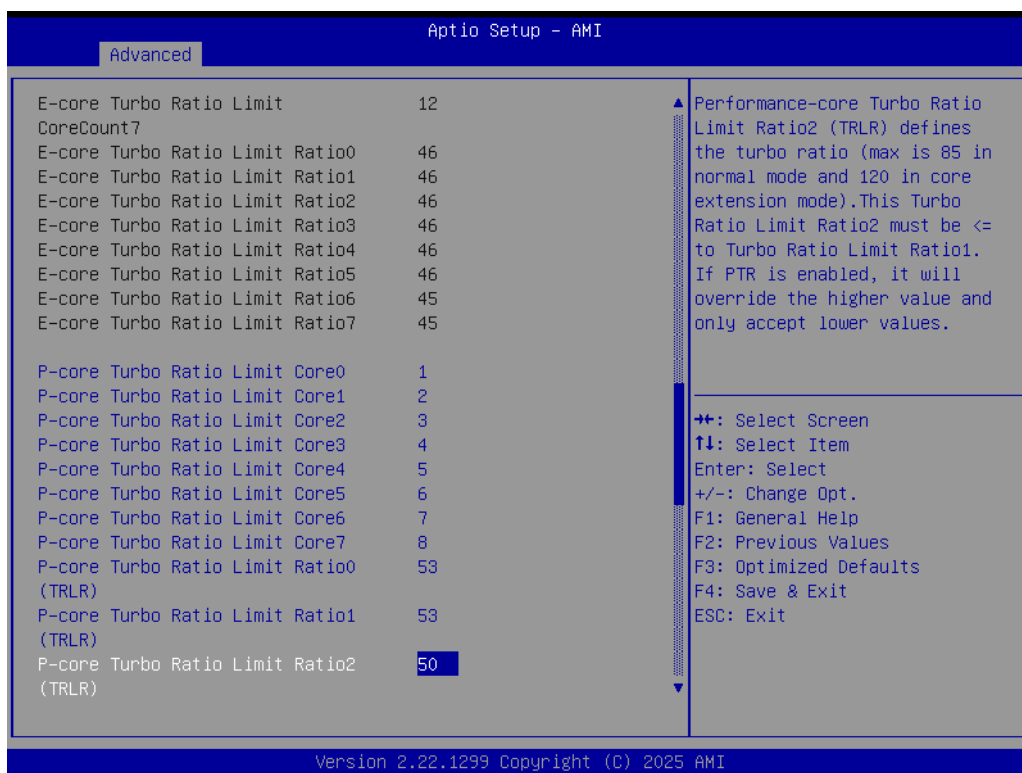
Advanced → Power & Performance → CPU – Power Management Control → View/Configure Turbo Ratio

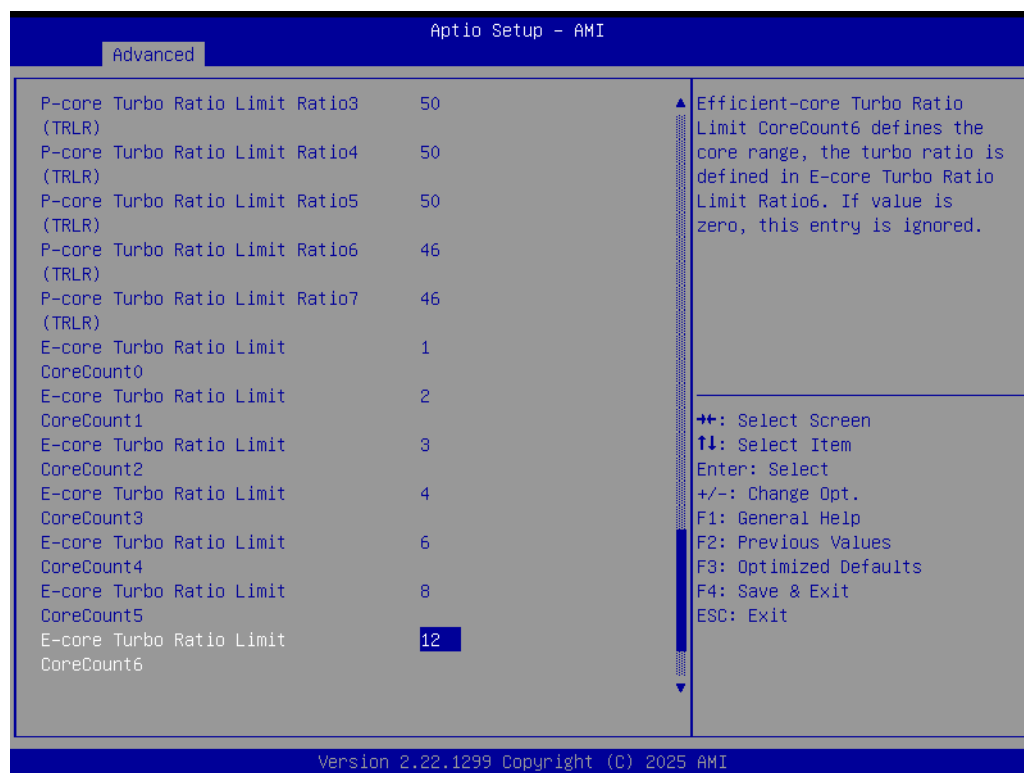


Turbo Ratio Limit Options

Advanced → Power & Performance → CPU – Power Management Control → View/Configure Turbo Ratio → Turbo Ratio Limit Options

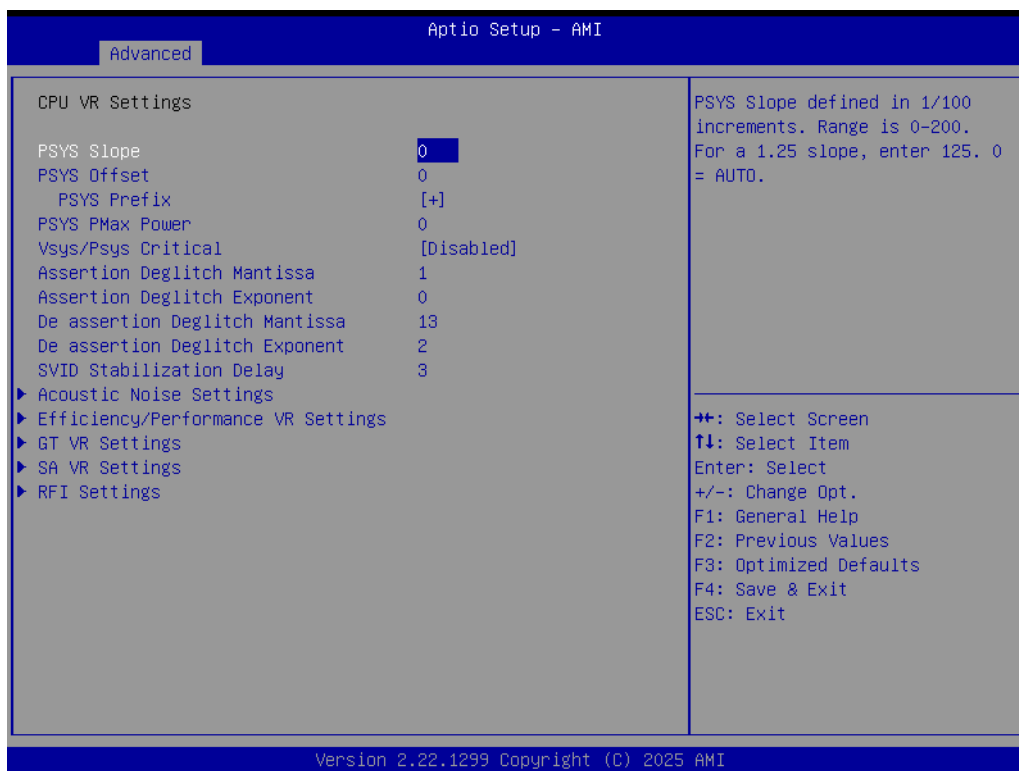






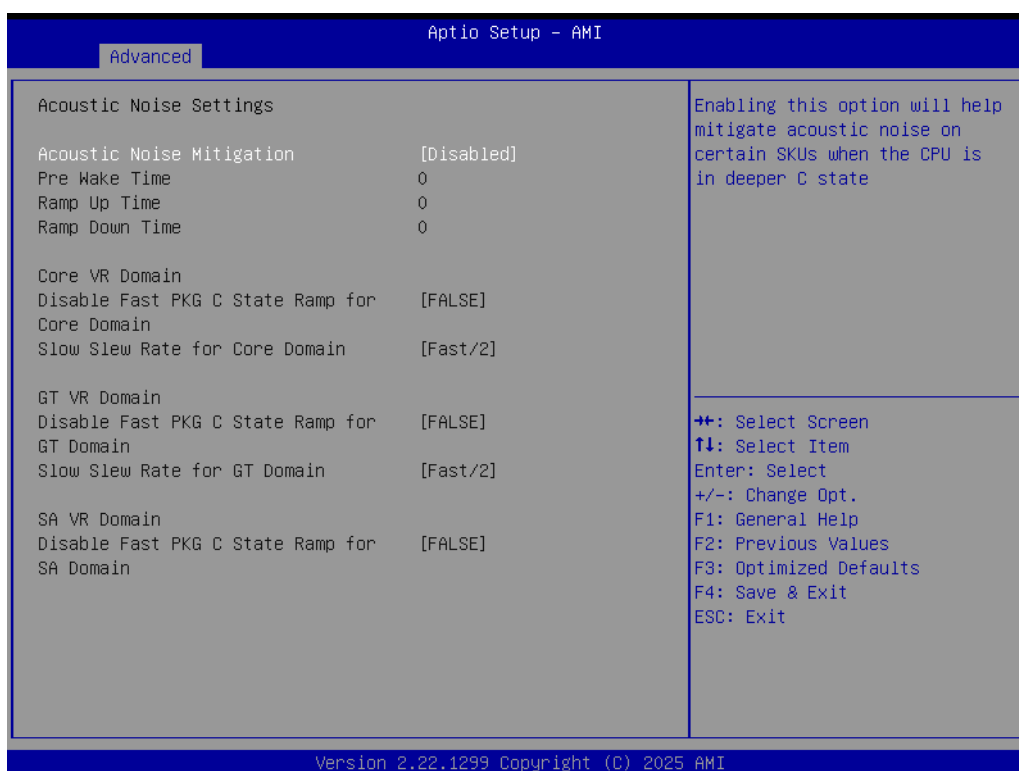
CPU VR Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings



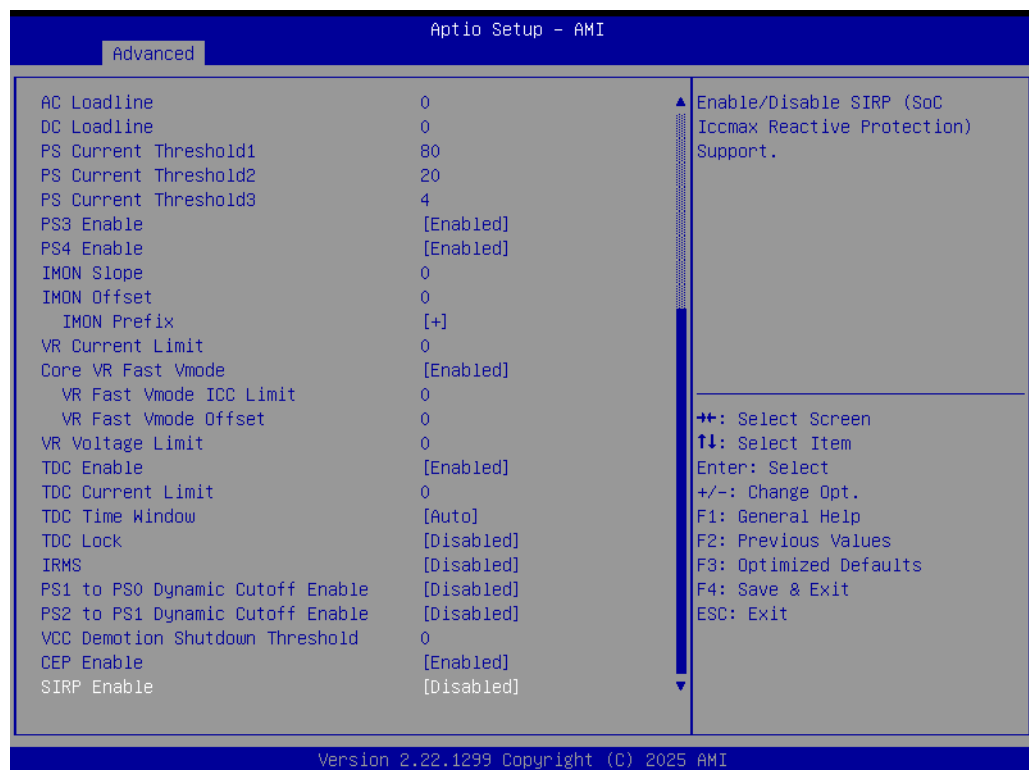
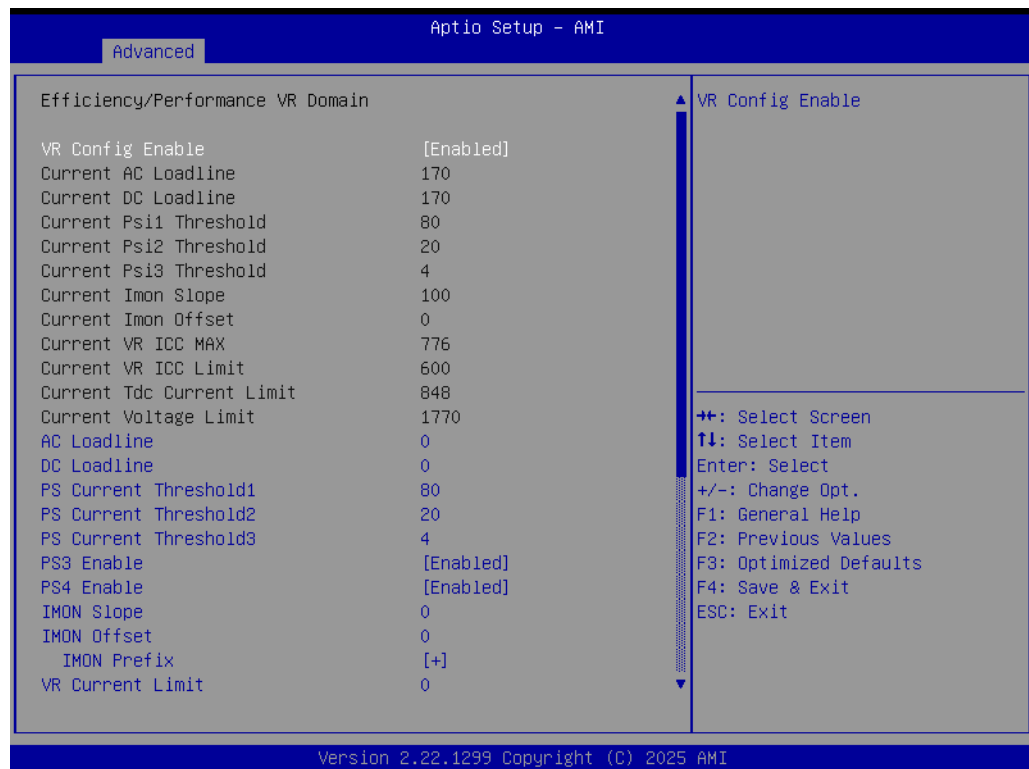
Acoustic Noise Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → Acoustic Noise Settings



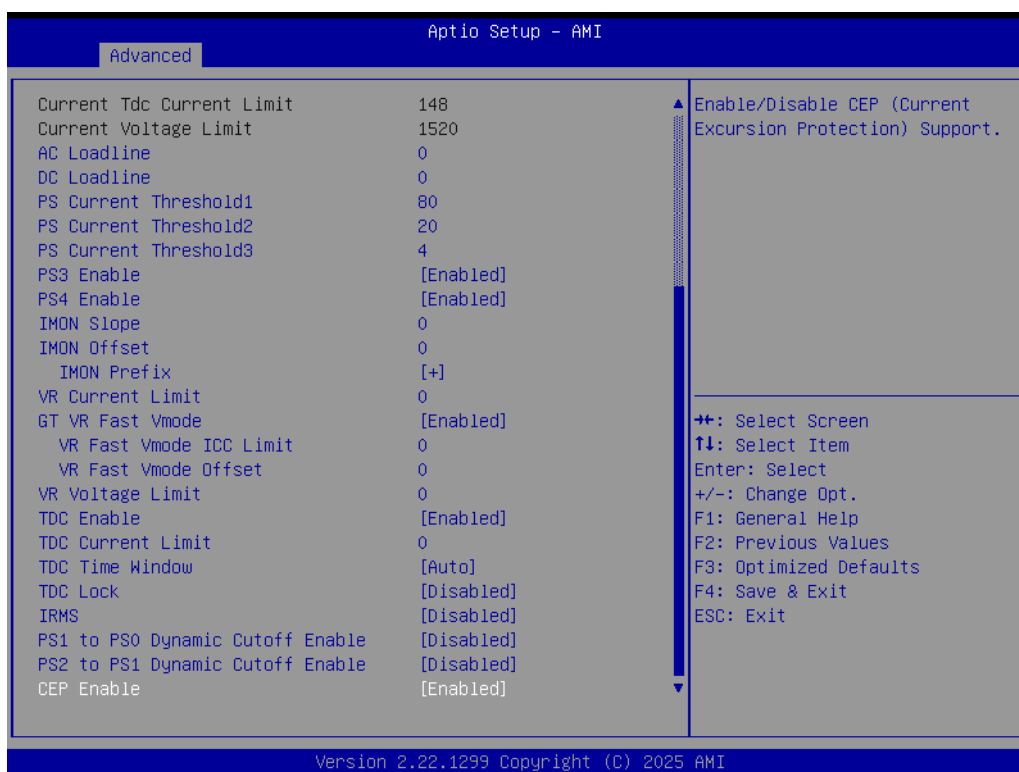
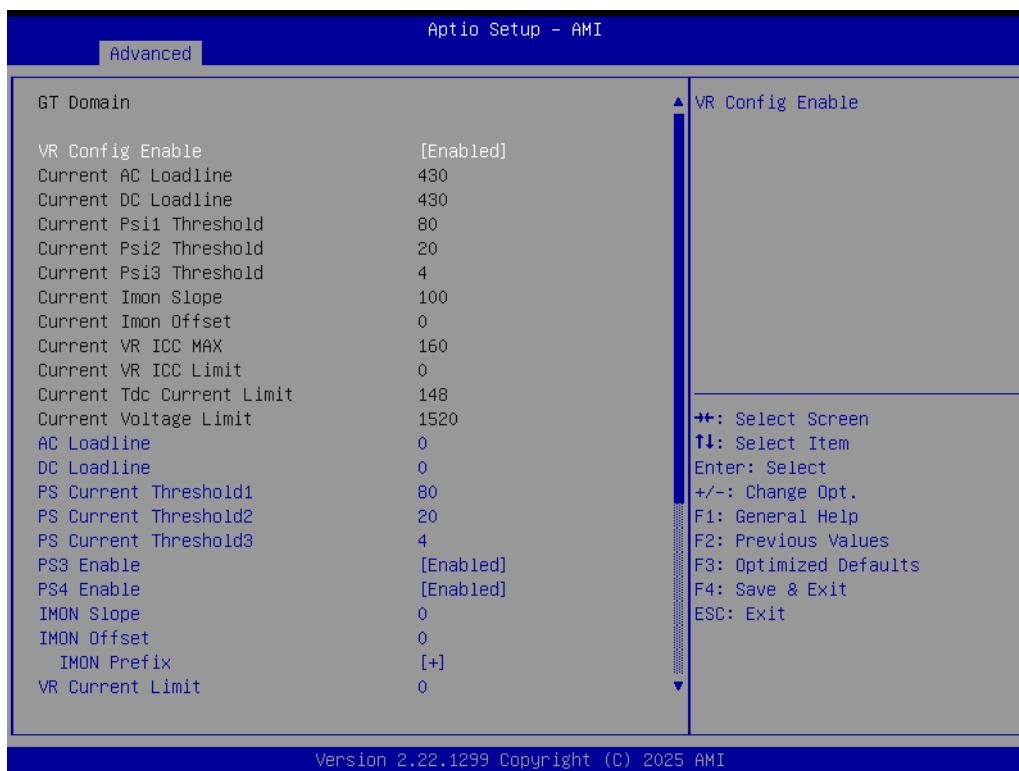
Efficiency/Performance VR Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU
VR Settings → Efficiency/Performance VR Settings



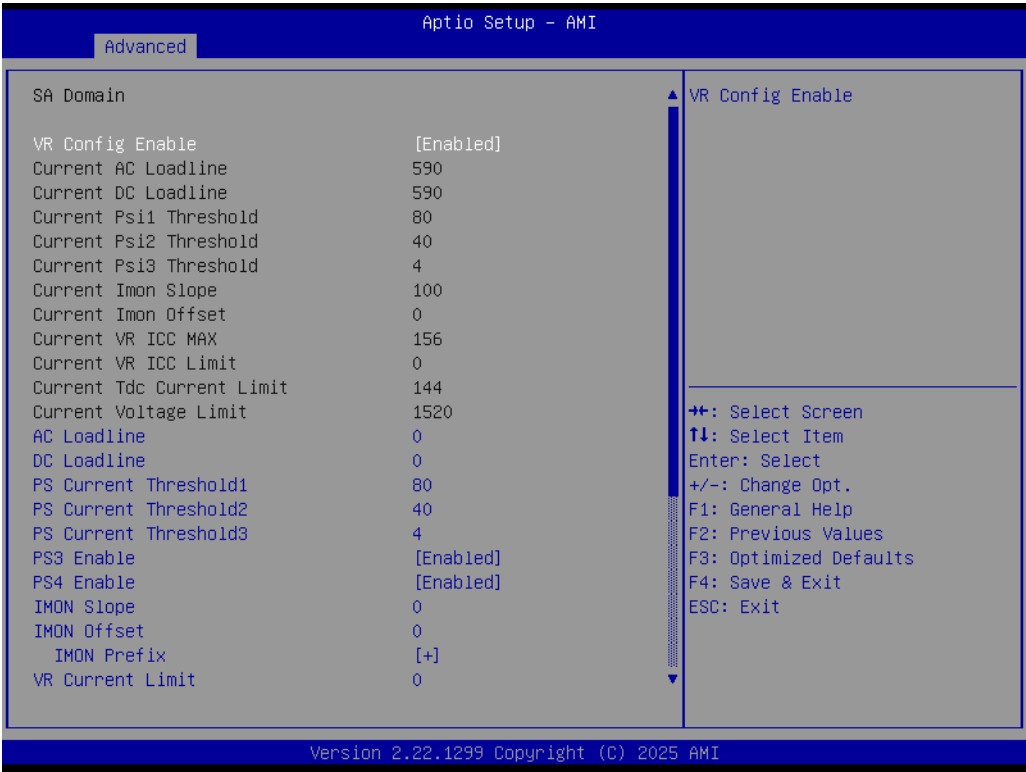
GT VR Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU
VR Settings → GT VR Settings



SA VR Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → SA VR Settings



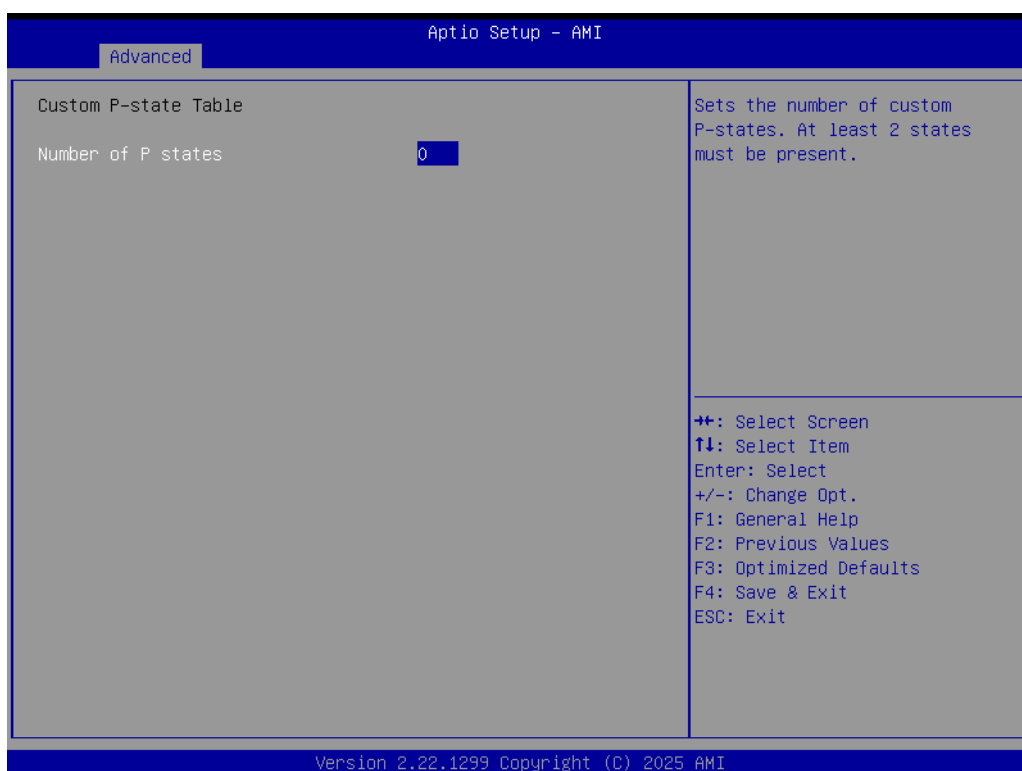
RFI Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → RFI Settings



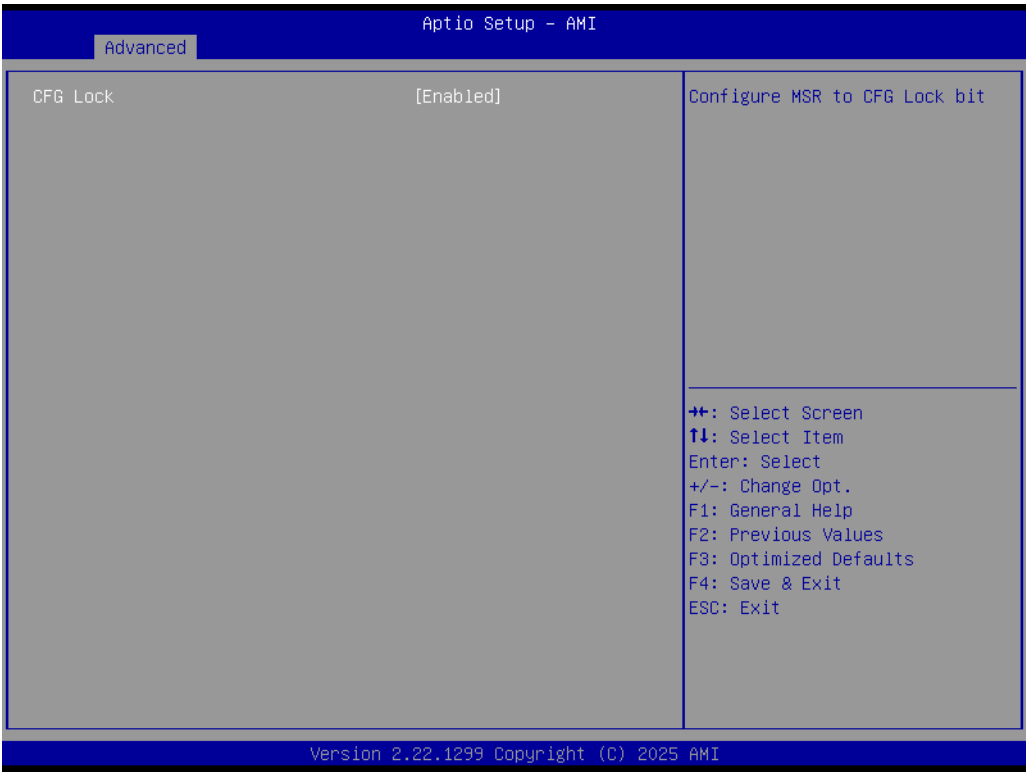
Custom P-state Table

Advanced → Power & Performance → CPU – Power Management Control → Custom P-state Table



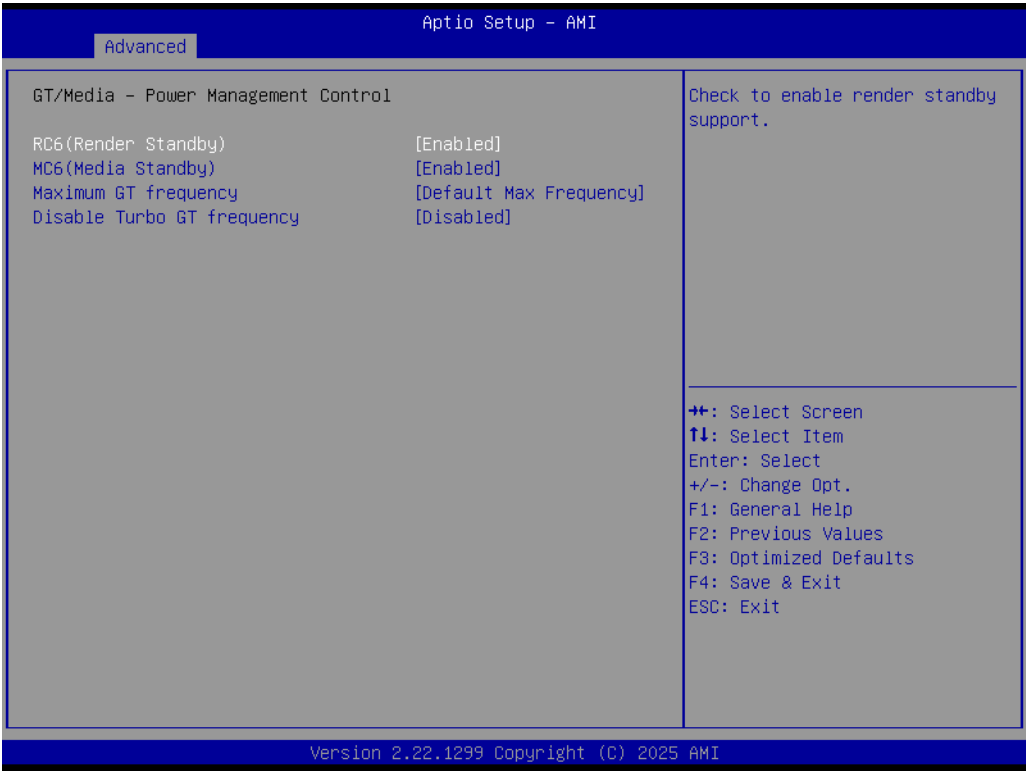
CFG Lock

Advanced → Power & Performance → CPU – Power Management Control → CFG Lock



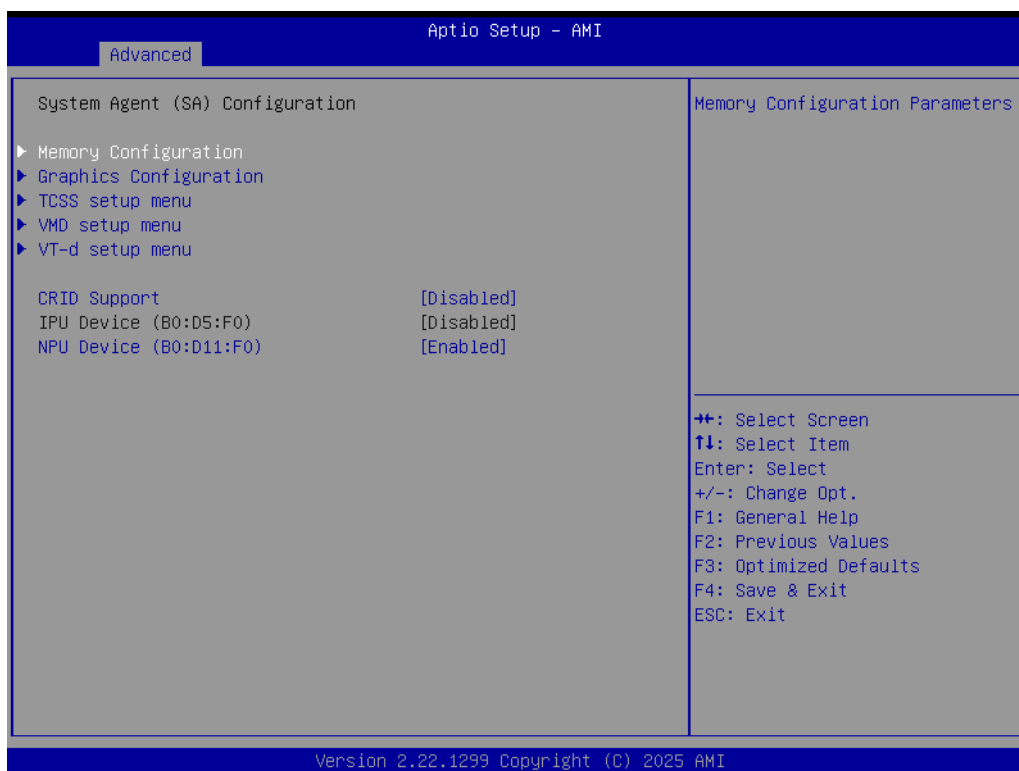
GT/Media – Power Management Control

Advanced → Power & Performance → GT/Media – Power Management Control



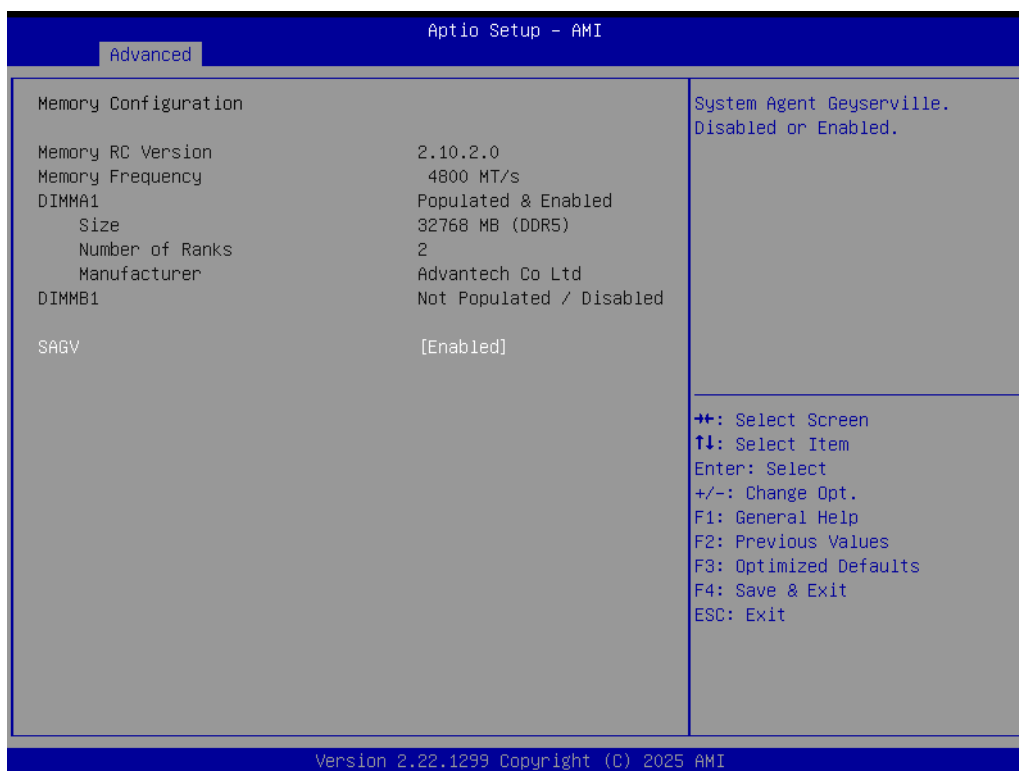
3.2.2.3 System Agent (SA) Configuration

Advanced → System Agent (SA) Configuration



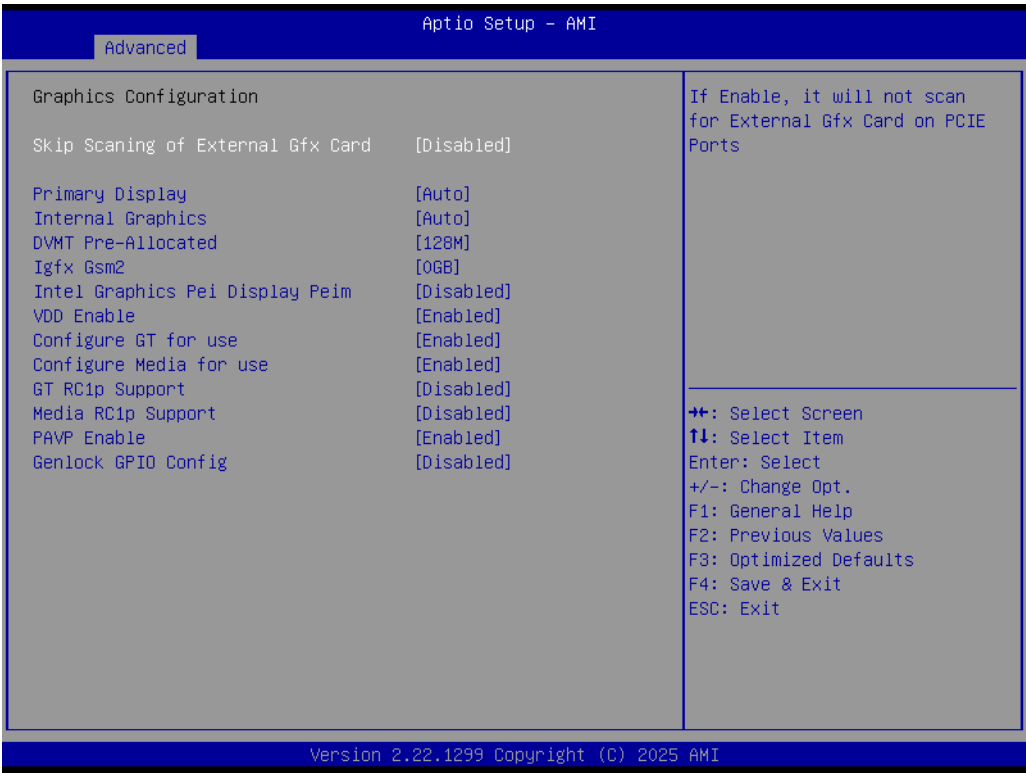
Memory Configuration

Advanced → System Agent (SA) Configuration → Memory Configuration



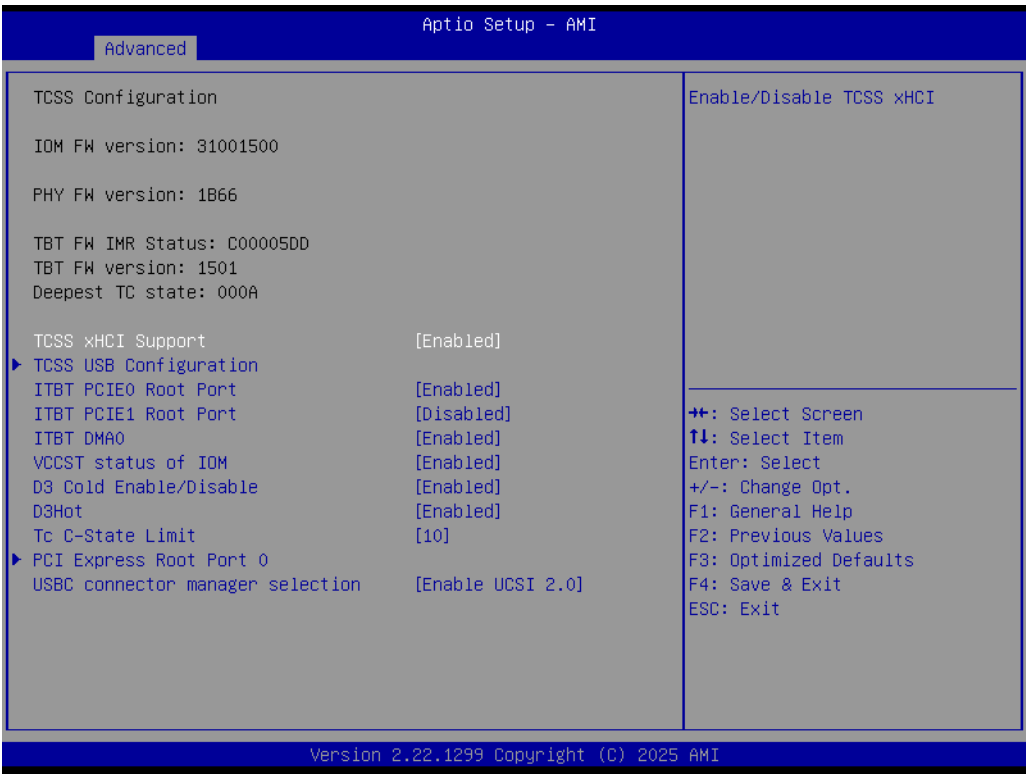
Graphics Configuration

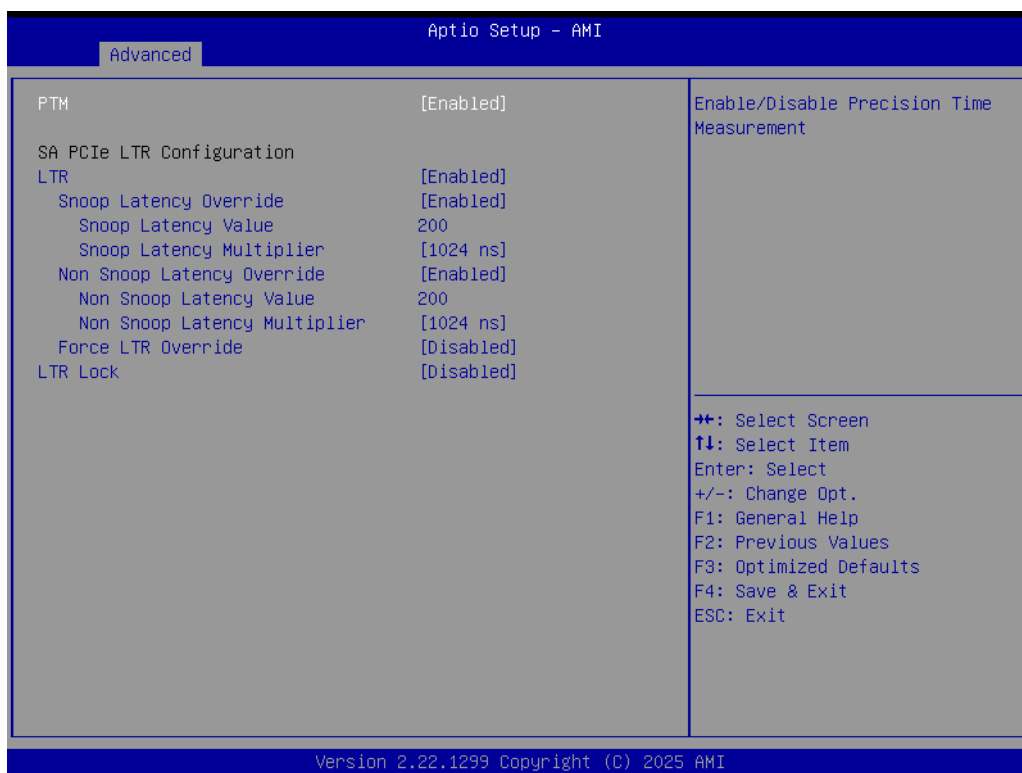
Advanced → System Agent (SA) Configuration → Graphics Configuration



TCSS Configuration

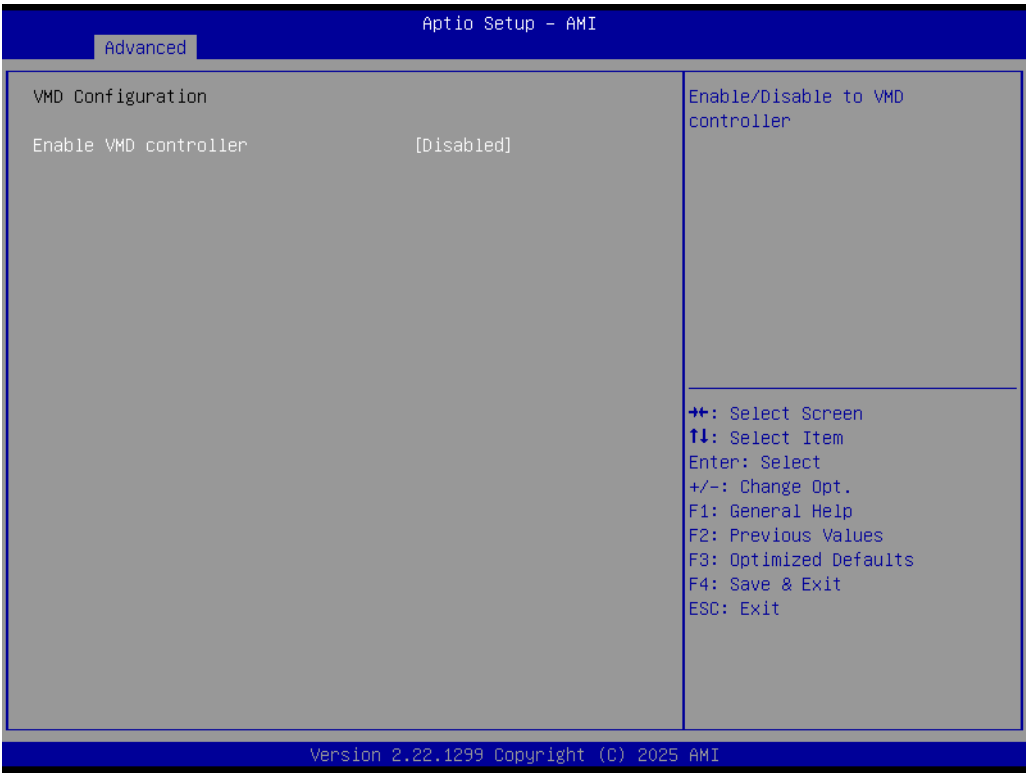
Advanced → System Agent (SA) Configuration → TCSS Configuration





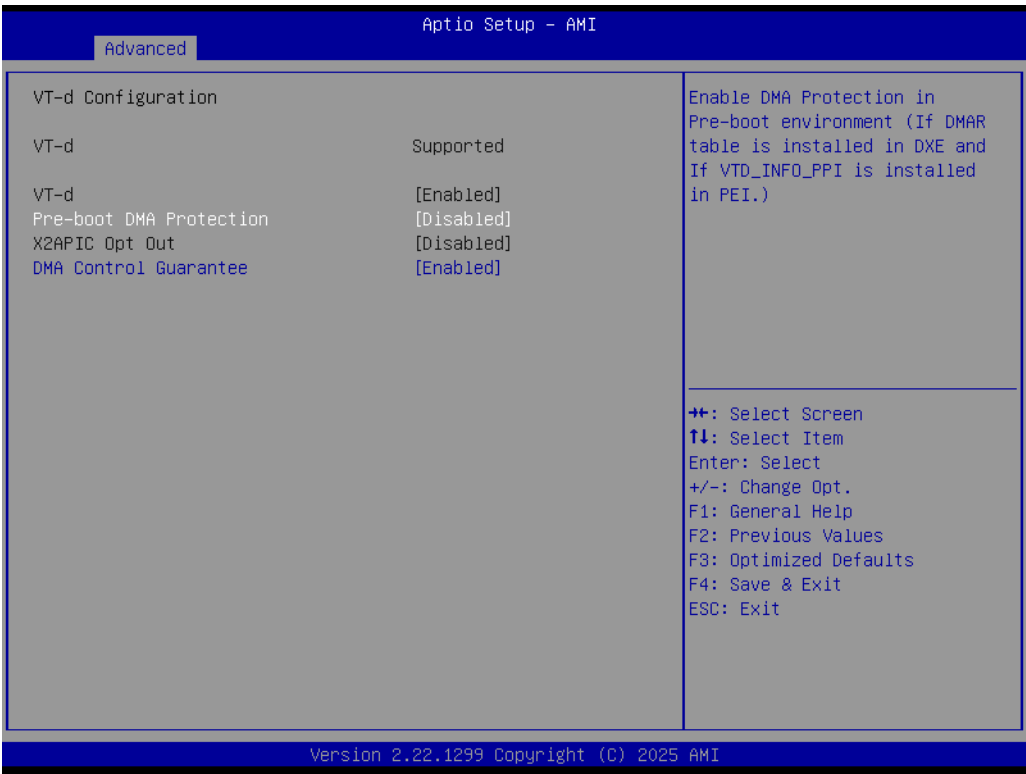
VMD Configuration

Advanced → System Agent (SA) Configuration → VMD Configuration



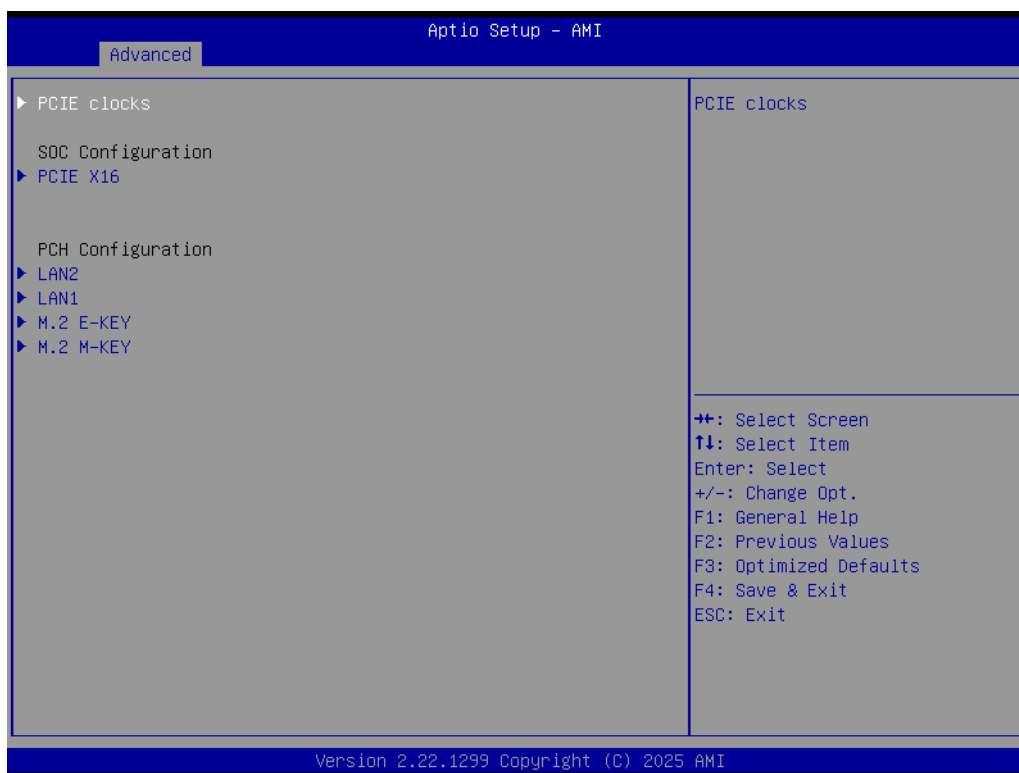
VT-d Configuration

Advanced → System Agent (SA) Configuration → VT-d Configuration



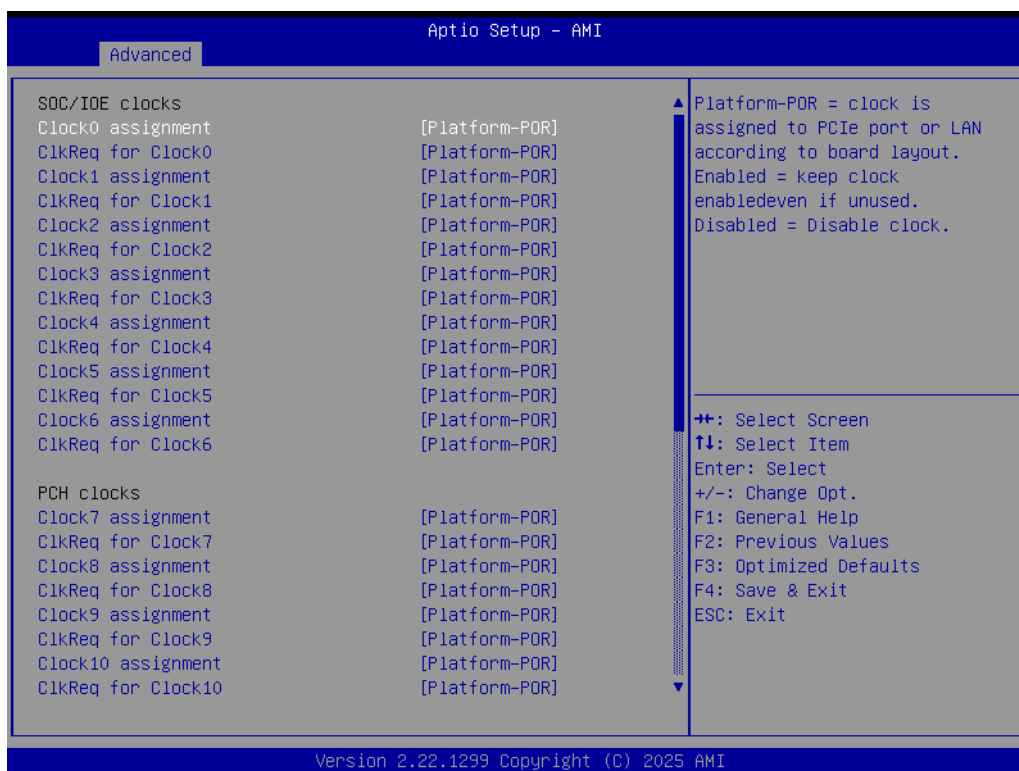
3.2.2.4 PCIE Configuration

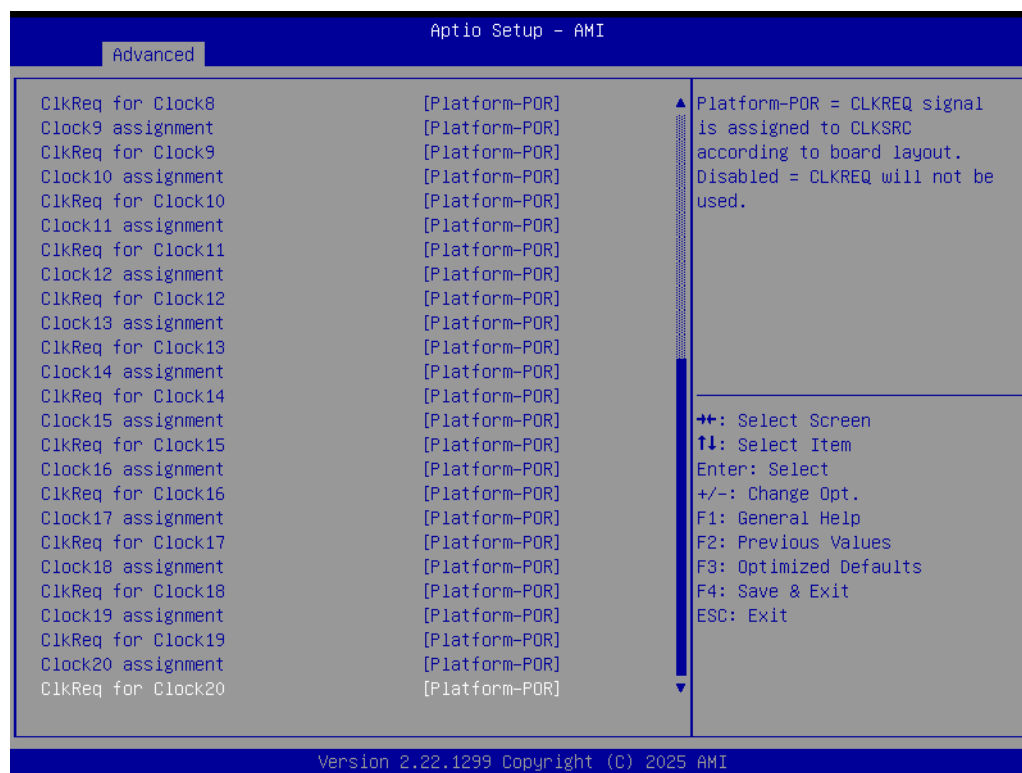
Advanced → PCIE Configuration



SOC Configuration

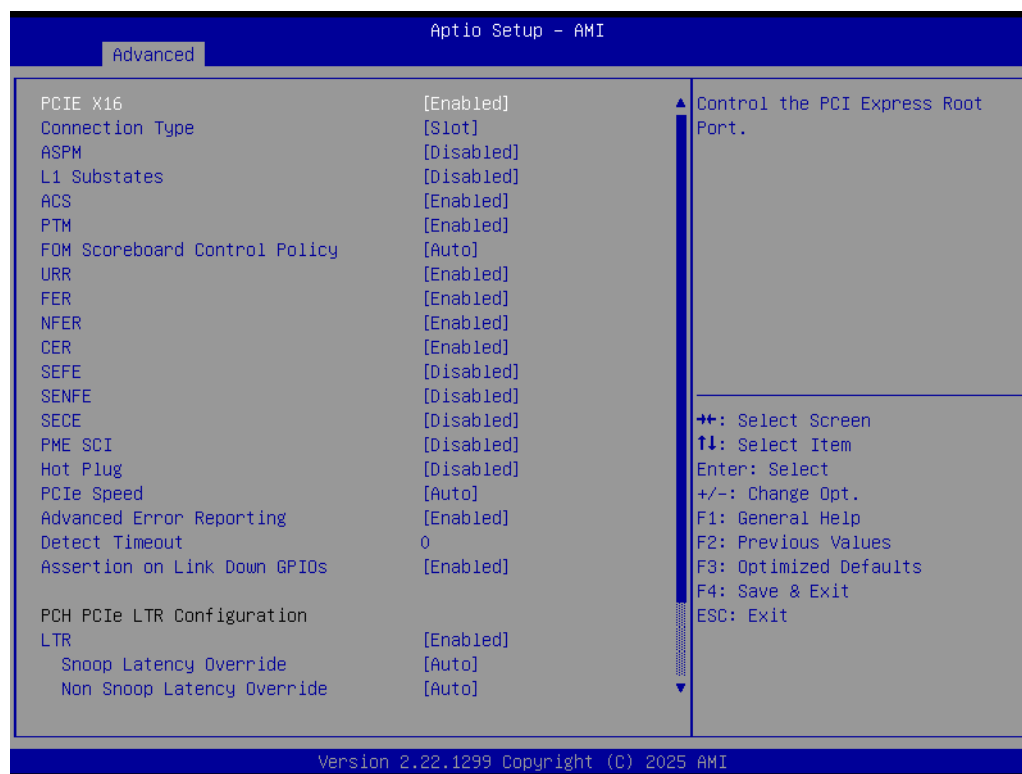
Advanced → PCIE Configuration → SOC Configuration

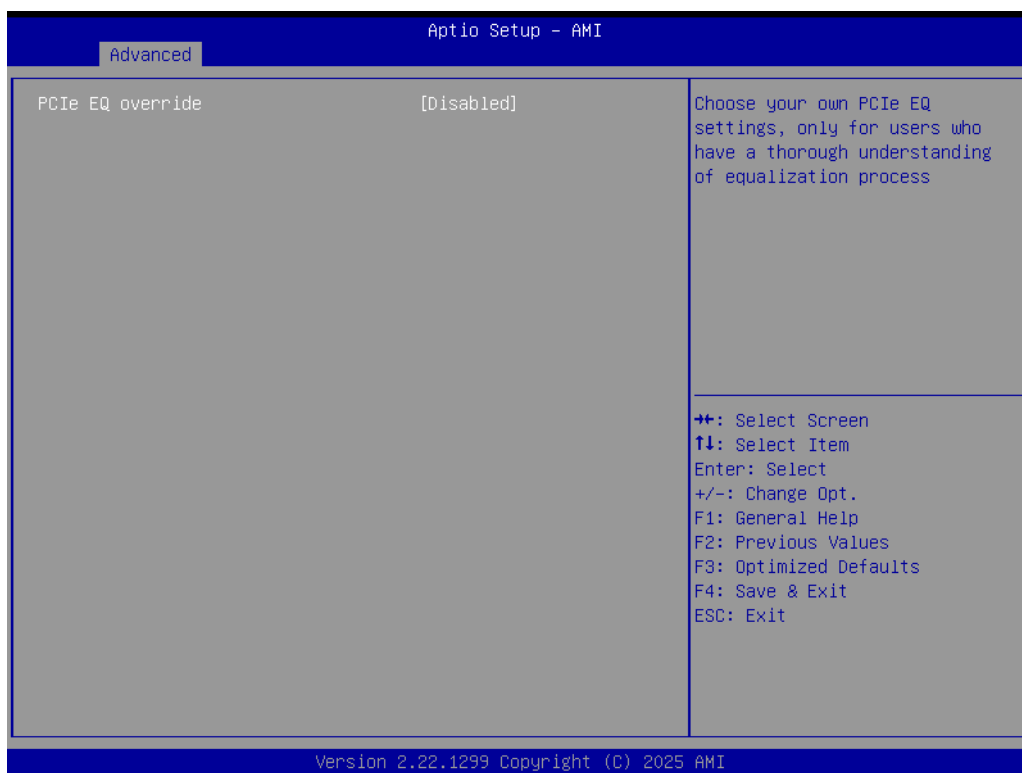
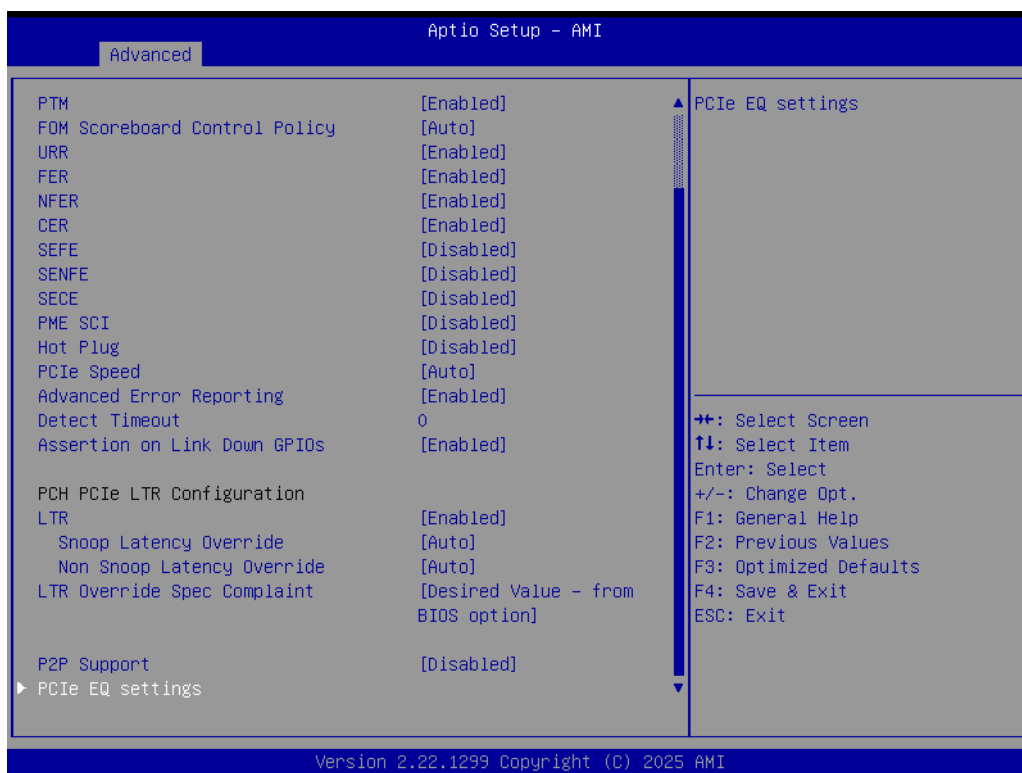




PCIE X16

Advanced → PCIE Configuration → PCIE X16



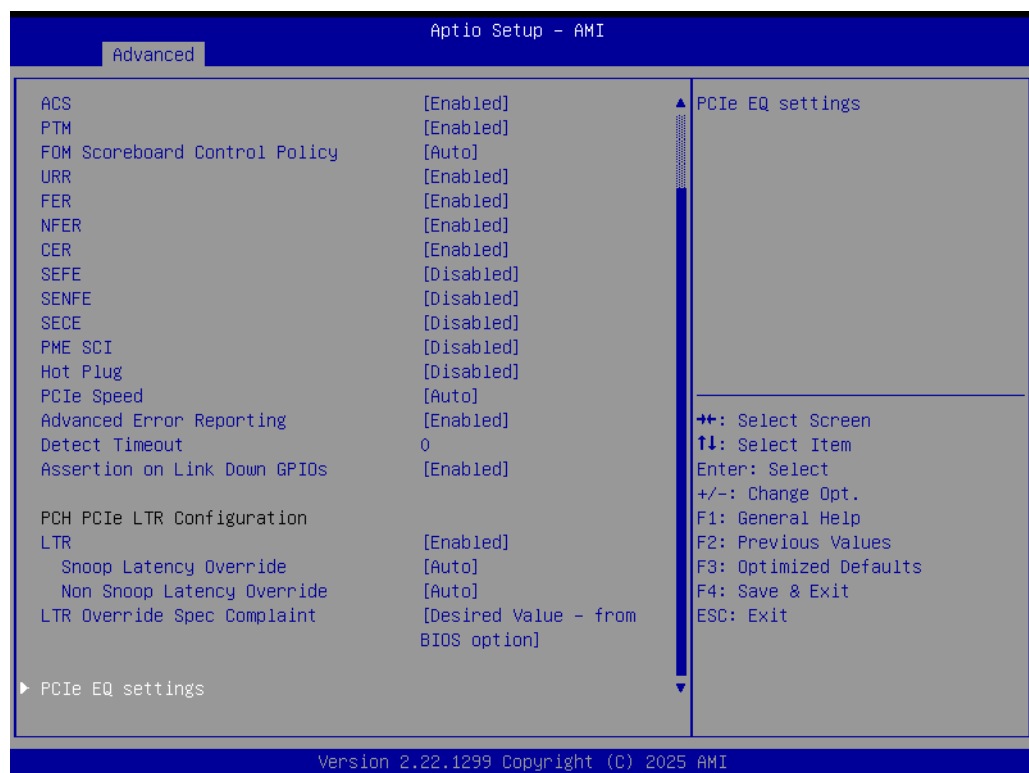
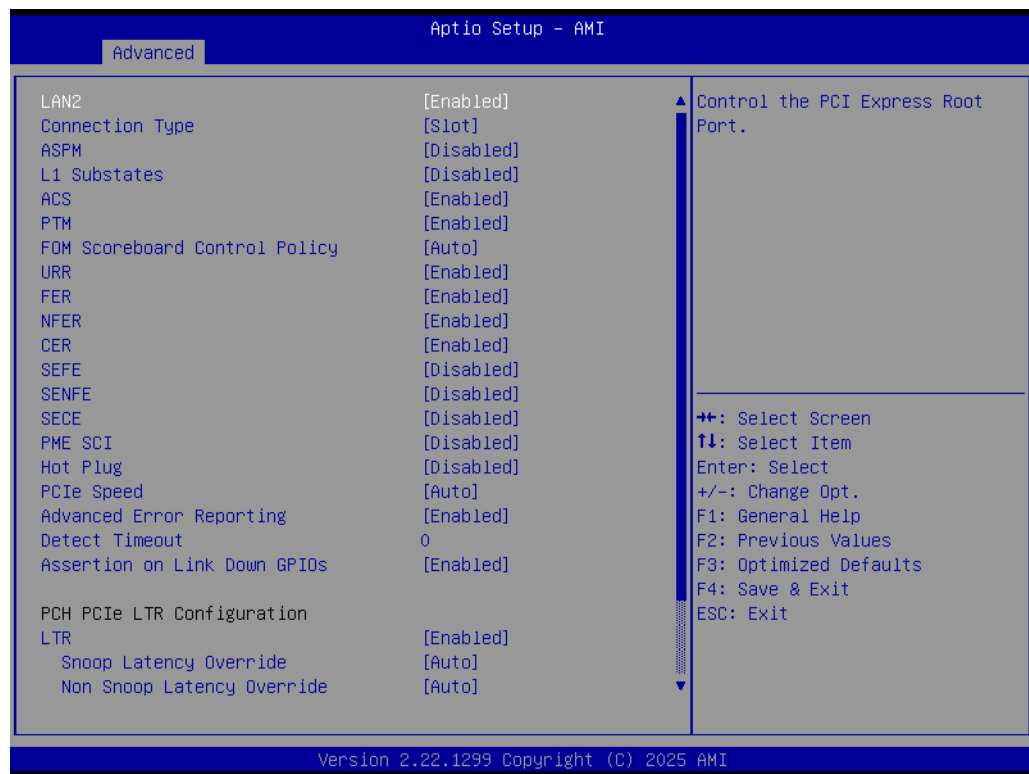


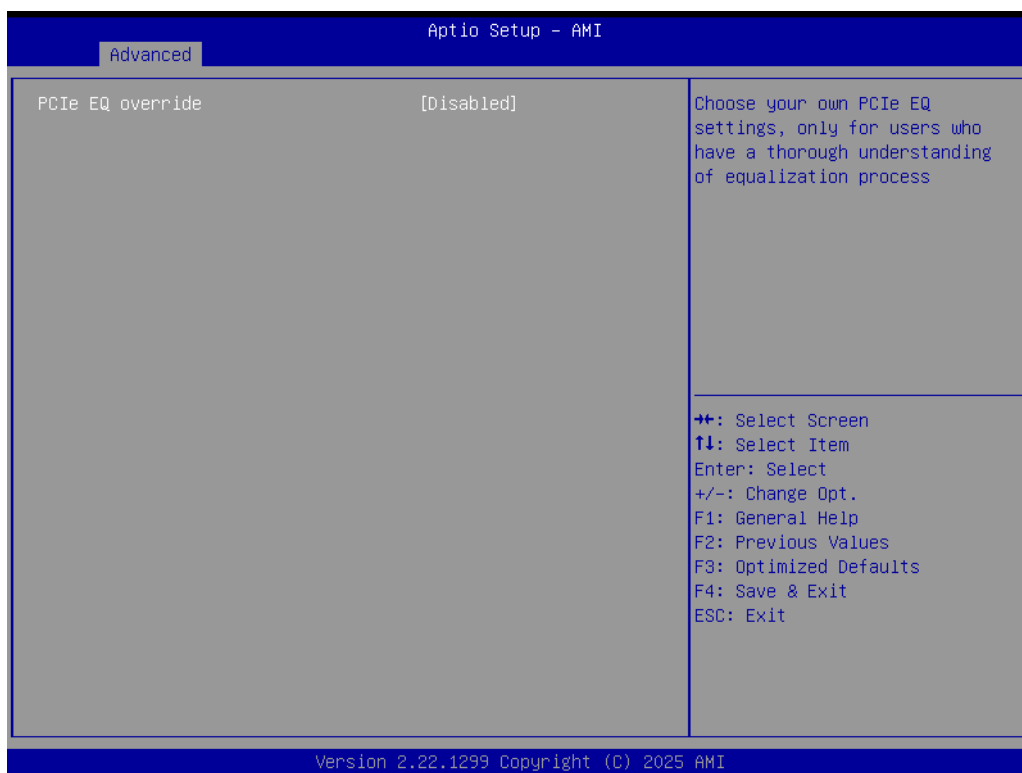
PCH Configuration

Advanced → PCIE Configuration → PCH Configuration

LAN2

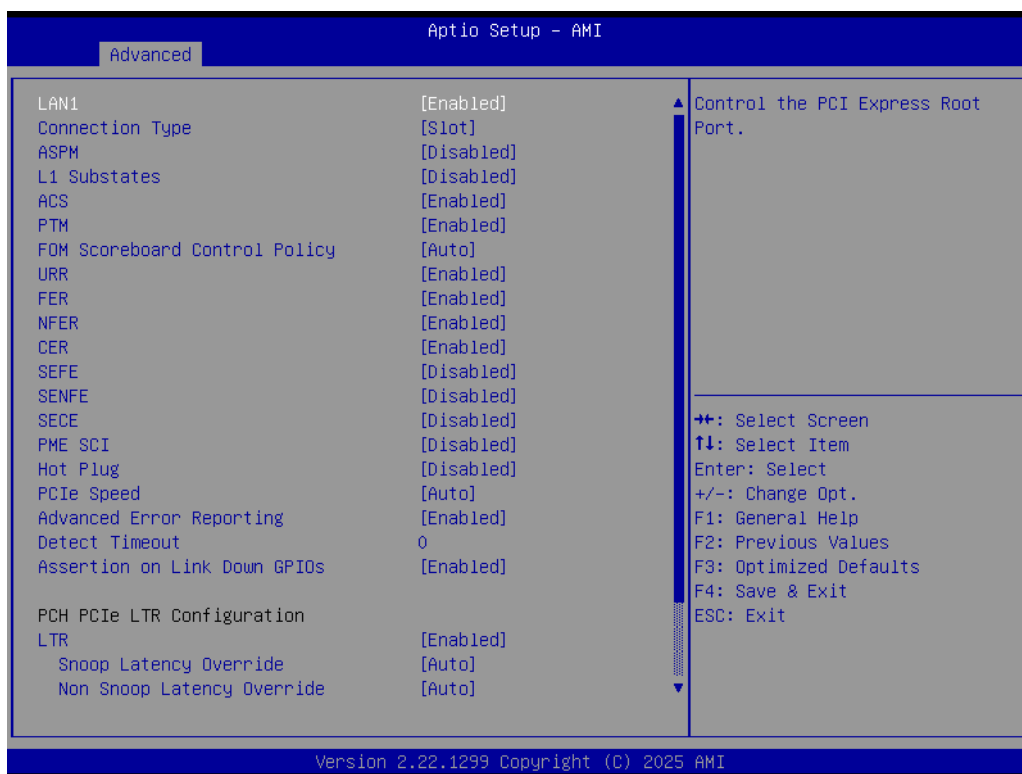
Advanced → PCIE Configuration → PCH Configuration → LAN2

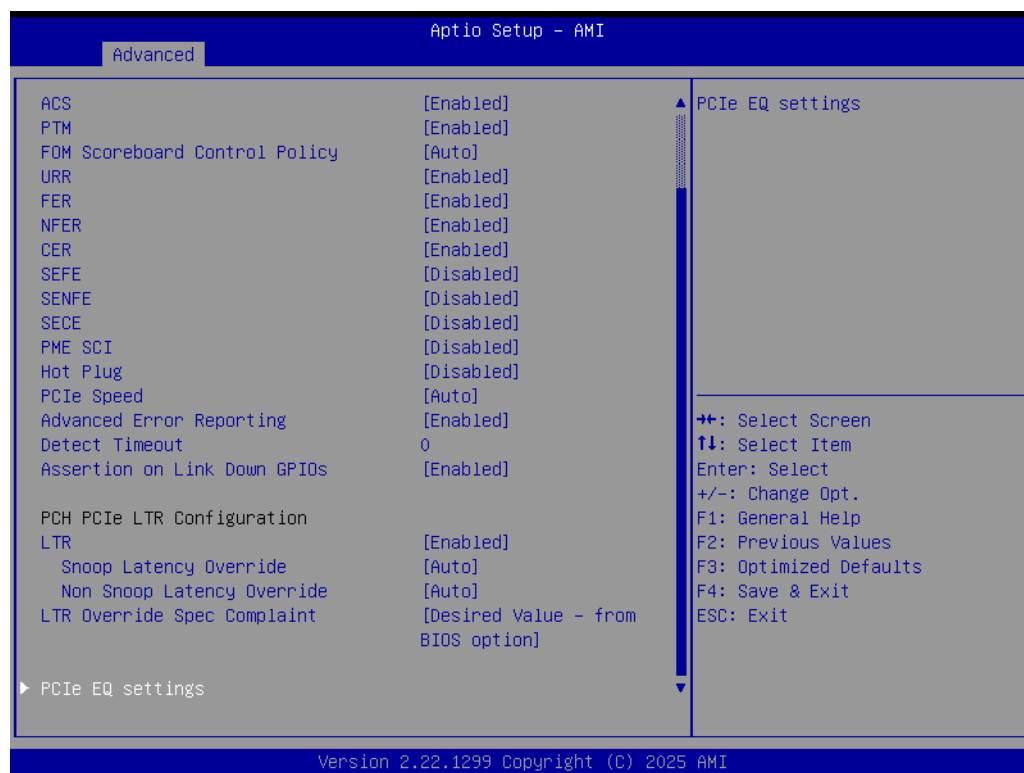




LAN1

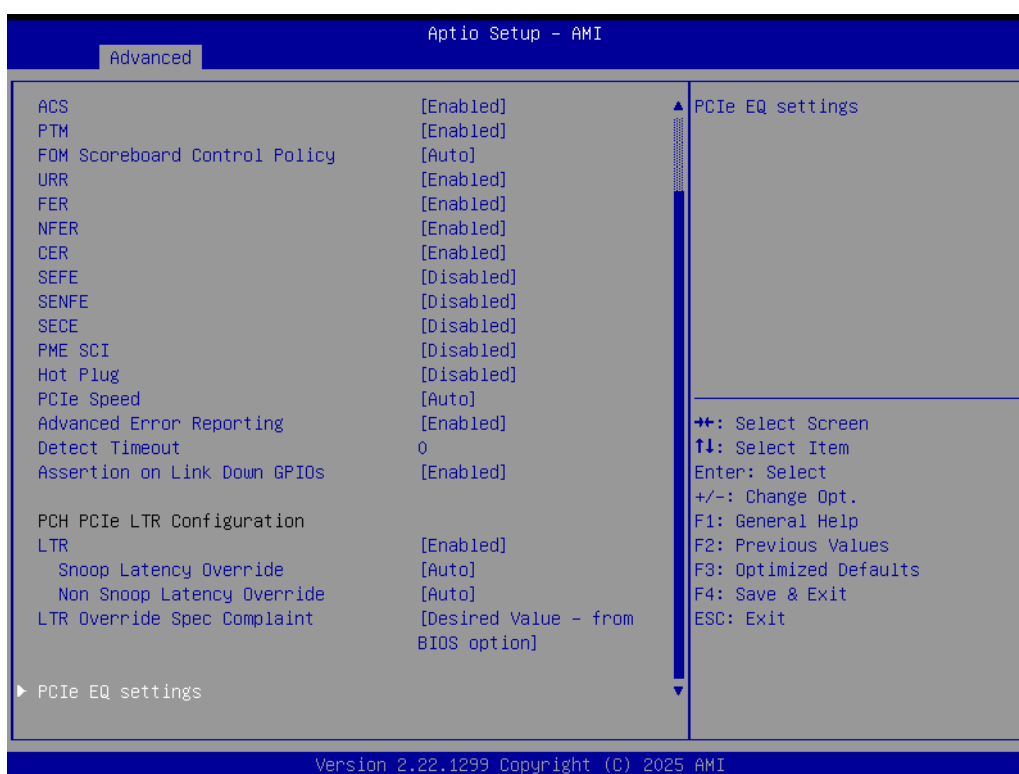
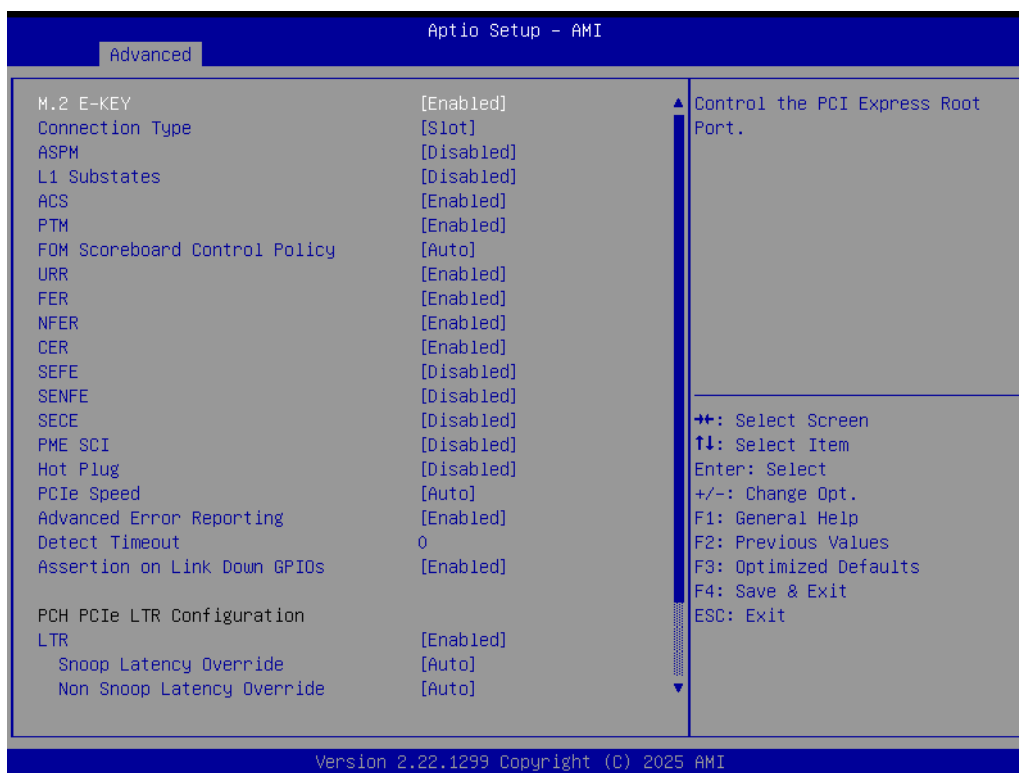
Advanced → PCIE Configuration → PCH Configuration → LAN1





M.2 E-Key

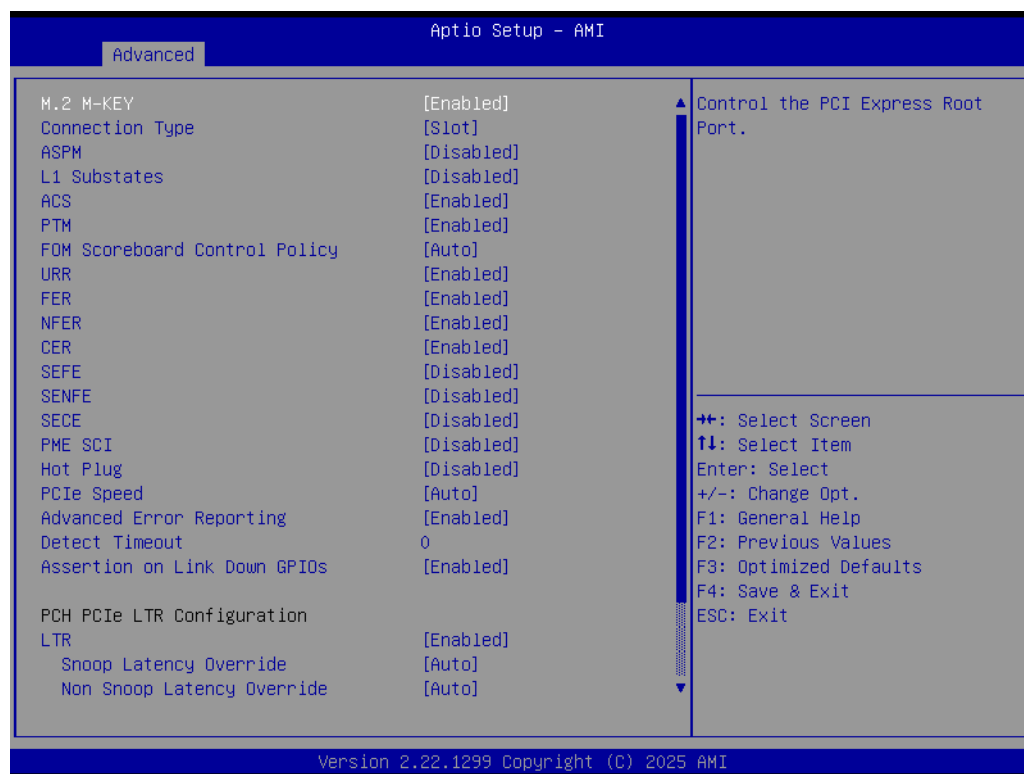
Advanced → PCIE Configuration → PCH Configuration → M.2 E-KEY

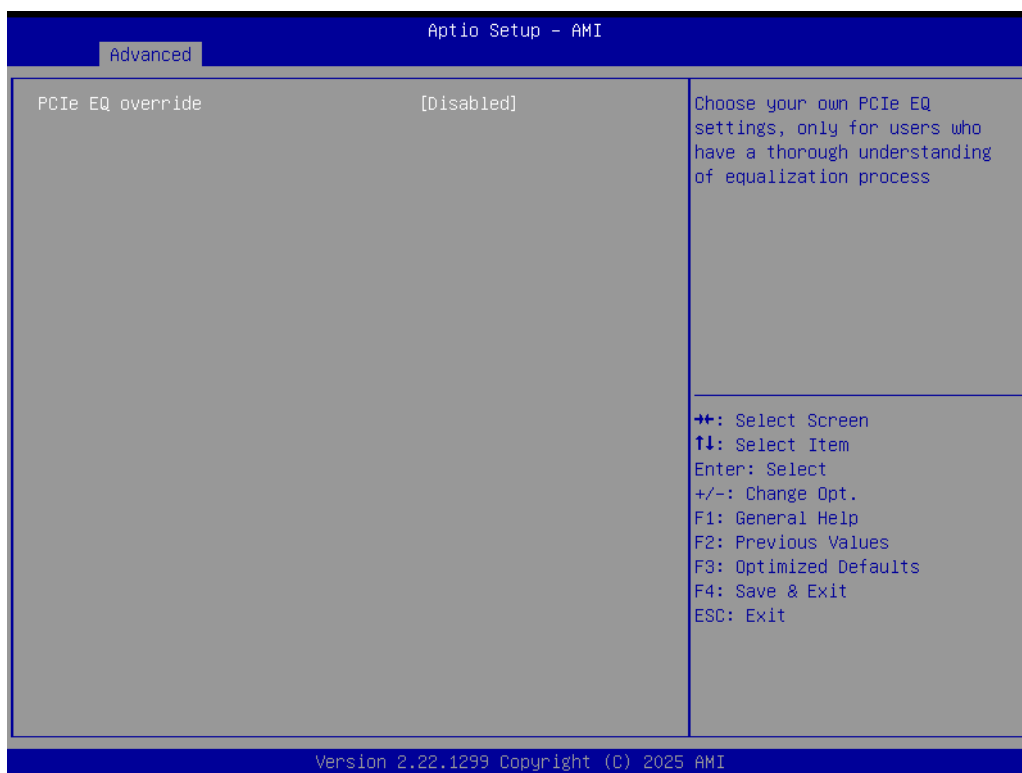
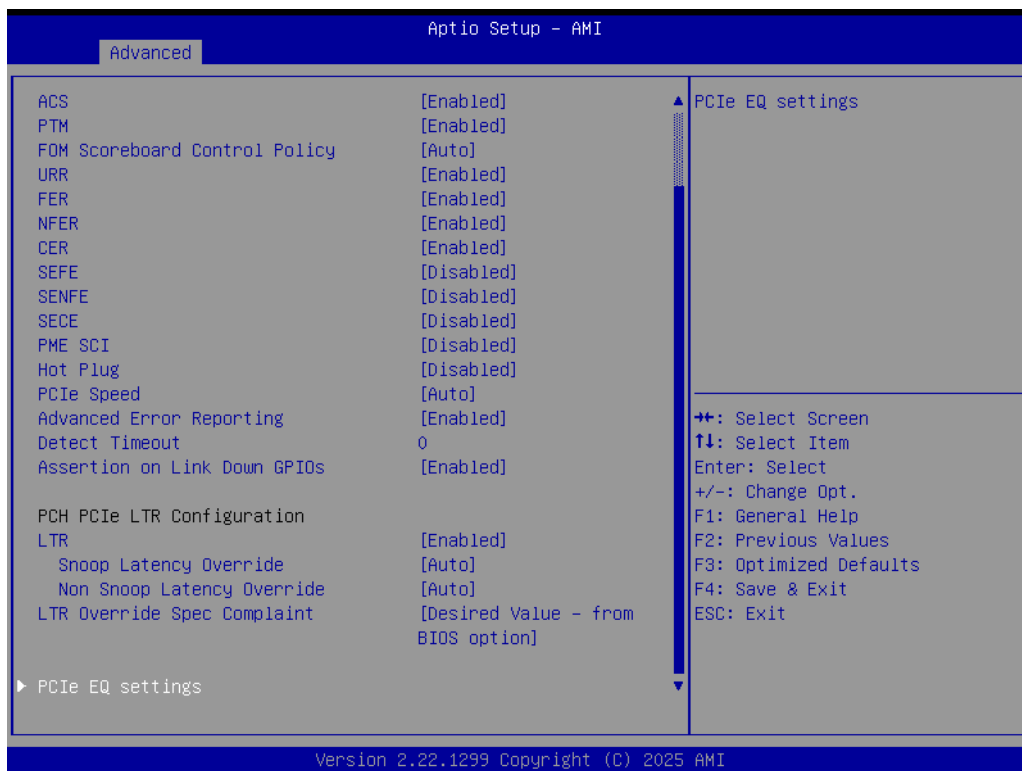




M.2 M-Key

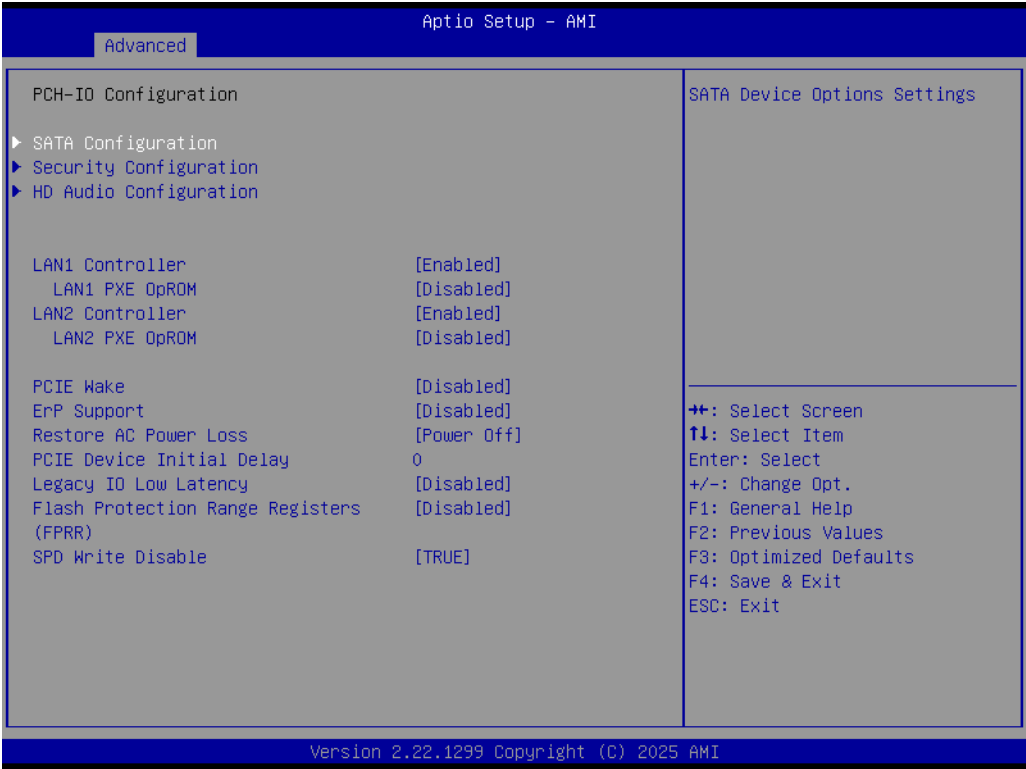
Advanced → PCIE Configuration → PCH Configuration → M.2 M-KEY





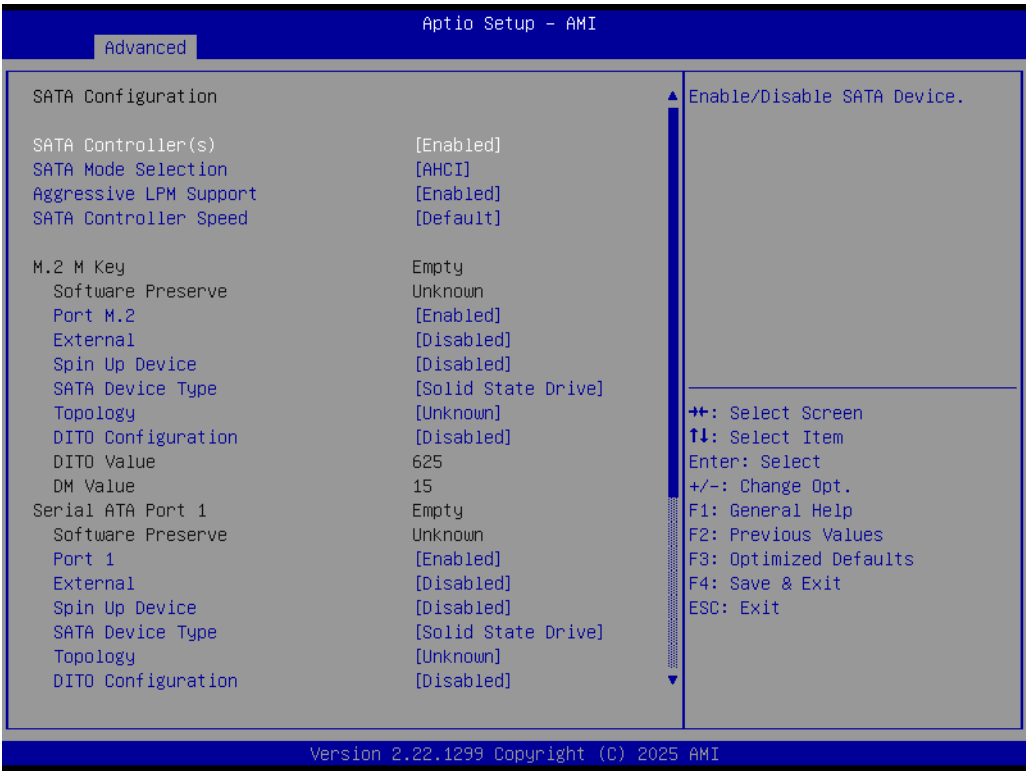
3.2.2.5 PCH-IO Configuration

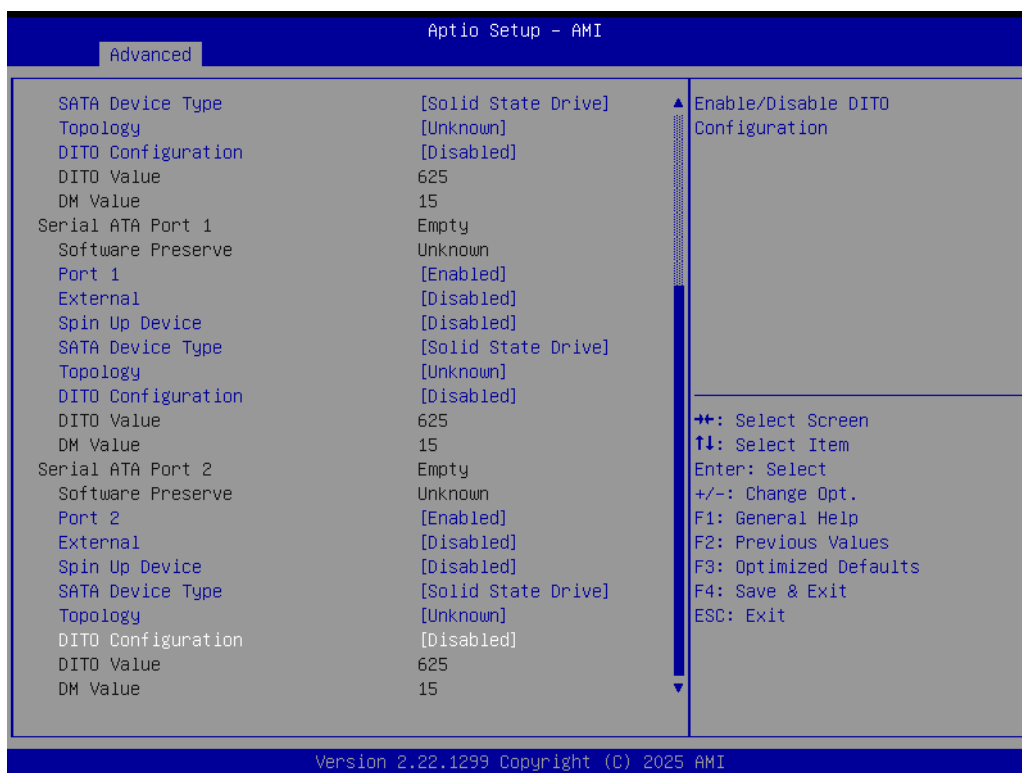
Advanced → PCH-IO Configuration



SATA Configuration

Advanced → PCH-IO Configuration → SATA Configuration





Security Configuration

Advanced → PCH-IO Configuration → Security Configuration



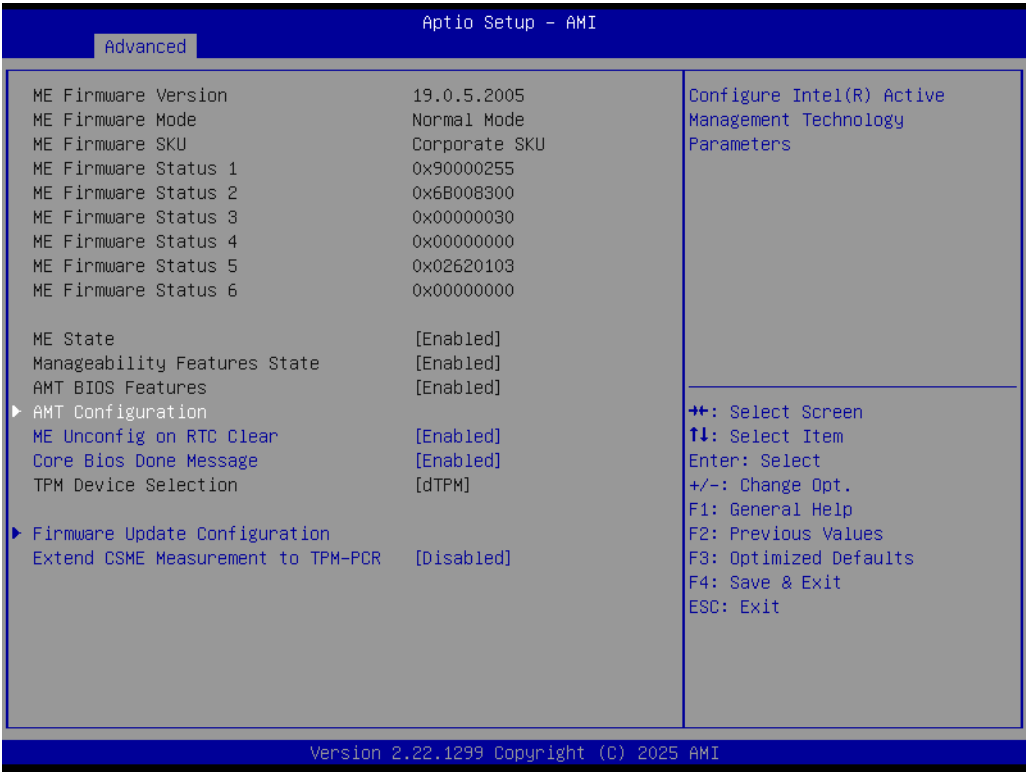
HD Audio Subsystem Configuration Settings

Advanced → PCH-IO Configuration → HD Audio Subsystem Configuration Settings



3.2.2.6 PCH-FW Configuration

Advanced → PCH-FW Configuration



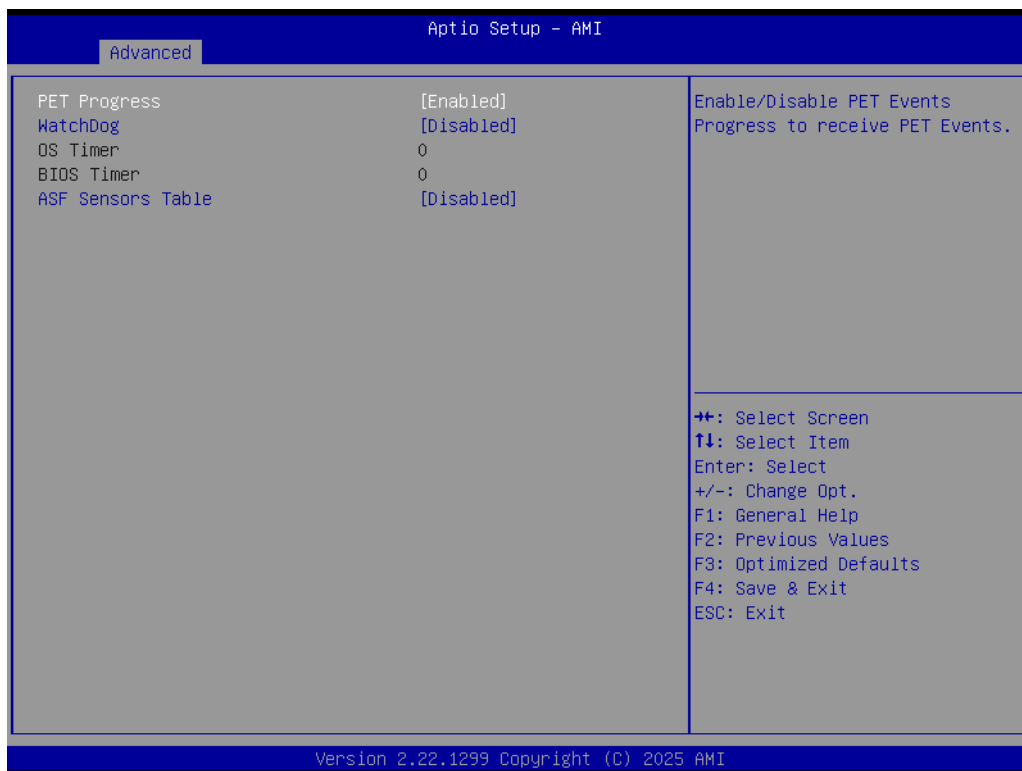
AMT Configuration

Advanced → PCH-FW Configuration → AMT Configuration



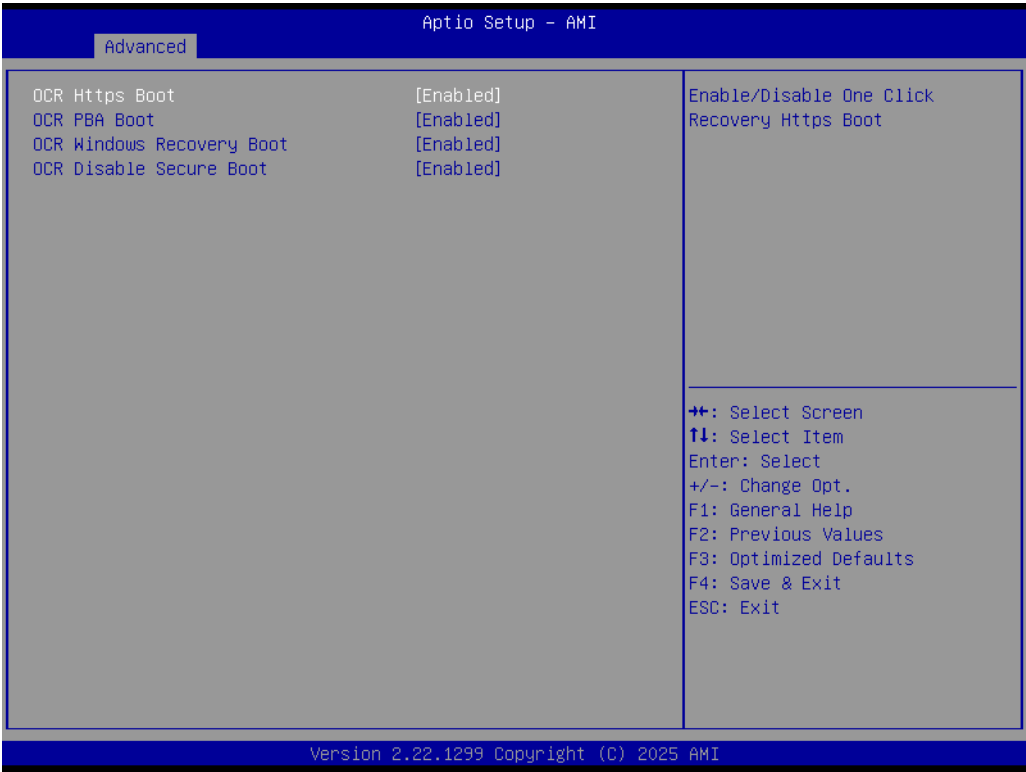
ASF Configuration

Advanced → PCH-FW Configuration → AMT Configuration → ASF Configuration



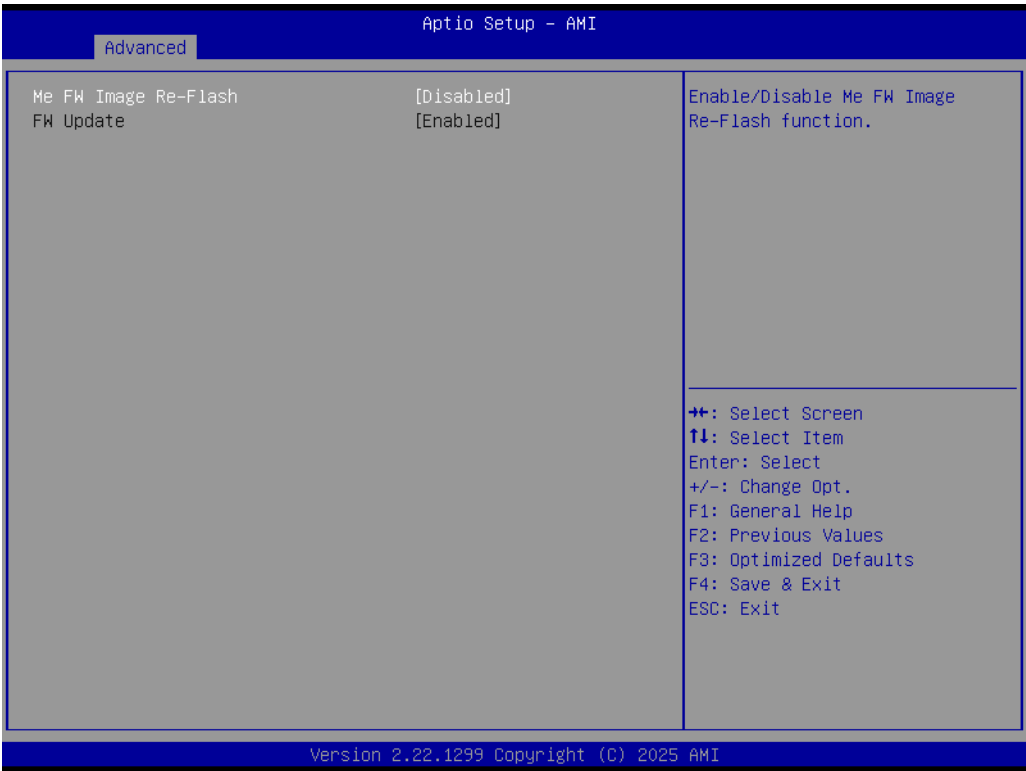
One Click Recovery (OCR) Configuration

Advanced → PCH-FW Configuration → AMT Configuration → One Click Recovery (OCR) Configuration



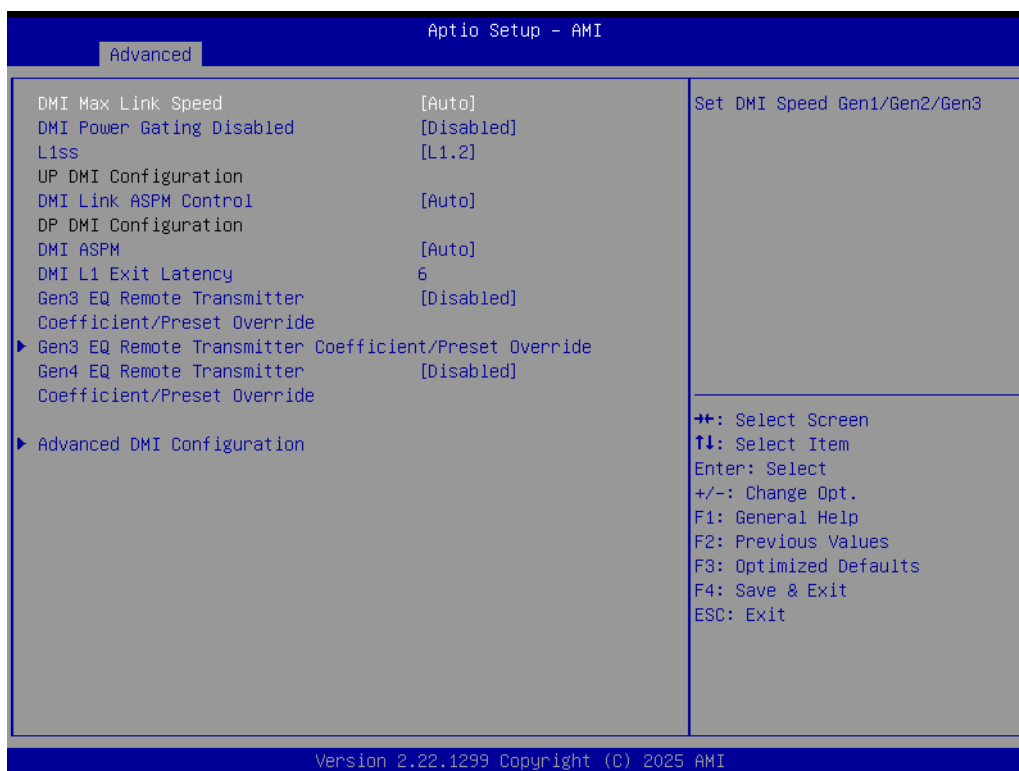
Firmware Update Configuration

Advanced → PCH-FW Configuration → Firmware Update Configuration



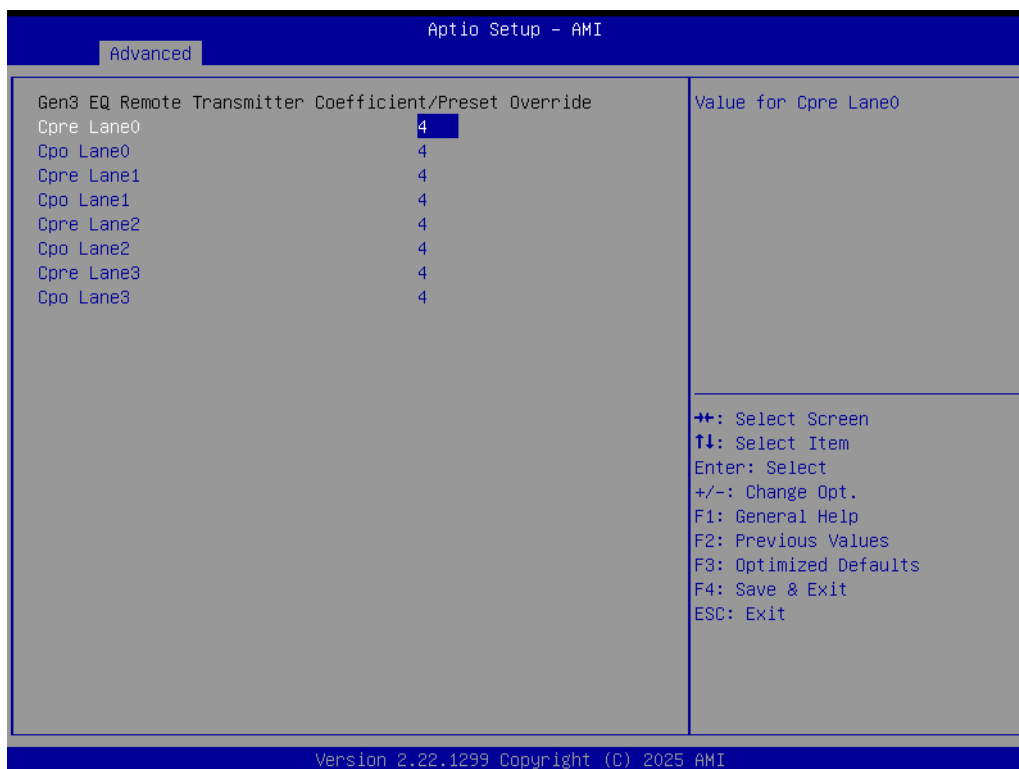
3.2.2.7 DMI Configuration

Advanced → DMI Configuration



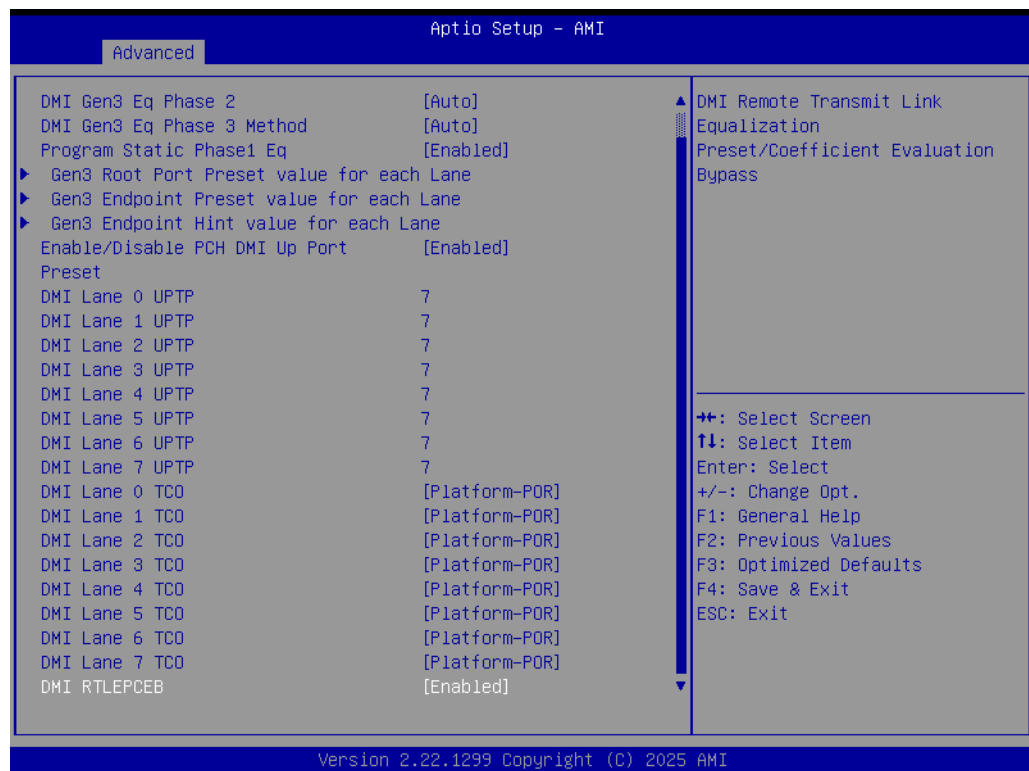
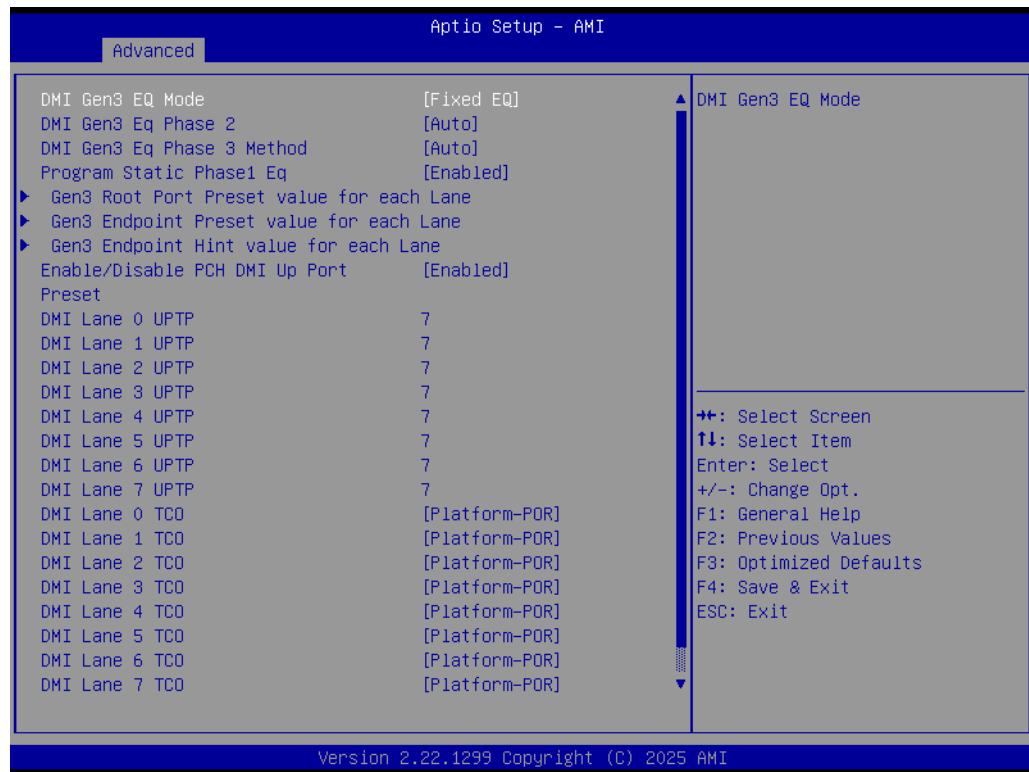
Gen3 EQ Remote Transmitter Coefficient/Preset Override

Advanced → DMI Configuration → Gen3 EQ Remote Transmitter Coefficient/Preset Override



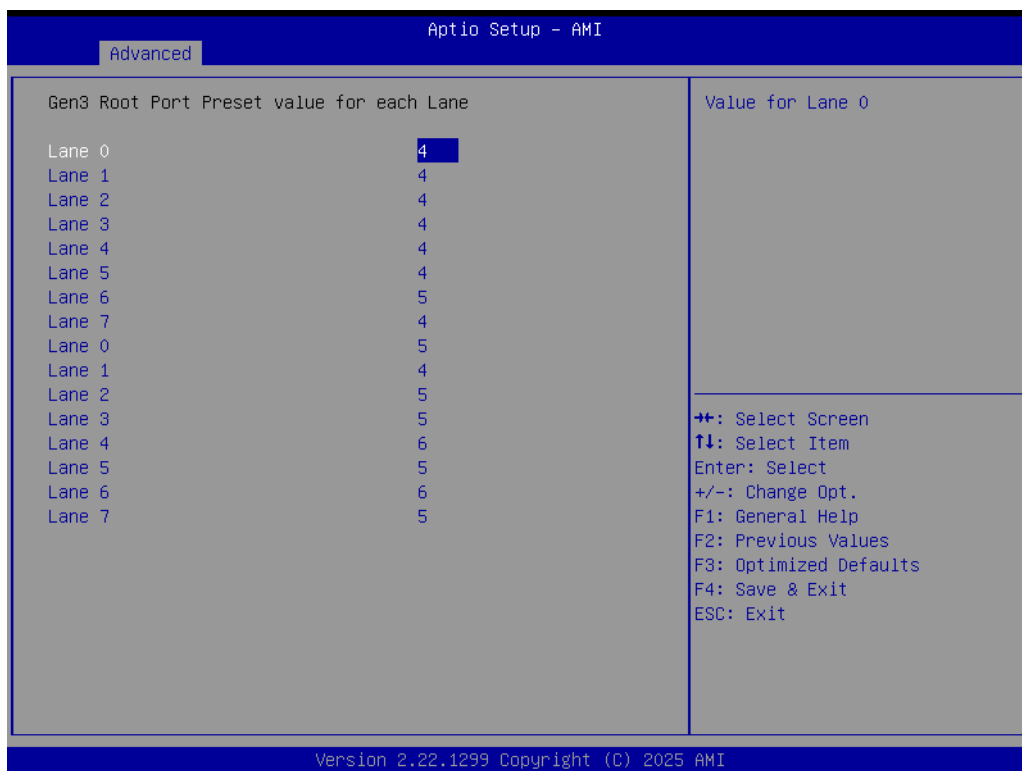
Advanced DMI Configuration

Advanced → DMI Configuration → Advanced DMI Configuration



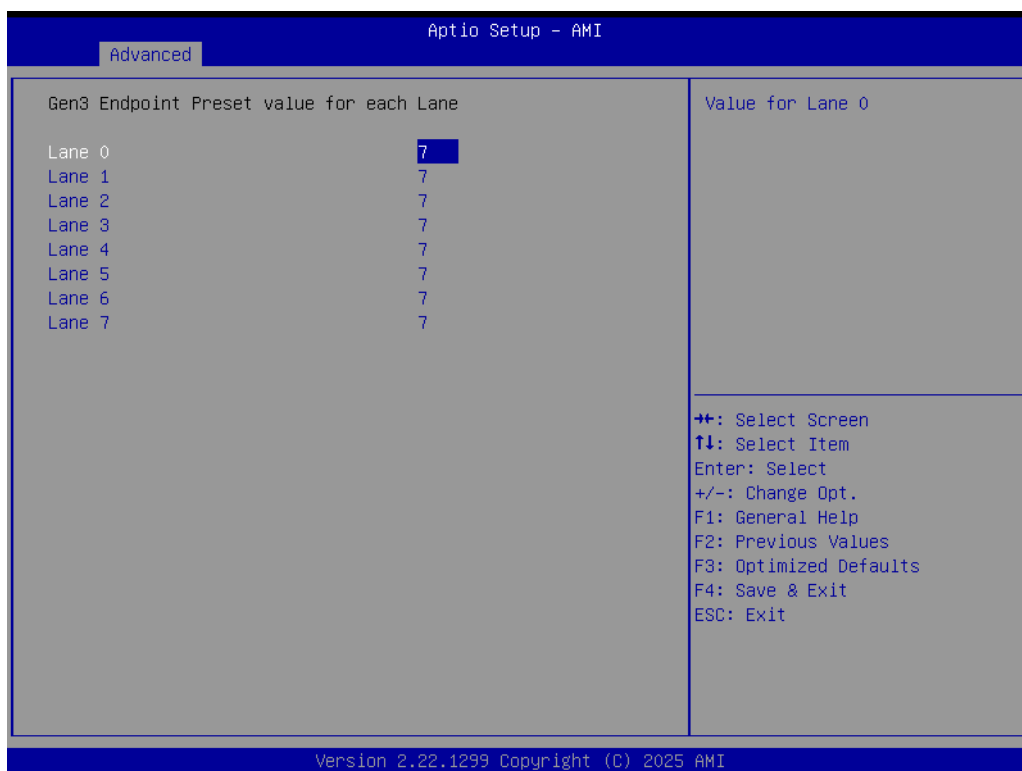
Gen3 Root Port Preset Value for Each Lane

Advanced → DMI Configuration → Advanced DMI Configuration → Gen3 Root Port Preset value for each Lane



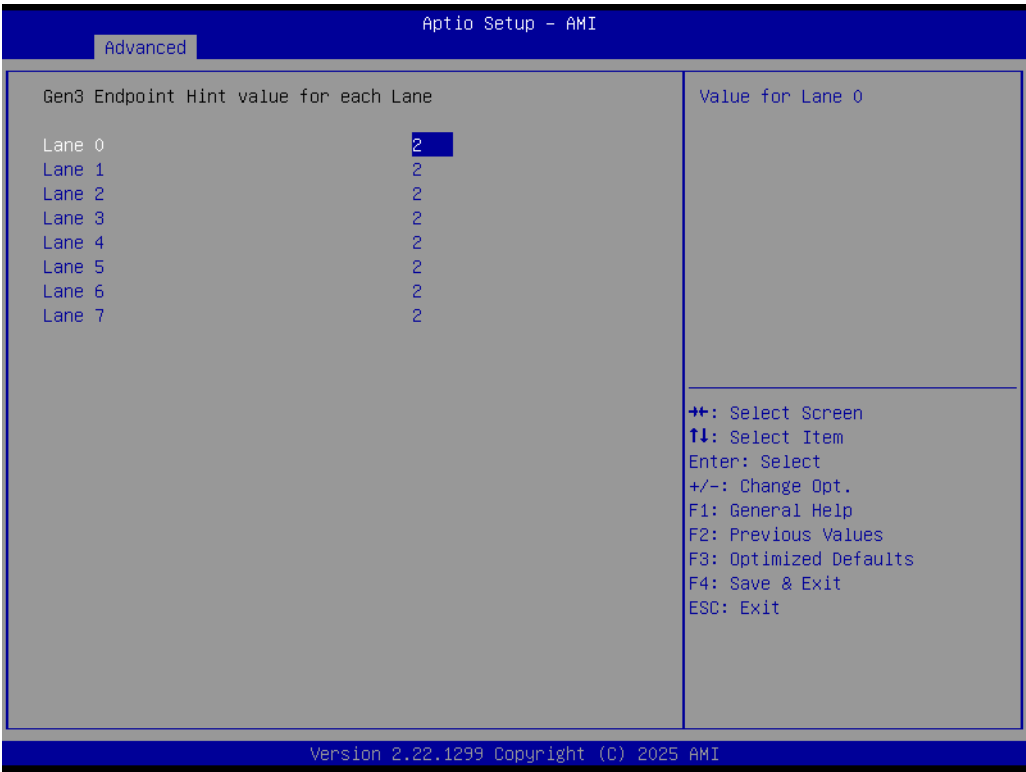
Gen3 Endpoint Preset Value for Each Lane

Advanced → DMI Configuration → Advanced DMI Configuration → Gen3 Endpoint Preset value for each Lane



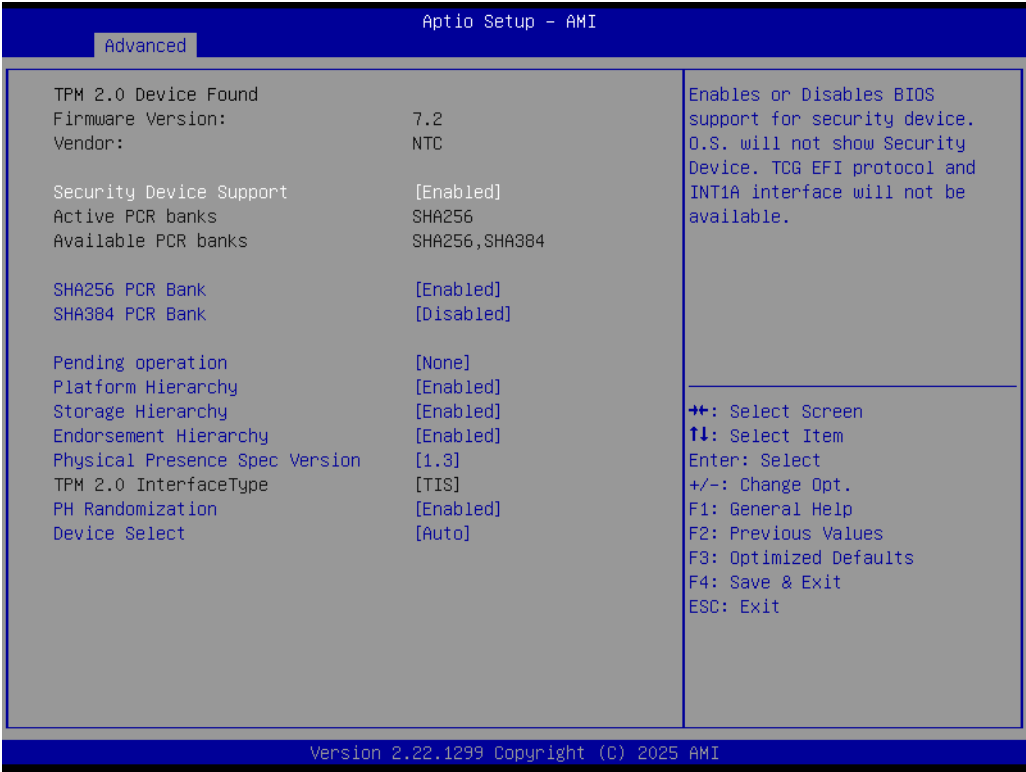
Gen3 Endpoint Hint Value for Each Lane

Advanced → DMI Configuration → Advanced DMI Configuration → Gen3 Endpoint Hint value for each Lane



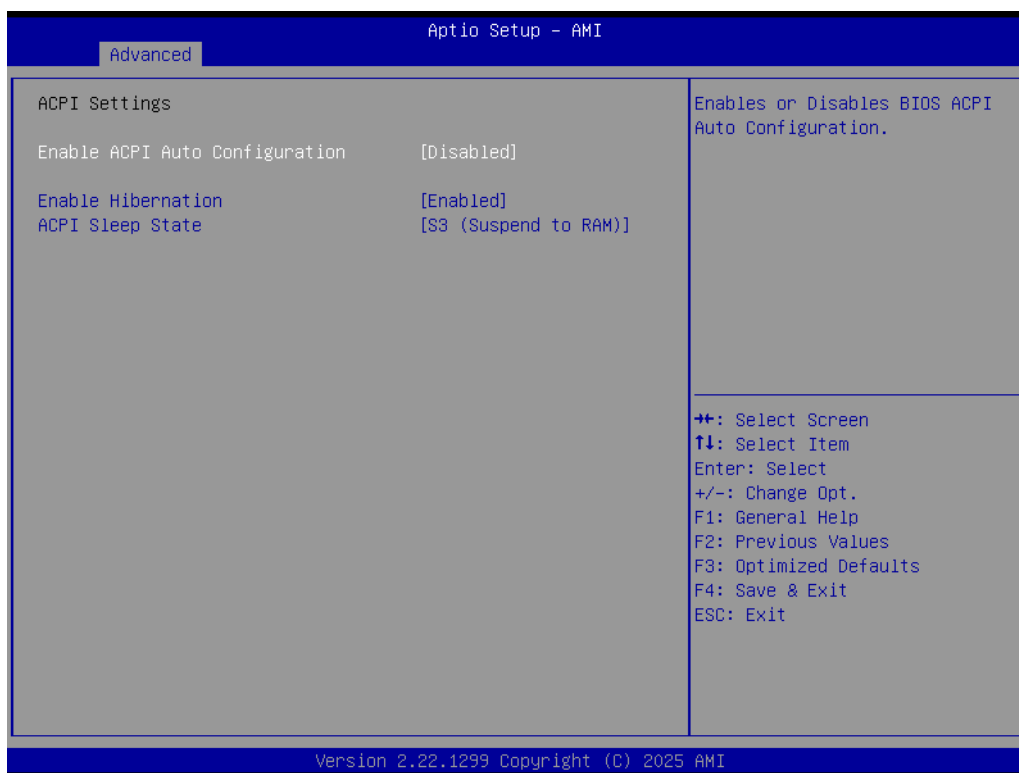
3.2.2.8 Trusted Computing

Advanced → Trusted Computing



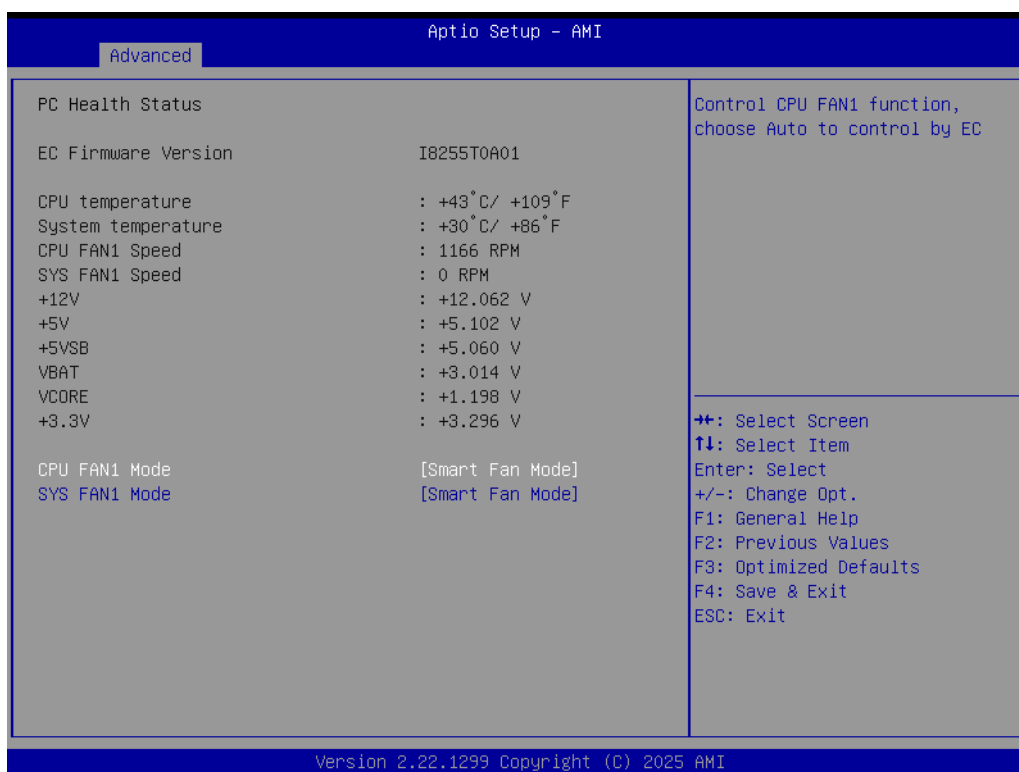
3.2.2.9 ACPI Settings

Advanced → ACPI Settings



3.2.2.10 IT5782 HW Monitor

Advanced → IT5782 HW Monitor



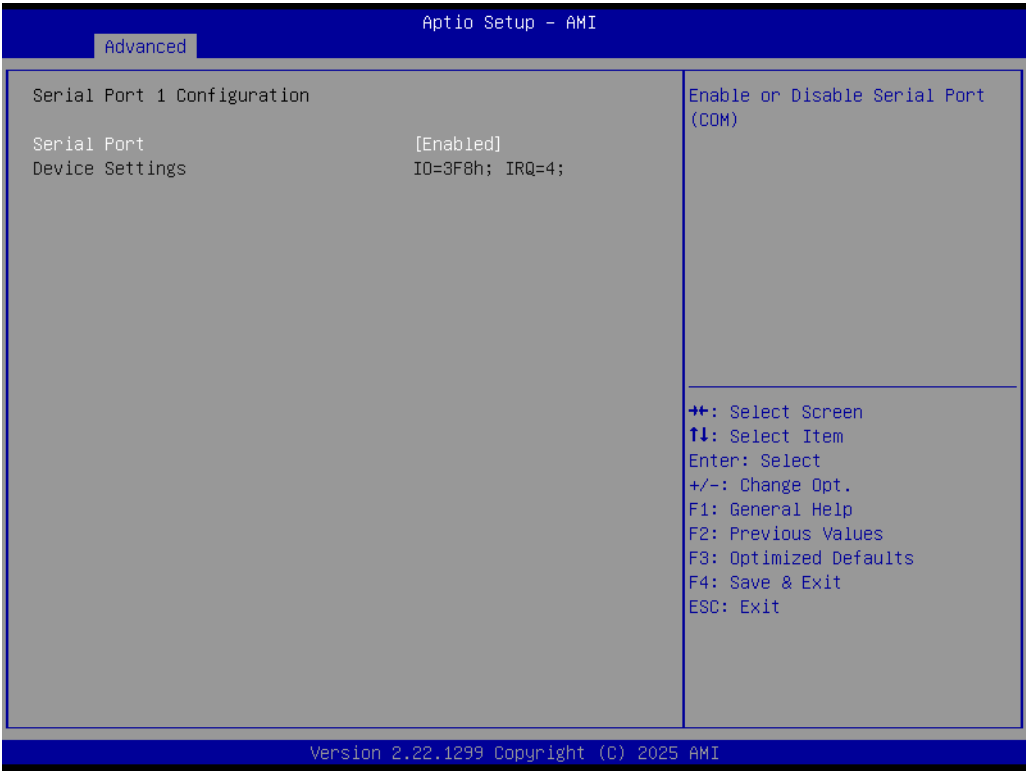
3.2.2.11 IT5782 Embedded Controller Configuration

Advanced → IT5782 Embedded Controller Configuration



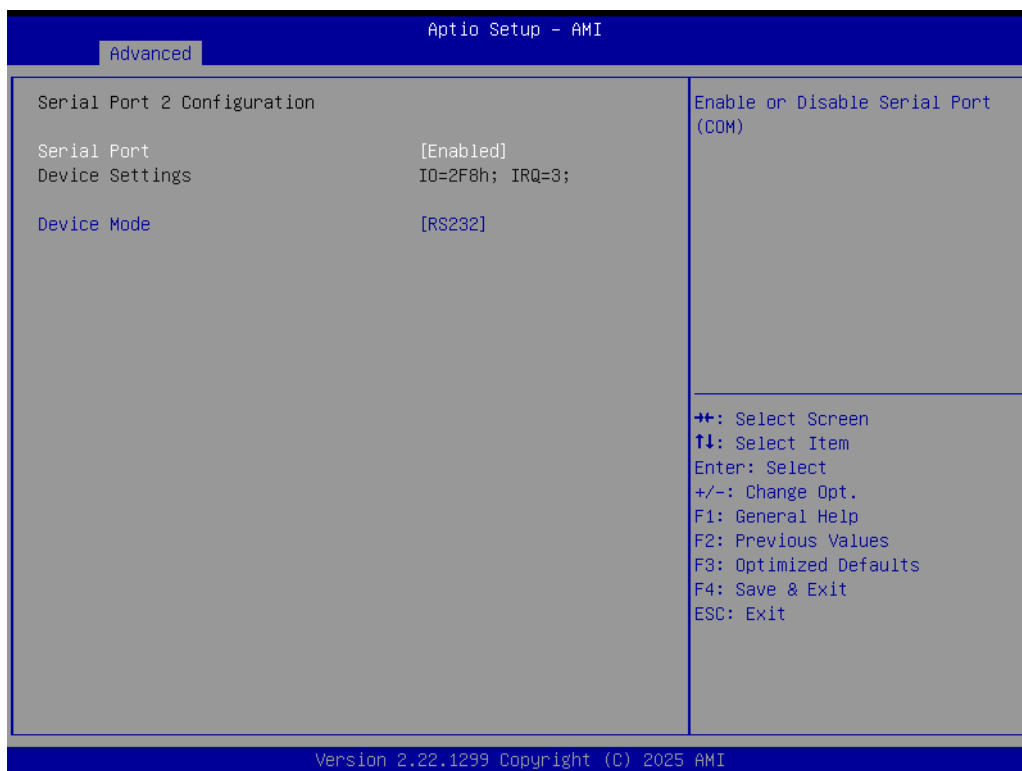
Serial Port 1 Configuration

Advanced → IT5782 Embedded Controller Configuration → Serial Port 1 Configuration



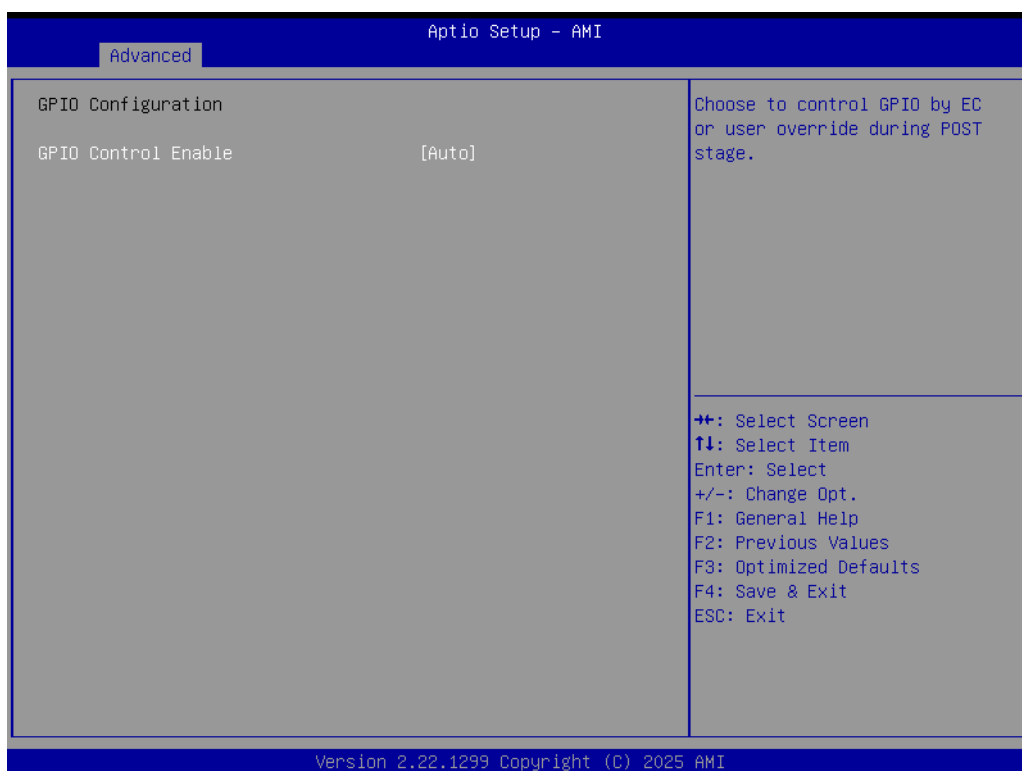
Serial Port 2 Configuration

Advanced → IT5782 Embedded Controller Configuration → Serial Port 2 Configuration

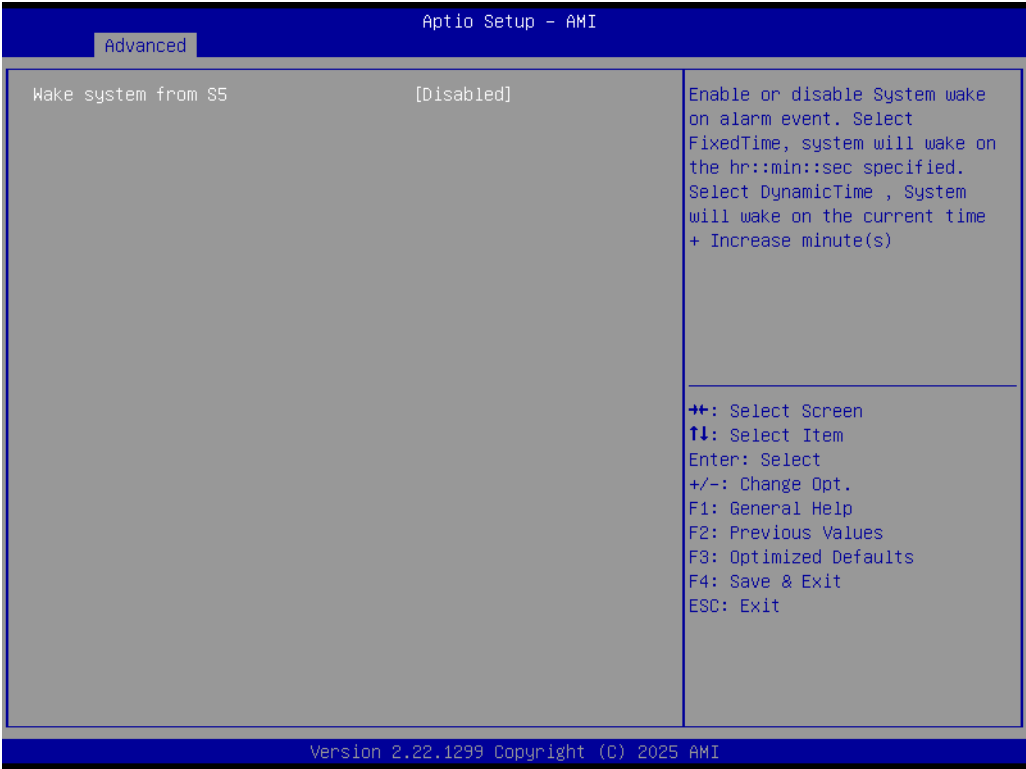


GPIO Configuration

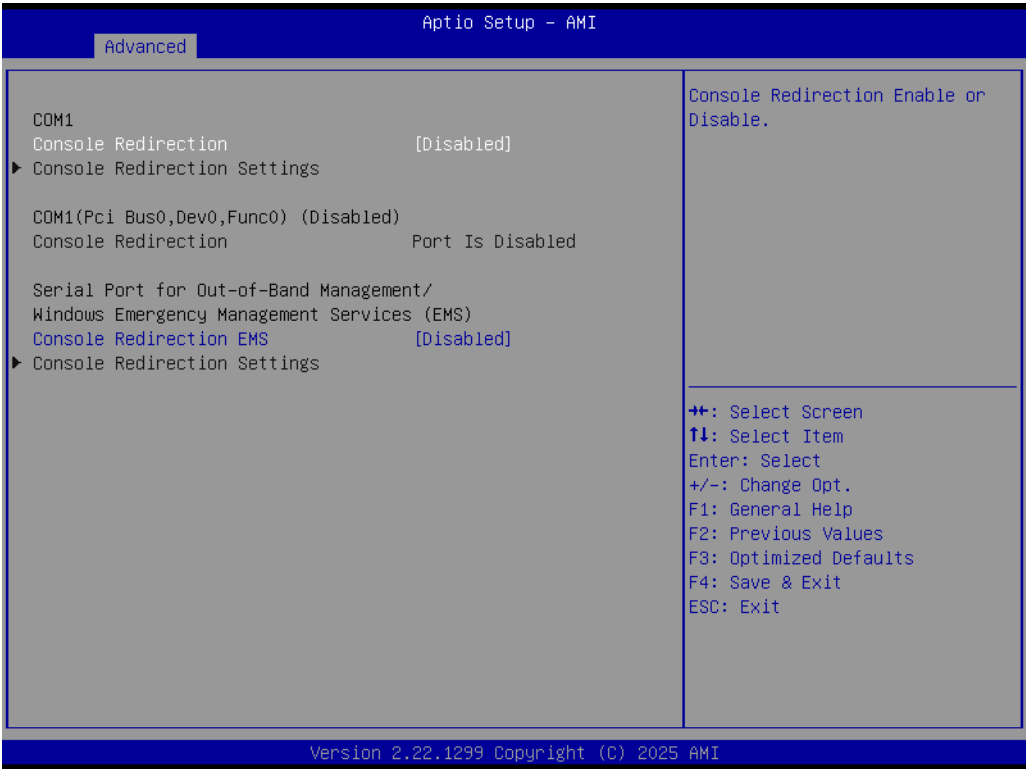
Advanced → IT5782 Embedded Controller Configuration → GPIO Configuration



3.2.2.12 S5 RTC Wake Settings
Advanced → S5 RTC Wake Settings

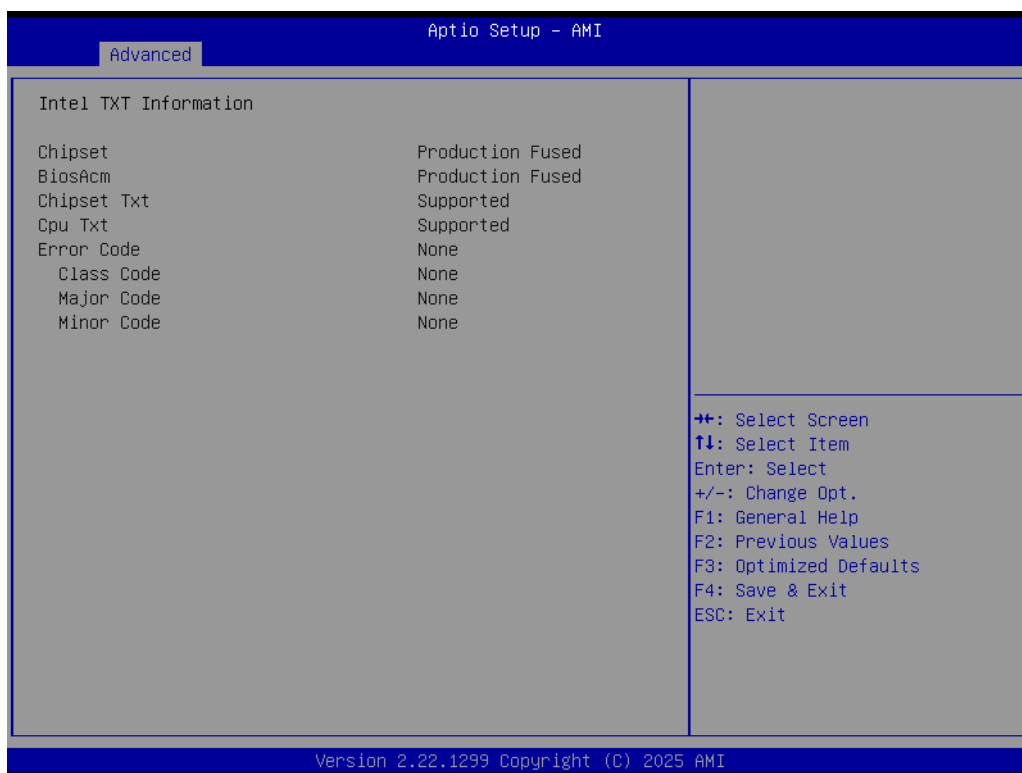


3.2.2.13 Serial Port Console Redirection
Advanced → Serial Port Console Redirection



3.2.2.14 Intel TXT Information

Advanced → Intel TXT Information

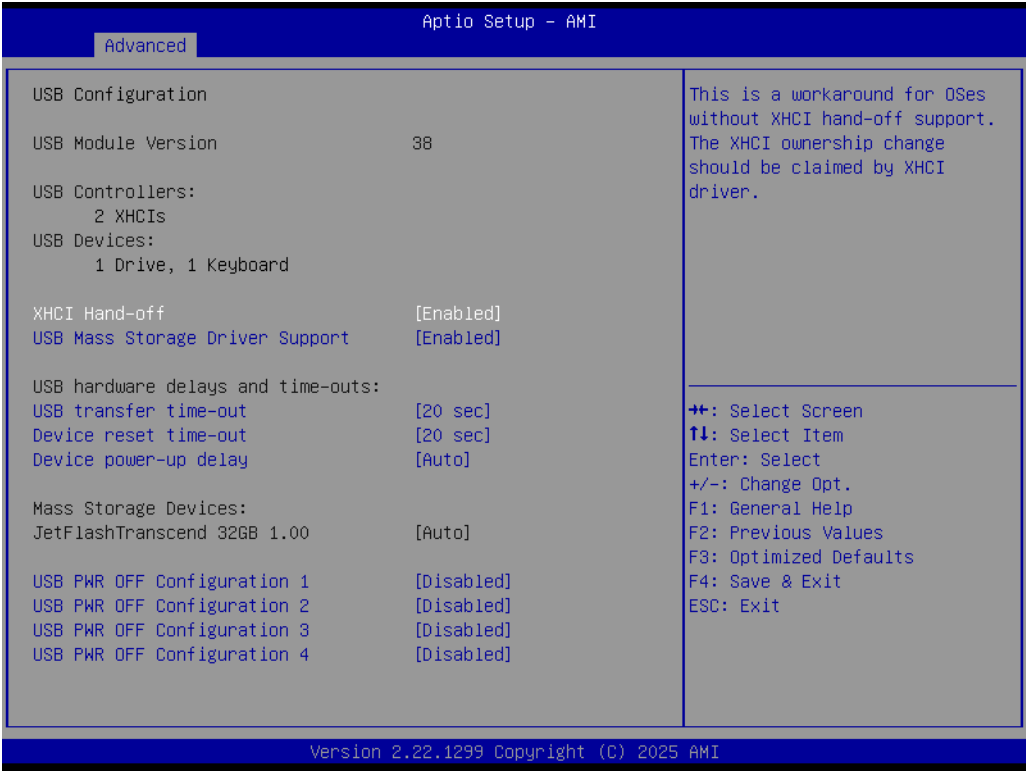


3.2.2.15 PCI Subsystem Settings

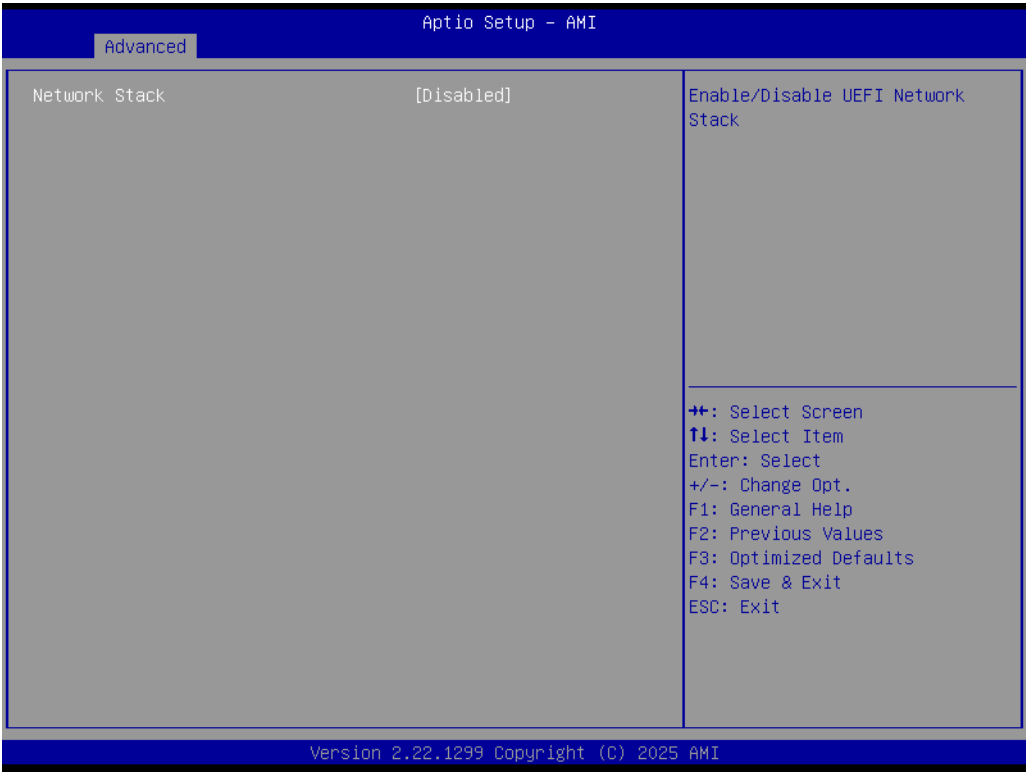
Advanced → PCI Subsystem settings



3.2.2.16 USB Configuration
Advanced → USB Configuration



3.2.2.17 Network Stack Configuration
Advanced → Network Stack Configuration



3.2.2.18 NVMe Configuration

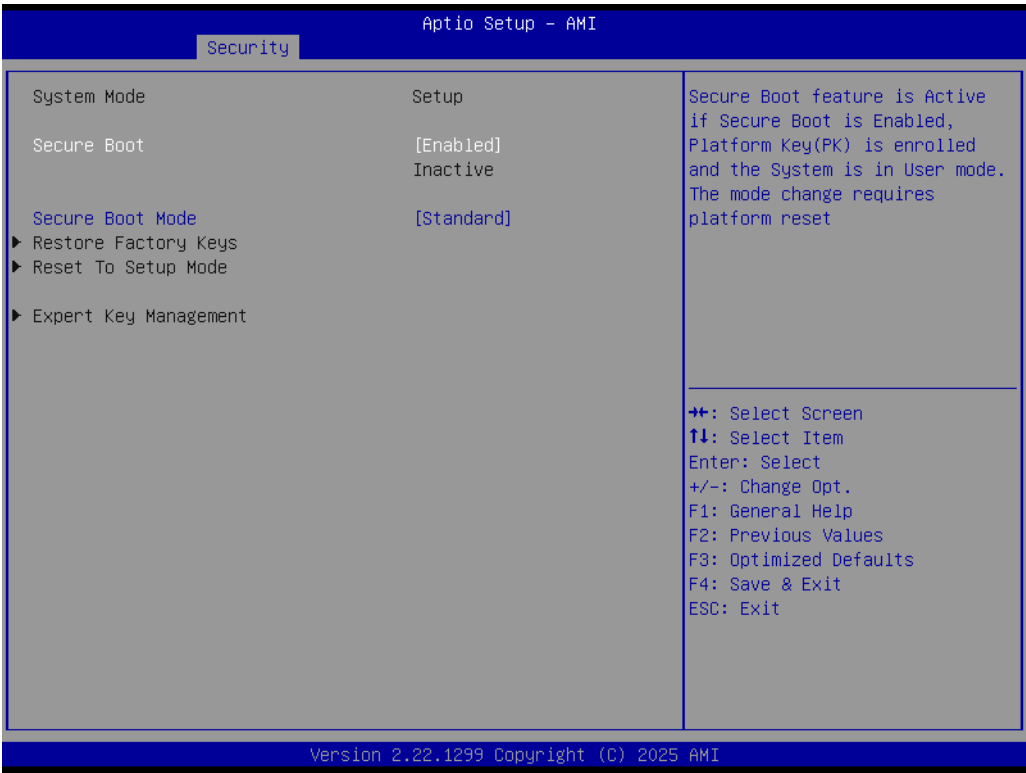
Advanced → NVMe Configuration



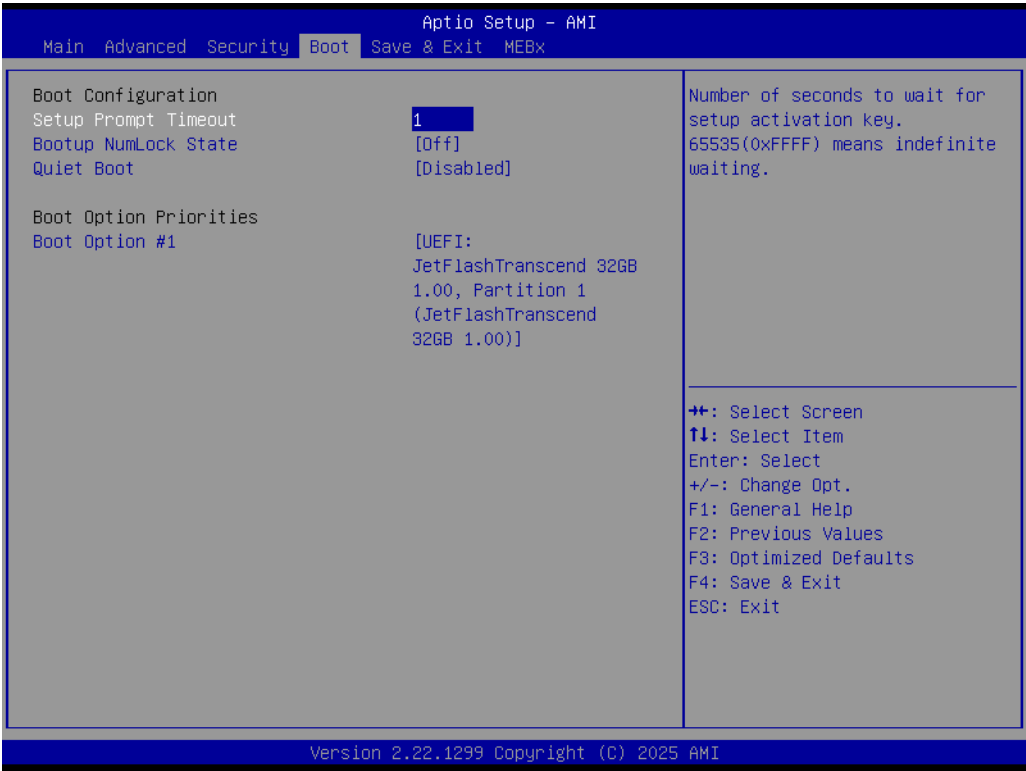
3.2.3 Security



Secure Boot
Security → Secure Boot



3.2.4 Boot Settings



3.2.5 Save & Exit Configuration



3.2.6 MEBx



Chapter 4

Software Introduction
& Service

4.1 Introduction

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft® Windows® embedded technology." We enable Windows® Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows® Embedded Software solutions easily and widely available to the embedded computing community.

4.2 Value-Added Software Services

Software API: An interface that defines the ways by which an application program may request services from libraries and/or operating systems. Provides not only the underlying drivers required but also a rich set of user-friendly, intelligent and integrated interfaces, which speeds development, enhances security and offers add-on value for Advantech platforms. It plays the role of catalyst between developer and solution, and makes Advantech embedded platforms easier and simpler to adopt and operate with customer applications.

4.2.1 Software API

4.2.1.1 Control

GPIO



General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch on/off the device. Our API also provides Programmable GPIO, which allows developers to dynamically set the GPIO input or output status.

SMBus



SMBus is the System Management Bus defined by Intel Corporation in 1995. It is used in personal computers and servers for low-speed system management communications. The SMBus API allows a developer to interface a embedded system environment and transfer serial messages using the SMBus protocols, allowing multiple simultaneous device control.

4.2.1.2 Display

Brightness Control



The Brightness Control API allows a developer to access embedded devices and easily control brightness.

Backlight



The Backlight API allows a developer to control the backlight (screen) on/off in embedded devices.

4.2.1.3 Monitor

Watchdog



A watchdog timer (WDT) is a device that performs a specific operation after a certain period of time if something goes wrong and the system does not recover on its own. A watchdog timer can be programmed to perform a warm boot (restarting the system) after a certain number of seconds.

Hardware Monitor



The Hardware Monitor (HWM) API is a system health supervision API that inspects certain condition indexes, such as fan speed, temperature and voltage.

4.2.1.4 Power Saving

CPU Speed



Makes use of Intel SpeedStep technology to save power consumption. The system will automatically adjust the CPU speed depending on the system loading.

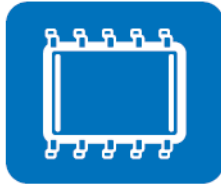
System Throttling



Refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. This API allows the user to adjust the clock from 87.5% to 12.5%.

4.2.2 Software Utility

BIOS Flash



The BIOS Flash utility allows customers to update the flash ROM BIOS version, or use it to back up current BIOS by copying it from the flash chip to a file on the customers' disk. The BIOS Flash utility also provides a command line version and an API for fast implementation into customized applications.

Embedded Security ID



The embedded application is the most important property of a system integrator. It contains valuable intellectual property, design knowledge and innovation, but this makes it vulnerable! Embedded Security ID utility provides reliable security functions for customers to secure their application data within the embedded BIOS.

Monitoring



Monitoring is a utility for customers to monitor system health, like voltage, CPU and system temperature and fan speed. These items are important to a device, if critical errors occur and are not solved immediately, permanent damage may be caused.

Chapter 5

Chipset Software
Installation Utility

5.1 Before You Begin

To facilitate the installation of the enhanced display drivers and utility software, read the instructions in this chapter carefully. The drivers for the AIMB-2710 are located on the Advantech support website: <http://support.advantech.com/Support/>. The drivers on the support website will guide and link you to the utilities and drivers under a Windows system. Updates are provided via Service Packs from Microsoft*.

Note!



The driver files on the website are compressed. Do not attempt to install the drivers by copying the files manually. You must download the files and decompress them first. Also, please use the supplied SETUP program to install the drivers.

Before you begin, it is important to note that most display drivers need to have the relevant software application already installed in the system prior to installing the enhanced display drivers. In addition, many of the installation procedures assume that you are familiar with both the relevant software applications and operating system commands. Review the relevant operating system commands and the pertinent sections of your application software's user manual before performing the installation.

5.2 Introduction

The Intel® Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured. This is needed for the proper functioning of the following features:

- Core PCI PnP services
- Serial ATA interface support
- USB support
- Identification of Intel® chipset components in the Device Manager

Note!



*This utility is used for the following versions of Windows, and it has to be installed **before** installing all the other drivers:*

- Windows 11 (64-bit)

Chapter 6

LAN Configuration

6.1 Introduction

The AIMB-2710 system features dual Gigabit Ethernet LANs via dedicated PCI-Express x1 lanes (Lan1: Intel I226-LM V-PRO 2.5 GbE and LAN2: Intel I226-V 2.5 GbE) that offer a bandwidth of up to 500 MB/sec, eliminating bottlenecks in the flow of network data by incorporating Gigabit Ethernet at 1000 Mbps.

6.2 Features

- Integrated 10/100/1000/2500 Mbps transceiver
- 10/100/1000/2500 Mbps triple-speed MAC
- High-speed RISC core with 24-KB cache
- On-chip voltage regulation
- Wake-on-LAN (WOL) support
- PCI Express X1 host interface

6.3 Installation

Note! *Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.*



The Intel I226-LM V-PRO (LAN1) and Intel I226-V (LAN2) Gigabit integrated controllers support all major network operating systems. However, the installation procedure varies between systems. Please follow the driver setup procedure instructions specific to the operating system installed.

6.4 Windows® 11 Driver Setup

Download the driver from support website on your computer and decompressed the file. Select the “Autorun” then navigate to the directory for your OS.

Note! *Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.*





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