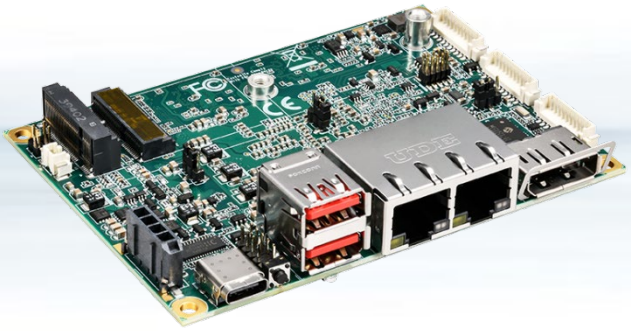
USER GUIDE



2.5"-SBC-AML/ADN

Doc. User Guide, Rev. 1.4

Doc. ID: [To be Determined]

kontron
The Power of IoT

www.kontron.com

This page has been intentionally left blank

2.5"-SBC-AML/ADN - USER GUIDE

Disclaimer

Kontron would like to point out that the information contained in this user guide may be subject to alteration, particularly as a result of the constant upgrading of Kontron products. This document does not entail any guarantee on the part of Kontron with respect to technical processes described in the user guide or any product characteristics set out in the user guide. Kontron assumes no responsibility or liability for the use of the described product(s), conveys no license or title under any patent, copyright or mask work rights to these products and makes no representations or warranties that these products are free from patent, copyright or mask work right infringement unless otherwise specified. Applications that are described in this user guide are for illustration purposes only. Kontron makes no representation or warranty that such application will be suitable for the specified use without further testing or modification. Kontron expressly informs the user that this user guide only contains a general description of processes and instructions which may not be applicable in every individual case. In cases of doubt, please contact Kontron.

Kontron Europe GmbH

Gutenbergstraße 2
85737 Ismaning
Germany
www.kontron.com

Intended Use

THIS DEVICE AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION OF NUCLEAR FACILITIES, THE NAVIGATION, CONTROL OR COMMUNICATION SYSTEMS FOR AIRCRAFT OR OTHER TRANSPORTATION, AIR TRAFFIC CONTROL, LIFE SUPPORT OR LIFE SUSTAINING APPLICATIONS, WEAPONS SYSTEMS, OR ANY OTHER APPLICATION IN A HAZARDOUS ENVIRONMENT, OR REQUIRING FAIL-SAFE PERFORMANCE, OR IN WHICH THE FAILURE OF PRODUCTS COULD LEAD DIRECTLY TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE (COLLECTIVELY, "HIGH RISK APPLICATIONS").

You understand and agree that your use of Kontron devices as a component in High Risk Applications is entirely at your risk. To minimize the risks associated with your products and applications, you should provide adequate design and operating safeguards. You are solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning your products. You are responsible to ensure that your systems (and any Kontron hardware or software components incorporated in your systems) meet all applicable requirements. Unless otherwise stated in the product documentation, the Kontron device is not provided with error-tolerance capabilities and cannot therefore be deemed as being engineered, manufactured or setup to be compliant for implementation or for resale as device in High Risk Applications. All application and safety related information in this document (including application descriptions, suggested safety measures, suggested Kontron products, and other materials) is provided for reference only.

Revision History

Revision	Brief Description of Changes	Date of Issue	Author/ Editor
1.0	Initial Issue	2025-Apr-18	YS
1.1	Add CE / FCC compliance standards	2025-Apr-30	YS
1.2	Update COM1 & COM2 pin definition	2025-May-28	YS
1.3	Add UR / CSA compliance standards	2025-Jun-10	YS
1.4	Modify power consumption	2025-Aug-14	YS

Terms and Conditions

Kontron warrants products in accordance with defined regional warranty periods. For more information about warranty compliance and conformity, and the warranty period in your region, visit https://www.kontron.com/terms-and-conditions.

Kontron sells products worldwide and declares regional General Terms & Conditions of Sale, and Purchase Order Terms & Conditions. Visit https://www.kontron.com/terms-and-conditions.

For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

Customer Support

Find Kontron contacts by visiting: https://www.kontron.com/support-and-services.

Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.

For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit https://www.kontron.com/support-and-services.

Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
NOTICE	NOTICE indicates a property damage message.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	Electric Shock! This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	ESD Sensitive Device! This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	HOT Surface! Do NOT touch! Allow to cool before servicing.
	Laser! This symbol informs of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠CAUTION

Danger of explosion if the battery is replaced incorrectly.

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit https://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with Kontron.

Kontron follows the WEEE directive

You are encouraged to return our products for proper disposal.

Table of Contents

List of Tables

List of Figures

1/ Introduction

This user guide describes the 2.5"-SBC-AML/ADN board made by Kontron. This board will also be denoted 2.5"-SBC-AML/ADN within this user guide.

Use of this user guide implies a basic knowledge of PC-AT hardware and software. This user guide focuses on describing the 2.5"-SBC-AML/ADN board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching on the power.

All configuration and setup of the CPU board is either carried out automatically or manually by the user via the BIOS setup menus.

Latest revision of this user guide, datasheet, thermal simulations, BIOS, drivers, BSP's (Board Support Packages), mechanical drawings (2D and 3D) can be downloaded from Kontron's Web Page.

2/ Installation Procedures

2.1. Installing the Board

NOTICE

ESD Sensitive Device!

Electrostatic discharge (ESD) can damage equipment and impair electrical circuitry.

- Wear ESD-protective clothing and shoes
- Wear an ESD-preventive wrist strap attached to a good earth ground
- Check the resistance value of the wrist strap periodically (1 MΩ to 10 MΩ)
- Transport and store the board in its antistatic bag
- Handle the board at an approved ESD workstation
- Handle the board only by the edges

To get the board running follow these steps. If the board shipped from KONTRON already has components like CPU cooler mounted, then skip the relevant steps below.

1. **Turn off the PSU (Power Supply Unit)**

NOTICE

Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected while configuring the board. Otherwise, components (RAM, LAN cards etc.) might get damaged. Make sure the DC single supply used is within the range between 9 V and 20 V with suitable cable kit and PS-ON# active.

NOTICE

The power supply unit shall comply with the requirements as defined in IEC 62368-1 according Clause 6.2.2 to power source category PS2 "Limited Power Source".

2. **Connecting interfaces**
   Insert all external cables for keyboard etc. A monitor must be connected in order to change BIOS settings.
3. **Connect and turn on PSU**
   Connect PSU to the board by the 3.0 mm pitch 1x4-pin wafer connector.
4. **BIOS setup**
   Enter the BIOS setup by pressing the <DEL> key during boot up.
   Enter "Exit Menu" and Load Setup Defaults.

To clear all BIOS setting, including Password protection, activate "Clear CMOS Jumper" for 10 sec (without power connected).

5. **Installing the thermal solution and mounting the board in chassis**

NOTICE

When installing the thermal solution on the board and mounting the board to chassis etc. please note that the board contains components on both sides of the PCB that can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the board on a chassis, it is recommended to use screws with an integrated washer and a diameter of > 7 mm. Do not use washers with teeth, as they can damage the PCB and cause short circuits.

2.2. Chassis Safety Standards

Before installing the 2.5"-SBC-AML/ADN in the chassis, users must evaluate the end product to ensure compliance with the requirements of the IEC60950-1 safety standard:

- The board must be installed in a suitable mechanical, electrical and fire enclosure.
- The system, in its enclosure, must be evaluated for temperature and airflow considerations.
- The board must be powered by a CSA or UL approved power supply that limits the maximum input current.
- For interfaces having a power pin such as external power or fan, ensure that the connectors and wires are suitably rated. All connections from and to the product shall be with SELV circuits only.
- Wires have suitable rating to withstand the maximum available power.
- The peripheral device enclosure fulfils the IEC60950-1 fire protecting requirements.

2.3. Lithium Battery Replacement

If replacing the lithium battery follow the replacement precautions stated in the notification below:

⚠CAUTION

Danger of explosion if the lithium battery is incorrectly replaced.

- Replace only with the same or equivalent type recommended by the manufacturer
- Dispose of used batteries according to the manufacturer's instructions

VORSICHT! Explosionsgefahr bei unsachgemäßem Austausch der Batterie.

- Ersatz nur durch denselben oder einen vom Hersteller empfohlenen gleichwertigen Typ
- Entsorgung gebrauchter Batterien nach Angaben des Herstellers

ATTENTION! Risque d'explosion avec l'échange inadéquat de la batterie.

- Remplacement seulement par le même ou un type équivalent recommandé par le producteur
- L'évacuation des batteries usagées conformément à des indications du fabricant

PRECAUCION! Peligro de explosión si la batería se sustituye incorrectamente.

- Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante
- Disponga las baterías usadas según las instrucciones del fabricante

ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering.

- Udskiftning må kun ske med batteri af samme fabrikat og type
- Levér det brugte batteri tilbage til leverandøren

ADVARSEL! Eksplosjonsfare ved feilaktig skifte av batteri.

- Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten
- Brukte batterier kasseres i henhold til fabrikantens instruksjoner

VARNING! Explosionsfara vid felaktigt batteribyte.

- Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren
- Kassera använt batteri enligt fabrikantens instruktion

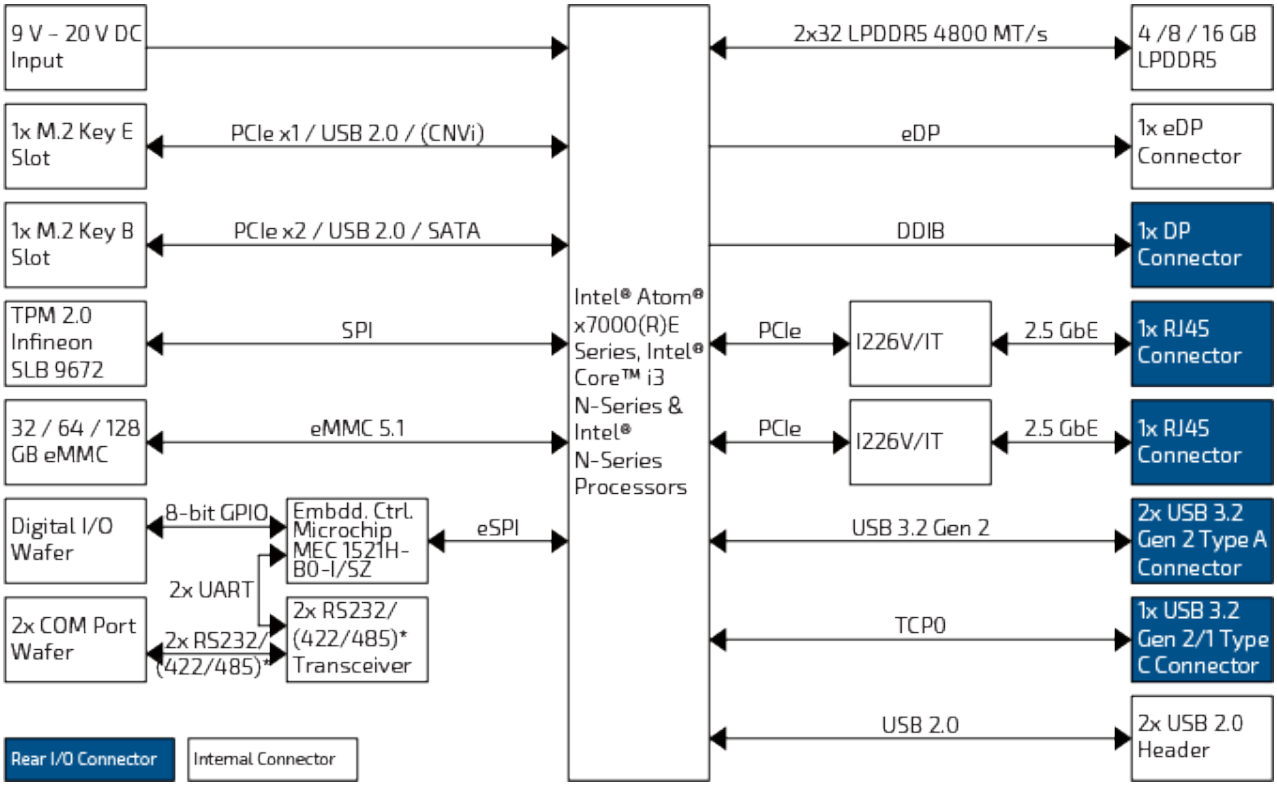
VAROITUS! Paristo voi räjähtää, jos se on virheellisesti asennettu.

- Vaihda paristo ainoastaan lalteval- mistajan suosittelemaan tyyppiln
- Hävitä käytetty paristo valmistajan ohjeiden mukaisesti

3/ System Specifications

3.1. System Block Diagram

Figure 1: System Block Diagram 2.5"-SBC-AML/ADN



(*: optional)

3.2. Component Main Data

The table below summarizes the features of the 2.5"-SBC-AML/ADN single board computer.

Table 1: Component Main Data

System	
Processor	▶ Intel® Atom® x7000RE Series Processors ▶ Intel® Atom® x7000E Series Processors ▶ Intel® Core™ i3 N-Series Processors ▶ Intel® N-Series Processors
Memory	▶ 4 GByte / 8 GByte / 16 GByte LPDDR5 4800 soldered memory
Video	
Display Interface	▶ 1x eDP (4096 x 2160 @ 60 Hz) ▶ 2x DP (4096 x 2160 @ 60 Hz, 1x Full-size DP on rear, 1x DP USB-C on rear)
Multiple Display	▶ Triple
Network Connection	
Ethernet	▶ 2x 2.5 GbE LAN (RJ45 on rear, Intel® I226-V/IT, with TSN for models with Atom® CPUs)
Peripheral Connection	
USB	▶ 2x USB 3.2 Gen 2 Type A (on rear) ▶ 1x USB 3.2 Gen 2 Type C (on rear, w/ DP & PD 5 V / 3 A, except Atom® x7000RE) ▶ 1x USB 3.2 Gen 1 Type C (on rear, w/ DP & PD 5 V / 3 A, only Atom® x7000RE) ▶ 2x USB 2.0 (by header)
Serial Port	▶ 2x RS232 (default) / RS232/422/485 (optional) (Tx/Rx only in RS232 signal, by header)
Other I/Os	▶ 4x DI (by wafer) ▶ 4x DO (by wafer)
Storage & Expansion	
eMMC	▶ 32 GByte / 64 GByte / 128 GByte eMMC
M.2	▶ 1x M.2 Key B (Type 2242 / 3042 / 3052 / 2280, w/ PCIe x2 / USB 2.0 / SATA / UIM) ▶ 1x M.2 Key E (Type 2230, w/ PCIe x1 / USB 2.0 / CNVi (Atom® x7000RE does not support CNVi))
SIM Card Holder	▶ 1x SIM Card Holder (by wafer)
Power	
Input Voltage	▶ DC 9 V ~ 20 V
Connector	▶ 1x4-pin pitch 3.0 mm Wafer
Firmware	
BIOS	▶ AMI uEFI BIOS w/ 256 Mb SPI Flash
Watchdog	▶ Programmable WDT to generate system reset event
H/W Monitor	▶ Voltages ▶ Temperatures
Real Time Clock	▶ Processor integrated RTC

System	
Security	▶ TPM 2.0 (Infineon SLB 9672)
System Control & Monitoring	
Button, Switch & Indicator	▶ 1x Power Button (on rear) ▶ 1x Power LED (Green, on rear)
Front Panel Header	▶ 1x Header for Power Button, Reset Button, Power LED & SATA LED
Cooling	
Cooling Method	▶ Passive
Software	
OS Support	▶ Windows 11 ▶ Windows 10 ▶ Linux
Mechanical	
Dimension (L x W)	▶ Pico-ITX (100 mm x 72 mm / 3.94" x 2.83")

3.3. Environmental Conditions

The 2.5"-SBC-AML/ADN is compliant with the following environmental conditions. It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within the allowed temperature range.

Table 2: Environmental Conditions

Operating Temperature	▶ 0 °C ~ 60 °C / 32 °F ~ 140 °F (Standard) ▶ -40 °C ~ 85 °C / -40 °F ~ 185 °F (Extreme)
Storage Temperature	▶ -20 °C ~ 80 °C / -4 °F ~ 176 °F (Standard) ▶ -55 °C ~ 85 °C / -67 °F ~ 185 °F (Extreme)
Humidity	▶ 0 % ~ 95 %

3.4. Standards and Certifications

The 2.5"-SBC-AML/ADN meets the following standards and certification tests.

Table 3: Standards and Certifications

CE Class B **UKCA**	▶ EN 55032: 2015 + A11: 2020, Class B ▶ BS EN 55032: 2015 + A11: 2020 ▶ CISPR 32: 2015 + COR1: 2016 ▶ EN 55032: 2015 + A1: 2020, Class B ▶ BS EN 55032: 2015 + A1: 2020 ▶ CISPR 32: 2015 + A1: 2019 ▶ EN 61000-3-2: 2014 ▶ EN IEC 61000-3-2: 2019 + A1: 2021 ▶ EN 61000-3-3: 2013 + A2: 2021 ▶ BS EN 61000-3-2:2014

	▶ BS EN IEC 61000-3-2: 2019 + A1: 2021 ▶ BS EN 61000-3-3: 2013 + A2: 2021 ▶ EN 55035: 2017 + A11: 2020 ▶ BS EN 55035: 2017 + A11: 2020 ▶ IEC 61000-4-2: 2008 ▶ IEC 61000-4-3: 2020 ▶ IEC 61000-4-4: 2012 ▶ IEC 61000-4-5: 2014 + A1: 2017 ▶ IEC 61000-4-6: 2023 ▶ IEC 61000-4-8: 2009 ▶ IEC 61000-4-11: 2020 + COR2: 2022 ▶ EN IEC 61000-6-2: 2019 ▶ EN IEC 61000-6-4: 2019
FCC Class B **ICES Class B**	▶ FCC CFR Title 47 Part 15 Subpart B, Class B ▶ ICES-003 Issue 7: 2020 Class B ▶ ANSI C63.4: 2014 ▶ ANSI C63.4a: 2017
UR (UL Recognized) **CSA**	▶ UL 62368-1, 3rd Ed. ▶ CSA C22.2 No. 62368-1:19, 3rd Ed.

3.5. Processor Support

The 2.5"-SBC-AML/ADN is designed to support Intel® Atom® x7000RE Series, Intel® Atom® x7000E Series, Intel® Core™ i3 N-Series and Intel® N-Series Processors. The BGA CPU is remounted from factory. Kontron has defined the CPU SKUs as listed in the following table for either standard or project-based board versions, so far all based on Embedded CPUs. Other CPU SKUs are expected at a later date.

Table 4: Processor Support

Name	Core #	Speed (GHz)	Turbo (GHz)	Embedd.	Cache	Socket	TDP (W)	TDP-down (W)	Tj (°C)
Intel® Atom® x7211RE	2	1.0	3.2	Yes	6M	FCBGA1264	6	-	105
Intel® Atom® x7213RE	2	2.0	3.4	Yes	6M	FCBGA1264	9	-	105
Intel® Atom® x7433RE	4	1.5	3.4	Yes	6M	FCBGA1264	9	-	105
Intel® Atom® x7835RE	8	1.3	3.6	Yes	6M	FCBGA1264	12	-	105
Intel® Atom® x7211E	2	1.0	3.2	Yes	6M	FCBGA1264	6	-	105
Intel® Atom® x7213E	2	1.7	3.2	Yes	6M	FCBGA1264	10	-	105
Intel® Atom® x7425E	4	1.5	3.4	Yes	6M	FCBGA1264	12	-	105
Intel® Core™ i3-N305	8	1.8	3.8	Yes	6M	FCBGA1264	15	9	105
Intel® N50	2	1.0	3.4	Yes	6M	FCBGA1264	6	-	105
Intel® N97	4	2.0	3.6	Yes	6M	FCBGA1264	12	-	105
Intel® N200	4	1.0	3.7	Yes	6M	FCBGA1264	6	-	105

Sufficient cooling must be applied to the CPU in order to remove the effect as listed as TDP (Thermal Design Power) in above table. The sufficient cooling is also depending on the worst case maximum ambient operating temperature and the actual worst case load of processor.

3.6. System Memory Support

The 2.5"-SBC-AML/ADN supports two LPDDR5 memory chips soldered from factory with following features:

- 2x LPDDR5 memory down
- Maximum memory speed of 4800 MHz
- Single channel
- Memory size option: 4 GB / 8 GB / 16 GB
- SPD timing supported
- In-band ECC supported

The soldered LPDDR5 memory supports the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance.

3.6.1. Memory Operating Frequencies

In all modes, the frequency of system memory is the lowest frequency of the memory chip soldered in the system. The memory chip's frequency can be determined through the SPD register on the memory chip.

The table below lists the resulting operating memory frequencies based on the combination of memory and processor.

Table 5: Memory Operating Frequencies

LPDDR Type	Module Name	Memory Data Transfer (MT/s)	Processor System Bus Frequency (MHz)	Resulting Memory Clock Frequency (MHz)	Peak Transfer Rate (MB/s)
LPDDR5 4800	PC5-38400	4800	2400	300	38400

3.7. On-board Graphics Subsystem

The 2.5"-SBC-AML/ADN supports Intel® UHD Graphics Gen12 technology for high quality graphics capabilities. All 2.5"-SBC-AML/ADN versions support triple displays pipes.

Triple displays can be used simultaneously and be used to implement independent or cloned display configuration.

The 2.5"-SBC-AML/ADN itself provides one internal eDP interface, one external full-szie DisplayPort connectors and one external DisplayPort over USB Type C connector.

Table 6: Triple-displays Configurations

Display 1	Display 2	Display 3	Max. Resolution (Px) at 60 Hz		
			Display 1	Display 2	Display 3
eDP	DP	DP USB-C	4096 x 2160	4096 x 2160	4096 x 2160

3.8. Power Input Voltage

In order to ensure safe operation of the board, the input power must monitor the input voltage and shut down if the voltage is out of range – refer to the actual input power specification. Please note, in order to keep the power consumption to a minimal level, boards do not implement a guaranteed minimum load. The 2.5"-SBC-AML/ADN board must be powered by a single DC input power within the range between 9 V and 20 V applied through the 3.0 mm pitch 1x4-pin wafer connector CN6 (see Chapter 7.1.1).

NOTICE

Hot Plugging power supply is not supported. Hot plugging might damage the board.

The voltages at the power input connector are required as follows:

Table 7: Power Input Voltages

Power Input	Min.	Max.	Note
9 V ~ 20 V	8.55 V	21 V	Should be ±5 %

3.9. Power Consumption

The power consumption is measured under the following software and hardware test condition.

- 2.5"-SBC-AML/ADN with Intel® Core™ i3-N305 (Octa Core @ 3.8 GHz) and Intel® Atom® x7835RE processor (Octa Core @ 3.6 GHz)

- Memory: 2x 4 GByte Micron LPDDR5 4800 SDRAM (Intel® Core™ i3-N305) / 2x 8 GByte Micron LPDDR5 4800 SDRAM (Intel® Atom® x7835RE)
- Storage: 128 GByte Micron eMMC + 128 GByte Transcend M.2 SATA SSD
- Operating System: Windows 11 IoT LTSC 24H2

The power consumption in different modes is as follows:

Table 8: Power Consumption

Power Status	Input Voltage	Power Consumption	
		Intel® Core™ i3-N305	Intel® Atom® x7835RE
Boot (Peak)	+19 V	52.25 W	51.11 W
	+9 V	41.04 W	42.21 W
Idle (S0)	+19 V	10.89 W	10.65 W
	+9 V	9.80 W	9.81 W
Full Run (S0)	+19 V	21.24 W	18.51 W
	+9 V	20.79 W	18.09 W
Sleep (S3)	+19 V	2.99 W	2.89 W
	+9 V	2.76 W	2.77 W
Shutdown (S4 / S5)	+19 V	3.06 W	3.06 W
	+9 V	2.83 W	2.72 W
Shutdown (PSM)	+19 V	559.55 mW	617.12 mW
	+9 V	313.84 mW	279.36 mW

4/ Connector Locations

4.1. Top Side

Figure 2: Top Side

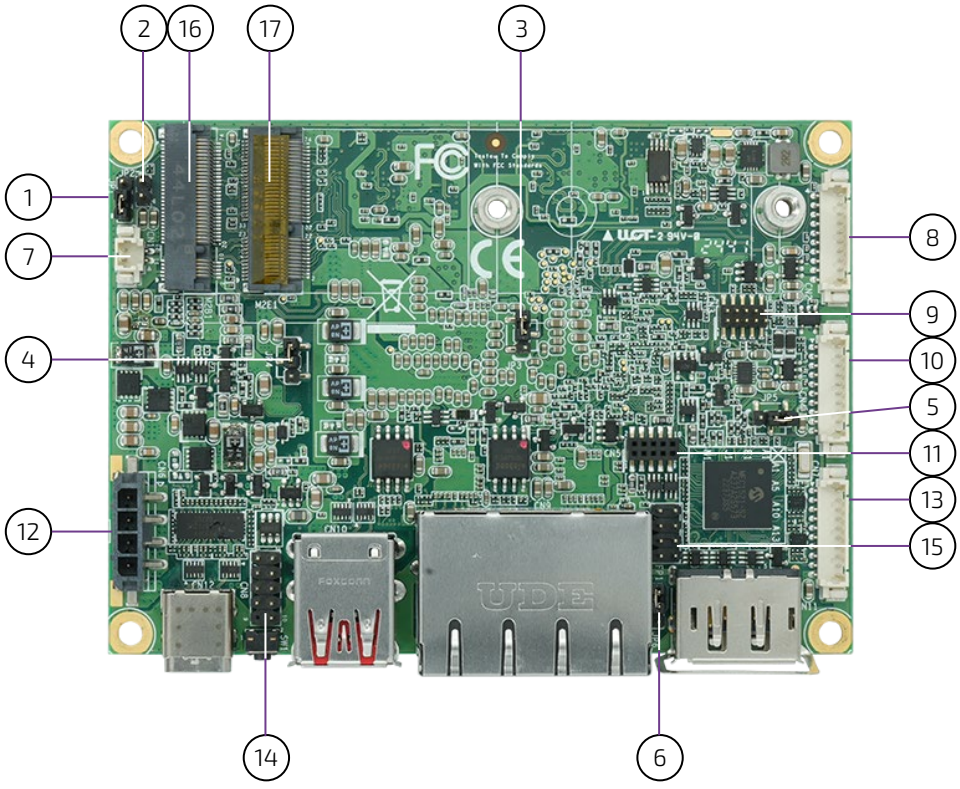


Table 9: Jumper List

Item	Designation	Description	See Chapter
1	JP1	Flash Descriptor Security Override Selection	7.11.1
2	JP2	Clear CMOS Selection	7.11.2
3	JP3	M.2 Key B Selection	7.11.3
4	JP4	USB Power Selection	7.11.4
5	JP5	eDP Panel Power Selection	7.11.5
6	JP6	AT / ATX Power Mode Selection	7.11.6

Table 10: Top Side Internal Connector Pin Assignment

Item	Designation	Description	See Chapter
7	CN1	RTC Power Input Wafer	7.1.2
8	CN2	RS232(/422/485) COM1 Wafer	7.4
9	CN3	SPI 10-Pins Header	7.7
10	CN4	RS232(/422/485) COM2 Wafer	7.4
11	CN5	P80 Holder	-
12	CN6	DC Power Input Wafer	7.1.1
13	CN7	DIO Wafer	7.6
14	CN8	USB 2.0 Port 3 & 4 Header	7.2
15	FP1	Front Panel Header 1	7.3
16	M2B1	M.2 Key B 2242 / 3042 / 3052 / 2280 Slot	7.8
17	M2E1	M.2 Key E 2230 Slot	7.9

4.2. Rear Side

Figure 3: Rear Side

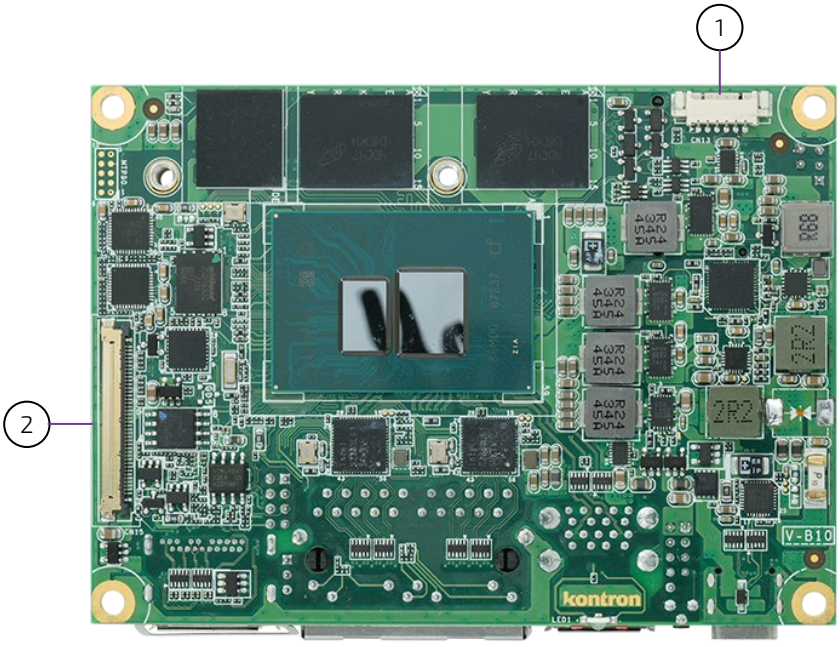


Table 11: Rear Side Internal Connector Pin Assignment

Item	Designation	Description	See Chapter
1	CN13	SIM Card Wafer for M2B1	7.10
2	CN15	eDP Connector	7.5

4.3. Connector Panel Side

Figure 4: Connector Panel Side

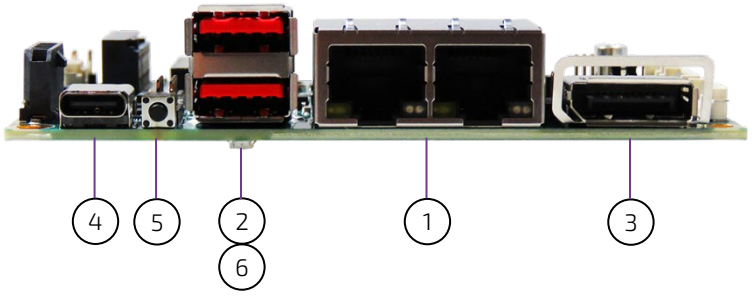


Table 12: Connector Panel Side Connector List

Item	Designation	Description	See Chapter
1	CN9	2.5 GbE LAN1 & LAN2 RJ45 Connector	6.1
2	CN10	USB 3.2 Gen 2 Port 1, 2 Type A Connector	6.4
3	CN11	DP Port 1 Connector	6.2
4	CN12	DP over USB 3.2 Gen 2 / Gen 1 Type C Connector	6.3
5	SW1	Power Button	6.5
6	LED1	Power LED	6.6

5/ Connector Definitions

The following defined terms are used within this user guide to give more information concerning the pin assignment and to describe the connector's signals.

Defined Term	Description
Pin	Shows the pin numbers in the connector
Signal	The abbreviated name of the signal at the current pin The notation "XX#" states that the signal "XX" is active low
Note	Special remarks concerning the signal
Designation	Type and number of item described
See Chapter	Number of the chapter within this user guide containing a detailed description

The abbreviation TBD is used for specifications that are not available yet or which are not sufficiently specified by the component vendors.

6/ I/O-Area Connectors

6.1. Ethernet Connectors (CN9)

The 2.5"-SBC-AML/ADN supports two channels of 10/100/1000/2500 Mbit Ethernet, which are based Intel® I226-V/IT controllers.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100 MByte and Category 5E, 6 or 6E with 1 Gbit/2.5 Gbit LAN networks.

The signals for the Ethernet ports are as follows:

Figure 5: Ethernet Connector CN9 – A (Left) & B (Right)

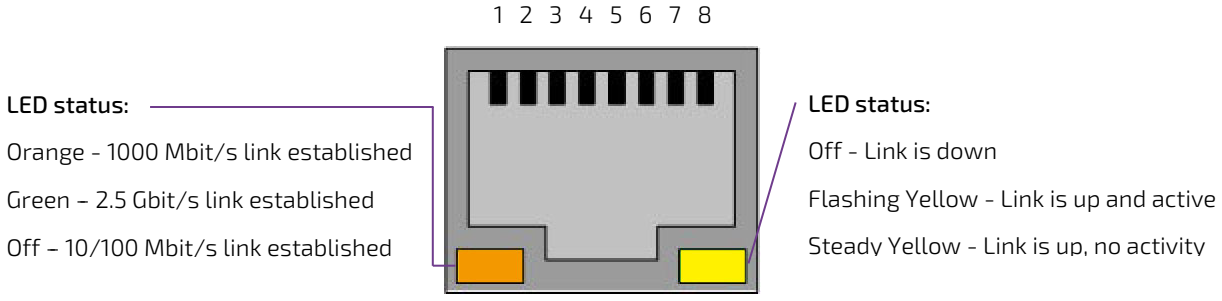


Table 13: Pin Assignment Ethernet Connectors CN9 – A (Left) & B (Right)

Pin	Signal	Note
1	BI_D1+	
2	BI_D1-	
3	BI_D2+	
4	BI_D3+	
5	BI_D3-	
6	BI_D2-	
7	BI_D4+	
8	BI_D4-	

Signal Description

Signal	Description
BI_D1+ / BI_D1-	In MDI mode, this is the first pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
BI_D2+ / BI_D2-	In MDI mode, this is the second pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
BI_D3+ / BI_D3-	In MDI mode, this is the third pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
BI_D4+ / BI_D4-	In MDI mode, this is the fourth pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DD+/- pair.In MDI crossover mode, this pair acts as the BI_DC+/- pair.

'MDI' – media dependent Interface

6.2. DP Connector (CN11)

The DP (DisplayPort) connectors are based on standard DP female port.

Figure 6: DP Connector CN11

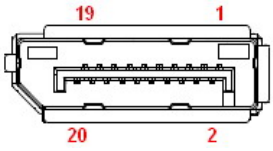


Table 14: Pin Assignment DP Connector CN11

Pin	Signal	Description	Note
1	ML_Lane0p	DisplayPort Lane 0 transmitter differential pair (+)	
2	GND	Ground	
3	ML_Lane0n	DisplayPort Lane 0 transmitter differential pair (-)	
4	ML_Lane1p	DisplayPort Lane 1 transmitter differential pair (+)	
5	GND	Ground	
6	ML_Lane1n	DisplayPort Lane 1 transmitter differential pair (-)	
7	ML_Lane2p	DisplayPort Lane 2 transmitter differential pair (+)	
8	GND	Ground	
9	ML_Lane2n	DisplayPort Lane 2 transmitter differential pair (-)	
10	ML_Lane3p	DisplayPort Lane 3 transmitter differential pair (+)	
11	GND	Ground	
12	ML_Lane3n	DisplayPort Lane 3 transmitter differential pair (-)	
13	Config1	Connected to ground, either directly or through a pulldown device	
14	Config2	Connected to ground, either directly or through a pulldown device	
15	AUX_CHp	DisplayPort Auxiliary channel differential pair (+)	
16	GND	Ground	
17	AUX_CHn	DisplayPort Auxiliary channel differential pair (-)	
18	Hot_Plug	DisplayPort hot plug detect	
19	GND	Ground	
20	DP_PWR	Power for connector	

6.3. DP over USB Type C Connector (CN12)

The DP (DisplayPort) over USB Type C connector supports DisplayPort Alternate Mode, USB 3.2 Gen 2 (variants with Intel® Atom® x7000E Series, Intel® Core™ i3 N-Series & Intel® N-Series processors) / Gen 1 (variants with Intel® Atom® x7000RE Series processors) and power delivery of up to 15 W (5 V at 3 A).

Figure 7: DP over USB Type C Connector CN12

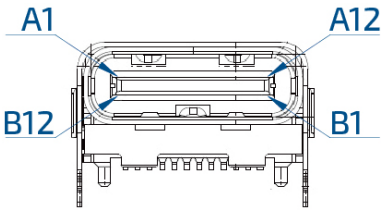


Table 15: Pin Assignment DP over USB Type C Connector CN12

Pin	Signal	Description	Note
A1	GND	Ground	
A2	CON_TX1P_C	USB 3.2 Tx differential pair (+) / DP Lane 2 Tx differential pair (+)	
A3	CON_TX1N_C	USB 3.2 Tx differential pair (-) / DP Lane 2 Tx differential pair (-)	
A4	+5V_VBUS*	+5 V bus power	
A5	CC1	Configuration channel signal 1	
A6	USB2_P	USB 2.0 differential pair (+), position 1	
A7	USB2_N	USB 2.0 differential pair (-), position 2	
A8	SBU1	Sideband use signal 1: DP Auxiliary channel differential pair (+)	
A9	+5V_VBUS*	+5 V bus power	
A10	CON_RX2N_C	DP Lane 0 Tx differential pair (-)	
A11	CON_RX2P_C	DP Lane 0 Tx differential pair (+)	
A12	GND	Ground	
B1	GND	Ground	
B2	CON_TX2P_C	DP Lane 1 Tx differential pair (+)	
B3	CON_TX2N_C	DP Lane 1 Tx differential pair (-)	
B4	+5V_VBUS*	+5 V bus power	
B5	CC2	Configuration channel signal 2	
B6	USB2_P	USB 2.0 differential pair (+), position 2	
B7	USB2_N	USB 2.0 differential pair (-), position 2	
B8	SUB2	Sideband use signal 2: DP Auxiliary channel differential pair (-)	
B9	+5V_VBUS*	+5 V bus power	
B10	CON_RX1N_C	USB 3.2 Rx differential pair (-) / DP Lane 3 Tx differential pair (-)	
B11	CON_RX1P_C	USB 3.2 Rx differential pair (+) / DP Lane 3 Tx differential pair (+)	
B12	GND	Ground	

* The power source of VBUX can be selected through JP4.

6.4. USB Connectors (I/O Area)

The external I/O connector panel supports one dual USB 3.2 Gen 2 connector (CN10).

USB 3.2 Gen 2 ports are backward compatible with USB 3.2 Gen 1 and USB 2.0.

Figure 8: USB 3.2 Gen 2 Connectors CN10 – Top & Bottom

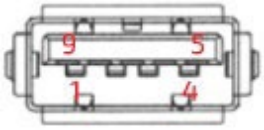


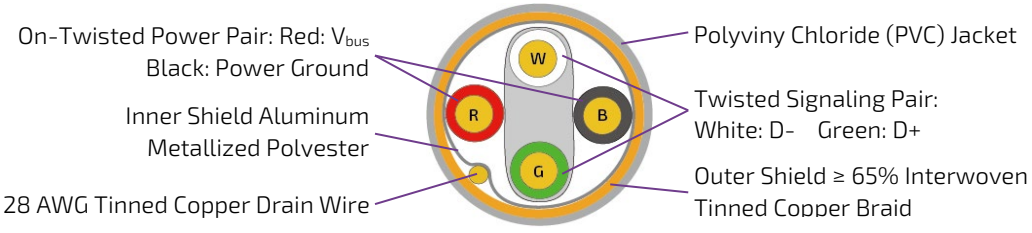
Table 16: Pin Assignment USB 3.2 Gen 2 Connectors CN10 – Top & Bottom

Pin	Signal	Description	Note
1	+USB_VCC*	+5 V power supply for USB device	
2	USB_D-	USB 2.0 differential pair (-)	
3	USB_D+	USB 2.0 differential pair (+)	
4	GND	Ground	
5	USB_RX-	USB 3.2 receiver differential pair (-)	
6	USB_RX+	USB 3.2 receiver differential pair (+)	
7	GND	Ground	
8	USB_TX-	USB 3.2 transmitter differential pair (-)	
9	USB_TX+	USB 3.2 transmitter differential pair (+)	

*** The power source of +USB_VCC can be selected through JP4.**

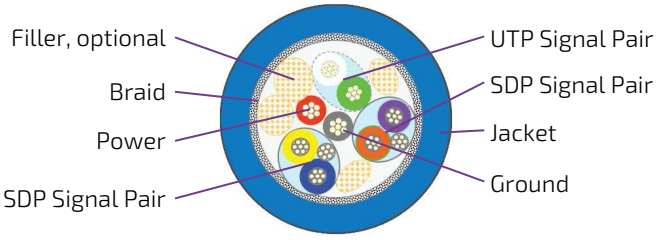
For HiSpeed rates it is required to use a USB cable, which is specified in USB 2.0 standard:

Figure 9: USB 2.0 High Speed Cable



For USB 3.2 cabling it is required to use only HiSpeed USB cable, specified in USB 3.2 standard:

Figure 10: USB 3.2 High Speed Cable



6.5. Power Button (SW1)

The external I/O connector panel supports a power button (SW1) for turning on and off the board.

6.6. LED Indicator (LED1)

The external I/O connector panel supports one power LED indicator (LED1) for power status indication.

Table 17: LED Indicator LED1

Power LED (LED1) Status	Description
Green LED On	S0 (Full On)
Green LED Blink	S3 (Suspend-To-RAM)
LED Off	S4 (Suspend-To-Disk), S5 (Soft Off) or EUP Mode or G3 (Mechanical Off)

7/ Internal Connectors

7.1. Power Connector

Power connector must be used to supply the board with a single DC power within the range between 9 V and 20 V (±5 %).

NOTICE

Hot plugging any of the power connector is not allowed.

Hot plugging might damage the board. In other words, turn off main supply etc. to make sure all the power lines are turned off when connecting to the motherboard.

7.1.1. Power Input Wafer (CN6)

The 1x4-pin 3.0 mm pitch power input wafer CN6 provides a single DC power within the range between 9 V and 20 V to the board.

Figure 11: Power Input Wafer CN6

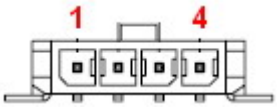


Table 18: Pin Assignment CN6

Pin	Signal	Description	Note
1	+Vin	Power input	
2	GND	Ground	
3	GND	Ground	
4	+Vin	Power input	
Connector Type			
B2W, 1x4-pin, 3.0 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	733-75-M104B6		
Terminal Model No.	733-70-FT0006		

7.1.2. RTC Power Input Wafer (CN1)

The 1x2-pin 1.25 mm pitch RTC power input wafer CN1 is intended to be connected to the battery. The battery provides power to the system clock to retain the time when power is turn off.

Figure 12: RTC Power Input Wafer CN1

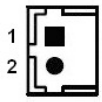


Table 19: Pin Assignment CN1

Pin	Signal	Description	Note
1	+VRTC	Real-time clock backup battery input	
2	GND	Ground	
Connector Type			
B2W, 1x2-pin, 1.25 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	712-75-02W001		
Terminal Model No.	712-70-T00001		

7.2. USB Connectors (Internal) (CN8)

The 10-pin 2.0 mm pitch USB port pin header CN8 supports two USB 2.0 ports.

Figure 13: USB 2.0 Port 3, 4 Pin Header CN8

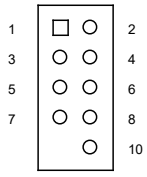


Table 20: Pin Assignment CN8

Pin	Signal	Description	Note
1	+USBVCC*	5 V supply. SB5V is supplied during power down to allow wakeup.	1 A max.
2	+USBVCC*	5 V supply. SB5V is supplied during power down to allow wakeup.	1 A max.
3	USB_DA-	USB 2.0 differential pair (-) for channel A	
4	USB_DB-	USB 2.0 differential pair (-) for channel B	
5	USB_DA+	USB 2.0 differential pair (+) for channel A	
6	USB_DB+	USB 2.0 differential pair (+) for channel B	
7	GND	Ground	
8	GND	Ground	
9	KEY		
10	GND	Ground	
Connector Type			
B2W, 2x5-pin, 2.0 mm pitch			
Mating Connector			
Vendor	Dupont		
Housing Model No.	WL2004H-2*5P(DP2.0)		
Terminal Model No.	KB931-21T1A		

* **The power source of +USBVCC can be selected through JP4.**

7.3. Front Panel Header (FP1)

The 8-pin 2.0 mm pitch front panel header FP1 supplies signals for the power button, reset button, M.2 Key B SSD LED and power LED.

Figure 14: Front Panel Header 1 FP1

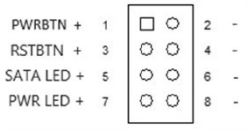


Table 21: Pin Assignment FP1

Pin	Signal	Description	Note
1	PWRBTN +	System power button (+)	
2	PWRBTN -	System power button (-)	
3	RSTBTN +	System reset button (+)	
4	RSTBTN -	System reset button (-)	
5	SATA_LED +	M.2 Key B SATA SSD activity LED (+). The LED lights up or flashes when data is ready from or written to the SSD.	
6	SATA_LED -	M.2 Key B SATA SSD activity LED (-).	
7	PWR_LED +	System Power LED (+). The LED lights up when users turn on the system power, and blinks when the system is in sleep mode.	
8	PWR_LED -	System Power LED (-)	
Connector Type			
B2W, 2x4-pin, 2.0 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	720-75-204B03		
Terminal Model No.	720-70-G00013		

7.4. Serial COM1 & COM2 Ports (CN2 & CN4)

The 10-pin 1.25 mm pitch serial COM wafers CN2 and CN4 provide RS232 connections.

All wafers support RS232 without hardware flow control.

They can support RS422 and RS485 serial communication additionally based on optional configurations. It must be stipulated when ordering, as appropriate signal routing must be applied at the factory. In addition, they support single communication mode on RS485 with only half-duplex configuration.

Figure 15: Serial COM CN2, CN4

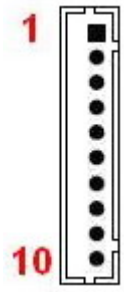


Table 22: Pin Assignment COM1 CN2, COM2 CN4

Pin	RS232 Signal	RS422 Signal	RS485 Signal	Note
1	-	TX-	DATA-	
2	-	-	-	
3	RXD	TX+	DATA+	
4	-	-	-	
5	TXD	RX+	-	
6	-	-	-	
7	-	RX-	-	
8	-	-	-	
9	GND	GND	GND	
10	+5V	+5V	+5V	500 mA max.
Connector Type				
B2W, 1x10-pin, 1.25 mm pitch				
Mating Connector				
Vendor	Pinrex			
Housing Model No.	712-75-10W001			
Terminal Model No.	712-70-T00001			

Table 23: Signal Description

Signal	Description
TXD	Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12 V) on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RXD	Received Data, receives data from the communications link.
DTR	Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to

Signal	Description
	establish communication link.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
TX+/-	Transmitted Data differential pair sends data to the communications link.
RX+/-	Received Data differential pair receives data from the communications link.
GND	Power Supply GND signal

7.5. eDP Connector (CN15)

The 40-pole 0.5 mm pitch connector CN15 provides eDP panel connection.

Figure 16: eDP Connector CN15

Table 24: Pin Assignment CN15

Pin	Signal	Description	Note
1	NC	No connection	
2	GND	Ground	
3	EDP_TXN3	eDP Lane 3 differential pair (-)	
4	EDP_TXP3	eDP Lane 3 differential pair (+)	
5	GND	Ground	
6	EDP_TXN2	eDP Lane 2 differential pair (-)	
7	EDP_TXP2	eDP Lane 2 differential pair (+)	
8	GND	Ground	
9	EDP_TXN1	eDP Lane 1 differential pair (-)	
10	EDP_TXP1	eDP Lane 1 differential pair (+)	
11	GND	Ground	
12	EDP_TXN0	eDP Lane 0 differential pair (-)	
13	EDP_TXP0	eDP Lane 0 differential pair (+)	
14	GND	Ground	
15	EDP_AUXP	eDP auxiliary channel differential pair (+)	
16	EDP_AUXN	eDP auxiliary channel differential pair (-)	
17	GND	Ground	
18	+VPNL_EDP*	+3.3 V / +5 V panel power supply	500 mA max.
19	+VPNL_EDP*	+3.3 V / +5 V panel power supply)	500 mA max.
20	+VPNL_EDP*	+3.3 V / +5 V panel power supply	500 mA max.
21	+VPNL_EDP*	+3.3 V / +5 V panel power supply	500 mA max.
22	NC	No connection	
23	GND	Ground	

Pin	Signal	Description	Note
24	GND	Ground	
25	GND	Ground	
26	GND	Ground	
27	EDP_HPD	eDP hot plug detect	
28	GND	Ground	
29	GND	Ground	
30	GND	Ground	
31	GND	Ground	
32	EDP_BKLTEN	eDP Backlight Enable	
33	BL_ADJ_PWM	Backlight adjustment PWM (Pulse Width Modulation) signal	
34	NC	No connection	
35	NC	No connection	
36	+12V_S0	+12 V backlight power supply	500 mA max.
37	+12V_S0	+12 V backlight power supply	500 mA max.
38	+12V_S0	+12 V backlight power supply	500 mA max.
39	+12V_S0	+12 V backlight power supply	500 mA max.
40	NC	No connection	
Connector Type			
B2W, 1x40-pin, 0.5 mm pitch			
Mating Connector			
Vendor	I-PEX		
Model No.	20455-040E-12		

* **Panel Power can be selected through JP5.**

7.6. Digital Input / Output Wafer (CN7)

The 10-pin 1.25 mm pitch wafer CN7 supports 8-bit digital input / output signals to provide powering-on function of the connected devices.

Figure 17: Digital Input / Output Wafer CN7

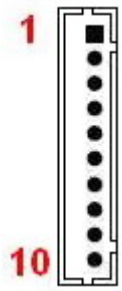


Table 25: Pin Assignment CN7

Pin	Signal	Description	Note
1	+5V	+5 V power supply	500 mA max.
2	DIO_0	Digital input / output channel 0	
3	DIO_1	Digital input / output channel 1	
4	DIO_2	Digital input / output channel 2	
5	DIO_3	Digital input / output channel 3	
6	DIO_4	Digital input / output channel 4	
7	DIO_5	Digital input / output channel 5	
8	DIO_6	Digital input / output channel 6	
9	DIO_7	Digital input / output channel 7	
10	GND	Ground	
Connector Type			
B2W, 1x10-pin, 1.25 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	712-75-10W001		
Terminal Model No.	712-70-T00001		

7.7. SPI 10-Pins Header (CN3)

The 10-pin 1.27 mm pitch header CN3 allows connection with a MCU (MicroController Unit) module for a particular application.

Figure 18: SPI 10-Pins Header CN3

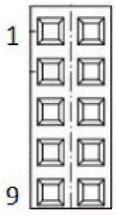


Table 26: Pin Assignment CN3

Pin	Signal	Description	Note
1	VDD	Primary supply input	
2	GND	Ground	
3	CS1#	SPI slave chip select bit 1	
4	CS0#	SPI slave chip select bit 0	
5	HOLD#	SPI HOLD	
6	SO	SPI slave serial data output	
7	SCK	SPI clock input	
8	WP#	Write-protect pin	
9	SI	SPI slave serial data input	
10	EN	Enable pin	
Connector Type			
B2B, 2x5-pin, 1.27 mm pitch			

7.8. M.2 Key B 2242 / 3042 / 3052 / 2280 Slot (M2B1)

The 2.5"-SBC-AML/ADN supports a M.2 module in format 2242 / 3042 / 3052 / 2280 with Key B. The M.2 specification supports PCIe x2, USB 2.0 and SATA 3.0 signals as well as UIM signals connected to SIM card wafer CN13. The slot can be used to integrate WWAN communication or other possible function to the mainboard.

Figure 19: M.2 Key B 2242 / 3042 / 3052 / 2280 Slot M2B1

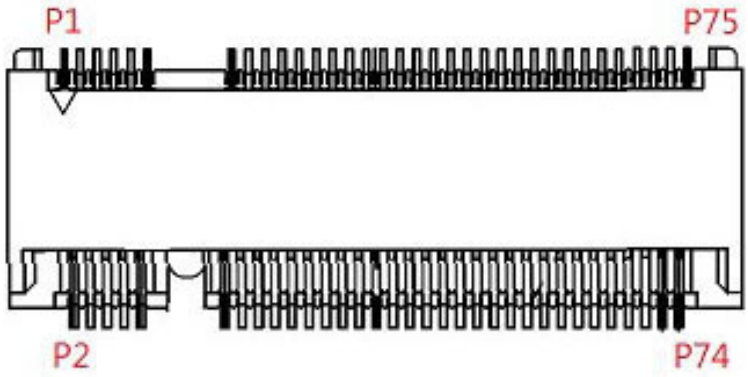


Table 27: Pin Assignment M2B1

Pin	Signal	Description	Note
1	-		
2	+3.3V	3.3 V power supply	
3	GND	Ground	
4	+3.3V	3.3 V power supply	
5	GND	Ground	
6	PWROFF#	M.2 module power enable	
7	USB_D+	USB 2.0 data differential pair (+)	
8	DISABLE#	Wireless disable	
9	USB_D-	USB 2.0 data differential pair (-)	
10	LED#	Device active signal	
11	GND	Ground	
12	KEY		
13	KEY		
14	KEY		
15	KEY		
16	KEY		
17	KEY		
18	KEY		
19	KEY		
20	-		
21	-		
22	-		
23	-		

Pin	Signal	Description	Note
24	-		
25	-		
26	-		
27	GND	Ground	
28	-		
29	PERn1	PCIe Lane 1 receiver pair (-)	
30	UIM_RESET*	SIM card reset	
31	PERp1	PCIe Lane 1 receiver pair (+)	
32	UIM_CLK*	SIM card clock	
33	GND	Ground	
34	UIM_DATA*	SIM card data	
35	PETn1	PCIe Lane 1 transmitter pair (-)	
36	UIM_PWR*	SIM card power	
37	PETp1	PCIe Lane 1 transmitter pair (+)	
38	-		
39	GND	Ground	
40	-		
41	PERn0 / SATA_B+	PCIe Lane 0 receiver pair (-) / SATA transmitter pair (+)	
42	-		
43	PERp0 / SATA_B-	PCIe Lane 0 receiver pair (+) / SATA transmitter pair (-)	
44	-		
45	GND	Ground	
46	-		
47	PETn0 / SATA_A-	PCIe Lane 0 transmitter pair (-) / SATA receiver pair (-)	
48	-		
49	PETp0 / SATA_A+	PCIe Lane 0 transmitter pair (+) / SATA receiver pair (+)	
50	PERST#	PCIe reset	
51	GND	Ground	
52	CLKREQ#	Reference clock request signal	
53	REFCLKn	PCIe reference clock pair (-)	
54	WAKE#	PCIe wake	
55	REFCLKp	PCIe reference clock pair (+)	
56	-		
57	GND	Ground	
58	-		
59	-		
60	-		
61	-		
62	-		
63	-		
64	-		
65	-		

Pin	Signal	Description	Note
66	SIM_DETECT	SIM card detect	
67	-		
68	SUSCLK	32.768 kHz clock supply input	
69	-		
70	+3.3V	3.3 V power supply	
71	GND	Ground	
72	+3.3V	3.3 V power supply	
73	GND	Ground	
74	+3.3V	3.3 V power supply	
75	-		

* These pins are connected to CN13 SIM card wafer directly.

7.9. M.2 Key E 2230 Slot (M2E1)

The 2.5"-SBC-AML/ADN supports a M.2 module in format 2230 with Key E. The M.2 specification supports PCIe x1, USB 2.0, UART, PCM and / or CNVi signals (variants with Intel® Atom® x7000RE Series processors do not support CNVi). The slot can be used to integrate WLAN (Wi-Fi or CNVi Wi-Fi) and / or Bluetooth communication or other possible function to the mainboard.

Figure 20: M.2 Key E 2230 Slot M2E1

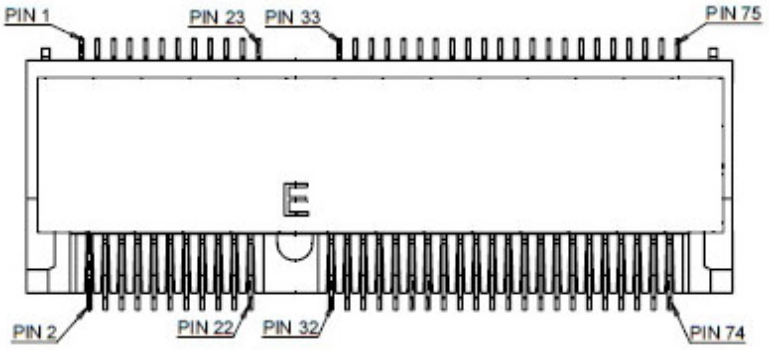


Table 28: Pin Assignment M2E1

Pin	Key E*		CNVi*		Note
	Signal	Description	Signal	Description	
1	GND	Ground	GND	Ground	
2	+3.3V_SB	3.3 V standby power supply	+3.3V_SB	3.3 V standby power supply	
3	USB_D+	USB 2.0 data diff. pair (+)	-		
4	+3.3V_SB	3.3 V standby power supply	+3.3V_SB	3.3 V standby power supply	
5	USB_D-	USB 2.0 data diff. pair (-)	-		
6	LED1#	Device active signal 1	LED1#	Device active signal 1	
7	GND	Ground	GND	Ground	
8	PCM_CLK	PCM synchronous data clock	-		
9	-		WGR_D1N	CNVio bus Rx Lane 1 (-)	
10	PCM_SYNC	PCM synchronous data sync	LCP_RSTN	RF companion (CRF) reset	
11	-		WGR_D1P	CNVio bus Rx Lane 1 (+)	
12	PCM_IN	PCM synchronous data input	-		
13	GND	Ground	GND	Ground	
14	PCM_OUT	PCM synchronous data output	CLKREQ0	Clock request	
15	-		WGR_D0N	CNVio bus Rx Lane 0 (-)	
16	LED2#	Device active signal 2	LED2#	Device active signal 2	
17	-		WGR_D0P	CNVio bus Rx Lane 0 (+)	
18	GND	Ground	GND	Ground	
19	GND	Ground	GND	Ground	
20	UART_WAKE#	UART wake-up	-		
21	-		WGR_CLKN	CNVio bus Rx clock (-)	
22	UART_RX	UART data input	BRI_RSP	BRI bus Rx	

Pin	Key E*		CNVi*		Note
	Signal	Description	Signal	Description	
23	-		WGR_CLKP	CNVio bus Rx clock (+)	
24	Key		Key		
25	Key		Key		
26	Key		Key		
27	Key		Key		
28	Key		Key		
29	Key		Key		
30	Key		Key		
31	Key		Key		
32	UART_TX	UART data output	RGI_DT	RGI bus Tx	
33	GND	Ground	GND	Ground	
34	UART_CTS	UART clear to send	RGI_RSP	RGI bus Rx	
35	PET0+	PCIe Lane 0 Tx pair (+)	-		
36	UART_RTS	UART request to send	BRI_DT	BRI bus Tx	
37	PET0-	PCIe Lane 0 Tx pair (-)	-		
38	Clink_RST	Wi-Fi CLINK host bus reset	-		
39	GND	Ground	GND	Ground	
40	Clink_DATA	Wi-Fi CLINK host bus data	-		
41	PER0+	PCIe Lane 0 Rx pair (+)	-		
42	Clink_CLK	Wi-Fi CLINK host bus clock	-		
43	PER0-	PCIe Lane 0 Rx pair (-)	-		
44	-		-		
45	GND	Ground	GND	Ground	
46	-		-		
47	REFCLK0+	PCIe reference clock pair (+)	-		
48	-		-		
49	REFCLK0-	PCIe reference clock pair (-)	-		
50	SUSCLK	32.768 kHz clock supply input	SUSCLK	32.768 kHz clock supply input	
51	GND	Ground	GND	Ground	
52	PERST0#	PCIe reset	-		
53	CLKREQ0#	Reference clock request signal	-		
54	W_DISABLE2#	Wireless disable 2	W_DISABLE2#	Wireless disable 2	
55	PEWAKE0#	PCIe wake	-		
56	W_DISABLE1#	Wireless disable 1	W_DISABLE1#	Wireless disable 1	
57	GND	Ground	GND	Ground	
58	-		-		
59	-		WT_D1N	CNVio bus Tx Lane 1 (-)	
60	-		-		
61	-		WT_D1P	CNVio bus Tx Lane 1 (+)	
62	-		-		
63	GND	Ground	GND	Ground	

Pin	Key E*		CNVi*		Note
	Signal	Description	Signal	Description	
64	-		-		
65	-		WT_D0N	CNVio bus Tx Lane 0 (-)	
66	PERST0#	PCIe reset	-		
67	-		WT_D0P	CNVio bus Tx Lane 0 (+)	
68	-		-		
69	GND	Ground	GND	Ground	
70	-		-		
71	-		WT_CLKN	CNVio bus Tx clock (-)	
72	+3.3V_SB	3.3 V standby power supply	+3.3V_SB	3.3 V standby power supply	
73	-		WT_CLKP	CNVio bus Tx clock (+)	
74	+3.3V_SB	3.3 V standby power supply	+3.3V_SB	3.3 V standby power supply	
75	GND	Ground	GND	Ground	

*** The board will auto-detect the module type and re-configure itself to an appropriate mode.**

7.10. SIM Card Wafer for M.2 Key B (CN13)

The SIM card wafer CN13 is intended to enable a SIM card holder to accommodate a SIM card and connected to UIM signals on the M.2 Key B slot M2B1.

Figure 21: SIM Card Wafer CN13

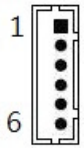


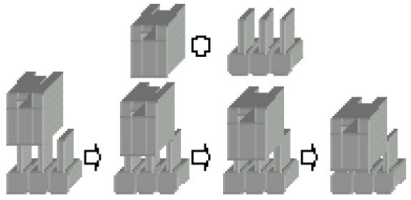
Table 29: Pin Assignment CN13

Pin	Signal	Description	Note
1	+UIM_PWR	Power +5 V or +3.3 V	
2	UIM_DATA	Input or output for serial data	
3	UIM_CLK	Clock signal	
4	UIM_RST	Reset signal	
5	UIM_CD	Card detect	
6	GND	Ground	

7.11. Switches and Jumpers

The product has several jumpers which must be properly configured to ensure correct operation.

Figure 22: Jumper Connector



For a three-pin jumper (see Figure 22), the jumper setting is designated “1-2" when the jumper connects pins 1 and 2. The jumper setting is designated “2-3" when pins 2 and 3 are connected and so on. You will see that one of the lines surrounding a jumper pin is thick, which indicates pin No.1.

To move a jumper from one position to another, use needle-nose pliers or tweezers to pull the pin cap off the pins and move it to the desired position.

7.11.1. Flash Descriptor Security Override Selection (JP1)

The 2.0 mm pitch "Flash Descriptor Security Override Selection" jumper JP1 can be used to specify whether to override the flash descriptor.

Figure 23: Flash Descriptor Security Override Selection JP1

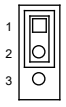


Table 30: Pin Assignment JP1

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	Controlled by EC (Embedded Controller) (Default)
-	X	Flash Security Override

“X" = Jumper set (short) and “-" = jumper not set (open)

7.11.2. Clear CMOS Selection (JP2)

The 2.0 mm pitch "Clear COMS Selection" jumper JP2 can be used to reset the Real Time Clock (RTC) and drain RTC well.

The jumper has one position: Pin 1-2 unmounted (default position) or mounted. More information on setting the "Clear CMOS Selection" jumper can be found in the following table.

Figure 24: Clear CMOS Selection JP2

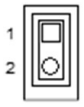


Table 31: Pin Assignment JP2

Jumper 1 Position	Description
Pin 1-2	
-	Normal Operation (default position)
X	Clear CMOS (board does not boot with the jumper in this position)

"X" = Jumper set (short) and "-" = jumper not set (open)

Do not leave the jumper in position 1-2, otherwise if the power is disconnected, the battery will fully deplete within a few weeks.

7.11.3. M.2 Key B Selection (JP3)

The 2.0 mm pitch "M.2 Key B Selection" jumper JP3 can be used to determine in which mode the M.2 Key B Slot M2B1 operates.

Figure 25: M.2 Key B Selection JP3

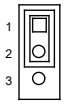


Table 32: Pin Assignment JP3

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	PCIe x2 (Default)
-	X	SATA

"X" = Jumper set (short) and "-" = jumper not set (open)

7.11.4. USB Power Selection (JP4)

The 2.0 mm pitch "USB Power Selection" jumper JP4 can be used to determine whether the USB ports are powered in the S4 / S5 state.

Figure 26: USB Power Selection JP4

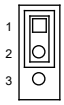


Table 33: Pin Assignment JP4

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	+5 V_S0 (Default)
-	X	+5 V_S5

"X" = Jumper set (short) and "-" = jumper not set (open)

7.11.5. eDP Panel Power Selection (JP5)

The 2.0 mm pitch "eDP Panel Power Selection" jumper JP5 can be used to select eDP panel power voltage.

Figure 27: eDP Panel Power Selection JP5

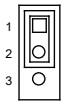


Table 34: Pin Assignment JP5

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	+3.3 V
-	X	+5 V

"X" = Jumper set (short) and "-" = jumper not set (open)

7.11.6. AT / ATX Power Mode Selection (JP6)

The 2.0 mm pitch jumper JP6 can be used to select AT power mode or ATX power mode.

Figure 28: AT / ATX Power Mode Selection JP6

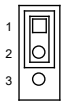


Table 35: Pin Assignment JP6

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	ATX Power Mode (Default)
-	X	AT Power Mode

"X" = Jumper set (short) and "-" = jumper not set (open)

8/ BIOS

8.1. Starting the uEFI BIOS

The 2.5"-SBC-AML/ADN is provided with a Kontron-customized, pre-installed and configured version of AMI Aptio® V uEFI BIOS. AMI BIOS firmware is based on the Unified Extensible Firmware Interface (UEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the 2.5"-SBC-AML/ADN.

The uEFI BIOS comes with a setup program that provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The setup program allows the accessing of various menus that provide functions or access to sub-menus with more specific functions of their own.

To start the uEFI BIOS setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <DEL> key.
4. If the uEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see Security menu), press <ENTER>, and proceed with step 5.
5. A setup menu will appear.

The 2.5"-SBC-AML/ADN uEFI BIOS setup program uses a hot key-based navigation system. A hot key legend bar is located on the bottom of the setup screens.

The following table provides information concerning the usage of these hot keys.

Table 36: Hotkeys Table

Signal	Description
<F1>	The <F1> key invokes the General Help window.
<->	The <Minus> key selects the next lower value within a field.
<+>	The <Plus> key selects the next higher value within a field.
<F2>	The <F2> key loads the previous values.
<F3>	The <F3> key loads the standard default values.
<F4>	The <F4> key saves the current settings and exit the uEFI BIOS setup.
<→> or <←>	The <Left/Right> arrows select major setup menus on the menu bar. For example: Main, Advanced, Security, etc.
<↑> or <↓>	The <Up/Down> arrows select fields in the current menu. For example: A setup function or a sub-screen.
<ESC>	The <ESC> key exits a major setup menu and enter the Exit setup menu. Pressing the <ESC> key in a sub-menu displays the next higher menu level.
<ENTER>	The <ENTER> key executes a command or select a submenu.

8.2. Starting the uEFI BIOS

The Setup utility features shows six menus in the selection bar at the top of the screen:

- Main
- Advanced
- Chipset
- Security
- Boot
- Save & Exit

The Setup menus are selected via the left and right arrow keys. The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white. Each Setup menu provides two main frames. The left frame displays all available functions. Functions that can be configured are displayed in blue. Functions displayed in gray provide information about the status or the operational configuration. The right frame displays an Item Specific Help window providing an explanation of the respective function.

8.2.1. Main Setup Menu

Upon entering the uEFI BIOS Setup program, the Main Setup menu is displayed. This screen lists the Main Setup menu sub-screens and provides basic system information. Additionally functions for setting the system time and date are offered.

Table 37: Main Setup Menu Sub-Screens and Functions

Function	Description
Product Information	Read only field. Displays information about the product name
BIOS Information	Read only field. Displays information about the system BIOS
FSP Information	Read only field. Display information about the FSP
Processor Information	Read only field. Display information about the processor
Memory Information	Read only field. Displays information about the memory
PCH Information	Read only field. Display information about the PCH
ME Information	Read only field. Display information about Intel Management Engine (ME) firmware
System Language	Read only field. [English] only
Platform Information	Sub-screen to board information.
System Date	Set System Date
System Time	Set System Time

Figure 29: BIOS Main Menu Screen System Data and Time

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
Product Information					
Product Name		2.5-SBC-ADN_AML			
BIOS Information					
BIOS Vendor		American Megatrends			
Core Version		5.27			
Compliancy		UEFI 2.8; PI 1.7			
Kontron BIOS Version		ADNUPXT.113 (x64)			
Access Level		Administrator			
FSP Information					
FSP Version		0C.02.89.40			
RC Version		0C.E0.89.40			
Build Date					
FSP Mode		Dispatch Mode			
Processor Information					
Name		Alder Lake ULX			
Type		Intel® Atom® x7835RE			
Speed		1300 MHz			
ID		0xB06E0			
Stepping		A0			
Package		Not Implemented Yet			
Number of Efficient-cores		8 Core(s) / 8 Thread(s)			
Microcode Revision		18			
GT Info		0x46D0			
IGFX GOP Version		21.0.1063			
Memory RC Version		0.0.4.74			
Total Memory		15872 MB			
Memory Frequency		4800 MHz			
PCH Information					
Name		PCH-N			
PCH SKU		N ASL IOT INDU SKU			
Stepping		A0			
Chipset Init Base Revision		4			
Chipset Init OEM Revision		0			
Package		Not Implemented Yet			
TXT Capability of Platform / PCH		Unsupported			
Production Type		Production			

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
Dual Output Fast Read support		Supported			
Read ID / Status Clock Freq		50 MHz			
Write and Erase Clock Freq		50 MHz			
Fast Read Clock Freq		50 MHz			
Fast Read support		Supported			
Number of Components		1 Component			
SPI Component 0 Density		32 MB			
eSPI Flash Sharing Mode		G3			
EC PECI Mode		Legacy PECI mode			
ME FW Version		16.50.12.1453		→ ←: Select Screen	
ME Firmware SKU		Consumer SKU		↑ ↓: Select Item	
PMC FW Version		160.50.0.1010		Enter: Select	
				+/-: Change Opt.	
System Language		[English]		F1: General Help	
> Platform Information				F2: Previous Values	
				F3: Optimized Defaults	
System Date		[Wed 04/16/2025]		F4: Save & Exit	
System Time		[16:50:26]		ESC: Exit	
Version 2.22.1293 Copyright (C) 2025 AMI					

Feature	Option	Description
System Date	[dd/mm/yyyy]	Set the Date. Use Tab to switch between Data elements. Default Ranges: Year: 1998 – 9999 Months: 1 – 12 Days: Dependent on month Range of Years may vary.
System Time	[hh:mm:ss]	Set the Time. Use Tab to switch between Time elements.

Figure 30: BIOS Main Menu Screen – Platform Information

Aptio Setup – AMI		
Main		
Board Information		
Product Name	2.5-SBC-AND_AML	
Serial #	Default string	
UUID	00020003-0004-0005-0006-000700080009	
KSC Information		
Controller	KSC Main Controller	
Operating Mode	Normal	
Board Name	2.5-AND_AML	
Platform ID	000B	→←: Select Screen
KSC SW Spec. Version	1.20	↑ ↓: Select Item
BIOS Protocol Version	2.3.1	Enter: Select
BIOS SW Spec. Version	1.18	+/-: Change Opt.
Core Firmware Version	1.4.1 Release	F1: General Help
Board Firmware Version	1.0.0 Release	F2: Previous Values
SCM Info	DB-8C-26-E2	F3: Optimized Defaults
		F4: Save & Exit
Boot Counter	N/A	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

Read only sub-screen.

8.2.2. Advanced Setup Menu

The Advanced setup menu provides sub-screens and functions for advanced configurations. The following sub-screen functions are included in the menu:

- cTDP, IBECC, Compliance Test, Audio, Power & ME FW Image Re-Flash Configuration
- Display Configuration
- Trusted Computing
- ACPI Settings
- Miscellaneous
- H/W Monitor
- S5 RTC Wake Settings
- Serial Port Console Redirection
- SIO Configuration
- USB Configuration
- Network Stack Configuration
- NVMe Configuration
- SDIO Configuration
- eDP Configurations
- COM Configurations
- Intel® Ethernet Controller I226-IT – C0:EA:C3:D2:0C:50
- Intel® Ethernet Controller I226-IT – C0:EA:C3:D2:0C:51

NOTICE

Setting items on this screen to incorrect values may cause the system to malfunction.

Figure 31: BIOS Advanced Menu

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
Configurable TDP Mode			[15W]		
In-Band ECC Support			[Enabled]		
Compliance Test Mode			[Disabled]		
HD Audio			[Enabled]		
Power Mode Selection			[ATX Mode]		
Restore AC Power Loss			[Power Off]		
Power Saving Mode			[Disabled]		
ME FW Image Re-Flash			[Disabled]		
> Display Configuration					
> Trusted Computing					
> ACPI Settings					
> Miscellaneous					
> H/W Monitor					
> S5 RTC Wake Settings					
> Serial Port Console Redirection					
> SIO Configuration					
> USB Configuration				→ ←: Select Screen	
> Network Stack Configuration				↑ ↓: Select Item	
> NVMe Configuration				Enter: Select	
> SDIO Configuration				+/-: Change Opt.	
> eDP Configurations				F1: General Help	
> COM Configurations				F2: Previous Values	
				F3: Optimized Defaults	
> Intel® Ethernet Controller I226-IT – C0:EA:C3:D2:0C:50				F4: Save & Exit	
> Intel® Ethernet Controller I226-IT – C0:EA:C3:D2:0C:51				ESC: Exit	
Version 2.22.1293 Copyright (C) 2025 AMI					

Feature	Option	Description
Configurable TDP Mode	[15W]	Configurable Processor Base Power (cTDP) Mode as 15W (Nominal) / 9W (Level 1) / Deactivate TDP selection. Deactivate option will set MSR to Nominal and MMIO to Zero. This option is only available for CPU i3 SKUs.
In-Band ECC Support	[Disabled], [Enabled]	Enable / Disable In-Band ECC. Will be enabled if memory has symmetric configuration
Compliance Test Mode	[Disabled], [Enabled]	Enable when using Compliance Load Board
HD Audio	[Disabled], [Enabled]	Control Detection of the HD-Audio device. [Disabled] = HDA will be unconditionally disabled. [Enabled] = HDA will be unconditionally enabled.
Power Mode Selection	[ATX mode]	Read only item.
Restore AC Power	[Power Off],	Choose options for restoring AC power loss

Feature	Option	Description
Loss	[Last State]	
Power Saving Mode	[Disabled], [Enabled]	Enable / Disable power saving mode
ME FW Image Re-Flash	[Disabled], [Enabled]	Enable / Disable ME FW Image Re-Flash function.

Figure 32: BIOS Advanced Menu - Display Configuration

Aptio Setup – AMI		
Advanced		
Display Configuration		
Primary Display	[IGFX]	→←: Select Screen
Internal Graphics	[Enabled]	↑ ↓: Select Item
Aperture Size	[256MB]	Enter: Select
		+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

Feature	Option	Description
Primary Display	[Auto], [IGFX], [PEG Slot], [PCH PCI]	Select which of IGFX / PEG / PCI Graphics device should be Primary Display or select HG for Hybrid Gfx.
Internal Graphics	[Enabled]	Read only item
Aperture Size	[128MB], [256MB], [512MB], [1024MB]	Select the Aperture Size. Note: Above 4GB MMIO BIOS assignment is automatically enabled when selecting > 2048MB aperture. To use this feature, please disable CSM Support.

Figure 33: BIOS Advanced Menu - Trusted Computing

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
TPM 2.0 Device Found					
Firmware Version:		16.13			
Vendor:		IFX			
Security Device Support		[Enable]			
Active PCR Banks*		SHA256			
Available PCR Banks*		SHA256, SHA384			
SHA256 PCR Bank*		[Enabled]			
SHA384 PCR Bank*		[Disabled]		→ ←: Select Screen	
				↑ ↓: Select Item	
Pending Operation*		[None]		Enter: Select	
Platform Hierarchy*		[Enabled]		+/-: Change Opt.	
Storage Hierarchy*		[Enabled]		F1: General Help	
Endorsement Hierarchy*		[Enabled]		F2: Previous Values	
Physical Presence Spec Version*		[1.3]		F3: Optimized Defaults	
TPM 2.0 Interface Type*		[TIS]		F4: Save & Exit	
Device Select*		[Auto]		ESC: Exit	
Version 2.22.1293 Copyright (C) 2025 AMI					

* These items appear only when enabling Security Device Support.

Feature	Option	Description
Security Device Support	[Disable], [Enable]	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
SHA256 PCR Bank	[Disabled], [Enabled]	Enable or Disable SHA256 PCR Bank
SHA384 PCR Bank	[Disabled], [Enabled]	Enable or Disable SHA384 PCR Bank
Pending Operation	[None], [TPM Clear]	Schedule an Operation for the Security Device. Note: Your Computer will reboot during restart in order to change State of Security Device.
Platform Hierarchy	[Disabled], [Enabled]	Enable or Disable Platform Hierarchy
Storage Hierarchy	[Disabled], [Enabled]	Enable or Disable Storage Hierarchy
Endorsement Hierarchy	[Disabled], [Enabled]	Enable or Disable Endorsement Hierarchy
Physical Presence Spec Version	[1.2], [1.3]	Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.
TPM 2.0 Interface Type	[TIS]	Read only item

Feature	Option	Description
Device Select	[TPM 1.2], [TPM 2.0], [Auto]	[TPM 1.2] will restrict support to TPM 1.2 devices [TPM 2.0] will restrict support to TPM 2.0 devices [Auto] will support both with default set to TPM 2.0 devices, if not found, TPM 1.2 devices will be enumerated

Figure 34: BIOS Advanced Menu – ACPI Settings

Aptio Setup – AMI		
Advanced		
ACPI Settings		
Enable ACPI Auto Configuration	[Disabled]	→←: Select Screen ↑ ↓: Select Item
Enable Hibernation*	[Enabled]	Enter: Select
ACPI Sleep State*	[S3 (Suspend to RAM)]	+/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* These items appear only when disabling Enable ACPI Auto Configuration.

Feature	Option	Description
Enable ACPI Auto Configuration	[Disable], [Enable]	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	[Disabled], [Enabled]	Enables or Disables System ability to Hibernate (OS / S4 Sleep State). This option may not be effective with some operating systems.
ACPI Sleep State	[Suspend Disabled], [S3 (Suspend to RAM)]	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.

Figure 35: BIOS Advanced Menu – Miscellaneous

Aptio Setup – AMI		
Advanced		
Miscellaneous Configuration > Preset DIO in BIOS > Control KSC firmware > Update KSC firmware > Generic eSPI Decode Ranges > Watchdog		
Reset Button Behavior	[Chipset Reset]	→←: Select Screen
I2C Speed	[100 KHz]	↑ ↓: Select Item
Onboard I2C Mode	[Multimaster]	Enter: Select
BIOS Test Mode	[Disabled]	+/-: Change Opt.
Last system reset through	[Power-on reset]	F1: General Help
Create GSPI ACPI dev	[Disabled]	F2: Previous Values
PCIe Wake	[Disabled]	F3: Optimized Defaults
		F4: Save & Exit
Onboard EEPROM Write Protect	[WP Enabled]	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

Feature	Option	Description
Reset Button Behavior	[Chipset Reset], [Power Cycle]	Select Reset Button Behavior: Chipset Reset & Power Cycle.
I2C Speed	[100 KHz], [400 KHz], [1 MHz]	Select I2C Bus Speed in KHz. For a default system 100 KHz should be an appropriate value.
Onboard I2C Mode	[Multimaster], [Busclear]	MultiMaster / BusClear
BIOS Test Mode	[Disabled]	Read only item
Last system reset through	[Power-on reset]	Read only item
Create GSPI ACPI dev	[Disabled], [Kontron Linux BSP], [Win10 RhProxy style]	If set to 'Kontron Linux BSP' then a generic GSPI device will be used by Kontron Linux BSP. 'Win10 RhProxy style' supports this driver type under Win10.
PCIe Wake	[Disabled], [Enabled]	Set to enable or disable PCIe wake. This would affect features such as Wake 0/1 and Wake from Lan (WOL).
Onboard EEPROM Write Protect	[WP Disabled], [WP Enabled]	Set WP enable or disable the Onboard EEPROM Write Protect

Figure 36: BIOS Advanced Menu – Miscellaneous – Preset DIO in BIOS

Aptio Setup – AMI
Advanced

Aptio Setup – AMI		
Advanced		
Allows to preset GPIOs during BIOS startup.		
GPIO OS usable	[GPIO 0 – GPIO 7]	
Control DIO in BIOS	[Disabled]	
DIO #0*	[Skip]	
Output level*(1)	[Low]	
DIO #1*	[Skip]	
Output level*(1)	[Low]	
DIO #2*	[Skip]	
Output level*(1)	[Low]	
DIO #3*	[Skip]	
Output level*(1)	[Low]	→←: Select Screen
DIO #4*	[Skip]	↑ ↓: Select Item
Output level*(1)	[Low]	Enter: Select
DIO #5*	[Skip]	+/-: Change Opt.
Output level*(1)	[Low]	F1: General Help
DIO #6*	[Skip]	F2: Previous Values
Output level*(1)	[Low]	F3: Optimized Defaults
DIO #7*	[Skip]	F4: Save & Exit
Output level*(1)	[Low]	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* These items appear only when enabling Control DIO in BIOS.

(1) This item appears only when selecting Output for DIO #0/1/2/3/4/5/6/7 respectively.

Feature	Option	Description
GPIO OS usable	[All available GPIO], [GPIO 0 – GPIO 7]	Set the GPIO OS usable
Control DIO in BIOS	[Disabled], [Enabled]	Enables or disables DIO GPIO control in BIOS. If set to 'disabled' then the GPIOs are not touched by BIOS.
DIO #0..7	[Input], [Output], [Skip]	Determine the type of the DIO configuration. If this is set to 'Skip' then this GPIO will be left untouched.
Output level	[Low], [High]	Set the level of a DIO pin

Figure 37: BIOS Advanced Menu – Miscellaneous – Control KSC firmware

Aptio Setup – AMI	
Advanced	
Allows to control KSC firmware related settings.	

Aptio Setup – AMI		
Advanced		
Lock FW update access	[Enabled]	→←: Select Screen ↑ ↓: Select Item
> KSC OTP area control		Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

Feature	Option	Description
Lock FW update access	[Disabled], [Enabled]	Locks access to KSC firmware area during runtime.

Figure 38: BIOS Advanced Menu – Miscellaneous – Control KSC firmware – KSC OTP area control

Aptio Setup – AMI		
Advanced		
Allows to control KSC OTP area related settings.		
KSC OTP access lock	[Enabled]	→←: Select Screen
KSC OTP write lock*	[Enabled]	↑ ↓: Select Item
KSC OTP area limit*	[Enabled]	Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* These items appear only when disabling KSC OTP access lock.

Feature	Option	Description
KSC OTP access lock	[Disabled], [Enabled]	Locks access to KSC OTP area during runtime.
KSC OTP write lock	[Disabled], [Enabled]	Locks write access to KSC OTP area during runtime.
KSC OTP area limit	[Disabled], [Enabled]	Limit access to KSC OTP area during runtime.

Figure 39: BIOS Advanced Menu – Miscellaneous – Update KSC firmware

Aptio Setup – AMI		
Advanced		
Allows to update KSC firmware from BIOS.		
Auto update KSC FW	[Disabled]	→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

Feature	Option	Description
Auto update KSC FW	[Disabled], [Enabled]	Updates KSC firmware to BIOS internal version (best known config) on next system start. To update FW set item to 'Enabled' and exit the setup using 'Save changes and exit'.

Figure 40: BIOS Advanced Menu – Miscellaneous – Generic eSPI Decode Ranges

Aptio Setup – AMI		
Advanced		
Generic eSPI Decode Ranges		
Generic LPC via eSPI Decode 1	[Disabled]	→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Base Address*	100	
Length*	8	
Version 2.22.1293 Copyright (C) 2025 AMI		

* These items appear only when enabling Generic LPC via eSPI Decode 1.

Feature	Option	Description
Generic LPC via eSPI Decode 1	[Disabled], [Enabled]	Enable generic LPC via eSPI decode range.
Base Address	Value input	Base address of the generic decode range. Valid between 0100h – FFF0h. Must be 8-byte aligned.

Feature	Option	Description
		Please note that it also has to be length-aligned.
Length	Value input	Length of the generic decode range in hexadecimal notation. Valid between 0008h – 0100h. Must be multiple of 8h.

Figure 41: BIOS Advanced Menu – Miscellaneous – Watchdog

Aptio Setup – AMI		
Advanced		
Watchdog Configuration.		
Auto-reload	[Disabled]	
Global Lock	[Disabled]	
WDT Strobe	[Disabled]	
Stage 1 Mode	[Disabled]	
Assert WDT Signal (1)	[Disabled]	
Stage 1 Timeout (2)	[1m]	→←: Select Screen
		↑ ↓: Select Item
Stage 2 Mode (3)	[Delay]	Enter: Select
Assert WDT Signal (1)	[Disabled]	+/-: Change Opt.
Stage 2 Timeout (2)	[1m]	F1: General Help
		F2: Previous Values
Stage 3 Mode (3)	[Delay]	F3: Optimized Defaults
Assert WDT Signal (1)	[Disabled]	F4: Save & Exit
Stage 3 Timeout (2)	[1m]	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

(1) This item appears only when selecting Reset or Delay for Stage 1/2/3 Mode.

(2) This item appears only when selecting Reset, Delay or WDT Signal only for Stage 1/2/3 Mode.

(3) This item appears only when selecting Delay or WDT Signal only for Stange N-1 Mode.

Feature	Option	Description
Auto-reload	[Disabled], [Enabled]	Enable automatic reload of watchdog timers on timeout.
Global Lock	[Disabled], [Enabled]	If set to enabled, all Watchdog registers (except WD_KICK) become read only until the board is reset.
WDT Strobe	[Disabled], [Enabled]	Enable / disable WDT Strobe input.
Stage 1/2/3 Mode	[Disabled], [Reset], [Delay], [WDT Signal only]	Select Action for this Watchdog stage
Assert WDT Signal	[Disabled], [Enabled]	Enable / disable assertion of WDT signal to baseboard on stage timeout.
Stage 1/2/3 Timeout	[1m],	Select Timeout value for this Watchdog stage

Feature	Option	Description
	[3m], [10m], [30m]	

Figure 42: BIOS Advanced Menu - H/W Monitor

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
KSC based H/W Monitor					
Temperature sensors:					
#1: CPU Temp		: + 74.6 C			
#2: PCH Temp		: + 65.0 C			
#3: SYSTEM Temp		: + 60.2 C			
				→ ←: Select Screen	
Voltage sensors:				↑ ↓: Select Item	
#1: V_IN		: 12.4 V		Enter: Select	
#2: 12V_S0		: 12.5 V		+/-: Change Opt.	
#3: 5V_S0		: 5.2 V		F1: General Help	
#4: 3V3_S0		: 3.4 V		F2: Previous Values	
#5: 3V_BAT		: 2.8 V		F3: Optimized Defaults	
				F4: Save & Exit	
Fan speed & control:				ESC: Exit	
Version 2.22.1293 Copyright (C) 2025 AMI					

Read only sub-screen

Figure 43: BIOS Advanced Menu – S5 RTC Wake Settings

Aptio Setup – AMI		
Advanced		
Wake system from S5	[Disabled]	
Wake up hour (1)	0	
Wake up minute (1)	0	→←: Select Screen
Wake up second (1)	0	↑ ↓: Select Item
Wake up minute increase (2)	1	Enter: Select
		+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

(1) These items appear only when selecting Fixed Time for Wake system from S5.

(2) This item appears only when selecting Dynamic Time for Wake system from S5.

Feature	Option	Description
Wake system from S5	[Disabled], [Fixed Time], [Dynamic Time]	Enable or disable System wake on alarm event. Select Fixed Time, system will wake on the hr::min::sec specified. Select Dynamic Time, system will wake on the current time + Increase minute(s).
Wake up hour	Value input	Select 0 – 23 For example, enter 3 for 3 am and 15 for 3 pm.
Wake up minute	Value input	Select 0 – 59 for Minute
Wake up second	Value input	Select 0 – 59 for Second
Wake up minute increase	Value input	1 - 5

Figure 44: BIOS Advanced Menu – Serial Port Console Redirection

Aptio Setup – AMI		
Advanced		
COM1		
Console Redirection	[Disabled]	
> Console Redirection Settings*		
		→←: Select Screen
COM2		↑ ↓: Select Item
Console Redirection	[Disabled]	Enter: Select
> Console Redirection Settings*		+/-: Change Opt.
		F1: General Help
Serial Port for Out-of-Band Management / Windows Emergency		F2: Previous Values
Management Services (EMS)		F3: Optimized Defaults
Console Redirection EMS	[Disabled]	F4: Save & Exit
> Console Redirection Settings*		ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* These items activate only when enabling Console Redirection (EMS).

Feature	Option	Description
Console Redirection (EMS)	[Disabled], [Enabled]	Console Redirection Enable or Disable.

Figure 45: BIOS Advanced Menu – Serial Port Console Redirection – COM01/2 Console Redirection Settings

Aptio Setup – AMI		
Advanced		
COM01/2		
Console Redirection Settings		
Terminal Type	[ANSI]	
Bits per second	[115200]	→←: Select Screen
Data Bits	[8]	↑ ↓: Select Item
Parity	[None]	Enter: Select
Stop Bits	[1]	+/-: Change Opt.
Flow Control	[None]	F1: General Help
VT-UTF8 Combo Key Support	[Enabled]	F2: Previous Values
Recorder Mode	[Disabled]	F3: Optimized Defaults
Resolution 100x31	[Disabled]	F4: Save & Exit
Putty KeyPad	[VT100]	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

Feature	Option	Description
Terminal Type	[VT100],	Emulation:

Feature	Option	Description
	[VT100Plus], [VT-UTF8], [ANSI]	[ANSI]: Extended ASCII char set. [VT100]: ASCII char set. [VT100Plus]: Extends VT100 to support color, function keys, etc. [VT-UTF8]: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	[9600], [19200], [38400], [57600], [115200]	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	[7], [8]	Data Bits
Parity	[None], [Even], [Odd], [Mark], [Space]	A parity bit can be sent with the data bits to detect some transmission errors. [Even]: parity bit is 0 if the num of 1's in the data bits is even. [Odd]: parity bit is 0 if num of 1's in the data bits is odd. [Mark]: parity bit is always 1. [Space]: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
Stop Bits	[1], [2]	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	[None], [Hardware RTS/CTS]	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start / stop signals.
VT-UTF8 Combo Key Support	[Disabled], [Enabled]	Enable VT-UTF8 Combination Key Support for ANSI / VT100 terminals
Recorder Mode	[Disabled], [Enabled]	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	[Disabled], [Enabled]	Enables or disables extended terminal resolution
Putty KeyPad	[VT100], [LINUX], [XTERMR6], [SCO], [ESCN], [VT400]	Select FunctionKey and KeyPad on Putty.

Figure 46: BIOS Advanced Menu – Serial Port Console Redirection – Console Redirection EMS Settings

Aptio Setup – AMI		
Advanced		
Out-of-Band Mgmt Port	[COM1]	
Terminal Type EMS	[VT-UTF8]	

Aptio Setup – AMI		
Advanced		
Bits per second EMS	[115200]	→←: Select Screen
Flow Control EMS	[None]	↑ ↓: Select Item
Data Bits EMS	8	Enter: Select
Parity EMS	None	+/-: Change Opt.
Stop Bits EMS	1	F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

Feature	Option	Description
Out-of-Band Mgmt Port	[COM1], [COM2]	Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.
Terminal Type EMS	[VT100], [VT100Plus], [VT-UTF8], [ANSI]	VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type / Emulation.
Bits per second EMS	[9600], [19200], [57600], [115200]	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Flow Control EMS	[None], [Hardware RTS/CTS], [Software Xon/Xoff]	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start / stop signals.

Figure 47: BIOS Advanced Menu – SIO Configuration

Aptio Setup – AMI	
Advanced	
AMI SIO Driver Version: A5.19.00	
Super IO Chip Logical Devices(s) Configuration > [*Active*] Serial Port 0 > [*Active*] Serial Port 1 WARNING: Logical Devices state on the left side of the control, reflects the current Logical Device state. Changes made during Setup Session will be shown after you restart the system.	→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI	

Figure 48: BIOS Advanced Menu – SIO Configuration – [*Active*] Serial Port 0

Aptio Setup – AMI		
Advanced		
Serial Port 0 Configuration		
Use This Device	[Enabled]	→←: Select Screen ↑ ↓: Select Item
Logical Device Settings:* Current: IO=3F8h; IRQ=4;*		Enter: Select +/-: Change Opt. F1: General Help
Possible:*	[Use Automatic Settings]	F2: Previous Values F3: Optimized Defaults
WARNING: Disabling SIO Logical Devices may have unwanted side effects. PROCEED WITH CAUTION.		F4: Save & Exit ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* These items appear only when enabling Use This Device.

Feature	Option	Description
Use This Device	[Disabled], [Enabled]	Enables or Disables this Logical Device.
Possible:	[Use Automatic Settings], [IO=3F8h; IRQ=4;], [IO=3F8h; IRQ=4;], [IO=2F8h; IRQ=3;]	Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.

Figure 49: BIOS Advanced Menu – SIO Configuration – [*Active*] Serial Port 1

Aptio Setup – AMI		
Advanced		
Serial Port 1 Configuration		
Use This Device	[Enabled]	→ ←: Select Screen ↑ ↓: Select Item
Logical Device Settings:*		Enter: Select
Current: IO=2F8h; IRQ=3;*		+/-: Change Opt.
Possible:*	[Use Automatic Settings]	F1: General Help F2: Previous Values F3: Optimized Defaults
WARNING: Disabling SIO Logical Devices may have unwanted side effects. PROCEED WITH CAUTION.		F4: Save & Exit ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* These items appear only when enabling Use This Device.

Feature	Option	Description
Use This Device	[Disabled], [Enabled]	Enables or Disables this Logical Device.
Possible:	[Use Automatic Settings], [IO=2F8h; IRQ=3;], [IO=2F8h; IRQ=3;], [IO=3F8h; IRQ=4;]	Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.

Figure 50: BIOS Advanced Menu - USB Configuration

Aptio Setup – AMI		
Advanced		
USB Configuration		
USB Module Version	32	
USB Controllers: 2 XHCIs USB Devices: 1 Keyboard		
Legacy USB Support	[Enabled]	→←: Select Screen
XHCI Hand-off	[Enabled]	↑ ↓: Select Item
USB Mass Storage Driver Support	[Enabled]	Enter: Select
		+/-: Change Opt.
USB hardware delays and time-outs:		F1: General Help
USB transfer time-out	[20 sec]	F2: Previous Values
Device reset time-out	[20 sec]	F3: Optimized Defaults
Device power-up delay	[Auto]	F4: Save & Exit
Device power-up delay in seconds*	5	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* This item appears only when selecting Manual for Device power-up delay.

Feature	Option	Description
Legacy USB Support	[Enabled], [Disabled], [Auto]	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
XHCI Hand-off	[Enabled], [Disabled]	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	[Disabled], [Enabled]	Enable / Disable USB Mass Storage Driver Support.
USB transfer time-out	[1 sec], [5 sec], [10 sec], [20 sec]	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	[10 sec], [20 sec], [30 sec], [40 sec]	USB mass storage device Start Unit command time-out.
Device power-up delay	[Auto], [Manual]	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub

Feature	Option	Description
		port the delay is taken from Hub descriptor.
Device power-up delay in seconds	Value input	Dealy range is 1 .. 40 seconds, in one second increments.

Figure 51: BIOS Advanced Menu - Network Stack Configuration

Aptio Setup – AMI		
Advanced		
Network Stack	[Disabled]	
IPv4 PXE Support*	[Disabled]	
IPv4 HTTP Support*	[Disabled]	→ ←: Select Screen
IPv6 PXE Support*	[Disabled]	↑ ↓: Select Item
IPv6 HTTP Support*	[Disabled]	Enter: Select
PXE boot wait time*	0	+/-: Change Opt.
Media detect count*	1	F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* These items appear only when enabling Network Stack.

Feature	Option	Description
Network Stack	[Disabled], [Enabled]	Enable / Disable UEFI Network Stack.
IPv4 PXE Support	[Disabled], [Enabled]	Enable / Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
IPv4 HTTP Support	[Disabled], [Enabled]	Enable / Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.
IPv6 PXE Support	[Disabled], [Enabled]	Enable / Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.
IPv6 HTTP Support	[Disabled], [Enabled]	Enable / Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.
PXE boot wait time	Value input	Wait time in seconds to press ESC key to abort the PXE boot. Use either + / - or numeric keys to set the value.
Media detect count	Value input	Number of times the presence of media will be checked. Use either + / - or numeric keys to set the value.

Figure 52: BIOS Advanced Menu - NVMe Configuration

Aptio Setup – AMI	
Advanced	
NVMe Configuration	
No NVMe Device Found	→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI	

Read only sub-screen

Figure 53: BIOS Advanced Menu - SDIO Configuration

Aptio Setup – AMI		
Advanced		
SDIO Configuration		
SDIO Access Mode	[Auto]	→←: Select Screen ↑ ↓: Select Item
Mass Storage Devices:		Enter: Select +/-: Change Opt.
Bus 0 Dev 1A Func 0		F1: General Help
eMMC 0IM20G (127.3GB)	[Auto]	F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

Feature	Option	Description
SDIO Access Mode	[Auto], [ADMA], [SDMA], [PIO]	[Auto]: Access SD device in DMA mode if controller supports it, otherwise in PIO mode. [DMA]: Access SD device in DMA mode. [PIO]: Access SD device in PIO mode.
eMMC 0IM20G (127.3GB)	[Auto], [Floppy], [Forced FDD], [Hard Disk]	Mass storage device emulation type. 'Auto' enumerates devices less than 530MB as floppies. 'Forced FDD' option can be used to force HDD formatted drive to boot as FDD.

Figure 54: BIOS Advanced Menu - eDP Configurations

Aptio Setup – AMI		
Advanced		
eDP Configurations		
Backlight Source Selection	[Controlled by PCH]	→←: Select Screen
Panel Brightness*	100	↑ ↓: Select Item
Panel PWM*	[Normal PWM]	Enter: Select
Panel PWM Frequency*	[200]	+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* These items appear only when selecting Controlled by EC for Backlight Soyrce Selection.

Feature	Option	Description
Backlight Source Selection	[Controlled by EC], [Controlled by PCH]	Set the backlight source Selection
Panel Brightness	Value input	Set panel brightness value controlled by EC. Range is between 0 – 100%
Panel PWM	[Normal PWM], [Inverted PWM]	Set panel PWM behavior
Panel PWM Frequency	[200], [1K], [5K], [10K], [20K], [30K], [40K]	Set panel PWM Frequency

Figure 55: BIOS Advanced Menu - COM Configurations

Aptio Setup – AMI		
Advanced		
COM Configurations		
COM1 Mode Selection	[RS-232]	→←: Select Screen
COM1 Transceiver	[Normal mode]	↑ ↓: Select Item
COM1 Internal Terminator Switch Control	[Terminator switch is disabled.]	Enter: Select
COM1 External Terminator Switch Control	[Terminator switch is disabled.]	+/-: Change Opt.
		F1: General Help
COM2 Mode Selection	[RS-232]	F2: Previous Values
COM2 Transceiver	[Normal mode]	F3: Optimized Defaults
COM2 Internal Terminator Switch Control	[Terminator switch is disabled.]	F4: Save & Exit
COM2 External Terminator Switch Control	[Terminator switch is disabled.]	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

Feature	Option	Description
COM1/2 Mode Selection	[RS-422 Single Master], [RS-232], [RS-485 with Auto Flow Control], [RS-422 Multi Master]	Mode selection for COM1/2
COM1/2 Transceiver	[Shutdown mode], [Normal mode]	Shutdown the Transceiver of COM1/2
COM1/2 Internal Terminator Switch Control	[Terminator switch is disabled.], [Terminator switch is enabled.]	Internal Terminator switch control for RS-422 / RS-485 of COM1/2
COM1/2 External Terminator Switch Control	[Terminator switch is disabled.], [Terminator switch is enabled.]	External Terminator switch control for RS-422 / RS-485 of COM1/2

Figure 56: BIOS Advanced Menu – Intel® Ethernet Controller I226-IT – C0:EA:C3:D2:0C:50/51

Aptio Setup – AMI		
Advanced		
UEFI Driver	Intel® 2.5G Ethernet Controller 0.10.06	
Device Name	Intel® Ethernet Controller I226-IT	
		→←: Select Screen
Link Status	[Disconnected]	↑ ↓: Select Item
		Enter: Select
MAC Address	C0:EA:C3:D2:0C:50/51	+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

Read only sub-screen

8.2.3. Chipset Setup Menu

The Chipset setup menu provides functions and a sub-screen for chipset configurations. The following sub-screen function is included in the menu:

- System Agent (SA) Configuration
- PCH-IO Configuration

Figure 57: BIOS Chipset Setup Menu

Aptio Setup – AMI					
Main	**Advanced**	**Chipset**	**Security**	**Boot**	**Save & Exit**
> System Agent (SA) Configuration > PCH-IO Configuration					
				→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
Version 2.22.1293 Copyright (C) 2025 AMI					

Figure 58: BIOS Chipset Setup Menu – System Agent (SA) Configuration

Aptio Setup – AMI		
Chipset		
System Agent (SA) Configuration		
VT-d	Supported	→ ←: Select Screen
		↑ ↓: Select Item
> Graphics Configuration		Enter: Select
		+/-: Change Opt.
VT-d	[Enabled]	F1: General Help
Above 4GB MMIO BIOS assignment	[Enabled]	F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

Feature	Option	Description
VT-d	[Enabled], [Disabled]	VT-d capability
Above 4GB MMIO BIOS assignment	[Enabled], [Disabled]	Enable / Disable above 4GB MemoryMappedIO BIOS assignment. This is enabled automatically when Aperture Size is set to 2048MB.

Figure 59: BIOS Chipset Setup Menu – System Agent (SA) Configuration – Graphics Configuration

Aptio Setup – AMI		
Chipset		
Graphics Configuration		
Graphics Turbo IMON Current	31	
Skip Scaning of External Gfx Card	[Disabled]	
> External Gfx Card Primary Display Configuration		
GTT Size	[8MB]	
PSMI SUPPORT	[Disabled]	
PSMI Region Size (1)	[32MB]	
Intel Graphics Pei Display Peim	[Disabled]	
VDD Enable	[Enabled]	
Configure GT for use	[Enabled]	→ ←: Select Screen
RC1p Support (2)	[Disabled]	↑ ↓: Select Item
PAVP Enable	[Enabled]	Enter: Select
Cdynmax Clamping Enable	[Disabled]	+/-: Change Opt.
Cd Clock Frequency	[Max CdClock freq based on Reference Clk]	F1: General Help

Aptio Setup – AMI		
Chipset		
Enable Display Audio Link in Pre-OS	[Disabled]	F2: Previous Values
IUER Button Enable	[Disabled]	F3: Optimized Defaults
> LCD Control		F4: Save & Exit
> Intel® Ultrabook Event Support		ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

(1) This item appears only when enabling PSMI SUPPORT.

(2) This item appears only when enabling Configure GT for use.

Feature	Option	Description
Graphics Turbo IMON Current	Value input	Graphics turbo IMON current values supported (14 - 31)
Skip Scaning of External Gfx Card	[Disabled], [Enabled]	If Enable, it will not scan for External Gfx Card on PEG and PCH PCIE Ports
GTT Size	[2MB], [4MB], [8MB]	Select the GTT Size
PSMI SUPPORT	[Disabled], [Enabled]	PSMI Enable / Disable
PSMI Region Size	[32MB], [288MB], [544MB], [800MB], [1024MB]	Select the PSMI Region Size: Range from 32MB to 1024MB
Intel Graphics Pei Display Peim	[Enabled], [Disabled]	Enable / Disable Pei (Early) Display
VDD Enable	[Disabled], [Enabled]	Enable / Disable forcing of VDD in the BIOS
Configure GT for use	[Enabled], [Disabled]	Enable / Disable GT configuration in BIOS
RC1p Support	[Enabled], [Disabled]	Enable / Disable RC1p support. If RC1p is enabled, send a RC1p frequency request to PMA based other conditions being met
PAVP Enable	[Enabled], [Disabled]	Enable / Disable PAVP
Cdynmax Clamping Enable	[Enabled], [Disabled]	Enable / Disable Cdynmax Clamping
Cd Clock Frequency	[192 Mhz], [307.2 Mhz], [556.8 Mhz], [652.8 Mhz], [Max CdClock freq based on Reference Clk]	Select the highest Cd Clock frequency supported by the platform
Enable Display Audio Link in Pre-OS	[Disabled], [Enabled]	[Enabled]: Display Audio Link will be enabled in Pre-OS. [Disabled]: Display Audio Link will be disabled in Pre-OS.

Feature	Option	Description
IUER Button Enable	[Disabled], [Enabled]	Enable / Disable IUER Button Functionality

Figure 60: BIOS Chipset Setup Menu – System Agent (SA) Configuration – Graphics Configuration – External Gfx Card Primary Display Configuration

Aptio Setup – AMI	
Chipset	
External Gfx Card Primary Display Configuration	
	→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI	

Figure 61: BIOS Chipset Setup Menu – System Agent (SA) Configuration – Graphics Configuration – LCD Control

Aptio Setup – AMI		
Chipset		
LCD Control		
LCD Panel Type	[VBIOS Default]	→←: Select Screen
Panel Scaling	[Auto]	↑ ↓: Select Item
Backlight Control	[PWM Normal]	Enter: Select
Active LFP	[eDP Port-A]	+/-: Change Opt.
Panel Color Depth	[18 Bit]	F1: General Help
Backlight Brightness	255	F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

Feature	Option	Description
LCD Panel Type	[VBIOS Default], [640x480 LVDS], [800x600 LVDS], [1024x768 LVDS], [1280x1024 LVDS],	Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.

Feature	Option	Description
	[1400x1050 LVDS1], [1400x1050 LVDS2], [1600x1200 LVDS], [1280x768 LVDS], [1680x1050 LVDS], [1920x1200 LVDS], [1600x900 LVDS], [1280x800 LVDS], [1280x600 LVDS], [2048x1536 LVDS], [1366x768 LVDS]	
Panel Scaling	[Auto], [Off], [Force Scaling]	Select the LCD panel scaling option used by the Internal Graphics Device.
Backlight Control	[PWM Inverted], [PWM Normal]	Back Light Control Setting
Active LFP	[No eDP], [eDP Port-A]	Select the Active LFP Configuration. [No LVDS]: VBIOS does not enable LVDS. [Int-LVDS]: VBIOS enables LVDS driver by Integrated encoder. [SDVO LVDS]: VBIOS enables LVDS driver by SDVO encoder. [eDP Port-A]: LFP Driven by Int-DisplayPort encoder from Port-A. [eDP Port-D]: LFP Driven by Int-DisplayPort encoder from Port-D (through PCH).
Panel Color Depth	[18 Bit], [24 Bit]	Select the LFP Panel Color Depth
Backlight Brightness	Value input	Set VBIOS Brightness. Range: 0 – 255.

Figure 62: BIOS Chipset Setup Menu – System Agent (SA) Configuration – Graphics Configuration – Intel® Ultrabook Event Support

Aptio Setup – AMI		
Chipset		
Intel® Ultrabook Event Support		
IUER Slate Enable	[Disabled]	→←: Select Screen
Slate Mode boot value (1)	[Laptop Mode]	↑ ↓: Select Item
Slate Mode on S3 and S4 resume (1)	[No change]	Enter: Select
IUER Dock Enable	[Disabled]	+/-: Change Opt.
Dock Mode boot value (2)	[Undocked]	F1: General Help
Dock Mode upon S3 and S4 resume (2)	[No change]	F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

(1) These items appear only when enabling IUER Slate Enable.

(2) These items appear only when enabling IUER Dock Enable.

Feature	Option	Description
IUER Slate Enable	[Disabled], [Enabled]	Enable / Disable IUER Slate Functionality
Slate Mode boot value	[Slate Mode], [Laptop Mode]	Choose Slate or Laptop as boot mode.
Slate Mode on S3 and S4 resume	[No change], [Toggle]	Keep it the same as Sx entry or toggle it.
IUER Dock Enable	[Disabled], [Enabled]	Enable / Disable IUER Dock Functionality
Dock Mode boot value	[Undocked], [Docked]	Choose Docked or Undocked as boot mode.
Dock Mode upon S3 and S4 resume	[No change], [Toggle]	Keep it the same as Sx entry or toggle it.

Figure 63: BIOS Chipset Setup Menu – PCH-IO Configuration

Aptio Setup – AMI		
Chipset		
PCH-IO Configuration		
> PCI Express Configuration		
> SATA Configuration		→ ←: Select Screen
> USB Configuration		↑ ↓: Select Item
		Enter: Select
> TSN GBE Configuration		+/-: Change Opt.
		F1: General Help
PCH LAN Controller	No GbE Region	F2: Previous Values
Port 80h Redirection	[LPC Bus]	F3: Optimized Defaults
Enhance Port 80h LPC Decoding*	[Enabled]	F4: Save & Exit
Compatible Revision ID	[Disabled]	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* This item activates only when selecting LPC Bus for Port 80h Redirection.

Feature	Option	Description
Port 80h Redirection	[LPC Bus], [PCIE Bus]	Control where the Port 80h cycles are sent.
Enhance Port 80h LPC Decoding	[Disabled], [Enabled]	Support the word / dword decoding of port 80h behind LPC
Compatible Revision ID	[Disabled]	Read only item

Figure 64: BIOS Chipset Setup Menu – PCH-IO Configuration – PCI Express Configuration

Aptio Setup – AMI		
Chipset		
PCI Express Configuration		
DMI Link ASPM Control	[Auto]	
Port8xh Decode	[Disabled]	
Port8xh Decode Port#*	0	
PCIe function swap	[Enabled]	
PCH PCIE Clock Gating	[Disabled]	
PCH PCIE Power Gating	[Disabled]	
> PCIe EQ settings		
PCI Express Root Port 1	Lane configured as USB / SATA / UFS	
PCI Express Root Port 2	Lane configured as USB / SATA / UFS	
PCI Express Root Port 3	Lane configured as USB / SATA / UFS	
> PCI Express Root Port 4		

Aptio Setup – AMI		
Chipset		
PCI Express Root Port 5	Not present in this SKU	
PCI Express Root Port 6	Not present in this SKU	→←: Select Screen
> PCI Express Root Port 7		↑ ↓: Select Item
PCI Express Root Port 8	Not present in this SKU	Enter: Select
> PCI Express Root Port 9		+/-: Change Opt.
PCI Express Root Port 10	Shadowed by x2 / x4 port	F1: General Help
> PCI Express Root Port 11		F2: Previous Values
PCI Express Root Port 12	Shadowed by x2 / x4 port	F3: Optimized Defaults
		F4: Save & Exit
> PCIE clocks		ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* This item appears only when enabling Port8xh Decode.

Feature	Option	Description
DMI Link ASPM Control	[Disabled], [L0s], [L1], [L0sL1], [Auto]	The control of Active State Power Management of the DMI Link.
Port8xh Decode	[Disabled], [Enabled]	PCI Express Port8xh Decode Enable / Disable.
Port8xh Decode Port#	Value input	Select PCI Express Port8xh Decode Root Port. User to ensure port availability
PCIe function swap	[Disabled], [Enabled]	When Disabled, prevents PCIE rootport function swap. If any function other than 0th is enabled, 0th will become visible.
PCH PCIE Clock Gating	[Disabled], [Enabled]	PCH PCI Express Clock Gating Enable / Disable for all port
PCH PCIE Power Gating	[Disabled], [Enabled]	PCH PCI Express Power Gating Enable / Disable for all port

Figure 65: BIOS Chipset Setup Menu – PCH-IO Configuration – PCI Express Configuration – PCIe EQ settings

Aptio Setup – AMI		
Chipset		
PCIe EQ override	[Disabled]	
PCIe EQ method*	[PCIe hardware EQ]	
PCIe EQ mode*	[Use presets during EQ]	
EQ PH1 downstream port transmitter present*	0	
EQ PH1 upstream port transmitter present*	0	
Enable EQ phase 2 local transmitter override*	[Disabled]	
Number of presents or coefficients used during phase 3*	0	
Preset 0*(1)	0	

Aptio Setup – AMI		
Chipset		
Preset 1*(1)	0	
Preset 2*(1)	0	
Preset 3*(1)	0	
Preset 4*(1)	0	
Preset 5*(1)	0	
Preset 6*(1)	0	
Preset 7*(1)	0	
Preset 8*(1)	0	
Preset 9*(1)	0	
Preset 10*(1)	0	
Pre-cursor coefficient 0*(2)	0	
Post-cursor coefficient 0*(2)	0	
Pre-cursor coefficient 1*(2)	0	
Post-cursor coefficient 1*(2)	0	
Pre-cursor coefficient 2*(2)	0	
Post-cursor coefficient 2*(2)	0	
Pre-cursor coefficient 3*(2)	0	
Post-cursor coefficient 3*(2)	0	
Pre-cursor coefficient 4*(2)	0	
Post-cursor coefficient 4*(2)	0	
Pre-cursor coefficient 5*(2)	0	
Post-cursor coefficient 5*(2)	0	→←: Select Screen
Pre-cursor coefficient 6*(2)	0	↑ ↓: Select Item
Post-cursor coefficient 6*(2)	0	Enter: Select
Pre-cursor coefficient 7*(2)	0	+/-: Change Opt.
Post-cursor coefficient 7*(2)	0	F1: General Help
Pre-cursor coefficient 8*(2)	0	F2: Previous Values
Post-cursor coefficient 8*(2)	0	F3: Optimized Defaults
Pre-cursor coefficient 9*(2)	0	F4: Save & Exit
Post-cursor coefficient 9*(2)	0	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* These items appear only when enabling PCIe EQ override.

(1) These items appear only when selecting Use presets during EQ for PCIe EQ mode.

(2) These items appear only when selecting Use coefficients during EQ for PCIe EQ mode.

Feature	Option	Description
PCIe EQ override	[Disabled], [Enabled]	Choose your own PCIe EQ settings, only for users who have a thorough understanding of equalization process
PCIe EQ method	[PCIe hardware EQ], [PCIe fixed EQ]	Choose PCIe EQ method
PCIe EQ mode	[Use presets during EQ], [Use coefficients	Choose EQ mode. Preset mode – root port will use presets during EQ process,

Feature	Option	Description
	during EQ]	Coefficient mode – root port will use coefficients during EQ process
EQ PH1 downstream port transmitter preset	Value input	Choose the value of the preset that will be used during phase 1 of the equalization
EQ PH1 upstream port transmitter preset	Value input	Choose the value of the preset that will be used during phase 1 of the equalization
Enable EQ phase 2 local transmitter override	[Disabled], [Enabled]	EQ Phase 2 local transmitter override can be used to debug issues with PCI devices equalization.
Number of presets or coefficients used during phase 3	Value input	Select how many presets or coefficients will be used during phase 3 of EQ. Please not that you have to set all of the list entries to valid values. The interpretation of this field depends on PCIe EQ mode
Preset 0..10	Value input	Choose the target preset value
Pre-cursor coefficient 0..9	Value input	Choose the target pre-cursor coefficient value
Post-cursor coefficient 0..9	Value input	Choose the target post-cursor coefficient value

Figure 66: BIOS Chipset Setup Menu – PCH-IO Configuration – PCI Express Configuration – PCI Express Root Port 4 / 7 / 9 / 11

Aptio Setup – AMI		
Chipset		
PCI Express Root Port 4 / 7 / 9 / 11	[Enabled]	
Connection Type*	[Slot]	
ASPM*	[Auto]	
L1 Substates*	[L1.1 & L1.2]	
L1 Low*	[Enabled]	
ACS*	[Enabled]	
PTM*	[Enabled]	
DPC*	[Disabled]	
EDPC*	[Enabled]	
URR*	[Disabled]	
FER*	[Disabled]	
NFER*	[Disabled]	
CER*	[Disabled]	
SEFE*	[Disabled]	
SENFE*	[Disabled]	
SECE*	[Disabled]	
PME SCI*	[Enabled]	
Hot Plug*	[Disabled]	
Advanced Error Reporting*	[Enabled]	
PCIe Speed*	[Auto]	
Transmitter Half Swing*	[Disabled]	

Aptio Setup – AMI		
Chipset		
Detect Timeout*	0	
Extra Bus Reserved*	0	
Reserved Memory*	10	
Reserved I/O*	4	
PCH PCIe LTR Configuration*		
LTR*	[Enabled]	
Snoop Latency Override*#	[Auto]	→←: Select Screen
Snoop Latency Value*#(1)	60	↑ ↓: Select Item
Snoop Latency Multiplier*#(1)	[1024 ns]	Enter: Select
Non Snoop Latency Override*#	[Auto]	+/-: Change Opt.
Non Snoop Latency Value*#(2)	60	F1: General Help
Non Snoop Latency Multiplier*#(2)	[1024 ns]	F2: Previous Values
		F3: Optimized Defaults
LTR Lock*	[Disabled]	F4: Save & Exit
Peer Memory Write Enable*	[Disabled]	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* These items appear only when enabling PCI Express Root Port 4 / 7 / 9 / 11.

These items appear only when enabling LTR.

(1) These items appear only when selecting Manual for Snoop Latency Override.

(2) These items appear only when selecting Manual for Mon Snoop Latency Override.

Feature	Option	Description
PCI Express Root Port 4 / 7 / 9 / 11	[Disabled], [Enabled]	Control the PCI Express Root Port.
Connection Type	[Bulit-in], [Slot]	[Built-in]: a built-in device is connected to this rootport. SlotImplemented bit will be clear. [Slot]: this rootport connects to user-accessible slot. SlotImplemented bit will be set.
ASPM	[Disabled], [L1], [Auto]	Set the ASPM Level: Force L0s – Force all links to L0s State AUTO – BIOS auto configure DISABLE – Disables ASPM
L1 Substates	[Disabled], [L1.1], [L1.1 & L1.2]	PCI Express L1 Substates settings.
L1 Low	[Disabled], [Enabled]	PCI Express L1 Low Substate Enable / Disable.
ACS	[Disabled], [Enabled]	Enable / Disable Access Control Services Extended Capability
PTM	[Disabled], [Enabled]	Enable / Disable Precision Time Measurement
DPC	[Disabled],	Enable / Disable Downstream Port Containment

Feature	Option	Description
	[Enabled]	
EDPC	[Disabled], [Enabled]	Enable / Disable Rootport extensions for Downstream Port Containment
URR	[Disabled], [Enabled]	PCI Express Unsupported Request Reporting Enable / Disable.
FER	[Disabled], [Enabled]	PCI Express Device Fatal Error Reporting Enable / Disable.
NFER	[Disabled], [Enabled]	PCI Express Device Non-Fatal Error Reporting Enable / Disable.
CER	[Disabled], [Enabled]	PCI Express Device Correctable Error Reporting Enable / Disable.
SEFE	[Disabled], [Enabled]	Root PCI Express System Error on Fatal Error Enable / Disable.
SENFE	[Disabled], [Enabled]	Root PCI Express System Error on Non-Fatal Error Enable / Disable.
SECE	[Disabled], [Enabled]	Root PCI Express System Error on Correctable Error Enable / Disable.
PME SCI	[Disabled], [Enabled]	PCI Express PME SCI Enable / Disable.
Hot Plug	[Disabled], [Enabled]	PCI Express Hot Plug Enable / Disable.
Advanced Error Reporting	[Disabled], [Enabled]	Advanced Error Reporting Enable / Disable.
PCIe Speed	[Auto], [Gen1], [Gen2], [Gen3]	Configure PCIe Speed
Transmitter Half Swing	[Disabled], [Enabled]	Transmitter Half Swing Enable / Disable.
Detect Timeout	Value input	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.
Extra Bus Reserved	Value input	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reserved Memory	Value input	Reserved Memory for this Root Bridge (1-20) MB
Reserved I/O	Value input	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.
LTR	[Disabled], [Enabled]	PCH PCIE Latency Reporting Enable / Disable
Snoop Latency Override	[Disabled], [Manual], [Auto]	Snoop Latency Override for PCH PCIE. [Disabled]: Disable override. [Manual]: Manually enter override values. [Auto] (default): Maintain default BIOS flow.
Snoop Latency Value	Value input	LTR Snoop Latency value of PCH PCIE
Snoop Latency Multiplier	[1 ns], [32 ns], [1024 ns], [32768 ns],	LTR Snoop Latency Multiplier of PCH PCIE

Feature	Option	Description
	[1048576 ns], [33554432 ns]	
Non Snoop Latency Override	[Disabled], [Manual], [Auto]	Non Snoop Latency Override for PCH PCIE. [Disabled]: Disable override. [Manual]: Manually enter override values. [Auto] (default): Maintain default BIOS flow.
Non Snoop Latency Value	Value input	LTR Non Snoop Latency value of PCH PCIE
Non Snoop Latency Multiplier	[1 ns], [32 ns], [1024 ns], [32768 ns], [1048576 ns], [33554432 ns]	LTR Non Snoop Latency Multiplier of PCH PCIE
LTR Lock	[Disabled], [Enabled]	PCIE LTR Configuration Lock
Peer Memory Write Enable	[Disabled], [Enabled]	Peer Memory Write Enable / Disable

Figure 67: BIOS Chipset Setup Menu – PCH-IO Configuration – PCI Express Configuration – PCIE clocks

Aptio Setup – AMI		
Chipset		
Clock0 assignment	[Enabled]	
ClkReq for Clock0	[Platform-POR]	
Clock1 assignment	[Enabled]	
ClkReq for Clock1	[Platform-POR]	
Clock2 assignment	[Enabled]	
ClkReq for Clock2	[Platform-POR]	
Clock3 assignment	[Enabled]	
ClkReq for Clock3	[Platform-POR]	
Clock4 assignment	[Enabled]	
ClkReq for Clock4	[Platform-POR]	
Clock5 assignment	[Enabled]	
ClkReq for Clock5	[Platform-POR]	→←: Select Screen
Clock6 assignment	[Enabled]	↑ ↓: Select Item
ClkReq for Clock6	[Platform-POR]	Enter: Select
Clock7 assignment	[Enabled]	+/-: Change Opt.
ClkReq for Clock7	[Platform-POR]	F1: General Help
Clock8 assignment	[Enabled]	F2: Previous Values
ClkReq for Clock8	[Platform-POR]	F3: Optimized Defaults
Clock9 assignment	[Enabled]	F4: Save & Exit
ClkReq for Clock9	[Platform-POR]	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

Feature	Option	Description
Clock0..9 assignment	[Platform-POR], [Enabled], [Disabled]	[Platform-POR]: clock is assigned to PCIe port or LAN according to board layout. [Enabled]: keep clock enabled even if unused. [Disabled]: Disable clock.
ClkReq for Clock0..9	[Platform-POR], [Disabled]	[Platform-POR]: CLKREQ signal is assigned to CLKSRC according to board layout. [Disabled]: CLKREQ will not be used.

Figure 68: BIOS Chipset Setup Menu – PCH-IO Configuration – SATA Configuration

Aptio Setup – AMI		
Chipset		
SATA Configuration		
SATA Controller(s)	[Enabled]	
SATA Mode Selection*	[AHCI]	
SATA Test Mode*	[Disabled]	
Aggressive LPM Support*(1)	[Enabled]	
Serial ATA Port 0*	Empty	
Software Preserve*	Unknown	
Port 0*	[Enabled]	
Hot Plug*	[Disabled]	
Configured as eSATA*(3)	Hot Plug supported	
External*	[Disabled]	
Mechanical Presence Switch*(2)	[Disabled]	
Spin Up Device*	[Disabled]	
SATA Device Type*	[Hard Disk Drive]	
Topology*	[Unknown]	
SATA Port 0 DevSlp*	[Disabled]	
DITO Configuration*	[Disabled]	
DITO Value*(4)	625	
DM Value*(4)	15	
Serial ATA Port 1*	Empty	
Software Preserve*	Unknown	
Port 1*	[Enabled]	
Hot Plug*	[Disabled]	
Configured as eSATA*(3)	Hot Plug supported	
External*	[Disabled]	
Mechanical Presence Switch*(2)	[Disabled]	
Spin Up Device*	[Disabled]	
SATA Device Type*	[Hard Disk Drive]	
Topology*	[Unknown]	
SATA Port 1 DevSlp*	[Disabled]	
DITO Configuration*	[Disabled]	

Aptio Setup – AMI		
Chipset		
DITO Value*(4)	625	
DM Value*(4)	15	
Serial ATA Port 2*	Empty	
Software Preserve*	Unknown	
Port 2*	[Enabled]	
Hot Plug*	[Disabled]	
Configured as eSATA*(3)	Hot Plug supported	
External*	[Disabled]	→←: Select Screen
Mechanical Presence Switch*(2)	[Disabled]	↑ ↓: Select Item
Spin Up Device*	[Disabled]	Enter: Select
SATA Device Type*	[Hard Disk Drive]	+/-: Change Opt.
Topology*	[Unknown]	F1: General Help
SATA Port 2 DevSlp*	[Disabled]	F2: Previous Values
DITO Configuration*	[Disabled]	F3: Optimized Defaults
DITO Value*(4)	625	F4: Save & Exit
DM Value*(4)	15	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* These items appear only when enabling SATA Controller(s).

(1) This item appears only when disabling SATA Test Mode.

(2) This item appears only when enabling Hot Plug.

(3) This item appears only when disabling External.

(4) These items appear only when enabling DITO Configuration.

Feature	Option	Description
SATA Controller(s)	[Enabled], [Disabled]	Enable / Disable SATA Device.
SATA Mode Selection	[AHCI]	Determines how SATA controller(s) operate.
SATA Test Mode	[Enabled], [Disabled]	Test Mode Enable / Disable (Loop Back).
Aggressive LPM Support	[Disabled], [Enabled]	Enable PCH to aggressively enter link power state.
Port 0..2	[Disabled], [Enabled]	Enable or Disable SATA Port
Hot Plug	[Disabled], [Enabled]	Designates this port as Hot Pluggable.
External	[Disabled], [Enabled]	Marks this port as external.
Mechanical Presence Switch	[Disabled], [Enabled]	Controls reporting if this port has an Mechanical Presence Switch. Note: Requires hardware support.
Spin Up Device	[Disabled], [Enabled]	If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up

Feature	Option	Description
		at boot. Otherwise all drives spin up at boot.
SATA Device Type	[Hard Disk Drive], [Solid State Drive]	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	[Unknown], [ISATA], [Direct Connect], [Flex], [M2]	Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
SATA Port 0..2 DevSlp	[Disabled], [Enabled]	Enable / Disable SATA Port 0..2 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
DITO Configuration	[Disabled], [Enabled]	Enable / Disable DITO Configuration
DITO Value	Value input	DITO Value
DM Value	Value input	DM Value

Figure 69: BIOS Chipset Setup Menu – PCH-IO Configuration – USB Configuration

Aptio Setup – AMI		
Chipset		
USB Configuration		
xDCI Support	[Disabled]	
USB2 PHY Sus Well Power Gating	[Enabled]	
USB PDO Programming	[Enabled]	
USB Overcurrent	[Enabled]	
USB Overcurrent Lock	[Enabled]	
USB Audio Offload	[Enabled]	
Enable HSII on xHCI	[Enabled]	
USB3.1 Portx Speed Selection	0	
USB Port Disable Override	[Disabled]	
USB SW Device Mode Port #0*	[Disabled]	
USB SW Device Mode Port #1*	[Disabled]	
USB SW Device Mode Port #2*	[Disabled]	
USB SW Device Mode Port #3*	[Disabled]	
USB SW Device Mode Port #4*	[Disabled]	
USB SW Device Mode Port #5*	[Disabled]	
USB SW Device Mode Port #6*	[Disabled]	
USB SW Device Mode Port #7*	[Disabled]	
USB SW Device Mode Port #8*	[Disabled]	
USB SW Device Mode Port #9*	[Disabled]	

Aptio Setup – AMI		
Chipset		
USB SS Physical Connector #0*	[Enabled]	
USB SS Physical Connector #1*	[Enabled]	
USB SS Physical Connector #2*	[Enabled]	
USB SS Physical Connector #3*	[Enabled]	
USB HS Physical Connector #0*	[Enabled]	
USB HS Physical Connector #1*	[Enabled]	→ ←: Select Screen
USB HS Physical Connector #2*	[Enabled]	↑ ↓: Select Item
USB HS Physical Connector #3*	[Enabled]	Enter: Select
USB HS Physical Connector #4*	[Enabled]	+/-: Change Opt.
USB HS Physical Connector #5*	[Enabled]	F1: General Help
USB HS Physical Connector #6*	[Enabled]	F2: Previous Values
USB HS Physical Connector #7*	[Enabled]	F3: Optimized Defaults
USB HS Physical Connector #8*	[Enabled]	F4: Save & Exit
USB HS Physical Connector #9*	[Enabled]	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

* These items appear only when selecting Select Per-Pin for USB Port Disable Override.

Feature	Option	Description
xDCI	[Disabled], [Enabled]	Enable / Disable xDCI (USB OTG Device).
USB2 PHY Sus Well Power Gating	[Disabled], [Enabled]	Select 'Enabled' to enable SUS Well PG for USB2 PHY. This option has no effect on PCH-H.
USB PDO Programming	[Disabled], [Enabled]	Select 'Enabled' if Port Disable Override functionality is used.
USB Overcurrent	[Disabled], [Enabled]	Select 'Disabled' for pin-based debug. If pin-based debug is enabled but USB overcurrent is not disabled, USB DbC does not work.
USB Overcurrent Lock	[Disabled], [Enabled]	Select 'Disabled' if Overcurrent functionality is used. Enabling this will make xHCI controller consume the Overcurrent mapping date
USB Audio Offload	[Disabled], [Enabled]	Enable / Disable USB Audio Offload functionality
Enable HSII on xHCI	[Disabled], [Enabled]	Enable / Disable HSII feature. It may lead to increased power consumption.
USB3.1 Portx Speed Selection	Value input	Port Selection value in decimal for Gen1; Default – Gen2; Bit 0 corresponds to Port 0 and so on.
USB Port Disable Override	[Disabled], [Select Per-Pin]	Selectively Enable / Disable the corresponding USB port from reporting a Device Connection to the controller.
USB SW Device Mode Port #0..9	[Disabled], [Enabled]	Enable Connector Event for device subscription.
USB SS Physical Connector #0..3	[Disabled], [Enabled]	Enable / Disable this USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.
USB HS Physical	[Disabled],	Enable / Disable this USB Physical Connector (physical port).

Feature	Option	Description
Connector #0..9	[Enabled]	Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.

8.2.4. Security Setup Menu

The Security setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive. The 2.5"-SBC-AML/ADN provides no factory-set passwords.

NOTICE

If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing <ENTER>. To set a password, enter it twice and acknowledge by pressing <ENTER>.

Figure 70: BIOS Security Setup Menu

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
Password Description If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights The password length must be in the following range:					
Minimum Length		3		→ ←: Select Screen	
Maximum length		20		↑ ↓: Select Item	
				Enter: Select	
Administrator Password				+/-: Change Opt.	
User Password				F1: General Help	
				F2: Previous Values	
> Secure Boot				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
Version 2.22.1293 Copyright (C) 2025 AMI					

Feature	Description
Administrator Password	Set administrator password
User Password	Set user password

If only the administrator's password is set, then only access to setup is limited. The password is only entered when entering setup.

If only the user's password is set, then the password is a power on password and must be entered to boot or enter setup. Within the setup menu the user has administrator rights.

Password length requirements are maximum 20 characters and minimum 3 characters.

Figure 71: BIOS Security Setup Menu – Secure Boot

Aptio Setup – AMI		
Security		
System Mode	Setup	
Secure Boot	[Disabled]	→←: Select Screen
	Not Active	↑ ↓: Select Item
		Enter: Select
Secure Boot Mode	[Standard]	+/-: Change Opt.
> Restore Factory Keys*		F1: General Help
> Reset To Setup Mode*		F2: Previous Values
		F3: Optimized Defaults
> Key Management*		F4: Save & Exit
		ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

*These items are selectable only when selecting Custom for Secure Boot Mode.

Feature	Option	Description
Secure Boot	[Disabled], [Enabled]	Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset.
Secure Boot Mode	[Standard], [Custom]	Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.
Restore Factory Keys	[Yes], [No]	Force System to User Mode. Install factory default Secure Boot key databases.
Reset to Setup Mode	[Yes], [No]	Delete all Secure Boot key databases from NVRAM.

Figure 72: BIOS Security Setup Menu – Secure Boot – Key Management

Aptio Setup – AMI				
Security				
Vendor Keys		Valid		
Factory Key Provision		[Disabled]		
> Restore Factory Keys				
> Reset To Setup Mode				
> Enroll Efi Image				
> Export Secure Boot variables				→←: Select Screen
				↑ ↓: Select Item
Secure Boot variable	Size	Keys	Key Source	Enter: Select
> Platform Key (PK)	0	0	No Keys	+/-: Change Opt.
> Key Exchange Keys (KEK)	0	0	No Keys	F1: General Help
> Authorized Signatures (db)	0	0	No Keys	F2: Previous Values
> Forbidden Signatures (dbx)	0	0	No Keys	F3: Optimized Defaults
> Authorized TimeStamps (dbt)	0	0	No Keys	F4: Save & Exit
> OsRecovery Signatures (dbr)	0	0	No Keys	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI				

Feature	Option	Description
Factory Key Provision	[Disabled], [Enabled]	Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode.
Reset Factory Keys	[Yes], [No]	Force System to User Mode. Install factory default Secure Boot key databases.
Reset to Setup Mode	[Yes], [No]	Delete all Secure Boot key databases from NVRAM.
Enroll Efi Image	Select a File system	Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db).
Export Secure Boot variables	Select a File system	Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device.
Platform Key (PK)	[Details], [Export], [Update], [Delete]	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate: (a) EFI_SIGNATURE_LIST (b) EFI_CERT_X509 (DER) (c) EFI_CERT_RSA2048 (bin) (d) EFI_CERT_SHAXXX 2. Authenticated UEFI Variable 3. EFI PE / COFF Image (SHA256) Key Source: Factory, External, Mixed
Key Exchange Keys (KEK)	[Details], [Export], [Update], [Append], [Delete]	
Authorized Signatures (db)	[Details], [Export], [Update], [Append],	

Feature	Option	Description
	[Delete]	
Forbidden Signatures (dbx)	[Details], [Export], [Update], [Append], [Delete]	
Authorized TimeStamps (dbt)	[Update], [Append]	
OsRecovery Signatures (dbr)	[Update], [Append]	

8.2.4.1. Remember the password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords results in being locked out of the system.

If the system cannot be booted because the User Password or the Supervisor Password are not known, contact Kontron Support for further assistance.

HDD security passwords cannot be cleared using the above method.

8.2.5. Boot Setup Menu

The boot setup menu lists the for boot device priority order, that is generated dynamically.

Figure 73: BIOS Boot Setup Menu

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
Boot Configuration					
Setup Prompt Timeout		1			
Bootup NumLock State		[On]		→←: Select Screen	
Quiet Boot		[Disabled]		↑ ↓: Select Item	
				Enter: Select	
Boot Option Priorities				+/-: Change Opt.	
Boot Option #1		[UEFI: Built-in EFI Shell]		F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
Version 2.22.1293 Copyright (C) 2025 AMI					

Feature	Option	Description
Setup Prompt Timeout	Value Input	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	[On], [Off]	Select the keyboard NumLock state. [On]: The keys on the keypad will act as numeric keys. [Off]: The keys on the keypad will act as cursor keys.
Quiet Boot	[Disabled], [Enabled]	Enables or disables Quiet Boot option
Boot Option #1	[UEFI: Built-in EFI Shell], [Disabled]	Sets the system boot order

8.2.6. Save & Exit Setup Menu

The exit setup menu provides functions for handling changes made to the UEFI BIOS settings and the exiting of the setup program.

Figure 74: BIOS Save & Exit Setup Menu

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
Save Options					
Save Changes and Exit					
Discard Changes and Exit					
Save Changes and Reset					
Discard Changes and Reset					
Save Changes					
Discard Changes				→ ←: Select Screen	
				↑ ↓: Select Item	
Default Options				Enter: Select	
Restore Defaults				+/-: Change Opt.	
Save as User Defaults				F1: General Help	
Restore User Defaults				F2: Previous Values	
				F3: Optimized Defaults	
Boot Override				F4: Save & Exit	
UEFI: Built-in EFI Shell*				ESC: Exit	
Version 2.22.1293 Copyright (C) 2025 AMI					

* This item appears only when selecting UEFI: Built-in EFI Shell for Boot Option #1.

Feature	Description
Save Changes and Exit	Exit system setup after saving the changes.
Discard Changes and Exit	Exit system setup without saving any changes.
Save Changes and Reset	Reset the system after saving the changes.
Discard Changes and Reset	Reset system setup without saving any changes.
Save Changes	Save Changes done so far to any of the setup options.
Discard Changes	Discard Changes done so far to any of the setup options.
Restore Defaults	Restore / Load Default values for all the setup options.
Save as User Defaults	Save the changes done so far as User Defaults.
Restore User Defaults	Restore the User Defaults to all the setup options.
UEFI: Built-in EFI Shell	Save configuration and reset.

Appendix A: List of Acronyms

The following table does not contain the complete acronyms used in signal names, signal type definitions or similar. A description of the signals is included in the I/O Connector and Internal connector chapters within this user guide.

Table 38: List of Acronyms

2D	Two-Dimensional
3D	Three-Dimensional
AT	Advanced Technology
ATX	Advanced Technology eXtended
BGA	Ball Grid Array
BIOS	Basic Input / Output System
BSP	Board Support Package
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DC	Direct Current
DDC	Display Data Channel
DIO	Digital Input / Output
DP	DisplayPort
ECC	Error-Correcting Code
EEE	Electrical and Electronic Equipment
EOS	Electrical OverStress
ESD	ElectroStatic Discharge
GbE	Gigabit Ethernet
HDD	Hard Disk Drive
HDMI	High Definition Multimedia Interface
LAN	Local Area Network
LED	Light Emitting Device
LVDS	Low-Voltage Differential Signaling
ME F/W	Management Engine Firmware
mPCIe	mini Peripheral Component Interconnect express
NGFF	Next Generation Form Factor
PC-AT	Personal Computer - Advanced Technology
PCB	Printed Circuit Board
PSU	Power Supply Unit
PVC	PolyViny Chloride
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read-Only Memory
RTC	Real-Time Clock
SATA	Serial Advanced Technology Attachment
SD	Secure Digital memory card
SDP	Serial Download Protocol
SELV	Safety Extra-Low Voltage
SIM	Subscriber Identity Module
SMBus	System Management Bus
SoC	System on Chip
SO-DIMM	Small Outline Dual In-line Memory Module
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
TDP	Thermal Design Power
TPM	Trusted Platform Module
UEFI	Unified Extensible Firmware Interface
USB	Universal Serial Bus
UTP	Update Transfer Protocol
VGA	Video Graphics Array
WDT	WatchDog Timer
WEEE	Waste Electrical and Electronic Equipment

About Kontron

Kontron is a global leader in IoT / Embedded Computing Technology (ECT) and offers individual solutions in the areas of Internet of Things (IoT) and Industry 4.0 through a combined portfolio of hardware, software and services. With its standard and customized products based on highly reliable state-of-the-art technologies, Kontron provides secure and innovative applications for a wide variety of industries. As a result, customers benefit from accelerated time-to-market, lower total cost of ownership, extended product lifecycles and the best fully integrated applications.

For more information, please visit: **www.kontron.com**

Global Headquarters

Kontron Europe GmbH

Gutenbergstraße 2
85737 Ismaning
Germany
Tel.: + 49 821 4086-0
Fax: + 49 821 4086-111
info@kontron.com