

# Approval Sheet

|                       |                               |
|-----------------------|-------------------------------|
| Customer              |                               |
| Product Number        | M5R0-GGHZBC1S                 |
| Data Rate             | 6400 MT/s                     |
| Pin                   | 288 pin                       |
| Cl-tRCD-tRP           | 52-52-52                      |
| Operating temperature | Tc=0 to 95°C                  |
| Date                  | 5 <sup>th</sup> November 2025 |

The Total Solution For  
Industrial Flash Storage

Rev 1.0

## 1. Features

- JEDEC Standard 288-pin Registered Dual In-Line Memory Module
- VDD=VDDQ= 1.1V (1.067V ~ 1.166V)
- VPP=1.8V (1.746V ~ 1.908V)
- VDDSPD= 1.8V
- On-die, internal, adjustable VREF generation for DQ,CA,CS
- 16n-bit prefetch
- Two independent I/O sub channels
- Programmable /CAS Latency: 22,26,28,30,32,36,40,42,46,50,52,54,56
- tREFI 3.9us for 0°C ≤Tcase < 85°C, tREFI 1.95us for 85°C < Tcase ≤ 95°C
- On-Die ECC
- PMIC on DIMM, nominal supply 12V/2.5A, VIN\_Bulk input supply range: 4.25 V to 15 V
- Fly-by topology
- I3C/I2C support
- Terminated control and C/A bus
- SPD EEPROM Hub and Integrated Thermal Sensor
- Halogen-free

### Specification

| Density | Data Rate | IC Configuration | DIMM Organization | Number of IC | Number of rank | Side | ECC |
|---------|-----------|------------------|-------------------|--------------|----------------|------|-----|
| 48GB    | 6400 MT/s | 3Gx8 (24Gb)      | 6Gx64             | 20           | 2              | 2    | Y   |

### Key timing parameters

| tCK<br>(ns) | tRCD<br>(ns) | tRP<br>(ns) | tRAS<br>(ns) | tRC<br>(ns) |
|-------------|--------------|-------------|--------------|-------------|
| 0.312       | 16.00        | 16.00       | 32           | 48.00       |

### tRFC parameter by IC Configuration

| Parameter  | IC Configuration |      |      |      | Unit |
|------------|------------------|------|------|------|------|
|            | 8Gb              | 16Gb | 24Gb | 32Gb |      |
| tRFC1,min  | 195              | 295  | 410  | 410  | ns   |
| tRFC2,min  | 130              | 160  | 220  | 220  | ns   |
| tRFCsb,min | 115              | 130  | 190  | 190  | ns   |

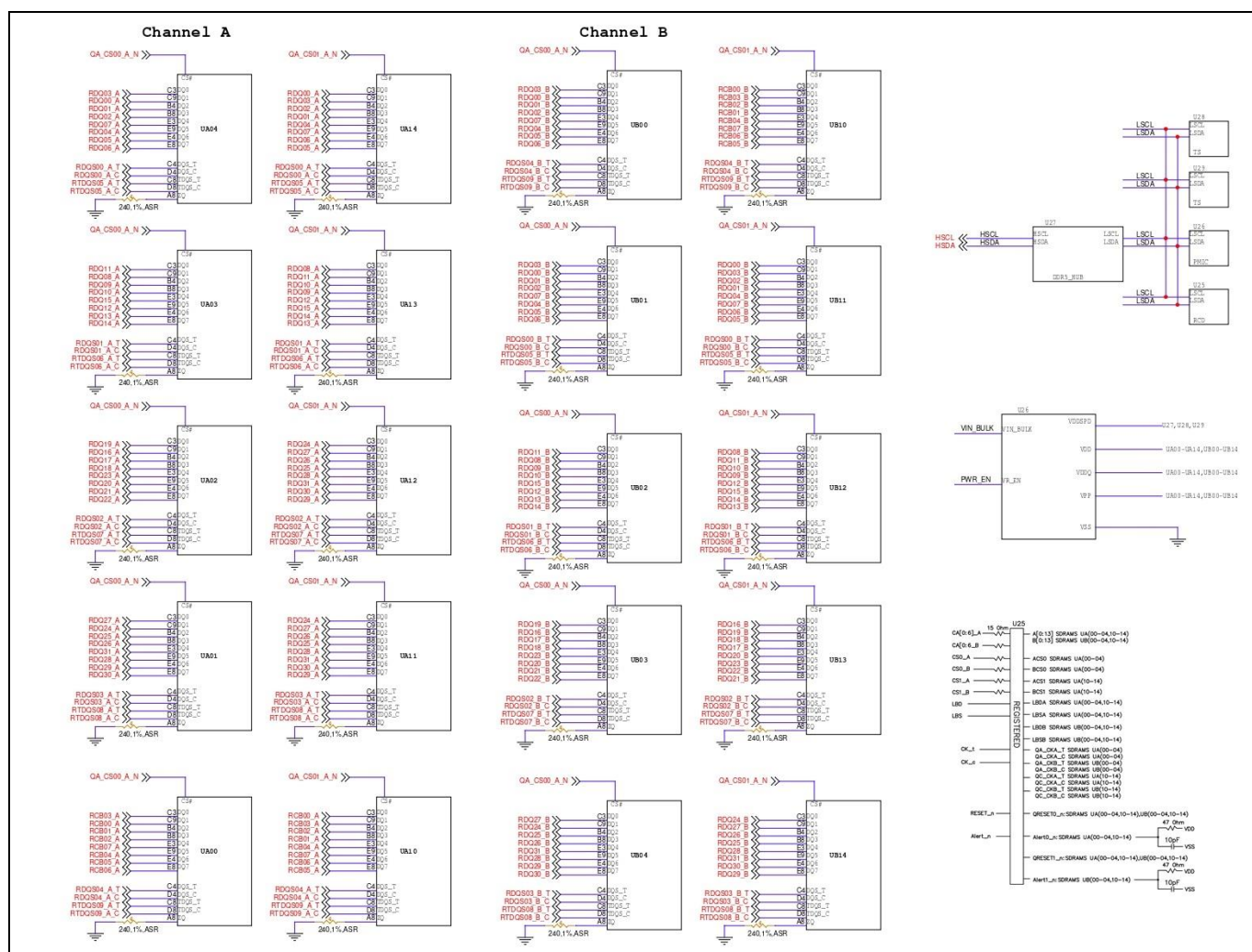
## 2. Pin Assignments

| 288-Pin DDR5 RDIMM Front |          |     |          |     |                              |     |          | 288-Pin DDR5 RDIMM Back |                                          |     |                     |     |                     |     |                     |
|--------------------------|----------|-----|----------|-----|------------------------------|-----|----------|-------------------------|------------------------------------------|-----|---------------------|-----|---------------------|-----|---------------------|
| Pin                      | Symbol   | Pin | Symbol   | Pin | Symbol                       | Pin | Symbol   | Pin                     | Symbol                                   | Pin | Symbol              | Pin | Symbol              | Pin | Symbol              |
| 1                        | VIN_BULK | 37  | Vss      | 73  | Vss                          | 109 | DQ5_B    | 145                     | VIN_BULK                                 | 181 | DQ22_A              | 217 | CK_t                | 253 | Vss                 |
| 2                        | RFU      | 38  | DQ21_A   | 74  | PAR_A                        | 110 | Vss      | 146                     | VIN_BULK                                 | 182 | Vss                 | 218 | CK_c                | 254 | DQ7_B               |
| 3                        | VIN_MGMT | 39  | Vss      | 75  | Vss                          | 111 | DQ8_B    | 147                     | PWR_GOOD_FAULT_n                         | 183 | DQ23_A              | 219 | Vss                 | 255 | Vss                 |
| 4                        | SCL      | 40  | DQ24_A   | 76  | CA0_B                        | 112 | Vss      | 148                     | SAA                                      | 184 | Vss                 | 220 | RFU                 | 256 | DQ10_B              |
| 5                        | SDA      | 41  | Vss      | 77  | Vss                          | 113 | DQ9_B    | 149                     | RFU                                      | 185 | DQ26_A              | 221 | CA1_B               | 257 | Vss                 |
| 6                        | Vss      | 42  | DQ25_A   | 78  | CA2_B                        | 114 | Vss      | 150                     | RFU                                      | 186 | Vss                 | 222 | Vss                 | 258 | DQ11_B              |
| 7                        | DQ0_A    | 43  | Vss      | 79  | Vss                          | 115 | DQS1_B_t | 151                     | Vss                                      | 187 | DQ27_A              | 223 | CA3_B               | 259 | Vss                 |
| 8                        | Vss      | 44  | DQS3_A_t | 80  | CA4_B                        | 116 | DQS1_B_c | 152                     | DQ2_A                                    | 188 | Vss                 | 224 | Vss                 | 260 | DQS6_B_c, TDQS6_B_c |
| 9                        | DQ1_A    | 45  | DQS3_A_c | 81  | Vss                          | 117 | Vss      | 153                     | Vss                                      | 189 | DQS8_A_c, TDQS8_A_c | 225 | CA5_B               | 261 | DQS6_B_t, TDQS6_B_t |
| 10                       | Vss      | 46  | Vss      | 82  | CA6_B                        | 118 | DQ12_B   | 154                     | DQ3_A                                    | 190 | DQS8_A_t, TDQS8_A_t | 226 | Vss                 | 262 | Vss                 |
| 11                       | DQS0_A_t | 47  | DQ28_A   | 83  | Vss                          | 119 | Vss      | 155                     | Vss                                      | 191 | Vss                 | 227 | PAR_B               | 263 | DQ14_B              |
| 12                       | DQS0_A_c | 48  | Vss      | 84  | CS0_B_n                      | 120 | DQ13_B   | 156                     | DQS5_A_c, TDQS5_A_c, DQS5_A_t, TDQS5_A_t | 192 | DQ30_A              | 228 | Vss                 | 264 | Vss                 |
| 13                       | Vss      | 49  | DQ29_A   | 85  | Vss                          | 121 | Vss      | 157                     | DQS5_A_t, TDQS5_A_t                      | 193 | Vss                 | 229 | CS1_B_n             | 265 | DQ15_B              |
| 14                       | DQ4_A    | 50  | Vss      | 86  | LBDRSP_A_n                   | 122 | DQ16_B   | 158                     | Vss                                      | 194 | DQ31_A              | 230 | Vss                 | 266 | Vss                 |
| 15                       | Vss      | 51  | CB0_A    | 87  | LBDRSP_B_n                   | 123 | Vss      | 159                     | DQ6_A                                    | 195 | Vss                 | 231 | RFU                 | 267 | DQ18_B              |
| 16                       | DQ5_A    | 52  | Vss      | 88  | Vss                          | 124 | DQ17_B   | 160                     | Vss                                      | 196 | CB2_A               | 232 | RFU                 | 268 | Vss                 |
| 17                       | Vss      | 53  | CB1_A    | 89  | CB4_B                        | 125 | Vss      | 161                     | DQ7_A                                    | 197 | Vss                 | 233 | Vss                 | 269 | DQ19_B              |
| 18                       | DQ8_A    | 54  | Vss      | 90  | Vss                          | 126 | DQS2_B_t | 162                     | Vss                                      | 198 | CB3_A               | 234 | CB6_B               | 270 | Vss                 |
| 19                       | Vss      | 55  | DQS4_A_t | 91  | CB5_B                        | 127 | DQS2_B_c | 163                     | DQ10_A                                   | 199 | Vss                 | 235 | Vss                 | 271 | DQS7_B_c, TDQS7_B_c |
| 20                       | DQ9_A    | 56  | DQS4_A_c | 92  | Vss                          | 128 | Vss      | 164                     | Vss                                      | 200 | DQS9_A_c, TDQS9_A_c | 236 | CB7_B               | 272 | DQS7_B_t, TDQS7_B_t |
| 21                       | Vss      | 57  | Vss      | 93  | DQS9_B_t, TDQS9_B_t, DBW_B_n | 129 | DQ20_B   | 165                     | DQ11_A                                   | 201 | DQS9_A_t, TDQS9_A_t | 237 | Vss                 | 273 | Vss                 |
| 22                       | DQS1_A_t | 58  | CB4_A    | 94  | DQS9_B_c, TDQS9_B_c          | 130 | Vss      | 166                     | Vss                                      | 202 | Vss                 | 238 | DQS4_B_c            | 274 | DQ22_B              |
| 23                       | DQS1_A_c | 59  | Vss      | 95  | Vss                          | 131 | DQ21_B   | 167                     | DQS6_A_c, TDQS6_A_c, DQS6_A_t, TDQS6_A_t | 203 | CB6_A               | 239 | DQS4_B_t            | 275 | Vss                 |
| 24                       | Vss      | 60  | CB5_A    | 96  | CB0_B                        | 132 | Vss      | 168                     | DQS6_A_t, TDQS6_A_t                      | 204 | Vss                 | 240 | Vss                 | 276 | DQ23_B              |
| 25                       | DQ12_A   | 61  | Vss      | 97  | Vss                          | 133 | DQ24_B   | 169                     | Vss                                      | 205 | CB7_A               | 241 | CB2_B               | 277 | Vss                 |
| 26                       | Vss      | 62  | ALERT_n  | 98  | CB1_B                        | 134 | Vss      | 170                     | DQ14_A                                   | 206 | Vss                 | 242 | Vss                 | 278 | DQ26_B              |
| 27                       | DQ13_A   | 63  | Vss      | 99  | Vss                          | 135 | DQ25_B   | 171                     | Vss                                      | 207 | RESET_n             | 243 | CB3_B               | 279 | Vss                 |
| 28                       | Vss      | 64  | CS0_A_n  | 100 | DQ0_B                        | 136 | Vss      | 172                     | DQ15_A                                   | 208 | Vss                 | 244 | Vss                 | 280 | DQ27_B              |
| 29                       | DQ16_A   | 65  | Vss      | 101 | Vss                          | 137 | DQS3_B_t | 173                     | Vss                                      | 209 | CS1_A_n             | 245 | DQ2_B               | 281 | Vss                 |
| 30                       | Vss      | 66  | CA0_A    | 102 | DQ1_B                        | 138 | DQS3_B_c | 174                     | DQ18_A                                   | 210 | Vss                 | 246 | Vss                 | 282 | DQS8_B_c, TDQS8_B_c |
| 31                       | DQ17_A   | 67  | Vss      | 103 | Vss                          | 139 | Vss      | 175                     | Vss                                      | 211 | CA1_A               | 247 | DQ3_B               | 283 | DQS8_B_t, TDQS8_B_t |
| 32                       | Vss      | 68  | CA2_A    | 104 | DQS0_B_t                     | 140 | DQ28_B   | 176                     | DQ19_A                                   | 212 | Vss                 | 248 | Vss                 | 284 | Vss                 |
| 33                       | DQS2_A_t | 69  | Vss      | 105 | DQS0_B_c                     | 141 | Vss      | 177                     | Vss                                      | 213 | CA3_A               | 249 | DQS5_B_c, TDQS5_B_c | 285 | DQ30_B              |
| 34                       | DQS2_A_c | 70  | CA4_A    | 106 | Vss                          | 142 | DQ29_B   | 178                     | DQS7_A_c, TDQS7_A_c                      | 214 | Vss                 | 250 | DQS5_B_t, TDQS5_B_t | 286 | Vss                 |
| 35                       | Vss      | 71  | Vss      | 107 | DQ4_B                        | 143 | Vss      | 179                     | DQS7_A_t, TDQS7_A_t                      | 215 | CA5_A               | 251 | Vss                 | 287 | DQ31_B              |
| 36                       | DQ20_A   | 72  | CA6_A    | 108 | Vss                          | 144 | RFU      | 180                     | Vss                                      | 216 | Vss                 | 252 | DQ6_B               | 288 | Vss                 |

### 3. Pin Descriptions

| Symbol                     | Type             | I/O Level | Description                      | Symbol                         | Type             | I/O Level | Description                 |
|----------------------------|------------------|-----------|----------------------------------|--------------------------------|------------------|-----------|-----------------------------|
| CK_t, CK_c                 | Input            | VDDQ      | Clock                            | DQ[31:0]_A<br>DQ[31:0]_B       | Input/<br>Output | VDDQ      | Data Input/Output           |
| CA[6:0]_A<br>CA[6:0]_B     | Input            | VDDQ      | Command/Address Inputs           | CB[7:0]_A<br>CB[7:0]_B         | Input/<br>Output | VDDQ      | ECC Check Bits Input/Output |
| CS[1:0]_A<br>CS[1:0]_B     | Input            | VDDQ      | Chip Select                      | DQS[9:0]_A_t<br>DQS[9:0]_B_t   | Input/<br>Output | VDDQ      | Data Strobe                 |
| PAR_A<br>PAR_B             | Input            | VDDQ      | Command and Address Parity Input | DQS[9:0]_A_c<br>DQS[9:0]_B_c   | Input/<br>Output | VDDQ      | Data Strobe                 |
| ALERT_n                    | Output           | VDDQ      | Alert                            | TDQS[9:0]_A_t<br>TDQS[9:0]_B_t | Input/<br>Output | VDDQ      | Termination Data Strobe     |
| RESET_n                    | CMOS<br>Input    | VDDQ      | Active Low Asynchronous Reset    | TDQS[9:0]_A_c<br>TDQS[9:0]_B_c | Input/<br>Output | VDDQ      | Termination Data Strobe     |
| PWR_GOOD/FAI<br>L_n        | Input/<br>Output | VDDQ      | Power Good Indicator             | VIN_BULK                       | Supply           |           | External Power Supply       |
| DM[3:0]_A_n<br>DM[3:0]_B_n | Input            | VDDQ      | Input Data Mask                  | VIN_MGMT                       | Supply           |           | External Power Supply       |
| HSCL                       | Input            | VOUT      | Host Sideband Bus Clock          | LBD<br>RSP_A_n                 | Output           | VDDQ      | Loopback data output        |
| HSDA                       | Input/Output     | VOUT      | Host Sideband Bus Data           | LBS                            | Output           | VDDQ      | Loopback data strobe output |
| HSA                        | Input            | GND       | Host Sideband Bus Device ID      | VSS                            | Supply           |           | Ground                      |
| RFU                        |                  |           | Reserved for future use          |                                |                  |           |                             |

#### 4. Function Block Diagram



## 5. Thermal Characteristics

| Symbol           | Parameter             |                        | Rating     | Units | Note    |
|------------------|-----------------------|------------------------|------------|-------|---------|
| T <sub>C</sub>   | Operation Temperature | Normal Operating Temp. | 0 to 85    | °C    | 1,2,3   |
|                  |                       | Extended Temp.         | 85 to 95   | °C    | 1,2,3,4 |
| T <sub>STG</sub> | Storage Temperature   |                        | -55 to 100 | °C    | 5       |

**Note:**

- Maximum operating case temperature; T<sub>C</sub> is measured in the center of the package.
- A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T<sub>C</sub> during operation.
- Device functionality is not guaranteed if the DRAM device exceeds the maximum T<sub>C</sub> during operation.
- If T<sub>C</sub> exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95μs interval refresh rate.
- Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

## 6. IDD, IDDQ and IPP Specifications

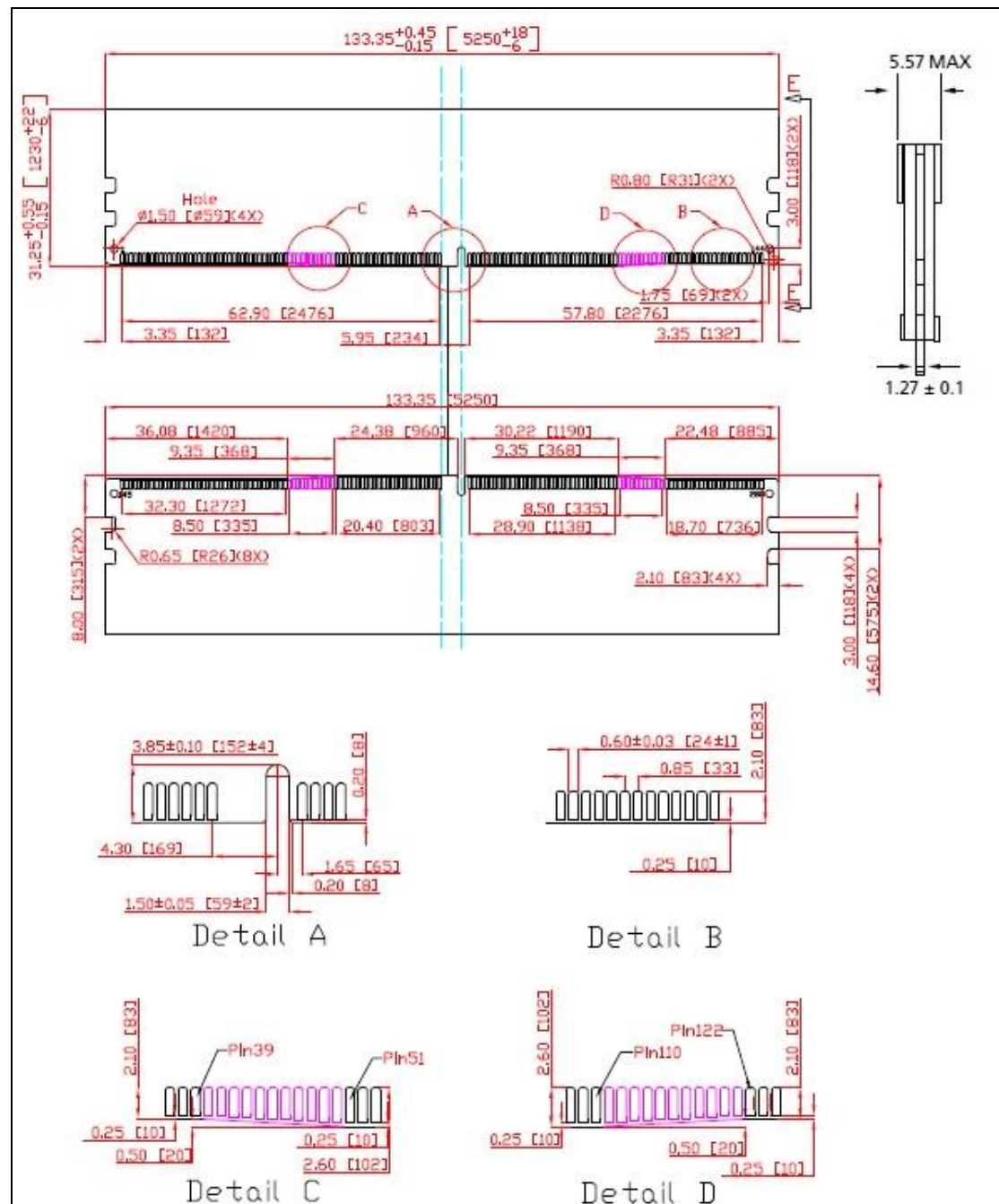
| Symbol | Description                                      | Value    |          | Units |
|--------|--------------------------------------------------|----------|----------|-------|
|        |                                                  | IDD Max. | IPP Max. |       |
| IDD0   | Operating One Bank Active-Precharge Current      | 1490     | 140      | mA    |
| IDD0F  | Operating Four Bank Active-Precharge Current     | 1850     | 230      | mA    |
| IDD2N  | Precharge Standby Current                        | 1360     | 120      | mA    |
| IDD2P  | Precharge Power-Down Current                     | 1160     | 100      | mA    |
| IDD3N  | Active Standby Current                           | 2440     | 300      | mA    |
| IDD3P  | Active Power-Down Current                        | 2880     | 280      | mA    |
| IDD4R  | Operating Burst Read Current                     | 3840     | 250      | mA    |
| IDD4W  | Operating Burst Write Current                    | 4050     | 280      | mA    |
| IDD5B  | Burst Refresh Current (Normal Refresh Mode)      | 3410     | 560      | mA    |
| IDD5C  | Burst Refresh Current (Same Bank Refresh Mode)   | 1940     | 230      | mA    |
| IDD6E  | Self Refresh Current: Extended Temperature Range | 1580     | 260      | mA    |
| IDD7   | Operating Bank Interleave Read Current           | 4560     | 660      | mA    |
| IDD8   | Maximum Power Saving Deep Power Down Current     | 840      | 100      | mA    |

The above information may be change due to the update of the device specifications and is for reference only.

## 7. Timing Parameters

| Parameter                                                                                                 | Symbol     | 6400                        |     | Unit |
|-----------------------------------------------------------------------------------------------------------|------------|-----------------------------|-----|------|
|                                                                                                           |            | Min                         | Max |      |
| Clock Timing                                                                                              |            |                             |     |      |
| Average clock period                                                                                      | tCK_AVG    | 0.312                       | -   | ns   |
| Command and Address Timing                                                                                |            |                             |     |      |
| Read to Read command delay for same bank group                                                            | tCCD_L     | 8nCK,<br>5ns<br>(MAX)       | -   | nCK  |
| WRITE to WRITE command delay for same bank group                                                          | tCCD_L_WR  | 32nCK,<br>20ns<br>(MAX)     | -   | nCK  |
| WRITE to WRITE command delay for same bank group, second WRITE not RMW                                    | tCCD_L_WR2 | 16nCK,<br>10ns<br>(MAX)     | -   | nCK  |
| Read to Read or Write to Write command delay for different bank group for BL16, BC8 OTF                   | tCCD_S     | 8                           | -   | nCK  |
| ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size                              | tRRD_S,2K  | 8                           | -   | nCK  |
| ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size                              | tRRD_S,1K  | 8                           | -   | nCK  |
| ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size                                   | tRRD_L,2K  | 8nCK,<br>5ns<br>(MAX)       | -   | nCK  |
| ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size                                   | tRRD_L,1K  | 8nCK,<br>5ns<br>(MAX)       | -   | nCK  |
| Four activate window for 2KB page size                                                                    | tFAW,2K    | 40nCK,<br>12.500ns<br>(MAX) | -   | ns   |
| Four activate window for 1KB page size                                                                    | tFAW,1K    | 32nCK,<br>10.000ns<br>(MAX) | -   | ns   |
| Delay from start of internal WRITE transaction to internal READ command for different bank group          | tWTR_S     | 2.5                         | -   | ns   |
| Delay from start of internal WRITE transaction to internal READ command for same bank group               | tWTR_L     | 10                          |     | ns   |
| Delay from start of internal WRITE transaction to internal READ with AUTO PRECHARGE command for same bank | tWTRA      | tWR-tRTP                    | -   | ns   |
| Internal READ command to PRECHARGE command delay                                                          | tRTP       | 7.5                         | -   | ns   |
| PRECHARGE to PRECHARGE delay                                                                              | tPPD       | 2                           | -   | nCK  |
| WRITE recovery time                                                                                       | tWR        | 30                          | -   | ns   |

## 8. Module Dimensions



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of  $\pm 0.15$  (6), unless otherwise specified.

## 9. RoHS Declaration

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Innodisk Corporation

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Tel: (02) 7703-3000 Internet: <https://www.innodisk.com/>

## RoHS 自我宣告書 (RoHS Declaration of Conformity)

## Manufacturer Products: All Innodisk EM FLASH, DRAM and EP products

- 一、宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及 (EU) 2015/863 關於 RoHS 之規範要求。  
Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.
- 二、本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。  
Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.
- 三、本公司聲明我們的產品符合 RoHS 指令的附件中 7(a)、7(c)-I、6(c) 允許豁免。  
We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.
- ※ 7(a) Lead in high melting temperature type solders (i.e. lead-based alloys containing 85% by weight or more lead).
- ※ 7(c)-I Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.
- ※ 6(c) Copper alloy containing up to 4% lead by weight. (This exemption applies to products that use antennas)

| Name of hazardous substance | Limited of RoHS ppm (mg/kg) |
|-----------------------------|-----------------------------|
| 鉛 (Pb)                      | < 1000 ppm                  |
| 汞 (Hg)                      | < 1000 ppm                  |
| 鎘 (Cd)                      | < 100 ppm                   |
| 六價鉻 (Cr 6+)                 | < 1000 ppm                  |
| 多溴聯苯 (PBBs)                 | < 1000 ppm                  |
| 多溴二苯醚 (PBDEs)               | < 1000 ppm                  |
| 鄰苯二甲酸二(2-乙基己基)酯 (DEHP)      | < 1000 ppm                  |
| 鄰苯二甲酸丁酯苯甲酯 (BBP)            | < 1000 ppm                  |
| 鄰苯二甲酸二丁酯 (DBP)              | < 1000 ppm                  |
| 鄰苯二甲酸二異丁酯 (DIBP)            | < 1000 ppm                  |

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宜鼎國際股份有限公司

Innodisk Corporation

立 保 證 書 人 (Guarantor)

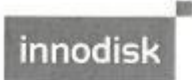
Company name 公司名稱：Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人：簡川勝

Company Representative Title 公司代表人職稱：Chairman 董事長

Date 日期：2023 / 06 / 14

## 10. REACH Declaration

|                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                                                                                          | <p>宜鼎國際股份有限公司<br/>Innodisk Corporation<br/>REACH Declaration</p> <p>Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: <a href="https://www.innodisk.com/">https://www.innodisk.com/</a></p> <p>Innodisk Corporation pursues its social responsibility for global environmental preservation by committing to be compliant with REACH regulation (REGULATION (EC) No 1907/2006). We hereby confirm that the product(s),</p> <p><b>Scope: Flash Memory, DRAM Module and Embedded Peripherals Products.</b></p> <p>■ The standard products of <b>not listed in the <u>Appendix2</u></b> meet the requirements of REACH SVHC regulations(SVHCs &lt; 0.1% in Article), as described in the candidate list table currently including 240 substances (release date: 23-JAN-2024) and shown on the ECHA website. <a href="https://echa.europa.eu/candidate-list-table">https://echa.europa.eu/candidate-list-table</a></p> <p>■ The standard products listed in the <b><u>Appendix2</u></b> contain(s) one or more hazardous substances or constituents exceeding 0.1 % by weight in article if not otherwise specified in candidate list table.</p> <p>Where the threshold value is exceeded, the substances in question are to be declared in accompanying. (SVHCs &gt; 0.1% in Article).</p> <p>■ Comply with REACH Annex XVII.</p> |
| <p style="text-align: center;"><b>Guarantor</b></p> <p>Company name 公司名稱: <u>Innodisk Corporation 宜鼎國際股份有限公司</u></p> <p>Company Representative 公司代表人: <u> Yichuan Chen 陳怡全</u></p> <p>Company Representative Title 公司代表人職稱: <u>Quality Assurance Div. SR. Manager 品質處經理</u></p> <p>Date 日期: <u>2024 / 02 / 19</u></p> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

## Revision Log

| Rev | Date                      | Modification        |
|-----|---------------------------|---------------------|
| 0.1 | 8 <sup>th</sup> July 2025 | Preliminary Edition |
| 1.0 | 8 <sup>th</sup> July 2025 | Official released   |