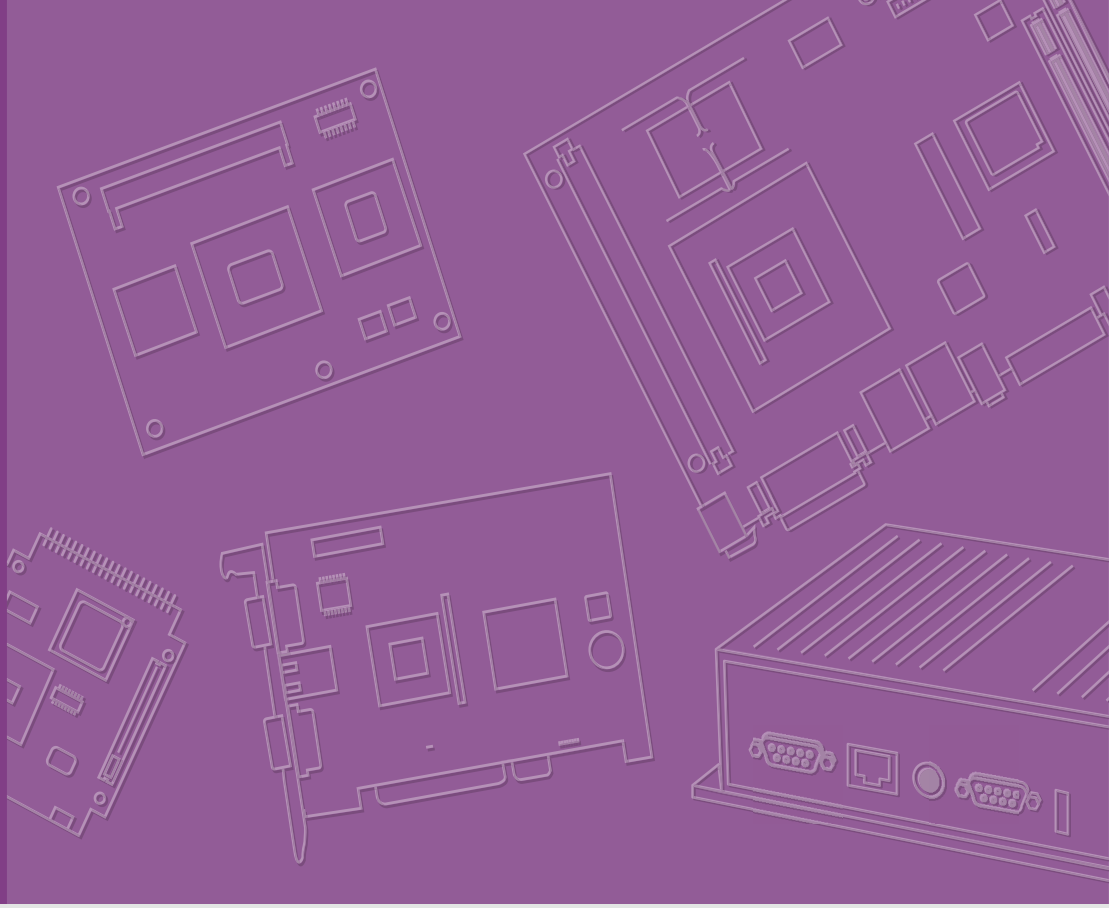

User Manual

ASR-A502

Intel® Core™ Ultra U/H-series 3.5" SBC

ADVANTECH

Enabling an Intelligent Planet

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Acknowledgments

For more information on this and other Advantech products, please visit our website at:
http://www.advantech.com

For technical support and service, please visit our support website at:
http://support.advantech.com/

This manual is for the ASR-A502.

Part No. 2006A50201 Edition 2
Printed in Taiwan October 2025

Product Warranty (2 Years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced free of charge during the warranty period. For out-of-warranty repairs, customers will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details.

If you believe your product to be defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

Declaration of Conformity

CE

This product has passed the CE test for environmental specifications. Test conditions for passing include the equipment being operated within an industrial enclosure. In order to protect the product from damage caused by electrostatic discharge (ESD) or EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

Technical Support and Assistance

1. Visit the Advantech website at www.advantech.com/support to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

- 1 x ASR-A502 SBC
- 1 x USB 2.0 cable 20 cm (P/N: 1700030406-01)
- 4 x COM RS-232 cable 20 cm (P/N: 1700031582-01)
- 1 x cooler 1970005512T001
- 1 x screw kit (4 sets of screws for an M.2 device)
- 1 x DeviceOn Package

Optional Accessories

- 1 x heat spreader for the ASR-A502 (P/N: 1970005998T001)
- 2P Phoenix to DC jack power cable (P/N: 1700009001)
- 4-wire COM RS-422/485 cables (P/N: 1700035016-01)
- CAN bus cable D-SUB 9P 15 cm (P/N: 1700030518-01)

Contents

Chapter 1

General Information

1.1 Introduction

The ASR-A502 is powered by Intel® Core™ Ultra H/U series processors featuring a hybrid core architecture for enhanced CPU performance, graphics, security, and I/O flexibility. It also integrates Advantech's embedded tools—including iManager 3.0, SUSI 4.0, and WISE-PaaS/DeviceOn—enabling efficient remote monitoring and control of system operations

1.2 Specifications

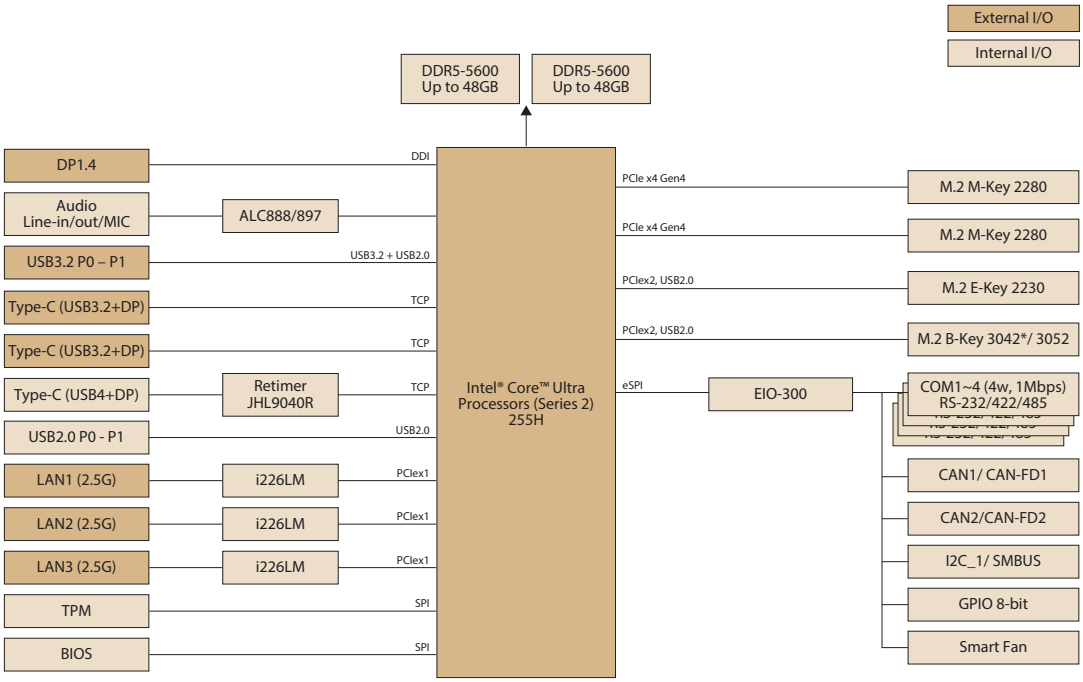
Table 1.1: Specifications

Platform	**Processor**	255H
	Max. Frequency	5.1 GHz
	Base Frequency (P-Core)	2 GHz
	Cores/Threads	16C, 6P+8E+2LE/ 16T
	LLC	24MB
	CPU TDP	28W
	Chipset	On-package Intel 600 Series Chipset
	BIOS	AMI EFI 256Mbit
Memory	**Technology**	DDR5-5600
	Max. Capacity	96GB
	Channel/Socket	Dual Channels / 2 Sockets
Graphics	**Controller**	Intel® Arc™ 140T GPU
	Max. Frequency	2.25 GHz
	GPU TOPS (Int8)	74 TOPS
	3D/HW Acceleration	DX12.2, OGL4.6, OCL3.0, HW encode/ decode: H.265 (HEVC), H.264, AV1, VP9
NPU	**Name**	Intel® AI Boost
	TOPS (Int8)	13 TPOS
Display I/F	**DisplayPort**	1 x DP 1.4a, up to 4096 x 2160 x 36bpp @60Hz
Ethernet	**Controller**	LAN1~3: Intel i226LM
	Speed	LAN1~3: 2.5GbE
Expansion	**M.2 E-Key**	1 x E-Key 2230 (PCIe x2, USB 2.0)
	M.2 B-Key	1 x B-Key 3042*/3052 (PCIe x2 / SATA, USB 2.0) with NanoSIM
	M.2 M-Key	2 x M-Key 2280 (PCIe x4 Gen.4 NVMe)
External I/O	**Ethernet**	3 x RJ-45
	DP	1
	USB Type-C	2 x USB 3.2 Gen2 x1 10Gbps, support DisplayPort 1.4 Alt. Mode
	USB Type-A	2 x USB 3.2 Gen2 x1 10Gbps
	Power Connector	2-pin Phoenix connector, optional 4-pin ATX connector

Table 1.1: Specifications		
Internal I/O	**USB4**	1 x USB4 with USB Type-C, bandwidth min. 20Gbps, max. 40Gbps, with USB4/ Display/ PCIe
	USB 2.0	2
	COM Port	4 x RS-232/422/485, max. 1Mbps
	CAN Bus	2 x CAN-FD
	Serial Bus	1 x I2C / SMBus
	Audio	Realtek ALC888s, Line-in/Line-out/MIC
	GPIO	8-bit general purpose input output I/O
	Fan	12V, 1A (4-wire)
	Front Panel Control	Power-on, Reset, Buzzer, CaseOpen
Board Features	**Watchdog Timer**	65536 level, 0~65535 sec
	TPM	Discrete TPM 2.0, fTPM* support by request
	SUSI	SW API for Hardware Monitor, Smart Fan Control, I2C, GPIO, WDT
Power	**Supply Voltage**	Vin: DC 12V~24V ± 10%; RTC Battery: Lithium 3V/210mAH
	Connector	2P Phoenix, optional to ATX 2x2-pin
	Power Management	AT (default), ATX
	Max. Consumption	155.16 (12V)/188.35 (24V)
	Idle Consumption	13.90 (12V)/15.55 (24V)
Environ-ment	**Temperature**	Operating: 0 ~ 60°C (32 ~ 140°F) Storage: -40 ~ 85°C (-40 ~ 185°F)
	Humidity	Operating: 40°C @ 95% relative humidity, non-condensing Storage: 60°C @ 95% relative humidity, non-condensing
	Vibration Resistance	3.5 Grms
Certification	**EMC**	CE, FCC Class B
Mechanical	**Dimensions**	146 x 102 mm (5.7 x 4")
	Net Weight	170 g

*Note: Supported by request.

1.3 Block Diagram



Chapter 2

Mechanical Specifications

2.1 Introduction

The compact form factor SBC is a new-generation SBC designed with a variety of mechanical improvements. This chapter includes board dimensions and assembly instructions for the standard thermal solution.

2.2 Board Layout: Dimensions

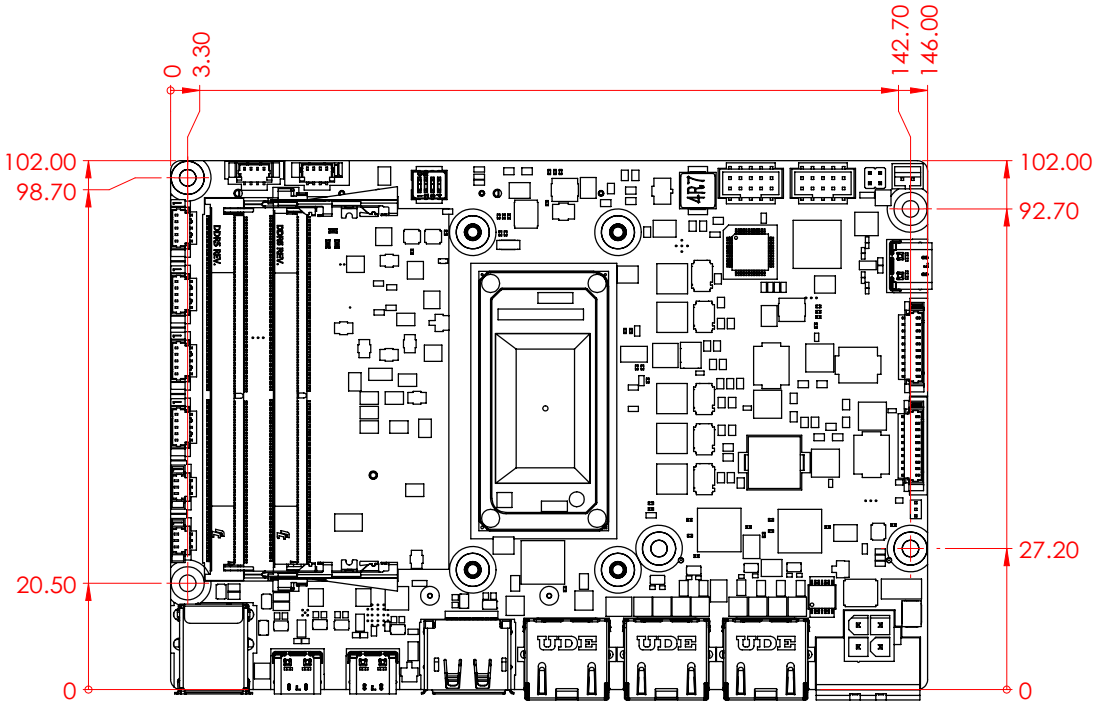


Figure 2.1 ASR-A502 Mechanical Diagram (Top Side)

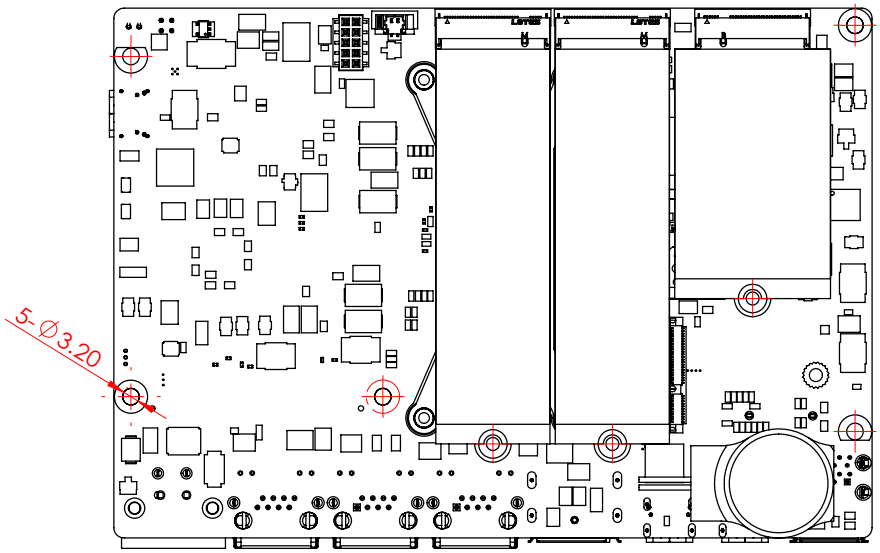


Figure 2.2 ASR-A502 Mechanical Diagram (Bottom Side)

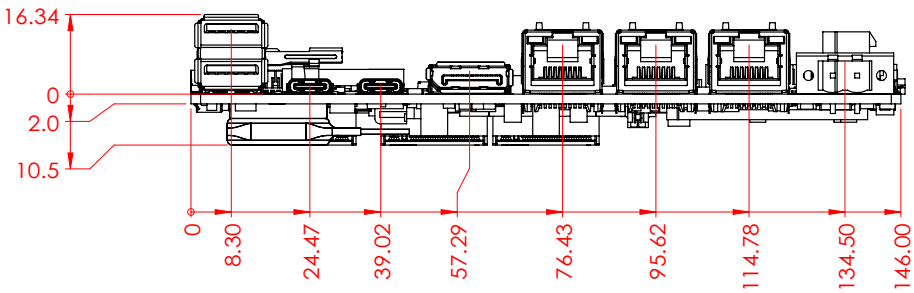


Figure 2.3 ASR-A502 Mechanical Diagram

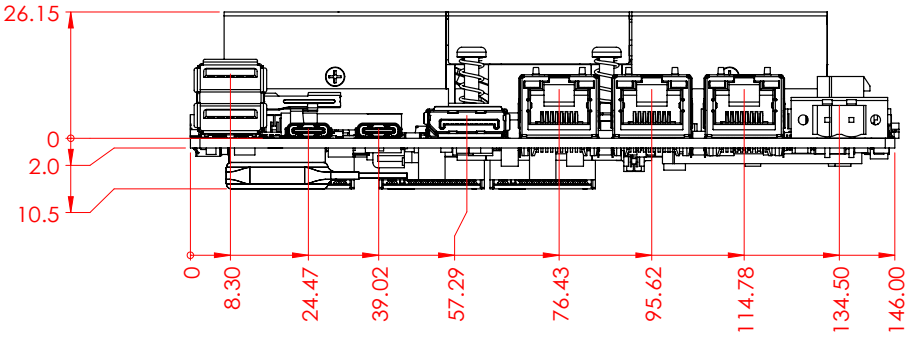


Figure 2.4 ASR-A502 Mechanical Diagram (with Cooler)

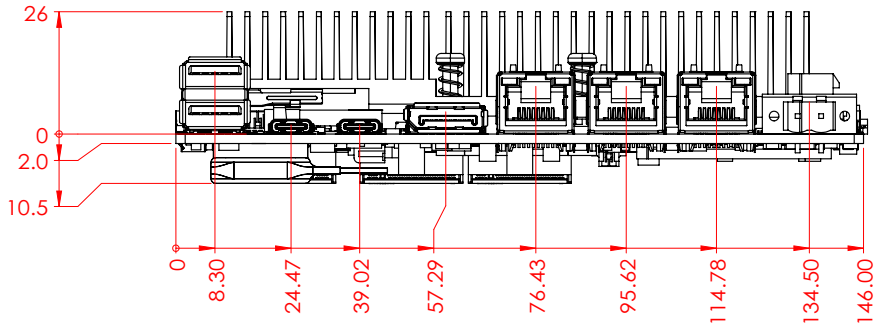


Figure 2.5 ASR-A502 Mechanical Diagram (with Heatsink)

Chapter 3

Jumpers and Connectors

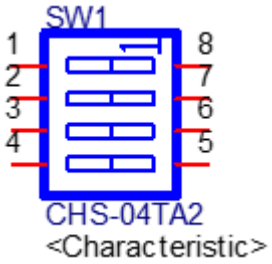
3.1 Jumper & Switches

The ASR-A502 has a number of jumpers that allow you to configure your system to suit your application. The table below lists the functions of the various jumpers.

3.1.1 Miscellaneous Selection Jumper: SW1

Table 3.1: Miscellaneous Selection Jumper: SW1

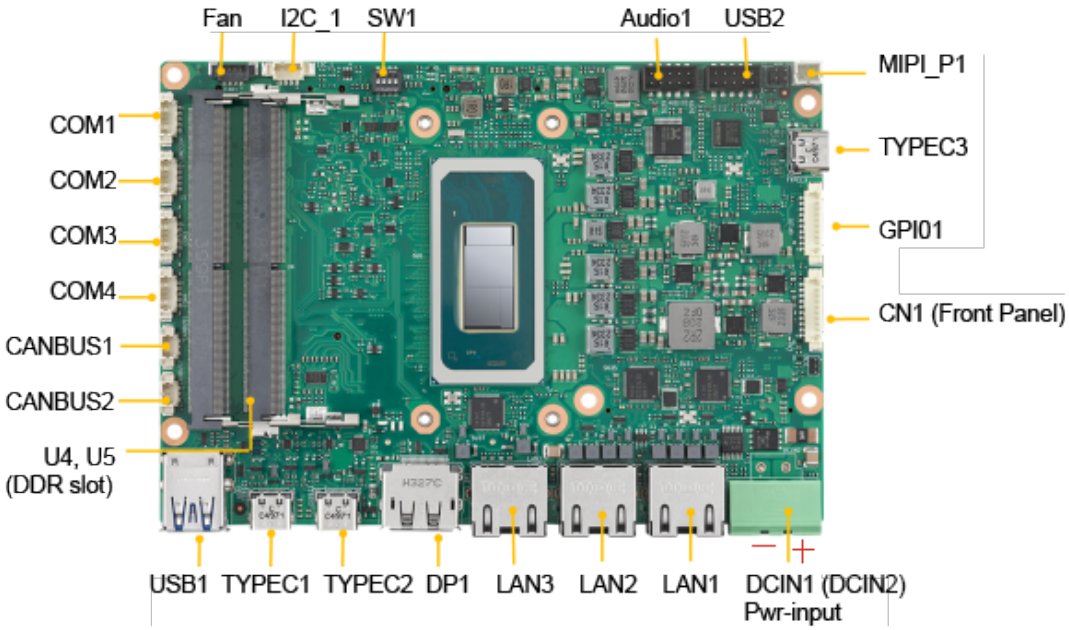
Jumper Short	Panel Functional
1	ATX_DET
2	LOAD_BIOS_DEFAULT (default off)
3	GPI (no function)
4	Topswap (no function, default on)
5	Topswap (no function, default on)
6	GPI (no function)
7	LOAD_BIOS_DEFAULT (On)
8	AT_DET# (default)

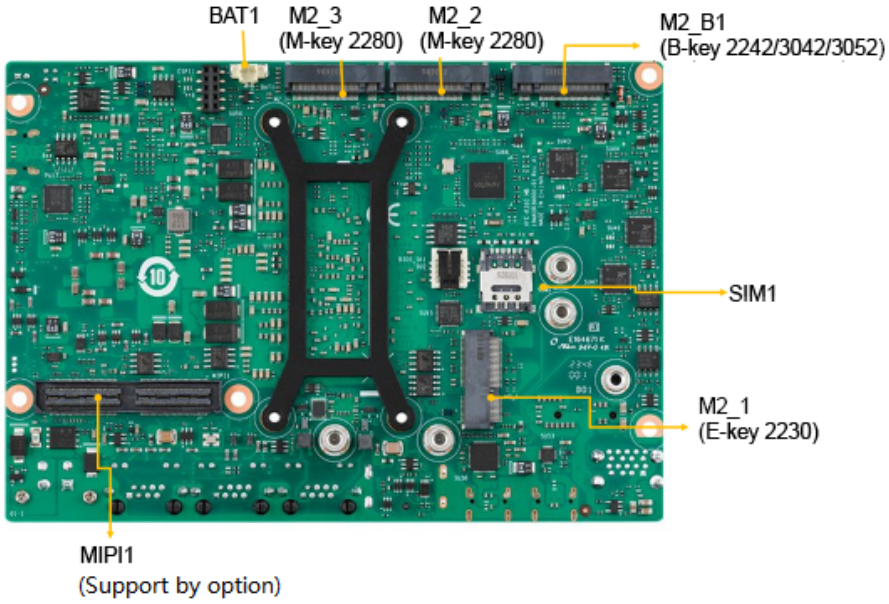


3.2 Connectors

Table 3.2: Connectors		
1	AUDIO1	Audio Internal Connector
2	BAT1	RTC battery Connector
3	CANBUS1	CAN Bus Port 0
4	CANBUS2	CAN Bus Port 1
5	CN1	Front Panel Internal Connector
6	COM1	COM Port Internal Connector 1
7	COM2	COM Port Internal Connector 2
8	COM3	COM Port Internal Connector 3
9	COM4	COM Port Internal Connector 4
10	DCIN1 DCIN2	DC Power Input Connector
11	DP1	DisplayPort Connector
12	FAN1	Smart FAN
13	GPIO1	GPIO Internal Connector
14	I2C_1	I2C/ SMBus Internal Connector
15	LAN1	I226 RJ-45 LAN Ports
16	LAN2	I226 RJ-45 LAN Ports
17	LAN3	I226 RJ-45 LAN Ports
20	M2_B1	M.2 Key-B Connector
21	M2_1	M.2 Key-E Connector
22	M2_2	M.2 Key-M Connector
23	M2_3	M.2 Key-M Connector
24	SW1	Miscellaneous Selection Jumper
25	TYPEC1	Type C Port (USB 3.2 / DP)
26	TYPEC2	Type C Port (USB 3.2 / DP)
27	TYPEC3	Type C Port (TBT4)
28	USB1	USB 3.2 Connector
29	USB2	USB 2.0 Internal Connector
30	U4	DDR5 SODIMM 5.2 mm
31	U5	DDR5 SODIMM 9.2 mm

3.3 Locating Connectors





3.4 Connector Pin Definitions

Table 3.3: CAN Bus Internal Connector: CANBUS1	
Pin	**Signal Pin Definition**
P/N	1654903500
Vendor MPN	ACES / 85205-03001
Pin	**Signal Definition**
1	CAN0_D+
2	CAN0_D-
3	GND

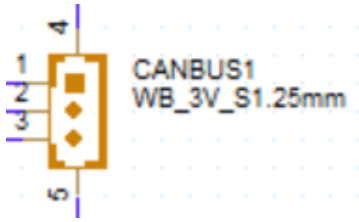


Table 3.4: CAN Bus Internal Connector: CANBUS2	
Pin	**Signal Pin Definition**
P/N	1654903500
Vendor MPN	ACES / 85205-03001
Pin	**Signal Definition**
1	CAN2_D+
2	CAN2_D-
3	GND

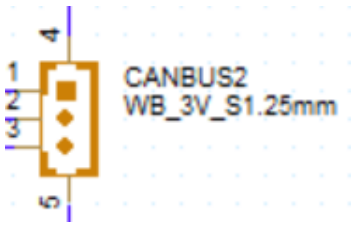


Table 3.5: I2C Internal Connector: I2C_1	
Pin	**Signal Pin Definition**
P/N	1655904020
Vendor MPN	ACES / 85205-04001
Pin	**Signal Definition**
1	GND
2	EC_I2C0_z_DAT
3	EC_I2C0_z_CLK
4	+V3.3_I2CCONN

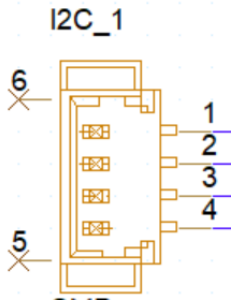


Table 3.6: Smart FAN Internal Connector: FAN1	
Pin	**Signal Pin Definition**
P/N	1653008788-01
Vendor MPN	ACES / 50273-00401-001
Pin	**Signal Definition**
1	GND
2	+V12
3	FAN_SPEED
4	FAN_V5_PWM

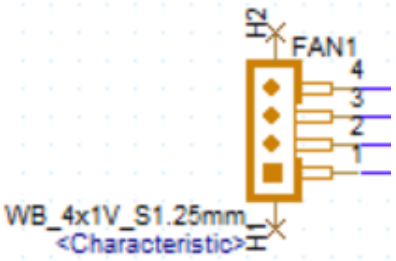


Table 3.7: USB 2.0 Dual-Port Internal Connector: USB2	
Pin	**Signal Pin Definition**
P/N	1653008214-01
Vendor MPN	Pinrex / 52C-90-10GBE0
Pin	**Signal Definition**
1	+V5SB_USB2
2	+V5SB_USB2
3	USB9_z_P-
4	USB10_z_P-
5	USB9_z_P+
6	USB10_z_P+
7	GND
8	GND
9	GND
10	NC

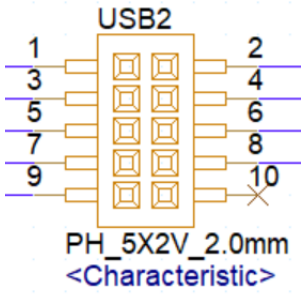


Table 3.8: Audio Internal Connector: AUDIO1	
Pin	**Signal Pin Definition**
P/N	1653008214-01
Vendor MPN	Pinrex / 52C-90-10GBE0
Pin	**Signal Definition**
1	LOUTR
2	LINR
3	GND_AUD
4	GND_AUD
5	LOUTL
6	LINL
7	GND_AUD
8	FRONT_JD
9	MIC1R
10	MIC1L

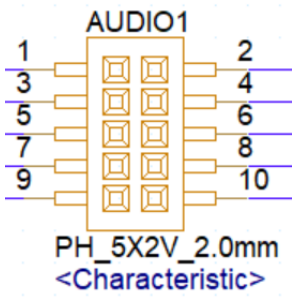


Table 3.9: COM Port Internal Connector 1: COM1	
Pin	**Signal Pin Definition**
P/N	1655004032
Vendor MPN	ACES / 85205-05701
Pin	**Signal Definition**
1	COM1_TXD
2	COM1_RTS#
3	COM1_RXD
4	COM1_CTS#
5	GND

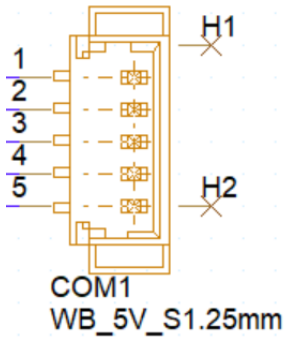


Table 3.10: COM Port Internal Connector 2: COM2	
Pin	**Signal Pin Definition**
P/N	1655004032
Vendor MPN	ACES / 85205-05701
Pin	**Signal Definition**
1	COM2_TXD
2	COM2_RTS#
3	COM2_RXD
9	COM2_CTS#
10	GND

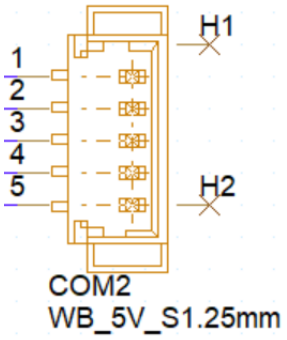


Table 3.11: COM Port Internal Connector 3: COM3	
Pin	**Signal Pin Definition**
P/N	1655004032
Vendor MPN	ACES / 85205-05701
Pin	**Signal Definition**
1	COM3_TXD
2	COM3_RTS#
3	COM3_RXD
4	COM3_CTS#
5	GND

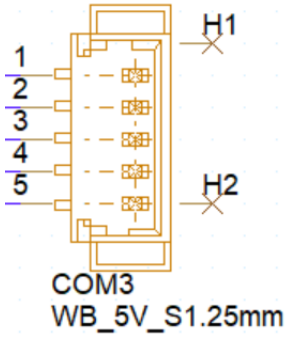


Table 3.12: COM Port Internal Connector 4: COM4	
Pin	**Signal Pin Definition**
P/N	1655004032
Vendor MPN	ACES / 85205-05701
Pin	**Signal Definition**
1	COM4_TXD
2	COM4_RTS#
3	COM4_RXD
4	COM4_CTS#
5	GND

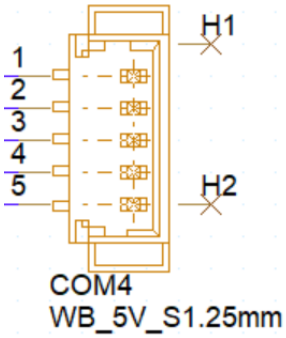


Table 3.13: Front Panel Internal Connector: CN1	
Pin	**Signal Pin Definition**
P/N	1653007728-02
Vendor MPN	ACES / 50273-0107N-002
Pin	**Signal Definition**
1	GND
2	BUZZER-
3	BUZZER+
4	CASEOPEN#
5	NC
6	FP_a_PSIN#
7	FP_a_RST#
8	+V3.3
9	NC
10	+V5

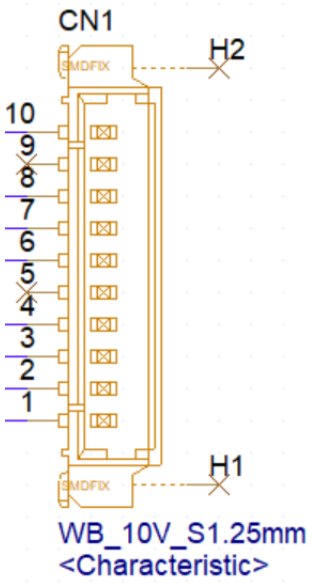


Table 3.14: GPIO Internal Connector: GPIO1	
Pin	**Signal Pin Definition**
P/N	1653007728-02
Vendor MPN	ACES / 50273-0107N-002
Pin	**Signal Definition**
1	GND
2	EC_P1_GPIO7
3	EC_P1_GPIO2
4	EC_P1_GPIO6
5	EC_P1_GPIO1
6	EC_P1_GPIO5
7	EC_P1_GPIO0
8	EC_P1_GPIO4
9	+V5_P1_GPIO
10	EC_P1_GPIO3

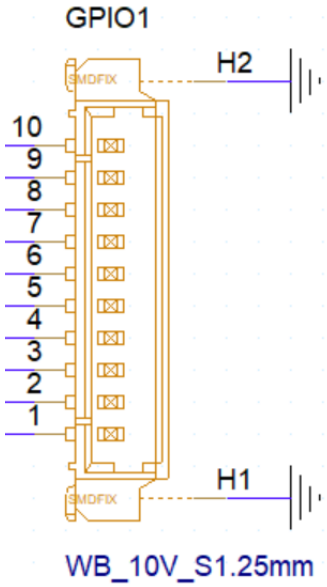


Table 3.15: RTC Battery Connector: BAT1	
Pin	**Signal Pin Definition**
1	+VBAT
2	GND

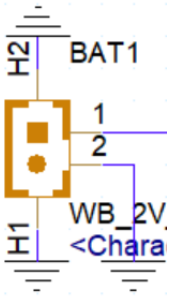


Table 3.16: M.2 E-Key Connector: M2_1	
Pin	**Signal Pin Definition**
1	GND
2	+V3.3SB_M.2_E
3	USB6_z_P+
4	+V3.3SB_M.2_E
5	USB6_z_P-
6	NC
7	GND
8	NC
9	NC
10	NC
11	NC
12	NC
13	NC
14	NC
15	NC
16	NC
17	NC
18	GND
19	NC
20	NC
21	NC
22	UART2_RXD
23	NC
32	UART2_TXD
33	GND
34	NC
35	PCIE_M2_z_TX3+
36	NC
37	PCIE_M2_z_TX3-

Table 3.16: M.2 E-Key Connector: M2_1	
38	CLINK_RST#
39	GND
40	CLINK_DATA
41	PCIE_M2_RX3+
42	CLINK_CLK
43	PCIE_M2_RX3-
44	CNV_PA_BLANKING
45	GND
46	NC
47	CLK0_M2E_z_PCIE+
48	NC
49	CLK0_M2E_z_PCIE-
50	SUSCLK_z_EKEY
51	GND
52	PLTRST_BUFFER#
53	PCIE_a_CLKREQ0#
54	BT_DISABLE#
55	PCIE_WAKE#_3.3
56	WIFI_DISABLE#
57	GND
58	NC
59	PCIE_M2_z_TX4+
60	NC
61	PCIE_M2_z_TX4-
62	NC
63	GND
64	NC
65	PCIE_M2_RX4+
66	NC
67	PCIE_M2_RX4-
68	PCIE_a_CLKREQ1#
69	GND
70	NC
71	CLK1_M2E_z_PCIE+
72	+V3.3SB_M.2_E
73	CLK1_M2E_z_PCIE-
74	+V3.3SB_M.2_E
75	GND
H1	NC
H2	NC
H3	GND
H4	GND

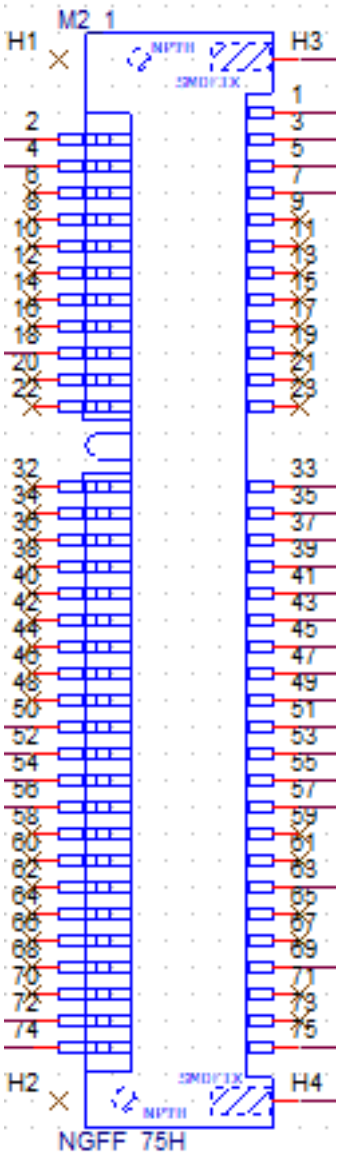


Table 3.17: M.2 M-Key Connector: M2_2	
Pin	**Signal Pin Definition**
1	GND
2	+V3.3_M.2_1
3	GND
4	+V3.3_M.2_1
5	PCIE3_KEY-M_RX3-
6	NC
7	PCIE3_KEY-M_RX3+
8	M.2_PLN#
9	GND
10	NC
11	PCIE3_KEY-M_a_TX3-
12	+V3.3_M.2_1
13	PCIE3_KEY-M_a_TX3+
14	+V3.3_M.2_1

Table 3.17: M.2 M-Key Connector: M2_2	
15	GND
16	+V3.3_M.2_1
17	PCIE3_KEY-M_RX2-
18	+V3.3_M.2_1
19	PCIE3_KEY-M_RX2+
20	NC
21	GND
22	NC
23	PCIE3_KEY-M_a_TX2-
24	NC
25	PCIE3_KEY-M_a_TX2+
26	NC
27	GND
28	NC
29	PCIE3_KEY-M_RX1-
30	NC
31	PCIE3_KEY-M_RX1+
32	GND
33	GND
34	USB8_z_P+
35	PCIE3_KEY-M_a_TX1-
36	USB8_z_P-
37	PCIE3_KEY-M_a_TX1+
38	GND
39	GND
40	NC
41	PCIE3_KEY-M_RX0-
42	NC
43	PCIE3_KEY-M_RX0+
44	NC
45	GND
46	NC
47	PCIE3_KEY-M_a_TX0-
48	NC
49	PCIE3_KEY-M_a_TX0+
50	PLTRST_M2M1_BUFFER#
51	GND
52	CLK0_M2MB_a_PCIE_REQ#
53	CK0_100M_a_MKEY_N
54	M2M1_PCIE_WAKE#
55	CK0_100M_a_MKEY_P
56	NC
57	GND
58	NC
67	NC
68	PCH_SUSCLK_R_M2M1
69	NC

Table 3.17: M.2 M-Key Connector: M2_2	
70	+V3.3_M.2_1
71	GND
72	+V3.3_M.2_1
73	GND
74	+V3.3_M.2_1
75	GND
H1	NC
H2	NC
H3	NC
H4	NC

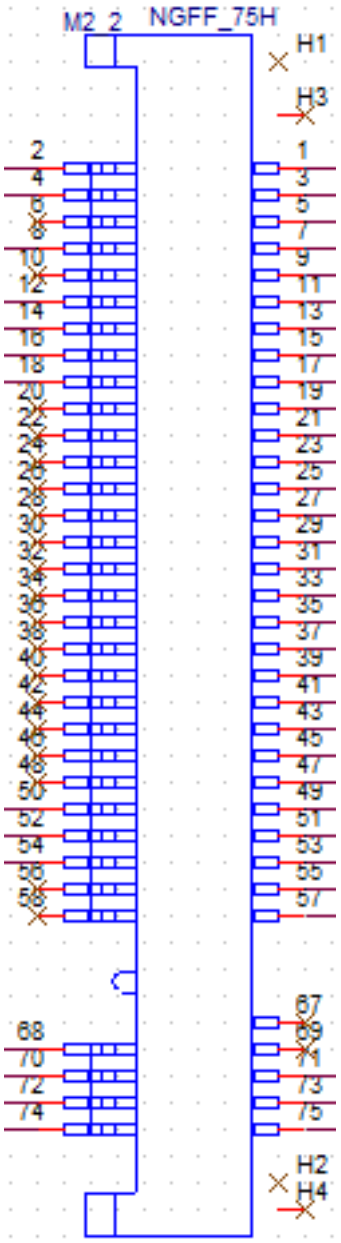


Table 3.18: M.2 M-Key Connector: M2_3	
Pin	**Signal Pin Definition**
1	GND
2	+V3.3_M.2_2
3	GND
4	+V3.3_M.2_2
5	PCIE4_KEY-M_RX3-
6	NC
7	PCIE4_KEY-M_RX3+
8	M2M1_PLN#
9	GND
10	NC
11	PCIE4_KEY-M_a_TX3-
12	+V3.3_M.2_2
13	PCIE4_KEY-M_a_TX3+
14	+V3.3_M.2_2
15	GND
16	+V3.3_M.2_2
17	PCIE4_KEY-M_RX2-
18	+V3.3_M.2_2
19	PCIE4_KEY-M_RX2+
20	NC
21	GND
22	NC
23	PCIE4_KEY-M_a_TX2-
24	NC
25	PCIE4_KEY-M_a_TX2+
26	NC
27	GND
28	NC
29	PCIE4_KEY-M_RX1-
30	NC
31	PCIE4_KEY-M_RX1+
32	NC
33	GND
34	NC
35	PCIE4_KEY-M_a_TX1-
36	NC
37	PCIE4_KEY-M_a_TX1+
38	NC
39	GND
40	NC
41	PCIE4_KEY-M_RX0-
42	NC
43	PCIE4_KEY-M_RX0+
44	NC
45	GND

Table 3.18: M.2 M-Key Connector: M2_3	
46	NC
47	PCIE4_KEY-M_a_TX0-
48	NC
49	PCIE4_KEY-M_a_TX0+
50	PLTRST_M2M2_BUFFER#
51	GND
52	CLK1_M2MB_a_PCIE_REQ#
53	CK1_100M_a_MKEY_N
54	M2M2_PCIE_WAKE#
55	CK1_100M_a_MKEY_P
56	NC
57	GND
58	NC
67	NC
68	PCH_SUSCLK_R_M2M2
69	NC
70	+V3.3_M.2_2
71	GND
72	+V3.3_M.2_2
73	GND
74	+V3.3_M.2_2
75	GND
H1	NC
H2	NC
H3	NC
H4	NC

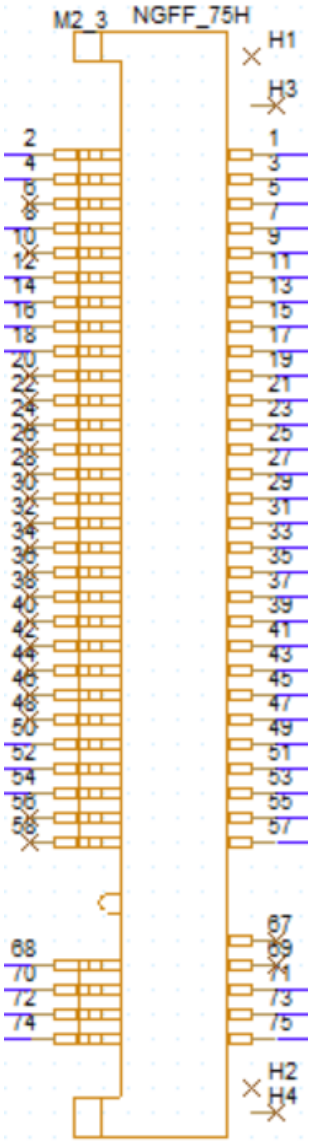


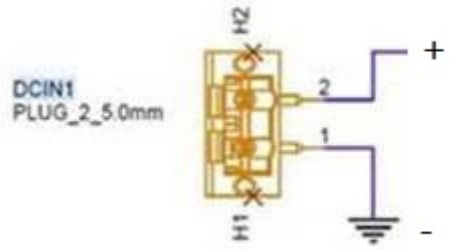
Table 3.19: M.2 B-Key Connector: M2_B1

Pin	Signal Pin Definition
1	M2B1_CFG3
2	+V3.3A_M.2_B
3	GND
4	+V3.3A_M.2_B
5	GND
6	M2B1_FULL_CARD_OFF#
7	USB_M2B1_P
8	M2B1_W_DISABLE1#
9	USB_M2B1_N
10	CAM1_SYNCOUT
11	GND
20	M2B1_PCIE_DIS
21	M2B1_CFG0
22	M2B1_ANT_CFG

Table 3.19: M.2 B-Key Connector: M2_B1	
23	M2B1_WAKE_ON_WWAN#
24	M2B1_ANT_TUNER
25	M2B1_DPR
26	M2B1_W_DISABLE2#
27	GND
28	NC
29	M2B1_PCIE_RX1-
30	M2B1_UIM_RESET
31	M2B1_PCIE_RX1+
32	M2B1_UIM_CLK
33	GND
34	M2B1_UIM_DATA
35	M2B1_PCIE_TX1-
36	M2B1_UIM_PWR
37	M2B1_PCIE_TX1+
38	NC
39	GND
40	NC
41	M2B1_PCIE_RX-
42	NC
43	M2B1_PCIE_RX+
44	NC
45	GND
46	NC
47	M2B1_PCIE_TX-
48	NC
49	M2B1_PCIE_TX+
50	M2B1_a_PERST#
51	GND
52	M2B1_a_CLKREQ#
53	CLK100M_a_M2B1-
54	M2B1_PCIEWAKE#
55	CLK100M_a_M2B1+
56	NC
57	GND
58	NC
59	NC
60	NC
61	NC
62	NC
63	NC
64	NC
65	NC
66	NC
67	M2B1_a_RESET#
68	M2B1_SUSCLK
69	M2_DET

Table 3.19: M.2 B-Key Connector: M2_B1	
70	+V3.3A_M.2_B
71	GND
72	+V3.3A_M.2_B
73	GND
74	+V3.3A_M.2_B
75	M2B1_CFG2
H1	NC
H2	NC
H3	GND
H4	GND

Table 3.20: Power Input: DCIN1	
Pin	**Signal Pin Definition**
1	Ground
2	+VIN



Chapter 4

AMI BIOS Setup

AMIBIOS has been integrated into a plethora of motherboards for decades. With the AMIBIOS Setup program, you can modify BIOS settings and control the various system features. This chapter describes the basic navigation of the ASR-A502 BIOS setup screens.

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in battery-backed CMOS so it retains the Setup information when the power is turned off.

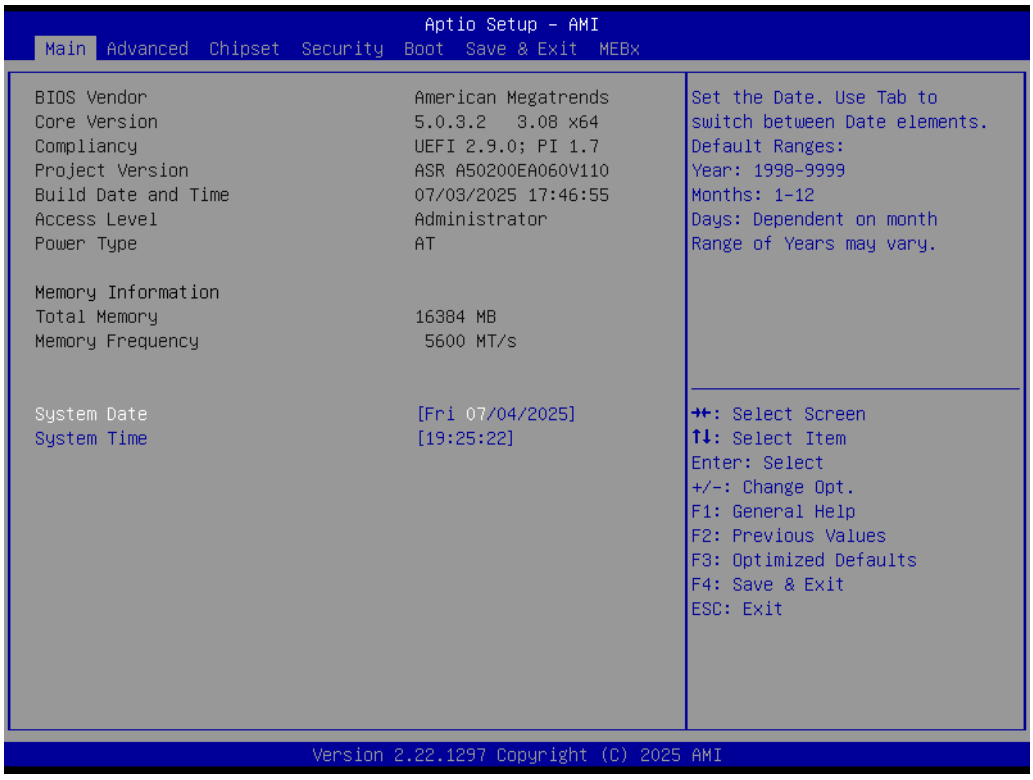
4.1 Entering Setup

Turn on the computer and check for the patch code. If there is a number assigned to the patch code, it means that the BIOS supports your CPU. If there is no number assigned to the patch code, please contact an Advantech application engineer to obtain an up-to-date patch code file. This will ensure that your CPU's system status is valid. After ensuring that you have a number assigned to the patch code, press <DEL> and you will immediately be allowed to enter Setup.

4.1.1 Main Setup

When you first enter the BIOS Setup Utility, you will encounter the Main setup screen.

You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



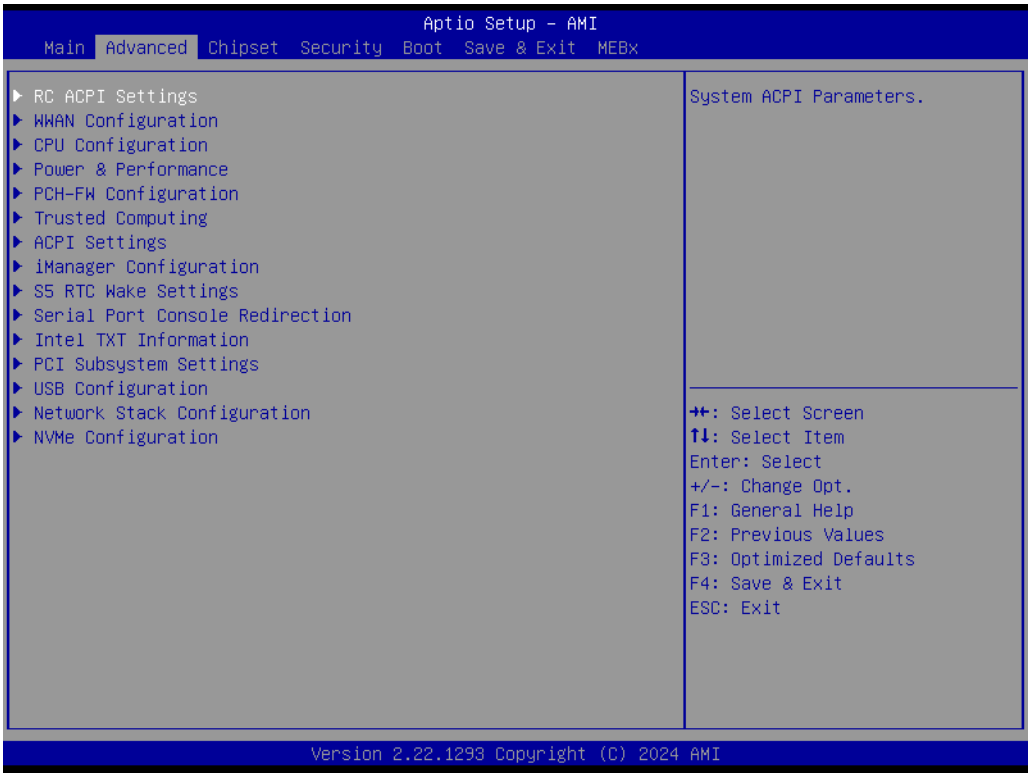
The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

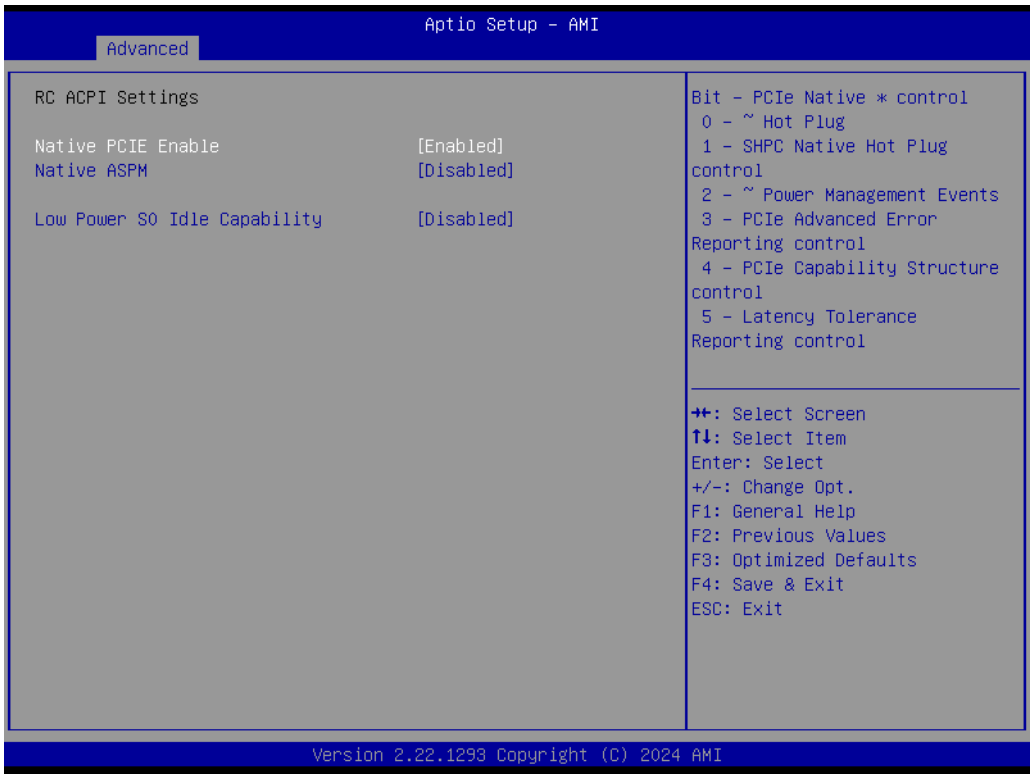
- **System Time / System Date**
  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

4.1.2 Advanced BIOS Features Setup

Select the Advanced tab from the ASR-A502 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub-menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screens is shown below. The sub-menus are described on the following pages.

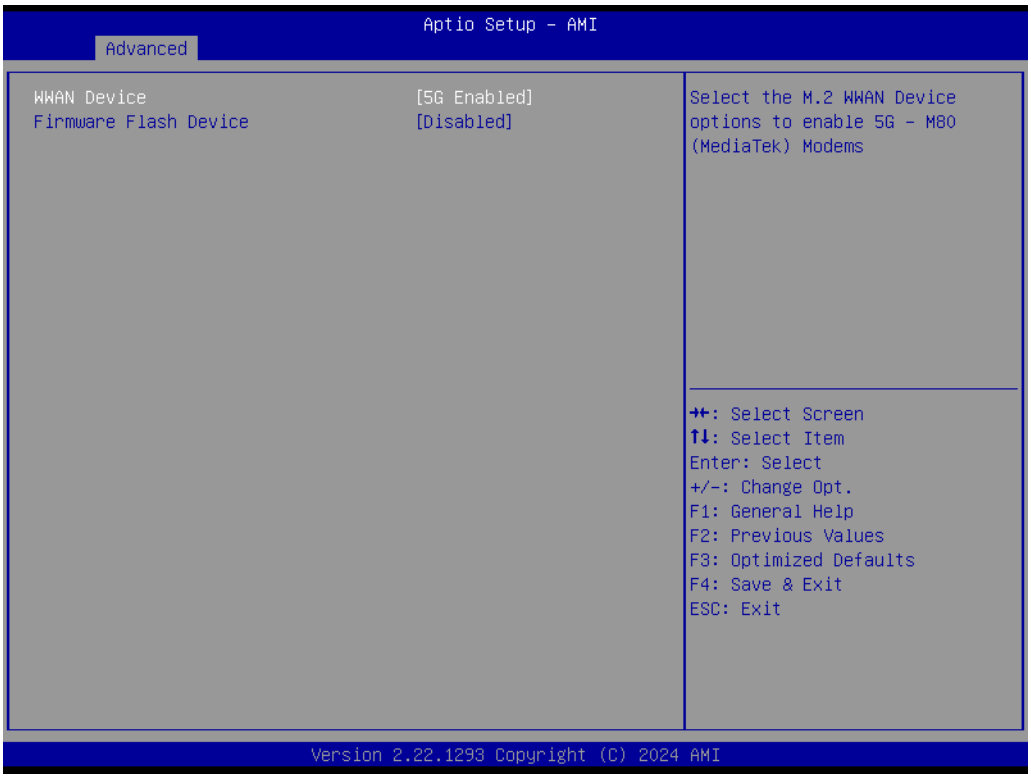


4.1.2.1 RC ACPI Settings



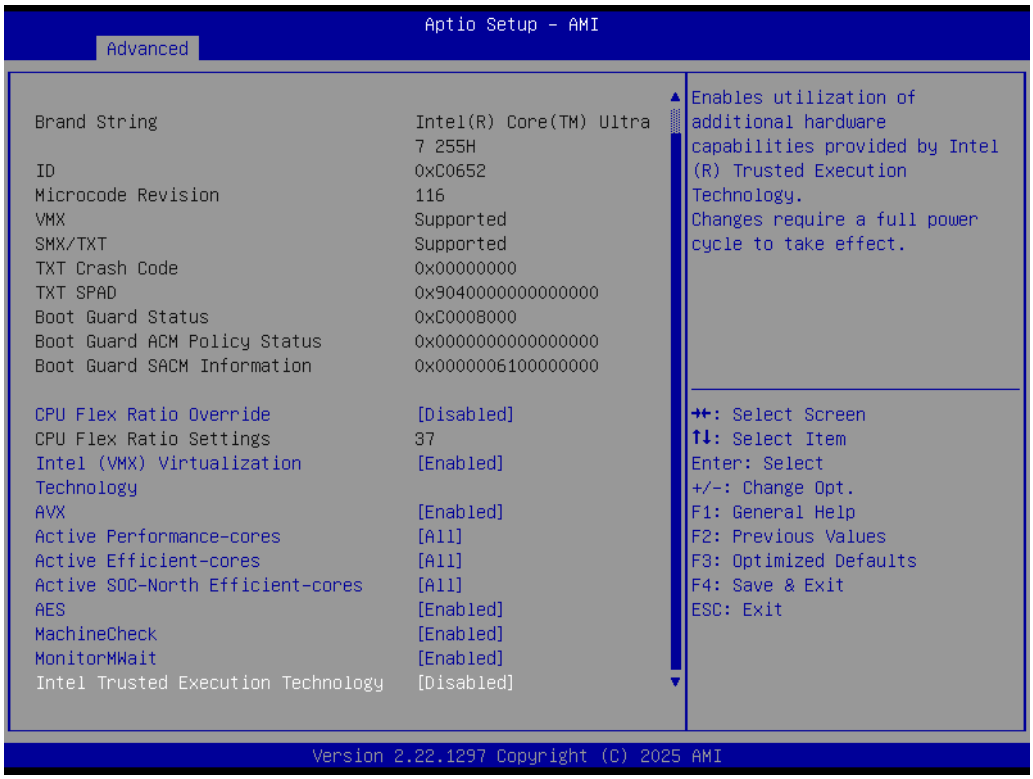
- **Native PCIE Enable**
  Enable/Disable PCIE Native Control reported in the ACPI Table.
- **Native ASPM**
  Choose if the ASPM feature is controlled by the OS or BIOS.
- **Low Power S0 Idle Capability**
  This can Enable/Disable ACPI Low Power S0 Idle Capability under the OS.

4.1.2.2 WWAN Configuration



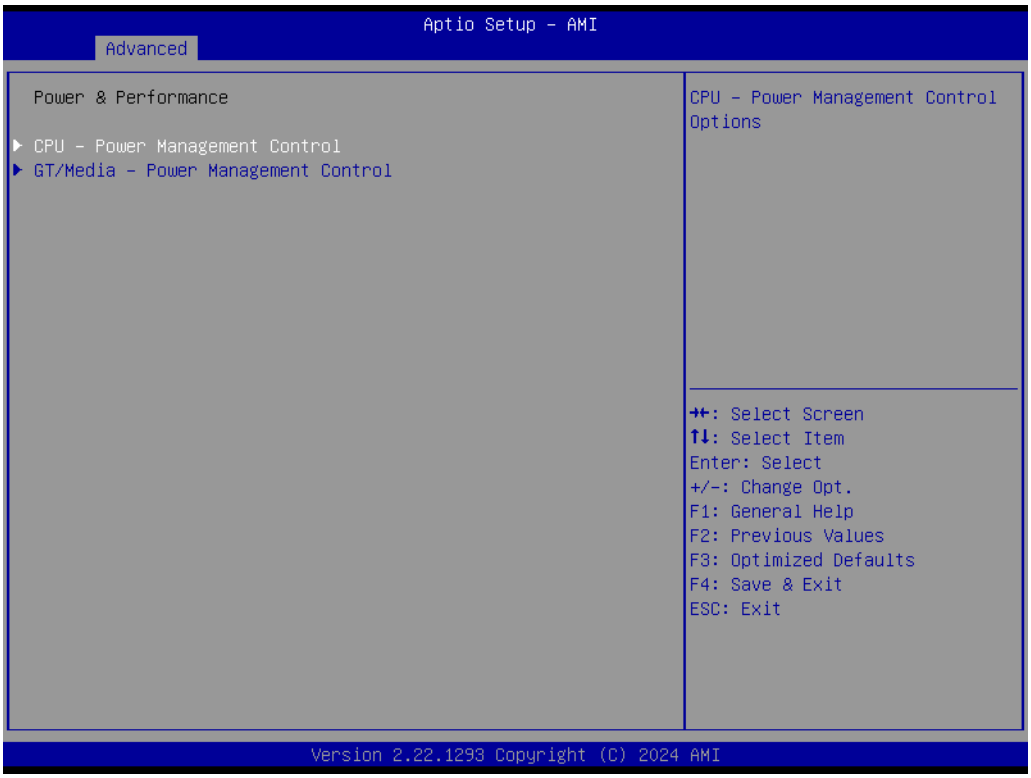
- **WWAN Device**
  Select the M.2 WWAN Device option to enable 5G Modems.
- **Firmware Flash Device**
  Enable or Disable a WWAN Firmware Flash Device.

4.1.2.3 CPU Configuration



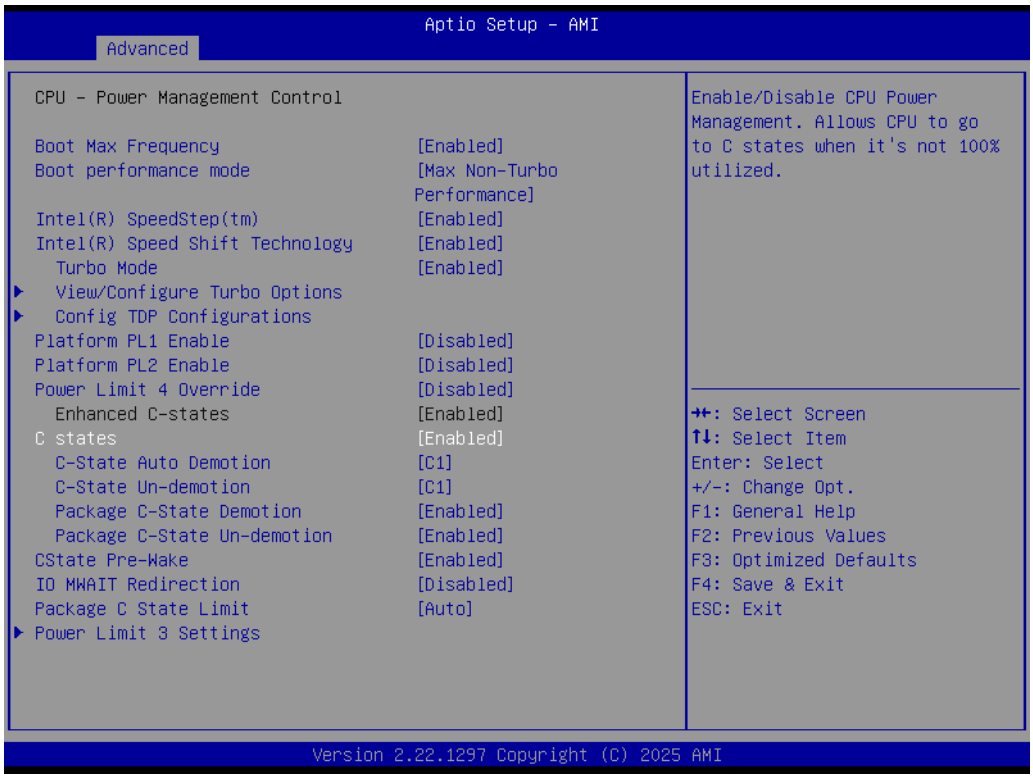
- **CPU Flex Ratio Override**
  Enable/Disable CPU Flex Ratio Programming.
- **Intel (VMX) Virtualization Technology**
  When Enabled, a VMM can utilize the additional hardware capability provided by Vanderpool Technology.
- **AVX**
  Enable/Disable the AVX 2/3 Instructions.
- **Active Performance-cores**
  Number of P-cores to enable in each processor package.
- **Active Efficient-cores**
  Number of E-cores to enable in each processor package.
- **Active SOC-North Efficient-Core**
  Number of SOC-North Efficient-cores to enable in SOC North.
- **Hyper-Threading**
  This item allows users to Enable/Disable Hyper-Threading Technology.
- **AES**
  Enable/Disable AES (Advanced Encryption Standard).
- **MachineCheck**
  Enable/Disable Machine Check.
- **MonitorMWait**
  Enable/Disable MonitorMWait.
- **Intel Trusted Execution Technology**
  Enables utilization of additional hardware capability provided by Intel® Trusted Execution Technology.

4.1.2.4 Power & Performance



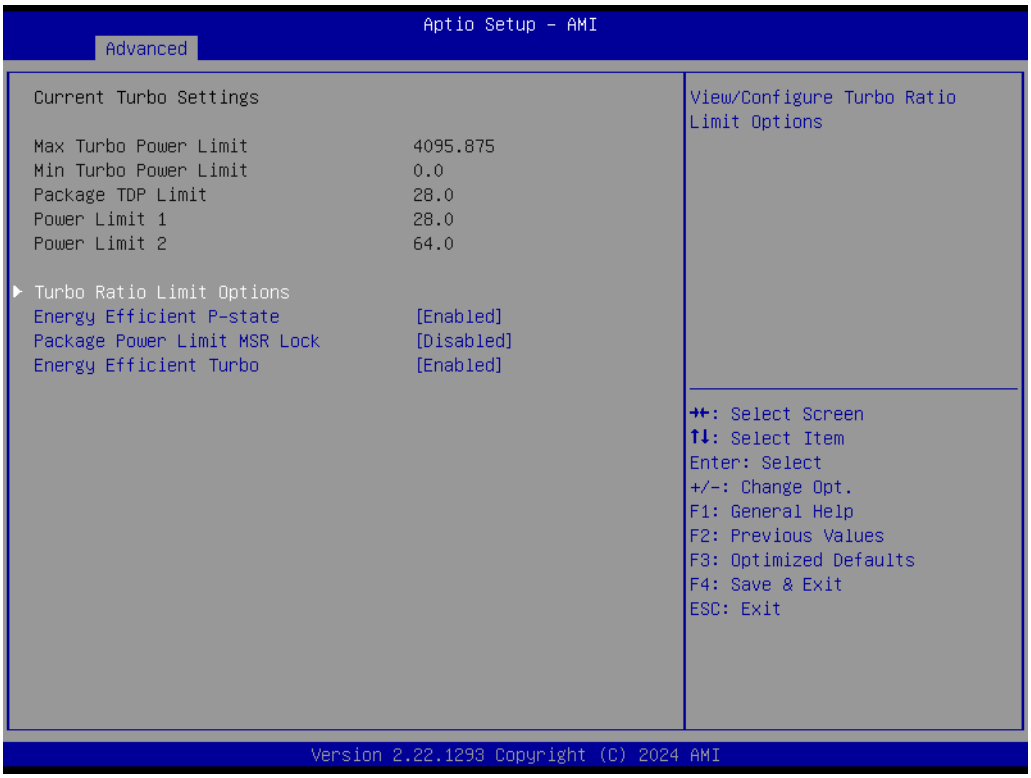
- **CPU – Power Management Control**
  CPU – Power Management Control Options.
- **GT – Power Management Control**
  GT – Power Management Control Options.

4.1.2.4.1 CPU - Power Management Control

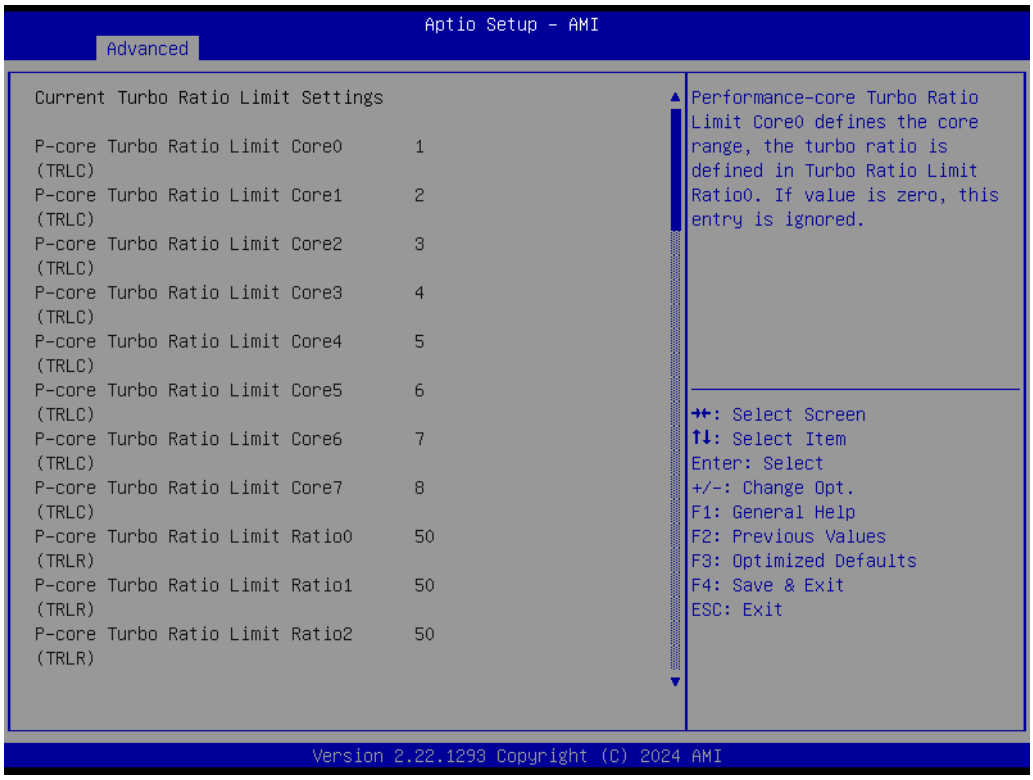


- **Boot Max Frequency**
  Enable/Disable Boot Maximum Frequency in CPU strap.
- **Boot performance mode**
  Select the performance state that the BIOS will set before OS handoff.
- **Intel® SpeedStep™**
  Allows more than two frequency ranges to be supported.
- **Intel® Speed Shift Technology**
  Enable/Disable Intel® Speed Shift Technology support.
- **Turbo Mode**
  Enable/Disable processor turbo mode.
- **View/Configure Turbo Options**
  View and Configure Turbo Options.
- **Config TDP Configuration**
  Config TDP Configurations.
- **Platform PL1 Enable**
  Enable/Disable Platform Power Limit 1 programming.
- **Platform PL2 Enable**
  Enable/Disable Platform Power Limit 1 programming.
- **Power Limit 4 Override**
  Enable/Disable Power Limit 4 override.
- **C states**
  Enable/Disable CPU Power Management.
- **PowerLimit 3 Settings**
  Power Limit 3 Settings.

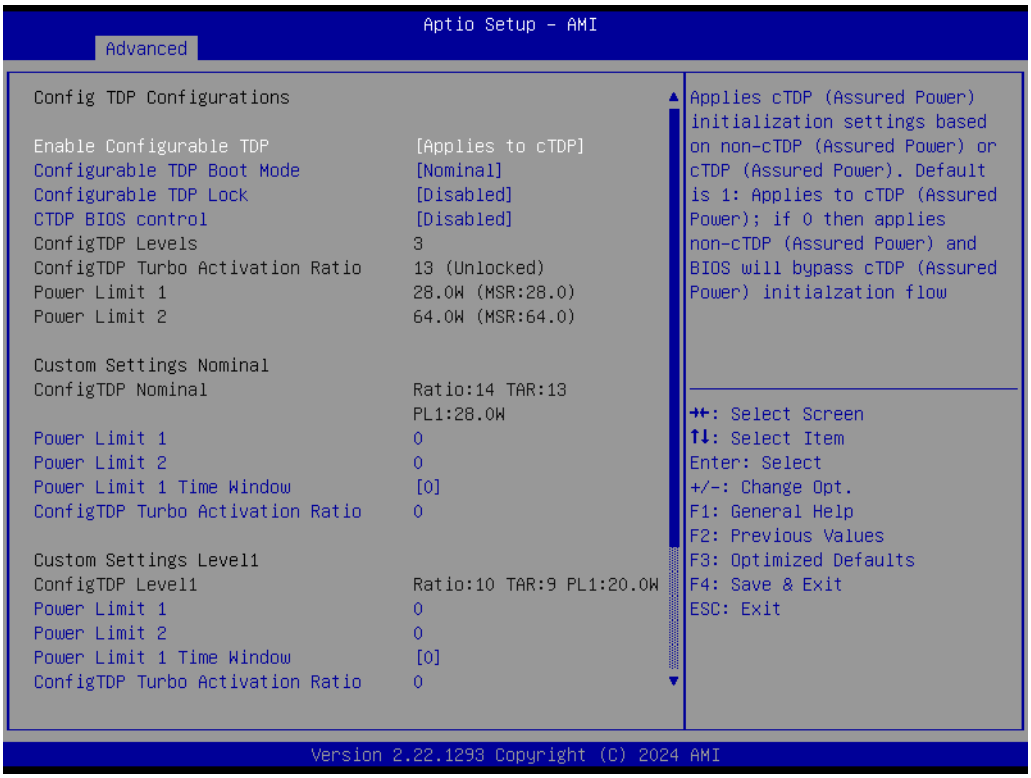
View/Configure Turbo Options



- **Turbo Ratio Limit Option**
  View/Configure Turbo Ratio Limit Options.
- **Energy Efficient P-state**
  Enable/Disable Energy Efficient P-state feature.
- **Package Power Limit MSR Lock**
  Enable/Disable locking of Package Power Limit settings.
- **Energy Efficient Turbo**
  Enable/Disable Energy Efficient Turbo feature.


Aptio Setup – AMI
Advanced
Current Turbo Ratio Limit Settings
P-core Turbo Ratio Limit Core0 (TRLC) 1
P-core Turbo Ratio Limit Core1 (TRLC) 2
P-core Turbo Ratio Limit Core2 (TRLC) 3
P-core Turbo Ratio Limit Core3 (TRLC) 4
P-core Turbo Ratio Limit Core4 (TRLC) 5
P-core Turbo Ratio Limit Core5 (TRLC) 6
P-core Turbo Ratio Limit Core6 (TRLC) 7
P-core Turbo Ratio Limit Core7 (TRLC) 8
P-core Turbo Ratio Limit Ratio0 (TRLR) 50
P-core Turbo Ratio Limit Ratio1 (TRLR) 50
P-core Turbo Ratio Limit Ratio2 (TRLR) 50
Performance-core Turbo Ratio Limit Core0 defines the core range, the turbo ratio is defined in Turbo Ratio Limit Ratio0. If value is zero, this entry is ignored.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2024 AMI

Config TDP Configurations

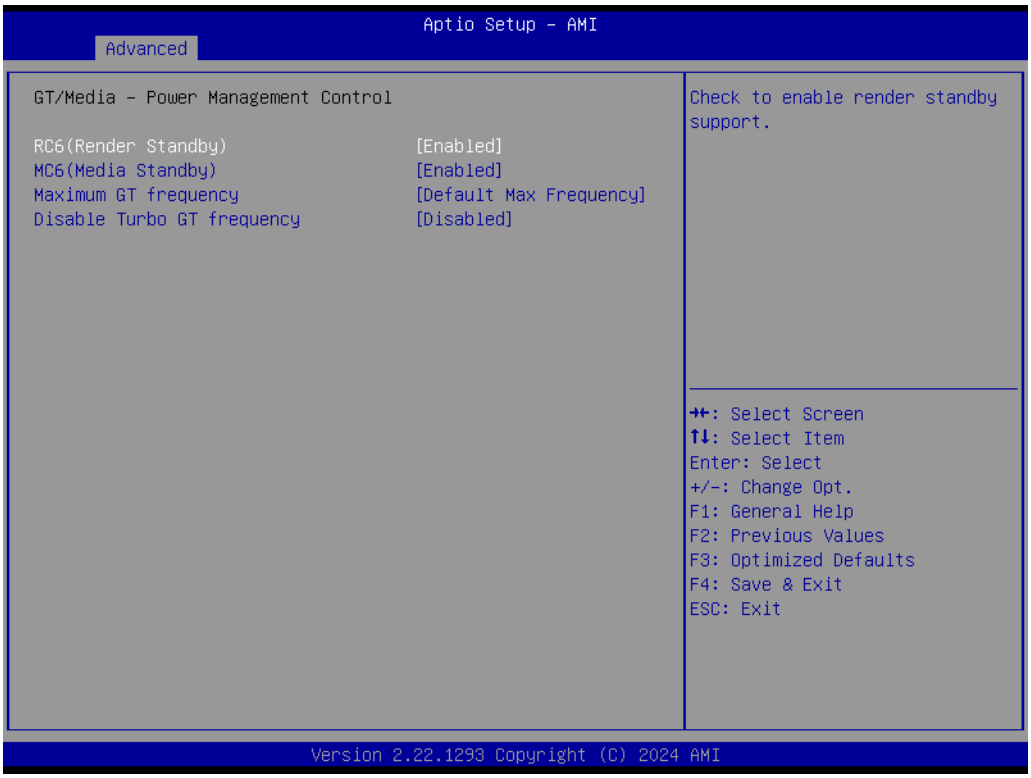


- **Enable Configurable TDP**
  Applies TDP initialization settings based on non-cTDP or cTDP.
- **Configurable TDP Boot Mode**
  Configurable TDP Mode as Nominal/Up/Down/Deactivate TDP selection.
- **Configurable TDP Lock**
  Configurable TDP Mode Lock sets the Lock bit.
- **CTDP BIOS control**
  Enables CTDP control via runtime ACPI BIOS method.
- **Power Limit 1**
  Power Limit 1 in milliwatts.
- **Power Limit 2**
  Power Limit 2 in milliwatts.
- **Power Limit 1 Time Window**
  Power Limit 1 Time Window value in seconds.
- **ConfigTDP Turbo Activation Ration**
  Custom value for Turbo Activation Ratio.

Power Limit 3 Settings

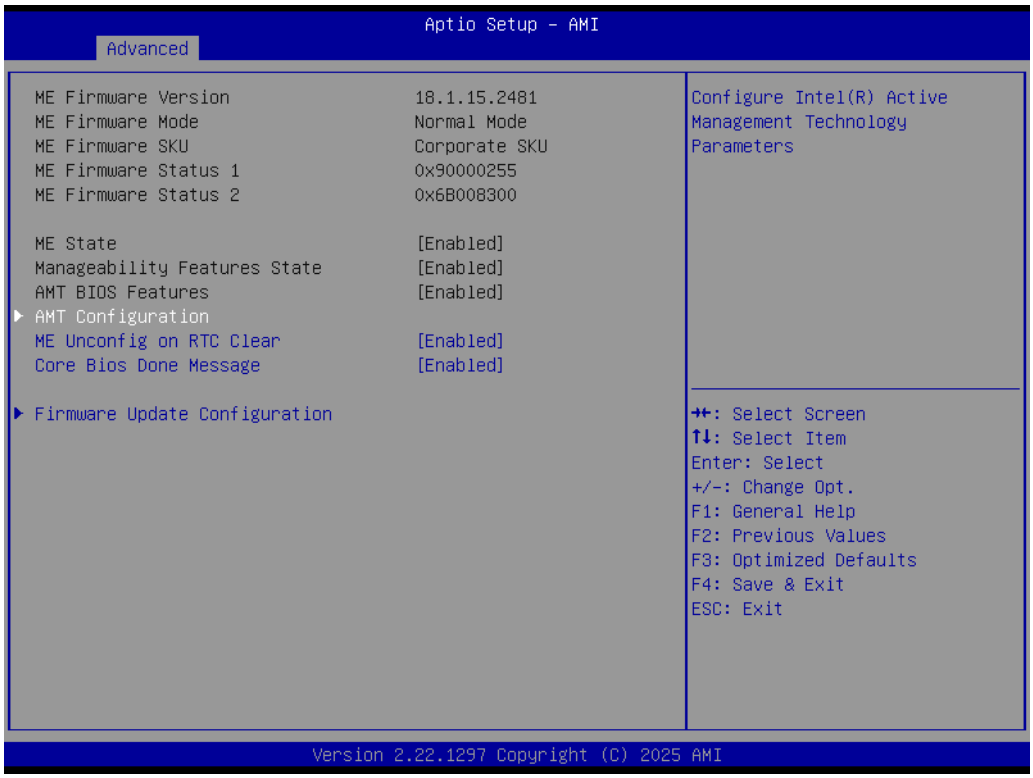
– **Power Limit 3 Override**
Enable/Disable Power Limit 3 override.

4.1.2.4.2GT - Power Management Control



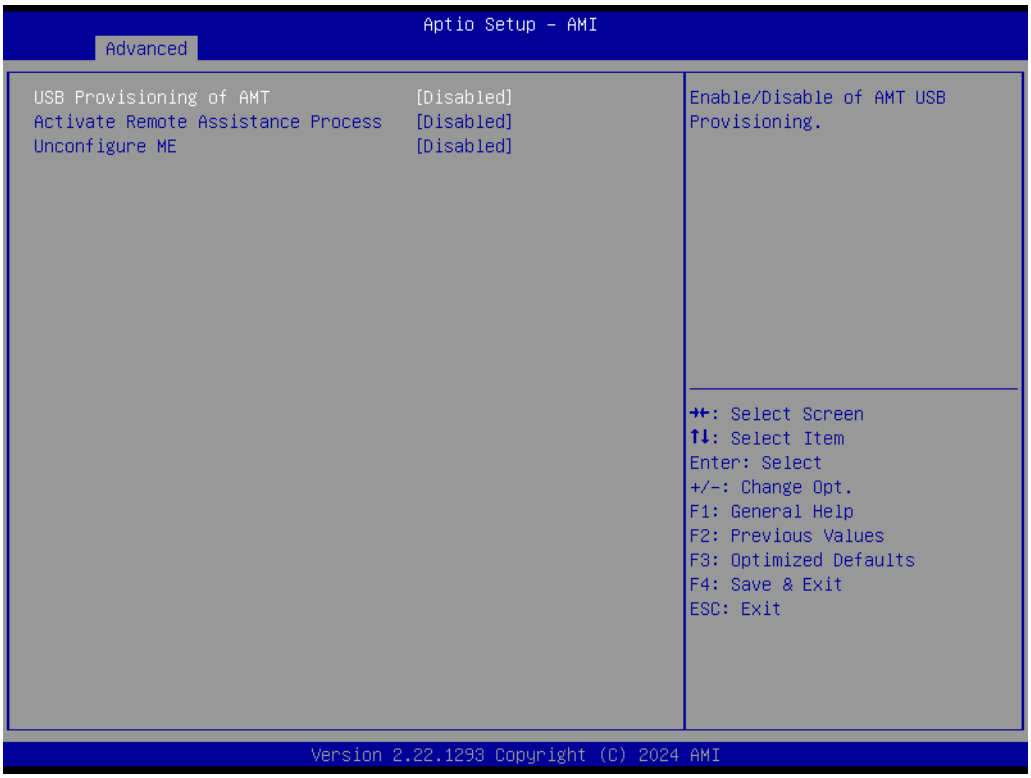
- **RC6 (Render Standby)**
  Check to enable render standby support.
- **Maximum GT frequency**
  Maximum GT frequency limited by user.
- **Disable Turbo GT frequency**
  Enabled/Disabled Turbo GT frequency.
- **MC6 (Media Standby)**
  Check to enable Media standby support.

4.1.2.5 PCH-FW Configuration



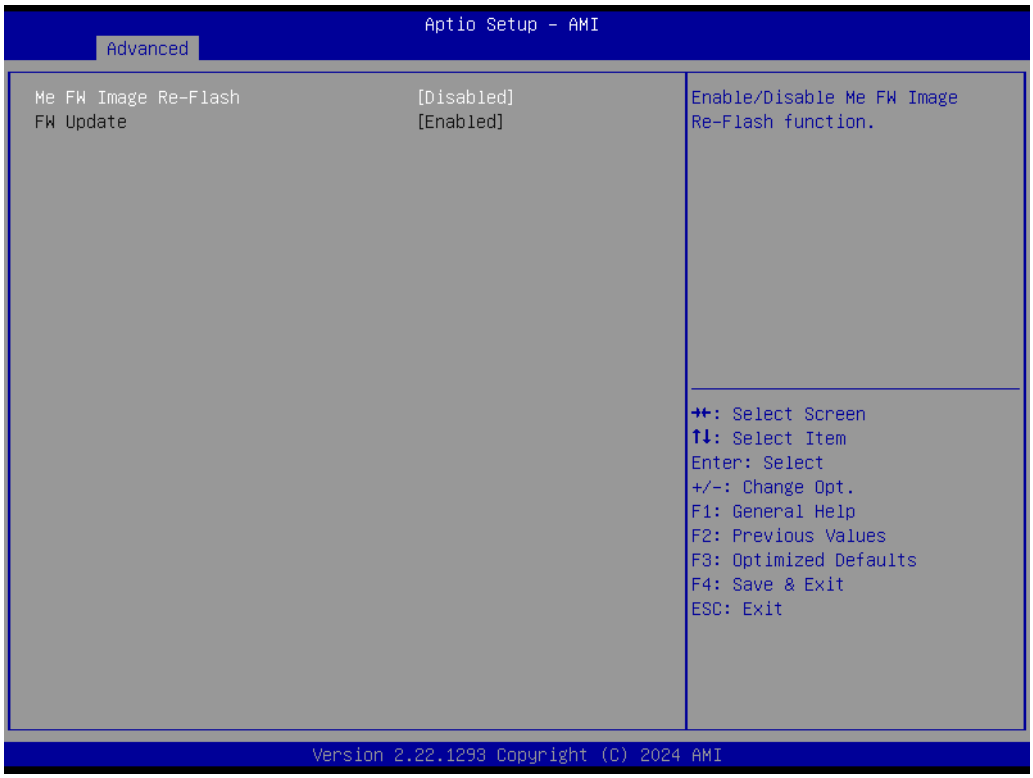
- **ME State**
  When Disabled ME will be put ME into Temporarily Disabled Mode.
- **Manageability Feature State**
  When Disabled, ME will not be unconfigured on RTC Clear.
- **AMT BIOS Features**
  When Disabled, ME will not be unconfigured on RTC Clear.
- **AMT Configuration**
  Configure Intel® Active Management Technology Parameters.
- **ME Unconfig on RTC Clear**
  When Disabled, ME will not be unconfigured on RTC Clear.
- **Core BIOS Done Message**
  Enable/Disable Core BIOS Done message sent to ME.
- **Firmware Update Configuration**
  Configure Management Engine Technology Parameters.

4.1.2.5.1 AMT Configuration

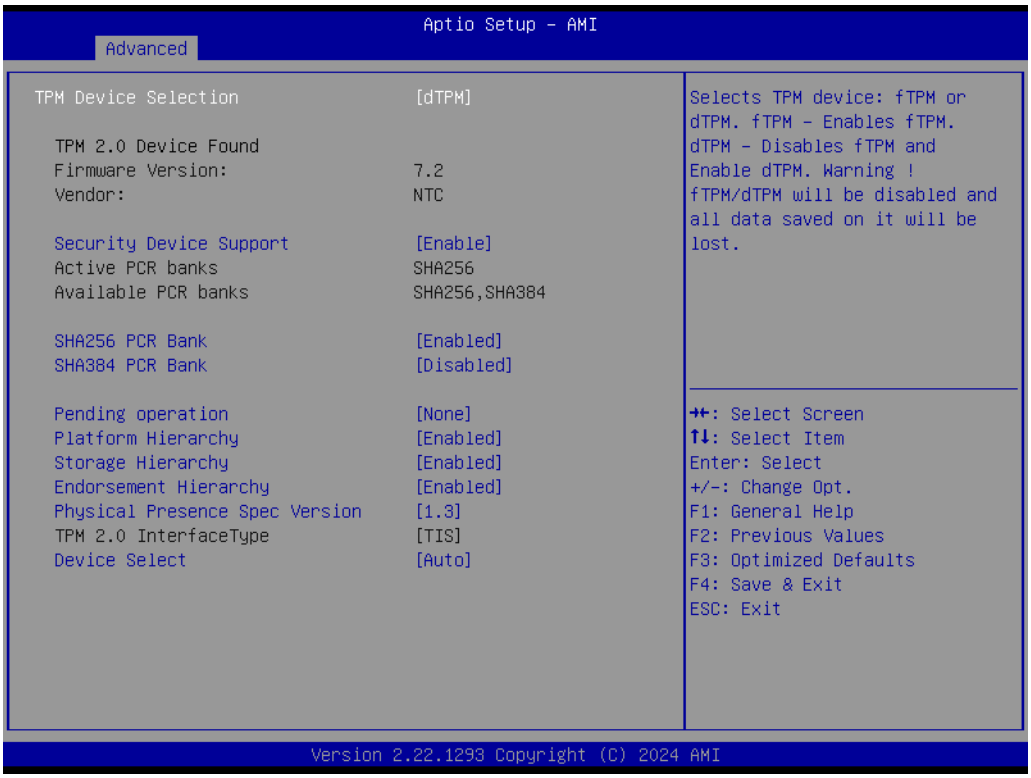


- **USB Provision of AMT**
  Enable/Disable of AMT BIOS Provisioning.
- **Active Remote Assistance Process**
  Trigger CIRA boot.
- **Unconfigure ME**
  Unconfigure ME with a reset of the MEBx password to default on next boot.

4.1.2.5.2AMT Configuration

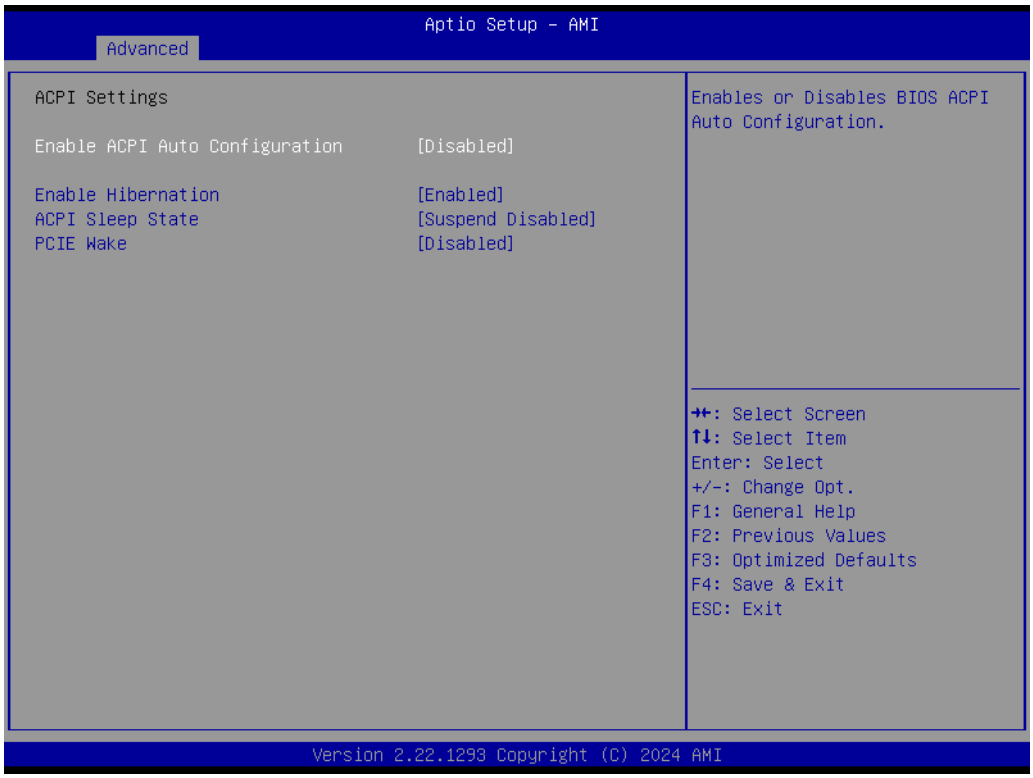


4.1.2.6 Trusted Computing



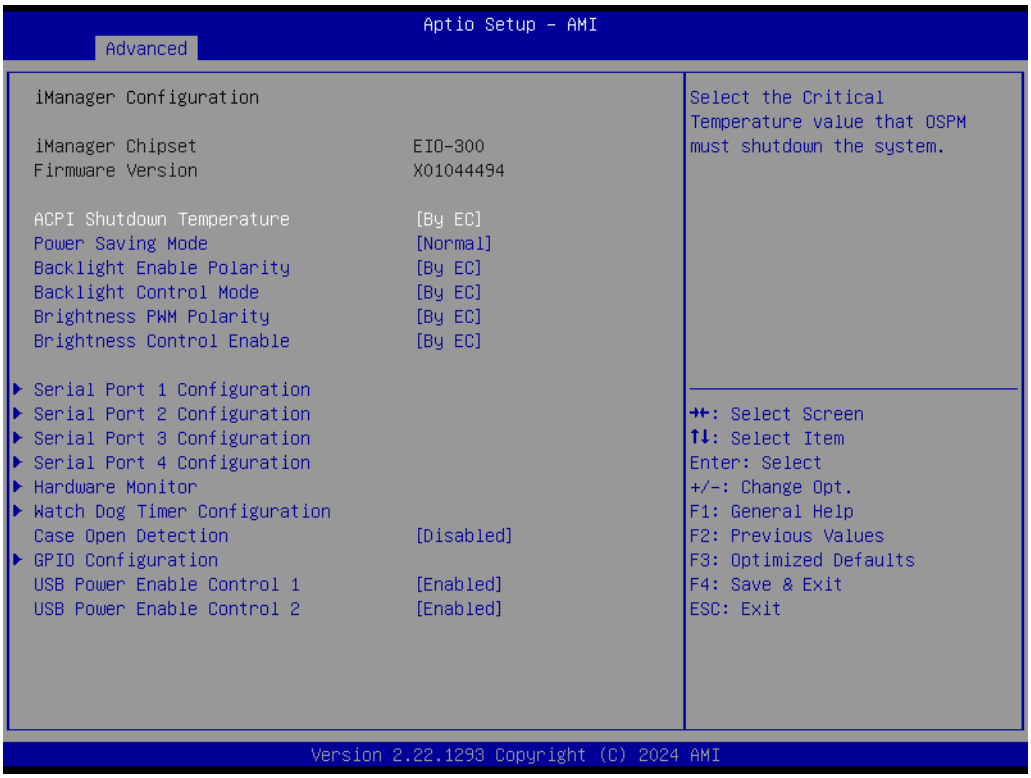
- **Security Device Support**
  Enable or Disable BIOS support for the security device.
- **SHA256 PCR Bank**
  Enable or Disable SHA256 PCR Bank.
- **Pending operation**
  Schedule an Operation for the security device.
- **Platform Hierarchy**
  Enable or Disable Platform Hierarchy.
- **Storage Hierarchy**
  Enable or Disable Storage Hierarchy.
- **Endorsement Hierarchy**
  Enable or Disable Endorsement Hierarchy.
- **Physical Presence Spec Version**
  Select to tell the OS to support PPI Spec Version 1.2 or 1.3.
- **Device Select**
  TPM 1.2 will restrict support to TPM 1.2 devices. TPM 2.0 will restrict support to TPM 2.0 devices.

4.1.2.7 ACPI Settings



- **Enable ACPI Auto Configuration**
  Enable or Disable BIOS ACPI auto configuration.
- **Enable Hibernation**
  Enables or Disables the System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
- **ACPI Sleep State**
  Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
- **PCIE Wake**
  Enable or Disable PCIE to wake the system from S5.

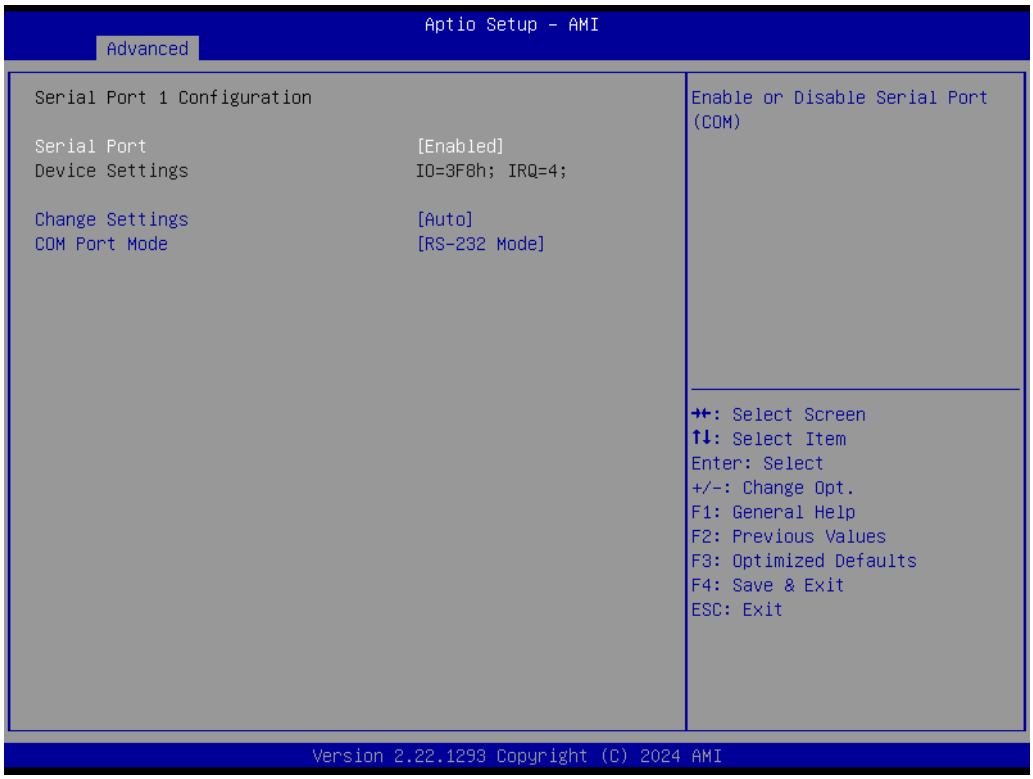
4.1.2.8 iManager Configuration



- **ACPI Shutdown Temperature**
  Enable/Disable CPU Shutdown Temperature.
- **Power Saving Mode**
  Enable/Disable power saving mode.
- **Backlight Enable Polarity**
  Switch Backlight Enable Polarity for Native or Invert.
- **Backlight Control Mode**
  Switch Backlight Control to PWM or DC mode.
- **Brightness PWM Polarity**
  Backlight Control Brightness PWM Polarity for Native or Invert.
- **Brightness Control Enable**
  Choose to control the LVDS brightness value by EC or User override during POST stage.
- **Serial Port 1 Configuration**
  Set Parameters of Serial Port 1.
- **Serial Port 2 Configuration**
  Set Parameters of Serial Port 2.
- **Serial Port 3 Configuration**
  Set Parameters of Serial Port 3.
- **Serial Port 4 Configuration**
  Set Parameters of Serial Port 4.
- **Hardware Monitor**
  Monitor hardware status.
- **Watch Dog Timer Configuration**
  Watch Dog Timer Configuration Page.
- **Case Open Detection**
  Enable or Disable the Case Open Detect Function.

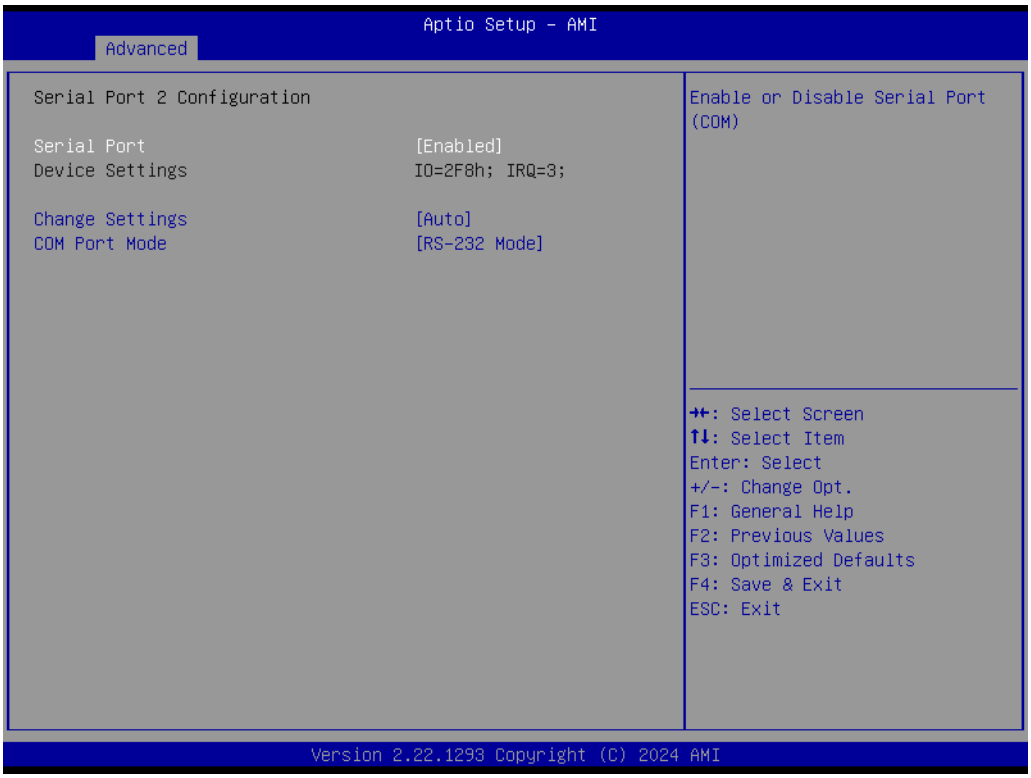
- **GPIO Configuration**
  GPIO Configuration Settings.

4.1.2.8.1 Serial Port 1 Configuration



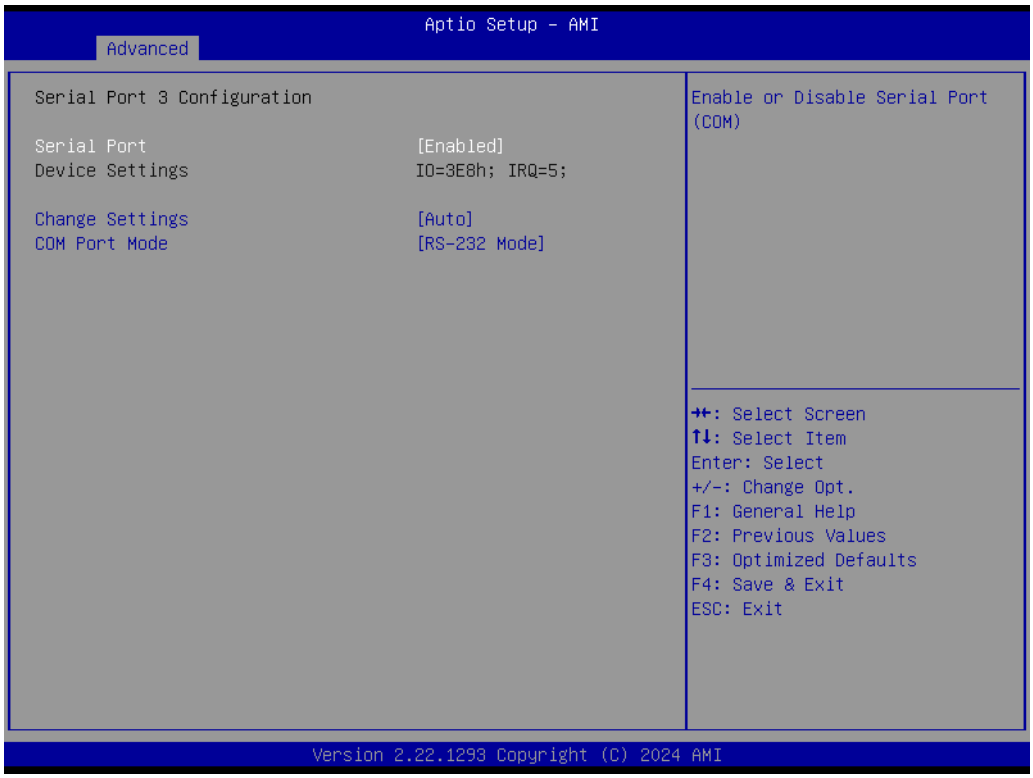
- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select an optimal settings for Super IO device.
- **COM Port Mode**
  COM Port Mode Select.

4.1.2.8.2Serial Port 2 Configuration



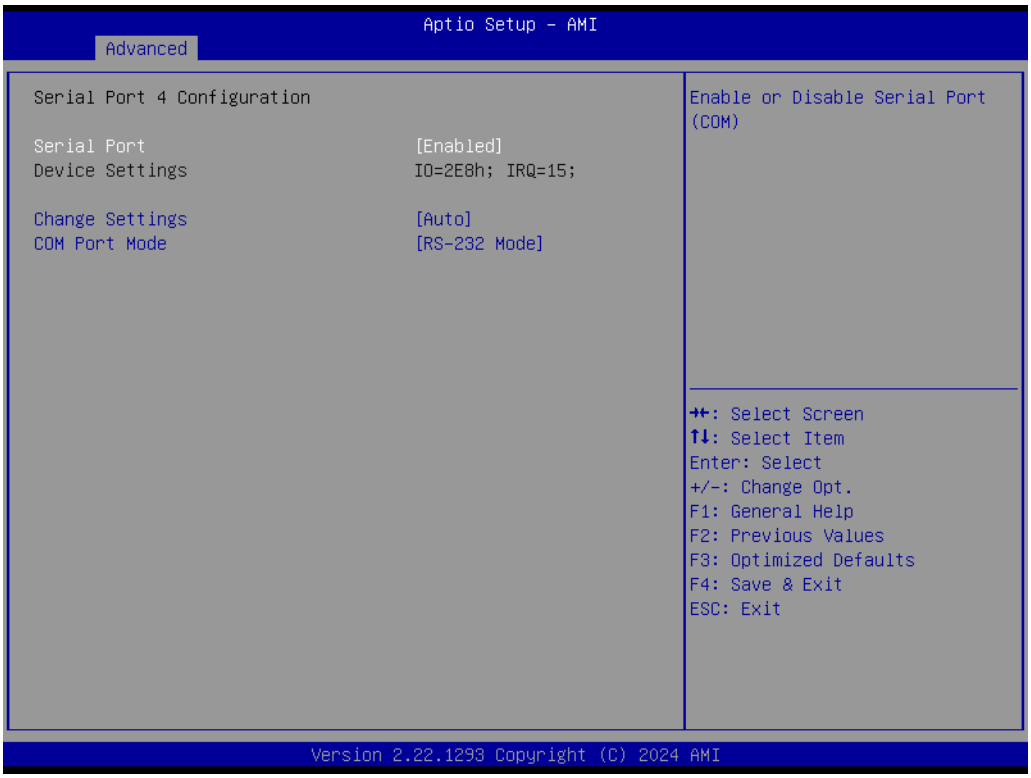
- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select an optimal settings for a Super IO device.
- **COM Port Mode**
  COM Port Mode Select.

4.1.2.8.3 Serial Port 3 Configuration



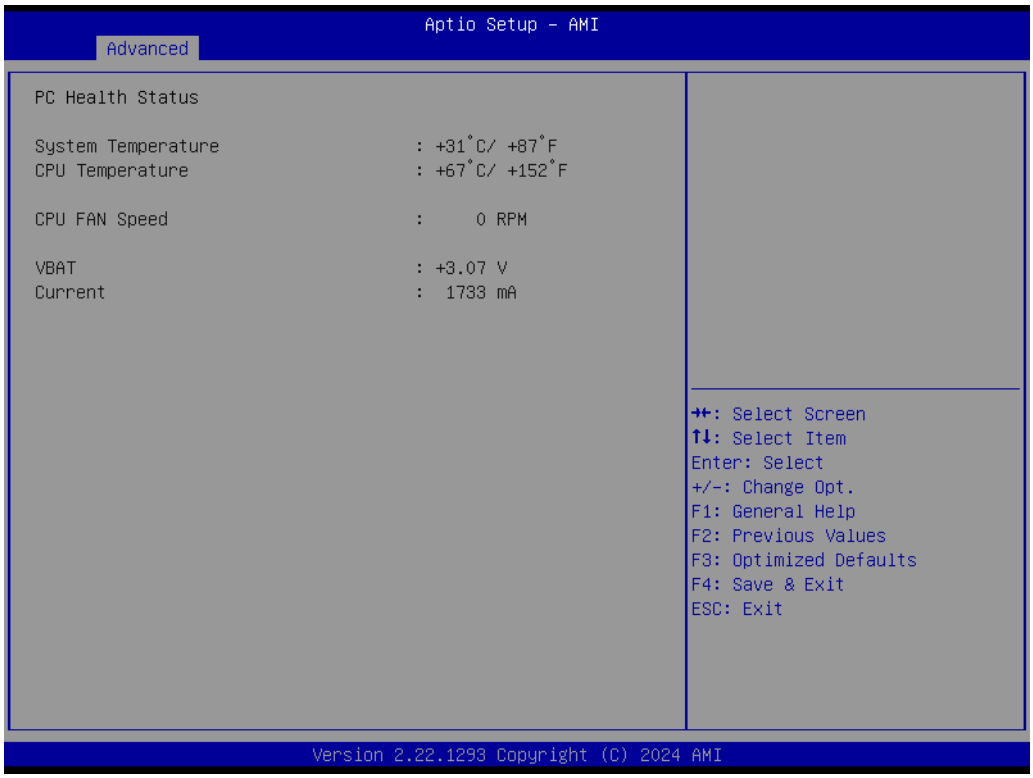
- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select an optimal settings for a Super IO device.
- **COM Port Mode**
  COM Port Mode Select.

4.1.2.8.4 Serial Port 4 Configuration

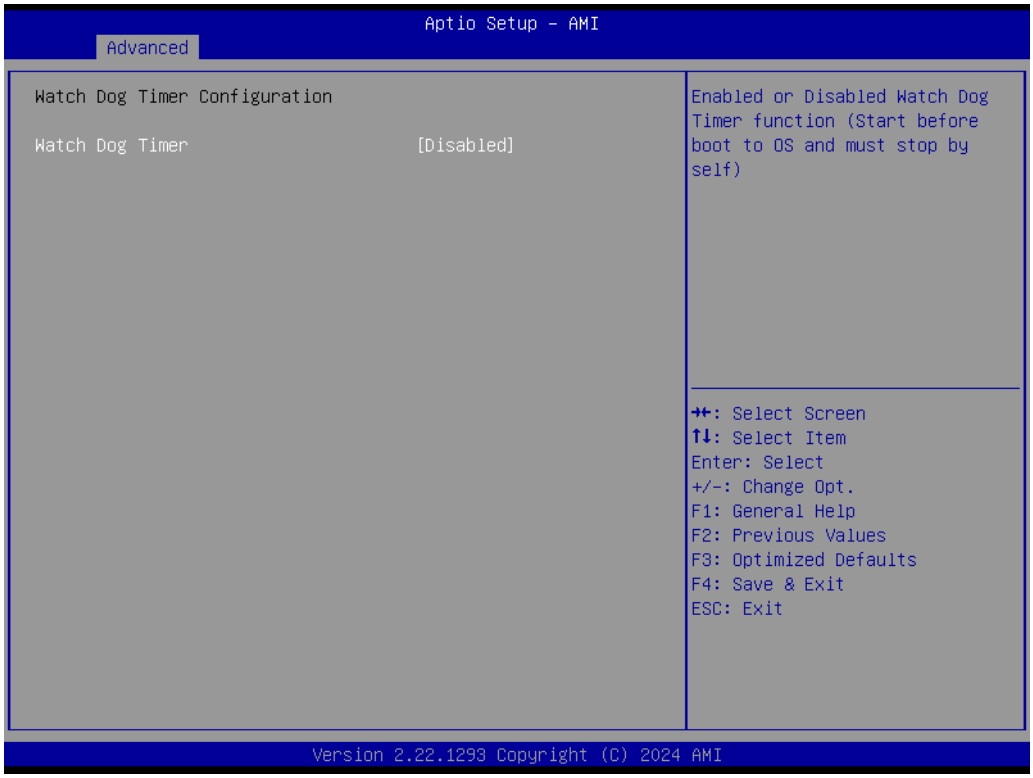


- **Serial Port**
  Enable or Disable Serial Port (COM).
- **Change Settings**
  Select optimal settings for a Super IO device.
- **COM Port Mode**
  COM Port Mode Select.

4.1.2.8.5Hardware Monitor

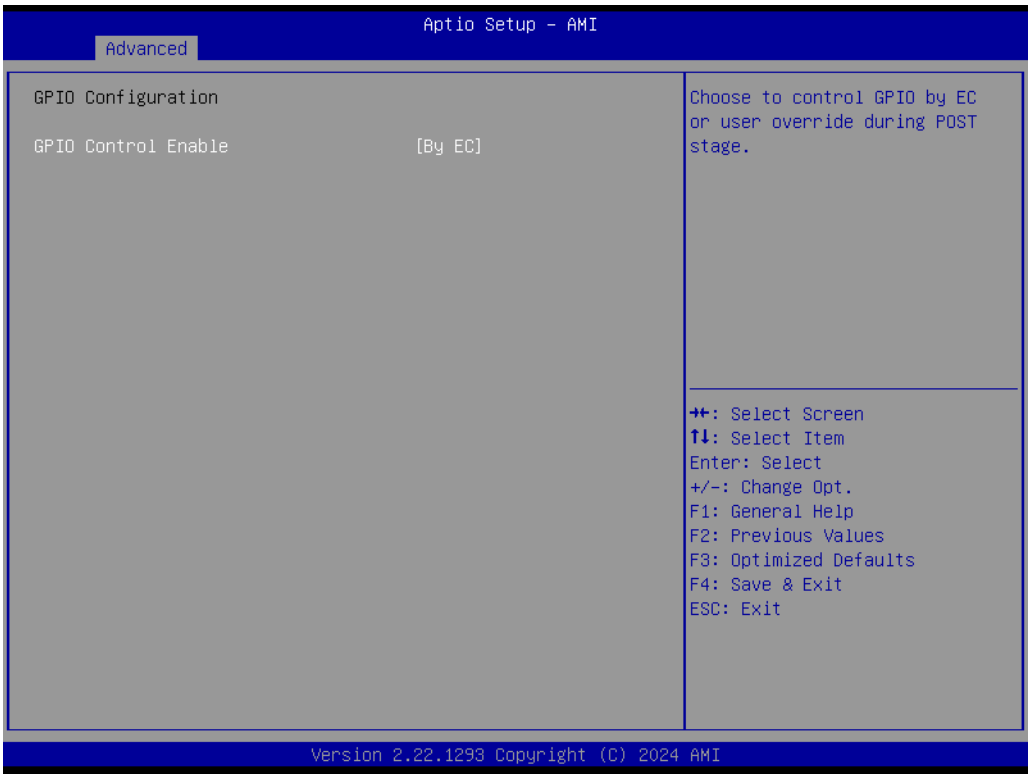


4.1.2.8.6Watch Dog Timer Configuration



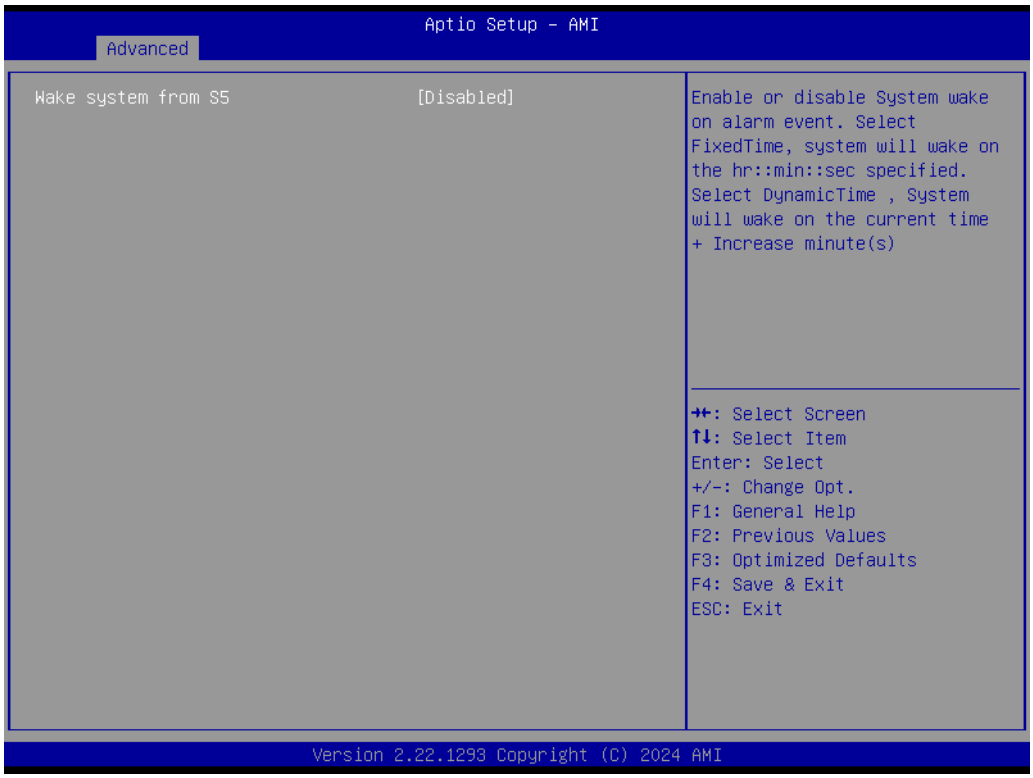
- **Watch Dog Timer**
  Enable or Disable the Watch Dog Timer Function.

4.1.2.8.7GPIO Configuration



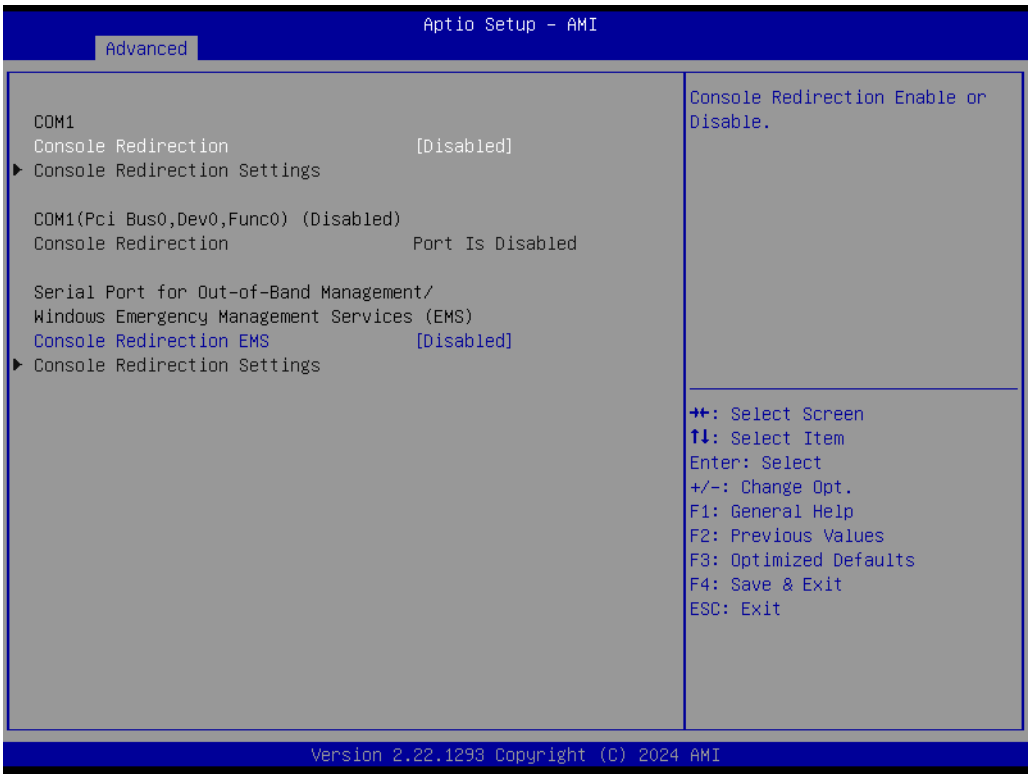
- **GPIO Control Enable**
  Choose to control GPIO by EC or user override during POST stage.
- **GPIO0/1/2/3/4/5/6/7**
  Configure GPIO0/1/2/3/4/5/6/7.

4.1.2.9 S5 RTC Wake Settings



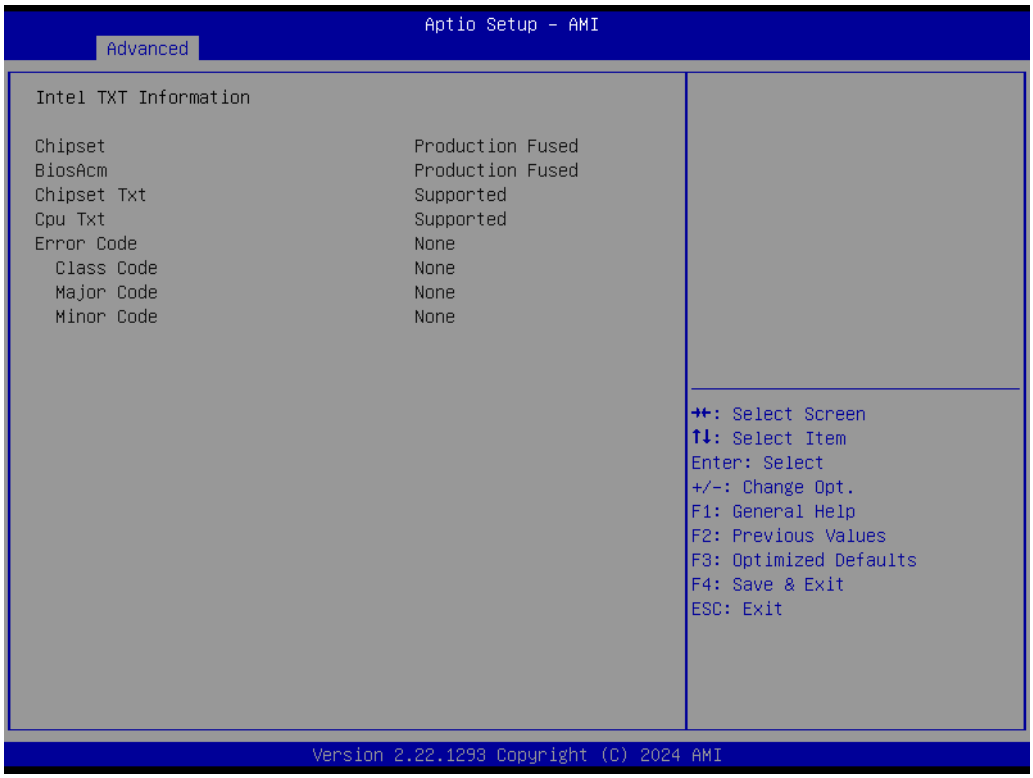
- **Wake system from S5**
  Enable or disable System wake on alarm event. Select FixedTime for the system to wake on the hr:min:sec specified.

4.1.2.10 Serial Port Console Redirection



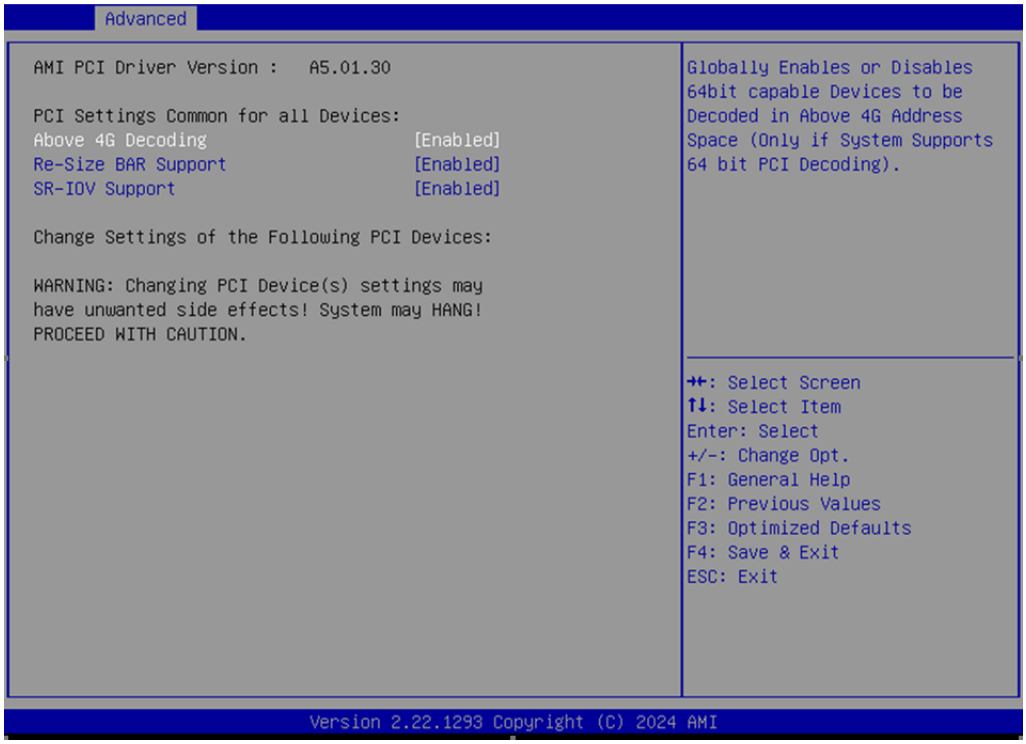
- **Console Redirection**
  This item allows users to configure console redirection detail settings.
- **Console Redirection EMS**
  This item allows users to enable or disable console redirection for Microsoft Windows Emergency Management Services (EMS).

4.1.2.11 Intel TXT Information



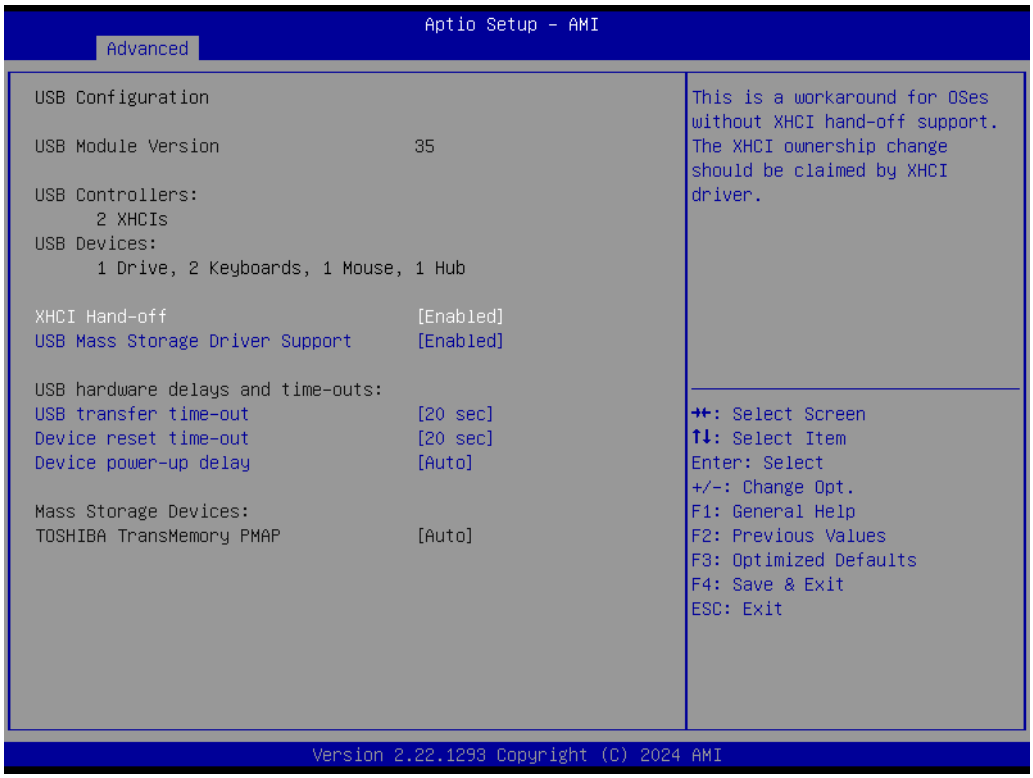
- **Intel TXT Information**
  Display Intel TXT information.

4.1.2.12 PCI Subsystem Settings



- **Above 4G Decoding**
  Globally Enables or Disables 64-bit capable Devices to be Decoded in the Above 4G Address Space. (Only if the system supports 64-bit PCI Decoding).
- **Re-size BAR Support**
  If the system has Resizable BAR capable PCIe Devices, this option Enables or Disables Resizable BAR Support.
- **SR-IOV Support**
  If the system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.

4.1.2.13 USB Configuration

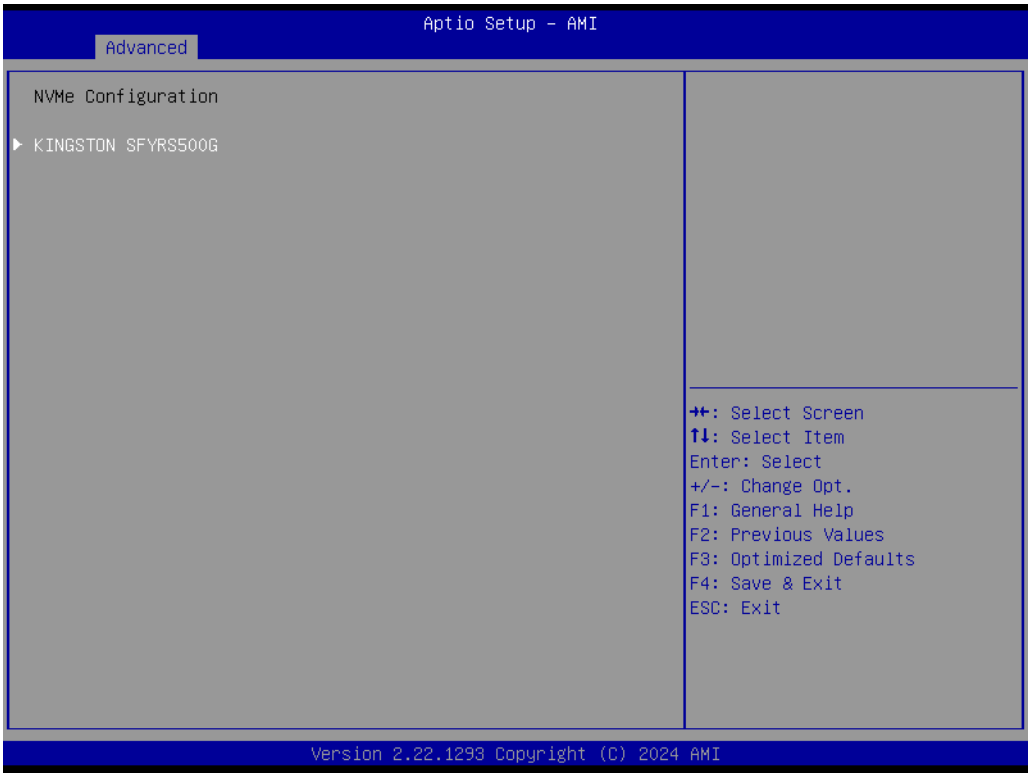


- **Legacy USB Support**
  Enables Legacy USB support. The AUTO option disables legacy support if no USB devices are connected. The DISABLE option will keep USB devices available only for EFI applications.
- **XHCI Hand-off**
  This is a workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
- **USB Mass Storage Driver Support**
  Enable/Disable USB Mass Storage Driver Support.
- **USB transfer time-out**
  Time-out value for control, Bulk, and interrupt transfers.
- **Device reset time-out**
  USB mass storage device start unit command time-out.
- **Device power-up delay**
  Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses a default value: for a Root port it is 100 ms, for a Hub port the delay is taken from the Hub descriptor.

4.1.2.14 Network Stack Configuration

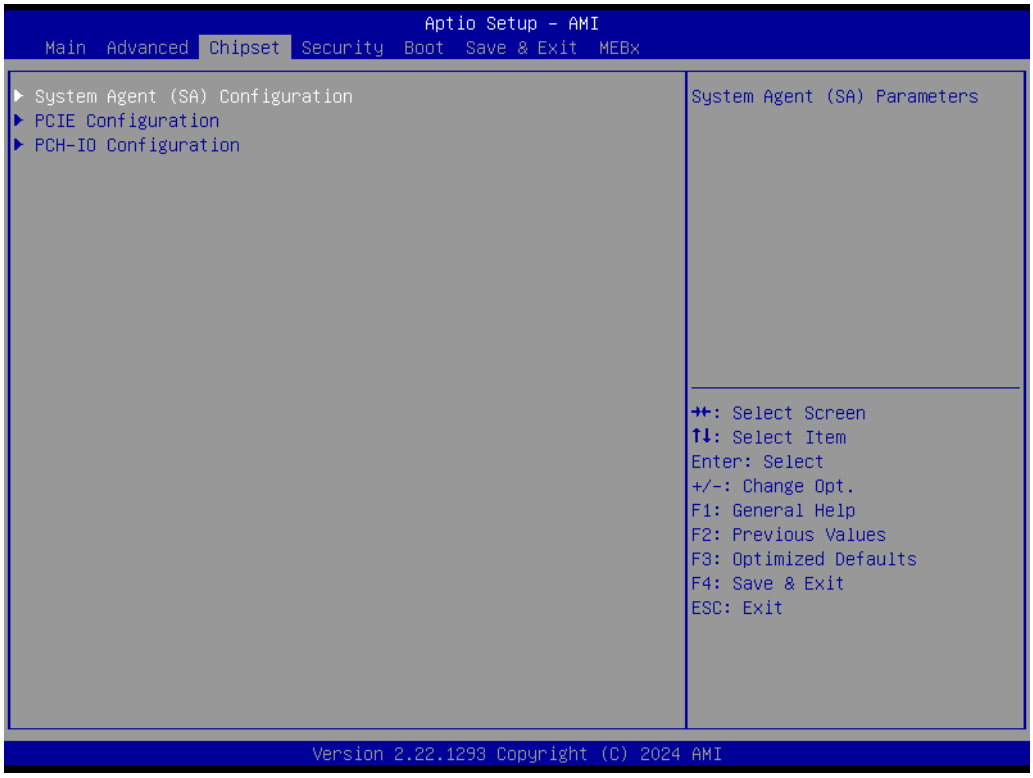
- **Network Stack**
  Enable/Disable UEFI Network Stack.

4.1.2.15 NVMe Configuration



4.1.3 Chipset Configuration

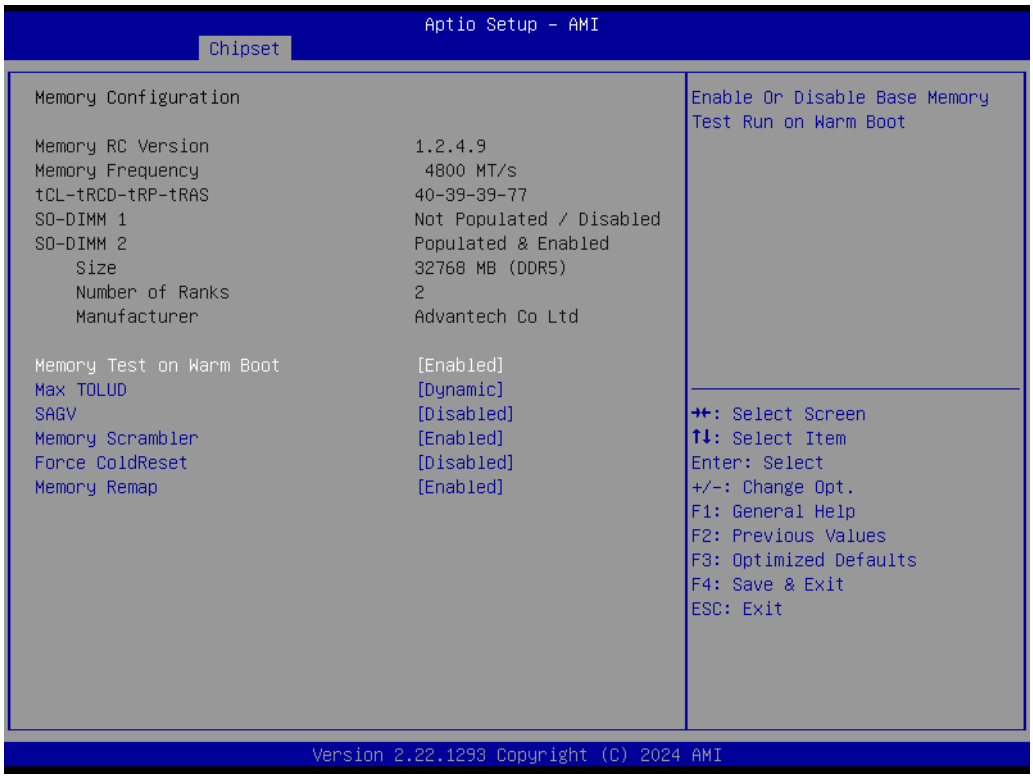
Select the Chipset tab from the ASR-A502 setup screen to enter the Chipset BIOS Setup screen. You can display a Chipset BIOS Setup option by highlighting it using the <Arrow> keys. All Plug and Play BIOS Setup options are described in this section. The Plug and Play BIOS Setup screen is shown below.



4.1.3.1 System Agent (SA) Configuration

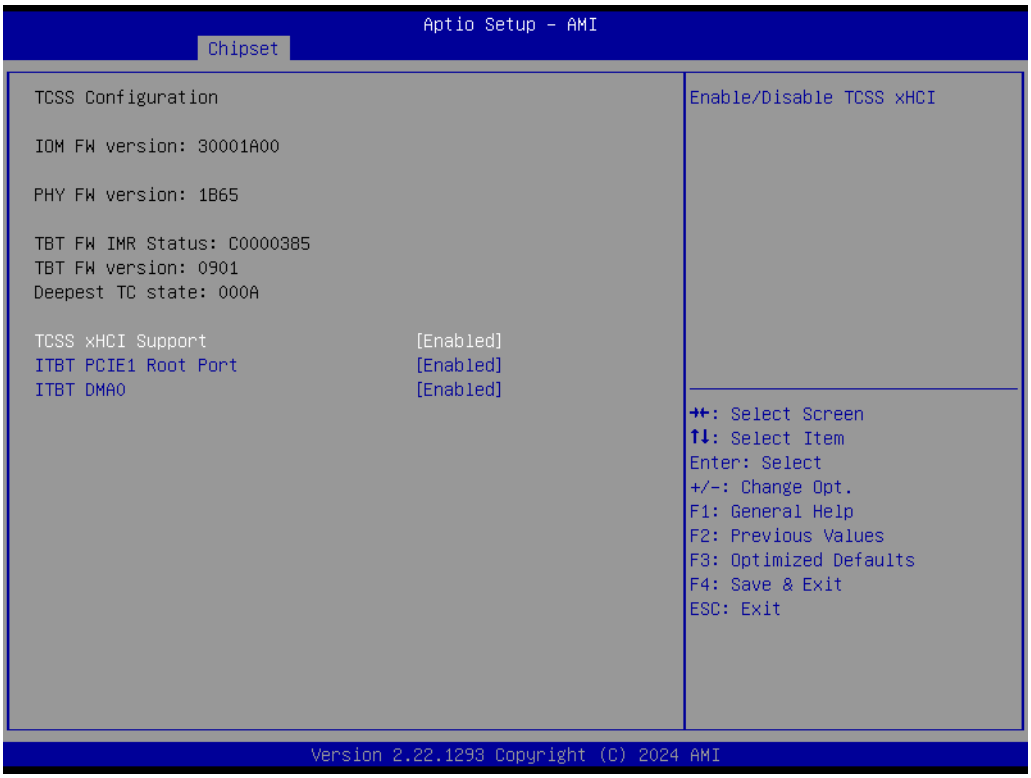
- **Memory Configuration**
  Memory Configuration Parameters.
- **TCSS setup menu**
  TCSS Configuration settings.
- **VMD setup menu**
  VMD setup
- **VT-d**
  VT-D capability.

4.1.3.1.1 Memory Configuration



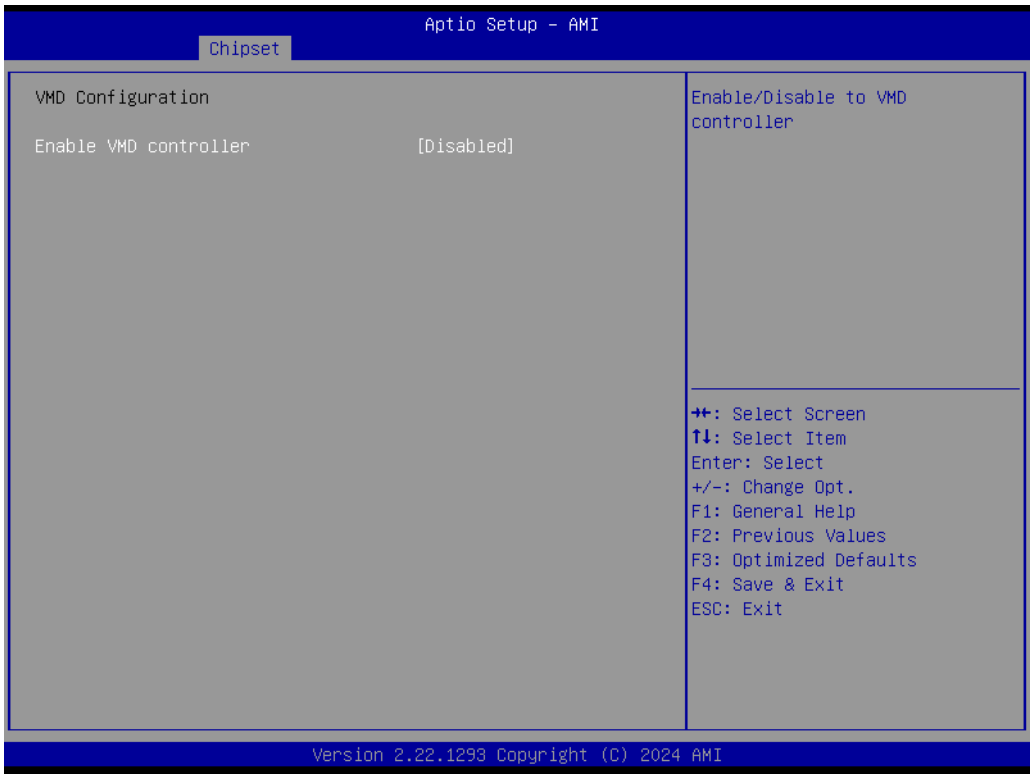
- **Memory Test on Warm Boot**
  Enable/Disable Base Memory Test Run on Warm Boot.
- **Max TOLUD**
  Maximum Value of TOLUD.
- **SA GV**
  System Agent Geyserville.
- **Memory Scrambler**
  Enable/Disable Memory Scrambler support.
- **Force ColdReset**
  Force ColdReset OR Choose MrcColdBoot mode.
- **Memory Remap**
  Enable/Disable Memory Remap above 4GB.

4.1.3.1.2TCSS Setup Menu

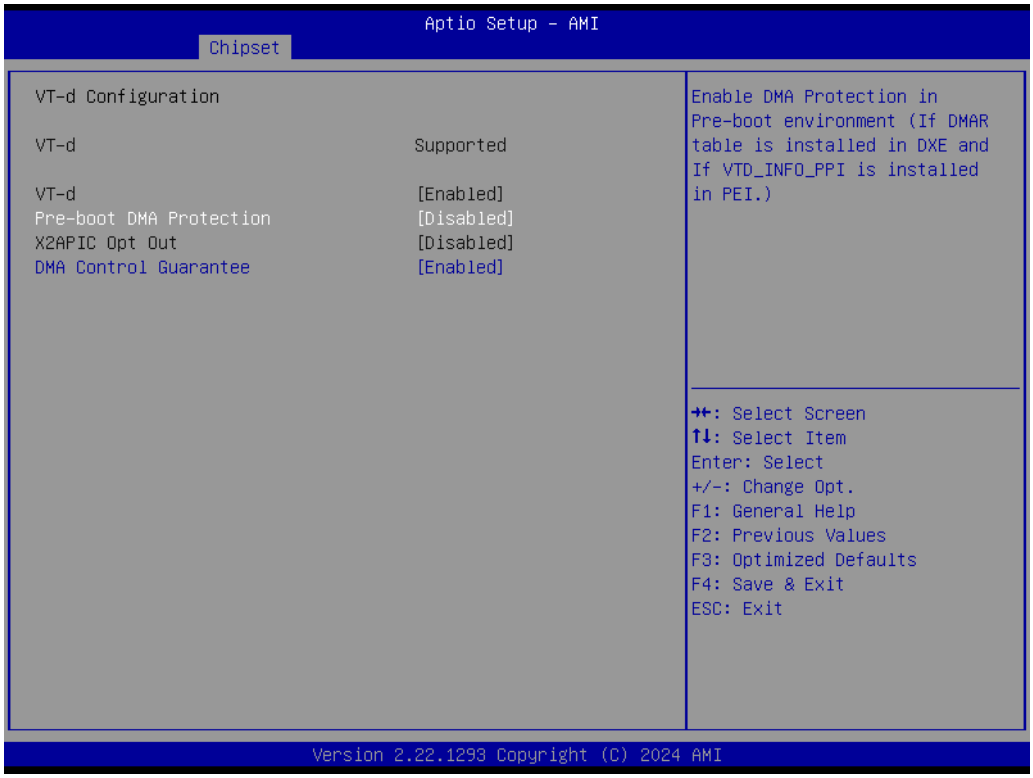


- **TCSS xHCI Support**
  Enable/Disable TCSS xHCI.
- **ITBT PECI1 Root Port**
  Enable/Disable ITBT PCIE Root.
- **ITBT DMA0**
  Enable/Disable ITBT DMA0.

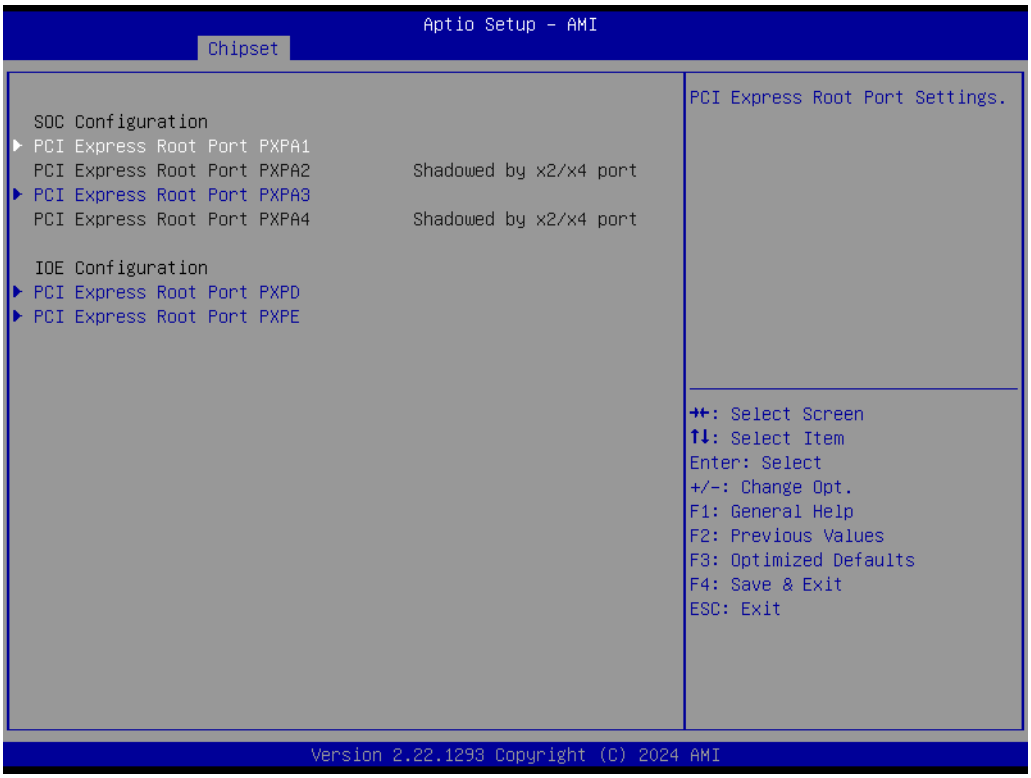
4.1.3.1.3VMD Setup Menu



4.1.3.1.4VT-d Setup Menu

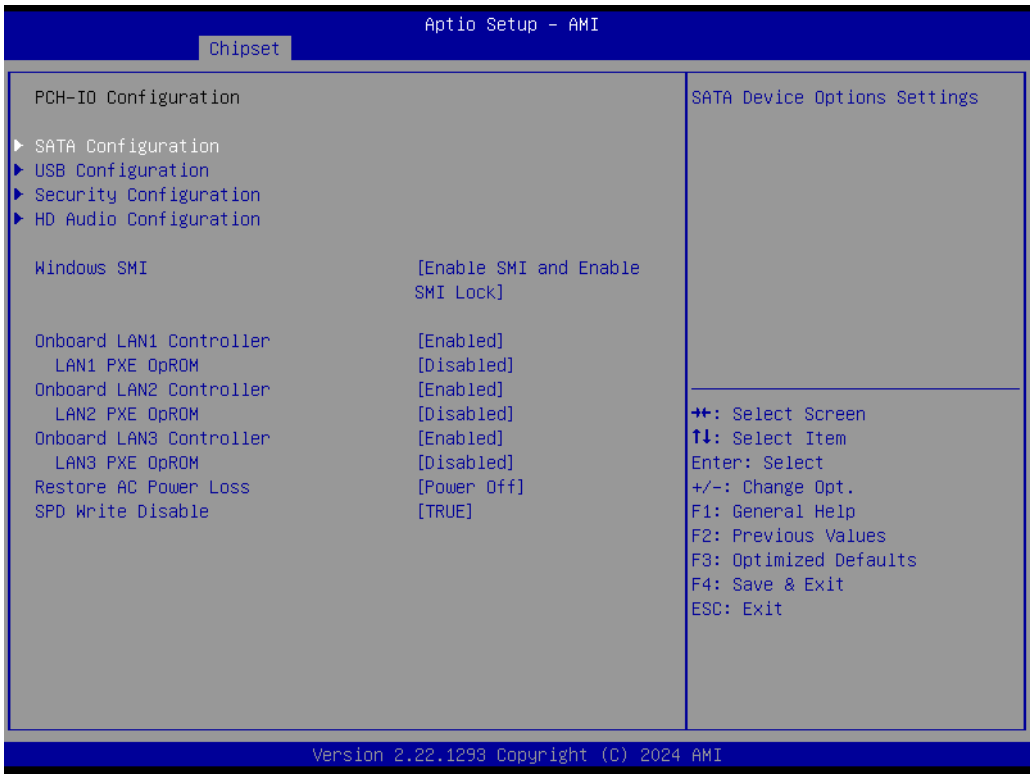


4.1.3.2 PCI Express Configuration



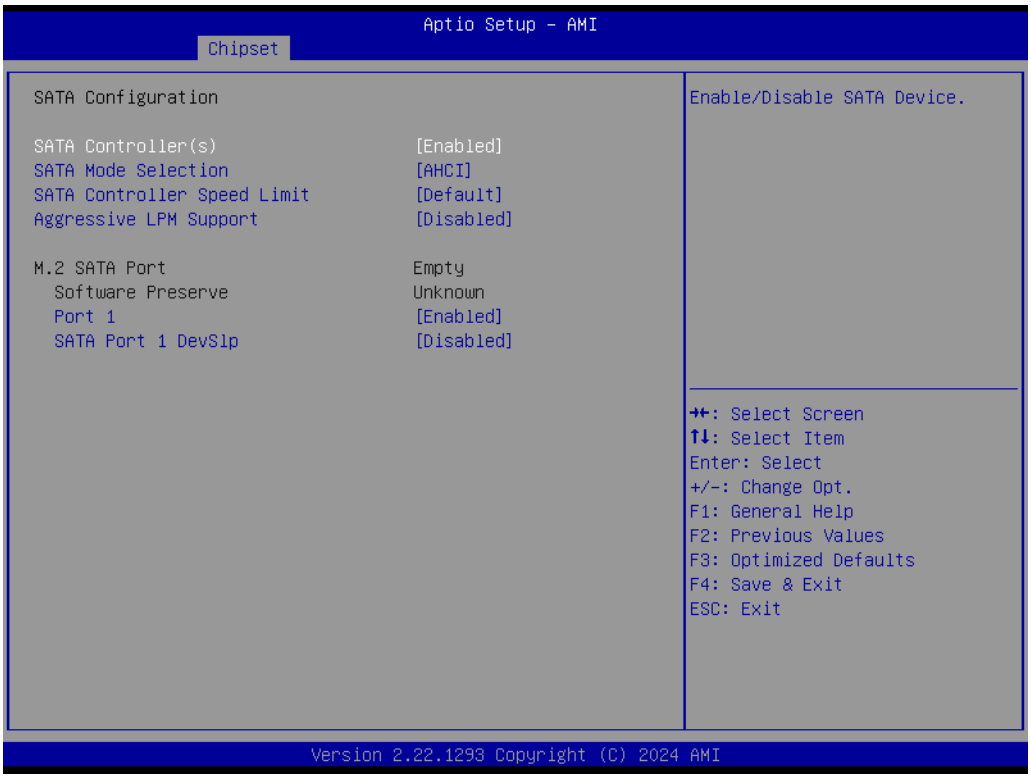
- **PCI Express Root Port PXPA1/PXPA2/PXPA3/PXPA4/PXPD/PXPE**
  PCI Express Root Port Settings.

4.1.3.3 PCH-IO Configuration



- **SATA Configuration**
  SATA Device Options Settings.
- **USB Configuration**
  USB Configuration Settings.
- **Security Configuration**
  Security Configuration Settings.
- **HD Audio Configuration**
  HD Audio Subsystem Configuration Settings.
- **PCH LAN Controller**
  Enable or Disable onboard NIC.
- **Wake on LAN Enable**
  Enable or Disable Integrated LAN to wake the system.
- **LAN1 PXE ROM**
  Enable or disable boot option for LAN1 Controller.
- **Onboard LAN2 Controller**
  Select to Enable or Disable onboard LAN2 Controller.
- **LAN2 PXE ROM**
  Enable or disable boot option for LAN2 Controller.
- **Restore AC Power Loss**
  Specify what state to go to when power is re-applied after a power failure (G3 state).
- **SPD Write Disable**
  Enable/Disable setting SPD Write Disable.

4.1.3.3.1 SATA Configuration

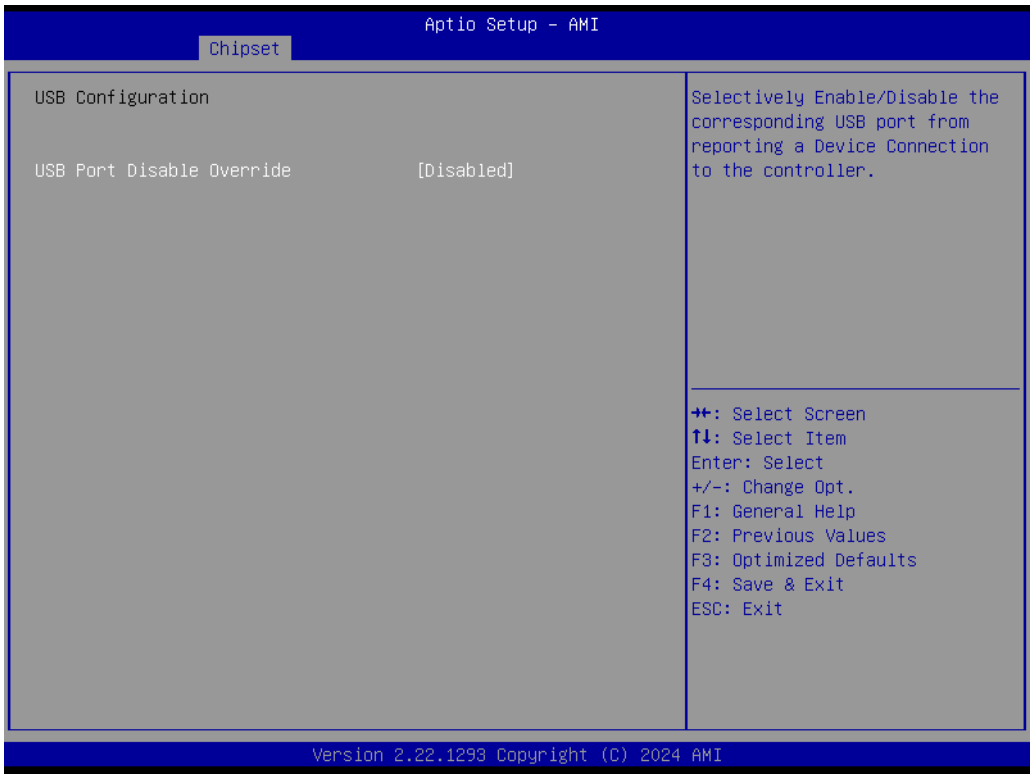


- **SATA Controller**
  Enable or Disable SATA Device.
- **SATA Mode Selection**
  Determines how SATA controllers operate.
- **SATA Controller Speed Limit**
  Indicates the maximum speed the SATA controller can support.
- **Aggressive LPM Support**
  Enable PCH to aggressively enter link power state.

M.2 SATA Port

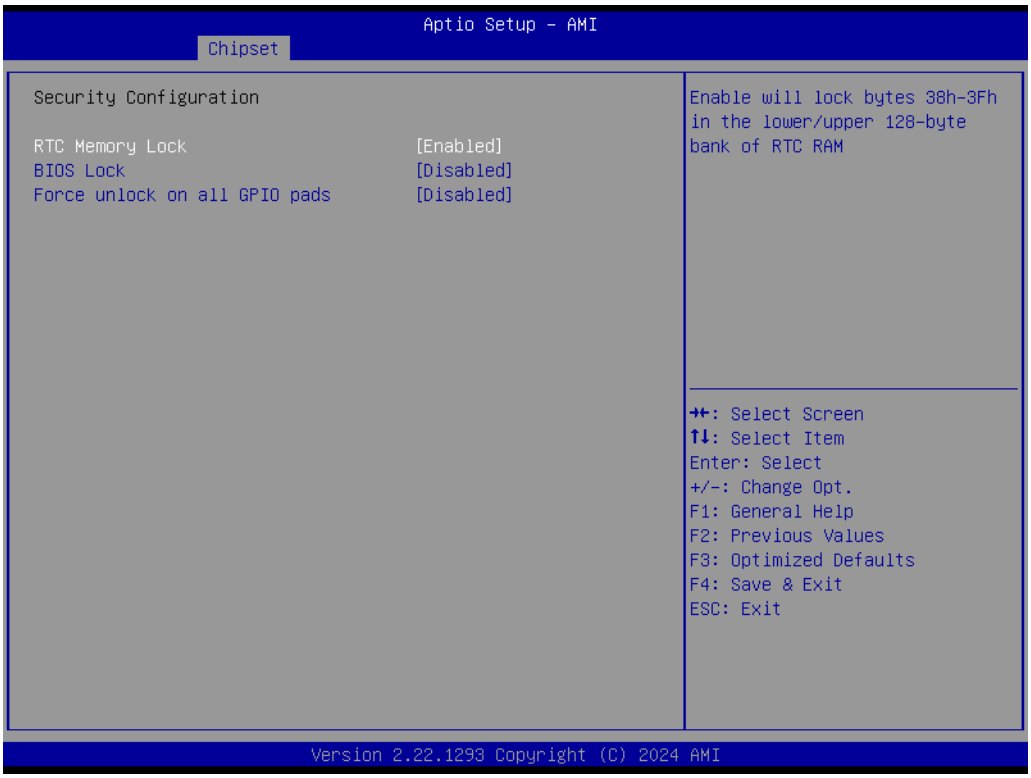
- **Port 1**
  Enable or Disable SATA Port.
- **SATA Port 1 DevSlp**
  Enable/Disable SATA Port 1 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen.

4.1.3.3.2USB Configuration



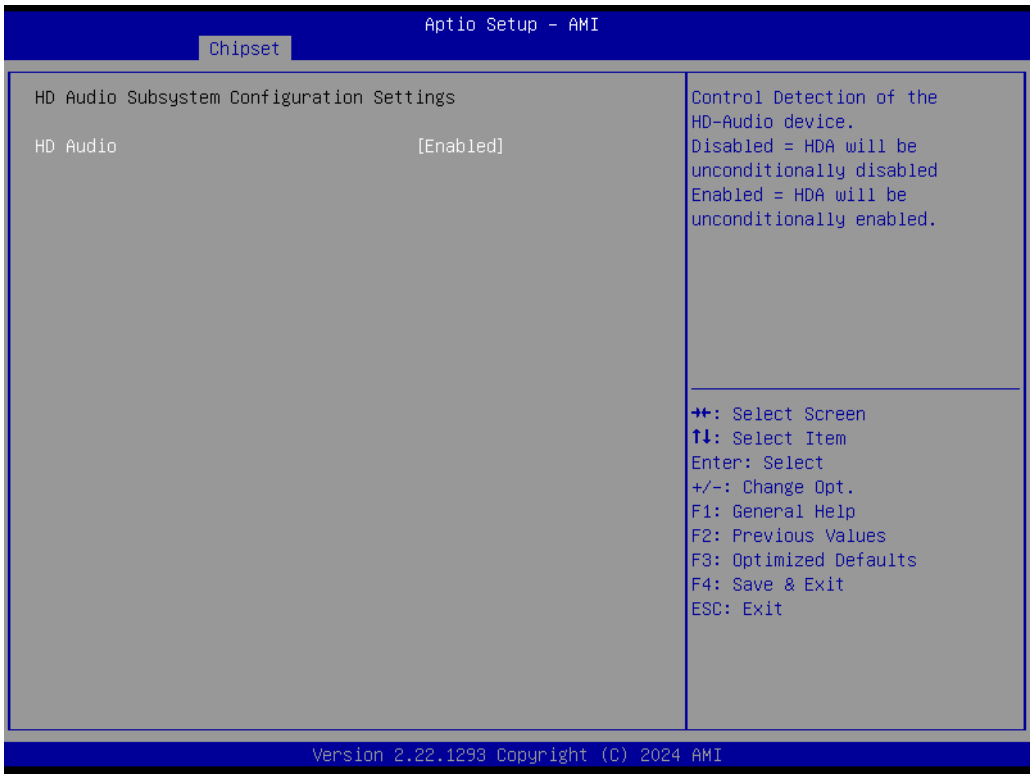
- **USB Port Disable Override**
  Selectively Enable/Disable the corresponding USB Port from reporting a Device Connection to the Controller.

4.1.3.3.3Security Configuration



- **RTC Memory Lock**
  Enable will lock bytes 38h-3Fh in the lower/upper 128-byte bank of RTC RAM.
- **BIOS Lock**
  Enable or Disable the PCH BIOS Lock Enable feature.
- **Force unlock on all GPIO pads**
  If Enabled, the BIOS will force all GPIO pads to be in an unlocked state.

4.1.3.3.4HD Audio Configuration



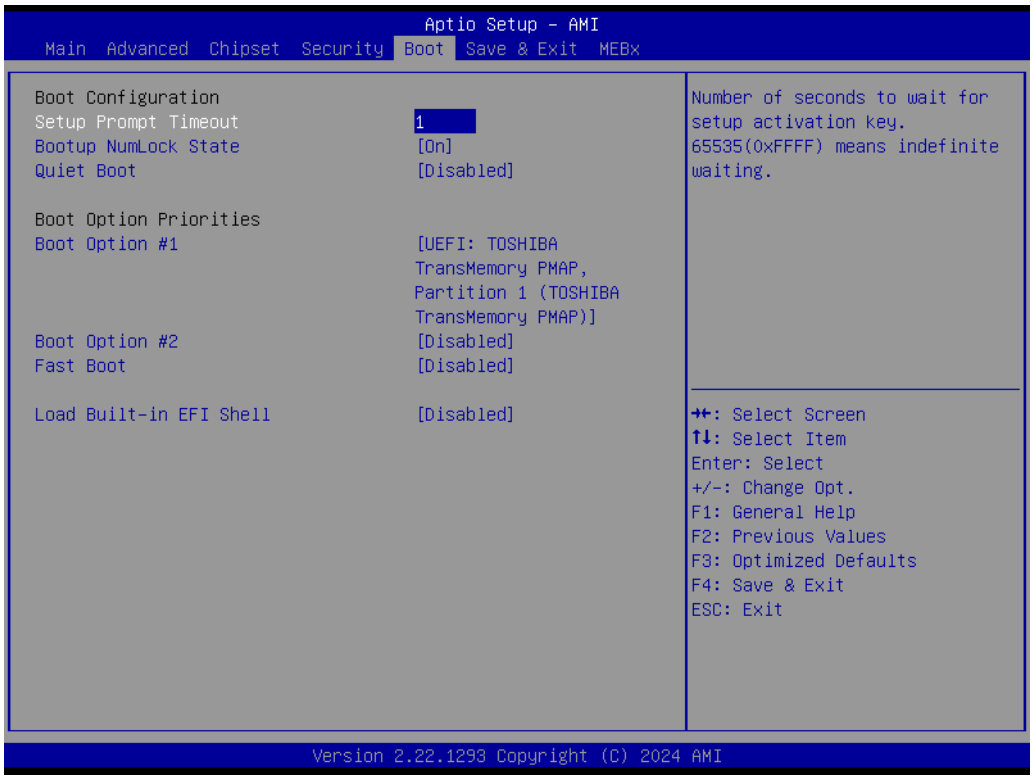
- **HD Audio**
  Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled. Enabled = HDA will be unconditionally Enabled.

4.1.4 Security

Select Security Setup from the ASR-A502 Setup main BIOS setup menu. All Security Setup options, such as password protection and virus protection are described in this section. To access the sub-menu for the following items, select the item and press <Enter>:

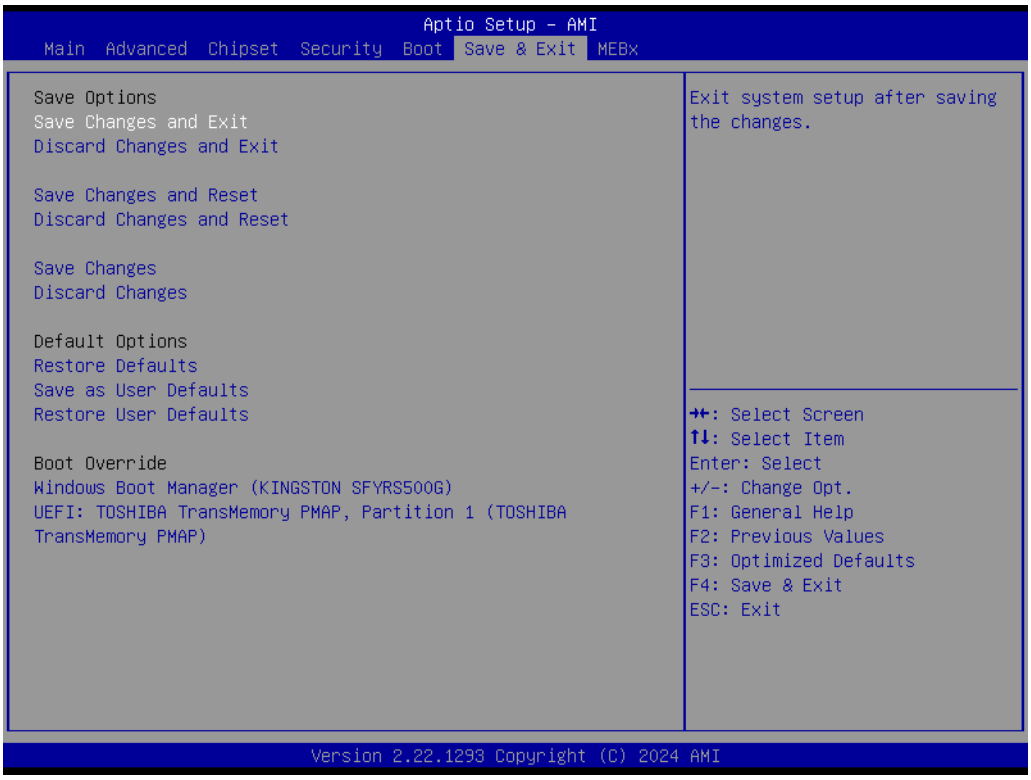
- **Change Administrator/User Password**
  Select this option and press <ENTER> to access the sub-menu, and then type in the password.
- **Secure Boot**
  Secure Boot Configurations.

4.1.5 Boot



- **Setup Prompt Timeout**
  Number of seconds that the firmware will wait before initiating the original default boot selection. A value of 0 indicates that the default boot selection is to be initiated immediately on boot. A value of 65535(0xFFFF) indicates that firmware will wait for user input before booting. This means the default boot selection is not automatically started by the firmware.
- **Bootup NumLock State**
  Select the keyboard NumLock state.
- **Quiet Boot**
  Enables or Disables the Quiet Boot option.
- **Boot Option #1**
  Sets the system boot order.
- **Fast Boot**
  Enables or Disables boot with initialization of a minimal set of devices required to launch the active boot option. It has no effect on BBS boot options.

4.1.6 Save & Exit



- **Save Changes and Exit**
  This item allows you to exit system setup after saving the changes.
- **Discard Changes and Exit**
  This item allows you to exit system setup without saving any changes.
- **Save Changes and Reset**
  This item allows you to reset the system after saving the changes.
- **Discard Changes and Reset**
  This item allows you to rest system setup without saving any changes.
- **Save Changes**
  This item allows you to save changes done so far to any of the options.
- **Discard Changes**
  This item allows you to discard changes done so far to any of the options.
- **Restore Defaults**
  This item allows you to restore default values for all the options.
- **Save as User Defaults**
  This item allows you to save the changes done so far as user defaults.
- **Restore User Defaults**
  This item allows you to restore the user defaults to all the options.
- **Boot Override**
  Boot device select can override your boot priority.

Appendix A

System Assignments

A.1 System I/O Ports

Table A.1: System I/O Ports

Addr. Range (Hex)	Device
00h-1Fh	DMA Controller
20h-2Dh	Interrupt Controller
2Eh–2Fh	Motherboard resources
30h-3Dh	Interrupt Controller
40h-43h	Timer/Counter
4Eh–4Fh	Motherboard resources
50h-53h	Timer/Counter
60h-6Fh	8042 (keyboard controller)/NMI Controller/Microcontroller
70h-7Fh	Real-time Controller
80h-8Fh	Debug Port/Reserved
90h-9Fh	Debug Port/Reset Generator
A0h-ADh	Interrupt Controller
B0h-B1h	Interrupt Controller
B4h-BDh	Power Management
200h-27Fh	CAN Bus Controller
280h-28Fh	I2C Controller
290h-29Fh	EC Index port and Data port
2A0h-2BFh	GPIO Controller
2C0h-2DFh	SMBus Controller
2E8h-2EFh	Communications Port (COM4)
2F0h-2F7h	EC/PMC Controller
2F8h-2FFh	Communications Port (COM2)
300h-37Fh	CANBus Controller
3E8h-3EFh	Communications Port (COM3)
3F8h-3FFh	Communications Port (COM1)
480h-4CFh	Motherboard resources
4D0h-4D1h	Interrupt Controller
680h-69Fh	Motherboard resources
A00h-AFFh	Motherboard resources
164Eh-164Fh	Motherboard resources
1800h-18FFh	Motherboard resources
CF9h-CF9h	Reset Generator

A.2 DMA Channel Assignments

Table A.2: DMA Channel Assignments	
Channel	**Function**
0	Available
1	Available
2	Available
3	Available
4	Direct memory access controller
5	Available
6	Available
7	Available

A.3 1st MB Memory Map

Table A.3: 1st MB Memory Map	
Addr. Range (Hex)	**Device**
E0000h - FFFFFh	System board
D0000h - DFFFFh	PCI Bus
C0000h - CFFFFh	System board
A0000h - BFFFFh	PCI Bus
A0000h - BFFFFh	Intel® HD Graphics
00000h - 9FFFFh	System board

A.4 Interrupt Assignments

Table A.4: Interrupt Assignments	
Interrupt#	**Interrupt source**
NMI	Parity error detected
IRQ0	System timer
IRQ1	Using SERIRQ, Keyboard Emulation
IRQ2	Interrupt from controller 2 (cascade)
IRQ3	Communications Port (COM2)
IRQ4	Communications Port (COM1)
IRQ5	EC Watch Dog
IRQ6	CAN Bus Controller
IRQ7	Communications Port (COM3)
IRQ8	System CMOS/real time clock
IRQ9	Microsoft ACPI-Compliant System
IRQ10	Communications Port (COM4)
IRQ11	Display Controller
IRQ12	Available
IRQ13	Numeric data processor
IRQ14	GPIO Controller
IRQ15	Reserved

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