innodisk

The Total Solution For Industrial Flash Storage

Approval Sheet

Customer	
Product Number	**M3S0-2GMVFCQE**
Module speed	**PC3-14900**
Pin	**204 pin**
Cl-tRCD-tRP	**13-13-13**
Operating Temp	**0℃~85℃**
Date	**26th August 2025**

Rev 1.0

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			CL	tRCD	tRP
		CL=9	CL=11	CL=13			
PC3-14900	**T**	1333	1600	1866	13	13	13

- JEDEC Standard 204-pin Small Outline Dual In-Line Memory Module
- Intend for PC3-14900 applications
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.5 Volt (-0.075/+0.075V)
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 96-ball BGA Package
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8μs (TC ≤ +85°C)
- 15/10/1 Addressing (row/column/rank)-2GB
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 5,6,7,8,9,10,11,13
  - Burst Length: switch on-the-fly: BL=8 or BC 4
- RoHS Compliant *(Section 11)*

2. Ordering Information

DDR3 SODIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M3S0-2GMVFCQE	2GB	PC3-14900	256Mx64	4	1	N

3. Pin Configurations (Front side/Back side)

X64 SODIMM

Front						Back					
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	69	DQ27	137	DQS4	2	VSS	70	DQ31	138	VSS
3	VSS	71	VSS	139	VSS	4	DQ4	72	VSS	140	DQ38
5	DQ0	73	CKE0	141	DQ34	6	DQ5	74	CKE1	142	DQ39
7	DQ1	75	VDD	143	DQ35	8	VSS	76	VDD	144	VSS
9	VSS	77	NC	145	VSS	10	/DQS0	78	A15*	146	DQ44
11	DM0	79	BA2	147	DQ40	12	DQS0	80	A14*	148	DQ45
13	VSS	81	VDD	149	DQ41	14	VSS	82	VDD	150	VSS
15	DQ2	83	A12, /BC	151	VSS	16	DQ6	84	A11	152	/DQS5
17	DQ3	85	A9	153	DM5	18	DQ7	86	A7	154	DQS5
19	VSS	87	VDD	155	VSS	20	VSS	88	VDD	156	VSS
21	DQ8	89	A8	157	DQ42	22	DQ12	90	A6	158	DQ46
23	DQ9	91	A5	159	DQ43	24	DQ13	92	A4	160	DQ47
25	VSS	93	VDD	161	VSS	26	VSS	94	VDD	162	VSS
27	/DQS1	95	A3	163	DQ48	28	DM1	96	A2	164	DQ52
29	DQS1	97	A1	165	DQ49	30	/RESET	98	A0	166	DQ53
31	VSS	99	VDD	167	VSS	32	VSS	100	VDD	168	VSS
33	DQ10	101	CK0	169	/DQS6	34	DQ14	102	CK1	170	DM6
35	DQ11	103	/CK0	171	DQS6	36	DQ15	104	/CK1	172	VSS
37	VSS	105	VDD	173	VSS	38	VSS	106	VDD	174	DQ54
39	DQ16	107	A10, /AP	175	DQ50	40	DQ20	108	BA1	176	DQ55
41	DQ17	109	BA0	177	DQ51	42	DQ21	110	/RAS	178	VSS
43	VSS	111	VDD	179	VSS	44	VSS	112	VDD	180	DQ60
45	/DQS2	113	/WE	181	DQ56	46	DM2	114	/S0	182	DQ61
47	DQS2	115	/CAS	183	DQ57	48	VSS	116	ODT0	184	VSS
49	VSS	117	VDD	185	VSS	50	DQ22	118	VDD	186	/DQS7
51	DQ18	119	A13*	187	DM7	52	DQ23	120	ODT1	188	DQS7
53	DQ19	121	/S1	189	VSS	54	VSS	122	NC	190	VSS
55	VSS	123	VDD	191	DQ58	56	DQ28	124	VDD	192	DQ62
57	DQ24	125	NC	193	DQ59	58	DQ29	126	VREFCA	194	DQ63
59	DQ25	127	VSS	195	VSS	60	VSS	128	VSS	196	VSS
61	VSS	129	DQ32	197	SA0	62	/DQS3	130	DQ36	198	/EVENT, NF
63	DM3	131	DQ33	199	VDDSPD	64	DQS3	132	DQ37	200	SDA
65	VSS	133	VSS	201	SA1	66	VSS	134	VSS	202	SCL
67	DQ26	135	/DQS4	203	VTT	68	DQ30	136	DM4	204	VTT

* This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

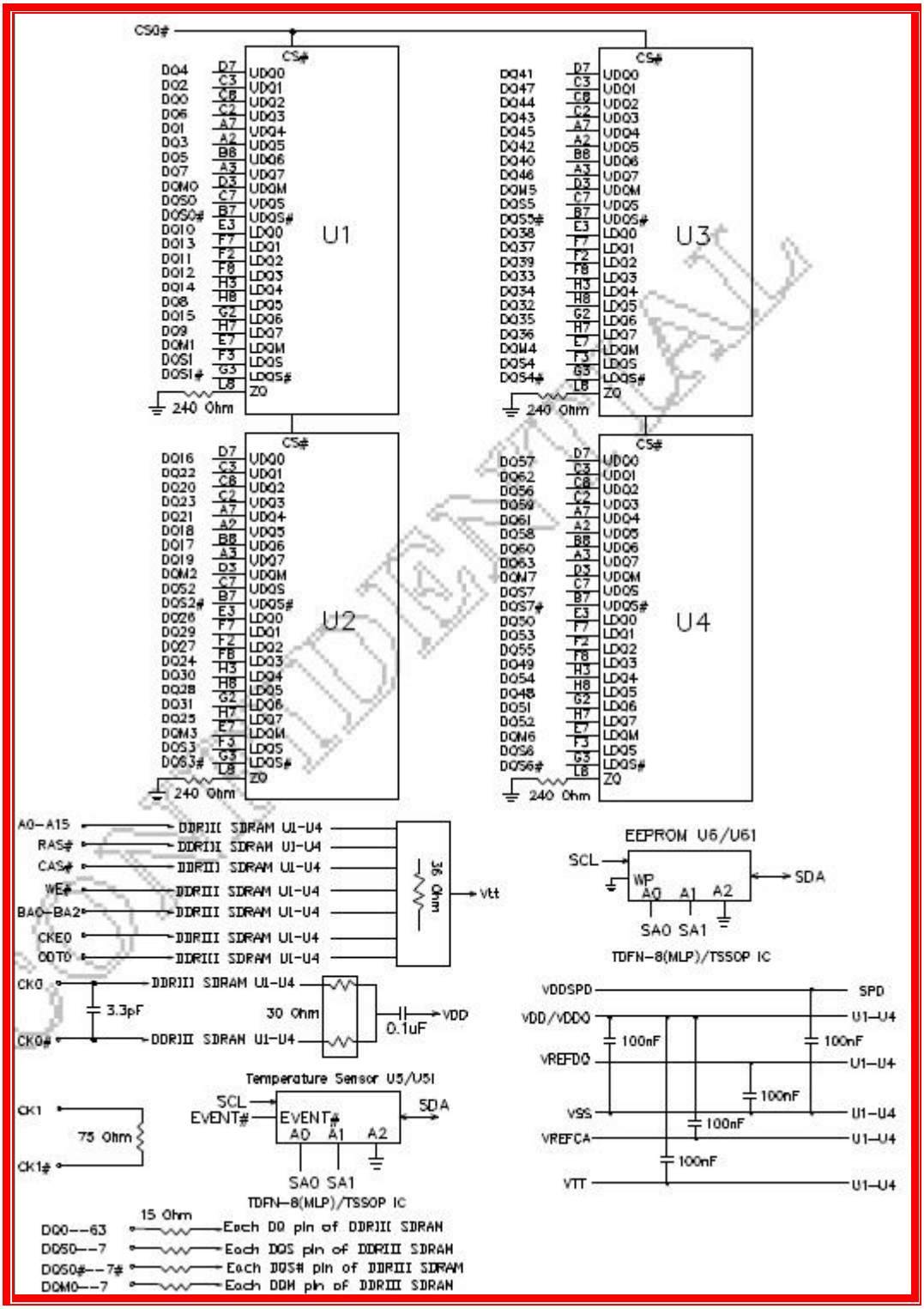
4. Architecture

Pin Definition

Pin Description					
Pin Name	Description	Number	Pin Name	Description	Number
CK[1:0]	Clock Inputs, positive line	2	DQ[63:0]	Data Input/Output	64
/CK[1:0]	Clock inputs, negative line	2	DM[7:0]	Data Masks	8
CKE[1:0]	Clock Enables	2	DQS[7:0]	Data strobes	8
/RAS	Row Address Strobe	1	/DQS[7:0]	Data strobes complement	8
/CAS	Column Address Strobe	1	/RESET	Reset Pin	1
/WE	Write Enable	1	TEST	Logic Analyzer specific test pin (No connect on SO-DIMM)	1
/S[1:0]	Chip Selects	2	/EVENT	Temperature event pin	1
A[9:0],A11,A[15:13]	Address Inputs	14	VDD	Core and I/O Power	18
A10,AP	Address Input/Autoprecharge	1	VSS	Ground	52
A12,/BC	Address Input/Burst chop	1			
BA[2:0]	SDRAM Bank Address	3	VREFDQ, VREFCA	Input/Output Reference	2
ODT[1:0]	On-die termination control	2	VDDSPD	SPD and Temp sensor Power	1
SCL	Serial Presence Detect (SPD) and Thermal sensor(TS) Clock Input	1	Vtt	Termination voltage	2
SDA	SPD and TS Data Input/Output	1	NC	Reserved for future use	2
SA[1:0]	SPD and TS address	2		**Total:**	**204**

5. Function Block Diagram:

- (2GB, 1 Rank, 256Mx16 DDR3L SDRAMs)



6. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 150	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.4 to +1.975	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.4 to +1.975	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.4 to +1.975	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.
3. Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

7. DRAM AC & DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
Recommended DC Operating Conditions - DDR3 (1.5V) operation						
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
VDDSPD	Supply Voltage	3	3.3	3.6	V	
V_{DDQ}	Supply Voltage	1.425	1.5	1.575	V	1,2
Single Ended AC/DC Input Levels						
V_{IH} (DC) DDR3	DC Input High (Logic1) Voltage	+ 90		V_{DD}	mV	3
V_{IL} (DC) DDR3	DC Input Low (Logic 0) Voltage	V_{SS}		- 90	mV	3
V_{IH} (AC) DDR3	AC Input High (Logic1) Voltage	+ 135			mV	3
V_{IL} (AC) DDR3	AC Input Low (Logic 0) Voltage			- 135	mV	3
V_{REFDQ} (DC)	Reference Voltage for DQ, DM inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
V_{REFCA} (DC)	Reference Voltage for ADD,CMD inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
Single Ended AC/DC Output Levels						
V_{OH} (DC)	DC output high measurement level (for IV curve linearity)	-	0.8 x VDDQ	-	V	
V_{OM} (DC)	DC output mid measurement level (for IV curve linearity)	-	0.5 x VDDQ	-	V	
V_{OL} (DC)	DC output low measurement level (for IV curve linearity)	-	0.2 x VDDQ	-	V	
V_{OH} (AC)	AC output high measurement level (for output SR)	-	VTT + 0.1 x VDDQ	-	V	6
V_{OL} (AC)	AC output low measurement level (for output SR)		VTT - 0.1 x VDDQ	-	V	6

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Differential AC/DC Input Levels						
V_{IHdiff} DDR3	Differential Input high	+0.2		Note 9	V	7
V_{ILdiff} DDR3	Differential Input logic Low	Note 9	-	-0.2	V	7

$V_{IHdiff(ac)}$ DDR3	Differential Input high ac	2* ($V_{IH(AC)}$- V_{REF})	-	Note 9	V	8
$V_{ILdiff(ac)}$ DDR3	Differential Input logic Low ac	Note 9	-	2* (V_{REF}- $V_{IL(AC)}$)	V	8
Differential AC and DC Output Levels						
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	-	+ 0.2 x VDDQ	-	V	10
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	-	- 0.2 x VDDQ	-	V	10

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
4. Recommended DC Operating Conditions - DDR3 (1.5V) operation : The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV); Recommended DC Operating Conditions - DDR3L (1.35V) operation: The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 13.5 mV)
5. For reference: approx. VDD/2.
6. The swing of ± 0.1 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2
7. Used to define a differential signal slew-rate.
8. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
9. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot.
10. The swing of ± 0.2 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

8. Operating, Standby, and Refresh Currents

- 2GB SODIMM (1 Rank, 256Mx16 DDR3L SDRAMs)

Symbol	Parameter/Condition		PC3-14900	Unit
I DD0	One bank; Active - Precharge		128	mA
I DD1	One bank; Active - Read - Precharge		180	mA
I DD2N	Precharge Standby Current		68	mA
IDD2NT	Precharge Standby ODT Current		88	mA
I DD2P	Precharge Power Down Current	Fast Mode	48	mA
	Precharge Power Down Current	Slow Mode	48	mA
I DD2Q	Pecharge Quiet Standby Current		60	mA
I DD3N	Active Standby Current		88	mA
I DD3P	Active Power-Down Current		68	mA
I DD4R	Operating Current Burst Read		368	mA
I DD4W	Operating Current Burst Write		424	mA
I DD5B	Burst Refresh Current		624	mA
I DD6	Self-Refresh Current: Normal Temperature Range		60	mA
I DD7	Operating Bank Interleave Read Current		528	mA
I DD8	RESET Low Current		IDD2P + 2mA	mA

9. Timing Parameters

Symbol	Parameter	PC3-14900		Unit
		Min.	Max.	
Clock Timing				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.071	<1.25	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-60	60	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-50	50	Ps
JIT (CC)	Cycle to Cycle Period Jitter	120		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	100		Ps
TERR (2per)	Cumulative error across 2 cycle	-88	88	Ps
TERR (3per)	Cumulative error across 3 cycle	-105	105	Ps
TERR (4per)	Cumulative error across 4 cycle	-117	117	Ps
TERR (5per)	Cumulative error across 5 cycle	-126	126	Ps
TERR (6per)	Cumulative error across 6 cycle	-133	133	Ps
TERR (7per)	Cumulative error across 7 cycle	-139	139	Ps
TERR (8per)	Cumulative error across 3 cycle	-145	145	Ps
TERR (9per)	Cumulative error across 4 cycle	-150	150	Ps
TERR (10per)	Cumulative error across 5 cycle	-154	154	Ps
TERR (11per)	Cumulative error across 6 cycle	-158	158	Ps
TERR (12per)	Cumulative error across 7 cycle	-161	161	Ps

TERR (nper)	Cumulative error across 13~50 cycle	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		Ps
Data Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDQSQ	DQS, DQS# to DQ skew, per group, per access	-	85	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-390	195	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	195	Ps
1.35V				
tDS(base) AC160	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	-	-	Ps
tDS(base) AC135		-	-	Ps
tDS(base) AC125		10	-	Ps
tDH(base) DC90	Data hold time from DQS, DQS# referenced to VIH(DC)VIL(DC) levels	30	-	Ps
1.5V				
tDS(base) AC175	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	-	-	Ps
tDS(base) AC150		-	-	Ps
tDS(base) AC135		68	-	Ps
tDH(base) DC100	Data hold time from DQS, DQS# referenced to VIH(DC)VIL(DC) levels	20	-	Ps
Data Strobe Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tRPRE	DQS,DQS# differential READ Preamble	0.9		tCK(avg)

tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)
tQSH	DQS, DQS# differential output high time	0.4		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.4		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)
tDQSCK	DQS, DQS# rising edge output access time from rising CK, CK#	-195	195	Ps
tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-390	195	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	195	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.27	0.27	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.18	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.18	-	tCK(avg)
Command and Address Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to Internal read command	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			

tRC	Refer to Section 1 Feature			
tCCD		4	-	nCK
tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup(tRP / tCK(avg))		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	34	9* tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4nCK, 5ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4nCK, 6ns)	-	
tFAW	Four activate window for 1KB page size	27	-	ns
tFAW	Four activate window for 2KB page size	35	-	ns
1.35V				
tIS(base) AC160	Command and Address setup time to CK, CK# referenced to VIH(AC) / VIL(AC) levels	-	-	Ps
tIS(base) AC135		-	-	Ps
tIS(base) AC125		75	-	Ps
tIH(base) DC90	Command and Address hold time from CK, CK# referenced to VIH(DC) / VIL(DC) levels	110	-	Ps
1.5V				
tIS(base) AC175	Command and Address setup time to CK, CK# referenced to VIH(AC) / VIL(AC) levels	-	-	Ps
tIS(base) AC150		-	-	Ps
tIS(base) AC135		65	-	Ps
tIS(base) AC125		150	-	Ps
tIH(base) DC100	Command and Address hold time from CK, CK# referenced to VIH(DC) / VIL(DC) levels	100	-	Ps

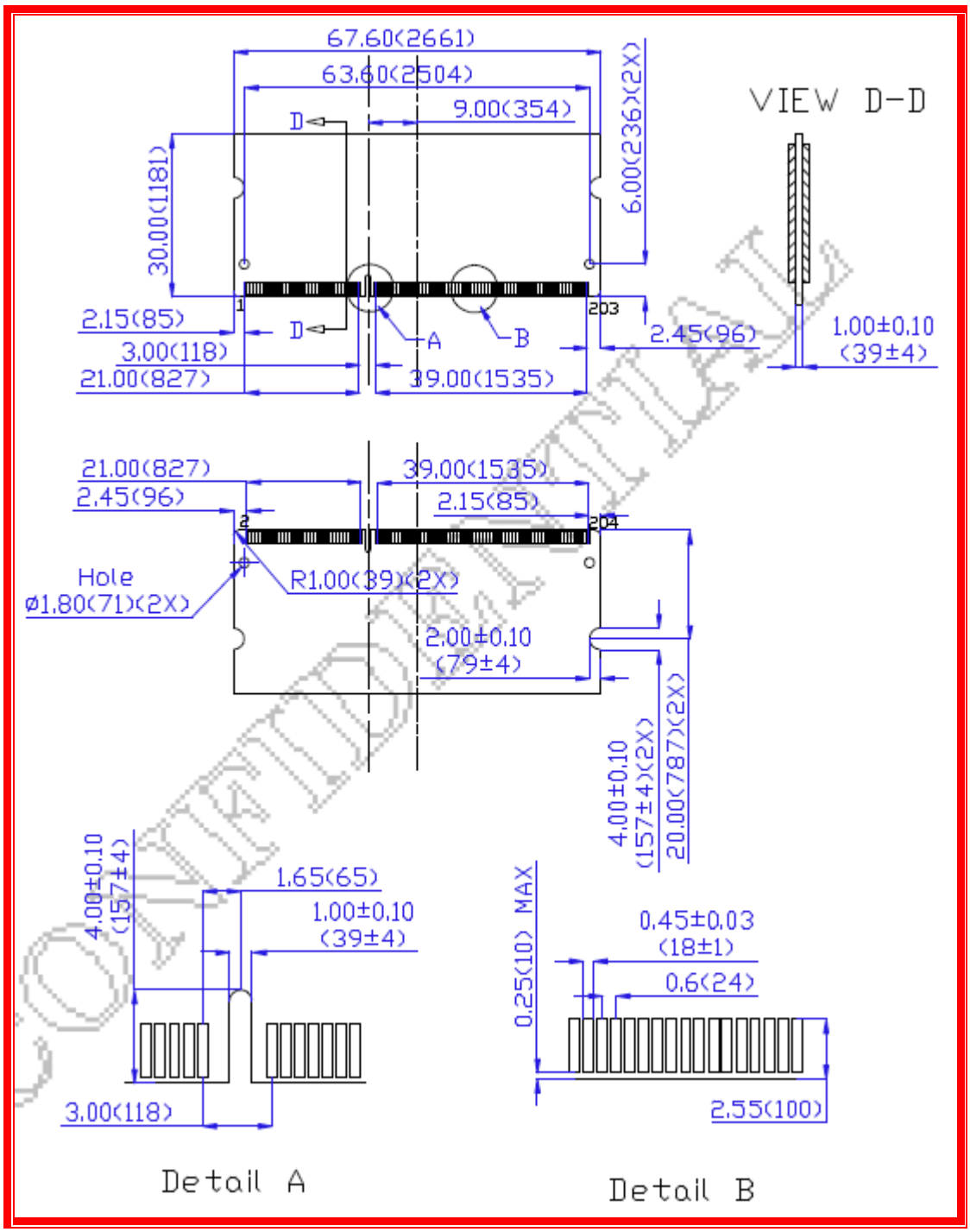
Calibration Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tZQinit	Power-up and RESET calibration time	Max. (512nCK, 640ns)	-	nCK
tZQoper	Normal operation Full calibration time	Max. (256nCK, 320ns)	-	nCK
tZQCS	Normal operation Short calibration time	Max. (64nCK, 80ns)	-	nCK
Reset Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK,tRFC(min) +10ns)	-	
Self Refresh Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXS	Exit Self Refresh to commands not requiring a locked DLL	Max(5nCK), tRFC(min)+ 10ns)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE(min)+ 1nCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5nCK, 10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5nCK, 10ns)	-	
Power Down Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**

tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24ns)	-	
tCKE	CKE minimum pulse width	max(3nCK,5ns)	-	
tCPDED	Command pass disable delay	2	-	nCK
tPD	Power Down Entry to Exit Timing	tCKE(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	nCK
ODT Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**

ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK
tAONPD	Asynchronous RTT turn-on delay (Powe-Down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns
tAON	RTT-turn-on	-195	195	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	tCK(avg)
Write Leveling Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	nCK
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	-	nCK
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	140	-	ps
tWLH	Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	140	-	ps
tWLO	Write leveling output delay	0	7.5	ns
tWLOE	Write leveling output error	0	2	ns

10. PACKAGE DIMENSION

- (2GB, 1 Rank, 256Mx16 DDR3L base SODIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

11. RoHS Declaration

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宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Internet: https://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Products: All Innodisk EM FLASH, DRAM and EP products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及(EU) 2015/863 關於 RoHS 之規範要求。
Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。
Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

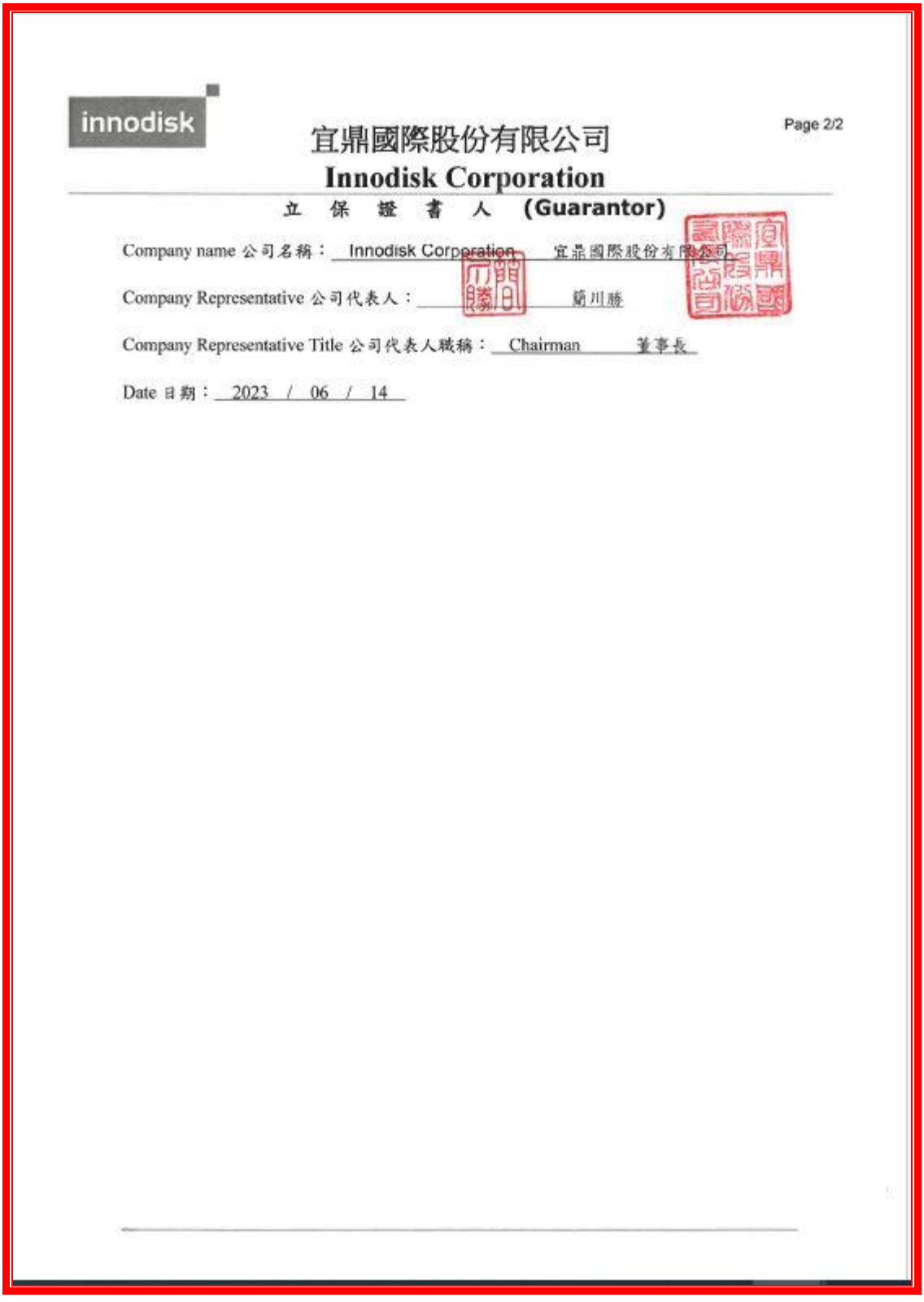
三、 本公司聲明我們的產品符合 RoHS 指令的附件中 7(a)、7(c)-I、6(c)允許豁免。
We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.

※ 7(a) Lead in high melting temperature type solders(i.e. lead-based alloys containing 85% by weight or more lead).

※ 7(c)-I Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.

※ 6(c) Copper alloy containing up to 4% lead by weight. (This exemption applies to products that use antennas)

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
鉛（Pb）	< 1000 ppm
汞（Hg）	< 1000 ppm
鎘（Cd）	< 100 ppm
六價鉻（Cr 6+）	< 1000 ppm
多溴聯苯（PBBs）	< 1000 ppm
多溴二苯醚（PBDEs）	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯（DEHP）	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯（BBP）	< 1000 ppm
鄰苯二甲酸二丁酯（DBP）	< 1000 ppm
鄰苯二甲酸二異丁酯（DIBP）	< 1000 ppm



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Page 2/2

宜鼎國際股份有限公司
Innodisk Corporation

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2023 / 06 / 14

12. Reach Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation
REACH Declaration

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: https://www.innodisk.com/

Innodisk Corporation pursues its social responsibility for global environmental preservation by committing to be compliant with REACH regulation (REGULATION (EC) No 1907/2006).
We hereby confirm that the product(s),

Scope: Flash Memory, DRAM Module and Embedded Peripherals Products.

■ The standard products of **not listed in** the ***Appendix2*** meet the requirements of REACH SVHC regulations(SVHCs < 0.1% in Article), as described in the candidate list table currently including 240 substances (release date: 23-JAN-2024) and shown on the ECHA website. https://echa.europa.eu/candidate-list-table

■ The standard products listed in the ***Appendix2*** contain(s) one or more hazardous substances or constituents exceeding 0.1 % by weight in article if not otherwise specified in candidate list table.
Where the threshold value is exceeded, the substances in question are to be declared in accompanying. (SVHCs > 0.1% in Article).

■ Comply with REACH Annex XVII.

Guarantor

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Yichuan Chen 陳怡全

Company Representative Title 公司代表人職稱：Quality Assurance Div. SR. Manager 品保處經理

Date 日期：2024 / 02 / 19

1

Revision Log

Rev	Date	Modification
0.1	26th August 2025	Preliminary Edition
1.0	26th August 2025	Official released.