RPS9HC

COM HPC® Client Size C
User's Manual

Copyright

This publication contains information that is protected by copyright. No part of it may be reproduced in any form or by any means or used to make any transformation/adaptation without the prior written permission from the copyright holders.

This publication is provided for informational purposes only. The manufacturer makes no representations or warranties with respect to the contents or use of this manual and specifically disclaims any express or implied warranties of merchantability or fitness for any particular purpose. The user will assume the entire risk of the use or the results of the use of this document. Further, the manufacturer reserves the right to revise this publication and make changes to its contents at any time, without obligation to notify any person or entity of such revisions or changes.

Changes after the publication's first release will be based on the product's revision. The website will always provide the most updated information.

© 2024. All Rights Reserved.

Trademarks

Product names or trademarks appearing in this manual are for identification purpose only and are the properties of the respective owners.

COM HPC® Specification Reference

PICMG® COM-HPC® Module Base Specification Revision 1.20

http://www.picmg.org/

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and the receiver.

- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

- Consult the dealer or an experienced radio TV technician for help.

Notice:

- The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

- Shielded interface cables must be used in order to comply with the emission limits.

Table of Contents

About this Manual

This manual can be downloaded from the website.

The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

Warranty

- Warranty does not cover damages or failures that occur from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.

- The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.

- Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.

- We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

- To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.

- Wear an antistatic wrist strap.

- Do all preparation work on a static-free surface.

- Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.

- Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

> **Important:**
> Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

- To avoid damage to the system, use the correct AC input voltage range.

- To reduce the risk of electric shock, unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

The accessories in the package may not come similar to the information listed below. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

- RPS9HC-R680E/Q670E/H610E Motherboard.

Optional Items

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

Before Using the System Board

Before using the system board, prepare basic system components.
If you are installing the system board in a new system, you will need at least the following internal components.

- Storage devices such as hard disk drive, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

Chapter 1 - Introduction

▶ Background

RPS9HC is a DFI standard product of COM HPC size-C module board and it will be developed based on Intel desktop platform Raptor lake-S/ SR.
This product will be designed with three different levels PCH called R680E, Q670E and H610E, main spec is listed below.

Function	RPS9HC-R680E	RPS9HC-Q670E	RPS9HC-H610E
ECC	V	X	X
vPro	V	V	X
Integrated 2.5Gb Ethernet with TSN support	V	X	X
RAID (PCIe/SATA)	V	V	X

▶ Specification

SYSTEM   Processor

Intel® Bartlett Lake-S Hybrid LGA 1700 Socket Processors
Intel® Core™ 7 251E (24 Cores, 36M Cache, up to 5.6 GHz); 65W
Intel® Core™ 7 251TE (24 Cores, 36M Cache, up to 5.4 GHz); 45W
Intel® Core™ 5 221E (14 Cores, 24M Cache, up to 5.2 GHz); 65W
Intel® Core™ 5 221TE (14 Cores, 24M Cache, up to 5.0 GHz); 45W
Intel® Core™ 5 211E (10 Cores, 20M Cache, up to 4.9 GHz); 65W
Intel® Core™ 5 211EF (10 Cores, 20M Cache, up to 4.9 GHz); 65W
Intel® Core™ 5 211TE (10 Cores, 20M Cache, up to 4.8 GHz); 45W
Intel® Core™ 3 201E (4 Cores, 12M Cache, up to 4.8 GHz); 60W
Intel® Core™ 3 201EF (4 Cores, 12M Cache, up to 4.8 GHz); 60W
Intel® Core™ 3 201TE (4 Cores, 12M Cache, up to 4.6 GHz); 45W

14th Gen Intel® Core™ Processors, LGA 1700 Socket Processors, TDP support up to 65W
Intel® Core™ I9-14900 (24 Cores, 36M Cache, up to 5.8 GHz); 65W
Intel® Core™ I9-14900T (24 Cores, 36M Cache, up to 5.5 GHz); 35W
Intel® Core™ I7-14700 (20 Cores, 33M Cache, up to 5.4 GHz); 65W
Intel® Core™ I7-14700T (20 Cores, 33M Cache, up to 5.2 GHz); 35W
Intel® Core™ I5-14500 (14 Cores, 24M Cache, up to 5.0 GHz); 65W
Intel® Core™ I5-14500T (14 Cores, 24M Cache, up to 4.8 GHz); 35W
Intel® Core™ I5-14400 (10 Cores, 20M Cache, up to 4.7 GHz); 65W
Intel® Core™ I5-14400T (10 Cores, 20M Cache, up to 4.5 GHz); 35W
Intel® Core™ I3-14100 (4 Cores, 12M Cache, up to 4.7 GHz); 60W
Intel® Core™ I3-14100T (4 Cores, 12M Cache, up to 4.4 GHz); 35W

		13th Gen Intel® Core™ Processors, LGA 1700 Socket Processors, TDP support up to 65W
		Intel® Core™ I9-13900E (24 Cores, 36M Cache, up to 5.2 GHz); 65W
		Intel® Core™ I9-13900TE (24 Cores, 36M Cache, up to 5.0 GHz); 35W
		Intel® Core™ I7-13700E (16 Cores, 30M Cache, up to 5.1 GHz); 65W
		Intel® Core™ I7-13700TE (16 Cores, 30M Cache, up to 4.8 GHz); 35W
		Intel® Core™ I7-13700T (16 Cores, 30M Cache, up to 4.9 GHz); 35W
		Intel® Core™ I5-13500E (14 Cores, 24M Cache, up to 4.6 GHz); 65W
		Intel® Core™ I5-13500TE (14 Cores, 24M Cache, up to 4.5 GHz); 35W
		Intel® Core™ I5-13500T (14 Cores, 24M Cache, up to 4.6 GHz); 35W
		Intel® Core™ I5-13400E (10 Cores, 20M Cache, up to 4.6 GHz); 65W
		Intel® Core™ I3-13100E (4 Cores, 12M Cache, up to 3.3 GHz); 60W
		Intel® Core™ I3-13100TE (4 Cores, 12M Cache, up to 4.1 GHz); 35W
		Intel® Core™ I3-13100T (4 Cores, 12M Cache, up to 4.2 GHz); 35W
SYSTEM	Chipset	Intel® R680E/Q670E/H610E Chipset
	Memory	4pcs DDR5 SO-DIMM up to 192GB Dual Channel DDR5 ECC support by R680 with i7 and i5
	BIOS	AMI SPI 256Mbit
GRAPHICS	Controller	Intel® HD Gen 9 Graphics
	Feature	OpenGL 4.5, DirectX 12, OpenCL 2.1 HW Decode: AVC/H.264, MPEG2, VC1/WMV9, JPEG/MJPEG, HEVC/H265, VP8, VP9 HW Encode: MPEG2, AVC/H264, JPEG, HEVC/H265, VP8, VP9
	Display	3 x DDI (HDMI/DP++) support to 8K 1 x eDP support to 5K
	Multiple Displays	eDP + 3 DDI
EXPANSION	Interface	1 x PCIe x16 (Gen5) 4 x PCIe x4 (Gen4) 2 x PCIe x4 (Gen3) 2 x PCIe x1 (Gen3) 1 x eSPI 1 x I2C 1 x SMBus 2 x UART (TX/RX/RTS/CTS)
AUDIO	Audio Codec	HD Audio
ETHERNET	Phy	2 x Intel® I226 series (10/100/1000Mbps/2.5G)
I/O	USB	4 x USB 3.2 Gen2 8 x USB 2.0
	SATA	2 x SATA 3.0 (up to 6Gb/s)
	GPIO	12 bit in/out
WATCHDOG TIMER	Output & Interval	System Reset, Programmable via Software from 1 to 255 Seconds

SECURITY	TPM	TPM2.0 (Available Upon Request)
Power	Type	12V, 5VSB, VCC_RTC (ATX mode) 12V, VCC_RTC (AT mode)
	Consumption	TBD
OS SUPPORT	Microsoft	Windows 10 IoT Enterprise 64-bit Windows 11
	Linux	Ubuntu 20.04
ENVIRONMENT	Temperature	Operating: 0 to 60°C Storage: -40 to 85°C
	Humidity	Operating: 5 to 90% RH Storage: 5 to 90% RH
	MTBF	TBD
MECHANICAL	Dimensions	COM HPC® Client Size C 6.30 x 4.72 (160mm x 120mm)
	Compliance	PICMG COM HPC® R1.15, Client Size C
STANDARDS AND CERTIFICATIONS	Certification	CE, FCC, RoHS

▶ Block Diagram
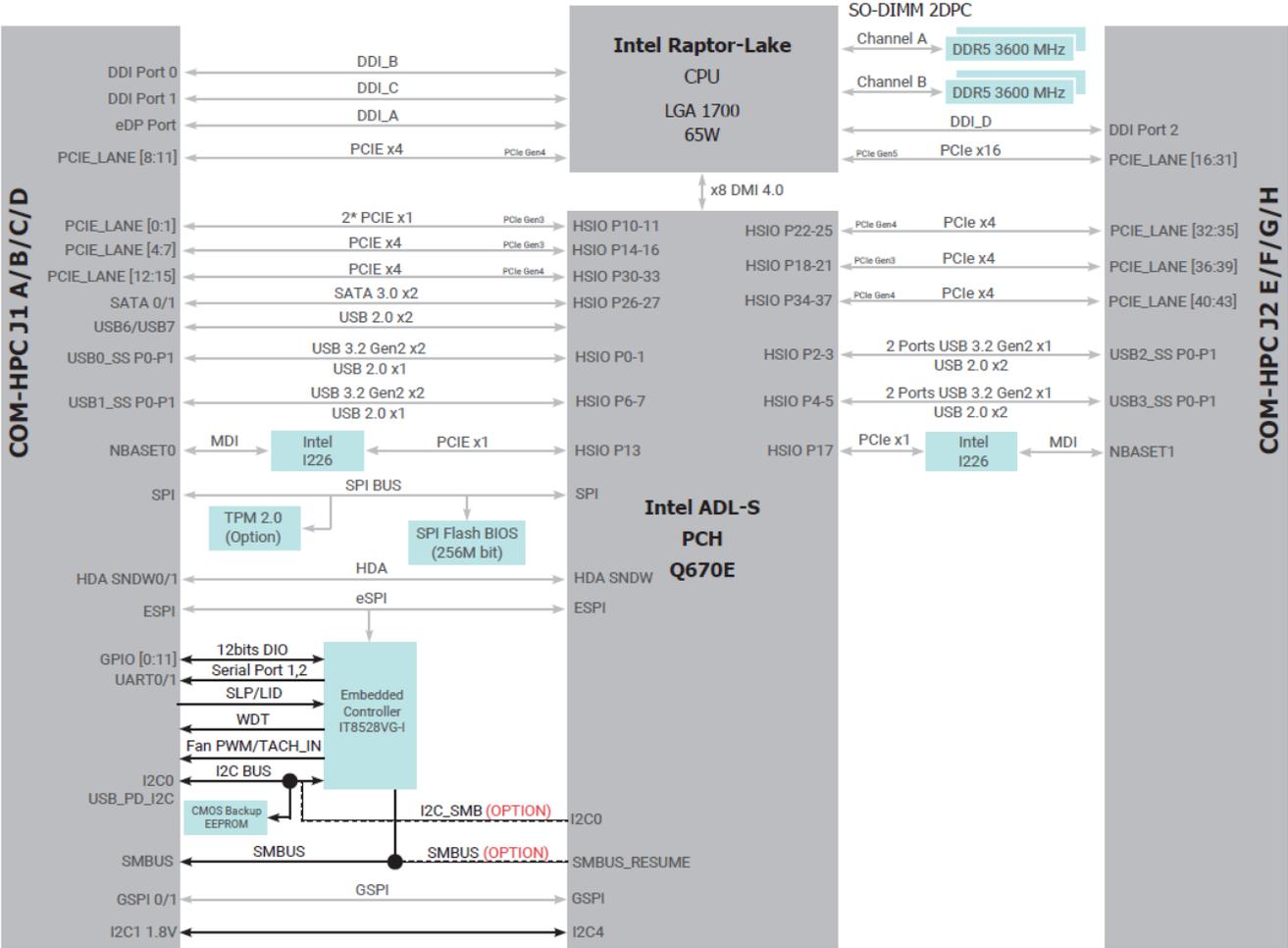
Chapter 2 - Concept

▶ **COM HPC® Module Standards**

The figure below shows the dimensions of the different types of COM HPC® modules.
RSP9HC is a COM HPC® Client Size C. The dimension is 160mm x 120mm.
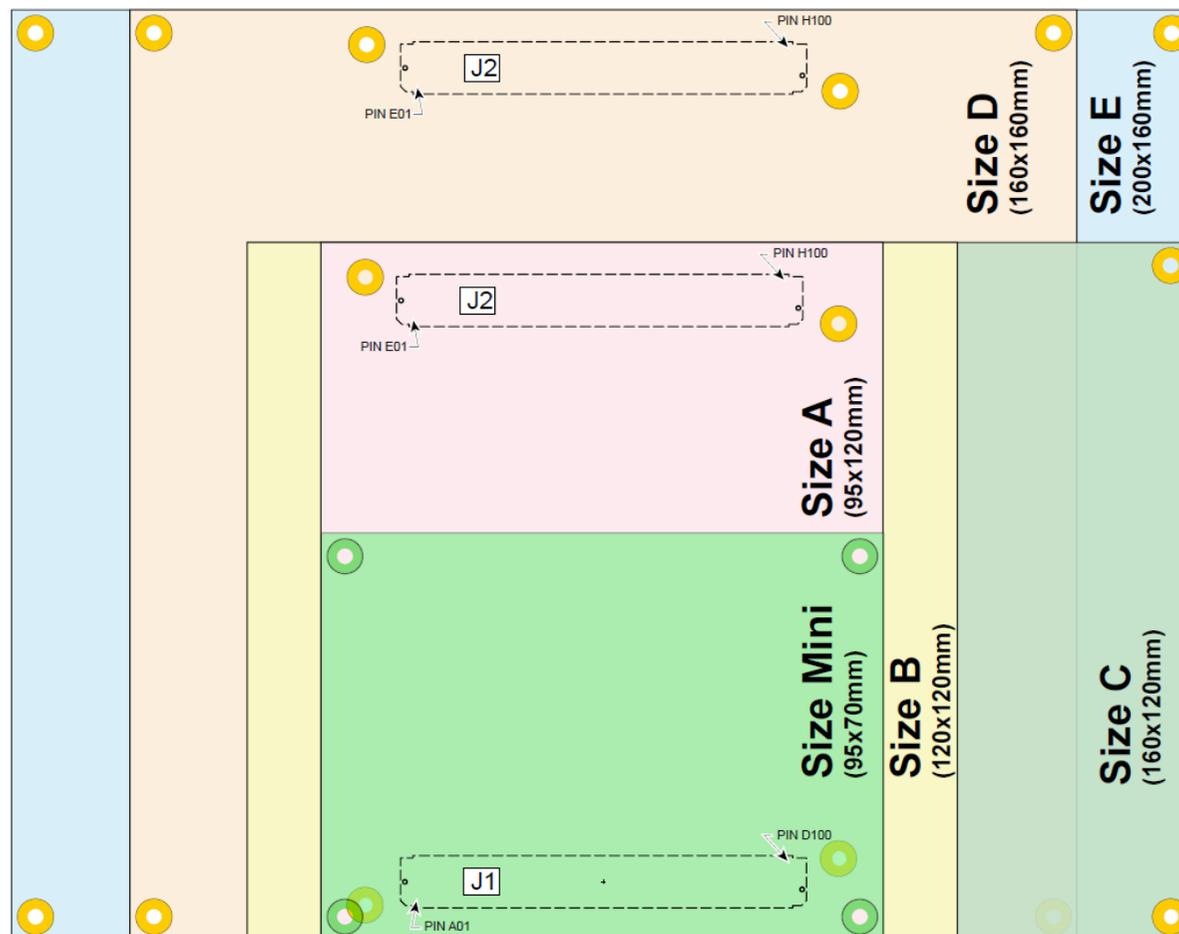
Chapter 3 - Hardware Installation

▶ Board Layout
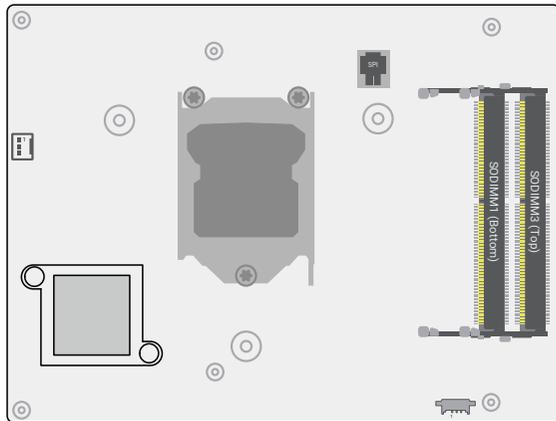
TOP VIEW
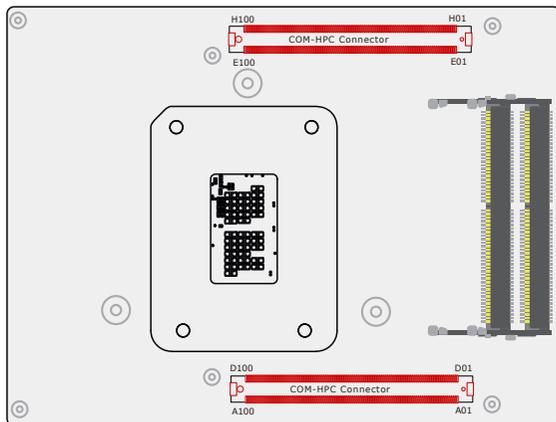
BOTTOM VIEW

▶ Pin Assignment

CPU Fan (J1)
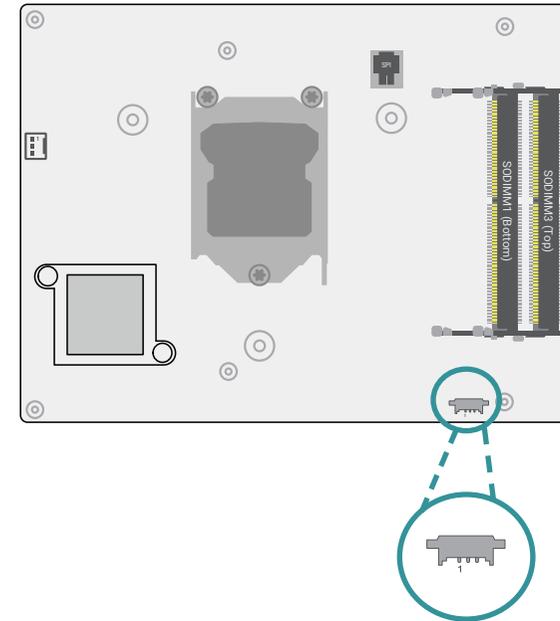
Pin	Assignment
1	FAN_TACH
2	FAN_OUT
3	GND

DEBUG UART (J2)
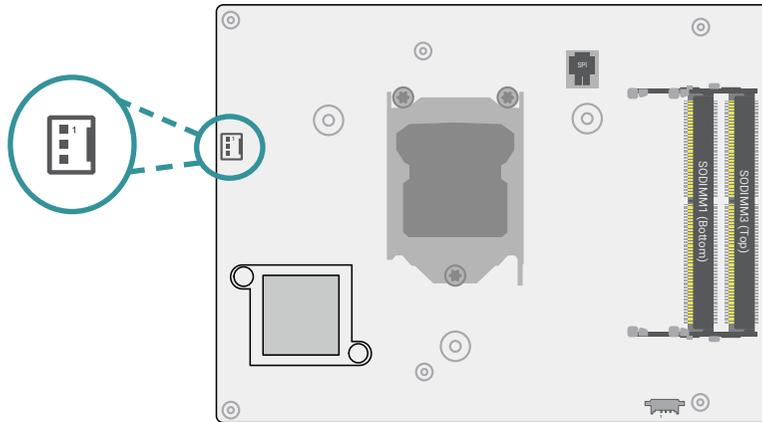
Pin	Assignment
1	GND
2	DEBUG_UART_RX
3	DEBUG_UART_TX

▶ Connector

The COM HPC® connector is used to interface the RPS9HC COM HPC® board to a carrier board. Connect the COM HPC® connector (located on the solder side of the board) to the COM HPC® connector on the carrier board.
Refer to the following pages for the pin functions of the connector.

COM-HPC Connector

COM-HPC Connector
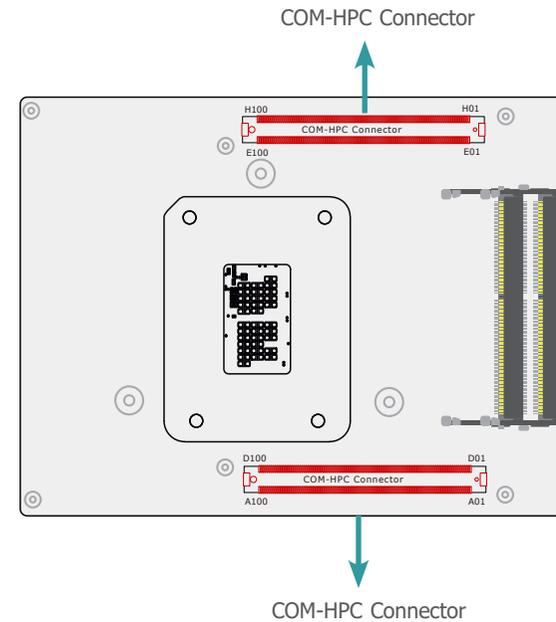
▶ **Mapping RPS9HC Connector with COM836 Carrier Board**

A Carrier Board

	R680E
	Support all

	Q670E
	PCIE4 SLOT not supported
	ETCN2 USB-A only support Gen1

	H610E
	PCIE2,PCIE3,PCIE4,PCIE6 SLOT not supported
	UBCN2 & ETCN2 USB-A not supported
	M2CN4 M2 M-Key not supported

H610E limitation:
1. Display Max 3
2. Only 1DPC for memory
3. DMI only x4
4. PCIe only Gen 3
5. USB speed refer HSIO table
6. Processor PCIex4 not support
7. no RAID support
8. vPro No support (LAN1/2 used i226V)
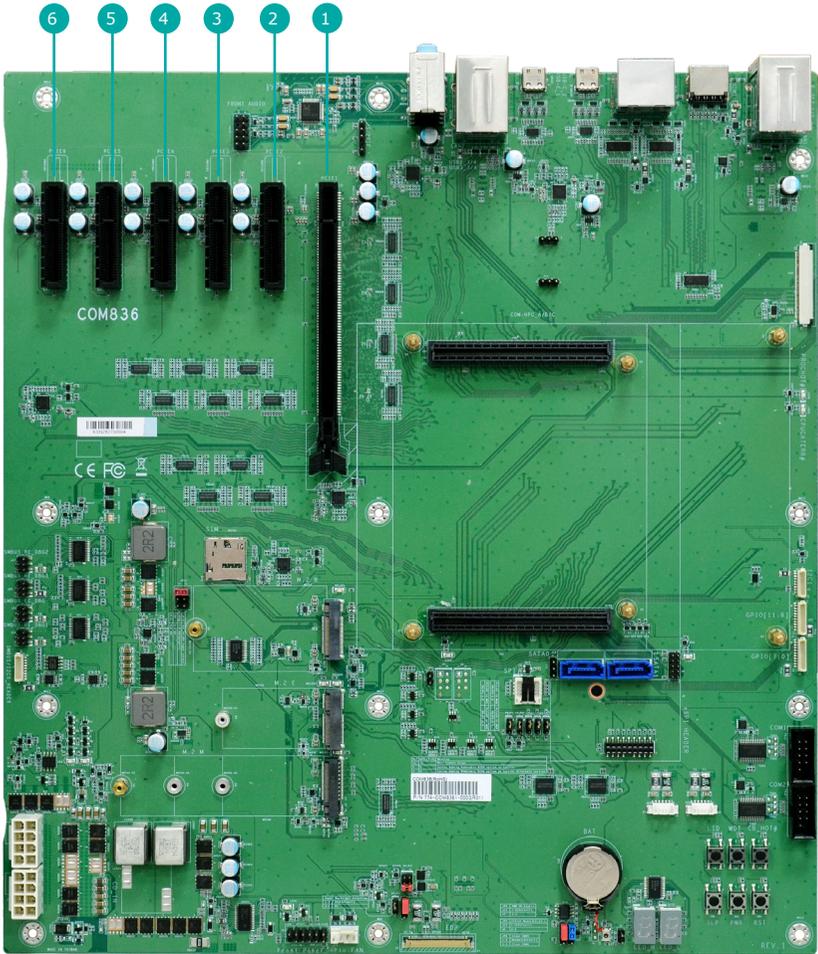
1	PCIE1	3	PCIE3	5	PCIE5
2	PCIE2	4	PCIE4	6	PCIE6

▶ **RPS9HC Module - Required and Optional Features**

Feature	RPS9HC Module/ COM-HPC SPEC Max	COM-HPC SPEC Notes
NBASE-T	2/2	All CPU Modules shall have at least one l000BASE-T capable port
Ethernet KR / KX	0/2	
SATA	2/2	
PCIe 0:47	44/48	
PCIe 48:63	N/A	All PCIe Reference Clocks required.
PCIe BMC	0/1	
PCIe Target on Module Support	0/2	Thisis primarily for Modules supporting FPGAs or GPUs
USB 2.0 Ports 0:7	8/8	USB 3.2 and USB4, if implemented, make use of USB 2.0 Ports 0:3
USB 3.2 Gen 1 or Gen 2	2/2	One SuperSpeed TX pair and one RX pair per port for USB 3.2 Gen 1 and 2
USB 3.2 Gen 2x2	2/4	Two SuperSpeed TX pairs and two RX pairs per port for USB 3.2 Gen 2x2
USB 4.0 Support	0/4	USB4 ports make use of USB 3.2 Gen 2x2 ports.
eSPI	1/1	X86 CPU Modules should implement the eSPI interface
Boot SPI Interface	1/1	
BIOS Select Options	1/1	
Digital Display Interfaces (DDI)	3/3	Additional display outputs may be available on the USB4 interfaces
eDP	1/1	
MIPI Display Serial Interface (DSI)	0/1	
MIPI Camera Serial Interface (CSI)	0/2	
Soundwire Audio	0/1	
12S Audio/ 2nd Soundwire /HDA	1/1	
Asynchronous Serial Ports	2/2	
12CPorts	2/2	
IPMB	0/1	Recommended but not required for Server Modules
General Purpose SPI Port	1/1	At least two GP_SPI chip selects shall be supported

Feature	RPS9HC Module/ COM-HPC SPEC Max	COM-HPC SPEC Notes
Power and System Management	1/1	
Rapid Shutdown	0/1	
Thermal Protection	1/1	
System Management Bus	1/1	
GPIO	12/ 12	
FuSa set of signals	0/1	
Module Type Pin Support	1/1	
Watchdog Timer	1/1	
Secondary Fan Tach and PWM	1/1	
VCC pins	28/28	
VCC_5V_SBY Support	2/2	
VCC_RTC	1/1	
Connector J1	1/1	
Connector J2	1/1	Vendors may omit J2 on Client Modules
GND	All	All available GND pins shall be used

▶ COM HPC® Connector Signal Description

PCI Express Signals - COM-HPC Group 0 High/Low

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

PCI Express Lanes	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended
PCIe00_TX-	D61	O PCIe	AC coupled on Module	PCIE_TX1N	RPS9HC BOM only implement PCIe00 and PCIe01, up to PCIe Gen 3 speed. PCIE02 & PCIe 03 default BOM no connect (If need to use, need custom the BIOS and BOM setting)
PCIe00_TX+	D62			PCIE_TX1P	
PCIe01_TX-	D64	O PCIe	AC coupled on Module	PCIE_TX2N	
PCIe01_TX+	D65			PCIE_TX2P	
PCIe02_TX-	D67	O PCIe	AC coupled on Module	BTB_PCIE_2_TXN	
PCIe02_TX+	D68			BTB_PCIE_2_TXP	
PCIe03_TX-	D70	O PCIe	AC coupled on Module	BTB_PCIE_3_TXN	
PCIe03_TX+	D71			BTB_PCIE_3_TXP	
PCIe04_TX-	D73	O PCIe	AC coupled on Module	PCIE_TX5N	RPS9HC default BIOS use PCIe x4, up to PCIe Gen 3 speed.
PCIe04_TX+	D74			PCIE_TX5P	
PCIe05_TX-	D76	O PCIe	AC coupled on Module	PCIE_TX6N	
PCIe05_TX+	D77			PCIE_TX6P	
PCIe06_TX-	D79	O PCIe	AC coupled on Module	PCIE_TX7N	
PCIe06_TX+	D80			PCIE_TX7P	
PCIe07_TX-	D82	O PCIe	AC coupled on Module	PCIE_TX8N	
PCIe07_TX+	D83			PCIE_TX8P	
PCIe08_TX-	A62	O PCIe	AC coupled on Module	EXP_A_TX_16_DN	RPS9HC CPU PCIe x4, default suggest to use NVME device or Hi BW Link x4 (this port only support one PCIe device)
PCIe08_TX+	A63			EXP_A_TX_16_DP	
PCIe09_TX-	A65	O PCIe	AC coupled on Module	EXP_A_TX_17_DN	
PCIe09_TX+	A66			EXP_A_TX_17_DP	
PCIe10_TX-	A68	O PCIe	AC coupled on Module	EXP_A_TX_18_DN	
PCIe10_TX+	A69			EXP_A_TX_18_DP	
PCIe11_TX-	A71	O PCIe	AC coupled on Module	EXP_A_TX_19_DN	
PCIe11_TX+	A72			EXP_A_TX_19_DP	
PCIe12_TX-	A74	O PCIe	AC coupled on Module	PCIE_TX21N	RPS9HC default BIOS use PCIe x4, up to PCIe Gen 4 speed. RPS9HC H610E SKU not support.
PCIe12_TX+	A75			PCIE_TX21P	
PCIe13_TX-	A77	O PCIe	AC coupled on Module	PCIE_TX22N	
PCIe13_TX+	A78			PCIE_TX22P	
PCIe14_TX-	A80	O PCIe	AC coupled on Module	PCIE_TX23N	
PCIe14_TX+	A81			PCIE_TX23P	
PCIe15_TX-	A83	O PCIe	AC coupled on Module	PCIE_TX24N	
PCIe15_TX+	A84			PCIE_TX24P	

Signals Description

PCI Express Differential Transmit Pairs 0 through 15

PCIe Group 0 Low and Group 0 High

If a Client Module has different classes of PCIe links (i.e. a mix of Gen 2 and Gen 3 or Gen 3 and Gen 4 or similar), then up to 8 of the higher bandwidth PCIe lanes should be mapped PCIe Group 0 High.

GROUP 0 High	15	NVME1 or GP Hi BW Link x4	x2	x2	
	14				
	13		x2	x2	
	12				
	11	NVME0 or GP Hi BW Link x4	NVME0 or GP Hi BW Link x4	x2	
	10				
	09			x2	x2
	08				
GROUP 0 Low	07	x1	x2	x4	
	06	x1			
	05	x1	x2		
	04	x1			x1
	03	x1	x1	x1	
	02	x1	x1	x1	
	01	x1	x1	x1	
	00	x1	x1	x1	X1

PCI Express Lanes	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended
PCIe00_RX-	C62	I PCIe	AC coupled off Module	PCIE_RX1N	
PCIe00_RX+	C63			PCIE_RX1P	
PCIe01_RX-	C65	I PCIe	AC coupled off Module	PCIE_RX2N	RPS9HC BOM only implement PCIe00 and PCIe01, up to PCIe Gen 3 speed. PCIE02 & PCIe 03 default BOM no connect (If need to use, need custom the BIOS and BOM setting)
PCIe01_RX+	C66			PCIE_RX2P	
PCIe02_RX-	C68	I PCIe	AC coupled off Module	BTB_PCIE_2_RXN	
PCIe02_RX+	C69			BTB_PCIE_2_RXP	
PCIe03_RX-	C71	I PCIe	AC coupled off Module	BTB_PCIE_3_RXN	
PCIe03_RX+	C72			BTB_PCIE_3_RXP	
PCIe04_RX-	C74	I PCIe	AC coupled off Module	PCIE_RX5N	
PCIe04_RX+	C75			PCIE_RX5P	
PCIe05_RX-	C77	I PCIe	AC coupled off Module	PCIE_RX6N	RPS9HC default BIOS use PCIe x4, up to PCIe Gen 3 speed.
PCIe05_RX+	C78			PCIE_RX6P	
PCIe06_RX-	C80	I PCIe	AC coupled off Module	PCIE_RX7N	
PCIe06_RX+	C81			PCIE_RX7P	
PCIe07_RX-	C83	I PCIe	AC coupled off Module	PCIE_RX8N	
PCIe07_RX+	C84			PCIE_RX8P	
PCIe08_RX-	B61	I PCIe	AC coupled off Module	EXP_A_RX_16_DN	
PCIe08_RX+	B62			EXP_A_RX_16_DP	
PCIe09_RX-	B64	I PCIe	AC coupled off Module	EXP_A_RX_17_DN	RPS9HC CPU PCIe x4, default suggest to use NVME device or Hi BW Link x4 (this port only support one PCIe device)
PCIe09_RX+	B65			EXP_A_RX_17_DP	
PCIe10_RX-	B67	I PCIe	AC coupled off Module	EXP_A_RX_18_DN	
PCIe10_RX+	B68			EXP_A_RX_18_DP	
PCIe11_RX-	B70	I PCIe	AC coupled off Module	EXP_A_RX_19_DN	
PCIe11_RX+	B71			EXP_A_RX_19_DP	
PCIe12_RX-	B73	I PCIe	AC coupled off Module	PCIE_RX21N	
PCIe12_RX+	B74			PCIE_RX21P	
PCIe13_RX-	B76	I PCIe	AC coupled off Module	PCIE_RX22N	RPS9HC default BIOS use PCIe x4, up to PCIe Gen 4 speed. RPS9HC H610E SKU not support.
PCIe13_RX+	B77			PCIE_RX22P	
PCIe14_RX-	B79	I PCIe	AC coupled off Module	PCIE_RX23N	
PCIe14_RX+	B80			PCIE_RX23P	
PCIe15_RX-	B82	I PCIe	AC coupled off Module	PCIE_RX24N	
PCIe15_RX+	B83			PCIE_RX24P	

Signals Description

PCI Express Differential Receive Pairs 0 through 15

PCIe Group 0 Low and Group 0 High

GROUP 0 High	15	NVME1 or GP Hi BW Link x4	x2	x2	
	14				
	13		x2	x2	
	12				
	11	NVME0 or GP Hi BW Link x4	NVME0 or GP Hi BW Link x4	x2	
	10				
	09			x2	x2
	08				
GROUP 0 Low	07	x1	x2	x4	
	06	x1			
	05	x1	x2		
	04	x1			x1
	03	x1	x1	x1	
	02	x1	x1	x1	
	01	x1	x1	x1	
	00	x1	x1	x1	X1

PCI Express Signals - COM-HPC Group 1

PCI Express Lanes	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
PCIe16_TX-	E45	O PCIe	AC coupled on Module	EXP_A_TX_0_DN		PCI Express Differential Transmit Pairs 16 through 31
PCIe16_TX+	E46			EXP_A_TX_0_DP		
PCIe17_TX-	E48	O PCIe	AC coupled on Module	EXP_A_TX_1_DN		PCIe Group 1
PCIe17_TX+	E49			EXP_A_TX_1_DP		
PCIe18_TX-	E51	O PCIe	AC coupled on Module	EXP_A_TX_2_DN		If a PEG port is implemented on a Module that includes J2, the PEG port shall be implemented on PCIe TX and RX lanes 16:31 (for x16) or 16:23 (for x8). A second x8 PEG port may be mapped to PCIe lanes 24:31.
PCIe18_TX+	E52			EXP_A_TX_2_DP		
PCIe19_TX-	E54	O PCIe	AC coupled on Module	EXP_A_TX_3_DN		If a Module has different classes of PCIe links (i.e. a mix of Gen 2 and Gen 3 or Gen 3 and Gen 4 or similar), then up to 16 of the higher bandwidth PCIe lanes should bemapped to this COM-HPC PCIe group.
PCIe19_TX+	E55			EXP_A_TX_3_DP		
PCIe20_TX-	E57	O PCIe	AC coupled on Module	EXP_A_TX_4_DN		
PCIe20_TX+	E58			EXP_A_TX_4_DP		
PCIe21_TX-	E60	O PCIe	AC coupled on Module	EXP_A_TX_5_DN		
PCIe21_TX+	E61			EXP_A_TX_5_DP		
PCIe22_TX-	E63	O PCIe	AC coupled on Module	EXP_A_TX_6_DN		
PCIe22_TX+	E64			EXP_A_TX_6_DP		
PCIe23_TX-	E66	O PCIe	AC coupled on Module	EXP_A_TX_7_DN	RPS9HC default BIOS setting: PCIe x16 for PEG & SSD application If need implement 2 PCIe device application on group 1, need set the BIOS and BOM (CPU CFG5). Also the carrier need implement the 2 clock source for these two PCIe device. (COM-HPC each group set one clock source from module)	
PCIe23_TX+	E67			EXP_A_TX_7_DP		
PCIe24_TX-	H44	O PCIe	AC coupled on Module	EXP_A_TX_8_DN		
PCIe24_TX+	H45			EXP_A_TX_8_DP		
PCIe25_TX-	H47	O PCIe	AC coupled on Module	EXP_A_TX_9_DN		
PCIe25_TX+	H48			EXP_A_TX_9_DP	Lane reversal application support by COM-HPC pin G19 (PEG_LANE_REV#) for layout routing.	
PCIe26_TX-	H50	O PCIe	AC coupled on Module	EXP_A_TX_10_DN		
PCIe26_TX+	H51			EXP_A_TX_10_DP		
PCIe27_TX-	H53	O PCIe	AC coupled on Module	EXP_A_TX_11_DN		
PCIe27_TX+	H54			EXP_A_TX_11_DP		
PCIe28_TX-	H56	O PCIe	AC coupled on Module	EXP_A_TX_12_DN		
PCIe28_TX+	H57			EXP_A_TX_12_DP		
PCIe29_TX-	H59	O PCIe	AC coupled on Module	EXP_A_TX_13_DN		
PCIe29_TX+	H60			EXP_A_TX_13_DP		
PCIe30_TX-	H62	O PCIe	AC coupled on Module	EXP_A_TX_14_DN		
PCIe30_TX+	H63			EXP_A_TX_14_DP		
PCIe31_TX-	H65	O PCIe	AC coupled on Module	EXP_A_TX_15_DN		
PCIe31_TX+	H66			EXP_A_TX_15_DP		

	PCIe Lane	Should (Preferred)	May (Option 1)	May (Option 2)	Shall (Min Req)
GROUP 1	31	PEG or GP Hi BW Link x16	2nd PEG or GP Hi BW Link x8 or 2x4	x4	
	30				
	29				
	28				
	27			x4	
	26				
	25				
	24				
	23		PEG or GP Hi BW Link x8	x4	
	22				
	21				
	20				
	19				
	18			x4	
	17				
	16				

PCI Express Lanes	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
PCIe16_RX-	F44	I PCIe	AC coupled off Module	EXP_A_RX_0_DN		PCI Express Differential Receive Pairs 16 through 31
PCIe16_RX+	F45			EXP_A_RX_0_DP		
PCIe17_RX-	F47	I PCIe	AC coupled off Module	EXP_A_RX_1_DN		PCIe Group1
PCIe17_RX+	F48			EXP_A_RX_1_DP		
PCIe18_RX-	F50	I PCIe	AC coupled off Module	EXP_A_RX_2_DN		
PCIe18_RX+	F51			EXP_A_RX_2_DP		
PCIe19_RX-	F53	I PCIe	AC coupled off Module	EXP_A_RX_3_DN		
PCIe19_RX+	F54			EXP_A_RX_3_DP		
PCIe20_RX-	F56	I PCIe	AC coupled off Module	EXP_A_RX_4_DN		
PCIe20_RX+	F57			EXP_A_RX_4_DP		
PCIe21_RX-	F59	I PCIe	AC coupled off Module	EXP_A_RX_5_DN		
PCIe21_RX+	F60			EXP_A_RX_5_DP		
PCIe22_RX-	F62	I PCIe	AC coupled off Module	EXP_A_RX_6_DN	RPS9HC default BIOS setting: PCIe x16 for PEG & SSD application If need implement 2 PCIe device application on group 1, need set the BIOS and BOM (CPU CFG5). Also the carrier need implement the 2 clock source for these two PCIe device. (COM-HPC each group set one clock source from module) Lane reversal application support by COM-HPC pin G19 (PEG_LANE_REV#) for layout routing.	
PCIe22_RX+	F63			EXP_A_RX_6_DP		
PCIe23_RX-	F65	I PCIe	AC coupled off Module	EXP_A_RX_7_DN		
PCIe23_RX+	F66			EXP_A_RX_7_DP		
PCIe24_RX-	G45	I PCIe	AC coupled off Module	EXP_A_RX_8_DN		
PCIe24_RX+	G46			EXP_A_RX_8_DP		
PCIe25_RX-	G48	I PCIe	AC coupled off Module	EXP_A_RX_9_DN		
PCIe25_RX+	G49			EXP_A_RX_9_DP		
PCIe26_RX-	G51	I PCIe	AC coupled off Module	EXP_A_RX_10_DN		
PCIe26_RX+	G52			EXP_A_RX_10_DP		
PCIe27_RX-	G54	I PCIe	AC coupled off Module	EXP_A_RX_11_DN		
PCIe27_RX+	G55			EXP_A_RX_11_DP		
PCIe28_RX-	G57	I PCIe	AC coupled off Module	EXP_A_RX_12_DN		
PCIe28_RX+	G58			EXP_A_RX_12_DP		
PCIe29_RX-	G60	I PCIe	AC coupled off Module	EXP_A_RX_13_DN		
PCIe29_RX+	G61			EXP_A_RX_13_DP		
PCIe30_RX-	G63	I PCIe	AC coupled off Module	EXP_A_RX_14_DN		
PCIe30_RX+	G64			EXP_A_RX_14_DP		
PCIe31_RX-	G66	I PCIe	AC coupled off Module	EXP_A_RX_15_DN		
PCIe31_RX+	G67			EXP_A_RX_15_DP		

	PCIe Lane	Should (Preferred)	May (Option 1)	May (Option 2)	Shall (Min Req)
GROUP 1	31	PEG or GP Hi BW Link x16	2nd PEG or GP Hi BW Link x8 or 2x4	x4	
	30				
	29				
	28				
	27			x4	
	26				
	25				
	24				
	23		PEG or GP Hi BW Link x8	x4	
	22				
	21				
	20				
	19			x4	
	18				
	17				
	16				

PCI Express Signals - COM-HPC Group 2

PCI Express Lanes	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
PCIe32_TX-	E21	O PCIe	AC coupled on Module	PCIE_TX13N		PCI Express Differential Transmit Pairs 32 through 47
PCIe32_TX+	E22			PCIE_TX13P		PCIe Group 2
PCIe33_TX-	E24	O PCIe	AC coupled on Module	PCIE_TX14N	RPS9HC default BIOS use PCIe x4, up to PCIe Gen 4 speed.	
PCIe33_TX+	E25			PCIE_TX14P		
PCIe34_TX-	E27	O PCIe	AC coupled on Module	PCIE_TX15N	RPS9HC H610E SKU not support.	
PCIe34_TX+	E28			PCIE_TX15P		
PCIe35_TX-	E30	O PCIe	AC coupled on Module	PCIE_TX16N		
PCIe35_TX+	E31			PCIE_TX16P		
PCIe36_TX-	E33	O PCIe	AC coupled on Module	PCIE_TX9N		
PCIe36_TX+	E34			PCIE_TX9P		
PCIe37_TX-	E36	O PCIe	AC coupled on Module	PCIE_TX10N	RPS9HC default BIOS use PCIe x4, up to PCIe Gen 4 speed.	
PCIe37_TX+	E37			PCIE_TX10P		
PCIe38_TX-	E39	O PCIe	AC coupled on Module	PCIE_TX11N	RPS9HC Q670E & H610E SKU not support.	
PCIe38_TX+	E40			PCIE_TX11P		
PCIe39_TX-	E42	O PCIe	AC coupled on Module	PCIE_TX12N		
PCIe39_TX+	E43			PCIE_TX12P		
PCIe40_TX-	H20	O PCIe	AC coupled on Module	PCIE_TX25N		
PCIe40_TX+	H21			PCIE_TX25P		
PCIe41_TX-	H23	O PCIe	AC coupled on Module	PCIE_TX26N	RPS9HC default BIOS use PCIe x4, up to PCIe Gen 4 speed.	
PCIe41_TX+	H24			PCIE_TX26P		
PCIe42_TX-	H26	O PCIe	AC coupled on Module	PCIE_TX27N		
PCIe42_TX+	H27			PCIE_TX27P	RPS9HC H610E SKU not support.	
PCIe43_TX-	H29	O PCIe	AC coupled on Module	PCIE_TX28N		
PCIe43_TX+	H30			PCIE_TX28P		
PCIe44_TX-	H32	O PCIe	AC coupled on Module	No Connect		
PCIe44_TX+	H33			No Connect		
PCIe45_TX-	H35	O PCIe	AC coupled on Module	No Connect		
PCIe45_TX+	H36			No Connect		
PCIe46_TX-	H38	O PCIe	AC coupled on Module	No Connect		
PCIe46_TX+	H39			No Connect		
PCIe47_TX-	H41	O PCIe	AC coupled on Module	No Connect		
PCIe47_TX+	H42			No Connect		

GROUP 2

47	x4	X8 or 2x4	x16
46			
45			
44			
43	x4		
42			
41			
40			
39	x4	x8	
38			
37			
36			
35	x4		
34			
33			
32			

PCI Express Lanes	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
PCIe32_RX-	F20	I PCIe	AC coupled off Module	PCIE_RX13N		PCI Express Differential Receive Pairs 32 through 47
PCIe32_RX+	F21			PCIE_RX13P		
PCIe33_RX-	F23	I PCIe	AC coupled off Module	PCIE_RX14N		PCIe Group 2
PCIe33_RX+	F24			PCIE_RX14P	RPS9HC default BIOS use PCIe x4, up to PCIe Gen 4 speed.	
PCIe34_RX-	F26	I PCIe	AC coupled off Module	PCIE_RX15N		
PCIe34_RX+	F27			PCIE_RX15P	RPS9HC H610E SKU not support.	
PCIe35_RX-	F29	I PCIe	AC coupled off Module	PCIE_RX16N		
PCIe35_RX+	F30			PCIE_RX16P		
PCIe36_RX-	F32	I PCIe	AC coupled off Module	PCIE_RX9N		
PCIe36_RX+	F33			PCIE_RX9P		
PCIe37_RX-	F35	I PCIe	AC coupled off Module	PCIE_RX10N	RPS9HC default BIOS use PCIe x4, up to PCIe Gen 4 speed.	
PCIe37_RX+	F36			PCIE_RX10P		
PCIe38_RX-	F38	I PCIe	AC coupled off Module	PCIE_RX11N	RPS9HC Q670E & H610E SKU not support.	
PCIe38_RX+	F39			PCIE_RX11P		
PCIe39_RX-	F41	I PCIe	AC coupled off Module	PCIE_RX12N		
PCIe39_RX+	F42			PCIE_RX12P		
PCIe40_RX-	G21	I PCIe	AC coupled off Module	PCIE_RX25N		
PCIe40_RX+	G22			PCIE_RX25P		
PCIe41_RX-	G24	I PCIe	AC coupled off Module	PCIE_RX26N		
PCIe41_RX+	G25			PCIE_RX26P	RPS9HC default BIOS use PCIe x4, up to PCIe Gen 4 speed.	
PCIe42_RX-	G27	I PCIe	AC coupled off Module	PCIE_RX27N		
PCIe42_RX+	G28			PCIE_RX27P	RPS9HC H610E SKU not support.	
PCIe43_RX-	G30	I PCIe	AC coupled off Module	PCIE_RX28N		
PCIe43_RX+	G31			PCIE_RX28P		
PCIe44_RX-	G33	I PCIe	AC coupled off Module	No Connect		
PCIe44_RX+	G34			No Connect		
PCIe45_RX-	G36	I PCIe	AC coupled off Module	No Connect		
PCIe45_RX+	G37			No Connect		
PCIe46_RX-	G39	I PCIe	AC coupled off Module	No Connect		
PCIe46_RX+	G40			No Connect		
PCIe47_RX-	G42	I PCIe	AC coupled off Module	No Connect		
PCIe47_RX+	G43			No Connect		

PCI Express Lanes	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
PCIe_BMC_TX-	A59	O PCIe	AC coupled on Module	No Connect		PCI Express Differential Transmit Pair for Carrier BMC (Board Management Controller); part of PCIe Group 0
PCIe_BMC_TX+	A60			No Connect		
PCIe_BMC_RX-	B58	I PCIe	AC coupled off Module	No Connect		PCI Express Differential Receive Pairs for Carrier BMC (Board Management Controller); part of PCIe Group 0
PCIe_BMC_RX+	B59			No Connect		

PCI Express Clock - PCIe Clock

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

> **Important:**
> Not support PCI Express Additional Signals to Support Module Based PCIe Targets.

PCI Express Lanes	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
PCIe_REFCLK0_LO-	C59	O LV_DIFF	PCIE Clock	CK_PE_100M_G0_LO_DN	According Carrier board PCIe device routing, may need clock buffer design for multi device application.	Reference clock pair for PCIe lanes [0:7], also referred to as PCIe Group 0 Low and for the PCIe_BMC link
PCIe_REFCLK0_LO+	C60			CK_PE_100M_G0_LO_DP		
PCIe_REFCLK0_HI-	C56	O LV_DIFF	PCIE Clock	CK_PE_100M_G0_HI_DN	According Carrier board PCIe device routing, may need clock buffer design for multi device application.	Reference clock pair for PCIe lanes [8:15] also referred to as PCIe Group 0 High
PCIe_REFCLK0_HI+	C57			CK_PE_100M_G0_HI_DP		
PCIe_REFCLK1-	E93	O LV_DIFF	PCIE Clock	CK_PE_100M_G1_DN	According Carrier board PCIe device routing, may need clock buffer design for multi device application.	Reference clock pair for PCIe lanes [16:31] also referred to as PCIe Group 1
PCIe_REFCLK1+	E94			CK_PE_100M_G1_DP		
PCIe_REFCLK2-	F92	O LV_DIFF	PCIE Clock	CK_PE_100M_G2_DN	According Carrier board PCIe device routing, may need clock buffer design for multi device application.	Reference clock pair for PCIe lanes [32:47] also referred to as PCIe Group 2
PCIe_REFCLK2+	F93			CK_PE_100M_G2_DP		
PCIe_REFCLK3-	G93	O LV_DIFF	PCIE Clock	No Connect	Not support for COM-HPC Client module	Reference clock pair for PCIe lanes [48:63] also referred to as PCIe Group 3
PCIe_REFCLK3+	G94			No Connect		

PCI Express Clock - PCIe Clock Request

PCI Express Lanes	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
PCIe_CLKREQ0_LO#	A56	Bi-Dir OD CMOS	3.3V / 3.3V	PCIE_CLKREQ0_LO#	Connect to PCIe device clock request pin or clock buffer request pin	PCIe reference clock request signal from Carrier target devices for PCIe_REFCLK0_LO clock pair Module PU 10K
PCIe_CLKREQ0_HI#	A57	Bi-Dir OD CMOS	3.3V / 3.3V	PCIE_CLKREQ0_HI#	Connect to PCIe device clock request pin or clock buffer request pin	PCIe reference clock request signal from Carrier target devices for PCIe_REFCLK0_HI clock pair Module PU 10K
PCIe_CLKREQ1#	E96	Bi-Dir OD CMOS	3.3V / 3.3V	PCIE_CLKREQ1#	Connect to PCIe device clock request pin or clock buffer request pin	PCIe reference clock request signal from Carrier target devices for PCIe_REFCLK1 clock pair Module PU 10K
PCIe_CLKREQ2#	E97	Bi-Dir OD CMOS	3.3V / 3.3V	PCIE_CLKREQ2#	Connect to PCIe device clock request pin or clock buffer request pin	PCIe reference clock request signals from Carrier target devices for PCIe_REFCLK2 clock pair Module PU 10K
PCIe_CLKREQ3#	F95	Bi-Dir OD CMOS	3.3V / 3.3V	No Connect	Not support for COM-HPC Client module	PCIe reference clock request signals from Carrier target devices for PCIe_REFCLK3 clock pair Module PU 10K

PCI Express Clock - PCIe LANE Reversal

PCI Express Lanes	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
PEG_LANE_REV#	G19	I CMOS	Open or GND	BTB_PEG_LANE_REV#	Lane reversal application support for layout routing. Defualt PU on RPS9HC	PCI Express Graphics lane reversal input strap, may be used to reverse the lane order of PEG lanes on supported platforms. Pull low on the Carrier Board to reverse lane order, otherwise leave pin open. Pulled up on Module or Module chipset to chipset specific power rail.

Digital Display Interfaces (DDI) – DDI Signals

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

The COM-HPC Client Module pinout allows for up to three Digital Display Interfaces (DDI) to provide DisplayPort and HDMI/DVI capabilities.
The Client Module DDIs may support any combination of DisplayPort and HDMI.
Module DDI ports should support both DP and HDMI modes. Modules that support Dual-Mode DDI interface shall implement the necessary muxing circuitry and control logic to ensure that the Module works properly with Carriers expecting DisplayPort or HDMI operation.

DDI	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
DDI0_PAIR0-	D22	O LV_DIFF	AC coupled off Module	DDIB_TX0N	RPS9HC mapping to DFI Carrier Board COM836 DDI set to HDMI	DDI 0 to 2 Pair[0:3] differential pairs
DDI0_PAIR0+	D23			DDIB_TX0P		
DDI0_PAIR1-	D25	O LV_DIFF	AC coupled off Module	DDIB_TX1N		
DDI0_PAIR1+	D26			DDIB_TX1P		
DDI0_PAIR2-	D28	O LV_DIFF	AC coupled off Module	DDIB_TX2N	Due to layout length requirement, suggest to use re-driver for better signal quality or meet the SPEC requirement.	
DDI0_PAIR2+	D29			DDIB_TX2P		
DDI0_PAIR3-	D31	O LV_DIFF	AC coupled off Module	DDIB_TX3N		
DDI0_PAIR3+	D32			DDIB_TX3P		
DDI1_PAIR0-	A23	O LV_DIFF	AC coupled off Module	DDIC_TX0N	RPS9HC mapping to DFI Carrier Board COM836 DDI set to DP++	
DDI1_PAIR0+	A24			DDIC_TX0P		
DDI1_PAIR1-	A26	O LV_DIFF	AC coupled off Module	DDIC_TX1N		
DDI1_PAIR1+	A27			DDIC_TX1P		
DDI1_PAIR2-	A29	O LV_DIFF	AC coupled off Module	DDIC_TX2N	Due to layout length requirement, suggest to use re-driver for better signal quality or meet the SPEC requirement.	
DDI1_PAIR2+	A30			DDIC_TX2P		
DDI1_PAIR3-	A32	O LV_DIFF	AC coupled off Module	DDIC_TX3N		
DDI1_PAIR3+	A33			DDIC_TX3P		
DDI2_PAIR0-	E06	O LV_DIFF	AC coupled off Module	DDID_TX0N	RPS9HC mapping to DFI Carrier Board COM836 DDI set to DP++	
DDI2_PAIR0+	E07			DDID_TX0P		
DDI2_PAIR1-	E09	O LV_DIFF	AC coupled off Module	DDID_TX1N		
DDI2_PAIR1+	E10			DDID_TX1P		
DDI2_PAIR2-	E12	O LV_DIFF	AC coupled off Module	DDID_TX2N	Due to layout length requirement, suggest to use re-driver for better signal quality or meet the SPEC requirement.	
DDI2_PAIR2+	E13			DDID_TX2P		
DDI2_PAIR3-	E15	O LV_DIFF	AC coupled off Module	DDID_TX3N		
DDI2_PAIR3+	E16			DDID_TX3P		

Digital Display Interfaces (DDI) – DDI AUX Signals

Display AUX Signals	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
DDI0_SDA_AUX-	D19	I/O LV_DIFF	AC coupled on Module	DDI0_AUX_N_COM		DP AUX function if DDI[0:2]_DDC_AUX_SEL is a no connect or driven to GND on the Carrier. HDMI/DVI I2C clock if DDI[0:2]_DDC_AUX_SEL is pulled or driven high on the Carrier.
DDI0_SDA_AUX+	D20			DDI0_AUX_P_COM		
DDI1_SDA_AUX-	A20	I/O LV_DIFF	AC coupled on Module	DDI1_AUX_N_COM	The AUX and DDC select circuit design on RPS9HC module.	
DDI1_SDA_AUX+	A21			DDI1_AUX_P_COM		AUX+ PD 100K on module AUX- PU 100K on module
DDI2_SDA_AUX-	E03	I/O LV_DIFF	AC coupled on Module	DDI2_AUX_N_COM	Use DDI[0:2]_AUX_SEL to select AUX signals or DDC CLK/DAT signals for each DDI.	
DDI2_SDA_AUX+	E04			DDI2_AUX_P_COM		
DDI0_DDC_AUX_SEL	C26	I CMOS	3.3V / 3.3V	DDI0_AUX_SEL		Selects the function of DDI[0:2]_SCL_AUX+ and DDI[0:2]_SDA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is unconnected on the Carrier, the AUX pair is used for the DP AUX+/- signals. If pulled or driven high on the Carrier, the AUX pair contains the HDMI[0:2] I2C CRTL_CLK and CTRL_DAT signals.
DDI1_DDC_AUX_SEL	C27			I CMOS		
DDI2_DDC_AUX_SEL	E18	I CMOS	3.3V / 3.3V	DDI2_AUX_SEL		

PCI Express Clock - Display HPD

Display HPD	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
DDI0_HPD	C28	I CMOS	3.3V / 3.3V	DDI0_HPD_BTB		
DDI1_HPD	C29	I CMOS	3.3V / 3.3V	DDI1_HPD_BTB		DDI Hot-Plug Detect
DDI2_HPD	E19	I CMOS	3.3V / 3.3V	DDI2_HPD_BTB		PD 100K on module.
eDP_HPD	C30	I CMOS	3.3V / 3.3V	EDP_HPD_BTB		

Digital Display Interfaces (DDI) – eDP Signals

DDI	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
eDP_TX0-	A38	O LV_DIFF	AC coupled off Module	EDP1_TX0N		
eDP_TX0+	A39			EDP1_TX0P		
eDP_TX1-	A41	O LV_DIFF	AC coupled off Module	EDP1_TX1N		
eDP_TX1+	A42			EDP1_TX1P		eDP differential data pairs
eDP_TX2-	A44	O LV_DIFF	AC coupled off Module	EDP1_TX2N		
eDP_TX2+	A45			EDP1_TX2P		
eDP_TX3-	A47	O LV_DIFF	AC coupled off Module	EDP1_TX3N		
eDP_TX3+	A48			EDP1_TX3P		

Digital Display Interfaces (DDI) – eDP AUX Signals / Control

Display AUX Signals	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
eDP_AUX-	A35	I/O LV_DIFF	AC coupled on Module	EDP1_AUXN		eDP AUX channel differential pair
eDP_AUX+	A36			EDP1_AUXP		
eDP_VDD_EN	C31	O CMOS	3.3V / 3.3V	eDP_VDD_EN		eDP power enable
eDP_BKLT_EN	C32	O CMOS	3.3V / 3.3V	eDP_BKLT_EN		eDP backlight enable
eDP_BKLT_CTRL	C33	O CMOS	3.3V / 3.3V	eDP_BKLTCTL		EDP backlight brightness control

USB – USB2

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

The COM-HPC Client Module supports up to eight USB 2.0 ports and up to four USB 3.2 Gen 2x2 or USB4 ports
A COM-HPC USB 3.2 Gen 2x2 port may alternatively be used as a USB 3.2 Gen 1 or Gen 2 port as well.
RPS9HC module default BIOS USB designed for DFI COM836 carrier board.

USB	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
USB0-	D16	I/O USB 2.0	3.3V Suspend / 3.3V	USBP_1N		USB 2.0 differential pairs, channels 0 through 7.
USB0+	D17			USBP_1P		
USB1-	D13	I/O USB 2.0	3.3V Suspend / 3.3V	USBP_2N		USB0 may be configured as a USB client
USB1+	D14			USBP_2P		
USB2-	C17	I/O USB 2.0	3.3V Suspend / 3.3V	USBP_3N		or as a host, or both at the Module designer's
USB2+	C18			USBP_3P	Connect to USB connector or device.	discretion. All other USB ports, if implemented,
USB3-	C14	I/O USB 2.0	3.3V Suspend / 3.3V	USBP_4N	-- For **DFI COM836** applicaion,	shall be host ports.
USB3+	C15			USBP_4P	6* USB2 signals:	If any SuperSpeed ports are implemented, then
USB4-	B16	I/O USB 2.0	3.3V Suspend / 3.3V	USBP_5N	Use on USB3.2 Gen2 Type-C & Type-A.	they must be supported by a USB 2.0 port,
USB4+	B17			USBP_5P	2* USB2 signals:	using one of the USB[0:3] ports from this pool.
USB5-	B13	I/O USB 2.0	3.3V Suspend / 3.3V	USBP_6N	Use on M.2 Key B & Key E.	Specific pairings are detailed below.
USB5+	B14			USBP_6P		
USB6-	A17	I/O USB 2.0	3.3V Suspend / 3.3V	USBP_7N		
USB6+	A18			USBP_7P		
USB7-	A14	I/O USB 2.0	3.3V Suspend / 3.3V	USBP_8N		
USB7+	A15			USBP_8P		

USB – USB Over Current

USB	Pin Number	Pin Type	Pwr Rail /Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
USB01_OC#	B28	I CMOS	3.3V Suspend / 3.3V	USBOC_01#		USB over-current sense, USB channels 0,1; channels 2,3; channels 4,5 and channels 6,7
USB23_OC#	B27	I CMOS	3.3V Suspend / 3.3V	USBOC_23#		respectively. A pull-up for each of these lines to the 3.3V Suspend rail shall be present on the Module. The pull-up should be 10K. An open drain driver from USB current monitors on the Carrier Board may drive this line low. The Carrier Board shall not not pull these lines up.
USB45_OC#	B26	I CMOS	3.3V Suspend / 3.3V	USBOC_45#		Note that the over-current limits for USB 2.0 and USB 3.0 are different; this is a Carrier board implementation item.
USB67_OC#	B25	I CMOS	3.3V Suspend / 3.3V	USBOC_67#		

USB – USB3.2 Gen2

USB	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
USB0_SSTX0-	D43	O USB SS	AC coupled on Module	USB3_TX1N		Four sets of SuperSpeed transmit pairs, used to realize the transmit side of two USB 3.2 Gen 2x2 ports. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. These ports shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB0_SSxxx+/- shall be used with the USB0 USB 2.0 pair and so on, USB1_SSxxx+/- with the USB1 USB 2.0 pair).
USB0_SSTX0+	D44			USB3_TX1P		
USB0_SSTX1-	D46	O USB SS	AC coupled on Module	USB3_TX2N		
USB0_SSTX1+	D47			USB3_TX2P		
USB1_SSTX0-	D37	O USB SS	AC coupled on Module	USB3_TX7N		
USB1_SSTX0+	D38			USB3_TX7P		
USB1_SSTX1-	D40	O USB SS	AC coupled on Module	USB3_TX8N		
USB1_SSTX1+	D41			USB3_TX8P		
USB0_SSRX0-	C44	I USB SS	AC coupled on Module	USB3_RX1N		Four sets of SuperSpeed receive pairs, used to realize the receive side of two USB 3.2 Gen 2x2 ports. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. These ports shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB0_SSxxx+/- shall be used with the USB0 USB 2.0 pair, USB1_SSxxx+/- with the USB1 USB 2.0 pair).
USB0_SSRX0+	C45			USB3_RX1P		
USB0_SSRX1-	C47	I USB SS	AC coupled on Module	USB3_RX2N		
USB0_SSRX1+	C48			USB3_RX2P		
USB1_SSRX0-	C38	I USB SS	AC coupled on Module	USB3_RX7N		
USB1_SSRX0+	C39			USB3_RX7P		
USB1_SSRX1-	C41	I USB SS	AC coupled on Module	USB3_RX8N		
USB1_SSRX1+	C42			USB3_RX8P		

USB	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
USB2_SSTX0-	H02	O USB SS	AC coupled on Module	USB3_TX3N		Four sets of SuperSpeed transmit pairs, used to realize the transmit side of two USB 3.2 Gen 2x2 ports. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. These ports shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB2_SSxxx+/- shall be used with the USB2 USB 2.0 pair, USB3_SSxxx+/- with the USB3 USB 2.0 pair).
USB2_SSTX0+	H03			USB3_TX3P		
USB2_SSTX1-	H25	O USB SS	AC coupled on Module	USB3_TX4N		
USB2_SSTX1+	H06			USB3_TX4P		
USB3_SSTX0-	H08	O USB SS	AC coupled on Module	USB3_TX5N		
USB3_SSTX0+	H09			USB3_TX5P		
USB3_SSTX1-	H11	O USB SS	AC coupled on Module	USB3_TX6N		
USB3_SSTX1+	H12			USB3_TX6P		
USB2_SSRX0-	G03	I USB SS	AC coupled on Module	USB3_RX3N		Four sets of SuperSpeed receive pairs, used to realize the receive side of two USB 3.2 Gen 2x2 ports. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. These ports shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB0_SSxxx+/- shall be used with the USB0 USB 2.0 pair, USB1_SSxxx+/- with the USB1 USB 2.0 pair).
USB2_SSRX0+	G04			USB3_RX3P		
USB2_SSRX1-	G06	I USB SS	AC coupled on Module	USB3_RX4N		
USB2_SSRX1+	G07			USB3_RX4P		
USB3_SSRX0-	G09	I USB SS	AC coupled on Module	USB3_RX5N		
USB3_SSRX0+	G10			USB3_RX5P		
USB3_SSRX1-	G12	I USB SS	AC coupled on Module	USB3_RX6N		
USB3_SSRX1+	G13			USB3_RX6P		

NBASE - T Ethernet

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

Two NBASE-T Ethernet ports, designated NBASET0 and NBASET1, are defined for the Client, and one for the Server. The ports may operate in 10 Gbps, 5 Gbps, 2.5 Gbps, 1 Gbps, 100 Mbps or 10 Mbps modes. Magnetics are to be on the Carrier Board. All COM-HPC Modules shall implement at least one port on the NBASET0 pin set and this shall be capable of the 1000BASE-T mode.

Gigabit Ethernet	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
NBASET0_MDI0-	D85	I/O MDI	3.3V Suspend / 3.3V	LAN1_MDI0_N	RPS9HC use i226LM or i226V, max support 2.5Gbe LAN.	Ethernet Controller 1: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 10 Gbps, 1 Gbps, 100 Mbps and 10 Mbps modes. Some pairs are unused in some modes, per the following:
NBASET0_MDI0+	D86			LAN1_MDI0_P		
NBASET0_MDI1-	D88			LAN1_MDI1_N		
NBASET0_MDI1+	D89			LAN1_MDI1_P		
NBASET0_MDI2-	D91			LAN1_MDI2_N		
NBASET0_MDI2+	D92			LAN1_MDI2_P		
NBASET0_MDI3-	D94			LAN1_MDI3_N		
NBASET0_MDI3+	D95			LAN1_MDI3_P		

	10000BASE-T 1000BASE-T	100BASE-TX	10BASE-T
MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-
MDI[2]+/-	B1_DC+/-		
MDI[3]+/-	B1_DD+/-		

Gigabit Ethernet	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
NBASET0_LINK_MAX#	D97	Output CMOS	3.3V Suspend / 3.3V	GBE0_LED_2500#		NBASE-T Ethernet Controller MAX Speed Link indicator, active low. If active, the link is established at the maximum speed that the Ethernet controller is capable of (which may be 10 Gbps, 5 Gbps, 2.5 Gbps etc). 20 mA or more current sink capability at VOL of 0.4V max. 20 mA or more current source capability at VOH of 2.4V min.
NBASET0_LINK_MID#	D98	Output CMOS	3.3V Suspend / 3.3V	GBE0_LED_1000#		NBASE-T Ethernet Controller MID Speed Link indicator, active low. If active, the link is established but at a speed lower than what the maximum speed that the Ethernet controlleris capable of. 20 mA or more current sink capability at VOL of 0.4V max. 20 mA or more current source capability at VOH of 2.4V min.
NBASET0_LINK_ACT#	D99	Output CMOS	3.3V Suspend / 3.3V	GBE0_LED_LINK_ACT#		NBASE-T Ethernet Controller activity indicator, active low. 20 mA or more current sink capability at VOL of 0.4V max. 20 mA or more current source capability at VOH of 2.4V min.
NBASET0_SDP	C98	I/O CMOS	3.3V Suspend / 3.3V	BTB_GBE0_SDP0 (Default No Connect to Carrier)	RPS9HC default no support, need to set FW for intel LAN and BOM	NBASE-T Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1 PPS signal.
NBASET0_CTREF	C99	REF	GND min 3.3V max	No Connect		Reference voltage for Carrier Board NBASET Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. If not needed, these pins may be left open on the Carrier. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.

Gigabit Ethernet	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
NBASET1_MDI0-	F71	I/O MDI	3.3V Suspend / 3.3V	LAN2_MDI0_N	RPS9HC use i226LM or i226V, max support 2.5Gbe LAN.	Ethernet Controller 1: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 10 Gbps, 1 Gbps, 100 Mbps and 10 Mbps modes. Some pairs are unused in some modes, per the following:
NBASET1_MDI0+	F72			LAN2_MDI0_P		
NBASET1_MDI1-	F74			LAN2_MDI1_N		
NBASET1_MDI1+	F75			LAN2_MDI1_P		
NBASET1_MDI2-	F77			LAN2_MDI2_N		
NBASET1_MDI2+	F78			LAN2_MDI2_P		
NBASET1_MDI3-	F80			LAN2_MDI3_N		
NBASET1_MDI3+	F81			LAN2_MDI3_P		

	10000BASE-T 1000BASE-T	100BASE-TX	10BASE-T
MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-
MDI[2]+/-	B1_DC+/-		
MDI[3]+/-	B1_DD+/-		

Gigabit Ethernet	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
NBASET1_LIN_MAX#	D97	Output CMOS	3.3V Suspend / 3.3V	GBE1_LED_2500#		NBASE-T Ethernet Controller MAX Speed Link indicator, active low. If active, the link is established at the maximum speed that the Ethernet controller is capable of (which may be 10 Gbps, 5 Gbps, 2.5 Gbps etc). 20 mA or more current sink capability at VOL of 0.4V max. 20 mA or more current source capability at VOH of 2.4V min.
NBASET1_LINK_MID#	D98	Output CMOS	3.3V Suspend / 3.3V	GBE1_LED_1000#		NBASE-T Ethernet Controller MID Speed Link indicator, active low. If active, the link is established but at a speed lower than what the maximum speed that the Ethernet controlleris capable of. 20 mA or more current sink capability at VOL of 0.4V max. 20 mA or more current source capability at VOH of 2.4V min.
NBASET1_LINK_ACT#	D99	Output CMOS	3.3V Suspend / 3.3V	GBE1_LED_LINK_ACT#		NBASE-T Ethernet Controller activity indicator, active low. 20 mA or more current sink capability at VOL of 0.4V max. 20 mA or more current source capability at VOH of 2.4V min.
NBASET1_SDP	C98	I/O CMOS	3.3V Suspend / 3.3V	BTB_GBE1_SDP0 (Default No Connect to Carrier)	RPS9HC default no support, need to set FW for intel LAN and BOM	NBASE-T Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1 PPS signal.
NBASET1_CTREF	C99	REF	GND min 3.3V max	No Connect		Reference voltage for Carrier Board NBASET Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. If not needed, these pins may be left open on the Carrier. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.

Serial ATA(SATA)

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

Two Serial ATA links for support of SATA-150 (revision 1.0, 1.5Gb/s), SATA-300 (revision 2.0, 3Gb/s), and SATA-600 (revision 3.0, 6Gb/s) devices are defined, for the Client Module and the Server Module.

Serial ATA	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
SATA0_TX-	D52	O SATA	AC coupled on Module	SATA_RX4N		Serial ATA Channel 0 transmit differential pair.
SATA0_TX+	D53			SATA_RX4P		
SATA0_RX-	D49	I SATA	AC coupled on Module	SATA_TX4N	Carrier board SATA connector need close module if no re-driver design.	Serial ATA Channel 0 receive differential pair.
SATA0_RX+	D50			SATA_TX4P		
SATA1_TX-	D58	O SATA	AC coupled on Module	SATA_RX5N	COM-HPC no define SATA LED, different with COM Express platform	Serial ATA Channel 1 transmit differential pair.
SATA1_TX+	D59			SATA_RX5P		
SATA1_RX-	D55	I SATA	AC coupled on Module	SATA_TX5N		Serial ATA Channel 1 receive differential pair.
SATA1_RX+	D56			SATA_TX5P		

eSPI

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

COM-HPC supports an eSPI port for general purpose I/O. The eSPI interface (like LPC before it) can be useful for general purpose devices such as Carrier Super I/O devices, Carrier CPLDs or FPGAs, hardware monitoring devices, and others.
The eSPI bus runs from a 1.8V supply. COM-HPC does not support LPC.
X86 CPU Module implementations should include the eSPI interface. ARM Module implementations may implement an eSPI or QSPI interface.
RPS9HC eSPI ESPI_CS0# device implement EC IT5782, carrier board can design 2nd eSPI device.

eSPI Signal	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
eSPI_IO0	A50	I/O CMOS	1.8V Suspend / 1.8V	BTB_ESPI_IO0		eSPI Master Data Input / Outputs. These are bi-directional input/output pins used to transfer data between master and slaves.
eSPI_IO1	A51	I/O CMOS	1.8V Suspend / 1.8V	BTB_ESPI_IO1		
eSPI_IO2	A52	I/O CMOS	1.8V Suspend / 1.8V	BTB_ESPI_IO2		
eSPI_IO3	A53	I/O CMOS	1.8V Suspend / 1.8V	BTB_ESPI_IO3		
eSPI_CS0#	B54	O CMOS	1.8V Suspend / 1.8V	BTB_ESPI_CS#		eSPI Master Chip Select Outputs. A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select pin. If an eSPI_CSx# pins is not in use, it shall be either pulled high or actively driven high.
eSPI_CS1#	B55	O CMOS	1.8V Suspend / 1.8V	ESPI_CS2#		
eSPI_CLK	A54	O CMOS	1.8V Suspend / 1.8V	BTB_ESPI_CLK		eSPI Master Clock Output. This pin provides the reference timing for all the serial input and output operations
eSPI_ALERT0#	B52	I CMOS	1.8V Suspend / 1.8V	ESPI_ALERT1#		eSPI pins used by eSPI slave to request service from the eSPI master.
eSPI_ALERT1#	B53	I CMOS	1.8V Suspend / 1.8V	ESPI_ALERT2#		eSPI pins used by eSPI slave to request service from the eSPI master.
eSPI_RST#	B56	O CMOS	1.8V Suspend / 1.8V	ESPI_RST#		eSPI Reset - resets the eSPI interface for both master and slaves. eSPI_RST# is typically driven from the eSPI master to eSPI slaves.

SPI

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

The Boot SPI interface is used to support loading all or parts of the system BIOS from a Module or Carrier based SPI (Serial Peripheral Interface) or SQI (Serial Quad Interface) flash device. The SPI or SQI flash device can be up to 64 MB (512 Mb). Two flash devices may be used on the Module, allowing up to 128 MB of boot code storage on the Module. Alternatively, there may be a flash device on the Carrier and / or on the Module, for a combined total of up to 128 MB. In most situations, only one flash device, either on the Module or on the Carrier, is used.

The SPI bus is clocked at either 20 MHz, 25 MHz, 33 MHz or 50 MHz. SPI devices selected shall support one of these frequencies. COM-HPC defines a VCC_BOOT_SPI pin that may be either 1.8V or 3.3V. A Carrier SPI flash device, if implemented, shall be powered by the VCC_BOOT_SPI pin provided.
RPS9HC module device have SPI flash and TPM, also support boot from Carrier SPI by EC control the chip select.
RPS9HC VCC_BOOT_SPI design with 3.3V level (3V3DU)

Boot SPI Interface	Pin Number	Pin Type	Pwr Rail /Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
BOOT_SPI_CS#	A50	O CMOS	VCC_BOOT_SPI / VCC_BOOT_SPI	CB_SPI_CS#		Chip select for Carrier Board SPI If the BOOT_SPI_CS# pin is not in use, it shall be either pulled high or actively driven high.
BOOT_SPI_IO0	A51	I/O CMOS	VCC_BOOT_SPI / VCC_BOOT_SPI	SPI_MOSI_CB	Carrier board design need take care the SPI routing method from intel design topology.	Bidirectional 4 bit data path out of and into a Carrier SPI flash operating in Serial Quad Interface (SQI) mode. If the flash memory device is operating in traditional Serial Peripheral Interface (SPI) mode, then signal BOOT_SPI_IO0 is used for getting serial data into the flash device (referred to as SI or MOSI in SPI Flash data sheets) and signal BOOT_SPI_IO1 is used to get serial data from the flash device (referred to as SO or MISO in flash data sheets)
BOOT_SPI_IO1	A52	I/O CMOS	VCC_BOOT_SPI / VCC_BOOT_SPI	SPI_MISO_CB		
BOOT_SPI_IO2	A53	I/O CMOS	VCC_BOOT_SPI / VCC_BOOT_SPI	SPI_IO2_CB		
BOOT_SPI_IO3	B54	I/O CMOS	VCC_BOOT_SPI / VCC_BOOT_SPI	SPI_IO3_CB		
BOOT_SPI_CLK	B55	O CMOS	VCC_BOOT_SPI / VCC_BOOT_SPI	SPI_CLK_CB		Clock from Module chipset to Carrier SPI
VCC_BOOT_SPI	A54	Power (Out from Module)	1.8V or 3.3V Suspend or S0 vendor specific	SPIPWR_3VDU	RPS9HC VCC_BOOT_SPI design with 3.3V level	Power supply for Carrier Board SPI – sourced from Module – nominally either 1.8V or 3.3V. The Module shall provide a minimum of 100mA on VCC_BOOT_SPI. Carriers shall use less than 100mA from this power source. VCC_BOOT_SPI shall only be used to power SPI devices on the Carrier Board. The Module vendor may choose what power domains the BOOT_SPI is active in.

MAFS and SAFS BIOS Configurations

COM-HPC Module

COM-HPC Carrier Board
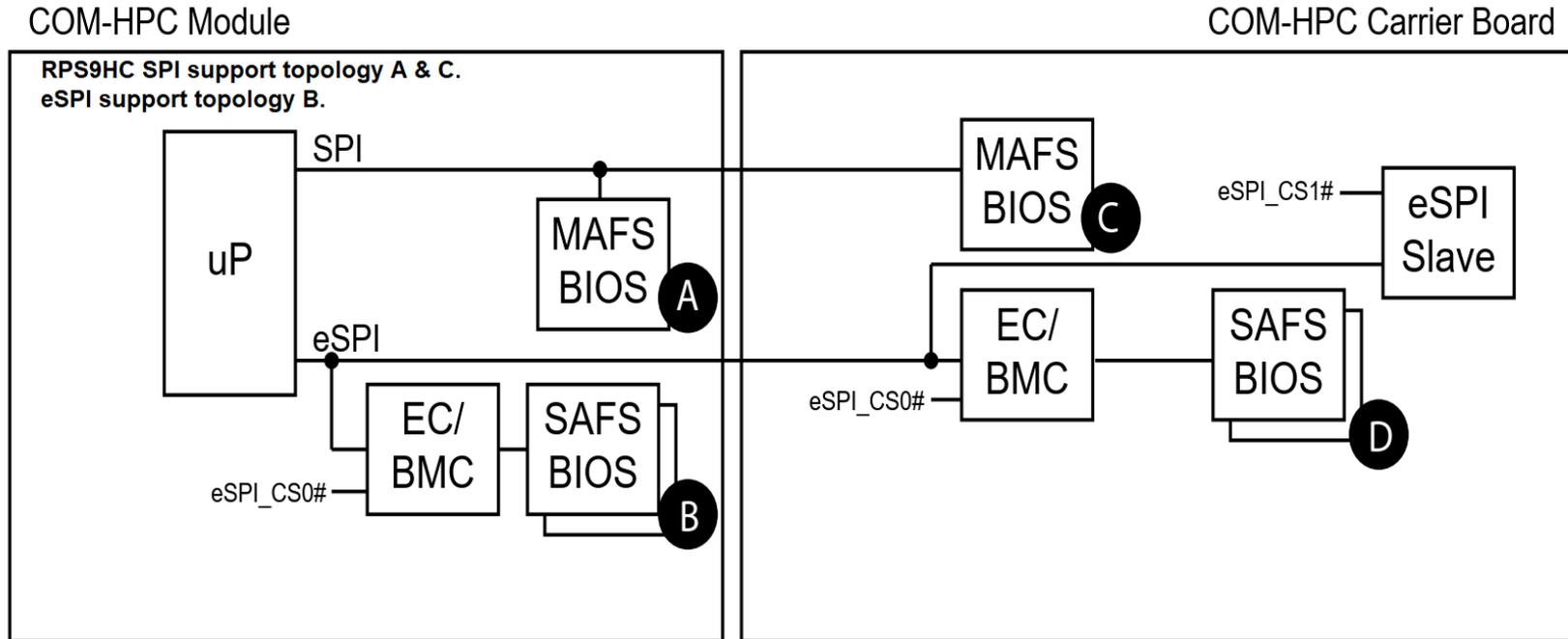
Note: Only B or D is supported, not both.

Boot SPI Interface	Pin Number	Pin Type	Pwr Rail /Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
BSEL2	B51	I	Module Specific. Leave Open on Carrier or pull hard to GND on Carrier	BIOS_SEL2		Boot Select pins. These pins distinguish between a SPI or eSPI BIOS boot and between an on—Module or off-Module BIOS.
BSEL1	B50	I		BIOS_SEL1		
BSEL0	B49	I		BIOS_SEL0		

Important:
Due to RPS9HC eSPI0_CS0# on module, RPS9HC Only supports Ref 7a, 6, 5, please refer to the document **PICMG® COM-HPC® Module Base Specification Revision 1.20** for more information.

Serial Audio Interfaces - Soundwire Audio Signals

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

Soundwire Signal	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
SNDW_DMIC_CLK0	C23	O	1.8V Suspend / 1.8V	SNDW_DMIC_CLK0		Clock for Soundwire transactions
SNDW_DMIC_DAT0	C24	I/O		SNDW_DMIC_DAT0		Bi-directional PCM audio data
SNDW_DMIC_CLK1	C20	O	1.8V Suspend / 1.8V	SNDW_DMIC_CLK1		Clock for Soundwire transactions
SNDW_DMIC_DAT1	C21	I/O		SNDW_DMIC_DAT1		Bi-directional PCM audio data

HDA Signal	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
HDA_BCLK	B23	O	1.8V Suspend / 1.8V	AUD_LINK_BCLK		HDA serial data clock
HDA_SDI	B22	I/O		AUD_LINK_SDI0		HDA serial TDM data input
HDA_SDO	B20	I/O		AUD_LINK_SDO		HDA serial TDM data output
HDA_SYNC	B19	O		AUD_LINK_SYNC		HDA sample synchronization signal
HDA_RST#	B21	O		AUD_LINK_RST-		HDA reset output

Asynchronous Serial Port Interfaces - UART0 * Support ouput BIOS debug message

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

Two logic level Module 5 wire (TX, RX, RTS#, CTS#, GND) asynchronous serial ports are provided for general purpose use and for use with debugging software that make use of the console redirect features available in many BIOSes and operating systems. The Module BIOS should support console redirect to the UART0 port.

Serial Port	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
UART0_TX	C89	O CMOS	3.3V Suspend / 3.3V	EC_TX0		Logic level asynchronous serial port transmit signal
UART0_RX	C90	I CMOS	3.3V Suspend / 3.3V	EC_RX0		Logic level asynchronous serial port receive signal PU on Module
UART0_RTS	C91	O CMOS	3.3V Suspend / 3.3V	EC_RTS0		Logic level asynchronous serial port Request to Send signal, active low
UART0_CTS	C92	I CMOS	3.3V Suspend / 3.3V	EC_CTS0		Logic level asynchronous serial port Clear to Send input, active low PU on Module

Asynchronous Serial Port Interfaces - UART1

Serial Port	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
UART1_TX	B87	O CMOS	3.3V Suspend / 3.3V	EC_TX1		Logic level asynchronous serial port transmit signal
UART1_RX	B88	I CMOS	3.3V Suspend / 3.3V	EC_RX1		Logic level asynchronous serial port receive signal PU on Module
UART1_RTS	B89	O CMOS	3.3V Suspend / 3.3V	EC_RTS1		Logic level asynchronous serial port Request to Send signal, active low
UART1_CTS	B90	I CMOS	3.3V Suspend / 3.3V	EC_CTS1		Logic level asynchronous serial port Clear to Send input, active low PU on Module

I2C Signals

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

Two general purpose I2C ports are defined for COM-HPC. The first of the two supports an ALERT# input. The ports shall support 100 kHz operation and should support 400 kHz operation. The ports should be multi-master capable. I2C0 is defined to operate from a 3.3V rail and I2C1 from a 1.8V rail. The I2C1 port may be I3C capable.

I2C Signal	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
I2C0_CLK	C93	I/O OD CMOS	3.3V Suspend / 3.3V	BTB_I2C_CLK		Clock I/O line for the general purpose I2C0 port PU 2K2 on Module
I2C0_DAT	C94	I/O OD CMOS	3.3V Suspend / 3.3V	BTB_I2C_DATA		Data I/O line for the general purpose I2C0 port PU 2K2 on Module
I2C0_ALERT#	C95	I CMOS	3.3V Suspend / 3.3V	BTB_I2C_ALERT#		Alert input / interrupt for I2C0 PU 2K2 on Module
I2C1_CLK	C96	I/O OD CMOS	1.8V Suspend/ 1.8V	PCH_1V8_I2C4_SCL		Clock I/O line for the general purpose I2C1 port PU 2K2 on Module
I2C1_DAT	C97	I/O OD CMOS	1.8V Suspend/ 1.8V	PCH_1V8_I2C4_SDA		Data I/O line for the general purpose I2C1 port PU 2K2 on Module
USB_PD_I2C_CLK	B35	Bi-Dir OD	3.3V Suspend / 3.3V	I2C_PD_CLK_BTB	DFI COM836 Carrier board designed 7-seg for Port 80 message. Reserve connection for USB-C PD.	COM-HPC Client and Server Modules should support exporting Port 80 information over the USB_PD I2C bus to Carrier hardware that implements a pair of 7-segment displays to show the codes.
USB_PD_I2C_DAT	B36	Bi-Dir OD	3.3V Suspend / 3.3V	I2C_PD_DATA_BTB		
USB_PD_ALERT#	B34	I	3.3V Suspend / 3.3V	I2C_PD_ALERT#		

SMBUS

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

The SMBus port is specified for system management functions. It is used on the Module to manage system functions such as reading the DRAM SPD EEPROM and setting clock synthesizer parameters. If the SMBus is used on the Carrier, then great care must be taken that no conflicts with the on-Module SMBus devices occur. It may be useful for implementation on the Carrier Board of standards such as Smart Battery. The maximum capacitance on the Carrier Board shall not shall not exceed 100pF.

SMBUS Signal	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
SMB_CLK	C86	I/O OD CMOS	3.3V Suspend / 3.3V	BTB_I2C_CLK		System Management Bus bidirectional clock line. PU on module
SMB_DAT	C87	I/O OD CMOS	3.3V Suspend / 3.3V	BTB_I2C_DATA		System Management Bus bidirectional data line. PU on module
SMB_ALERT#	C88	I CMOS	3.3V Suspend / 3.3V	BTB_I2C_ALERT#		System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. PU on module

GSPI

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

Miscellaneous	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
GP_SPI_MISO	B94	I CMOS	3.3V / 3.3V	PCH_3V3_GSPI0_MISO		Serial data into the COM-HPC Module from the Carrier GP_SPI device (Master In Slave Out) Module PU
GP_SPI_MOSI	B93	O CMOS	3.3V / 3.3V	PCH_3V3_GSPI0_MOSI		Serial data from the COM-HPC Module to the Carrier GP_SPI device (Master Out Slave In)
GP_SPI_CLK	B99	O CMOS	3.3V / 3.3V	PCH_3V3_GSPI0_CLK		Clock from the Module to Carrier GP_SPI device
GP_SPI_CS0#	B95	O CMOS	3.3V / 3.3V	PCH_3V3_GSPI0_CS0#		
GP_SPI_CS1#	B96	O CMOS	3.3V / 3.3V	PCH_3V3_GSPI0_CS1#		GP_SPI chip selects, active low
GP_SPI_CS2#	B97	O CMOS	3.3V / 3.3V	No connect	No support for RPS9HC	
GP_SPI_CS3#	B98	O CMOS	3.3V / 3.3V	No connect		
GP_SPI_ALERT#	B100	I CMOS	3.3V / 3.3V	PCH_GSPI0_ALERT#		Alert (interrupt) from a Carrier GP_SPI device to the Module Module PU

Power and System Management

Pin Types
I : Input to the Module
O : Output from the Module
I/O : Bi-directional input / output signal
OD : Open drain output
RSVD : pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

Signals VIN_PWR_OK, RSTBTN#, and PLTRST# shall be supported for all COM-HPC Modules. Signal VIN_PWR_OK indicates that all the power to the Module is stable within the specified range and can be used to enable Module internal power supplies.
On COM Express designs, the VIN_PWR_OK line is used to hold off a CPU boot to allow off Module devices such as large FPGAs enough time to be configured. This method should not be used on COM-HPC designs. An alternative method, pausing the Module boot by BIOS code monitoring the RSTBTN# line.

Miscellaneous	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description	Module PU/PD
PWRBTN#	B02	I CMOS	3.3V Suspend / 3.3V	CB_PWRBTN#		A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down (with a sustained low).	PU
RSTBTN#	C02	I CMOS	3.3V Suspend / 3.3V	SYS_RST-		Reset button input. The RSTBTN# may be level sensitive (active low) or may be triggered by the falling edge of the signal.	PU
PLTRST#	A12	O CMOS	3.3V Suspend / 3.3V	PLTRST#_BTB		Platform Reset: output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. PLTRST# should remain asserted (low) while the RSTBTN# is low.	
VIN_PWR_OK	C06	I CMOS	3.3V Suspend / 3.3V	CB_PWROK		Power OK from main power supply. A high value indicates that the power is good.	PU
SUS_S3#	B08	O CMOS	3.3V Suspend / 3.3V	EC_PM_SLP_S3#		Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board should be used to enable the non-standby power on a typical ATX supply. Even in single input supply system implementations (AT mode, no standby input), the SUS_S3# Module output should be used disable any Carrier voltage regulators when SUS_S3# is low, to prevent bleed leakage from Carrier circuits into the Module.	
SUS_S4_S5#	C08	O CMOS	3.3V Suspend / 3.3V	EC_PM_SLP_S4#		Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	
SUS_CLK	A87	O CMOS	3.3V Suspend / 3.3V	PCH_SUSCLK		32.768 kHz +/- 100 ppm clock used by Carrier peripherals such as M.2 cards in their low power modes.	
WAKE0#	D10	I CMOS	3.3V Suspend / 3.3V	PCIE_WAKE-		PCI Express wake up signal.	PU
WAKE1#	D11	I CMOS	3.3V Suspend / 3.3V	BTB_WAKE1#		General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.	PU
BATLOW#	A11	I CMOS	3.3V Suspend / 3.3V	PM_BATLOW#		Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	PU

Miscellaneous	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description	Module PU/PD
LID#	B45	I CMOS	3.3V Suspend / 3.3V	LID_BTN#		LID switch. Low active signal used by the ACPI operating system for a LID switch.	PU
SLEEP#	B46	I CMOS	3.3V Suspend / 3.3V	SLP_BTN#		Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	PU
TAMPER#	B06	I CMOS	VCC_RTC / 3.3V	BTB_TAMPER#		Tamper or Intrusion detection line on VCC_RTC power well. Carrier hardware pulls this low on a Tamper event	PU
AC_PRESENT	D34	I CMOS	3.3V Suspend / 3.3V	BTB_AC_PRESENT		Driven hard low on Carrier if system AC power is not present	PU
RSMRST_OUT#	B86	O CMOS	3.3V Suspend / 3.3V	RSMRST_OUT#		This is a buffered copy of the internal Module RSMRST# (Resume Reset, active low) signal. The internal Module RSMRST# signal is an input to the chipset or SOC and when it transitions from low to high it indicates that the suspend well power rails are stable. USB devices on the Carrier that are to be active in S5 / S3 / S0 should not have their 5V supply applied before RSMRST_OUT# goes high. RSMRST_OUT# shall be a 3.3V CMOS Module output, active in all power states.	
RAPID_SHUTDOWN	E01	I CMOS	5.0V Suspend/ 5.0V	BTB_RAPID_SHUTDOWN	EC implement. Need to custom software to trigger event.	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 μs. Pull-down / disable on Module if RAPID_SHUTDOWN pin is not asserted.	
CARRIER_HOT#	C04	I CMOS	3.3V / 3.3V	BTB_THRM#	PCH implement. Need to custom software to trigger event.	Input from off-Module temp sensor indicating an over-temp situation.	PU
THERMTRIP#	B06	O CMOS	3.3V / 3.3V	BTB_THERMTRIP#		Active low output indicating that the CPU has entered thermal shutdown.	
CATERR#	F11	O CMOS	3.3V / 3.3V	BTB_CATERR#		Active low output indicating a temperature excursion event on the COM-HPC Module	
PROCHOT#	F10	O CMOS	3.3V / 3.3V	BTB_PROCHOT#		Active low output indicating that the CPU has entered thermal shutdown	

General Purpose Input Outputs

GPIO	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description	Module PU/PD
GPIO_00	A88	I/O CMOS	3.3V Suspend / 3.3V	BTB_GPIO0			PU
GPIO_01	A89	I/O CMOS	3.3V Suspend / 3.3V	BTB_GPIO1			PU
GPIO_02	A90	I/O CMOS	3.3V Suspend / 3.3V	BTB_GPIO2			
GPIO_03	A91	I/O CMOS	3.3V Suspend / 3.3V	BTB_GPIO3			PU
GPIO_04	A92	I/O CMOS	3.3V Suspend / 3.3V	BTB_GPIO4			PU 100K
GPIO_05	A93	I/O CMOS	3.3V Suspend / 3.3V	BTB_GPIO5		General purpose input / output pins. Upon a hardware reset, these pins should be configured as inputs. As inputs, these pins shouldbe able to generate an interrupt to the Module host.	PU 100K
GPIO_06	A94	I/O CMOS	3.3V Suspend / 3.3V	BTB_GPIO6			PU 100K
GPIO_07	A95	I/O CMOS	3.3V Suspend / 3.3V	BTB_GPIO7			PU 100K
GPIO_08	A96	I/O CMOS	3.3V Suspend / 3.3V	BTB_GPIO8			PU 100K
GPIO_09	A97	I/O CMOS	3.3V Suspend / 3.3V	BTB_GPIO9			PU 100K
GPIO_10	A98	I/O CMOS	3.3V Suspend / 3.3V	BTB_GPIO10			PU 100K
GPIO_11	A99	I/O CMOS	3.3V Suspend / 3.3V	BTB_GPIO11			PU 100K

Module Type Definition

Module Type Definition	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description	Module PU/PD
TYPE0	A100	PDS	3.3V Suspend / 3.3V	BTB_TYPE00		The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). These pins shall be pulled up on the Carrier, to Carrier standby voltage rail of 5V or less. Carrier hardware reads the level on these straps.	
TYPE1	C100	PDS	3.3V Suspend / 3.3V	BTB_TYPE01	RPS9HC fixed TYPE[2:0] = 000 Carrier Board should have TYPE check circuit for different power input and protect.	The Carrier Board should implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX PS_ON# signal to an ATX power supply or otherwise deactivates VCC to the COM-HPC Module) if an incompatible Module pin-out type is detected. All three TYPE[x] pins should be monitored by the Carrier. The Carrier Board logic may also implement a fault indicator such as an LED. This is discussed in Section 8.5 and diagramed in two figures in that Section.	
TYPE2	D100	PDS	3.3V Suspend / 3.3V	BTB_TYPE02			

	Module Connections			Meaning
Ref	TYPE2	TYPE1	TYPE0	
7	NC	NC	NC	Mini Module – Wide Range 8V to 20V input
6	NC	NC	GND	Reserved
5	NC	GND	NC	Reserved
4	NC	GND	GND	Server Module – Fixed 12V input
3	GND	NC	NC	Reserved
2	GND	NC	GND	Reserved
1	GND	GND	NC	Client Module - Wide Range 8V to 20V input
0	GND	GND	GND	Client Module – Fixed 12V input

Miscellaneous Signals

Miscellaneous	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description	Module PU/PD
WD_OUT		O CMOS	3.3V/ 3.3V	CB_PWRBTN#		Output indicating that a watchdog time-out event has occurred.	
WD_STROBE#		I CMOS	3.3V/ 3.3V	SYS_RST-		Strobe input to watchdog timer. Periodic strobing prevents the watchdog, if enabled, from timing out.	PU
FAN_PWMOUT		O CMOS	3.3V/ 3.3V	PLTRST#_BTB		Fan speed control for a secondary system fan. The primary fan control signals for CPU thermal management are on the Module, along with a vendor specific connector. Fan controllers use the Pulse Width Modulation (PWM) technique to control the fan speed, via the FAN_PWMOUT signal. Carrier designers should buffer this signal with an open drain FET and pullup or other robust Carrier device(s).	PU
FAN_TACHIN		I OD CMOS	3.3V/ 3.3V	CB_PWROK		Fan tachometer input for a fan with a two pulse per revolution output for the secondary fan.	PU
TEST#		I OD CMOS	3.3V Suspend	EC_PM_SLP_S3#		Module input to allow vendor specific Module test mode(s). Carrier designers should leave this pin open on the Carrier. Designers involved in the design of specialty Carriers for Module test may pull this line to GND or possibly to a Module specific analog voltage between GND and 3.3V to select a test mode.	
RSVD						Reserved pins. These may be assigned functions in future versions of this specification. Reserved pins shall not be connected to anything, and shall not be connected to each other.	

Power and Ground

Miscellaneous	Pin Number	Pin Type	Pwr Rail / Tolerance	RPS9HC Net Name	Carrier Board Design Recommended	Signals Description
VCC	A01-A09, B01, B03, B05, B07, B09 C01, C03, C05, C07, C09 D01-D09	Power	3.3V Suspend / 3.3V	12V		Primary power input: fixed +12V on the Client Type 0; wide range +8V to +20V on the Client Type 1; fixed +12V on the Server. Refer to Section 8 Module Input Power Specifications further details. All available VCC pins on the connector
VCC_5V_SBY	B24, G01	Power	3.3V Suspend / 3.3V			Standby power input: +5.0V nominal. Refer to Section 8 Module Input Power Specifications for further details. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design. Two pin are defined.
VCC_RTC	A86	Power	3.3V Suspend / 3.3V	VBAT_BTB		Real-time clock circuit-power input. Nominally +3.0V. Refer to Section 8 Module Input Power Specifications for details.
GND		GND	3.3V Suspend / 3.3V	GND		Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane(s).

▶ Cooling Option

Heat Sink

The COM HPC connector is used to interface the RPS9HC COM HPC board to a carrier board. Connect the COM HPC connector (located on the solder side of the board) to the COM HPD connector on the carrier board.

Top View of the Heat Sink

Bottom View of the Heat Sink

Important:
Remove the plastic covering from the thermal pads prior to mounting the heat sink onto board.

▶ Installing RPS9HC onto a Carrier Board

1. Grasp RPS9HC by its edges and position it on top of the carrier board with its COM HPC Express connectors aligned with the COM HPC connector on the carrier board. This will also help align the mountings holes of RPS9HC with the standoffs on the carrier board.

Important:
The carrier board (COM836) used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install RPS9HC onto the carrier board of your choice. .
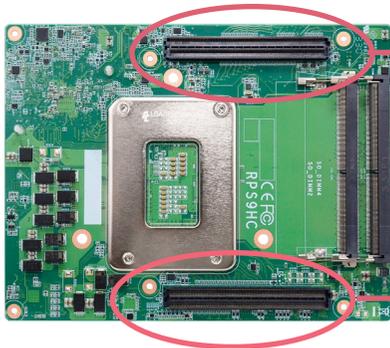
COM HPC connectors
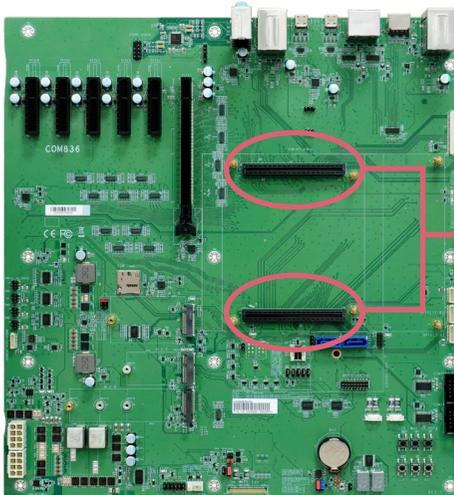
COM HPC connectors on the carrier board

2. Align the mounting holes of the heatsink with the mounting holes of the module. Use the
    provided mounting screws to install the heat sink onto the module.

Chapter 4 - BIOS Setup

Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.

It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

> **Note:**
> The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.
The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message Press DEL to run setup will appear on the screen. If the message disappears before you respond, restart the system or press the Reset button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

Legends

KEYs	Function
Right and Left Arrows	Moves the highlight left or right to select a menu.
Up and Down Arrows	Moves the highlight up or down between submenus or fields.
<Esc>	Exits to the BIOS setup utility
+ (plus key)	Scrolls forward through the values or options of the hightlighted field.
- (minus key)	Scolls backward through the values or options of the hightlighted field.
<F1>	Displays general help
<F2>	Displays previous values
<F9>	Optimized defaults
<F10>	Saves and reset the setup program.
<Enter>	Press <Enter> to enter the highlighted submenu

Scroll Bar

When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu

When ▶ appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

▶ **Main**

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.

```
                          Aptio Setup - AMI
    Main  Advanced  Chipset  Security  Boot  Save & Exit  MEBx

  Project Name              RPS9HC                Set the Date. Use Tab to
  BIOS Version              B248.01A              switch between Date elements.
  EC Version                E247.16A              Default Ranges:
                                                  Year: 1998-2121
  FSP version               0C.00.C6.50           Months: 1-12
  RC version                0C.E0.C6.50           Days: Dependent on month
                                                  Range of Years may vary.
  13th Gen Intel(R) Core(TM) i9-13900TE
  ID                        0xB0671
  Stepping                  B0
  Number of Efficient-cores 16Core(s) / 16Thread(s)
  Number of Performance-cores 8Core(s) / 16Thread(s)
  Microcode Revision        125
                                                  ↔: Select Screen
  Memory RC Version         0.0.4.199             ↑↓: Select Item
  Total Memory              16384 MB              Enter: Select
  Memory Frequency           4000 MHz             +/- : Change Opt.
                                                  F1: General Help
  PCH SKU                   PCH-S R680E           F2: Previous Values
  ME FW Version             16.1.27.2216          F9: Optimized Defaults
  ME Firmware SKU           Corporate SKU         F10: Save & Reset
  PMC FW Version            160.2.0.1041          ESC: Exit

  System Date               [Fri 01/01/2021]
  System Time               [00:01:24]

                Version 2.22.1292 Copyright (C) 2024 AMI
```

System Date

The date format is <month>, <date>, <year>. Press Tab to switch to the next field and press - or + to modify the value.

System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

▶ **Advanced**

The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Important:
Setting incorrect field values may cause the system to malfunction.

```
                          Aptio Setup - AMI
    Main  Advanced  Chipset  Security  Boot  Save & Exit  MEBx

  ▶ CPU Configuration                    CPU Configuration Parameters
  ▶ Power & Performance
  ▶ PCH-FW Configuration
  ▶ Trusted Computing
  ▶ IT5782 Super IO Configuration
  ▶ Serial Port Console Redirection
  ▶ ACPI Settings
  ▶ Network Stack Configuration
  ▶ NVMe Configuration
  ▶ DFI EC HW Monitor
  ▶ DFI WDT Configuration

  ▶ Tls Auth Configuration
                                         ↔: Select Screen
                                         ↑↓: Select Item
                                         Enter: Select
                                         +/- : Change Opt.
                                         F1: General Help
                                         F2: Previous Values
                                         F9: Optimized Defaults
                                         F10: Save & Reset
                                         ESC: Exit

                Version 2.22.1292 Copyright (C) 2024 AMI
```

▶ **Advanced**

CPU Configuration

▶ **Advanced**

Power & Performance

```
                    Aptio Setup - AMI
 Advanced

 CPU Configuration                             When enabled, a VMM can
                                               utilize the additional
 Intel (VMX) Virtualization    [Enabled]       hardware capabilities provided
 Technology                                    by Vanderpool Technology.
 Hyper-Threading               [Enabled]
 AES                           [Enabled]




                                               →←: Select Screen
                                               ↑↓: Select Item
                                               Enter: Select
                                               +/- : Change Opt.
                                               F1: General Help
                                               F2: Previous Values
                                               F9: Optimized Defaults
                                               F10: Save & Reset
                                               ESC: Exit


              Version 2.22.1292 Copyright (C) 2024 AMI
```

```
                    Aptio Setup - AMI
 Advanced

 Power & Performance                           CPU - Power Management Control
                                               Options
 ▶ CPU - Power Management Control
 ▶ GT - Power Management Control




                                               →←: Select Screen
                                               ↑↓: Select Item
                                               Enter: Select
                                               +/- : Change Opt.
                                               F1: General Help
                                               F2: Previous Values
                                               F9: Optimized Defaults
                                               F10: Save & Reset
                                               ESC: Exit


              Version 2.22.1292 Copyright (C) 2024 AMI
```

Intel (VMX) Virtualization Technology

When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Hyper-threading

Enables this field for Windows XP and Linux which are optimized for Hyper-Threading technology. Select disabled for other OSes not optimized for Hyper-Threading technology. When disabled, only one thread per enabled core is enabled.

AES

Enable/Disable AES (Advanced Encryption Standard)

▶ **Advanced**

Power & Performance ▶ **CPU- Power Management Control**

```
                              Aptio Setup - AMI
       Advanced

    CPU - Power Management Control                     Enable/Disable processor Turbo
                                                       Mode (requires EMTTM enabled
      Turbo Mode                    [Enabled]          too). AUTO means enabled.
    ▶ Configure Turbo Options
      C states                      [Disabled]




                                                       ↔: Select Screen
                                                       ↑↓: Select Item
                                                       Enter: Select
                                                       +/- : Change Opt.
                                                       F1: General Help
                                                       F2: Previous Values
                                                       F9: Optimized Defaults
                                                       F10: Save & Reset
                                                       ESC: Exit


                    Version 2.22.1292 Copyright (C) 2024 AMI
```
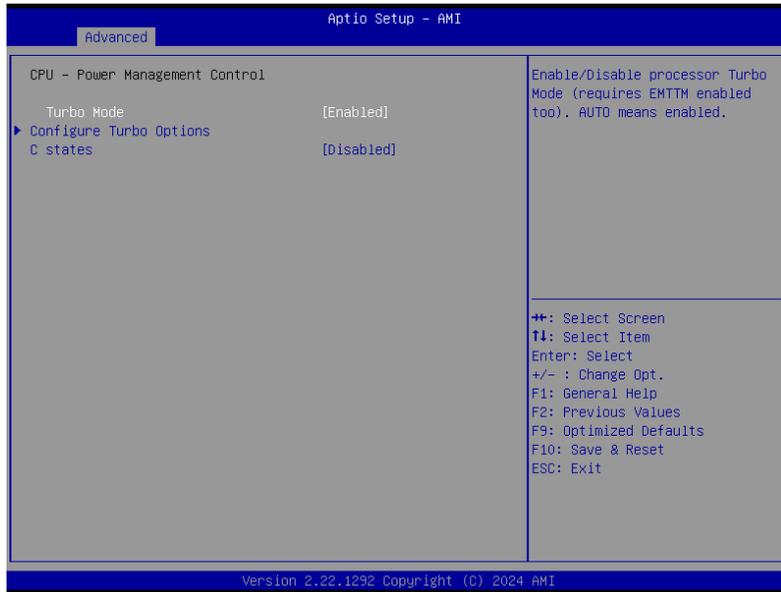
Turbo Mode

Enable or disable turbo mode of the processor. This field will only be displayed when EIST is enabled.

C states

Enable or disable CPU Power Management. It allows CPU to enter C states when it's not 100% utilized.

▶ **Advanced**

Power & Performance ▶ **GT- Power Management Control**

```
                              Aptio Setup - AMI
       Advanced

    GT - Power Management Control                      Check to enable render standby
                                                       support.
    RC6(Render Standby)             [Enabled]




                                                       ↔: Select Screen
                                                       ↑↓: Select Item
                                                       Enter: Select
                                                       +/- : Change Opt.
                                                       F1: General Help
                                                       F2: Previous Values
                                                       F9: Optimized Defaults
                                                       F10: Save & Reset
                                                       ESC: Exit


                    Version 2.22.1292 Copyright (C) 2024 AMI
```

RC6 (Render Standby)
Check to enable render standby support.

▶ **Advanced**

PCH-FW Configuration

```
                            Aptio Setup – AMI
       Advanced

    ME State                        [Enabled]        When Disabled ME will be put
    Manageability Features State    [Enabled]        into ME Temporarily Disabled
    AMT BIOS Features               [Enabled]        Mode.
    ME Unconfig on RTC Clear        [Enabled]

  ▶ Firmware Update Configuration




                                                     →←: Select Screen
                                                     ↑↓: Select Item
                                                     Enter: Select
                                                     +/- : Change Opt.
                                                     F1: General Help
                                                     F2: Previous Values
                                                     F9: Optimized Defaults
                                                     F10: Save & Reset
                                                     ESC: Exit


                    Version 2.22.1292 Copyright (C) 2024 AMI
```

ME State
Enable or disable Management Engine. When this field is set to Disabled, ME will be put into ME Temporarily Disabled Mode. The following fields will only appear when ME State is enabled.

Manageability Features State
Enable or disable Intel(R) Manageability features. This option disables/enables Manageability Features support in FW. To disable, support platform must be in an unprovisioned state first.

AMT BIOS Features
When disabled, AMT BIOS features are no longer supported and user is no longer able to access MEBx Setup. This option does not disable manageability features in FW.

AMT Configuration
This section is used to configure Intel(R) Active Management Technology Parameters. Please refer to the following pages.

ME Unconfig on RTC Clear
When disabled, ME will not be unconfigured on RTC Clear.

Firmware Update Configuration
Please refer to the following pages.

▶ **Advanced**

Trusted Computing

```
                            Aptio Setup – AMI
       Advanced

    TPM 2.0 Device Found                             Enables or Disables BIOS
    Firmware Version:               7.85             support for security device.
    Vendor:                         IFX             O.S. will not show Security
                                                     Device. TCG EFI protocol and
    Security Device Support         [Enable]         INT1A interface will not be
    Active PCR banks                SHA256           available.
    Available PCR banks             SHA256


    Pending operation               [None]




                                                     →←: Select Screen
                                                     ↑↓: Select Item
                                                     Enter: Select
                                                     +/- : Change Opt.
                                                     F1: General Help
                                                     F2: Previous Values
                                                     F9: Optimized Defaults
                                                     F10: Save & Reset
                                                     ESC: Exit


                    Version 2.22.1292 Copyright (C) 2024 AMI
```

Security Device Support

This field is used to enable or disable BIOS support for the security device such as an TPM 2.0 to achieve hardware-level security via cryptographic keys. TCG EFI protocol and INT1A interface will not be available.

Pending operation

To clear the existing TPM encryption, select TPM Clear and restart the system. This field is not available when Security Device Support is disabled. Schedule an Operation for the security Device. NOTE: Your computer will reboot during restart in order to change State of Security Device.

▶ **Advanced**

IT5782 Super IO Configuration

```
                        Aptio Setup - AMI
      Advanced

      IT5782 Super IO Configuration          Set Parameters of Serial Port
                                             1 (COMA)
      Super IO Chip              IT5782
    ▶ Serial Port 1 Configuration
    ▶ Serial Port 2 Configuration




                                             →←: Select Screen
                                             ↑↓: Select Item
                                             Enter: Select
                                             +/- : Change Opt.
                                             F1: General Help
                                             F2: Previous Values
                                             F9: Optimized Defaults
                                             F10: Save & Reset
                                             ESC: Exit


                Version 2.22.1292 Copyright (C) 2024 AMI
```
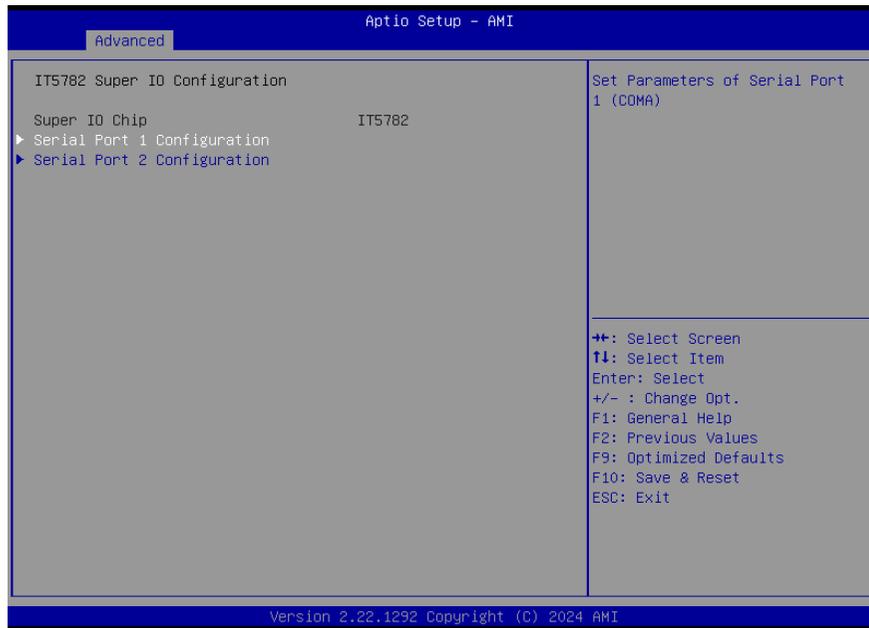
Serial Port 1 Configuration

Set Parameters of Serial Port 1 (COMA)

Serial Port 2 Configuration

Set Parameters of Serial Port 2 (COMB)

Note:
The sub-menus are detailed in following sections.

▶ **Advanced**

IT5782 Super IO Configuration ▶ **Serial Port 1, 2 Configuration**

```
                        Aptio Setup - AMI
      Advanced

    Serial Port 1 Configuration             Enable or Disable Serial Port
                                            (COM)
    Serial Port              [Enabled]
    Device Settings          IO=3F8h; IRQ=4;

    Change Settings          [Auto]



                                            →←: Select Screen
                                            ↑↓: Select Item
                                            Enter: Select
                                            +/- : Change Opt.
                                            F1: General Help
                                            F2: Previous Values
                                            F9: Optimized Defaults
                                            F10: Save & Reset
                                            ESC: Exit

                Version 2.22.1292 Copyright (C) 2024 AMI
```

```
                        Aptio Setup - AMI
      Advanced

    Serial Port 2 Configuration             Enable or Disable Serial Port
                                            (COM)
    Serial Port              [Enabled]
    Device Settings          IO=2F8h; IRQ=3;

    Change Settings          [Auto]



                                            →←: Select Screen
                                            ↑↓: Select Item
                                            Enter: Select
                                            +/- : Change Opt.
                                            F1: General Help
                                            F2: Previous Values
                                            F9: Optimized Defaults
                                            F10: Save & Reset
                                            ESC: Exit

                Version 2.22.1292 Copyright (C) 2024 AMI
```

Serial Port
Enable or disable serial port.

Change Settings
Select an optimal settings for Super IO Device.

▶ **Advanced**

Serial Port Console Redirection

```
                              Aptio Setup - AMI
        Advanced

    COM1                                          Console Redirection Enable or
    Console Redirection            [Disabled]     Disable.
  ▶ Console Redirection Settings

    COM2
    Console Redirection            [Disabled]
  ▶ Console Redirection Settings




                                                  →←: Select Screen
                                                  ↑↓: Select Item
                                                  Enter: Select
                                                  +/- : Change Opt.
                                                  F1: General Help
                                                  F2: Previous Values
                                                  F9: Optimized Defaults
                                                  F10: Save & Reset
                                                  ESC: Exit



                     Version 2.22.1292 Copyright (C) 2024 AMI
```
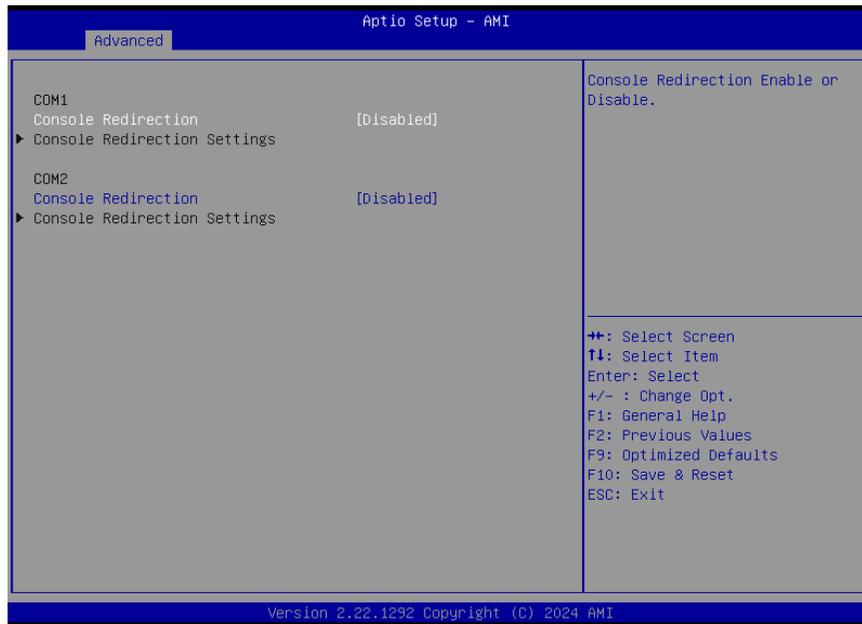
Console Redirection

By enabling Console Redirection of a COM port, the sub-menu of console redirection settings will become available for configuration as detailed in the following.

▶ **Advanced**

Serial Port Console Redirection ▶ Console Redirection Settings

```
                          Aptio Setup - AMI
    ┌──────────────────────────────────────────────────────────────────┐
    │ Advanced                                                          │
    ├──────────────────────────────────────────────────────────────────┤
    │ COM1                                    Emulation: ANSI: Extended  │
    │ Console Redirection Settings            ASCII char set. VT100: ASCII│
    │                                         char set. VT100Plus: Extends│
    │ Terminal Type              [VT100Plus]  VT100 to support color,    │
    │ Bits per second            [115200]     function keys, etc. VT-UTF8:│
    │ Data Bits                  [8]          Uses UTF8 encoding to map  │
    │ Parity                     [None]       Unicode chars onto 1 or more│
    │ Stop Bits                  [1]          bytes.                     │
    │ Flow Control               [None]                                 │
    │ VT-UTF8 Combo Key Support  [Enabled]                              │
    │ Recorder Mode              [Disabled]                             │
    │ Resolution 100x31          [Enabled]                             │
    │ Putty KeyPad               [VT100]      ┌──────────────────────┐  │
    │                                         │ →←: Select Screen     │  │
    │                                         │ ↑↓: Select Item       │  │
    │                                         │ Enter: Select         │  │
    │                                         │ +/- : Change Opt.     │  │
    │                                         │ F1: General Help      │  │
    │                                         │ F2: Previous Values   │  │
    │                                         │ F9: Optimized Defaults │  │
    │                                         │ F10: Save & Reset     │  │
    │                                         │ ESC: Exit             │  │
    │                                         └──────────────────────┘  │
    ├──────────────────────────────────────────────────────────────────┤
    │              Version 2.22.1292 Copyright (C) 2024 AMI              │
    └──────────────────────────────────────────────────────────────────┘
```

```
                          Aptio Setup - AMI
    ┌──────────────────────────────────────────────────────────────────┐
    │ Advanced                                                          │
    ├──────────────────────────────────────────────────────────────────┤
    │ COM2                                    Emulation: ANSI: Extended  │
    │ Console Redirection Settings            ASCII char set. VT100: ASCII│
    │                                         char set. VT100Plus: Extends│
    │ Terminal Type              [VT100Plus]  VT100 to support color,    │
    │ Bits per second            [115200]     function keys, etc. VT-UTF8:│
    │ Data Bits                  [8]          Uses UTF8 encoding to map  │
    │ Parity                     [None]       Unicode chars onto 1 or more│
    │ Stop Bits                  [1]          bytes.                     │
    │ Flow Control               [None]                                 │
    │ VT-UTF8 Combo Key Support  [Enabled]                              │
    │ Recorder Mode              [Disabled]                             │
    │ Resolution 100x31          [Enabled]                             │
    │ Putty KeyPad               [VT100]      ┌──────────────────────┐  │
    │                                         │ →←: Select Screen     │  │
    │                                         │ ↑↓: Select Item       │  │
    │                                         │ Enter: Select         │  │
    │                                         │ +/- : Change Opt.     │  │
    │                                         │ F1: General Help      │  │
    │                                         │ F2: Previous Values   │  │
    │                                         │ F9: Optimized Defaults │  │
    │                                         │ F10: Save & Reset     │  │
    │                                         │ ESC: Exit             │  │
    │                                         └──────────────────────┘  │
    ├──────────────────────────────────────────────────────────────────┤
    │              Version 2.22.1292 Copyright (C) 2024 AMI              │
    └──────────────────────────────────────────────────────────────────┘
```

Configure the serial settings of the current COM port.

Terminal Type

Select terminal type: VT100, VT100+, VT-UTF8 or ANSI.

Bits per second

Select serial port transmission speed: 9600, 19200, 38400, 57600 or 115200.

Data Bits

Select data bits: 7 bits or 8 bits.

Parity

Select parity bits: None, Even, Odd, Mark or Space.

Stop Bits

Select stop bits: 1 bit or 2 bits.

Flow Control

Select flow control type: None or Hardware RTS/CTS. Flow Control is for RS485 mode and is only supported by Serial Port 1 (COM1).

VT-UTF8 Combo Key Support

Enable or disable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.

Recorder Mode

With this mode enabled only text will be sent. This is to capture Terminal data.

Resolution 100x31

Enables or disables extended terminal resolution.

Putty Keypad

Select FunctionKey and KeyPad on Putty.

- VT100
- LINUX
- XTERMR6
- SCO
- ESCN
- VT400

▶ **Advanced**

ACPI Settings

```
                              Aptio Setup - AMI
        Advanced

ACPI Settings                                    Enable or disable System wake
                                                 on alarm event. When enabled,
Wake System from S5 via RTC        [Disabled]    System will wake on the
State After G3                     [S0 State]    hr::min::sec specified




                                                 →←: Select Screen
                                                 ↑↓: Select Item
                                                 Enter: Select
                                                 +/- : Change Opt.
                                                 F1: General Help
                                                 F2: Previous Values
                                                 F9: Optimized Defaults
                                                 F10: Save & Reset
                                                 ESC: Exit



                        Version 2.22.1292 Copyright (C) 2024 AMI
```
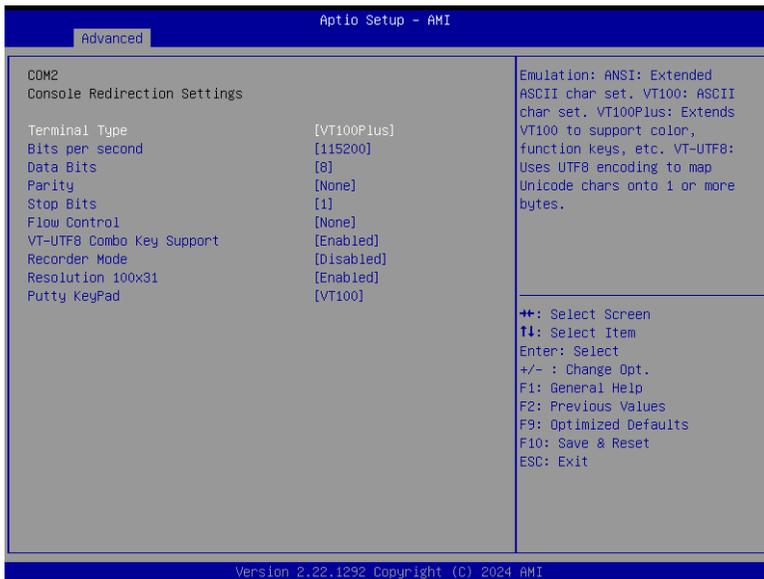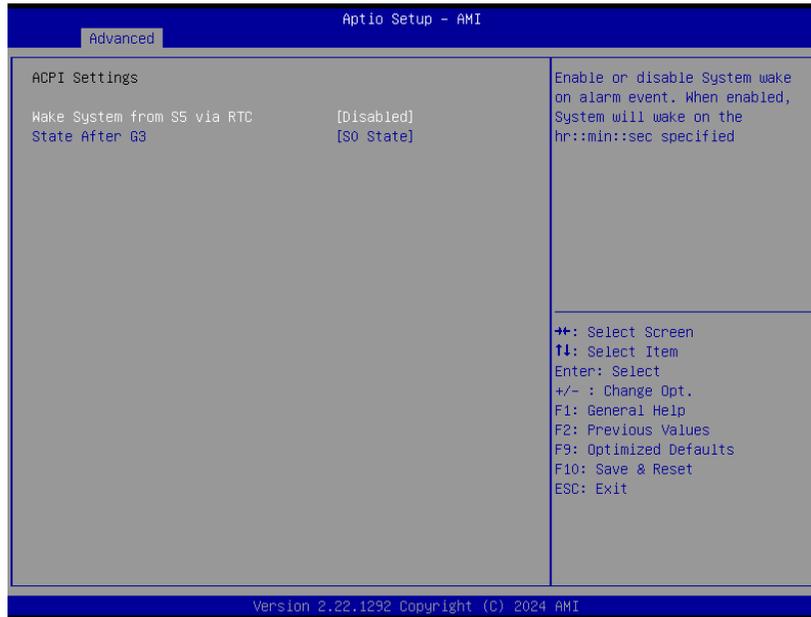
Wake system from S5 via RTC

When Enabled, the system will automatically power up at a designated time every day. Once it's switched to [Enabled], please set up the time of day — hour, minute, and second — for the system to wake up.

State After G3

Select between S0 State, and S5 State. This field is used to specify what state the system

is set to return to when power is re-applied after a power failure (G3 state).

• **S0 State**   The system automatically powers on after power failure.

• **S5 State**   The system enter soft-off state after power failure. Power-on signal input is required to power up the system.

• **Last State**   The system returns to the last state right before power failure.

▶ **Advanced**

Network Stack Configuration

```
                              Aptio Setup - AMI
        Advanced

    Network Stack                    [Enabled]         Enable/Disable UEFI Network
    IPv4 PXE Support                 [Disabled]        Stack
    IPv4 HTTP Support                [Disabled]
    IPv6 PXE Support                 [Disabled]
    IPv6 HTTP Support                [Disabled]
    PXE boot wait time               0
    Media detect count               1




                                                      →←: Select Screen
                                                      ↑↓: Select Item
                                                      Enter: Select
                                                      +/- : Change Opt.
                                                      F1: General Help
                                                      F2: Previous Values
                                                      F9: Optimized Defaults
                                                      F10: Save & Reset
                                                      ESC: Exit




                     Version 2.22.1292 Copyright (C) 2024 AMI
```

Network Stack

Enable or disable UEFI network stack. The following fields will appear when this field is en-abled.

Ipv4 PXE Support

Enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be avail-able.

Ipv4 HTTP Support

Enable or disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be avail-able.

Ipv6 PXE Support

Enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be avail-able.

Ipv6 HTTP Support

Enable or disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be avail-able.

PXE boot wait time

Set the wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

Media detect count

Set the number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

▶ **Advanced**

NVMe Configuration

```
                        Aptio Setup - AMI
    Advanced

    NVMe Configuration

    No NVME Device Found

                                              ↔: Select Screen
                                              ↑↓: Select Item
                                              Enter: Select
                                              +/- : Change Opt.
                                              F1: General Help
                                              F2: Previous Values
                                              F9: Optimized Defaults
                                              F10: Save & Reset
                                              ESC: Exit

                Version 2.22.1292 Copyright (C) 2024 AMI
```
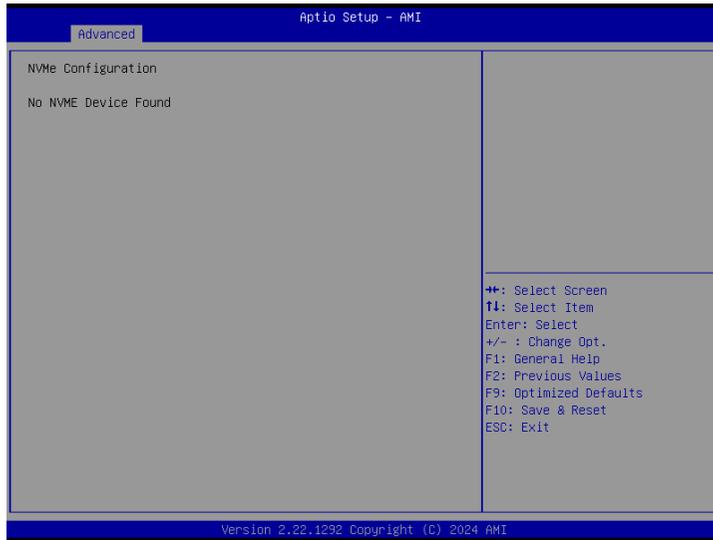
NVMe Configuration

NVMe Device Options Settings

▶ **Advanced**

DFI EC HW Monitor

```
                        Aptio Setup - AMI
    Advanced

    Pc Health Status                          Smart Fan function setting

  ▶ Smart Fan Function

    Case Open                 [Disabled]

    CPU Temperature           : +62 %
    CPU FAN Speed             : 3957 RPM
    VBAT                      : +2.908 V
    VCore                     : +1.162 V
    VDDQ                      : +1.097 V
    3.3V                      : +3.317 V
    +12V                      : +11.884 V
                                              ↔: Select Screen
                                              ↑↓: Select Item
                                              Enter: Select
                                              +/- : Change Opt.
                                              F1: General Help
                                              F2: Previous Values
                                              F9: Optimized Defaults
                                              F10: Save & Reset
                                              ESC: Exit

                Version 2.22.1292 Copyright (C) 2024 AMI
```
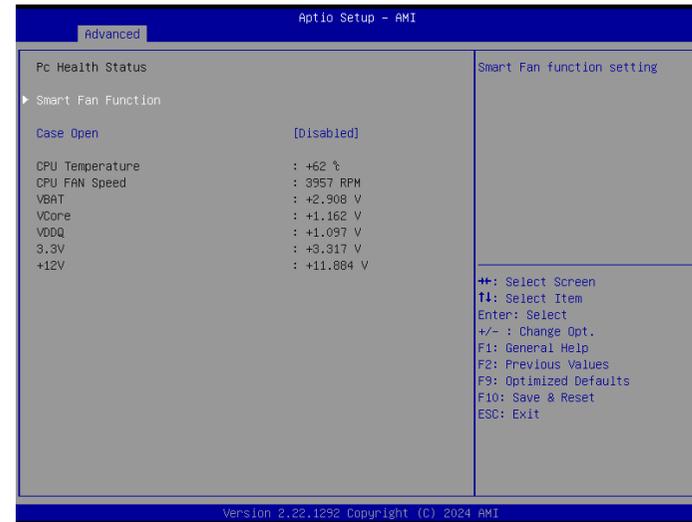
▶ **Advanced**

DFI EC HW Monitor ▶ Smart Fan Function

```
                              Aptio Setup - AMI
      Advanced

    Smart Fan Function                                     CPU Smart Fan Mode Select

      CPU Smart Fan Mode              [Smart Fan]
        Boundary 1                    30
        Boundary 2                    40
        Boundary 3                    50
        Boundary 4                    60
        Speed Count 1                 35
        Speed Count 2                 60
        Speed Count 3                 80
        Speed Count 4                 100

                                                        →←: Select Screen
                                                        ↑↓: Select Item
                                                        Enter: Select
                                                        +/- : Change Opt.
                                                        F1: General Help
                                                        F2: Previous Values
                                                        F9: Optimized Defaults
                                                        F10: Save & Reset
                                                        ESC: Exit

                     Version 2.22.1292 Copyright (C) 2024 AMI
```

Smart Fan is a fan speed moderation strategy dependent on the current system temperature. When the system temperature goes higher than the Boundary setting, the fan speed will be turned up to the setting of the Fan Speed Count that bears the same index as the Boundary field.

▼ **CPU Smart Fan Mode = [Smart Fan]**

Boundary 1 to Boundary 4

Set the boundary temperatures that determine the fan speeds accordingly, the value ranging from 0-127℃. For example, when the system temperature reaches Boundary 1 setting, the fan speed will be turned up to the designated speed of the Fan Speed Count 1 field.

Fan Speed Count 1 to Fan Speed Count 4

Set the fan speed, the value ranging from 1-100%, 100% being full speed. The fans will operate according to the specified boundary temperatures above-mentioned.

▶ **Advanced**

DFI WDT Configuration

```
                              Aptio Setup - AMI
      Advanced

    DFI WDT Configuration                                  Enable/Disable Watchdog Timer

    Watchdog Timer                   [Enabled]
      Output Options                 [Mode1]
      Enable Delay                   300
      Timeout Delay                  150

                                                        →←: Select Screen
                                                        ↑↓: Select Item
                                                        Enter: Select
                                                        +/- : Change Opt.
                                                        F1: General Help
                                                        F2: Previous Values
                                                        F9: Optimized Defaults
                                                        F10: Save & Reset
                                                        ESC: Exit

                     Version 2.22.1292 Copyright (C) 2024 AMI
```
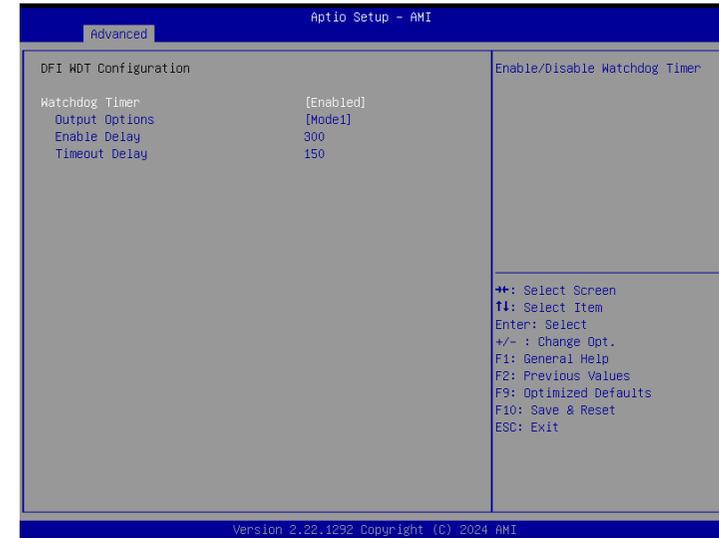
Watchdog Timer

Enable or disable watchdog timer.

Output Options

Mode1 = A Watchdog timeout causes the system to be reset.
Mode2 = WDT pin goes high upon timeout of the watchdog timer.
Mode3 = Generate NMI upon timeout of the watchdog timer.

Enable Delay

The enable delay allows time for the OS to boot and the application to load and initialize. The unit is 1 sec.

Timeout Delay

The timeout delay allows time for period of the watchdog timer. The unit is 0.1 sec.

▶ **Advanced**

Tls Auth Configuration

```
                        Aptio Setup - AMI
        Advanced

▶ Server CA Configuration                    Press <Enter> to configure
                                             Server CA.
▶ Client Cert Configuration




                                             ↔: Select Screen
                                             ↑↓: Select Item
                                             Enter: Select
                                             +/- : Change Opt.
                                             F1: General Help
                                             F2: Previous Values
                                             F9: Optimized Defaults
                                             F10: Save & Reset
                                             ESC: Exit


              Version 2.22.1292 Copyright (C) 2024 AMI
```
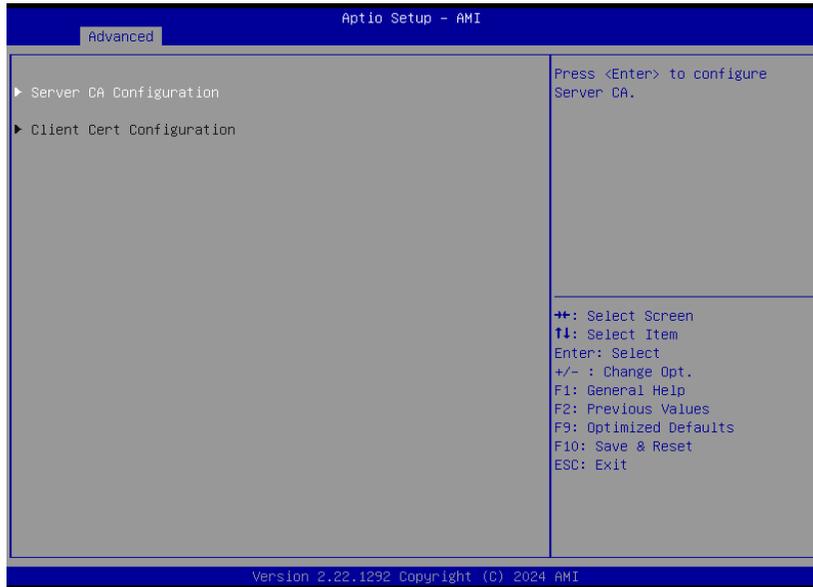
Server CA Configuration

Press <Enter> to configure Server CA.

▶ **Chipset**
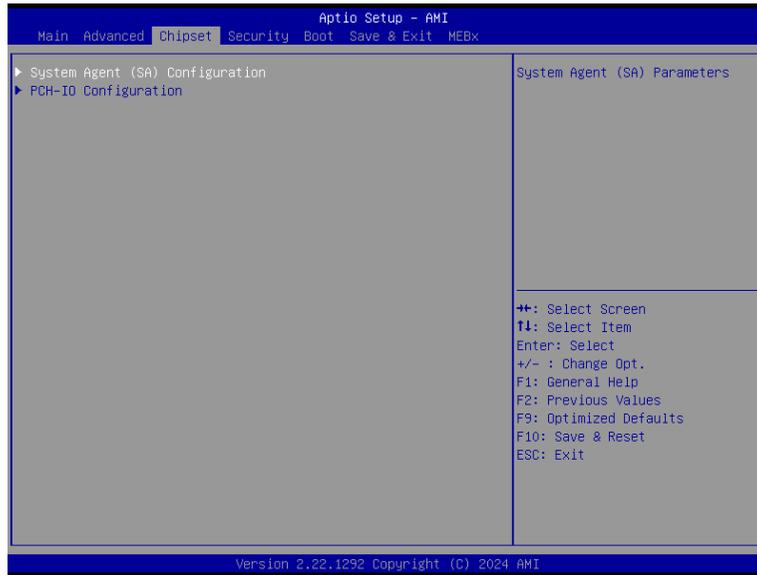
Please select a submenu and press Enter. The submenus are detailed in the following pages.

▶ Chipset

System Agnet (SA) Configuration
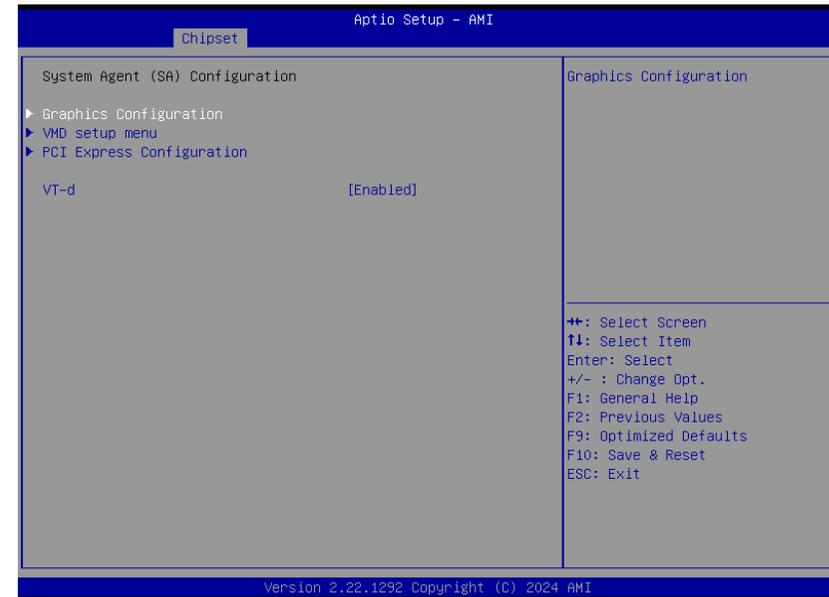
Graphics Configuration
Settings about graphic.

VMD setup menu
VMD Configuration Settings

PCI Express Configuration :

VT-d
VT-d capability.

PCH-IO Configuration

```
                          Aptio Setup - AMI
      ┌─────────┐
      │ Chipset │
      └─────────┘
  PCH-IO Configuration                        PCI Express Configuration
                                              settings
▶ PCI Express Configuration
▶ SATA Configuration
▶ HD Audio Configuration




                                              →←: Select Screen
                                              ↑↓: Select Item
                                              Enter: Select
                                              +/- : Change Opt.
                                              F1: General Help
                                              F2: Previous Values
                                              F9: Optimized Defaults
                                              F10: Save & Reset
                                              ESC: Exit



              Version 2.22.1292 Copyright (C) 2024 AMI
```
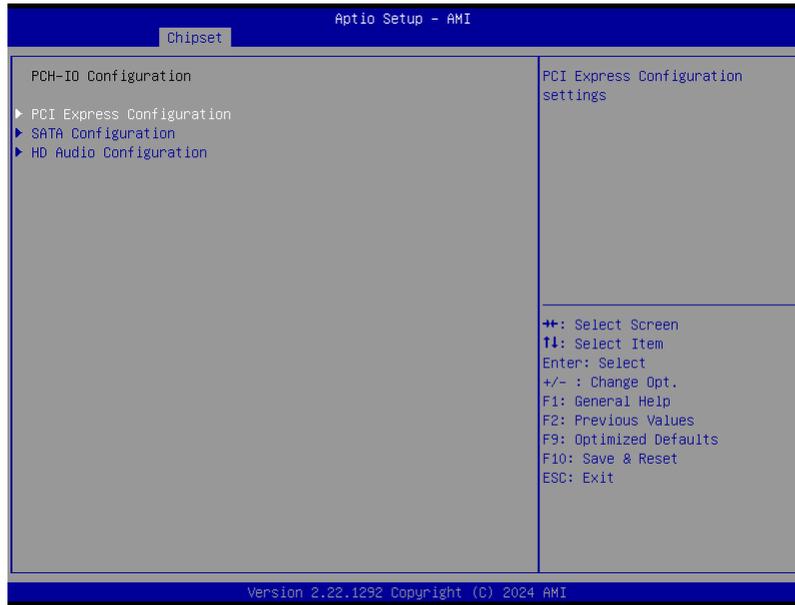
PCI Express Configuration

PCI Express Configuration Settings

SATA And RST Configuration

SATA Device Otpions Settings

HD Audio Configuration

HD Audio Subsystem Configuration Settings

PCH-IO Configuration▶ **PCI Express Configuration**

```
                          Aptio Setup - AMI
      ┌─────────┐
      │ Chipset │
      └─────────┘
  PCI Express Configuration                    PCI Express Root Port Settings.

▶ PCI Express Root Port 1
▶ PCI Express Root Port 2
▶ Onboard LAN 1
▶ Onboard LAN 2
▶ PCI Express Root Port 5
▶ PCI Express Root Port 9
▶ PCI Express Root Port 13
▶ PCI Express Root Port 21
▶ PCI Express Root Port 25


                                              →←: Select Screen
                                              ↑↓: Select Item
                                              Enter: Select
                                              +/- : Change Opt.
                                              F1: General Help
                                              F2: Previous Values
                                              F9: Optimized Defaults
                                              F10: Save & Reset
                                              ESC: Exit


              Version 2.22.1292 Copyright (C) 2024 AMI
```
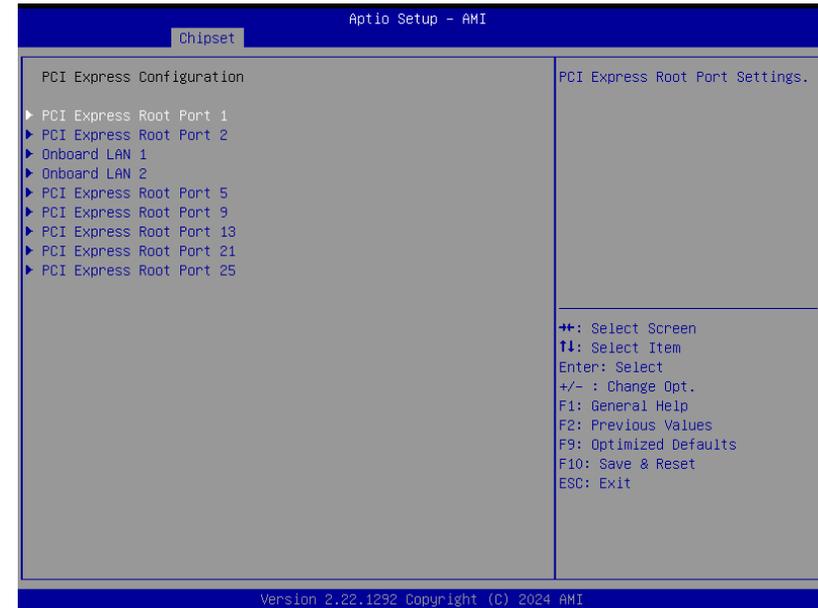
Select one of the PCI Express channels and press enter to configure the following settings.

PCI Express Root Port 1, 2, 5, 9, 13, 21, 25, Onboard LAN1&2

Control the PCI Express Root Port.

▶ **Chipset**

PCH-IO Configuration▶ SATA Configuration

```
                          Aptio Setup - AMI
          Chipset

    SATA Configuration                               Enable/Disable SATA Device.

    SATA Controller(s)          [Enabled]
    SATA Speed                  [Auto]

    Serial ATA Port 1           Empty
      Port 4                    [Enabled]
    Serial ATA Port 2           Empty
      Port 5                    [Enabled]

                                                 →←: Select Screen
                                                 ↑↓: Select Item
                                                 Enter: Select
                                                 +/- : Change Opt.
                                                 F1: General Help
                                                 F2: Previous Values
                                                 F9: Optimized Defaults
                                                 F10: Save & Reset
                                                 ESC: Exit

                    Version 2.22.1292 Copyright (C) 2024 AMI
```
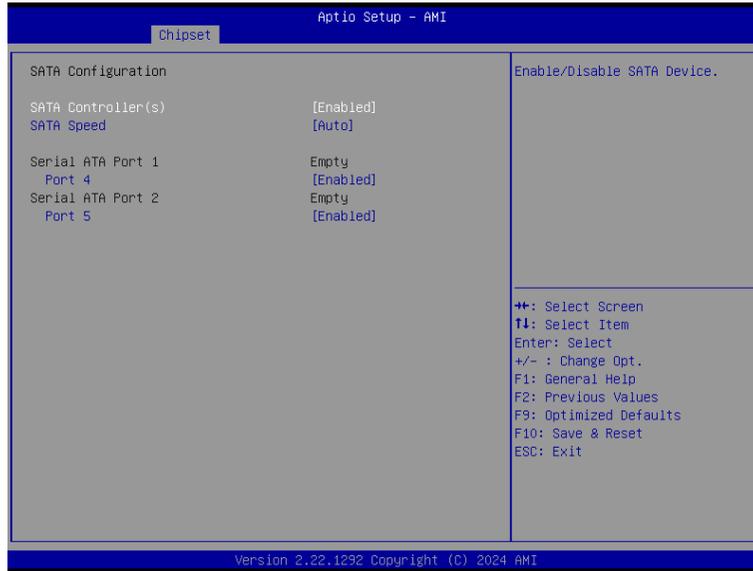
SATA Controller(s)

This field is used to enable or disable the Serial ATA controller.

SATA Speed

This field is used to select SATA speed generation limit: Auto, Gen1, Gen2 or Gen3.

▶ **Chipset**

PCH-IO Configuration▶ HD Audio Configuration

```
                          Aptio Setup - AMI
          Chipset

    HD Audio Subsystem Configuration Settings        Control Detection of the
                                                     HD-Audio device.
    HD Audio                    [Enabled]            Disabled = HDA will be
                                                     unconditionally disabled
                                                     Enabled = HDA will be
                                                     unconditionally enabled.

                                                 →←: Select Screen
                                                 ↑↓: Select Item
                                                 Enter: Select
                                                 +/- : Change Opt.
                                                 F1: General Help
                                                 F2: Previous Values
                                                 F9: Optimized Defaults
                                                 F10: Save & Reset
                                                 ESC: Exit

                    Version 2.22.1292 Copyright (C) 2024 AMI
```
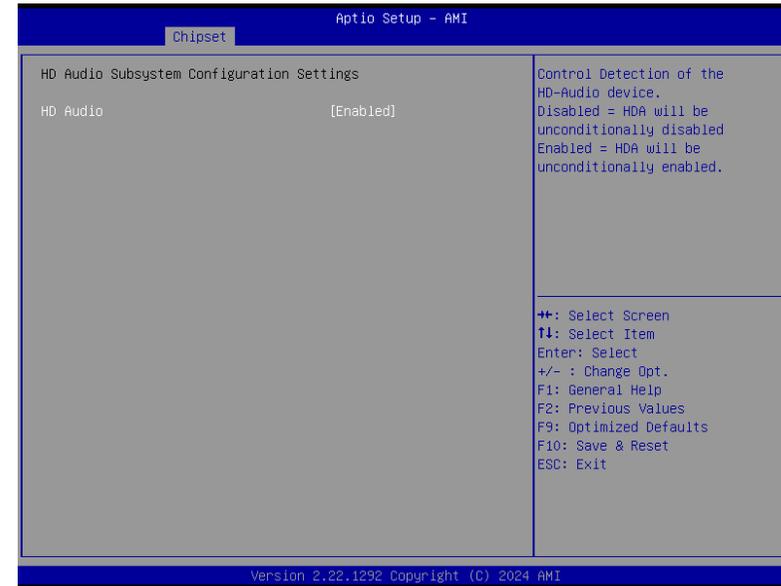
HD Audio

Control the detection of the HD Audio device.

- **Disabled** HDA will be unconditionally disabled.

- **Enabled** HDA will be unconditionally enabled.

▶ **Security**

Secure Boot
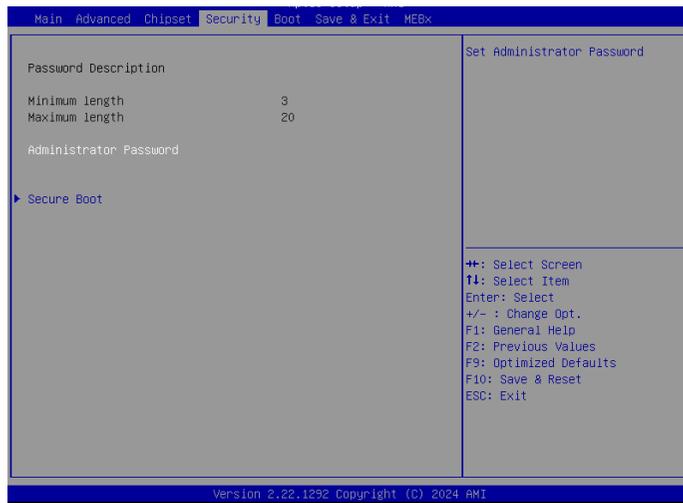
Administrator Password

Set the administrator password. To clear the password, input nothing and press enter when a new password is asked. Administrator Password will be required when entering the BIOS.

User Password

Set the user password. To clear the password, input nothing and press enter when a new password is asked. User Password will be required when powering up the system.

Secure Boot

The Secure Boot store a database of certificates in the firmware and only allows the OSes with authorized signatures to boot on the system. To activate Secure Boot, please make sure that Secure Boot is [Enabled], Platform Key (PK) is enrolled, System Mode is User, and CSM is disabled. After enabling/disabling Secure Boot, please save the configuration and restart the system. When configured and activated correctly, the Secure Boot status will be Active.

Secure Boot Mode

Select the secure boot mode — Standard or Custom. When set to Custom, the following fields will be configurable for the user to manually modify the key database.

Restore Factory Keys

Force system to User Mode. Load OEM-defined factory defaults of keys and databases onto the Secure Boot. Press Enter and a prompt will show up for you to confirm.

Reset To Setup Mode

Clear the database from the NVRAM, including all the keys and signatures installed in the Key Management menu. Press Enter and a prompt will show up for you to confirm.

Key Management

Enables expert users to modify Secure Boot Policy variables

without full authentication.

▶ **Boot**

```
                          Aptio Setup - AMI
     Main  Advanced  Chipset  Security  Boot  Save & Exit  MEBx

  Boot Configuration                              Number of seconds to wait for
  Setup Prompt Timeout             1              setup activation key.
  Bootup NumLock State             [On]           65535(0xFFFF) means indefinite
  Quiet Boot                       [Disabled]     waiting.

  Boot Option Priorities
  Boot Option #1                   [UEFI: Generic Flash
                                   Disk 8.07, Partition 1
                                   (Generic Flash Disk
                                   8.07)]

                                                  →←: Select Screen
                                                  ↑↓: Select Item
                                                  Enter: Select
                                                  +/- : Change Opt.
                                                  F1: General Help
                                                  F2: Previous Values
                                                  F9: Optimized Defaults
                                                  F10: Save & Reset
                                                  ESC: Exit

              Version 2.22.1292 Copyright (C) 2024 AMI
```

Setup Prompt Timeout

Set the number of seconds to wait for the setup activation key. 65535 (0xFFFF) denotes indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state: On or Off.

Quiet Boot

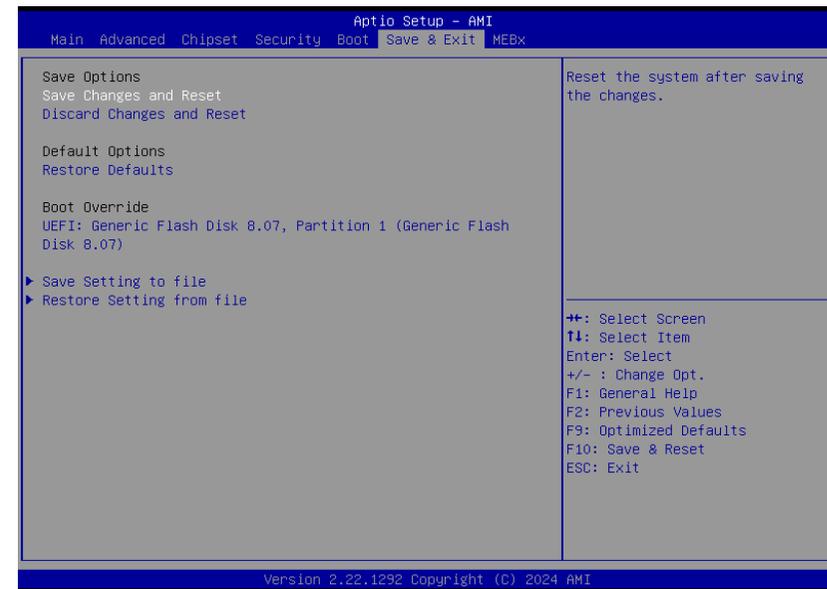This section is used to enable or disable quiet boot option.

Boot Option Priorities

Rearrange the system boot order of available boot devices.

Fast Boot

Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

▶ **Save & Exit**

```
                          Aptio Setup - AMI
     Main  Advanced  Chipset  Security  Boot  Save & Exit  MEBx

  Save Options                                    Reset the system after saving
  Save Changes and Reset                          the changes.
  Discard Changes and Reset

  Default Options
  Restore Defaults

  Boot Override
  UEFI: Generic Flash Disk 8.07, Partition 1 (Generic Flash
  Disk 8.07)

  ▶ Save Setting to file
  ▶ Restore Setting from file

                                                  →←: Select Screen
                                                  ↑↓: Select Item
                                                  Enter: Select
                                                  +/- : Change Opt.
                                                  F1: General Help
                                                  F2: Previous Values
                                                  F9: Optimized Defaults
                                                  F10: Save & Reset
                                                  ESC: Exit

              Version 2.22.1292 Copyright (C) 2024 AMI
```

Save Changes and Reset

To save the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system after saving all changes made.

Discard Changes and Reset

To discard the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system setup without saving any changes.

Restore Defaults

To restore and load the optimized default values, select this field and then press <Enter>. A dia-log box will appear. Select Yes to restore the default values of all the setup options.

Boot Override

Move the cursor to an available boot device and press Enter, and then the system will immediately boot from the selected boot device. The Boot Override function will only be effective for the current boot. The Boot Option Priorities configured in the Boot menu will not be changed.

• **Save Setting to file** Select this option to save BIOS configuration settings to a USB flash device.

• **Restore Setting from file** This field will appear only when a USB flash device is detected. Select this field to restore set-ting from the USB flash device.

▶ **MEBx**

```
                        Aptio Setup - AMI
       Main  Advanced  Chipset  Security  Boot  Save & Exit  MEBx

    Intel(R) ME Password                    MEBx Login












                                        ↔: Select Screen
                                        ↑↓: Select Item
                                        Enter: Select
                                        +/- : Change Opt.
                                        F1: General Help
                                        F2: Previous Values
                                        F9: Optimized Defaults
                                        F10: Save & Reset
                                        ESC: Exit



                 Version 2.22.1292 Copyright (C) 2024 AMI
```

▶ **Updating the BIOS**

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files and specific instructions about how to update BIOS with the flash utility.

▶ **Notice: BIOS SPI ROM**

- 1. The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.

- 2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.

- 3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

> **Note:**
> a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.
>
> b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not.
>
> c. After updating unique MAC Address from manufacturing, NVM will be protected immediately after power cycle.
> Users cannot update NVM or MAC address.