

# Approval Sheet

|                |                                |
|----------------|--------------------------------|
| Customer       |                                |
| Product Number | ACT1GHR72N8G1333S              |
| Module speed   | PC3-10600                      |
| Pin            | 240pin                         |
| Cl-tRCD-tRP    | 9-9-9                          |
| Date           | 15 <sup>th</sup> December 2015 |

Approval by Customer

P/N:

Signature:

Date:

Sales: \_\_\_\_\_ Sr. Technical Manager: John Hsieh



## **ACT1GHR72N8G1333S**

# **1GB DDR3-1333 Registered ECC Module Specification**

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Produced by Innodisk Taiwan.

## Description

ACTICA ACT1GHR72N8G1333S is a high speed 1GB DDR3-1333 Registered ECC. It is designed for mission critical application memory solution. This DIMM includes Error Checking and Correcting (ECC) for maximum reliability. The modules is constructed using 128Mx8 SDRAMs, and is fully compliant with JEDEC specifications. Decoupling capacitors are mounted on the PCB board for better signal integrity. The DIMM feature serial presence detect (SPD) based on a serial EEPROM device using the 2-pin I2C protocol.

## Features

- 240-pin Registered Dual Inline Memory Module (RDIMM)
- Memory Module Organization 128Mx72
- Height: 30 mm
- CL-tRCD-tRP : 9-9-9
- JEDEC standard 1.5V ( $\pm 0.075V$ )
- VDDQ = 1.5V ( $\pm 0.075V$ )
- 8 independent internal bank
- Burst Length: 4, 8(Interleave/nibble sequential)
- Bi-directional Differential Data-Strobe
- On Die Termination (ODT)
- Eight-bit prefetch architecture
- Average Refresh Period 7.8us at lower than a  $T_{CASE}$  85°C, 3.9us at 85°C <  $T_{CASE}$  < 95 °C
- RoHS Compliant

## Address Range

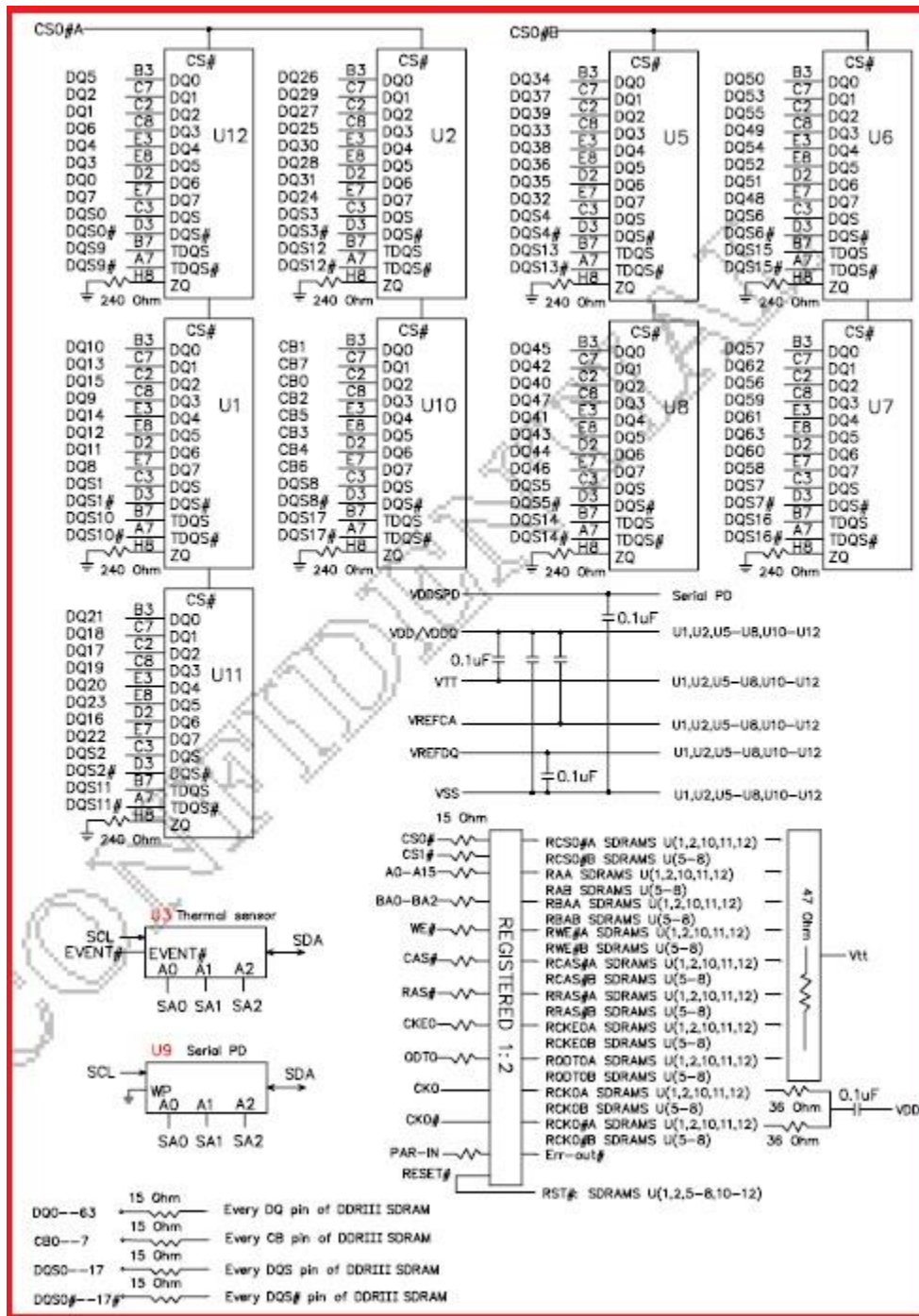
| Module Organization | Row address | Column Address | Bank Address | Auto Precharge |
|---------------------|-------------|----------------|--------------|----------------|
| 128Mx72             | A0-A13      | A0-A9          | BA0-BA2      | A10/AP         |

## Pin Description

| Pin Name                | Description                                                  | Pin Name                            | Description                                           |
|-------------------------|--------------------------------------------------------------|-------------------------------------|-------------------------------------------------------|
| Ck0                     | Clock Input, positive line                                   | Par_In                              | Parity bit for the Address and Control bus            |
| CK0/                    | Clock Input, negative line                                   | Err_Out                             | Parity error found on the Address and Control bus     |
|                         |                                                              | ODT[0]                              | On Die Termination Inputs                             |
|                         |                                                              | DQ[63:0]                            | Data Input/Output                                     |
| CKE[1:0]                | Clock Enables                                                | CB[7:0]                             | Data check bits Input/Output                          |
| TEST                    | Memory bus test toll (Not Connected and Not Usable on DIMMs) | DQS[8:0]                            | Data strobes                                          |
| RAS/                    | Row Address Strobe                                           | DQS/[8:0]                           | Data strobes, negative line                           |
| CAS/                    | Column Address Strobe                                        | DM[8:0]/<br>DQS[17:9]<br>TDQS[17:9] | Data Masks/ Data strobes, Termination data strobes    |
| WE/                     | Write Enable                                                 | DQS/[17:9]<br>TDQS/[17:9]           | Data strobes, negative line, Termination data strobes |
| S[3:0]                  | Chip Selects                                                 | EVENT/                              | Reserved for optional hardware temperature sensing    |
|                         |                                                              | RESET/                              | Register and SDRAM control pin                        |
| A[9:0],A11,<br>A[15:13] | Address Inputs                                               | VDD                                 | Power Supply                                          |
| A10/AP                  | Address Input/Autoprecharge                                  | VSS                                 | Ground                                                |
| A12/BC                  | Address Input/Burst chop                                     | VREFDQ                              | Reference Voltage for DQ                              |
| BA[2:0]                 | SDRAM Bank Addresses                                         | VREFCA                              | Reference Voltage for CA                              |
| SCL                     | Serial Presence Detect (SPD) Clock Input                     | VTT                                 | Termination Voltage                                   |
| SDA                     | SPD Data Input/Output                                        | VDDSPD                              | SPD Power                                             |
| SA[2:0]                 | SPD Address Inputs                                           | RFU                                 | Reserved for Future Use                               |

**Pin Configuration (Front side/Back side)**

| Pin | Front      | Pin | Back                 | Pin | Front           | Pin | Back                    | Pin | Front          | Pin | Back                 | Pin | Front | Pin | Back                 |
|-----|------------|-----|----------------------|-----|-----------------|-----|-------------------------|-----|----------------|-----|----------------------|-----|-------|-----|----------------------|
| 1   | VREFD<br>Q | 121 | VSS                  | 31  | DQ25            | 151 | VSS                     | 60  | VDD            | 180 | A3                   | 91  | DQ41  | 211 | VSS                  |
| 2   | VSS        | 122 | DQ4                  | 32  | VSS             | 152 | DM3,DQS12<br>,TDQS12    | 61  | A2             | 181 | A1                   | 92  | VSS   | 212 | DM5,DQS14<br>,TDQS14 |
| 3   | DQ0        | 123 | DQ5                  | 33  | /DQS3           | 153 | NC,DQS12<br>,TDQS12     | 62  | VDD            | 182 | VDD                  | 93  | /DQS5 | 213 | NC,DQS14<br>,TDQS14  |
| 4   | DQ1        | 124 | VSS                  | 34  | DQS3            | 154 | VSS                     | 63  | NC,CK1         | 183 | VDD                  | 94  | DQS5  | 214 | VSS                  |
| 5   | VSS        | 125 | DM0,DQS9<br>,TDQS9   | 35  | VSS             | 155 | DQ30                    | 64  | NC,/CK1        | 184 | CK0                  | 95  | VSS   | 215 | DQ46                 |
| 6   | /DQS0      | 126 | NC,DQS9<br>,TDQS9    | 36  | DQ26            | 156 | DQ31                    | 65  | VDD            | 185 | /CK0                 | 96  | DQ42  | 216 | DQ47                 |
| 7   | DQS0       | 127 | VSS                  | 37  | DQ27            | 157 | VSS                     | 66  | VDD            | 186 | VDD                  | 97  | DQ43  | 217 | VSS                  |
| 8   | VSS        | 128 | DQ6                  | 38  | VSS             | 158 | CB4,NC                  | 67  | VREFCA         | 187 | /EVENT,NC            | 98  | VSS   | 218 | DQ52                 |
| 9   | DQ2        | 129 | DQ7                  | 39  | CB0,NC          | 159 | CB5,NC                  | 68  | NC/PAR<br>R_IN | 188 | A0                   | 99  | DQ48  | 219 | DQ53                 |
| 10  | DQ3        | 130 | VSS                  | 40  | CB0,NC          | 160 | VSS                     | 69  | VDD            | 189 | VDD                  | 100 | DQ49  | 220 | VSS                  |
| 11  | VSS        | 131 | DQ12                 | 41  | VSS             | 161 | DM8,DQS17<br>,TDQS17,NC | 70  | A10/AP         | 190 | BA1                  | 101 | VSS   | 221 | DM6,DQS15<br>,TDQS15 |
| 12  | DQ8        | 132 | DQ13                 | 42  | /DQS8           | 162 | NC,DQS17<br>,TDQS17     | 71  | BA0            | 191 | VDD                  | 102 | /DQS6 | 222 | NC,DQS15<br>,TDQS15  |
| 13  | DQ9        | 133 | VSS                  | 43  | DQS8            | 163 | VSS                     | 72  | VDD            | 192 | /RAS                 | 103 | DQS6  | 223 | VSS                  |
| 14  | VSS        | 134 | DM1,DQS10<br>,TDQS10 | 44  | VSS             | 164 | CB6,NC                  | 73  | /WE            | 193 | /S0                  | 104 | VSS   | 224 | DQ54                 |
| 15  | /DQS1      | 135 | NC,DQS10<br>,TDQS10  | 45  | CB2,NC          | 165 | CB7,NC                  | 74  | /CAS           | 194 | VDD                  | 105 | DQ50  | 225 | DQ55                 |
| 16  | DQS1       | 136 | VSS                  | 46  | CB3,NC          | 166 | VSS                     | 75  | VDD            | 195 | ODT0                 | 106 | DQ51  | 226 | VSS                  |
| 17  | VSS        | 137 | DQ14                 | 47  | VSS             | 167 | NC(TEST)                | 76  | /S1,NC         | 196 | A13                  | 107 | VSS   | 227 | DQ60                 |
| 18  | DQ10       | 138 | DQ15                 | 48  | VTT,NC          | 168 | /RESET                  | 77  | ODT1,N<br>C    | 197 | VDD                  | 108 | DQ56  | 228 | DQ61                 |
| 19  | DQ11       | 139 | VSS                  |     | KEY             |     |                         | 78  | VDD            | 198 | /S3,NC               | 109 | DQ57  | 229 | VSS                  |
| 20  | VSS        | 140 | DQ20                 | 49  | VTT,NC          | 169 | CKE1,NC                 | 79  | /S2,NC         | 199 | VSS                  | 110 | VSS   | 230 | DM7,DQS16<br>,TDQS16 |
| 21  | DQ16       | 141 | DQ21                 | 50  | CKE0            | 170 | VDD                     | 80  | VSS            | 200 | DQ36                 | 111 | /DQS7 | 231 | DM7,DQS16<br>,TDQS16 |
| 22  | DQ17       | 142 | VSS                  | 51  | VDD             | 171 | NC                      | 81  | DQ32           | 201 | DQ37                 | 112 | DQS7  | 232 | VSS                  |
| 23  | VSS        | 143 | DM2,DQS11<br>,TDQS11 | 52  | BA2             | 172 | A14                     | 82  | DQ33           | 202 | VSS                  | 113 | VSS   | 233 | DQ62                 |
| 24  | /DQS2      | 144 | NC,DQS11<br>,TDQS11  | 53  | /ERR_O<br>UT/NC | 173 | VDD                     | 83  | VSS            | 203 | DM4,DQS13<br>,TDQS13 | 114 | DQ58  | 234 | DQ63                 |
| 25  | DQS2       | 145 | VSS                  | 54  | VDD             | 174 | A12 / /BC               | 84  | /DQS4          | 204 | NC,DQS13<br>,TDQS13  | 115 | DQ59  | 235 | VSS                  |
| 26  | VSS        | 146 | DQ22                 | 55  | A11             | 175 | A9                      | 85  | DQS4           | 205 | VSS                  | 116 | VSS   | 236 | VDDSPD               |
| 27  | DQ18       | 147 | DQ23                 | 56  | A7              | 176 | VDD                     | 86  | VSS            | 206 | DQ38                 | 117 | SA0   | 237 | SA1                  |
| 28  | DQ19       | 148 | VSS                  | 57  | VDD             | 177 | A8                      | 87  | DQ34           | 207 | DQ39                 | 118 | SCL   | 238 | SDA                  |
| 29  | VSS        | 149 | DQ28                 | 58  | A5              | 178 | A6                      | 88  | DQ35           | 208 | VSS                  | 119 | SA2   | 239 | VSS                  |
| 30  | DQ24       | 150 | DQ29                 | 59  | A4              | 179 | VDD                     | 89  | VSS            | 209 | DQ44                 | 120 | VTT   | 240 | VTT                  |
|     |            |     |                      |     |                 |     |                         | 90  | DQ40           | 210 | DQ45                 |     |       |     |                      |

**Block Diagram**

**IDD Specification Parameter**

(IDD values are for full operating range of Voltage and Temperature)

| Symbol | Proposed Conditions                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Value | Units |
|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|
| IDD0   | <b>Operating one bank active-precharge current;</b><br>CKE: High; External clock: On; tCK, nRC, nRAS, CL; BL: 8a; AL: 0; CS: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling ; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registersb; ODT Signal: stable at 0; Pattern Details                                          | 315   | mA    |
| IDD1   | <b>Operating one bank active-read-precharge current;</b><br>CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL; BL: 8a; AL: 0; CS: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling ; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registersb; ODT Signal: stable at 0;                                                      | 378   | mA    |
| IDD2P0 | <b>Precharge power-down current;</b><br>CKE: Low; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO:MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registersb; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit                                                                                                                              | 90    | mA    |
| IDD2P1 | <b>Precharge power-down current;</b><br>CKE: Low; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO:MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registersb; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit                                                                                                                              | 108   | mA    |
| IDD2Q  | <b>Precharge quiet standby current;</b><br>CKE: High; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registersb; ODT Signal: stable at 0                                                                                                                                                               | 135   | mA    |
| IDD2N  | <b>Precharge standby current;</b><br>CKE: High; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registersb; ODT Signal: stable at 0                                                                                                                                                              | 135   | mA    |
| IDD3P  | <b>Active power-down current;</b><br>CKE: Low; External clock: On; tCK, CL: AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO:MID-LEVEL;DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registersb; ODT Signal: stable at 0                                                                                                                                                                 | 135   | mA    |
| IDD3N  | <b>Active standby current;</b><br>CKE: High; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registersb; ODT Signal: stable at 0                                                                                                                                                                   | 180   | mA    |
| IDD4W  | <b>Operating burst write current;</b><br>CKE: High; External clock: On; AL: 0; CS: High between WR; Command, Address, Bank Address Inputs: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH                         | 630   | mA    |
| IDD4R  | <b>Operating burst read current;</b><br>CKE: High; External clock: On; AL: 0; CS: High between RD; Command, Address, Bank Address Inputs: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM:stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0                                | 630   | mA    |
| IDD5B  | <b>Burst refresh current;</b><br>CKE: High; External clock: On; AL: 0; CS: High between REF; Command, Address, Bank Address Inputs: partially toggling ; Data IO: MID-LEVEL;DM:stable at 0; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registersb; ODT Signal: stable at 0                                                                                                                                                      | 800   | mA    |
| IDD6   | <b>Self refresh current;</b><br>TCASE: 0 - 85°C; Auto Self-Refresh (ASR): Disabledd; Self-Refresh Temperature Range (SRT): Normale; CKE: Low; External clock: Off; CK and CK: LOW; AL: 0; CS, Command, Address, Bank Address, Data IO: MID-LEVEL;DM:stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registersb; ODT Signal: MID-LEVEL                                                                                    | 90    | mA    |
| IDD7   | <b>Operating bank interleave read current;</b><br>CKE: High; External clock: On; AL: CL-1; CS: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM:stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registersb; ODT Signal: stable at 0 | 1170  | mA    |
| IDD8   | <b>RESET Low Current RESET :</b> Low; External clock : off; CK and CK : LOW; CKE : FLOATING ; CS, Command, Address, Bank Address, Data IO : FLOATING ; ODT Signal : FLOATING                                                                                                                                                                                                                                                                                        | 90    | mA    |

## Absolute Maximum DC ratings

| Symbol                             | Parameter                                                   | Rating         | Units | Notes |
|------------------------------------|-------------------------------------------------------------|----------------|-------|-------|
| V <sub>DD</sub>                    | Voltage on V <sub>DD</sub> pin relative to V <sub>SS</sub>  | -0.4V ~ 1.975V | V     | 1,3   |
| V <sub>DDQ</sub>                   | Voltage on V <sub>DDQ</sub> pin relative to V <sub>SS</sub> | -0.4V ~ 1.975V | V     | 1,3   |
| V <sub>IN</sub> , V <sub>OUT</sub> | Voltage on any pin relative to V <sub>SS</sub>              | -0.4V ~ 1.975V | V     | 1     |
| T <sub>STG</sub>                   | Storage Temperature                                         | -55 ~ +100     | °C    | 1, 2  |

Note:

- 1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2) Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- 3) V<sub>DD</sub> and V<sub>DDQ</sub> must be within 300mV of each other at all times; and V<sub>REF</sub> must be not greater than 0.6 x V<sub>DDQ</sub>. When V<sub>DD</sub> and V<sub>DDQ</sub> are less than 500mV; V<sub>REF</sub> may be equal to or less than 300mV.

## AC and DC Operating Conditions

Recommended DC Operating Conditions (SSTL - 1.8)

| Symbol           | Parameter                 | Rating |      |       | Units | Notes |
|------------------|---------------------------|--------|------|-------|-------|-------|
|                  |                           | Min.   | Typ. | Max.  |       |       |
| V <sub>DD</sub>  | Supply Voltage            | 1.425  | 1.5  | 1.575 | V     | 1,2   |
| V <sub>DDQ</sub> | Supply Voltage for Output | 1.425  | 1.5  | 1.575 | V     | 1,2   |

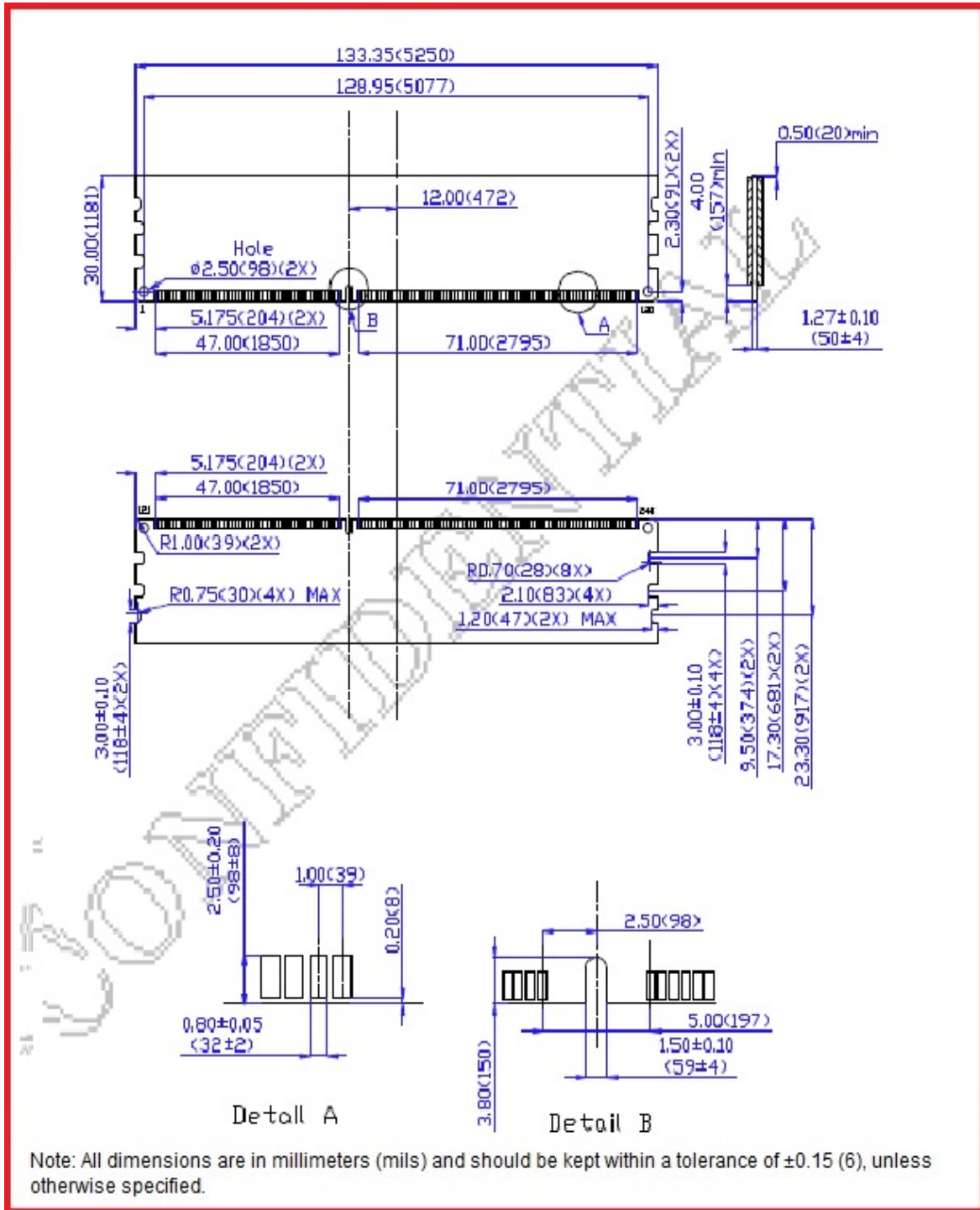
Note :

- 1) Under all conditions V<sub>DDQ</sub> must be less than or equal to V<sub>DD</sub>.
- 2) V<sub>DDQ</sub> tracks with V<sub>DD</sub>. AC parameters are measured with V<sub>DD</sub> and V<sub>DDQ</sub> tied together.

## Input/Output Capacitance

| Symbol          | Parameter                                                 | Max. | Units |
|-----------------|-----------------------------------------------------------|------|-------|
| C <sub>CK</sub> | Input capacitance, CK and /CK                             | 1.4  | pF    |
| C <sub>I</sub>  | Input capacitance (All other input only pins)             | 1.3  |       |
| C <sub>ZQ</sub> | Input/output capacitance of ZQ pin                        | 3    |       |
| C <sub>IO</sub> | Input/output capacitance (DQ, DM, DQS, /DQS, TDQS, /TDQS) | 2.3  |       |

**Physical Dimension** (drawing not in scale) Units : in Millimeters



## RoHS Declaration



### Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product ACT1GHR72N8G1333S complies with the requirement of RoHS directives 2002/95/EC and 2006/122/EC.

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3<sup>rd</sup> party test reports of the component/ raw materials used in the manufacture of products.

✚ RoHS Exemptions Applied Of 7(C)-I for Resist.

| Name of hazardous substance      | Limited of RoHS ppm (mg/kg) |
|----------------------------------|-----------------------------|
| Cd                               | < 100 ppm                   |
| Pb                               | < 1000 ppm                  |
| Hg                               | < 1000 ppm                  |
| Chromium VI (Cr+6)               | < 1000 ppm                  |
| Polybromodiphenyl ether (PBDE)   | < 1000 ppm                  |
| Polybrominated Biphenyls (PBB)   | < 1000 ppm                  |
| Perfluorooctane Sulfonate (PFOS) | Not Contained               |

Date issued: 2014/09/05

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Authorized Signature :

QA Dept. Director – Ryan Tsai