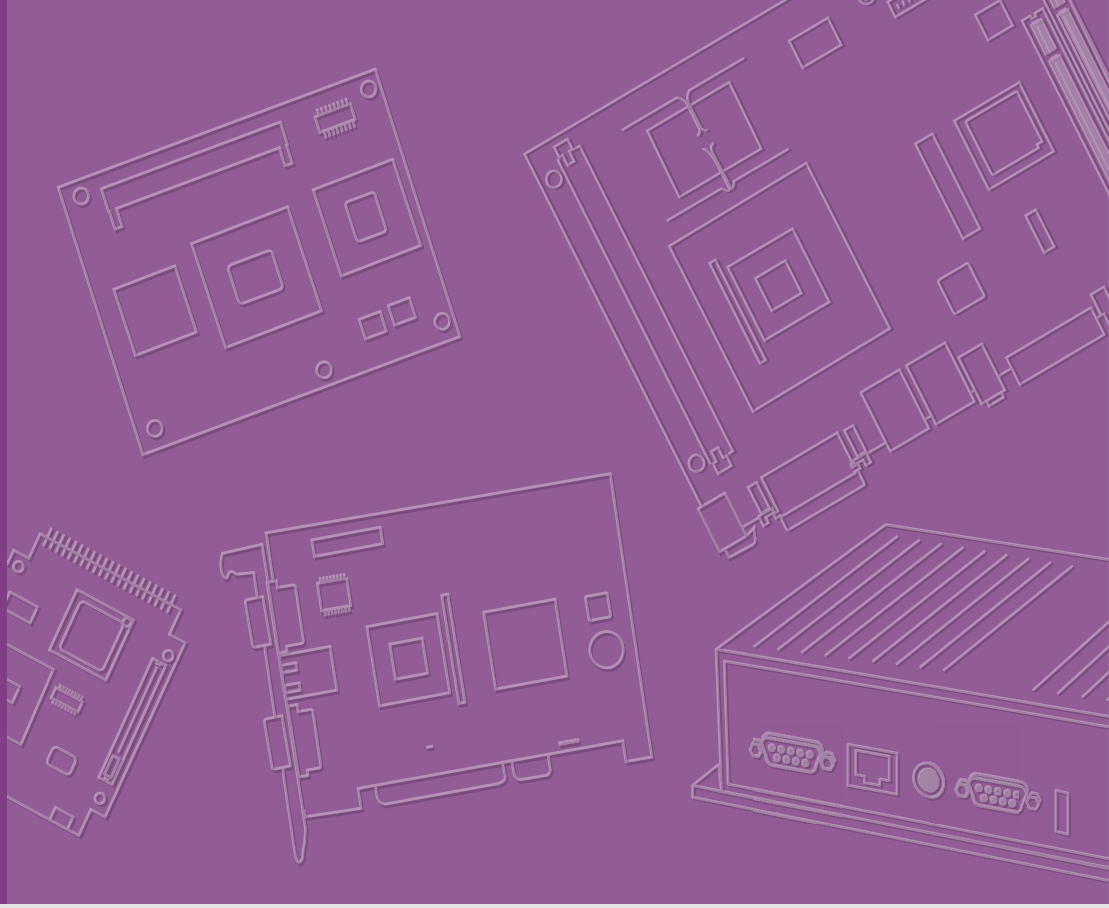

User Manual

AIMB-593

Micro-ATX Motherboard
AMD EPYC 8004 Series
Processor

ADVANTECH

Enabling an Intelligent Planet

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Product Warranty (2 Years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced free of charge during the warranty period. For out-of-warranty repairs, customers will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details.

If you believe your product to be defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

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A Message to the Customer

Advantech Customer Services

Each and every Advantech product is built to the most exacting specifications to ensure reliable performance in the harsh and demanding conditions typical of industrial environments. Whether your new Advantech equipment is destined for the laboratory or the factory floor, you can be assured that your product will provide the reliability and ease of operation for which the name Advantech has come to be known. Your satisfaction is our primary concern. Here is a guide to Advantech's customer services. To ensure you get the full benefit of our services, please follow the instructions below carefully.

Technical Support

We want you to get the maximum performance from your products. So if you run into technical difficulties, we are here to help. For the most frequently asked questions, you can easily find answers in your product documentation. These answers are normally a lot more detailed than the ones we can give over the phone.

So please consult this manual first. If you still cannot find the answer, gather all the information or questions that apply to your problem, and with the product close at hand, call your dealer. Our dealers are well trained and ready to give you the support you need to get the most from your Advantech products. In fact, most problems reported are minor and are able to be easily solved over the phone.

In addition, free technical support is available from Advantech engineers every business day. We are always ready to give advice on application requirements or specific information on the installation and operation of any of our products.

Declaration of Conformity

FCC Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

CPU Compatibility

Processor Number	Code Name	Max_TDP (W)	Cores	Max Speed (GHz)	Smart Cache (L3)	Lithography	ADVANTECH P/N	Result
AMD EPYC 8534P	Siena	200	64	3.1	128MB	5nm	96MPEY-8534P-64CE	PASS
AMD EPYC 8434P	Siena	200	48	3.1	128MB	5nm	96MPEY-8434P-48CE	PASS
AMD EPYC 8324P	Siena	180	32	3	128MB	5nm	96MPEY-8324P-32CE	PASS
AMD EPYC 8224P	Siena	160	24	3	64MB	5nm	96MPEY-8224P-24CE	PASS
AMD EPYC 8124P	Siena	125	16	2.95	64MB	5nm	96MPEY-8124P-16CE	PASS
AMD EPYC 8C24P	Siena	100	12	2.95	32MB	5nm	96MPEY-8C24P-12CE	PASS

ECC Memory Compatibility

Category	Speed	Capacity	Vendor	Module P/N	Chip P/N	ADVANTECH P/N	ECC	Result
DDR5	4800	16GB	Advantech	AD5R480016G10-BSSB	SEC210 K4RAH086VBBCQK	AD5R480016G10-BSSB	ECC	PASS
DDR5	6400	16GB	Advantech	AQD-D5V16GR64-HB	H5CG48AHBDX018 441A	AQD-D5V16GR64-HB	ECC	PASS
DDR5	4800	32GB	Advantech	AD5R480032G20-BSSB	SEC210 K4RAH086VBBQK	AD5R480032G20-BSSB	ECC	PASS
DDR5	5600	64GB	Advantech	AD5R560064G40-SHYA	H5CG44AGBDX018 503V	N/A	ECC	PASS
DDR5	4800	96GB	Advantech	SQR RD5N96G4K8SRUB	SEC537 PDRQM4DCBG12	SQR RD5N96G4K8SRUB	ECC	PASS

Initial Inspection

Before you begin installing your motherboard, please make sure that the following materials have been shipped:

- 1 x AIMB-593 Motherboard
- 1 x I/O port bracket
- 1 x startup manual
- 1 x warranty card
- 2 x Screws (M2.5*4L)

If any of these items are missing or damaged, contact your distributor or sales representative immediately. We carefully inspect the AIMB-593 mechanically and electrically before shipment. It should be free of marks and scratches and in perfect working order upon receipt. As you unpack the AIMB-593, check it for signs of shipping damage. (for example, a damaged box, scratches, or dents, etc.) If it is damaged or it does not meet the specifications, notify our service department or your local sales representative immediately. Also notify the carrier. Retain the shipping carton and packing materials for inspection by the carrier. After inspection, we will arrange to repair or replace the unit.

Contents

Chapter 1

General Information

1.1 Introduction

AIMB-593 is powered by AMD® EPYC™ 8004 Series processors (LGA 4844, SP6, up to 200W TDP), delivering robust performance and power efficiency for a wide range of industrial applications. This Micro-ATX motherboard supports up to 96 GB of six-channel DDR5-4800 MT/s memory across six 288-pin RDIMMs slots. It features extensive I/O connectivity, including four PCIe Gen5 x16 slots (6 x PCIe slots total with an extension board), two MCIO 8i connectors (supporting CXL and two PCIe 5.0 ports), two 2.5GbE LAN ports, two 10GbE LAN ports, five USB 3.2 Gen 1 ports, and one COM port. The AIMB-593 also offers two M.2 M-key slots for NVMe SSDs.

Features

- AMD® EPYC™ 8004 series Processors, max. 64Core
- Supports 576GB DDR5 4800MT/s with 6 x RDIMMs for data transfer
- 2 x M.2 M-Key 2280 slots (PCIe Gen5 x4) for high-speed NVMe SSDs
- Up to 5 x PCIe Gen5x16 slots, default onboard 4 x PCIe Gen5x16 slots
- 2 MCIO x8 (offer extension board for additional 2 PCIe slots)
- Intel® X710-AT2 dual 10GbE ports & I226 dual GbE ports

1.2 Specifications

1.2.1 System

- **CPU:** Supports AMD® EPYC™ 8004 series Processors (LGA 4844, SP6, up to 200W TDP)
- **BIOS:** AMI EFI 256 Mbit SPI BIOS
- **Storage Interface:** Two M.2 M-Key 2280 for NVMe SSD (PCIe Gen5x4)

1.2.2 Memory

- **RAM:** Supports six channel DDR5 4800MT/s RDIMMs, up to 576GB Max

1.2.3 Input/Output

- **Serial ports:** Supports one RS-232 serial port
- **USB port:** Supports five USB 3.2 Gen1
- **GPIO connector:** 8-bit general purpose Input/Output.

1.2.4 Ethernet LAN

- Supports dual 10/100/1000/2500 Mbps Ethernet port (s) and dual 10/100/1000/2500/10000 Mbps Ethernet port (s)
- **Controller:**
  - LAN1: Intel I226-LM 2.5 GbE
  - LAN2: Intel I226-LM 2.5 GbE
  - LAN3: Intel X710-AT2 10 GbE
  - LAN4: Intel X710-AT2 10 GbE

1.2.5 Industrial Features

- **Watchdog timer:** Can generate a system reset. The watchdog timer is programmable, with each unit equal to one second or one minute (255 levels).

1.2.6 Mechanical and Environmental Specifications

- **Operating temperature:** 0 ~ 60°C (32 ~ 140°F)
- **Storage temperature:** -40 ~ 85°C (-40 ~ 185°F)
- **Humidity:** 5 ~ 95% non-condensing.
- **Power supply voltage:**

Table 1.1: Power supply voltage

Operation	+5V	3.3V	12V	12V_8P
Configuration: AMD EPYC 8534P 64-core Processor 3.1GHz with RDIMM DDR5 4800 32GB*6pcs	2.79833A	1.77855A	1.52298A	9.64435A
Standby (5Vsb)	3A			

- **Power consumption:**
- **Board size:** 244 mm x 244 mm (9.6” x 9.6”) x 2.4mm
- **Board weight:** 1.5 kg

1.3 Jumpers and Connectors

Connectors on the AIMB-593 motherboard link it to devices such as hard disk drives and a keyboard. In addition, the board has a number of jumpers used to configure the system for your application. Later sections in this chapter give instructions on setting jumpers. Chapter 2 gives instructions for connecting external devices to your mother-board.

1.4 Board Layout: Jumper and Connector Locations

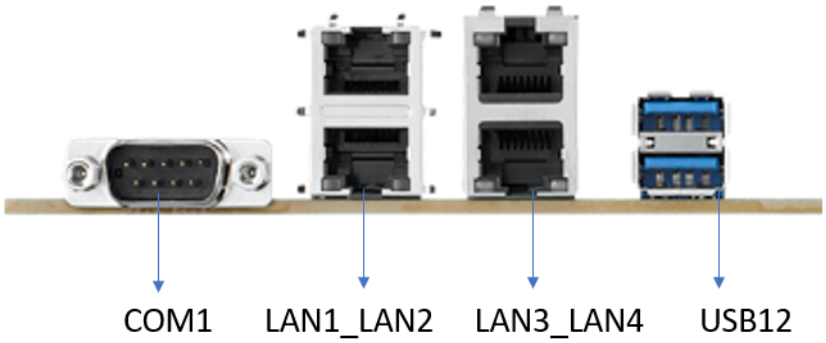


Figure 1.1 Rear I/O

Table 1.2: I/O Connector

Item	Description	Part Reference
1	COM1 Connector	COM1
2	RJ45 Connector	LAN1_LAN2
3	RJ45 Connector	LAN3_LAN4
4	USB Connector	USB12

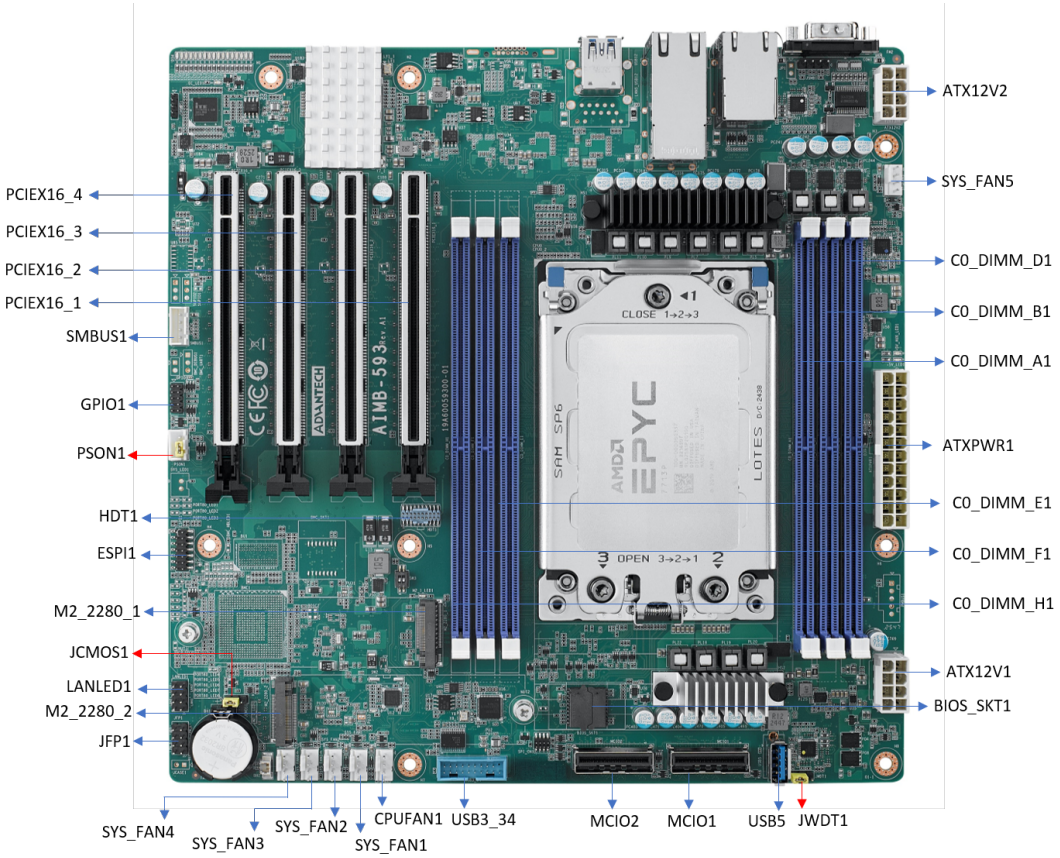


Figure 1.2 Jumper and Connector Locations (Top Side)

Table 1.3: Connector/Header List

Item	Description	Part Reference
1	ATX 24 Pin Power Connector	ATXPWR1
2	ATX 8 Pin Power Connector	ATX12V1
3	ATX 8 Pin Power Connector	ATX12V2
4	SMBus connector	SMBUS1
5	GPIO pin header	GPIO1
6	AT / ATX Mode selection	PSON1
7	LED port 80 pin header	ESPI1
8	LAN1 LED/ LAN2 LED/ LAN3 LED/ LAN4 LED	LANLED1
9	PWRBTN#/ RESET#/HDD LED/ PWR LED pin header	JFP1
10	BATTERY connector	BH2
11	CPU FAN Connector	CPUFAN1
12	System Fan #1 Connector	SYS_FAN1
13	System Fan #2 Connector	SYS_FAN2
14	System Fan #3 Connector	SYS_FAN3
15	System Fan #4 Connector	SYS_FAN4
16	System Fan #5 Connector	SYS_FAN5
17	USB Connector	USB3_34
19	MCIO Connector	MCIO1
20	MCIO Connector	MCIO2
21	USB Connector	USB5
22	Watchdog timer selection	JWDT1

Table 1.3: Connector/Header List		
23	DDR5 RDIMM Socket A1	C0_DIMM_A1
24	DDR5 RDIMM Socket B1	C0_DIMM_B1
25	DDR5 RDIMM Socket D1	C0_DIMM_D1
26	DDR5 RDIMM Socket E1	C0_DIMM_E1
27	DDR5 RDIMM Socket F1	C0_DIMM_F1
28	DDR5 RDIMM Socket H1	C0_DIMM_H1
29	M.2 M-KEY Connector	M2_2280_1
30	M.2 M-KEY Connector	M2_2280_2
31	HDT Debug Connector	HDT1
32	SPI BIOS Flash Socket	BIOS_SKT1
33	Power program pin header	JSMB1
34	PCI Express x16 slot	PCIEX16_1
35	PCI Express x16 slot	PCIEX16_2
36	PCI Express x16 slot	PCIEX16_3
37	PCI Express x16 slot	PCIEX16_4
38	CMOS Mode selection	JCMOS1

1.5 AIMB-593 Board Diagram

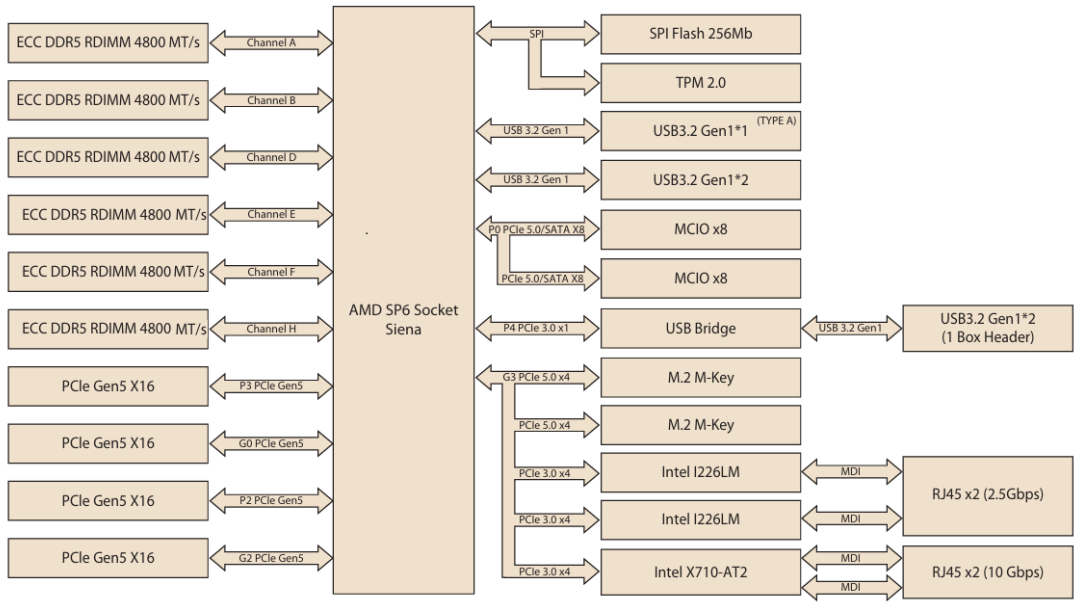


Figure 1.3 AIMB-593 Board Diagram

1.6 Safety Precautions

Warning! *Always disconnect the power cord from the chassis before working on the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced service personnel should open the PC chassis.*

Caution! *Always ground yourself to remove any static charge before touching the motherboard. Modern electronic devices are very sensitive to electrostatic discharges. As a safety precaution, use a grounding wrist strap whenever handling the hardware. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis.*

Caution! *The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if the battery is incorrectly replaced. Replace the battery only with the same or an equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*

Caution! *There is a danger of explosion if the battery is incorrectly installed. Do not attempt to recharge, disassemble, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*

1.7 Jumper Settings

This section provides instructions on how to configure your motherboard by setting the jumpers. It also includes the motherboard's default settings and your options for each jumper. You can configure your motherboard to match the needs of your application by setting the jumpers. A jumper is a metal bridge that closes an electrical circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them.

1.7.1 How to Set Jumpers

To close (or turn on) a jumper, connect the pins with the clip. To open (or turn off) a jumper, remove the clip. Some jumpers consist of three pins labeled 1, 2, and 3. In this case, connect either pins 1 and 2 or pins 2 and 3. A pair of needle-nose pliers may be useful when setting jumpers.

1.7.2 Watchdog Timer Selection (JWDT1)

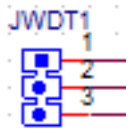
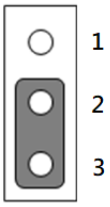
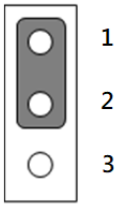


Table 1.4:

Pin	Signal
1	EC_WDTRST#
2	WDT#
3	+V3.3_AUX

Table 1.5:

Function	Jumper Setting
Disable JWDT1(2-3)	
Enable (Default) JWDT1(1-2)	

1.7.3 AT/ATX Mode Selection (PSON1)

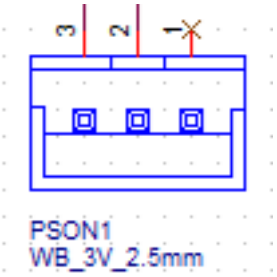
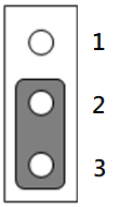
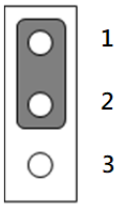


Table 1.6:

Pin	Signal
1	NC
2	AT
3	ATX

Table 1.7:

Function	Jumper Setting
ATX Mode (Default) PSON1(2-3)	
AT Mode PSON1	

1.7.4 CMOS Mode Selection (JCMOS1)

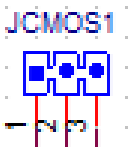
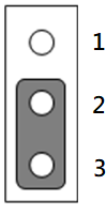
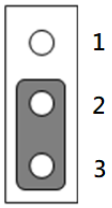


Table 1.8:	
Pin	**Signal**
1	+V3.3_RTC_JMP
3	+V3.3_CPU0_RTC
5	GND

Table 1.9:	
Function	**Jumper Settings**
Normal (Default) JCMOS1(1-2)	
Clear CMOS JCMOS(2-3)	

1.8 System Memory

AIMB-593 has six 288-pin DDR5 memory sockets for modules with maximum capacity of 576GB (maximum 96GB for each DIMM).

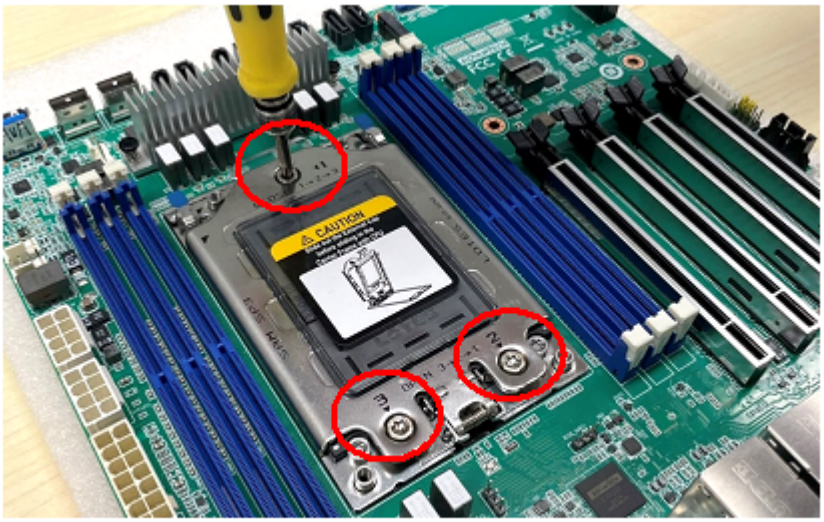
1.9 Memory Installation Procedures

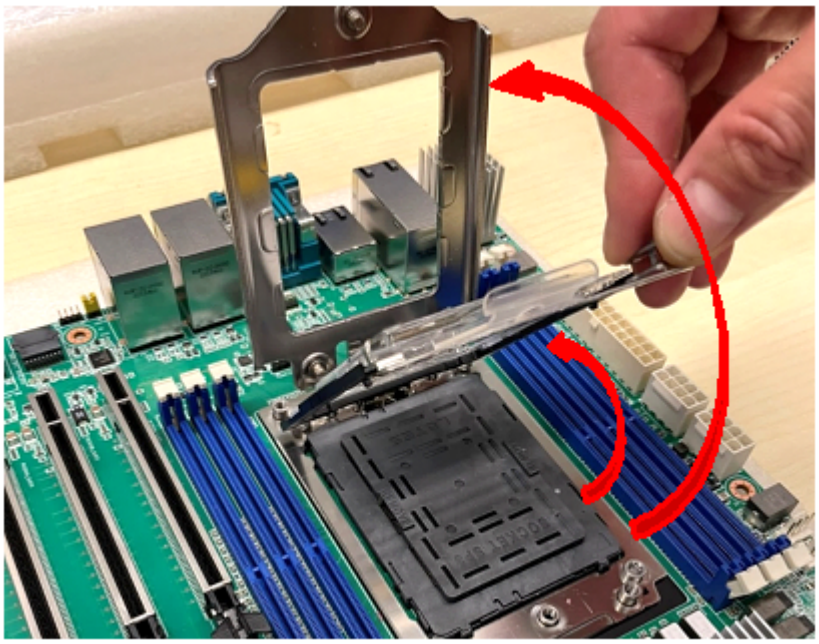
To install DIMMs, first make sure the two handles on the DIMM socket are in the open position; that is, the handles should lean outward. Slowly slide the DIMM module along the plastic guides on both ends of the socket. Then press the DIMM module firmly but gently into the socket (avoid applying excessive force) until you hear a click, indicating that the two handles have automatically locked the module into place. To remove the memory module, push both handles outward and the memory module will be ejected automatically.

1.10 Processor Installation

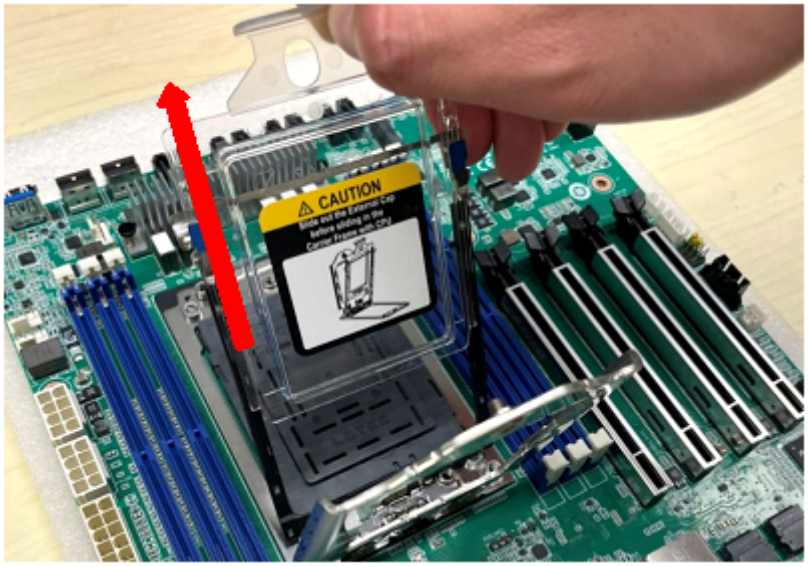
The AIMB-593 is designed for AMD EPYC 8004 Series processors. Please follow the processor installation as shown below.

1. Undo the three screws (shown above in red circles) from the top of the socket retention mechanism (SRM). Then rotate the retention frame and rail frame (with the external cap).

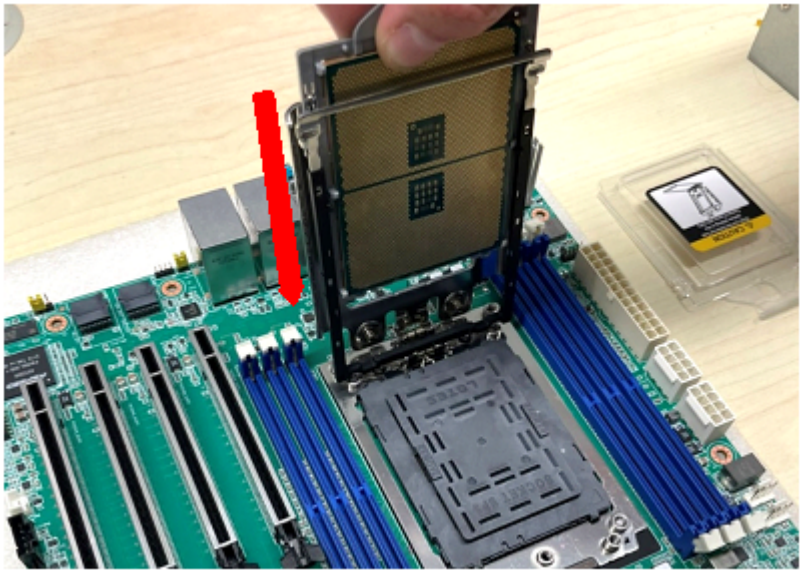


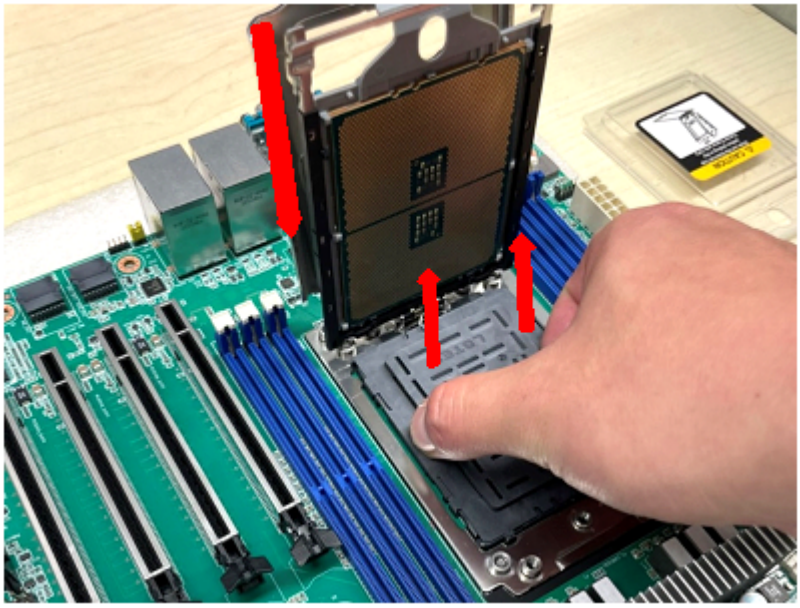


2. Remove the external cap by pulling upwards.

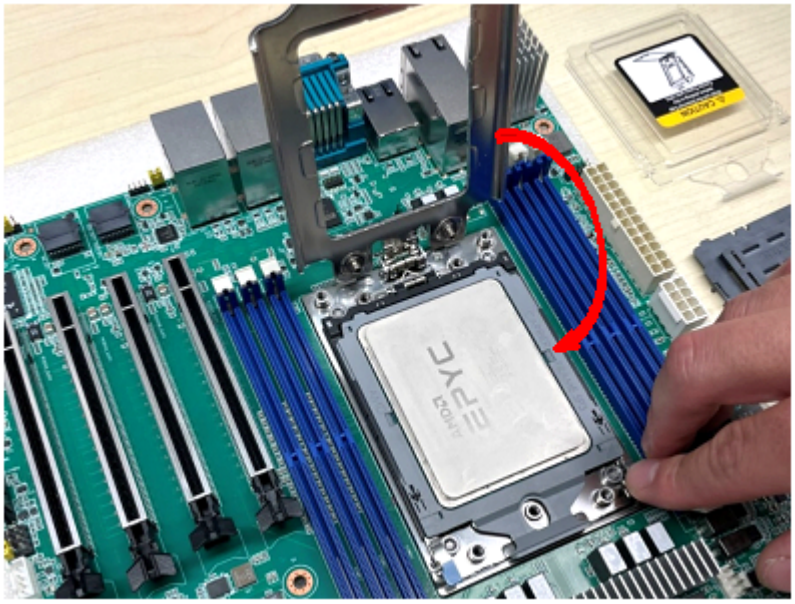


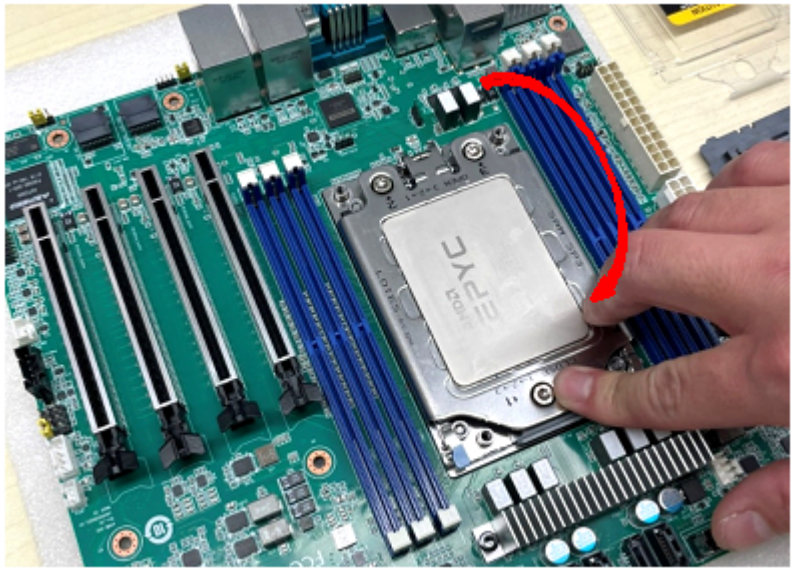
3. Install the carrier frame/CPU package onto the rail frame, then remove the PnP cover cap. Be very careful not to drop the PnP cover cap into the exposed contact field during the removal process.



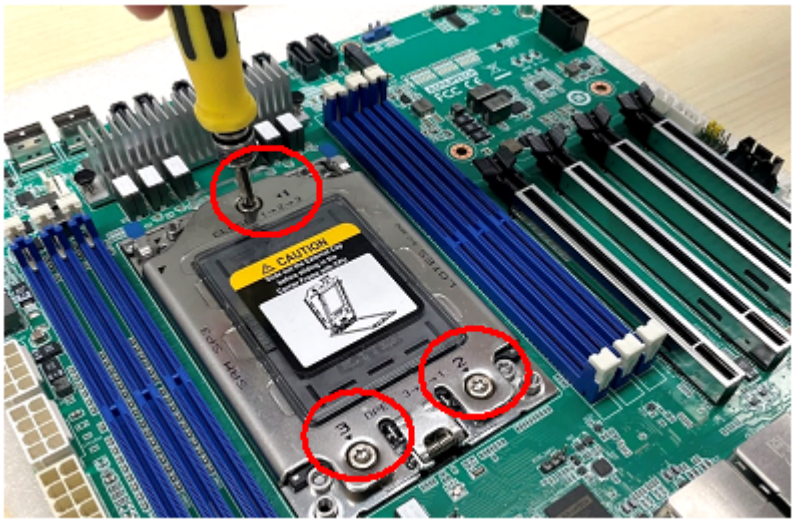


4. Rotate and push the rail frame and retention frame until they are in the horizontal position.

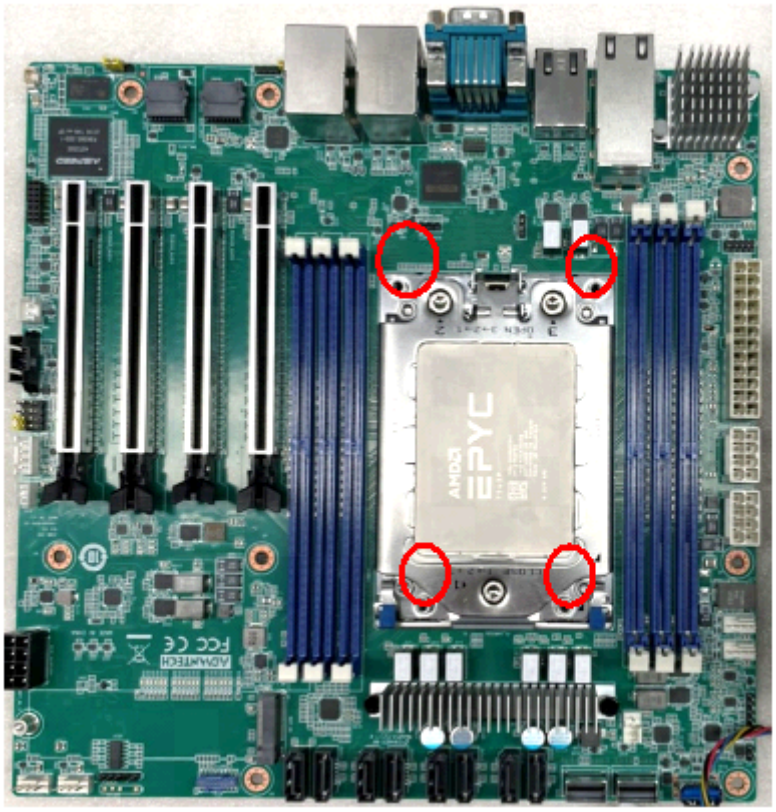




5. Tighten the three screws (shown above in red circles) by using a T-20 screw-driver.



6. Install the processor heatsink module into the socket retention mechanism (SRM) by using a T-20 screwdriver (follow the heatsink label direction 1-2-3-4).



Chapter 2

Connecting Peripherals

2.1 Introduction

You can access most of the connectors from the top of the board as it is being installed in the chassis. If you have a number of cards installed or have a packed chassis, you may need to partially remove the card to make all the connections.

2.2 I/O Connector

2.2.1 ATX 24 Pin Power Connector (ATXPWR1)

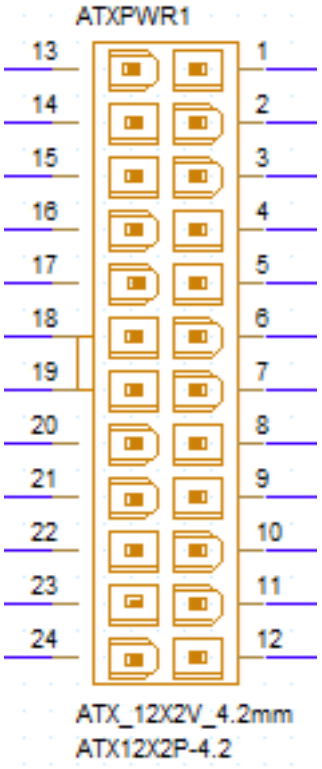


Table 2.1: ATX 24 Pin Power Connector (ATXPWR1)

Pin	Signal	Pin	Signal
P1	+V3.3	P13	+V3.3
P2	+V3.3	P14	-V12
P3	GND	P15	GND
P4	+V5	P16	PS ON
P5	GND	P17	GND
P6	+V5	P18	GND
P7	GND	P19	GND
P8	POWER GOOD	P20	-V5
P9	+V5SB	P21	+V5
P10	+V12	P22	+V5
P11	+V12	P23	+V5
P12	+V3.3	P24	GND

2.2.2 ATX 8 Pin Power Connector (ATX12V1)

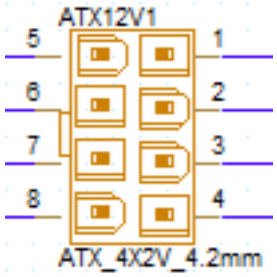


Table 2.2: ATX 8 Pin Power Connector (ATX12V1)

Pin	Signal	Pin	Signal
P1	GND	P5	+V12_8P_0
P2	GND	P6	+V12_8P_0
P3	GND	P7	+V12_8P_0
P4	GND	P8	+V12_8P_0

2.2.3 ATX 8 Pin Power Connector (ATX12V2)

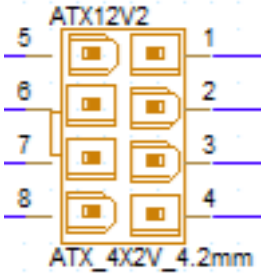


Table 2.3: ATX 8 Pin Power Connector (ATX12V2)

Pin	Signal	Pin	Signal
P1	GND	P5	+V12
P2	GND	P6	+V12
P3	GND	P7	+V12_8P_0
P4	GND	P8	+V12_8P_0

2.2.4 COM1 Connector (COM1))

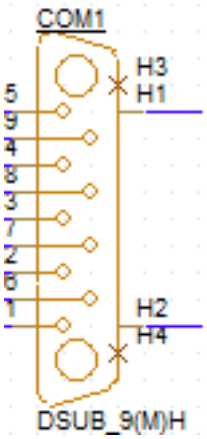


Table 2.4: COM1 Connector (COM1))

Pin	Signal	Pin	Signal
1	B_COM1_DCD	2	B_COM1_RXD#
3	B_COM1_TXD#	4	B_COM1_DTR
5	GND	6	B_COM1_DSR
7	B_COM1_RTS	8	B_COM1_CTS
9	B_COM1_RI		

2.2.5 RJ45 Connector (LAN1_LAN2)

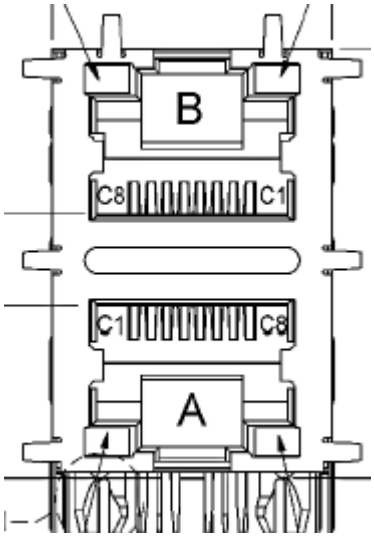


Table 2.5: RJ45 Connector (LAN1_LAN2)

Pin	Signal	Pin	Signal
RA1	LAN1_MDI_P0	RB1	LAN2_MDI_P0
RA2	LAN1_MDI_N0	RB2	LAN2_MDI_N0
RA3	LAN1_MDI_P1	RB3	LAN2_MDI_P1
RA4	LAN1_MDI_N1	RB4	LAN2_MDI_N1
RA5	LAN1_MDI_P2	RB5	LAN2_MDI_P2
RA6	LAN1_MDI_N2	RB6	LAN2_MDI_N2
RA7	LAN1_MDI_P3	RB7	LAN2_MDI_P3
RA8	LAN1_MDI_N3	RB8	LAN2_MDI_N3

2.2.6 RJ45 Connector (LAN3_LAN4)

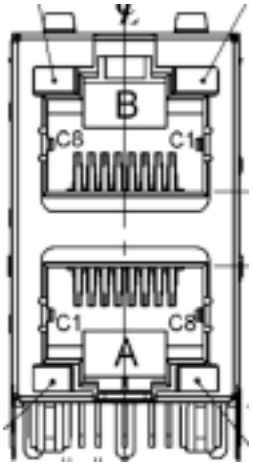


Table 2.6: RJ45 Connector (LAN3_LAN4)

Pin	Signal	Pin	Signal
A1	X710_MDI0_0_P	B1	X710_MDI1_0_P
A2	X710_MDI0_0_N	B2	X710_MDI1_0_N
A4	X710_MDI0_1_P	B4	X710_MDI1_1_P
A5	X710_MDI0_1_N	B5	X710_MDI1_1_N
A7	X710_MDI0_2_P	B7	X710_MDI1_2_P
A8	X710_MDI0_2_N	B8	X710_MDI1_2_N
A10	X710_MDI0_3_P	B10	X710_MDI1_3_P
A11	X710_MDI0_3_N	B11	X710_MDI1_3_N

2.2.7 USB Connector (USB12)

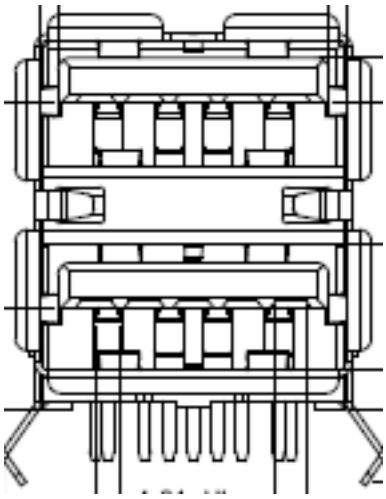


Table 2.7: USB Connector (USB12)

Pin	Signal	Pin	Signal
2	USB2_CPU0_USB3C1_a_N2	11	USB2_CPU0_USB3C1_a_N1
3	USB2_CPU0_USB3C1_a_P2	12	USB2_CPU0_USB3C1_a_P1
5	USB3_CPU0_USB3C1_b_RX_N2	14	USB3_CPU0_USB3C1_b_RX_N1
6	USB3_CPU0_USB3C1_b_RX_P2	15	USB3_CPU0_USB3C1_b_RX_P1
8	USB3_CPU0_USB3C1_b_TX_N2	17	USB3_CPU0_USB3C1_b_TX_N1
9	USB3_CPU0_USB3C1_b_TX_P2	18	USB3_CPU0_USB3C1_b_TX_P1

2.2.8 SMBus Connector (SMBUS1)

Table 2.8: SMBus Connector (SMBUS1)

Pin	Signal
1	+V5_SMBUS
2	CN_SMB_CLK
3	CN_SMB_DATA
4	GND

2.2.9 GPIO Pin Header (GPIO1)

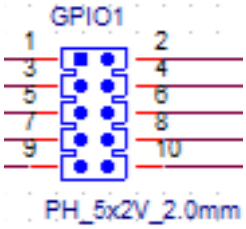


Table 2.9: GPIO Pin Header (GPIO1)

Pin	Signal	Pin	Signal
1	CN_GPIO0	2	CN_GPIO4
3	CN_GPIO1	4	CN_GPIO5
5	CN_GPIO2	6	CN_GPIO6
7	CN_GPIO3	8	CN_GPIO7
9	+VCC_GPIO	10	GND

2.2.10 LED Port 80 Pin Header (ESPI1)

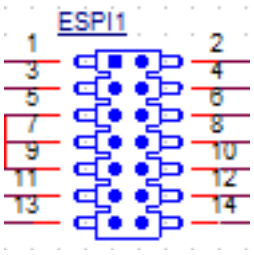


Table 2.10: LED Port 80 Pin Header (ESPI1)

Pin	Signal	Pin	Signal
1	CPU0_P80_ESPI_DAT1	2	CPU0_P80_ESPI_CLK
3	CPU0_P80_ESPI_DAT0	4	CPU0_P80_ESPI_RST_N
5	+V3.3	6	CPU0_P80_ESPI_CS_N
7	GND	8	CPU0_P80_ESPI_DAT3
9	+V3.3_AUX	10	CPU0_P80_ESPI_DAT2
11	+V1.8_AUX_CPU0	12	ESPI_SMB_CLK
13	CPU0_P80_ESPI_ALERT	14	ESPI_SMB_DATA

2.2.11 LAN1 LED/LAN2 LED/LAN3 LED/LAN4 LED (LANLED1)

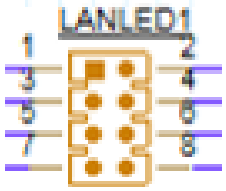


Table 2.11: LAN1 LED/LAN2 LED/LAN3 LED/LAN4 LED (LANLED1)

Pin	Signal	Pin	Signal
1	LAN1_LED2_ACT#	2	LAN2_LED2_ACT#
3	+V3.3_AUX	4	+V3.3_AUX
5	LAN3_ACT_LVC3#	6	LAN4_ACT_LVC3#
7	+V3.3_AUX	8	+V3.3_AUX

2.2.12 PWRBTN#/ RESET#/HDD LED/ PWR LED Pin Header (JFP1)

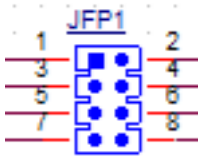


Table 2.12: PWRBTN#/ RESET#/HDD LED/ PWR LED Pin Header (JFP1)

Pin	Signal	Pin	Signal
1	FP_RST_BTN_N	2	FP_PWR_BTN_N
3	GND	4	GND
5	+V3.3_AUX	6	+V3.3
7	PWRLED#	8	SATA_LED_N

2.2.13 Battery Connector (BH2)

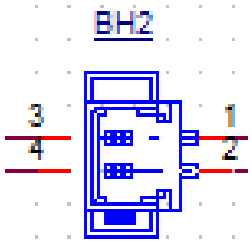


Table 2.13: Battery Connector (BH2)

Pin	Signal
1	+VBAT
2	GND
3	GND
4	GND

2.2.14 CPU FAN Connector (CPUFAN1)

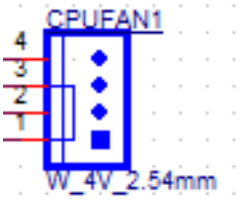


Table 2.14: CPU FAN Connector (CPUFAN1)

Pin	Signal
1	GND
2	+V12
3	TACH
4	PWM

2.2.15 System Fan Connector (SYS_FAN1~5)

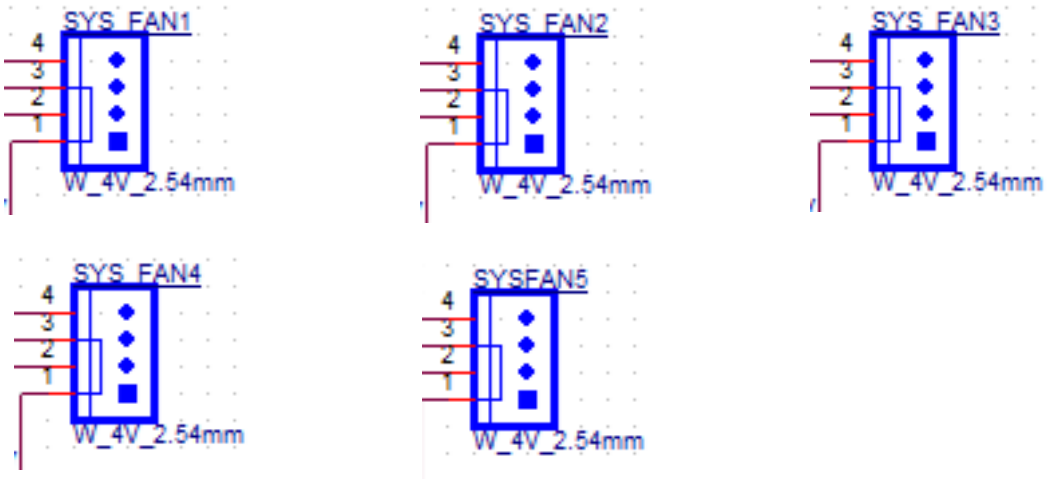


Table 2.15: System Fan Connector (SYS_FAN1_5)

Pin	Signal
1	GND
2	+V12
3	TACH
4	PWM

2.2.16 USB Connector (USB3_34)

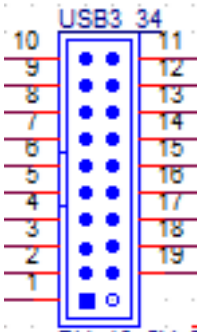


Table 2.16: USB Connector (USB3_34)

Pin	Signal	Pin	Signal
1	+V5_USB3_34	11	USB2_CTRL_USB3H1_a_P4
2	USB3_CTRL_USB3H1_a_RX_N3	12	USB2_CTRL_USB3H1_a_N4
3	USB3_CTRL_USB3H1_a_RX_P3	13	GND
4	GND	14	USB3_CTRL_USB3H1_b_TX_P4
5	USB3_CTRL_USB3H1_b_TX_N3	15	USB3_CTRL_USB3H1_b_TX_N4
6	USB3_CTRL_USB3H1_b_TX_P3	16	GND
7	GND	17	USB3_CTRL_USB3H1_a_RX_P4
8	USB2_CTRL_USB3H1_a_N3	18	USB3_CTRL_USB3H1_a_RX_N4
9	USB2_CTRL_USB3H1_a_P3	19	+V5_USB3_34
10	NC	20	NC

2.2.17 MCIO Connector (MCIO1)

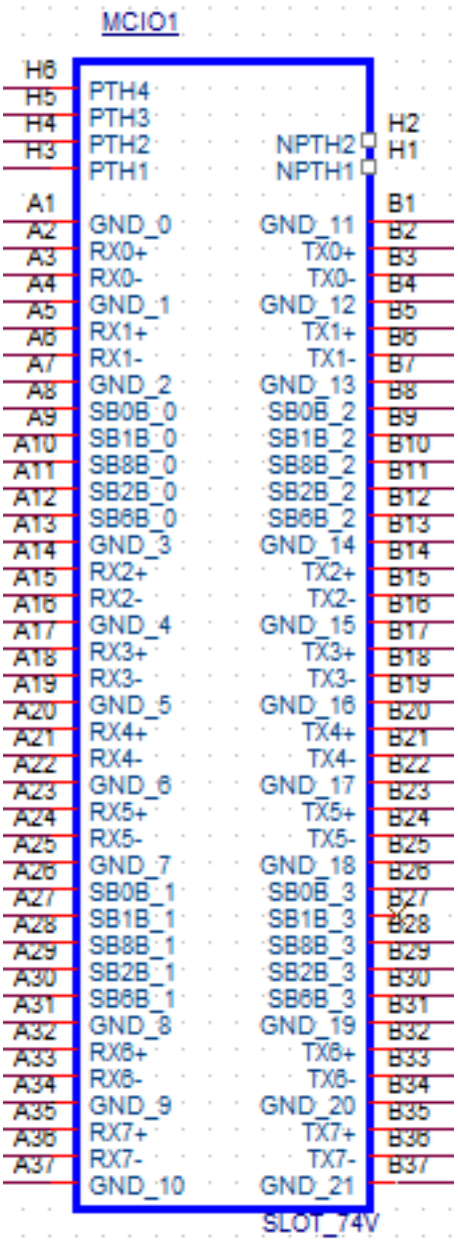


Table 2.17: MCIO Connector. (MCIO1)			
Pin	**Signal**	**Pin**	**Signal**
A1	GND	B1	GND
A2	PCIE_CPU0_MCIO1_RX_P0	B2	PCIE_CPU0_MCIO1_TX_P0
A3	PCIE_CPU0_MCIO1_RX_N0	B3	PCIE_CPU0_MCIO1_TX_N0
A4	GND	B4	GND
A5	PCIE_CPU0_MCIO1_RX_P1	B5	PCIE_CPU0_MCIO1_TX_P1
A6	PCIE_CPU0_MCIO1_RX_N1	B6	PCIE_CPU0_MCIO1_TX_N1
A7	GND	B7	GND
A8	MCIO1_NVME1_SMB_CLK	B8	MCIO1_HP_SMB_CLK
A9	MCIO1_NVME1_SMB_DATA	B9	MCIO1_HP_SMB_DATA
A10	GND	B10	GND
A11	CLK100M_BUFF_MCIO1_a_P	B11	PCIE_RST_MCIO1_NVME1_N
A12	CLK100M_BUFF_MCIO1_a_N	B12	MCIO1_NVME1_PRSNT_N
A13	GND	B13	GND
A14	PCIE_CPU0_MCIO1_RX_P2	B14	PCIE_CPU0_MCIO1_TX_P2
A15	PCIE_CPU0_MCIO1_RX_N2	B15	PCIE_CPU0_MCIO1_TX_N2
A16	GND	B16	GND
A17	PCIE_CPU0_MCIO1_RX_P3	B17	PCIE_CPU0_MCIO1_TX_P3
A18	PCIE_CPU0_MCIO1_RX_N3	B18	PCIE_CPU0_MCIO1_TX_N3
A19	GND	B19	GND
A20	PCIE_CPU0_MCIO1_RX_P4	B20	PCIE_CPU0_MCIO1_TX_P4
A21	PCIE_CPU0_MCIO1_RX_N4	B21	PCIE_CPU0_MCIO1_TX_N4
A22	GND	B22	GND
A23	PCIE_CPU0_MCIO1_RX_P5	B23	PCIE_CPU0_MCIO1_TX_P5
A24	PCIE_CPU0_MCIO1_RX_N5	B24	PCIE_CPU0_MCIO1_TX_N5
A25	GND	B25	GND
A26	MCIO1_NVME2_SMB_CLK	B26	MCIO_HP_SMB_ALERT_N
A27	MCIO1_NVME2_SMB_DATA	B27	NC
A28	GND	B28	GND
A29	CLK100M_BUFF_MCIO2_a_P	B29	PCIE_RST_MCIO1_NVME2_N
A30	CLK100M_BUFF_MCIO2_a_N	B30	MCIO1_NVME2_PRSNT_N
A31	GND	B31	GND
A32	PCIE_CPU0_MCIO1_RX_P6	B32	PCIE_CPU0_MCIO1_TX_P6
A33	PCIE_CPU0_MCIO1_RX_N6	B33	PCIE_CPU0_MCIO1_TX_N6
A34	GND	B34	GND
A35	PCIE_CPU0_MCIO1_RX_P7	B35	PCIE_CPU0_MCIO1_TX_P7
A36	PCIE_CPU0_MCIO1_RX_N7	B36	PCIE_CPU0_MCIO1_TX_N7
A37	GND	B37	GND

2.2.18 MCIO Connector (MCIO2)

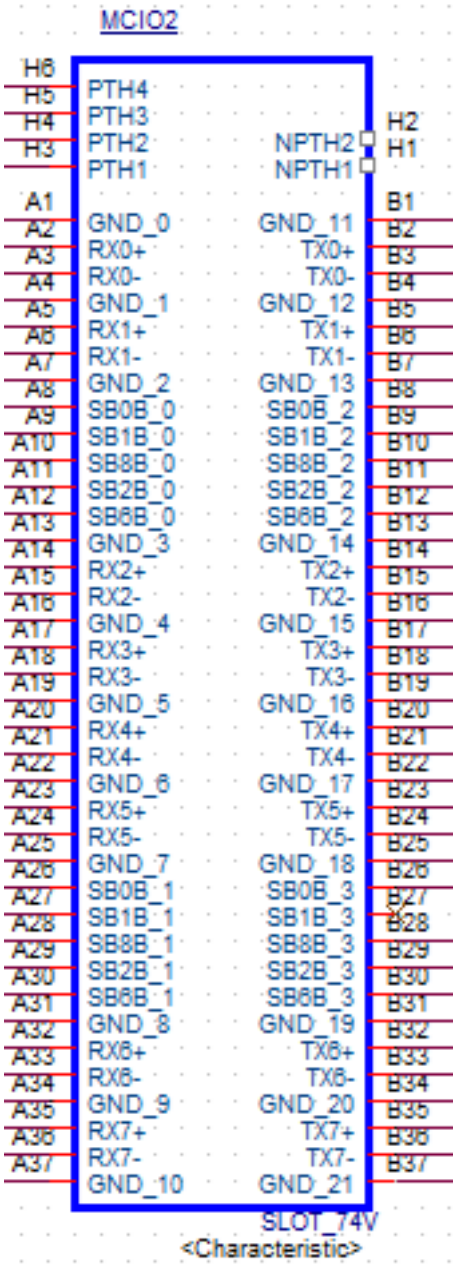


Table 2.18: MCIO Connector (MCIO2)

Pin	Signal	Pin	Signal
A1	GND	B1	GND
A2	PCIE_CPU0_MCIO2_RX_P0	B2	PCIE_CPU0_MCIO2_TX_P0
A3	PCIE_CPU0_MCIO2_RX_N0	B3	PCIE_CPU0_MCIO2_TX_N0
A4	GND	B4	GND
A5	PCIE_CPU0_MCIO2_RX_P1	B5	PCIE_CPU0_MCIO2_TX_P1
A6	PCIE_CPU0_MCIO2_RX_N1	B6	PCIE_CPU0_MCIO2_TX_N1
A7	GND	B7	GND
A8	MCIO2_NVME1_SMB_CLK	B8	MCIO2_HP_SMB_CLK
A9	MCIO2_NVME1_SMB_DATA	B9	MCIO2_HP_SMB_DATA
A10	GND	B10	GND
A11	CLK100M_BUFF_MCIO3_a_P	B11	PCIE_RST_MCIO2_NVME1_N
A12	CLK100M_BUFF_MCIO3_a_N	B12	MCIO2_NVME1_PRSNT_N
A13	GND	B13	GND
A14	PCIE_CPU0_MCIO2_RX_P2	B14	PCIE_CPU0_MCIO2_TX_P2
A15	PCIE_CPU0_MCIO2_RX_N2	B15	PCIE_CPU0_MCIO2_TX_N2
A16	GND	B16	GND
A17	PCIE_CPU0_MCIO2_RX_P3	B17	PCIE_CPU0_MCIO2_TX_P3
A18	PCIE_CPU0_MCIO2_RX_N3	B18	PCIE_CPU0_MCIO2_TX_N3
A19	GND	B19	GND
A20	PCIE_CPU0_MCIO2_RX_P4	B20	PCIE_CPU0_MCIO2_TX_P4
A21	PCIE_CPU0_MCIO2_RX_N4	B21	PCIE_CPU0_MCIO2_TX_N4
A22	GND	B22	GND
A23	PCIE_CPU0_MCIO2_RX_P5	B23	PCIE_CPU0_MCIO2_TX_P5
A24	PCIE_CPU0_MCIO2_RX_N5	B24	PCIE_CPU0_MCIO2_TX_N5
A25	GND	B25	GND
A26	MCIO2_NVME2_SMB_CLK	B26	MCIO_HP_SMB_ALERT_N
A27	MCIO2_NVME2_SMB_DATA	B27	NC
A28	GND	B28	GND
A29	CLK100M_BUFF_MCIO4_a_P	B29	PCIE_RST_MCIO2_NVME2_N
A30	CLK100M_BUFF_MCIO4_a_N	B30	MCIO2_NVME2_PRSNT_N
A31	GND	B31	GND
A32	PCIE_CPU0_MCIO2_RX_P6	B32	PCIE_CPU0_MCIO2_TX_P6
A33	PCIE_CPU0_MCIO2_RX_N6	B33	PCIE_CPU0_MCIO2_TX_N6
A34	GND	B34	GND
A35	PCIE_CPU0_MCIO2_RX_P7	B35	PCIE_CPU0_MCIO2_TX_P7
A36	PCIE_CPU0_MCIO2_RX_N7	B36	PCIE_CPU0_MCIO2_TX_N7
A37	GND	B37	GND

2.2.19 USB Connector (USB5)

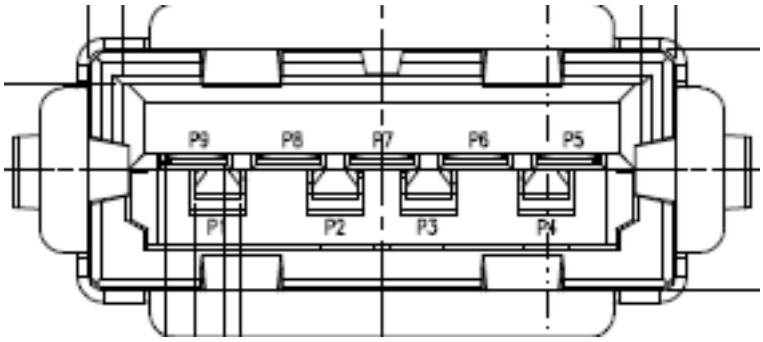


Table 2.19: USB Connector (USB5)

Pin	Signal	Pin	Signal
1	+V5_USB3_5	2	USB2_CPU0_USB3A1_a_N1
3	USB2_CPU0_USB3A1_a_P1	4	GND
5	USB3_CPU0_USB3A1_b_RX_N1	6	USB3_CPU0_USB3A1_b_RX_P1
7	GND	8	USB3_CPU0_USB3A1_b_TX_N1
9	USB3_CPU0_USB3A1_b_TX_P1		

2.2.20 DDR5 RDIMM Socket: A1(C0_DIMM_A1), B1(C0_DIMM_B1), D1(C0_DIMM_D1), E1(C0_DIMM_E1), F1(C0_DIMM_F1), H1(C0_DIMM_H1)

Please refer to JEDEC STANDARD

2.2.21 M.2 M-KEY Connector (M2_2280_1)

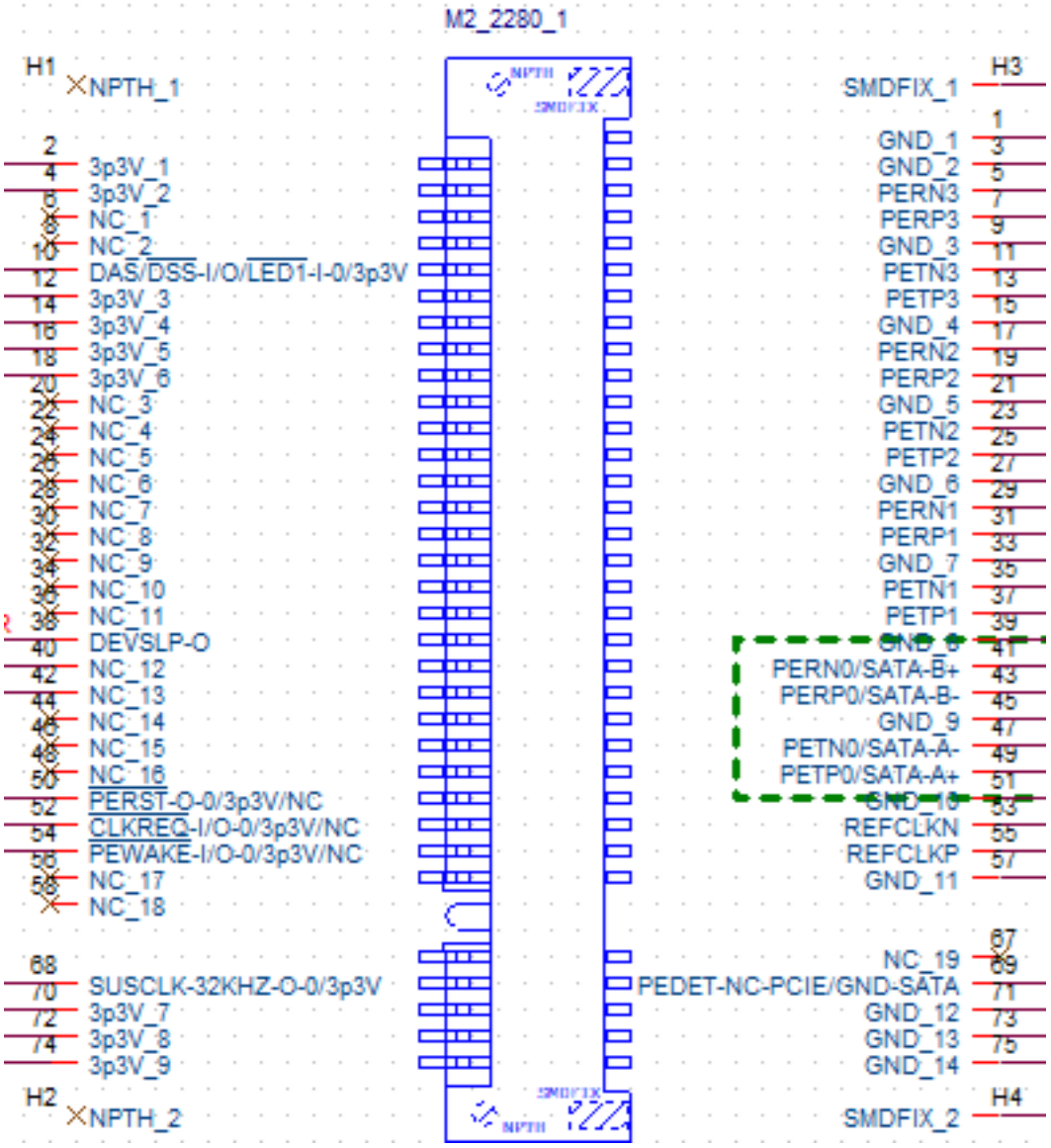


Table 2.20: M.2 M-KEY Connector (M2_2280_1)

Pin	Signal	Pin	Signal
1	M2_1_PRSNT_N	2	+V3.3
3	GND	4	+V3.3
5	PCIE_CPU0_M2_1_a_RX_N3	6	NC
7	PCIE_CPU0_M2_1_a_RX_P3	8	NC
9	GND	10	M2_1_LED_N
11	PCIE_CPU0_M2_1_a_TX_N3	12	+V3.3
13	PCIE_CPU0_M2_1_a_TX_P3	14	+V3.3
15	GND	16	+V3.3
17	PCIE_CPU0_M2_1_a_RX_N2	18	+V3.3
19	PCIE_CPU0_M2_1_a_RX_P2	20	NC
21	GND	22	NC
23	PCIE_CPU0_M2_1_a_TX_N2	24	NC
25	PCIE_CPU0_M2_1_a_TX_P2	26	NC

Table 2.20: M.2 M-KEY Connector (M2_2280_1)			
27	GND	28	NC
29	PCIE_CPU0_M2_1_a_RX_N1	30	NC
31	PCIE_CPU0_M2_1_a_RX_P1	32	NC
33	GND	34	NC
35	PCIE_CPU0_M2_1_a_TX_N1	36	NC
37	PCIE_CPU0_M2_1_a_TX_P1	38	DEVSLP_SSATA2_M2_1_R
39	GND	40	R_M2_1_SMB_CLK
41	PCIE_CPU0_M2_1_a_RX_P0	42	R_M2_1_SMB_DATA
43	PCIE_CPU0_M2_1_a_RX_N0	44	NC
45	GND	46	NC
47	PCIE_CPU0_M2_1_a_TX_N0	48	NC
49	PCIE_CPU0_M2_1_a_TX_P0	50	PCIE_RST_M2_1_N
51	GND	52	CLKREQ15_M2_1#
53	CLK100M_BUFF_M2_1_a_N	54	WAKE#
55	CLK100M_BUFF_M2_1_a_P	56	NC
57	GND	58	NC
59		60	
61		62	
63		64	
65		66	
67	NC	68	SUSCLK_32K_M2_1
69	M2_1_SSD_PEDET	70	+V3.3
71	GND	72	+V3.3
73	GND	74	+V3.3
75	GND		

2.2.22 M.2 M-KEY Connector (M2_2280_2)

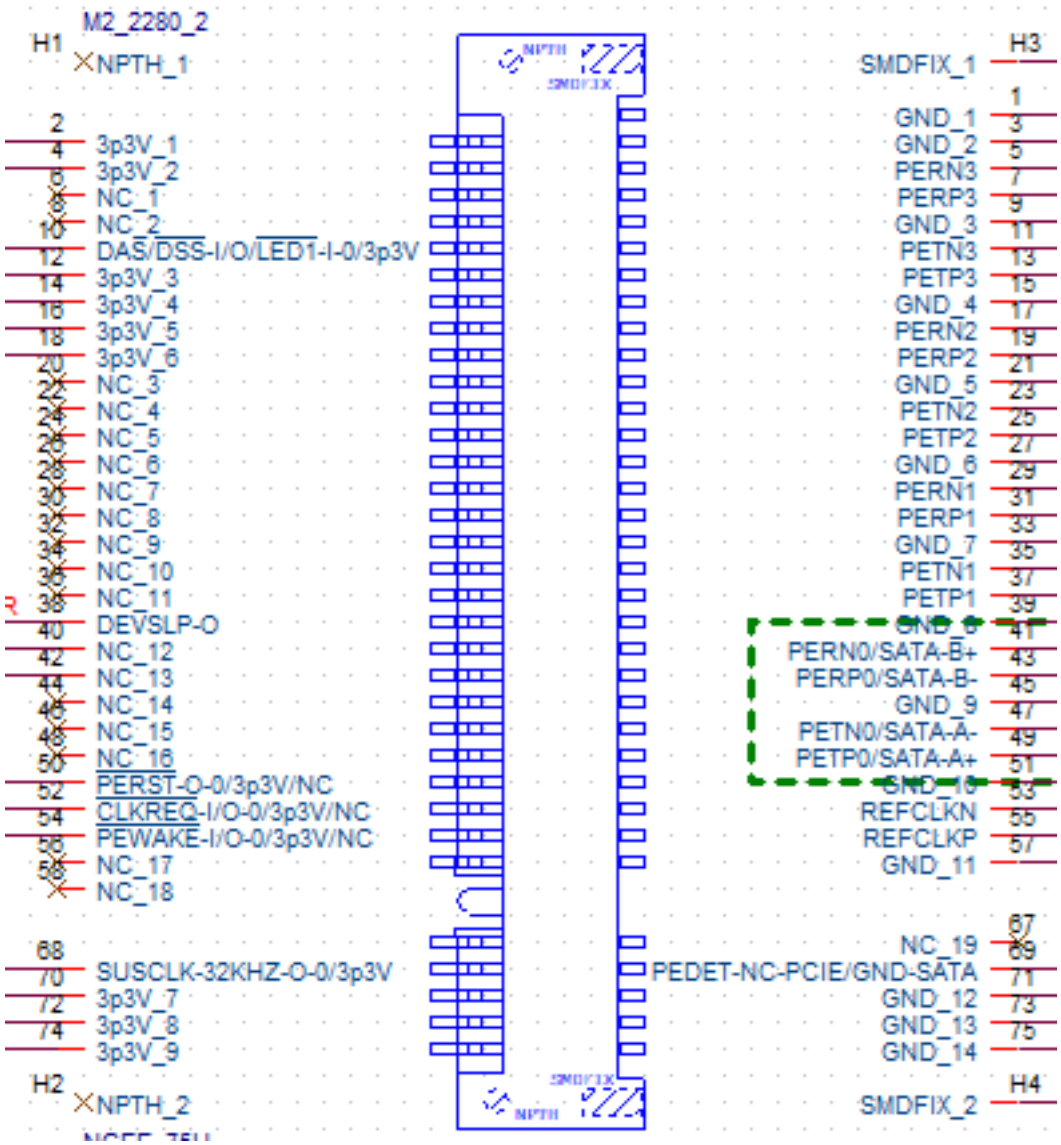


Table 2.21: M.2 M-KEY Connector (M2_2280_2)

Pin	Signal	Pin	Signal
1	M2_2_PRSNT_N	2	+V3.3
3	GND	4	+V3.3
5	PCIE_CPU0_M2_2_a_RX_N3	6	NC
7	PCIE_CPU0_M2_2_a_RX_P3	8	NC
9	GND	10	M2_2_LED_N
11	PCIE_CPU0_M2_2_a_TX_N3	12	+V3.3
13	PCIE_CPU0_M2_2_a_TX_P3	14	+V3.3
15	GND	16	+V3.3
17	PCIE_CPU0_M2_2_a_RX_N2	18	+V3.3
19	PCIE_CPU0_M2_2_a_RX_P2	20	NC
21	GND	22	NC
23	PCIE_CPU0_M2_2_a_TX_N2	24	NC
25	PCIE_CPU0_M2_2_a_TX_P2	26	NC

Table 2.21: M.2 M-KEY Connector (M2_2280_2)			
27	GND	28	NC
29	PCIE_CPU0_M2_2_a_RX_N1	30	NC
31	PCIE_CPU0_M2_2_a_RX_P1	32	NC
33	GND	34	NC
35	PCIE_CPU0_M2_2_a_TX_N1	36	NC
37	PCIE_CPU0_M2_2_a_TX_P1	38	DEVSLP_SSATA2_M2_2_R
39	GND	40	R_M2_2_SMB_CLK
41	PCIE_CPU0_M2_2_a_RX_P0	42	R_M2_2_SMB_DATA
43	PCIE_CPU0_M2_2_a_RX_N0	44	NC
45	GND	46	NC
47	PCIE_CPU0_M2_2_a_TX_N0	48	NC
49	PCIE_CPU0_M2_2_a_TX_P0	50	PCIE_RST_M2_2_N
51	GND	52	CLKREQ15_M2_2#
53	CLK100M_BUFF_M2_2_a_N	54	WAKE#
55	CLK100M_BUFF_M2_2_a_P	56	NC
57	GND	58	NC
59		60	
61		62	
63		64	
65		66	
67	NC	68	SUSCLK_32K_M2_2
69	M2_2_SSD_PEDET	70	+V3.3
71	GND	72	+V3.3
73	GND	74	+V3.3
75	GND		

2.2.23 HDT Debug Connector (HDT1)

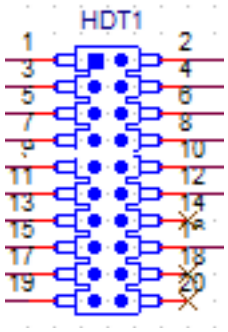


Table 2.22: HDT Debug Connector (HDT1)

Pin	Signal	Pin	Signal
1	+V1.8_AUX_CPU0	2	CPU0_TCK
3	GND	4	CPU0_TMS
5	GND	6	CPU0_TDI
7	GND	8	CPU0_TDO
9	CPU0_TRST_N	10	CPU0_HDT_CONN_PWROK
11	CPU0_XTRIG_L6	12	CPU0_HDT_CONN_RESET_L
13	CPU0_XTRIG_L7	14	NC
15	CPU0_XTRIG_L5	16	CPU0_DBREQ_N
17	GND	18	NC
19	+V1.8_AUX_CPU0	20	NC

2.2.24 SPI BIOS FLASH Socket (BIOS_SKT1)

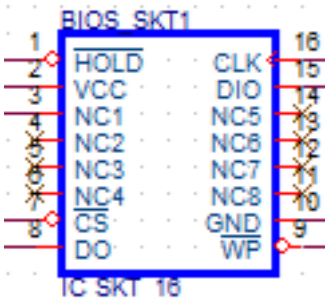


Table 2.23: SPI BIOS FLASH Socket (BIOS_SKT1)

Pin	Signal	Pin	Signal
1	SPI_SKT_HOLD#_R	9	SPI_SKT_WP#_R
2	+V1.8_SPI	10	GND
3	NC	11	NC
4	NC	12	NC
5	NC	13	NC
6	NC	14	NC
7	SPI_SKT_CS#0_R	15	SPI_SKT_MOSI_R
8	SPI_SKT_MISO_R	16	SPI_SKT_CLK_R

2.2.25 PCI Express X16 Slot (PCIEX16_1)

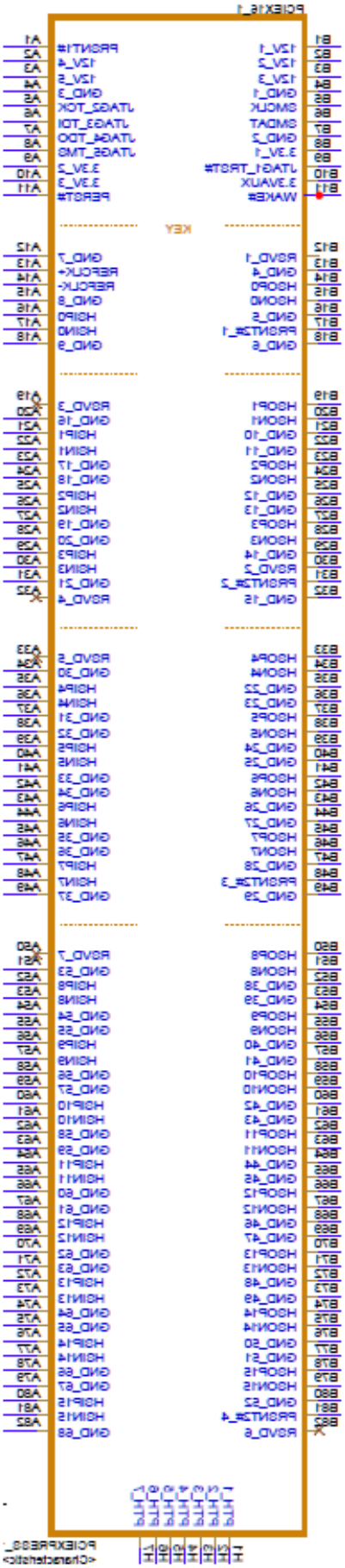


Table 2.24: PCI Express X16 Slot (PCIEX16_1)			
Pin	**Signal**	**Pin**	**Signal**
A1	GND	B1	+V12
A2	+V12	B2	+V12
A3	+V12	B3	+V12
A4	GND	B4	GND
A5	GND	B5	SMB_CPU_SCL_3.3V_AUX
A6	+V3.3_SLOT	B6	SMB_CPU_SDA_3.3V_AUX
A7	+V3.3_SLOT	B7	GND
A8	+V3.3_SLOT	B8	+V3.3_SLOT
A9	+V3.3_SLOT	B9	GND
A10	+V3.3_SLOT	B10	+V3.3_AUX
A11	PCIE_RST_SLOT1_N	B11	WAKE#
A12	GND	B12	NC
A13	CLK100M_CPU0_SLOT1_a_P	B13	GND
A14	CLK100M_CPU0_SLOT1_a_N	B14	PCIE_CPU0_SLOT1_TX_P0
A15	GND	B15	PCIE_CPU0_SLOT1_TX_N0
A16	PCIE_CPU0_SLOT1_RX_P0	B16	GND
A17	PCIE_CPU0_SLOT1_RX_N0	B17	SLOT1_PRSNT_N
A18	GND	B18	GND
A19	NC	B19	PCIE_CPU0_SLOT1_TX_P1
A20	GND	B20	PCIE_CPU0_SLOT1_TX_N1
A21	PCIE_CPU0_SLOT1_RX_P1	B21	GND
A22	PCIE_CPU0_SLOT1_RX_N1	B22	GND
A23	GND	B23	PCIE_CPU0_SLOT1_TX_P2
A24	GND	B24	PCIE_CPU0_SLOT1_TX_N2
A25	PCIE_CPU0_SLOT1_RX_P2	B25	GND
A26	PCIE_CPU0_SLOT1_RX_N2	B26	GND
A27	GND	B27	PCIE_CPU0_SLOT1_TX_P3
A28	GND	B28	PCIE_CPU0_SLOT1_TX_N3
A29	PCIE_CPU0_SLOT1_RX_P3	B29	GND
A30	PCIE_CPU0_SLOT1_RX_N3	B30	SLOT1_PH_PB_N
A31	GND	B31	SLOT1_PRSNT_N
A32	NC	B32	GND
A33	NC	B33	PCIE_CPU0_SLOT1_TX_P4
A34	GND	B34	PCIE_CPU0_SLOT1_TX_N4
A35	PCIE_CPU0_SLOT1_RX_P4	B35	GND
A36	PCIE_CPU0_SLOT1_RX_N4	B36	GND
A37	GND	B37	PCIE_CPU0_SLOT1_TX_P5
A38	GND	B38	PCIE_CPU0_SLOT1_TX_N5
A39	PCIE_CPU0_SLOT1_RX_P5	B39	GND
A40	PCIE_CPU0_SLOT1_RX_N5	B40	GND
A41	GND	B41	PCIE_CPU0_SLOT1_TX_P6
A42	GND	B42	PCIE_CPU0_SLOT1_TX_N6
A43	PCIE_CPU0_SLOT1_RX_P6	B43	GND
A44	PCIE_CPU0_SLOT1_RX_N6	B44	GND
A45	GND	B45	PCIE_CPU0_SLOT1_TX_P7

Table 2.24: PCI Express X16 Slot (PCIEX16_1)			
A46	GND	B46	PCIE_CPU0_SLOT1_TX_N7
A47	PCIE_CPU0_SLOT1_RX_P7	B47	GND
A48	PCIE_CPU0_SLOT1_RX_N7	B48	SLOT1_PRSNT_N
A49	GND	B49	GND
A50	GND	B50	PCIE_CPU0_SLOT1_TX_P8
A51	GND	B51	PCIE_CPU0_SLOT1_TX_N8
A52	PCIE_CPU0_SLOT1_RX_P8	B52	GND
A53	PCIE_CPU0_SLOT1_RX_N8	B53	GND
A54	GND	B54	PCIE_CPU0_SLOT1_TX_P9
A55	GND	B55	PCIE_CPU0_SLOT1_TX_N9
A56	PCIE_CPU0_SLOT1_RX_P9	B56	GND
A57	PCIE_CPU0_SLOT1_RX_N9	B57	GND
A58	GND	B58	PCIE_CPU0_SLOT1_TX_P10
A59	GND	B59	PCIE_CPU0_SLOT1_TX_N10
A60	PCIE_CPU0_SLOT1_RX_P10	B60	GND
A61	PCIE_CPU0_SLOT1_RX_N10	B61	GND
A62	GND	B62	PCIE_CPU0_SLOT1_TX_P11
A63	GND	B63	PCIE_CPU0_SLOT1_TX_N11
A64	PCIE_CPU0_SLOT1_RX_P11	B64	GND
A65	PCIE_CPU0_SLOT1_RX_N11	B65	GND
A66	GND	B66	PCIE_CPU0_SLOT1_TX_P12
A67	GND	B67	PCIE_CPU0_SLOT1_TX_N12
A68	PCIE_CPU0_SLOT1_RX_P12	B68	GND
A69	PCIE_CPU0_SLOT1_RX_N12	B69	GND
A70	GND	B70	PCIE_CPU0_SLOT1_TX_P13
A71	GND	B71	PCIE_CPU0_SLOT1_TX_N13
A72	PCIE_CPU0_SLOT1_RX_P13	B72	GND
A73	PCIE_CPU0_SLOT1_RX_N13	B73	GND
A74	GND	B74	PCIE_CPU0_SLOT1_TX_P14
A75	GND	B75	PCIE_CPU0_SLOT1_TX_N14
A76	PCIE_CPU0_SLOT1_RX_P14	B76	GND
A77	PCIE_CPU0_SLOT1_RX_N14	B77	GND
A78	GND	B78	PCIE_CPU0_SLOT1_TX_P15
A79	GND	B79	PCIE_CPU0_SLOT1_TX_N15
A80	PCIE_CPU0_SLOT1_RX_P15	B80	GND
A81	PCIE_CPU0_SLOT1_RX_N15	B81	SLOT1_PRSNT_N
A82	GND	B82	NC

2.2.26 PCI Express X16 Slot (PCIEX16_2)

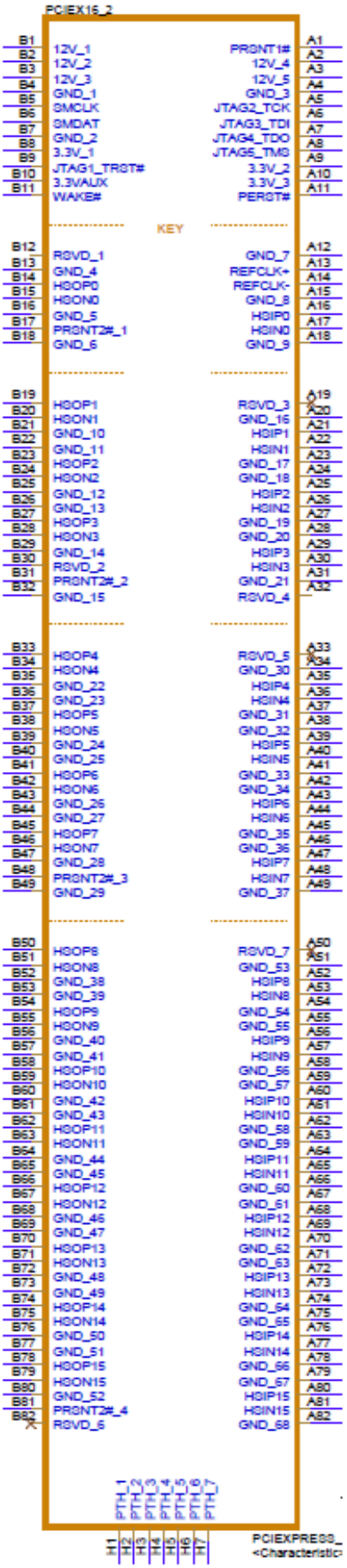


Table 2.25: PCI Express X16 Slot (PCIEX16_2)			
Pin	**Signal**	**Pin**	**Signal**
A1	GND	B1	+V12
A2	+V12	B2	+V12
A3	+V12	B3	+V12
A4	GND	B4	GND
A5	GND	B5	SMB_CPU_SCL_3.3V_AUX
A6	+V3.3_SLOT	B6	SMB_CPU_SDA_3.3V_AUX
A7	+V3.3_SLOT	B7	GND
A8	+V3.3_SLOT	B8	+V3.3_SLOT
A9	+V3.3_SLOT	B9	GND
A10	+V3.3_SLOT	B10	+V3.3_AUX
A11	PCIE_RST_SLOT2_N	B11	WAKE#
A12	GND	B12	NC
A13	CLK100M_CPU0_SLOT2_a_P	B13	GND
A14	CLK100M_CPU0_SLOT2_a_N	B14	PCIE_CPU0_SLOT2_TX_P0
A15	GND	B15	PCIE_CPU0_SLOT2_TX_N0
A16	PCIE_CPU0_SLOT2_RX_P0	B16	GND
A17	PCIE_CPU0_SLOT2_RX_N0	B17	SLOT1_PRSNT_N
A18	GND	B18	GND
A19	NC	B19	PCIE_CPU0_SLOT2_TX_P1
A20	GND	B20	PCIE_CPU0_SLOT2_TX_N1
A21	PCIE_CPU0_SLOT2_RX_P1	B21	GND
A22	PCIE_CPU0_SLOT2_RX_N1	B22	GND
A23	GND	B23	PCIE_CPU0_SLOT2_TX_P2
A24	GND	B24	PCIE_CPU0_SLOT2_TX_N2
A25	PCIE_CPU0_SLOT2_RX_P2	B25	GND
A26	PCIE_CPU0_SLOT2_RX_N2	B26	GND
A27	GND	B27	PCIE_CPU0_SLOT2_TX_P3
A28	GND	B28	PCIE_CPU0_SLOT2_TX_N3
A29	PCIE_CPU0_SLOT2_RX_P3	B29	GND
A30	PCIE_CPU0_SLOT2_RX_N3	B30	SLOT2_PH_PB_N
A31	GND	B31	SLOT2_PRSNT_N
A32	NC	B32	GND
A33	NC	B33	PCIE_CPU0_SLOT2_TX_P4
A34	GND	B34	PCIE_CPU0_SLOT2_TX_N4
A35	PCIE_CPU0_SLOT2_RX_P4	B35	GND
A36	PCIE_CPU0_SLOT2_RX_N4	B36	GND
A37	GND	B37	PCIE_CPU0_SLOT2_TX_P5
A38	GND	B38	PCIE_CPU0_SLOT2_TX_N5
A39	PCIE_CPU0_SLOT2_RX_P5	B39	GND
A40	PCIE_CPU0_SLOT2_RX_N5	B40	GND
A41	GND	B41	PCIE_CPU0_SLOT2_TX_P6
A42	GND	B42	PCIE_CPU0_SLOT2_TX_N6
A43	PCIE_CPU0_SLOT2_RX_P6	B43	GND
A44	PCIE_CPU0_SLOT2_RX_N6	B44	GND
A45	GND	B45	PCIE_CPU0_SLOT2_TX_P7

Table 2.25: PCI Express X16 Slot (PCIEX16_2)			
A46	GND	B46	PCIE_CPU0_SLOT2_TX_N7
A47	PCIE_CPU0_SLOT2_RX_P7	B47	GND
A48	PCIE_CPU0_SLOT2_RX_N7	B48	SLOT2_PRSNT_N
A49	GND	B49	GND
A50	GND	B50	PCIE_CPU0_SLOT2_TX_P8
A51	GND	B51	PCIE_CPU0_SLOT2_TX_N8
A52	PCIE_CPU0_SLOT2_RX_P8	B52	GND
A53	PCIE_CPU0_SLOT2_RX_N8	B53	GND
A54	GND	B54	PCIE_CPU0_SLOT2_TX_P9
A55	GND	B55	PCIE_CPU0_SLOT2_TX_N9
A56	PCIE_CPU0_SLOT2_RX_P9	B56	GND
A57	PCIE_CPU0_SLOT2_RX_N9	B57	GND
A58	GND	B58	PCIE_CPU0_SLOT2_TX_P10
A59	GND	B59	PCIE_CPU0_SLOT2_TX_N10
A60	PCIE_CPU0_SLOT2_RX_P10	B60	GND
A61	PCIE_CPU0_SLOT2_RX_N10	B61	GND
A62	GND	B62	PCIE_CPU0_SLOT2_TX_P11
A63	GND	B63	PCIE_CPU0_SLOT2_TX_N11
A64	PCIE_CPU0_SLOT2_RX_P11	B64	GND
A65	PCIE_CPU0_SLOT2_RX_N11	B65	GND
A66	GND	B66	PCIE_CPU0_SLOT2_TX_P12
A67	GND	B67	PCIE_CPU0_SLOT2_TX_N12
A68	PCIE_CPU0_SLOT2_RX_P12	B68	GND
A69	PCIE_CPU0_SLOT2_RX_N12	B69	GND
A70	GND	B70	PCIE_CPU0_SLOT2_TX_P13
A71	GND	B71	PCIE_CPU0_SLOT2_TX_N13
A72	PCIE_CPU0_SLOT2_RX_P13	B72	GND
A73	PCIE_CPU0_SLOT2_RX_N13	B73	GND
A74	GND	B74	PCIE_CPU0_SLOT2_TX_P14
A75	GND	B75	PCIE_CPU0_SLOT2_TX_N14
A76	PCIE_CPU0_SLOT2_RX_P14	B76	GND
A77	PCIE_CPU0_SLOT2_RX_N14	B77	GND
A78	GND	B78	PCIE_CPU0_SLOT2_TX_P15
A79	GND	B79	PCIE_CPU0_SLOT2_TX_N15
A80	PCIE_CPU0_SLOT2_RX_P15	B80	GND
A81	PCIE_CPU0_SLOT2_RX_N15	B81	SLOT2_PRSNT_N
A82	GND	B82	NC

2.2.27 PCI Express X16 Slot (PCIEX16_3)

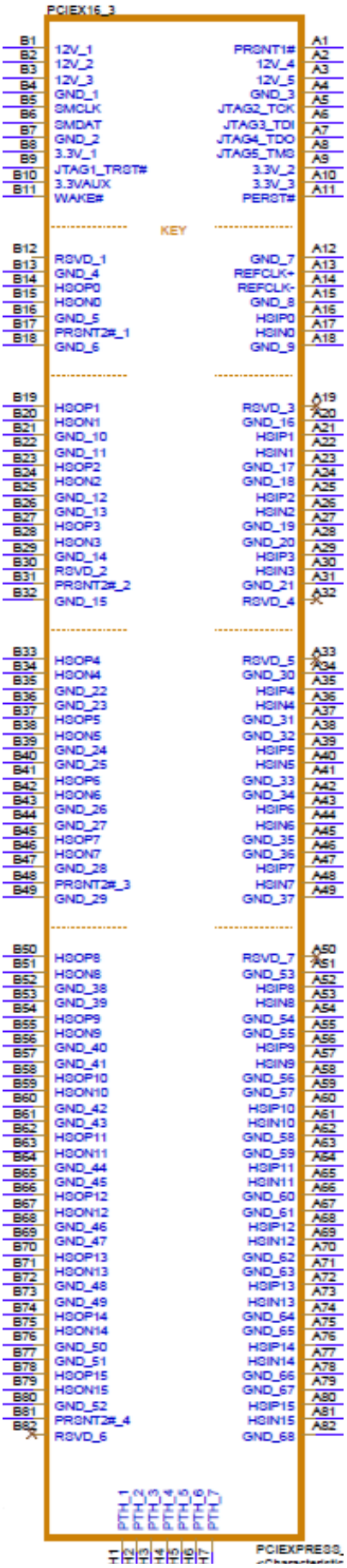


Table 2.26: PCI Express X16 Slot (PCIEX16_3)			
Pin	**Signal**	**Pin**	**Signal**
A1	GND	B1	+V12
A2	+V12	B2	+V12
A3	+V12	B3	+V12
A4	GND	B4	GND
A5	GND	B5	SMB_CPU_SCL_3.3V_AUX
A6	+V3.3_SLOT	B6	SMB_CPU_SDA_3.3V_AUX
A7	+V3.3_SLOT	B7	GND
A8	+V3.3_SLOT	B8	+V3.3_SLOT
A9	+V3.3_SLOT	B9	GND
A10	+V3.3_SLOT	B10	+V3.3_AUX
A11	PCIE_RST_SLOT3_N	B11	WAKE#
A12	GND	B12	NC
A13	CLK100M_CPU0_SLOT3_a_P	B13	GND
A14	CLK100M_CPU0_SLOT3_a_N	B14	PCIE_CPU0_SLOT3_TX_P0
A15	GND	B15	PCIE_CPU0_SLOT3_TX_N0
A16	PCIE_CPU0_SLOT3_RX_P0	B16	GND
A17	PCIE_CPU0_SLOT3_RX_N0	B17	SLOT1_PRSNT_N
A18	GND	B18	GND
A19	NC	B19	PCIE_CPU0_SLOT3_TX_P1
A20	GND	B20	PCIE_CPU0_SLOT3_TX_N1
A21	PCIE_CPU0_SLOT3_RX_P1	B21	GND
A22	PCIE_CPU0_SLOT3_RX_N1	B22	GND
A23	GND	B23	PCIE_CPU0_SLOT3_TX_P2
A24	GND	B24	PCIE_CPU0_SLOT3_TX_N2
A25	PCIE_CPU0_SLOT3_RX_P2	B25	GND
A26	PCIE_CPU0_SLOT3_RX_N2	B26	GND
A27	GND	B27	PCIE_CPU0_SLOT3_TX_P3
A28	GND	B28	PCIE_CPU0_SLOT3_TX_N3
A29	PCIE_CPU0_SLOT3_RX_P3	B29	GND
A30	PCIE_CPU0_SLOT3_RX_N3	B30	SLOT2_PH_PB_N
A31	GND	B31	SLOT2_PRSNT_N
A32	NC	B32	GND
A33	NC	B33	PCIE_CPU0_SLOT3_TX_P4
A34	GND	B34	PCIE_CPU0_SLOT3_TX_N4
A35	PCIE_CPU0_SLOT3_RX_P4	B35	GND
A36	PCIE_CPU0_SLOT3_RX_N4	B36	GND
A37	GND	B37	PCIE_CPU0_SLOT3_TX_P5
A38	GND	B38	PCIE_CPU0_SLOT3_TX_N5
A39	PCIE_CPU0_SLOT3_RX_P5	B39	GND
A40	PCIE_CPU0_SLOT3_RX_N5	B40	GND
A41	GND	B41	PCIE_CPU0_SLOT3_TX_P6
A42	GND	B42	PCIE_CPU0_SLOT3_TX_N6
A43	PCIE_CPU0_SLOT3_RX_P6	B43	GND
A44	PCIE_CPU0_SLOT3_RX_N6	B44	GND
A45	GND	B45	PCIE_CPU0_SLOT3_TX_P7

Table 2.26: PCI Express X16 Slot (PCIEX16_3)			
A46	GND	B46	PCIE_CPU0_SLOT3_TX_N7
A47	PCIE_CPU0_SLOT3_RX_P7	B47	GND
A48	PCIE_CPU0_SLOT3_RX_N7	B48	SLOT2_PRSNT_N
A49	GND	B49	GND
A50	GND	B50	PCIE_CPU0_SLOT3_TX_P8
A51	GND	B51	PCIE_CPU0_SLOT3_TX_N8
A52	PCIE_CPU0_SLOT3_RX_P8	B52	GND
A53	PCIE_CPU0_SLOT3_RX_N8	B53	GND
A54	GND	B54	PCIE_CPU0_SLOT3_TX_P9
A55	GND	B55	PCIE_CPU0_SLOT3_TX_N9
A56	PCIE_CPU0_SLOT3_RX_P9	B56	GND
A57	PCIE_CPU0_SLOT3_RX_N9	B57	GND
A58	GND	B58	PCIE_CPU0_SLOT3_TX_P10
A59	GND	B59	PCIE_CPU0_SLOT3_TX_N10
A60	PCIE_CPU0_SLOT3_RX_P10	B60	GND
A61	PCIE_CPU0_SLOT3_RX_N10	B61	GND
A62	GND	B62	PCIE_CPU0_SLOT3_TX_P11
A63	GND	B63	PCIE_CPU0_SLOT3_TX_N11
A64	PCIE_CPU0_SLOT3_RX_P11	B64	GND
A65	PCIE_CPU0_SLOT3_RX_N11	B65	GND
A66	GND	B66	PCIE_CPU0_SLOT3_TX_P12
A67	GND	B67	PCIE_CPU0_SLOT3_TX_N12
A68	PCIE_CPU0_SLOT3_RX_P12	B68	GND
A69	PCIE_CPU0_SLOT3_RX_N12	B69	GND
A70	GND	B70	PCIE_CPU0_SLOT3_TX_P13
A71	GND	B71	PCIE_CPU0_SLOT3_TX_N13
A72	PCIE_CPU0_SLOT3_RX_P13	B72	GND
A73	PCIE_CPU0_SLOT3_RX_N13	B73	GND
A74	GND	B74	PCIE_CPU0_SLOT3_TX_P14
A75	GND	B75	PCIE_CPU0_SLOT3_TX_N14
A76	PCIE_CPU0_SLOT3_RX_P14	B76	GND
A77	PCIE_CPU0_SLOT3_RX_N14	B77	GND
A78	GND	B78	PCIE_CPU0_SLOT3_TX_P15
A79	GND	B79	PCIE_CPU0_SLOT3_TX_N15
A80	PCIE_CPU0_SLOT3_RX_P15	B80	GND
A81	PCIE_CPU0_SLOT3_RX_N15	B81	SLOT3_PRSNT_N
A82	GND	B82	NC

2.2.28 PCI Express X16 Slot (PCIEX16_4)

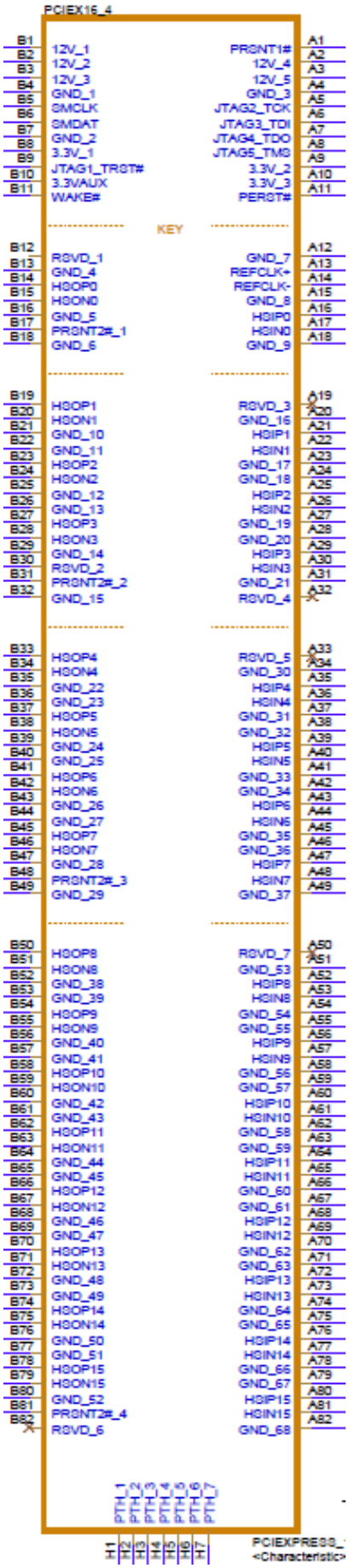


Table 2.27: PCI Express x16 Slot (PCIEX16_4)			
Pin	**Signal**	**Pin**	**Signal**
A1	GND	B1	+V12
A2	+V12	B2	+V12
A3	+V12	B3	+V12
A4	GND	B4	GND
A5	GND	B5	SMB_CPU_SCL_3.3V_AUX
A6	+V3.3_SLOT	B6	SMB_CPU_SDA_3.3V_AUX
A7	+V3.3_SLOT	B7	GND
A8	+V3.3_SLOT	B8	+V3.3_SLOT
A9	+V3.3_SLOT	B9	GND
A10	+V3.3_SLOT	B10	+V3.3_AUX
A11	PCIE_RST_SLOT4_N	B11	WAKE#
A12	GND	B12	NC
A13	CLK100M_CPU0_SLOT4_a_P	B13	GND
A14	CLK100M_CPU0_SLOT4_a_N	B14	PCIE_CPU0_SLOT4_TX_P0
A15	GND	B15	PCIE_CPU0_SLOT4_TX_N0
A16	PCIE_CPU0_SLOT4_RX_P0	B16	GND
A17	PCIE_CPU0_SLOT4_RX_N0	B17	SLOT1_PRSNT_N
A18	GND	B18	GND
A19	NC	B19	PCIE_CPU0_SLOT4_TX_P1
A20	GND	B20	PCIE_CPU0_SLOT4_TX_N1
A21	PCIE_CPU0_SLOT4_RX_P1	B21	GND
A22	PCIE_CPU0_SLOT4_RX_N1	B22	GND
A23	GND	B23	PCIE_CPU0_SLOT4_TX_P2
A24	GND	B24	PCIE_CPU0_SLOT4_TX_N2
A25	PCIE_CPU0_SLOT4_RX_P2	B25	GND
A26	PCIE_CPU0_SLOT4_RX_N2	B26	GND
A27	GND	B27	PCIE_CPU0_SLOT4_TX_P3
A28	GND	B28	PCIE_CPU0_SLOT4_TX_N3
A29	PCIE_CPU0_SLOT4_RX_P3	B29	GND
A30	PCIE_CPU0_SLOT4_RX_N3	B30	SLOT2_PH_PB_N
A31	GND	B31	SLOT2_PRSNT_N
A32	NC	B32	GND
A33	NC	B33	PCIE_CPU0_SLOT4_TX_P4
A34	GND	B34	PCIE_CPU0_SLOT4_TX_N4
A35	PCIE_CPU0_SLOT4_RX_P4	B35	GND
A36	PCIE_CPU0_SLOT4_RX_N4	B36	GND
A37	GND	B37	PCIE_CPU0_SLOT4_TX_P5
A38	GND	B38	PCIE_CPU0_SLOT4_TX_N5
A39	PCIE_CPU0_SLOT4_RX_P5	B39	GND
A40	PCIE_CPU0_SLOT4_RX_N5	B40	GND
A41	GND	B41	PCIE_CPU0_SLOT4_TX_P6
A42	GND	B42	PCIE_CPU0_SLOT4_TX_N6
A43	PCIE_CPU0_SLOT4_RX_P6	B43	GND
A44	PCIE_CPU0_SLOT4_RX_N6	B44	GND
A45	GND	B45	PCIE_CPU0_SLOT4_TX_P7

Table 2.27: PCI Express x16 Slot (PCIEX16_4)			
A46	GND	B46	PCIE_CPU0_SLOT4_TX_N7
A47	PCIE_CPU0_SLOT4_RX_P7	B47	GND
A48	PCIE_CPU0_SLOT4_RX_N7	B48	SLOT2_PRSNT_N
A49	GND	B49	GND
A50	GND	B50	PCIE_CPU0_SLOT4_TX_P8
A51	GND	B51	PCIE_CPU0_SLOT4_TX_N8
A52	PCIE_CPU0_SLOT4_RX_P8	B52	GND
A53	PCIE_CPU0_SLOT4_RX_N8	B53	GND
A54	GND	B54	PCIE_CPU0_SLOT4_TX_P9
A55	GND	B55	PCIE_CPU0_SLOT4_TX_N9
A56	PCIE_CPU0_SLOT4_RX_P9	B56	GND
A57	PCIE_CPU0_SLOT4_RX_N9	B57	GND
A58	GND	B58	PCIE_CPU0_SLOT4_TX_P10
A59	GND	B59	PCIE_CPU0_SLOT4_TX_N10
A60	PCIE_CPU0_SLOT4_RX_P10	B60	GND
A61	PCIE_CPU0_SLOT4_RX_N10	B61	GND
A62	GND	B62	PCIE_CPU0_SLOT4_TX_P11
A63	GND	B63	PCIE_CPU0_SLOT4_TX_N11
A64	PCIE_CPU0_SLOT4_RX_P11	B64	GND
A65	PCIE_CPU0_SLOT4_RX_N11	B65	GND
A66	GND	B66	PCIE_CPU0_SLOT4_TX_P12
A67	GND	B67	PCIE_CPU0_SLOT4_TX_N12
A68	PCIE_CPU0_SLOT4_RX_P12	B68	GND
A69	PCIE_CPU0_SLOT4_RX_N12	B69	GND
A70	GND	B70	PCIE_CPU0_SLOT4_TX_P13
A71	GND	B71	PCIE_CPU0_SLOT4_TX_N13
A72	PCIE_CPU0_SLOT4_RX_P13	B72	GND
A73	PCIE_CPU0_SLOT4_RX_N13	B73	GND
A74	GND	B74	PCIE_CPU0_SLOT4_TX_P14
A75	GND	B75	PCIE_CPU0_SLOT4_TX_N14
A76	PCIE_CPU0_SLOT4_RX_P14	B76	GND
A77	PCIE_CPU0_SLOT4_RX_N14	B77	GND
A78	GND	B78	PCIE_CPU0_SLOT4_TX_P15
A79	GND	B79	PCIE_CPU0_SLOT4_TX_N15
A80	PCIE_CPU0_SLOT4_RX_P15	B80	GND
A81	PCIE_CPU0_SLOT4_RX_N15	B81	SLOT4_PRSNT_N
A82	GND	B82	NC

Chapter 3

BIOS Operation

3.1 Introduction

With the AMI BIOS Setup program, you can modify BIOS settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning special features on or off. This chapter describes the basic navigation of the AIMB-593 setup screens.

3.2 BIOS Setup

The AIMB-593 Series system has AMI BIOS built in, with a CMOS SETUP utility that allows users to configure required settings or to activate certain system features. The CMOS SETUP saves the configuration in the CMOS RAM of the motherboard. When the power is turned off, the battery on the board supplies the necessary power to preserve the CMOS RAM.

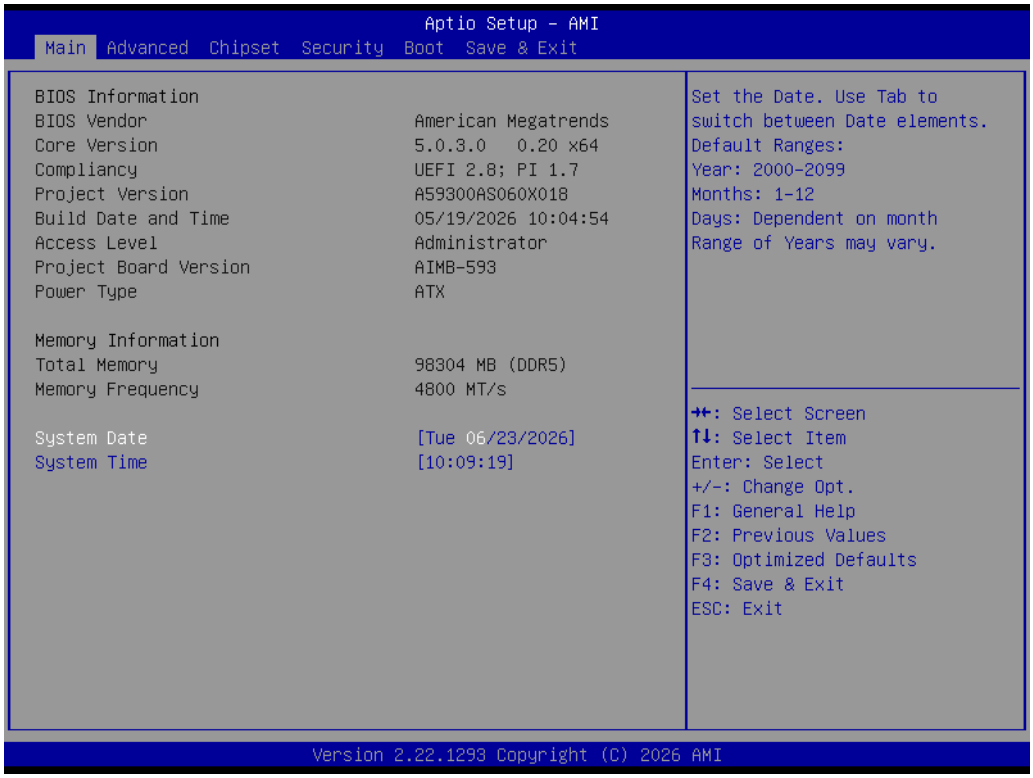
When the power is turned on, press the <Del> button during the BIOS POST (Power-On Self-Test) to access the CMOS SETUP screen.

Table 3.1: Control Keys

< ↑ >< ↓ >< ← >< → >	Move to select item
<Enter>	Select item
<Esc>	Main Menu - Quit and not save changes into CMOS Sub-Menu - Exit current page and return to Main Menu
<Page Up/+>	Increase the numeric value or make changes
<Page Down/->	Decrease the numeric value or make changes
<F1>	General help, for Setup Sub Menu
<F2>	Item Help
<F5>	Loads previous values
<F7>	Load Setup Defaults
<F10>	Save all CMOS changes

3.2.1 Main Menu

Press <Del> to enter the AMI BIOS CMOS Setup Utility. The Main Menu will appear on the screen. Use the arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.



The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the legend.

Above the legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

- **System Time/System Date**

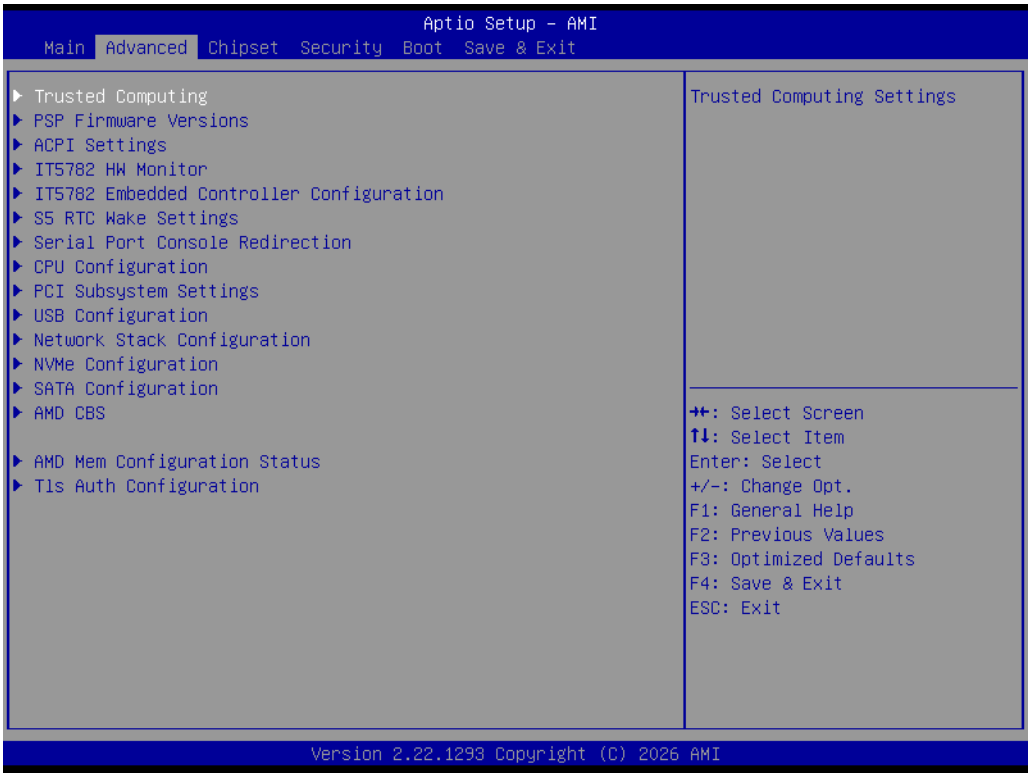
  Use this option to change the system time and date. Highlight the System Time or System Date using the keys. Enter new values via the keyboard. Press the or keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

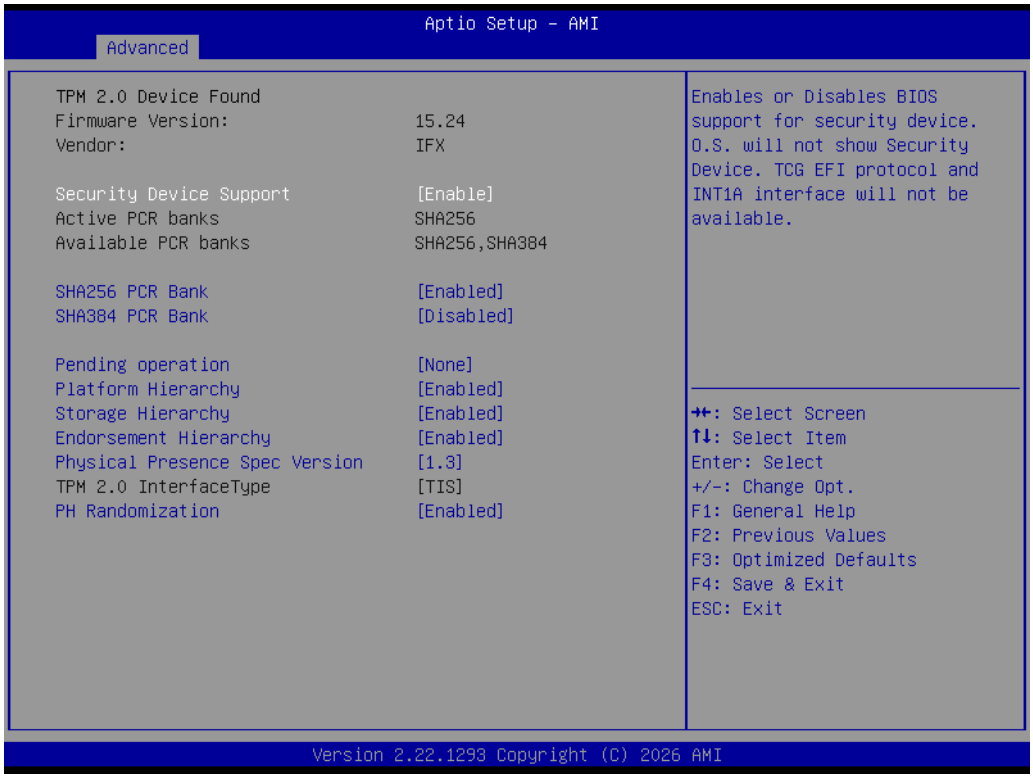
3.2.2 Advanced BIOS Features

Select the Advanced tab from the AIMB-593 setup menu to enter the Advanced BIOS setup page. Users can select any item in the left frame of the screen, such as CPU configuration. Select an Advanced BIOS setup option by highlighting the text using the keys. All Advanced BIOS setup options are described in this section. The Advanced BIOS setup menu screen is shown below. The sub-menus are described in the following pages.

3.2.2.1 Trusted Computing

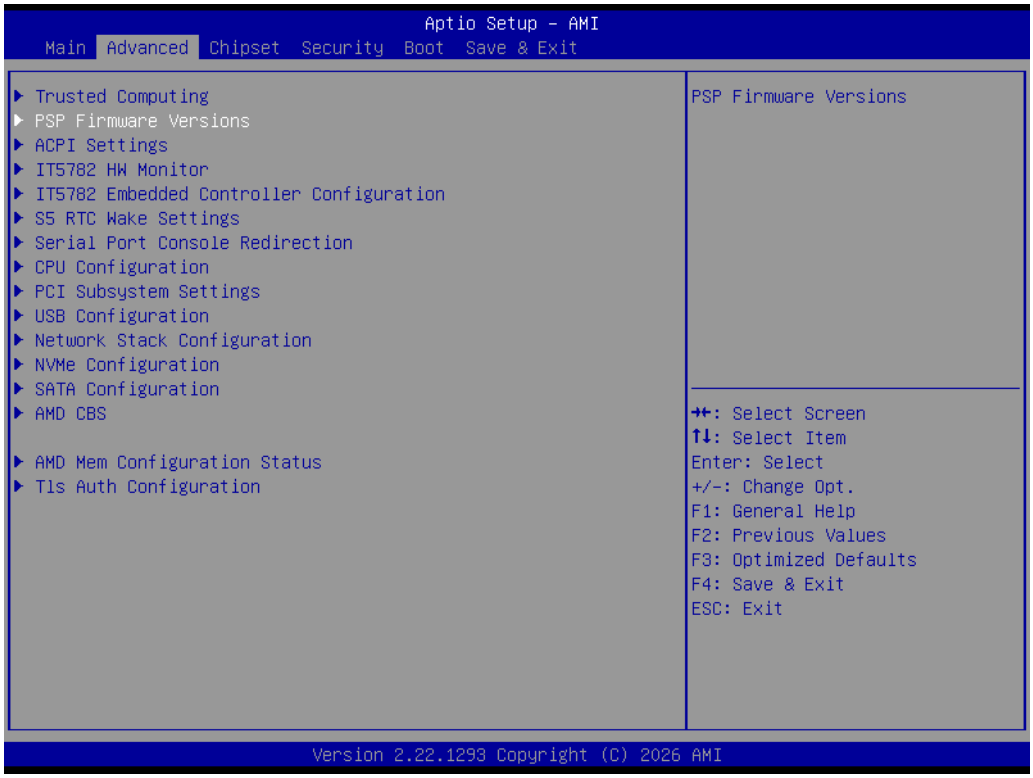
Advanced → Trusted Computing

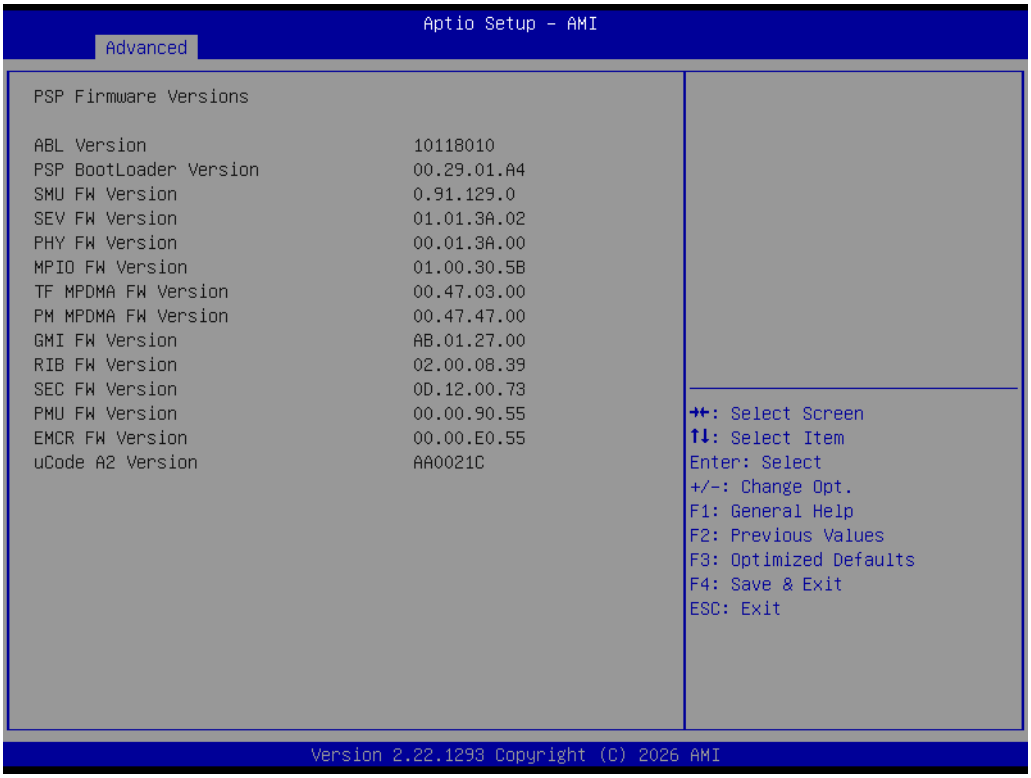




3.2.2.2 PSF Firmware Versions

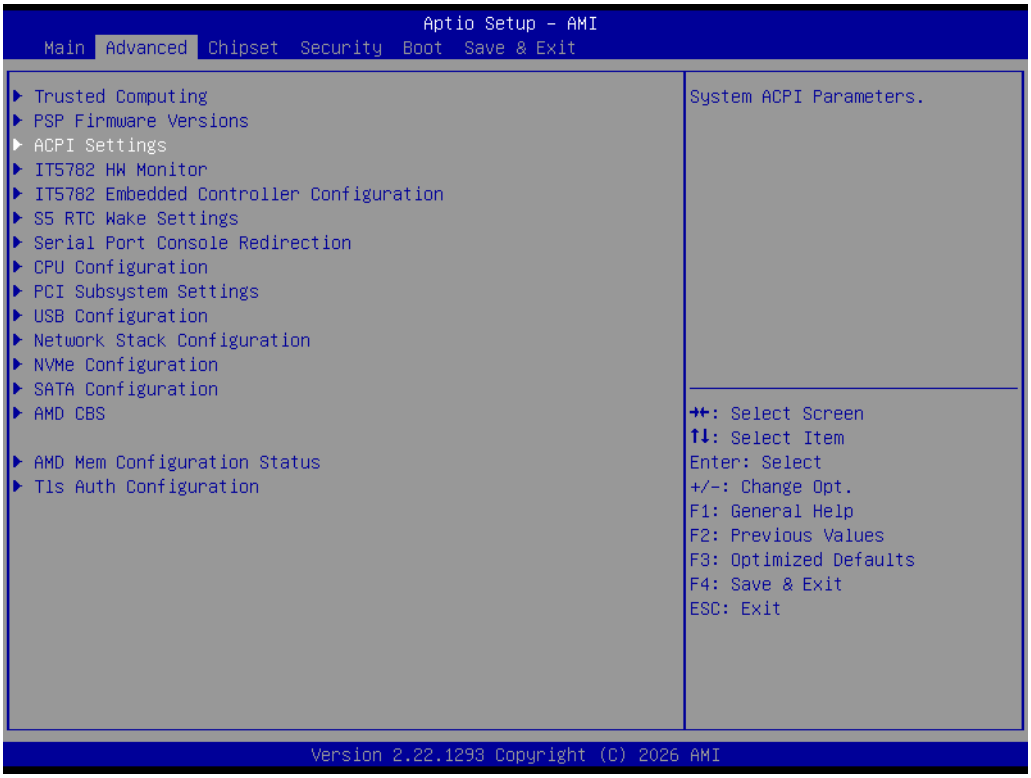
Advanced → PSF Firmware Versions

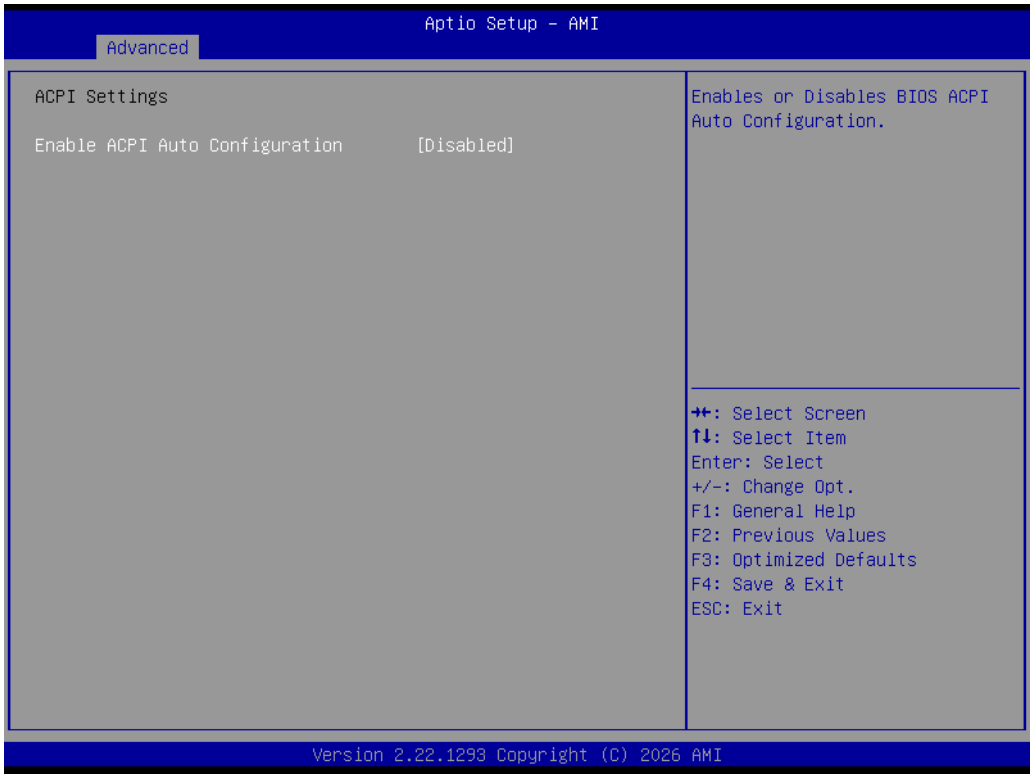




3.2.2.3 ACPI Setting

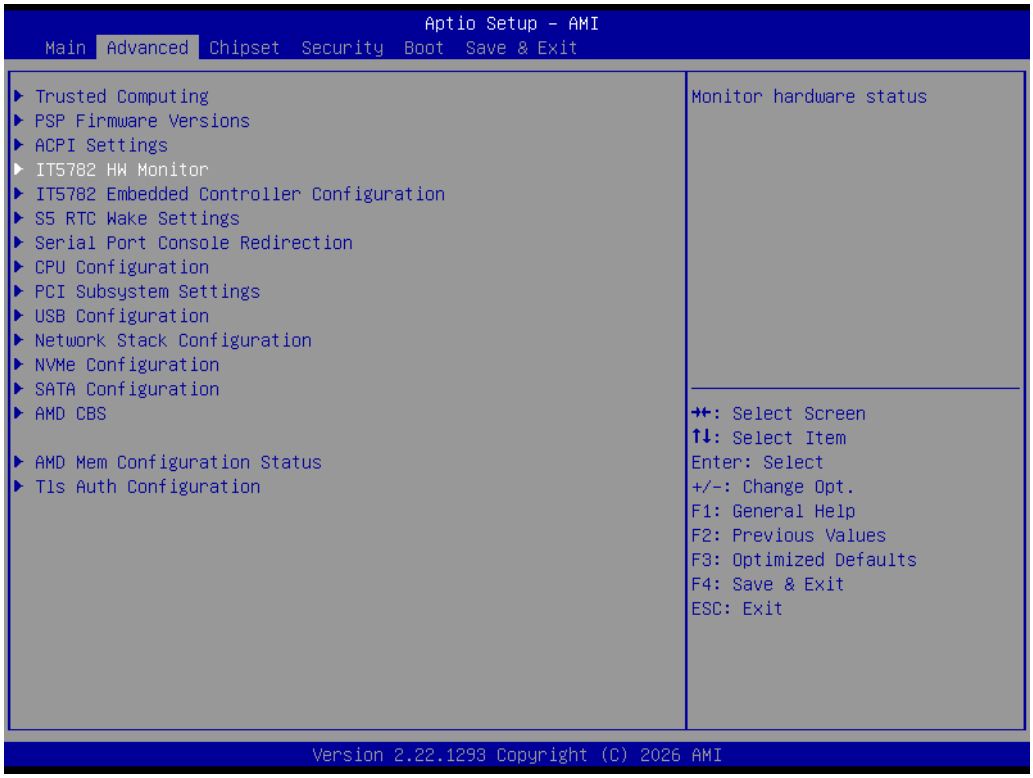
Advanced → ACPI Setting

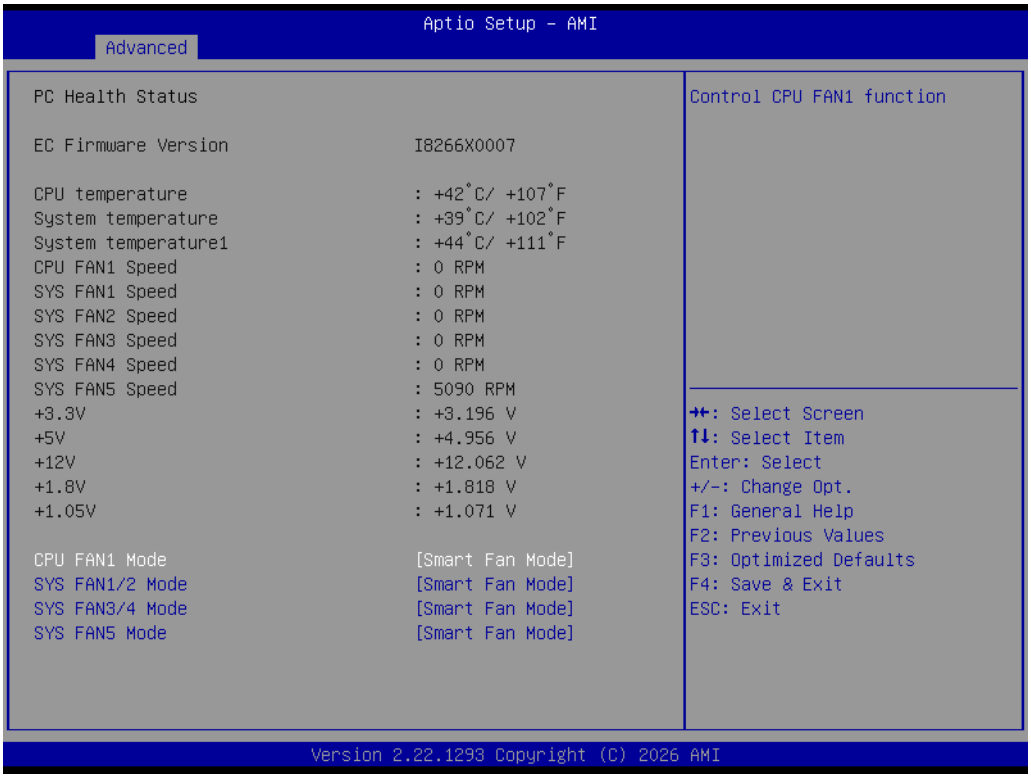




3.2.2.4 IT5782 HW Monitor

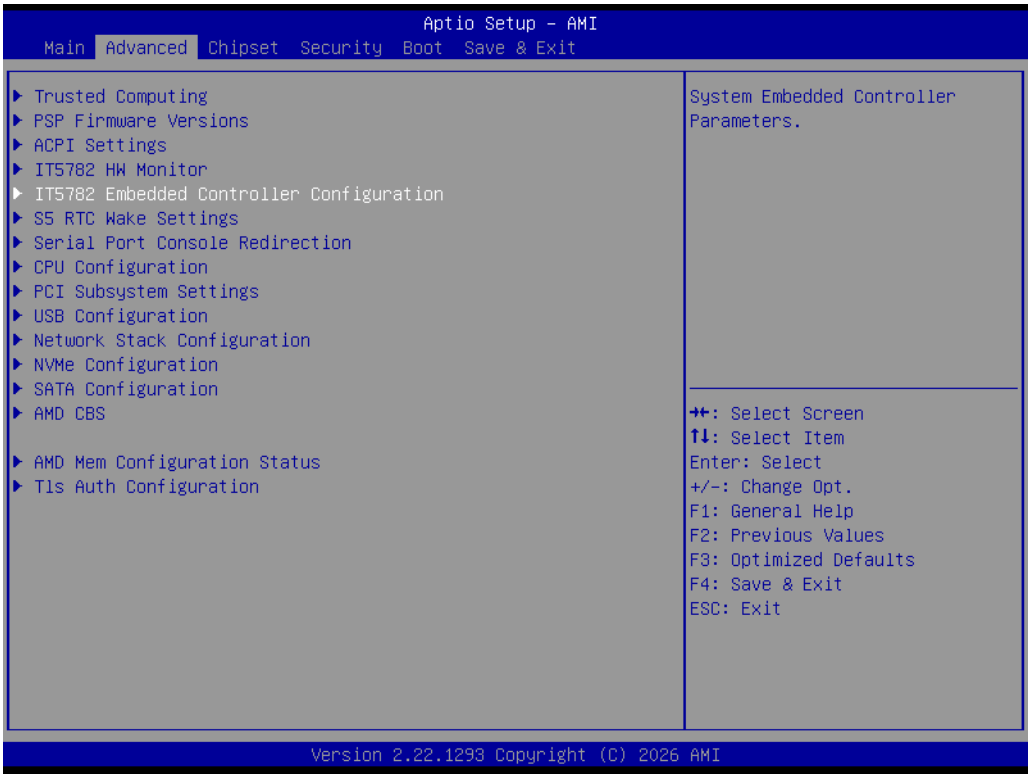
Advanced → IT5782 HW Monitor



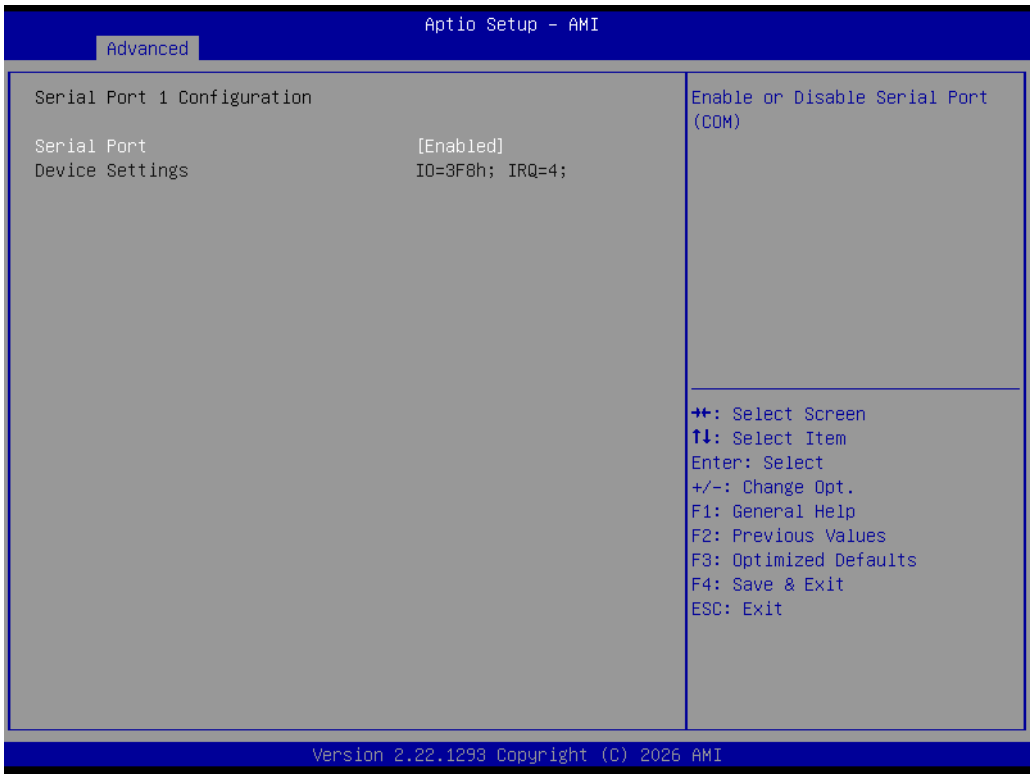


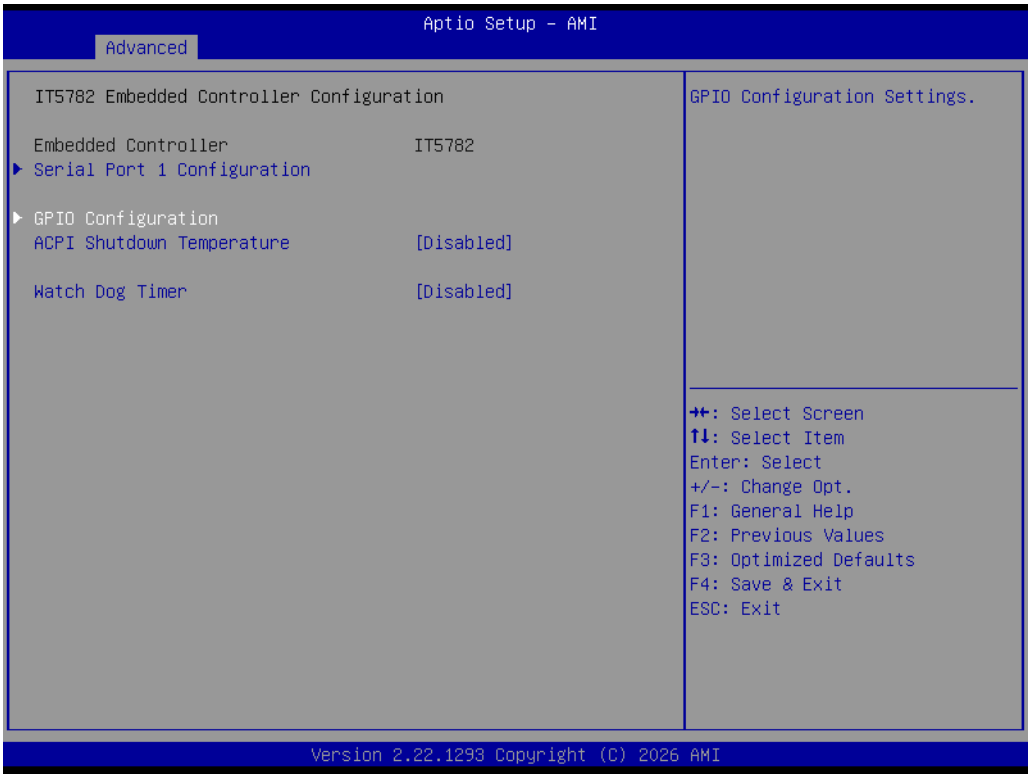
3.2.2.5 IT5782 Embedded Controller Configuration

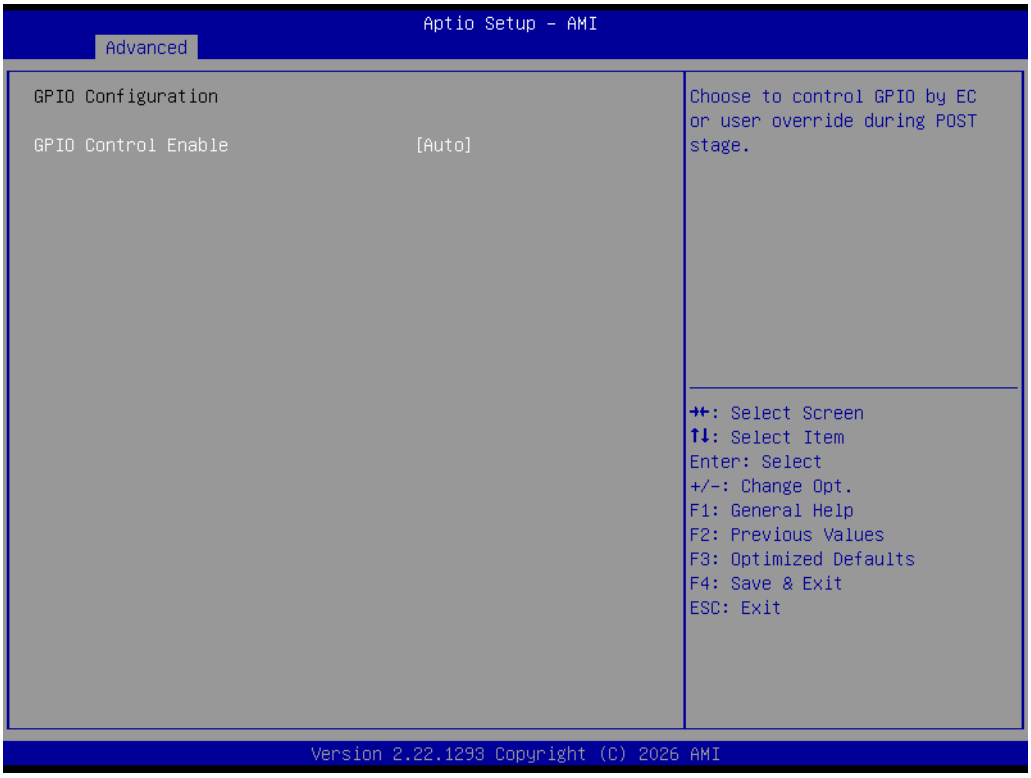
Advanced → IT5782 Embedded Controller Configuration




Aptio Setup – AMI
Advanced
IT5782 Embedded Controller Configuration
Embedded Controller IT5782
Serial Port 1 Configuration
GPIO Configuration
ACPI Shutdown Temperature [Disabled]
Watch Dog Timer [Disabled]
Set Parameters of Serial Port 1 (COMA)
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

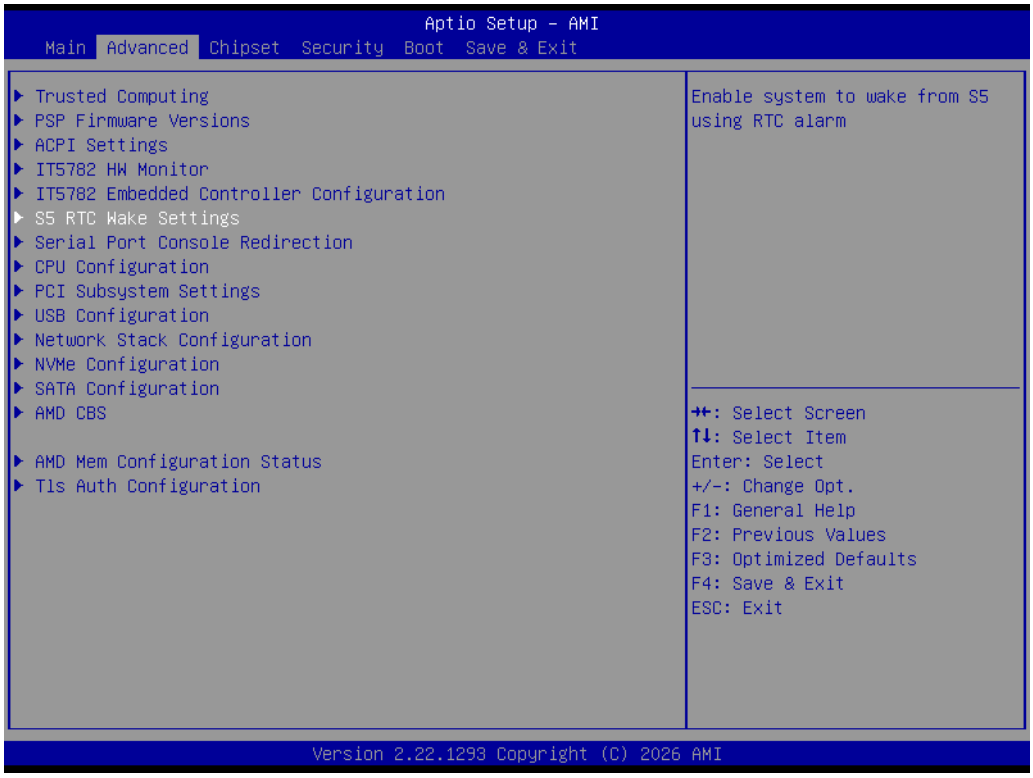

Aptio Setup – AMI
Advanced
Serial Port 1 Configuration
Serial Port [Enabled]
Device Settings IO=3F8h; IRQ=4;
Enable or Disable Serial Port (COM)
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

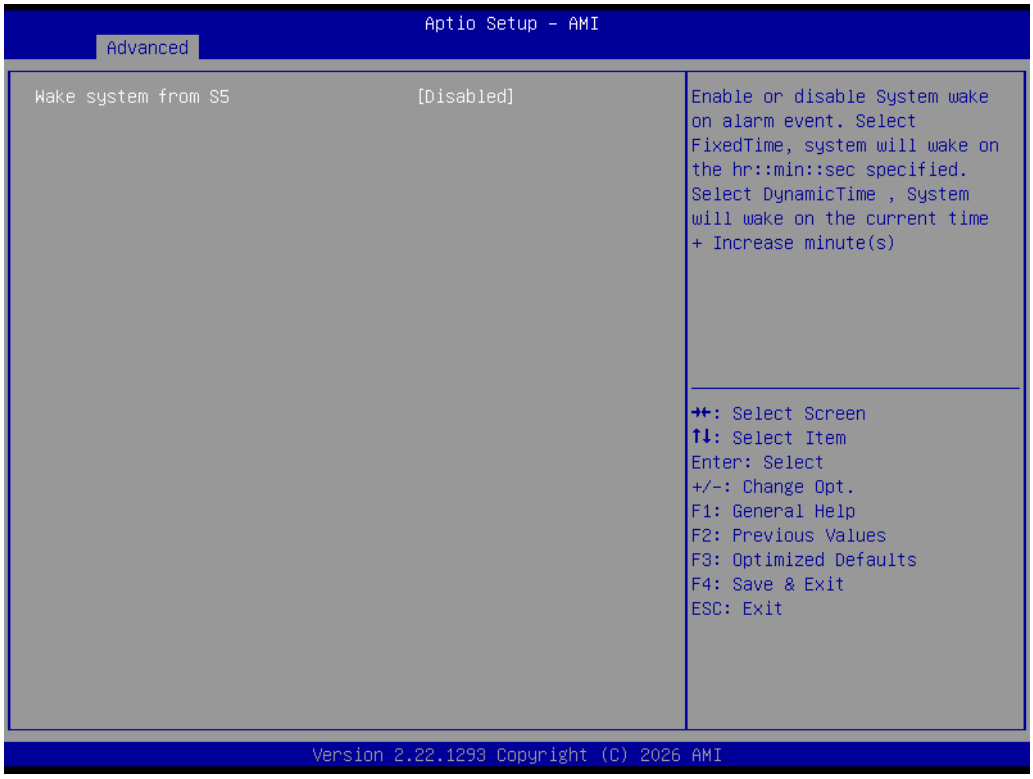

Aptio Setup – AMI
Advanced
IT5782 Embedded Controller Configuration
Embedded Controller IT5782
Serial Port 1 Configuration
GPIO Configuration
ACPI Shutdown Temperature [Disabled]
Watch Dog Timer [Disabled]
GPIO Configuration Settings.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
GPIO Configuration
GPIO Control Enable [Auto]
Choose to control GPIO by EC or user override during POST stage.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

3.2.2.6 RTC Wake Setting

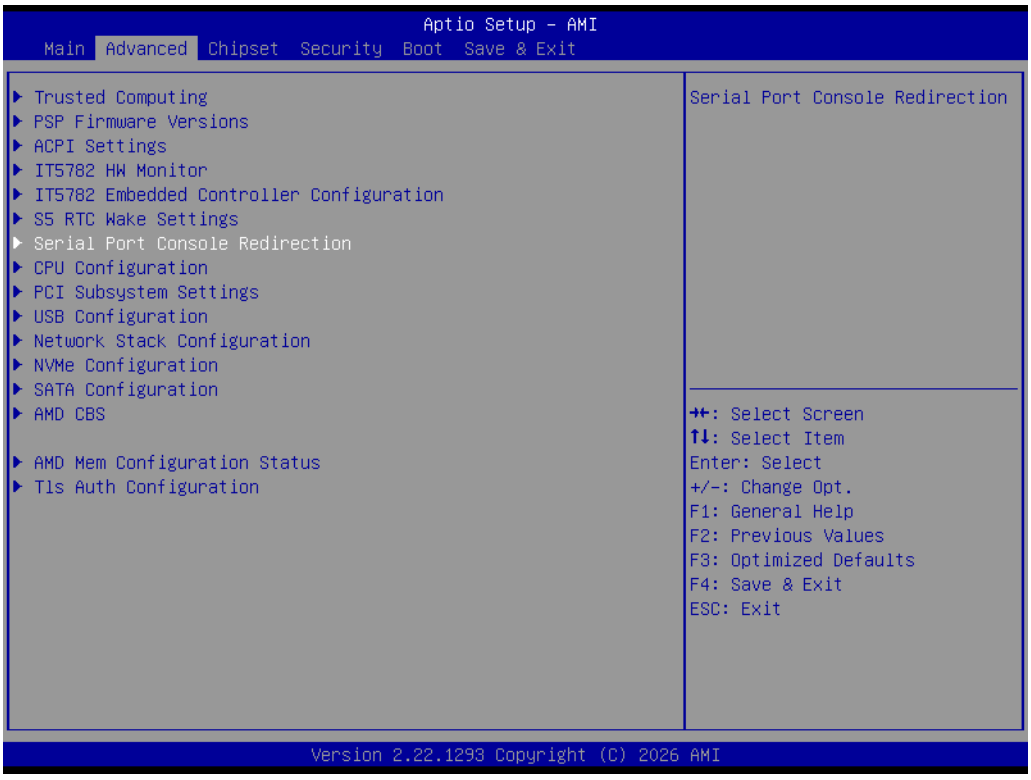
Advanced → S5 RTC Wake Setting

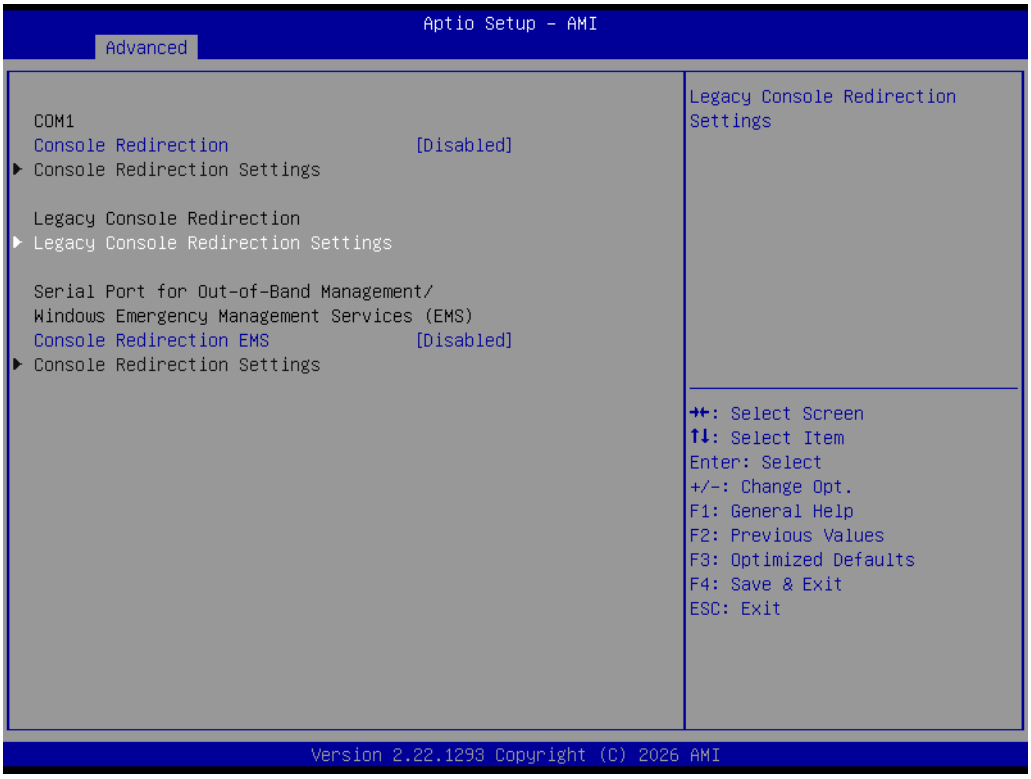


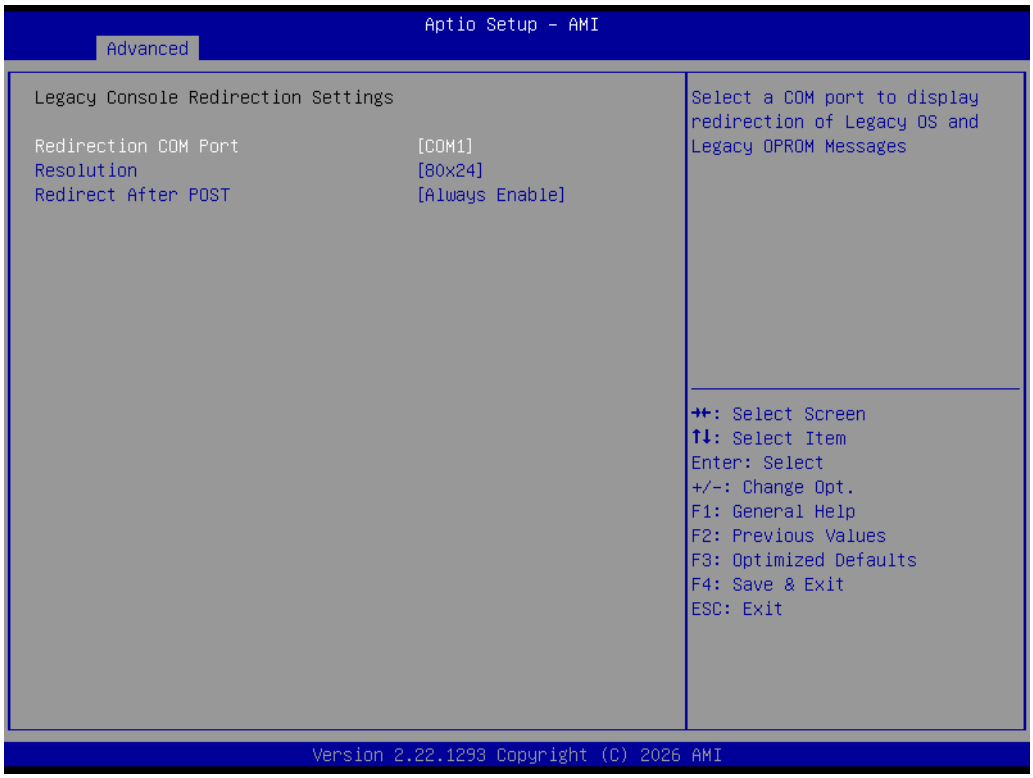


3.2.2.7 Serial Port Console Redirection

Advanced → Serial Port Console Redirection

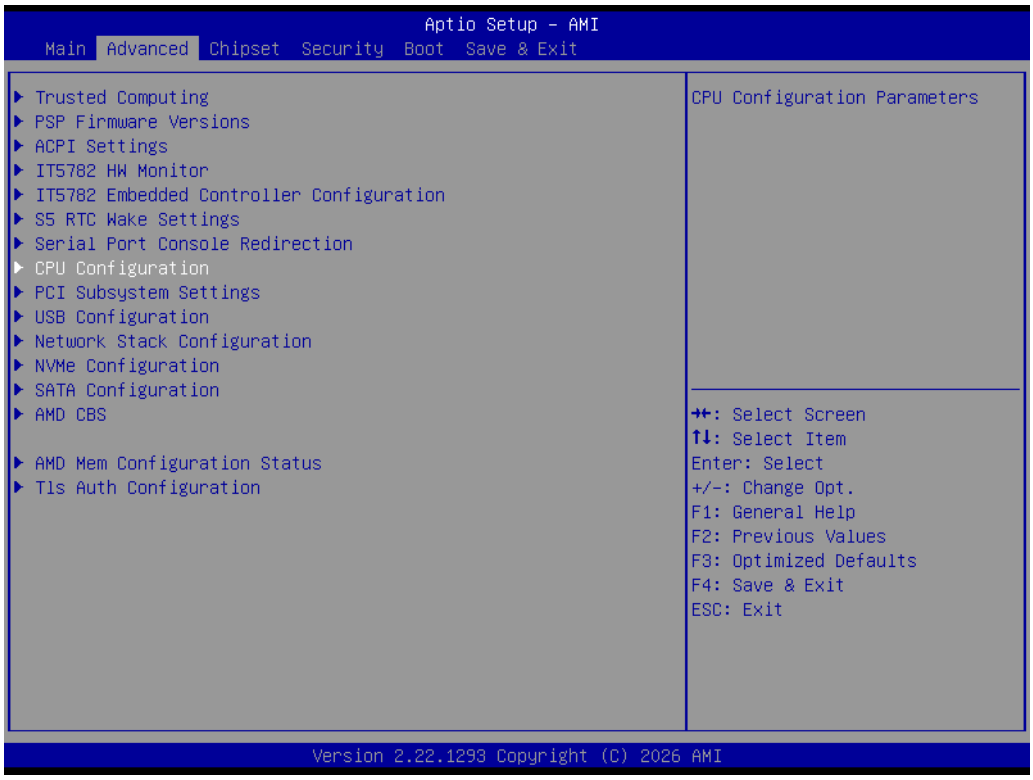


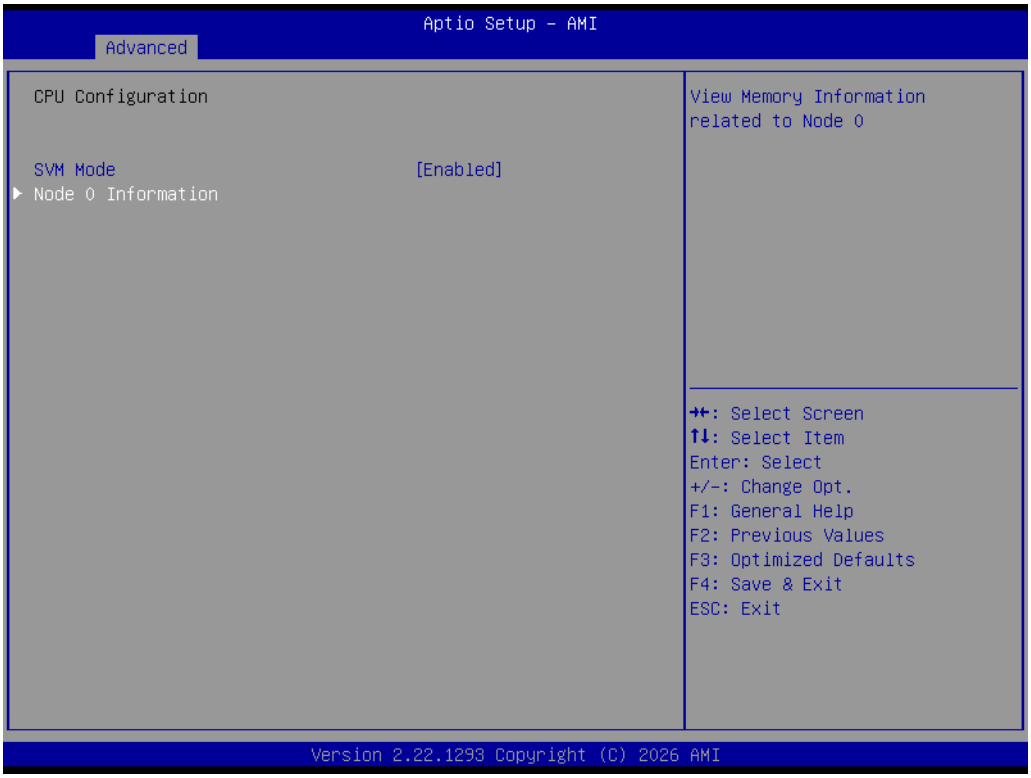


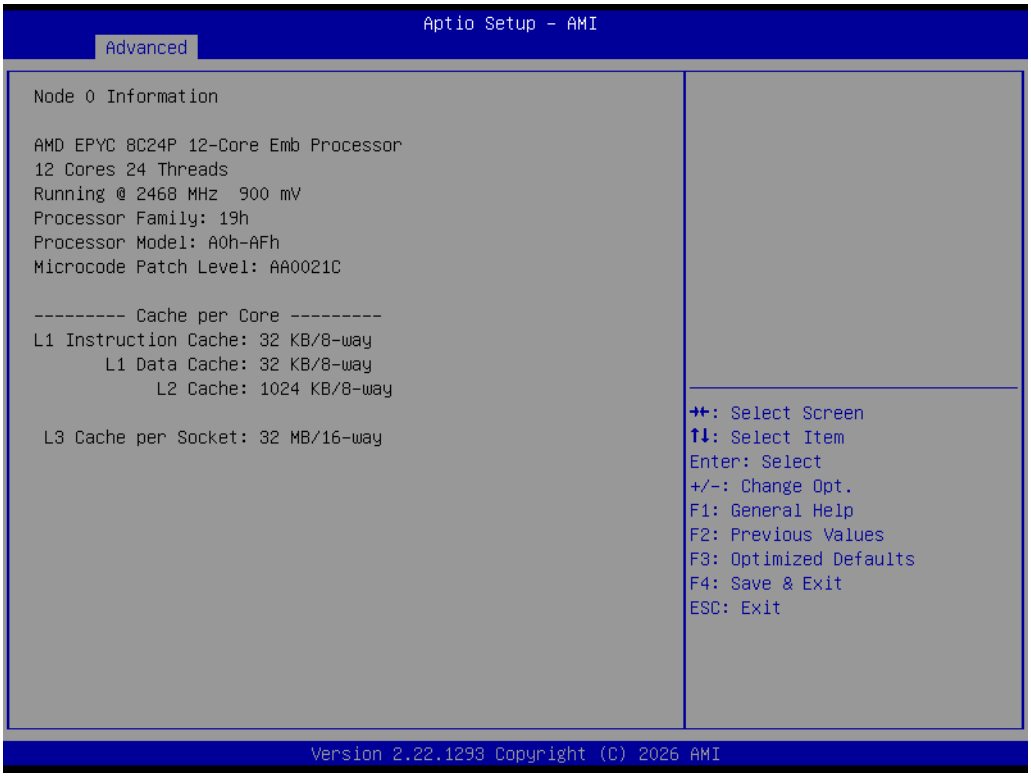


3.2.2.8 CPU Configuration

Advanced → CPU Configuration

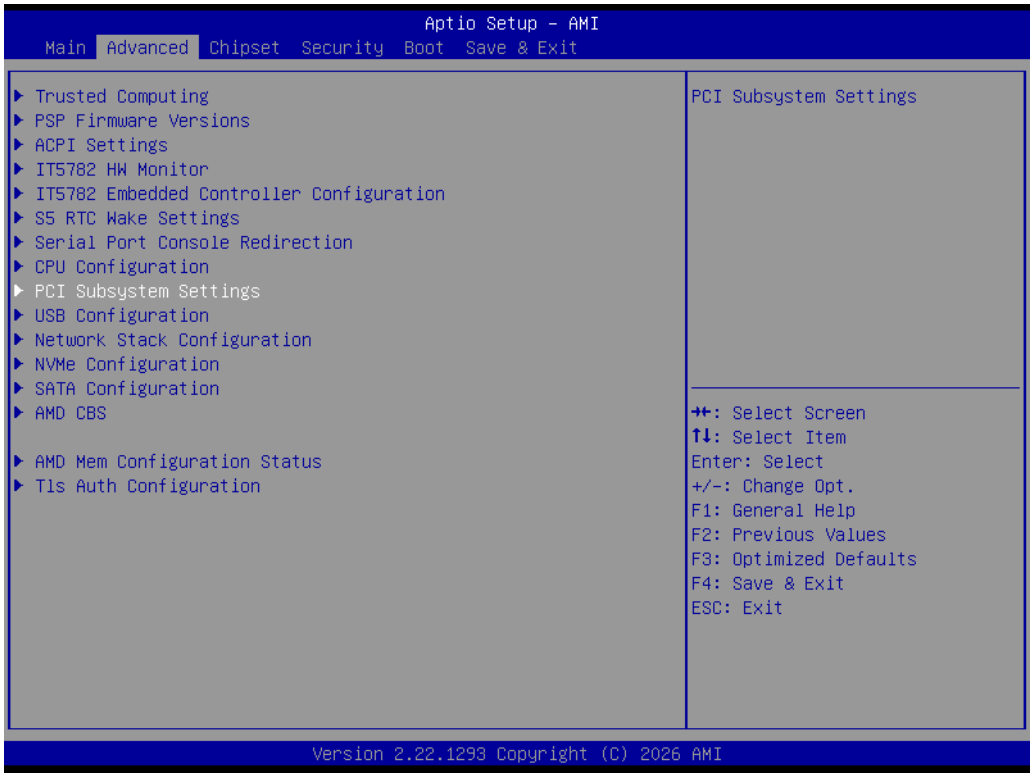


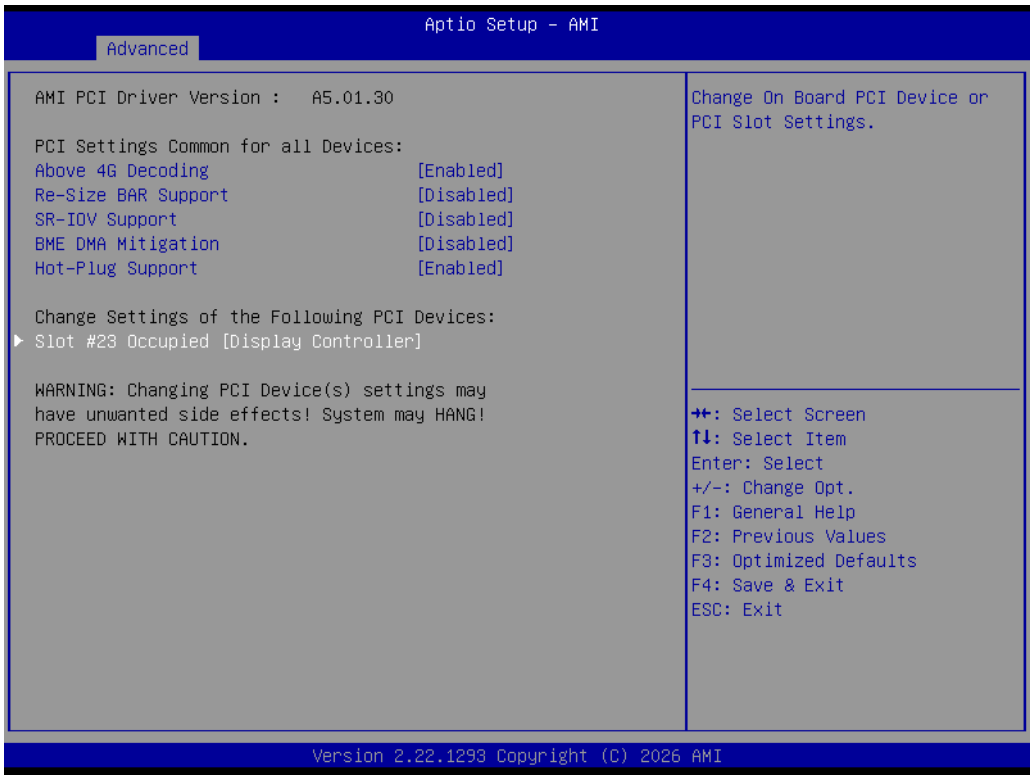

Aptio Setup – AMI
Advanced
CPU Configuration
SVM Mode [Enabled]
Node 0 Information
View Memory Information related to Node 0
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

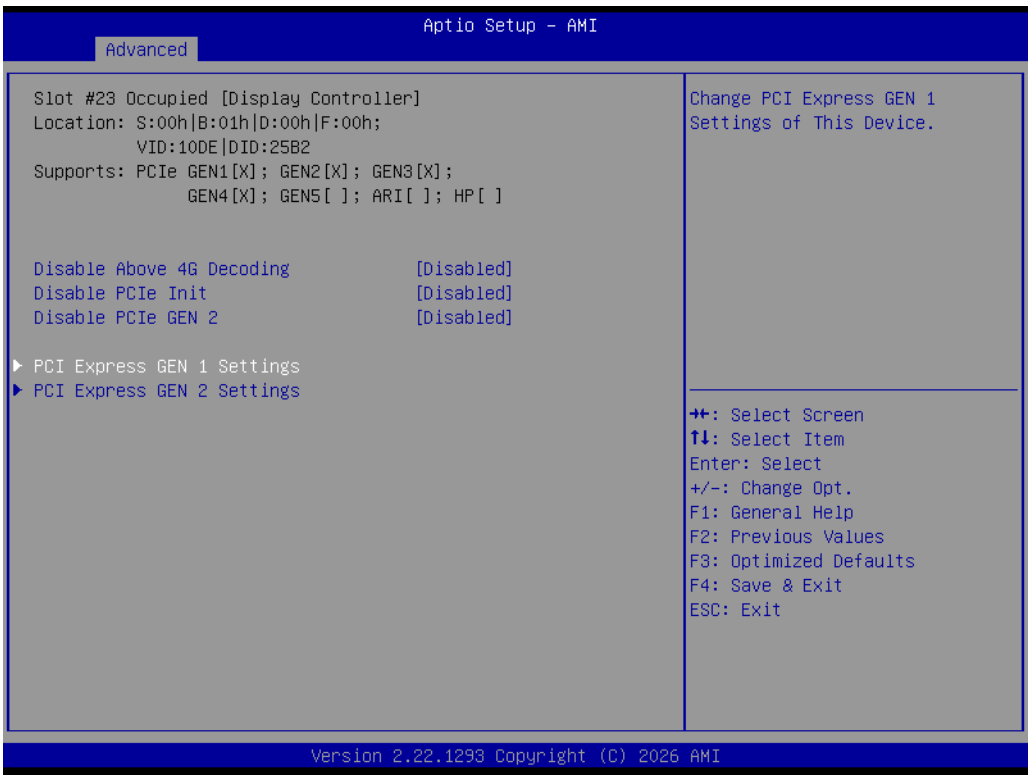

Aptio Setup – AMI
Advanced
Node 0 Information
AMD EPYC 8C24P 12-Core Emb Processor
12 Cores 24 Threads
Running @ 2468 MHz 900 mV
Processor Family: 19h
Processor Model: A0h-AFh
Microcode Patch Level: AA0021C
--------- Cache per Core ---------
L1 Instruction Cache: 32 KB/8-way
L1 Data Cache: 32 KB/8-way
L2 Cache: 1024 KB/8-way
L3 Cache per Socket: 32 MB/16-way
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

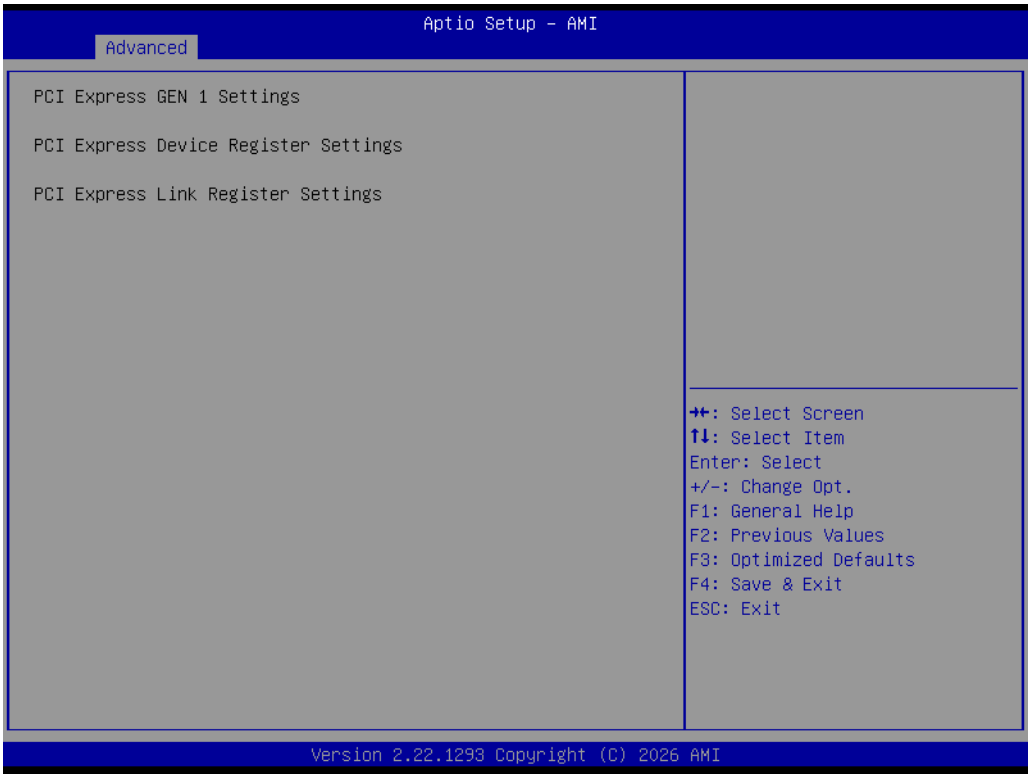
3.2.2.9 PCI Subsystem Setting

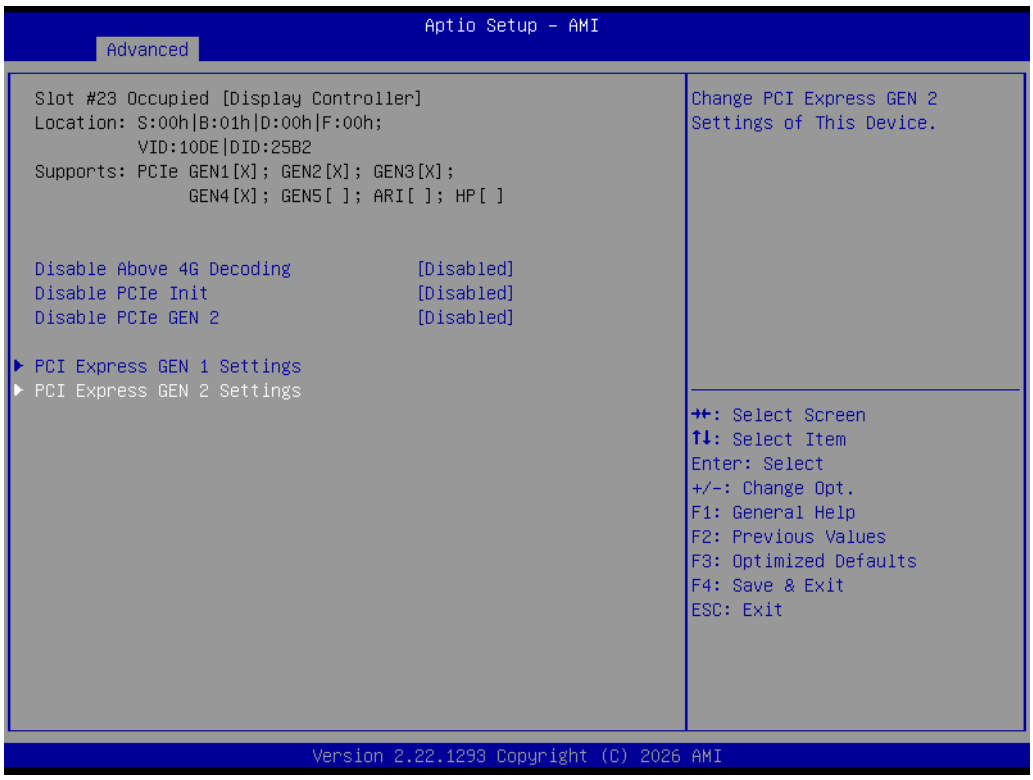
Advanced → PCI Subsystem Setting

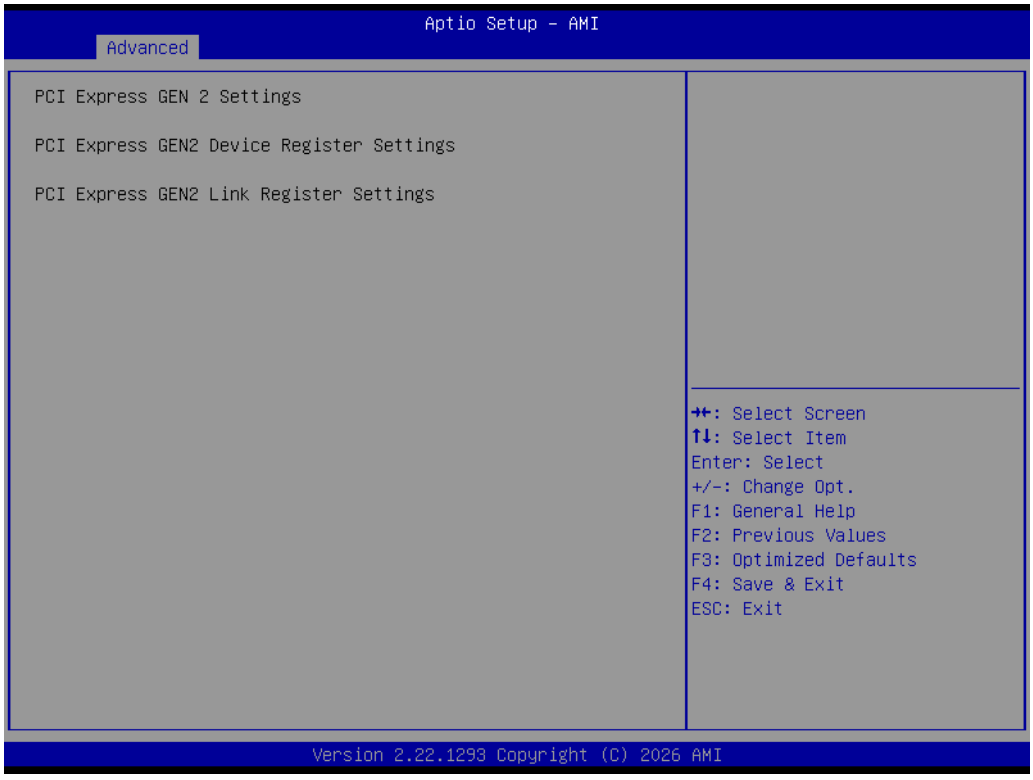





Aptio Setup – AMI
Advanced
Slot #23 Occupied [Display Controller]
Location: S:00h|B:01h|D:00h|F:00h;
VID:10DE|DID:25B2
Supports: PCIe GEN1[X]; GEN2[X]; GEN3[X];
GEN4[X]; GEN5[ ]; ARI[ ]; HP[ ]
Disable Above 4G Decoding [Disabled]
Disable PCIe Init [Disabled]
Disable PCIe GEN 2 [Disabled]
PCI Express GEN 1 Settings
PCI Express GEN 2 Settings
Change PCI Express GEN 1 Settings of This Device.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
PCI Express GEN 1 Settings
PCI Express Device Register Settings
PCI Express Link Register Settings
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
Slot #23 Occupied [Display Controller]
Location: S:00h|B:01h|D:00h|F:00h;
VID:10DE|DID:25B2
Supports: PCIe GEN1[X]; GEN2[X]; GEN3[X];
GEN4[X]; GEN5[ ]; ARI[ ]; HP[ ]
Disable Above 4G Decoding [Disabled]
Disable PCIe Init [Disabled]
Disable PCIe GEN 2 [Disabled]
PCI Express GEN 1 Settings
PCI Express GEN 2 Settings
Change PCI Express GEN 2 Settings of This Device.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
PCI Express GEN 2 Settings
PCI Express GEN2 Device Register Settings
PCI Express GEN2 Link Register Settings
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
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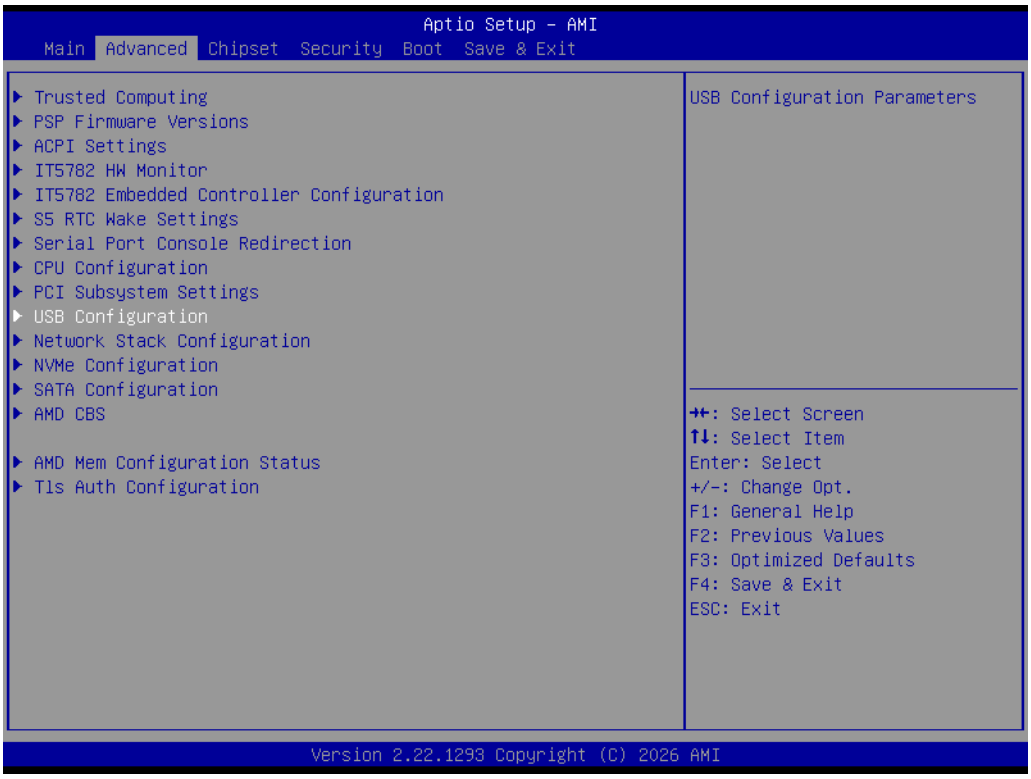
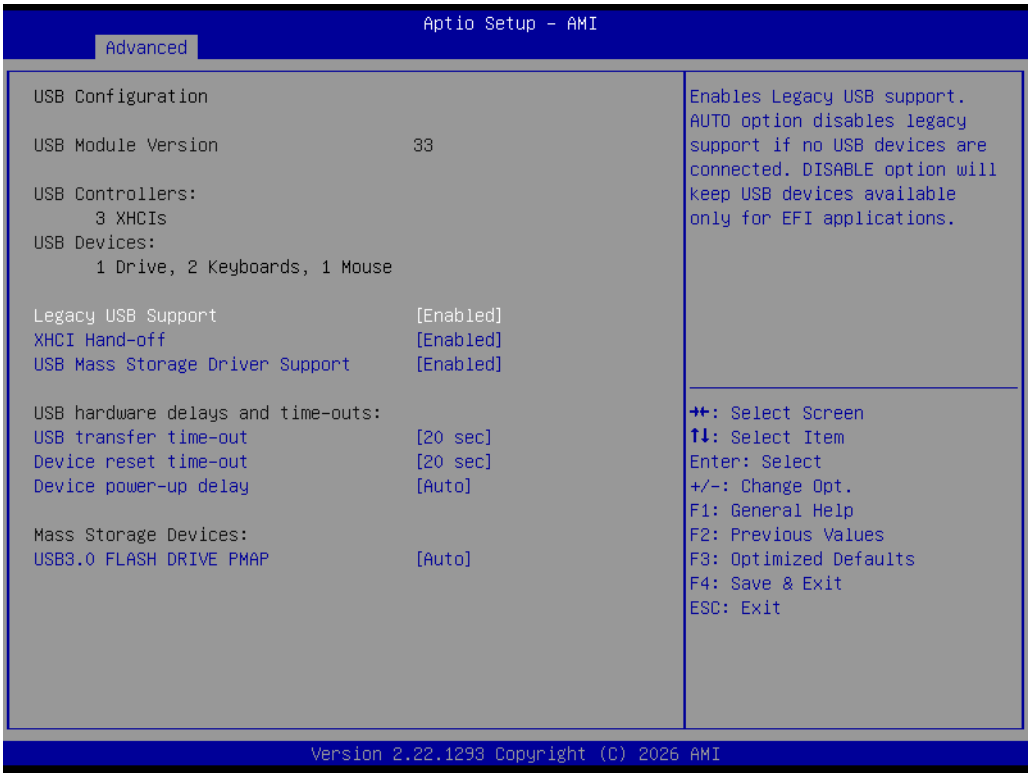
3.2.2.10 USB Configuration

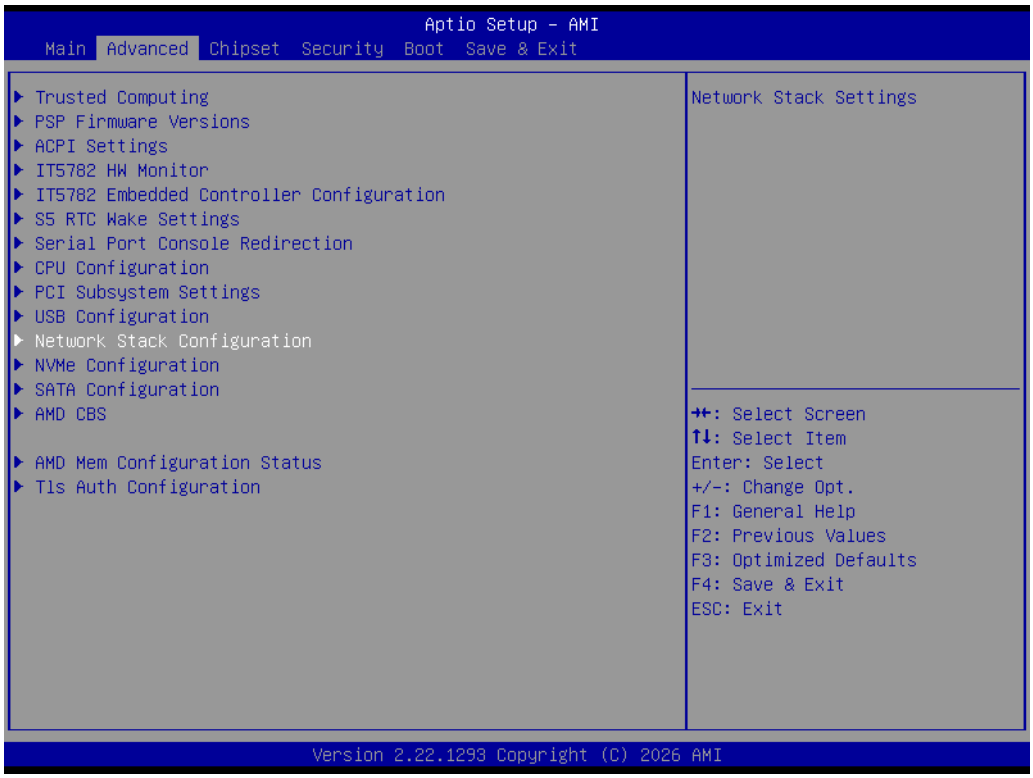
Advanced → USB Configuration

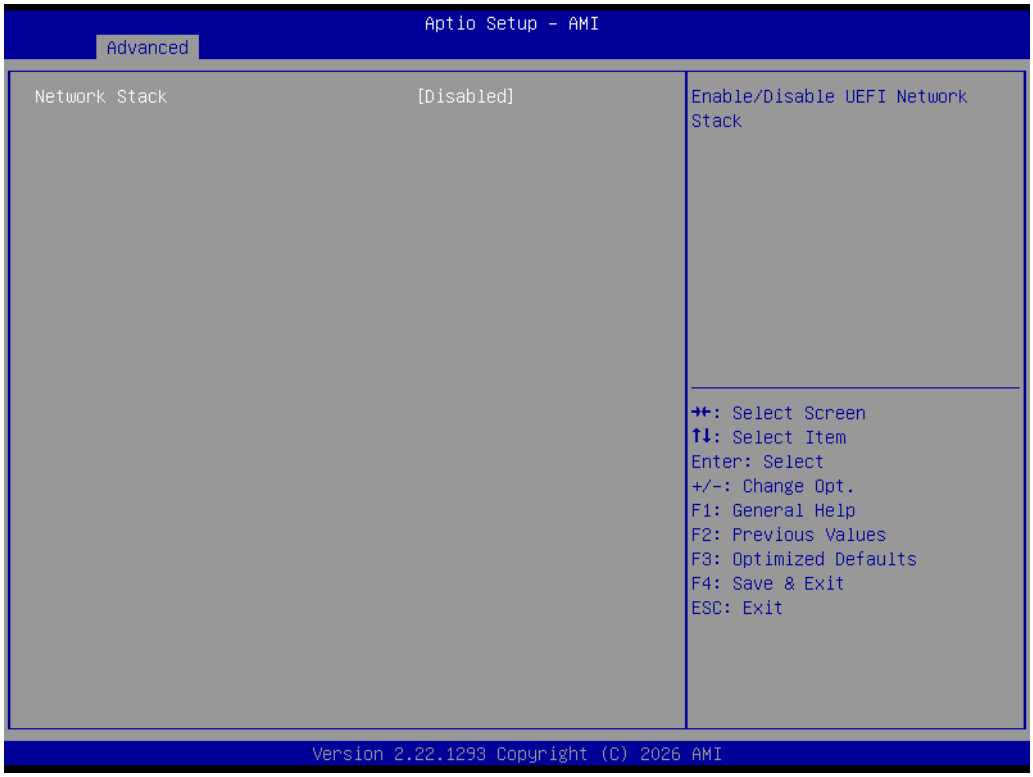




3.2.2.11 Network Stack Configuration

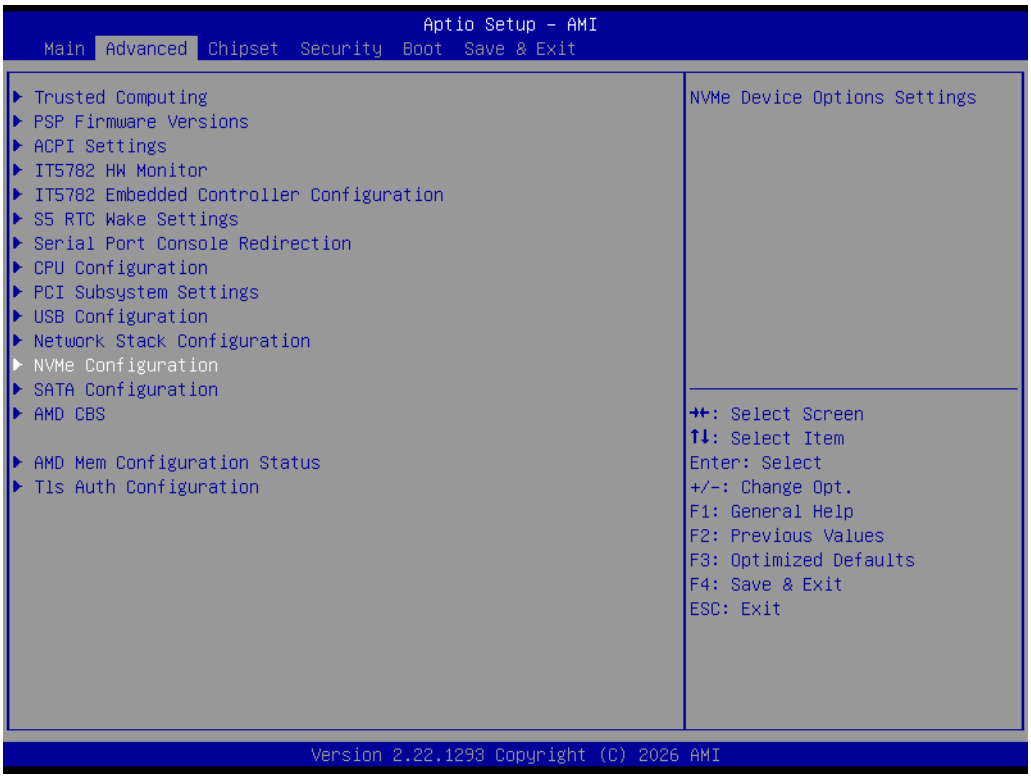
Advanced → Network Stack Configuration

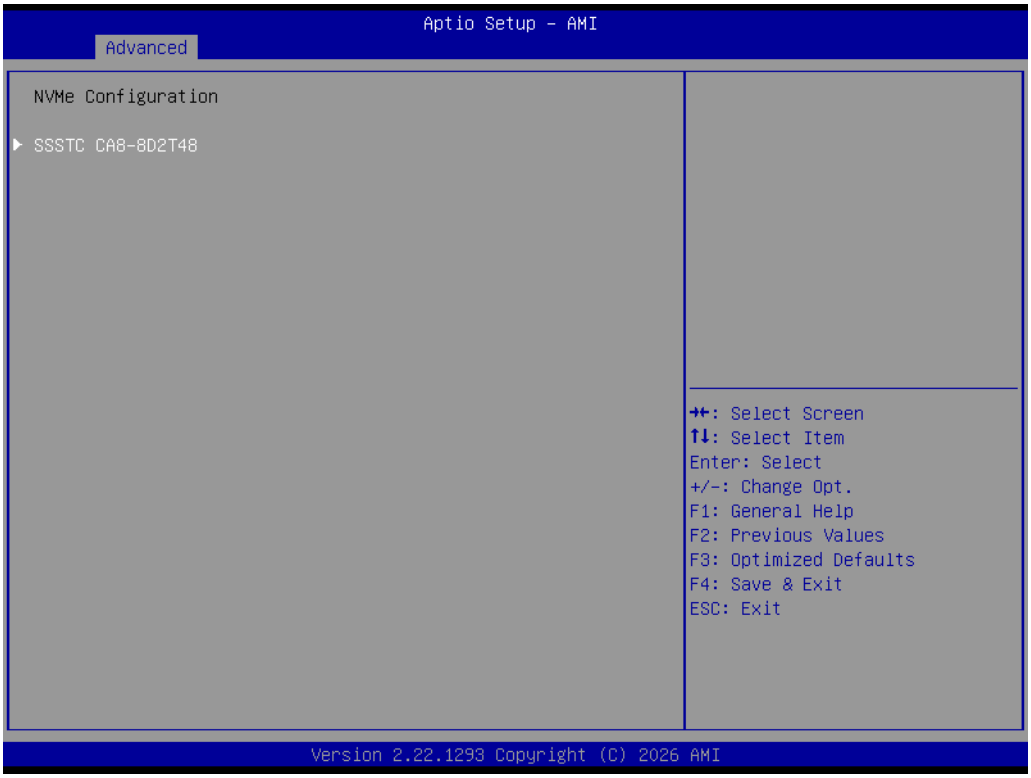




3.2.2.12 NVMe Configuration

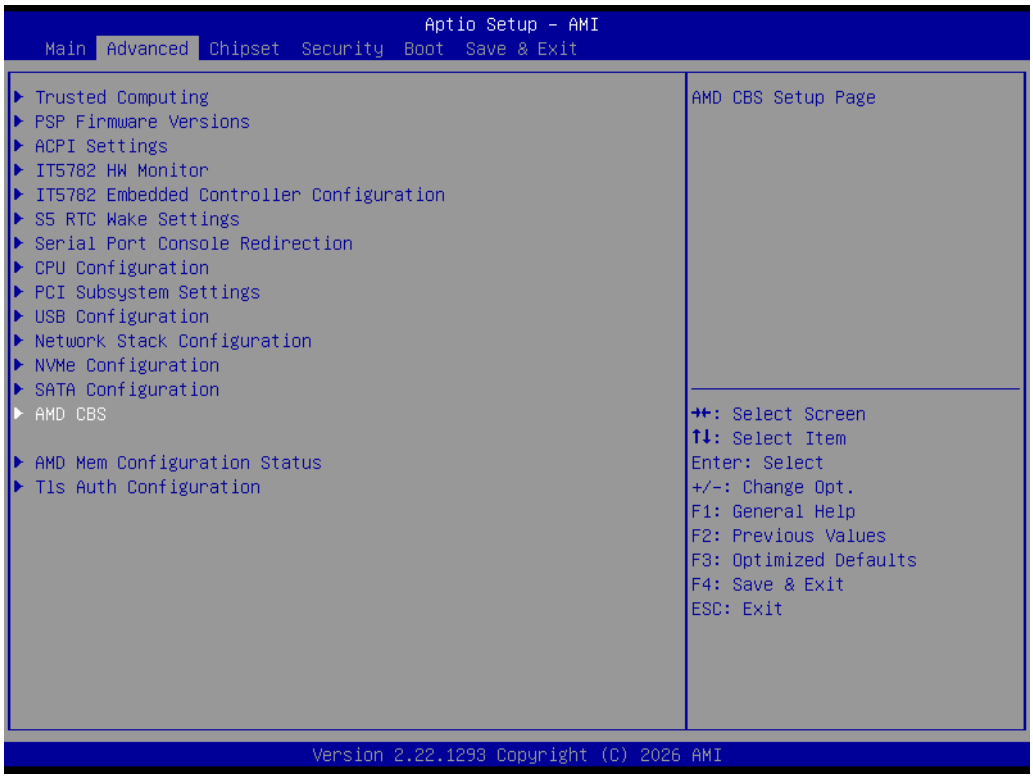
Advanced → NVMe Configuration

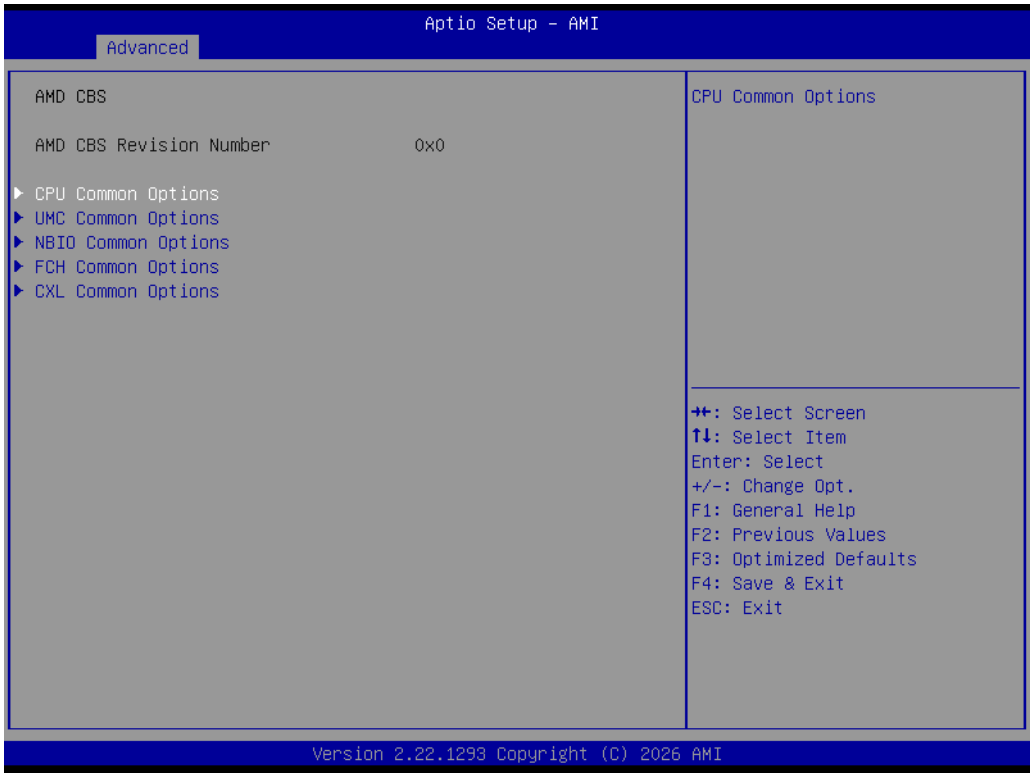


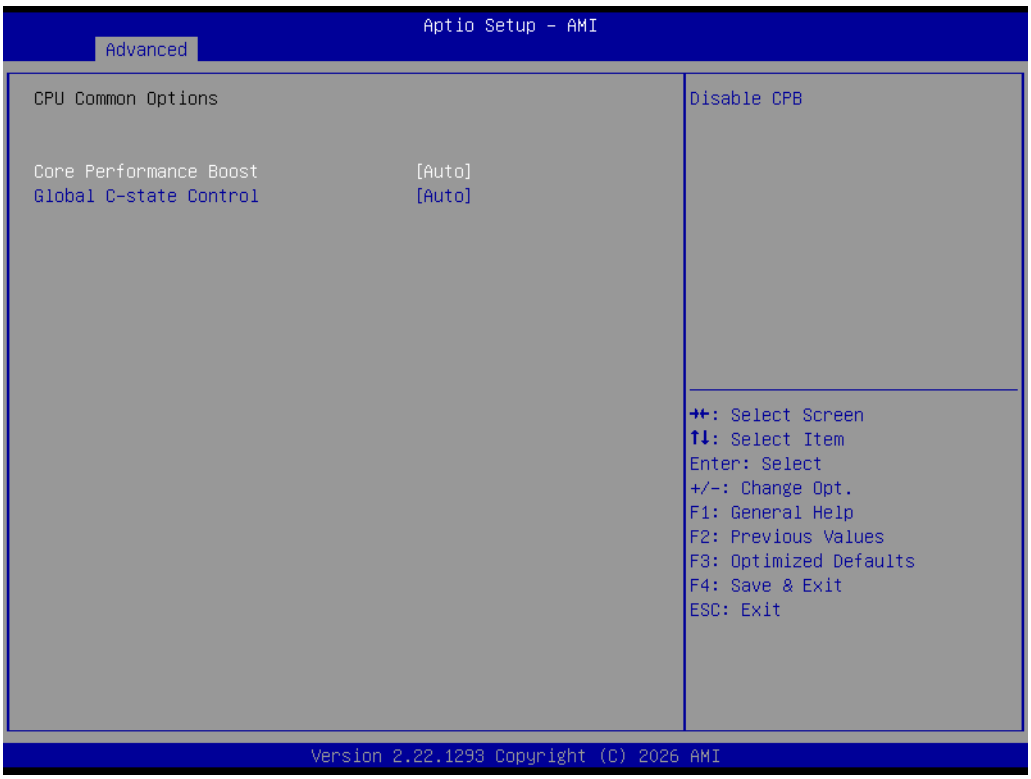


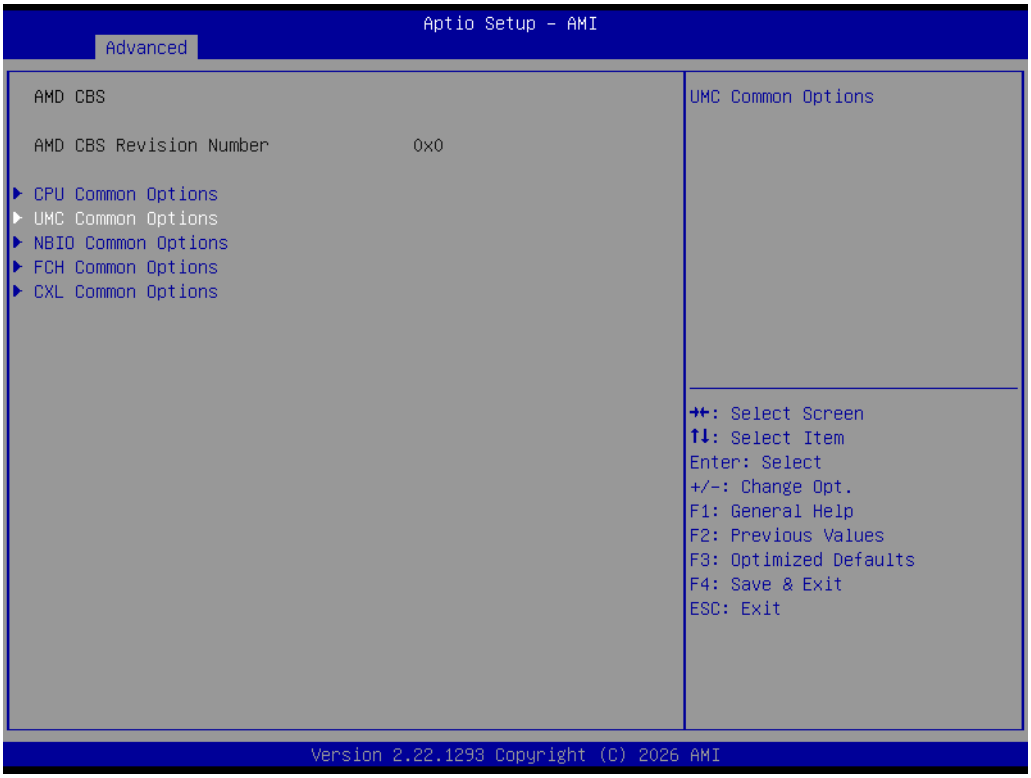
3.2.2.13 AMD CBS

Advanced → AMD CBS

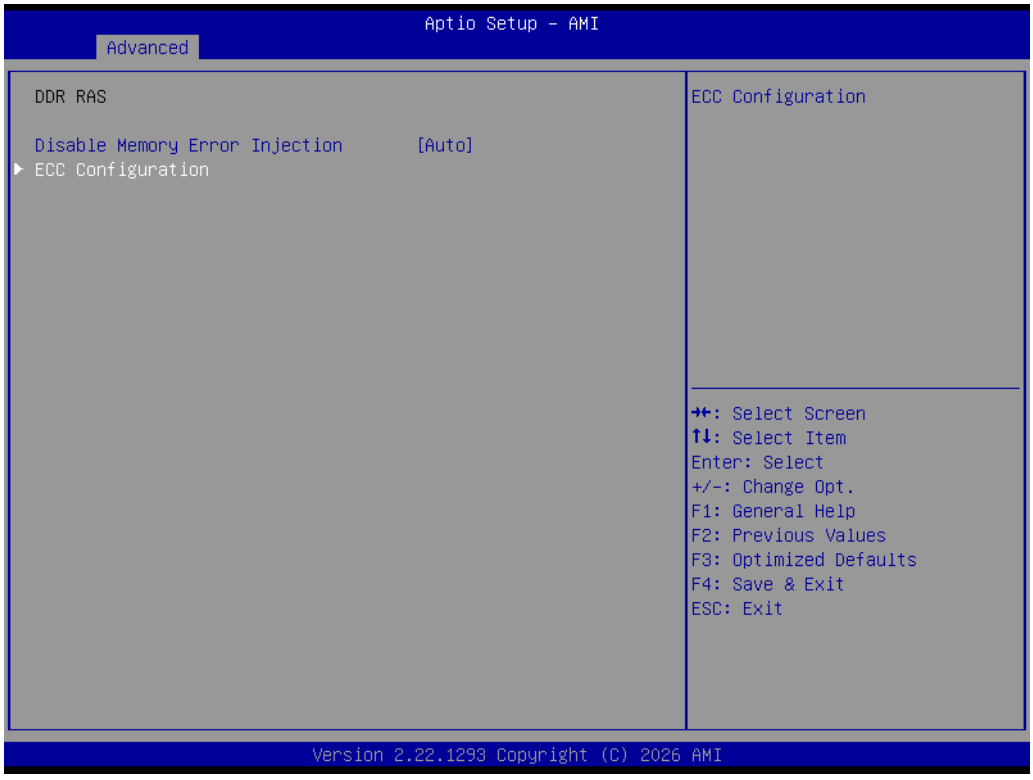




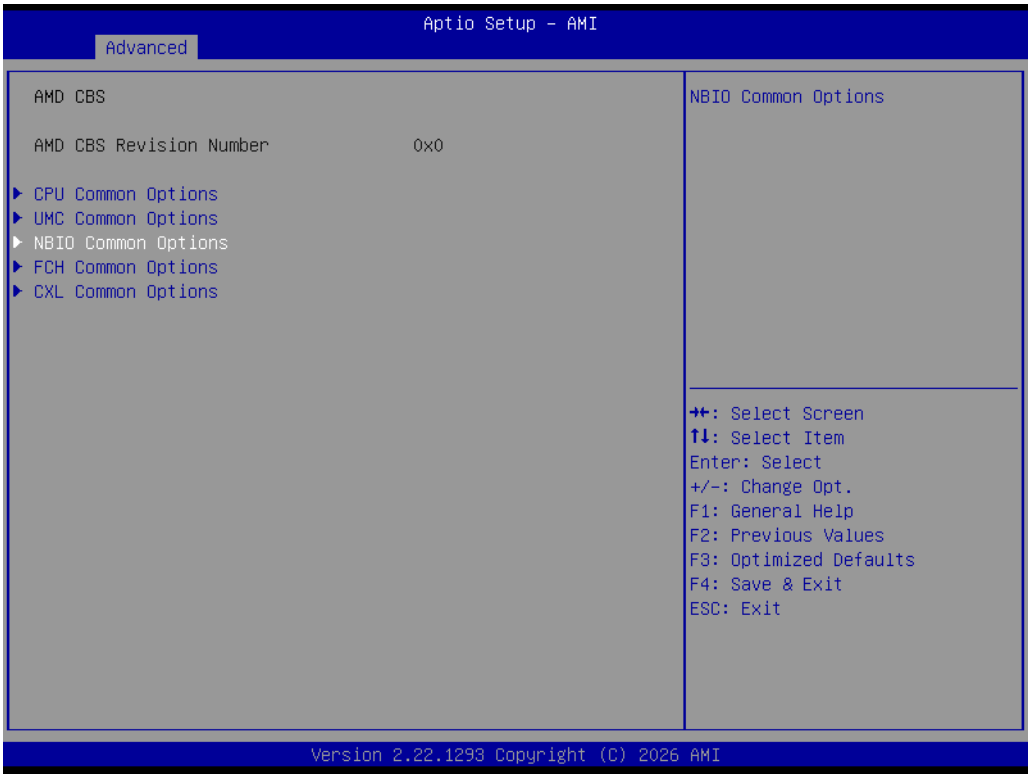

Aptio Setup – AMI
Advanced
CPU Common Options
Core Performance Boost [Auto]
Global C-state Control [Auto]
Disable CPB
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

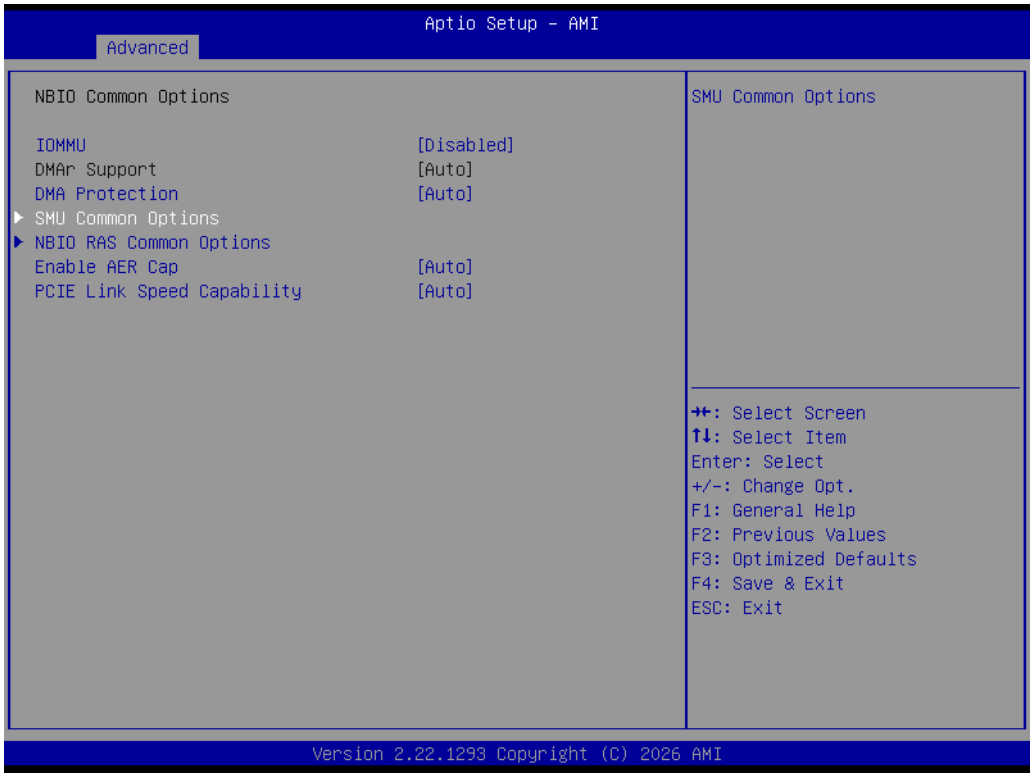

Aptio Setup – AMI
Advanced
AMD CBS
AMD CBS Revision Number 0x0
CPU Common Options
UMC Common Options
NBIO Common Options
FCH Common Options
CXL Common Options
UMC Common Options
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

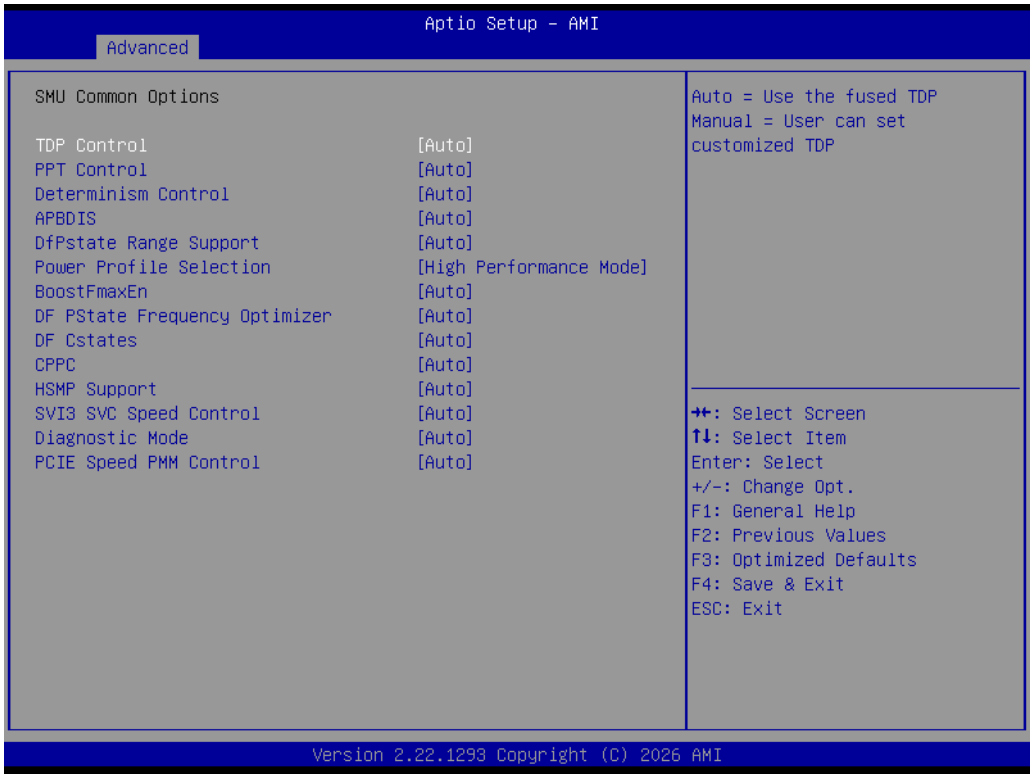

Aptio Setup – AMI
Advanced
UMC Common Options
DDR RAS
DDR RAS
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

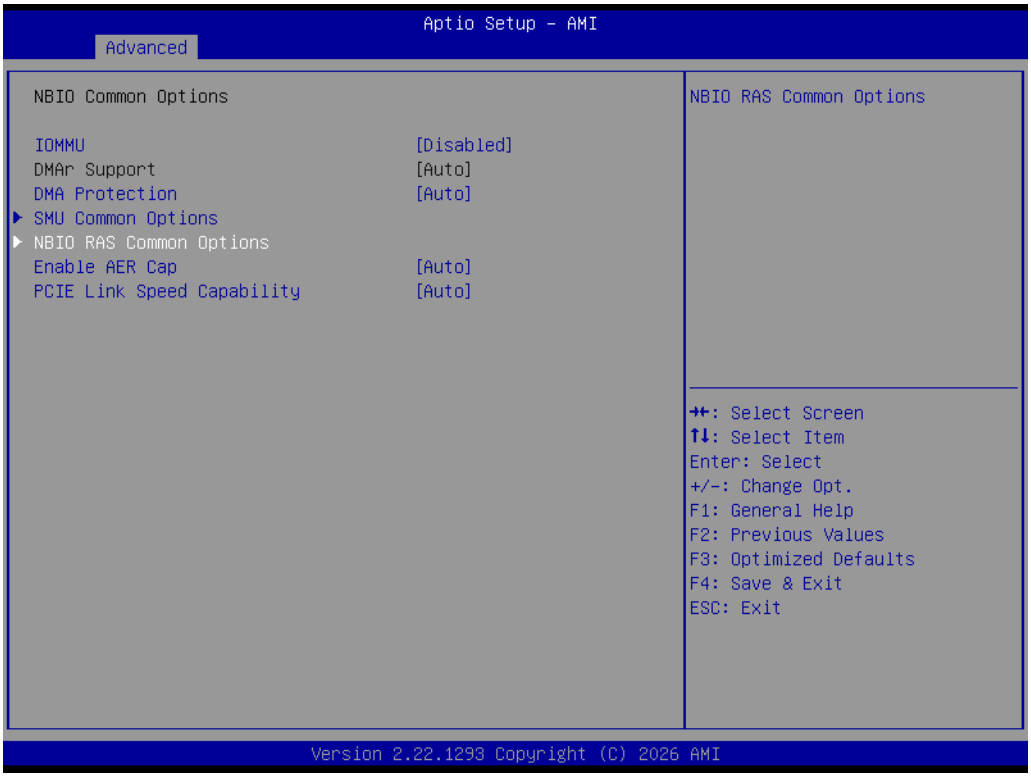

Aptio Setup – AMI
Advanced
DDR RAS
Disable Memory Error Injection [Auto]
ECC Configuration
ECC Configuration
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

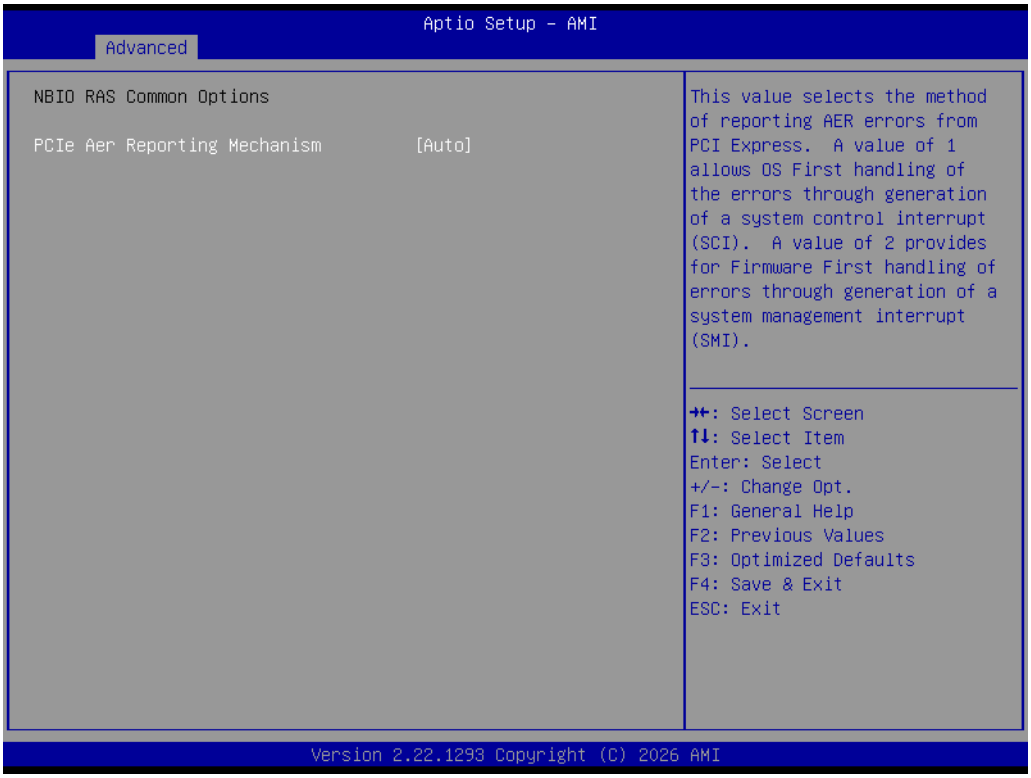

Aptio Setup – AMI
Advanced
ECC Configuration
DRAM ECC Symbol Size [Auto]
DRAM ECC Enable [Auto]
DRAM UECC Retry [Disabled]
Max DRAM UECC Error Replay 8
Memory Clear [Auto]
Address XOR after ECC [Auto]
DRAM ECC Symbol Size (x4/x16)
-
UMC_CH::EccCtrl[EccSymbolSize16
, EccSymbolSize]
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

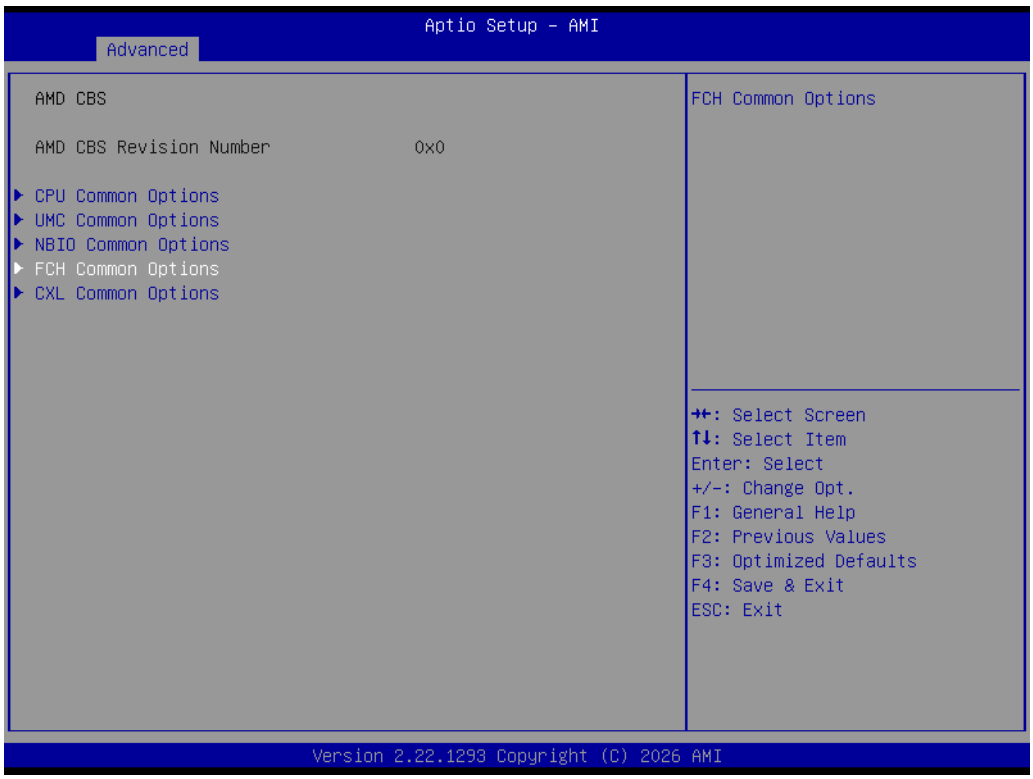

Aptio Setup – AMI
Advanced
AMD CBS
AMD CBS Revision Number 0x0
▶ CPU Common Options
▶ UMC Common Options
▶ NBIO Common Options
▶ FCH Common Options
▶ CXL Common Options
NBIO Common Options
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

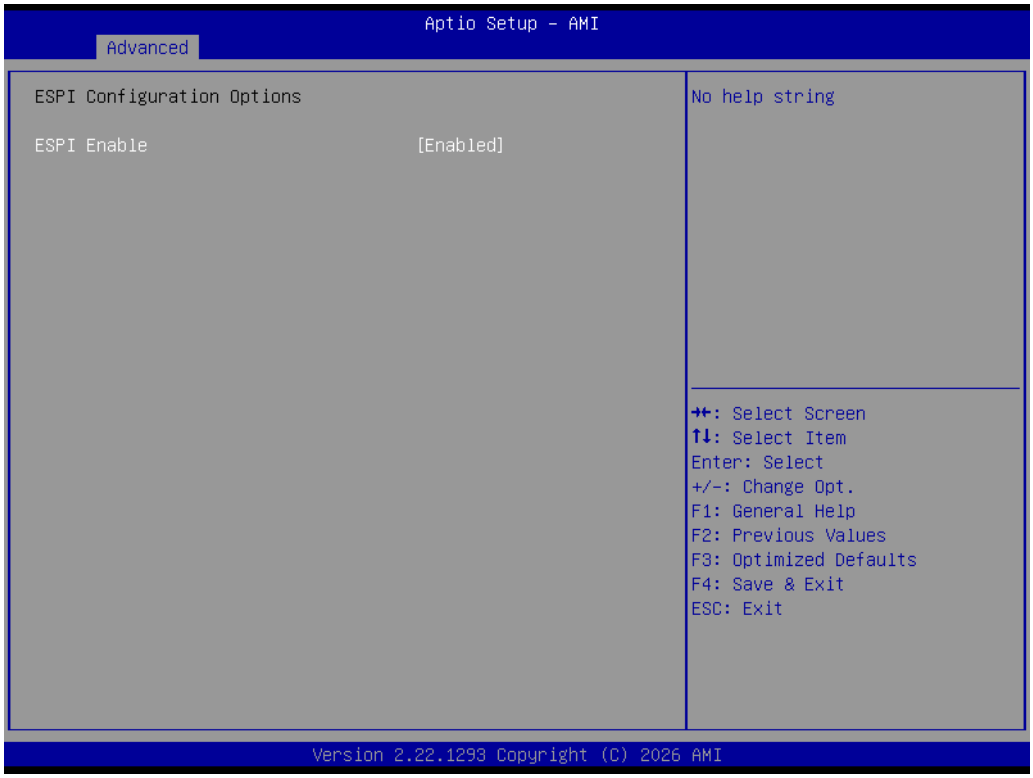

Aptio Setup – AMI
Advanced
NBIO Common Options
IOMMU [Disabled]
DMAr Support [Auto]
DMA Protection [Auto]
SMU Common Options
NBIO RAS Common Options
Enable AER Cap [Auto]
PCIE Link Speed Capability [Auto]
SMU Common Options
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

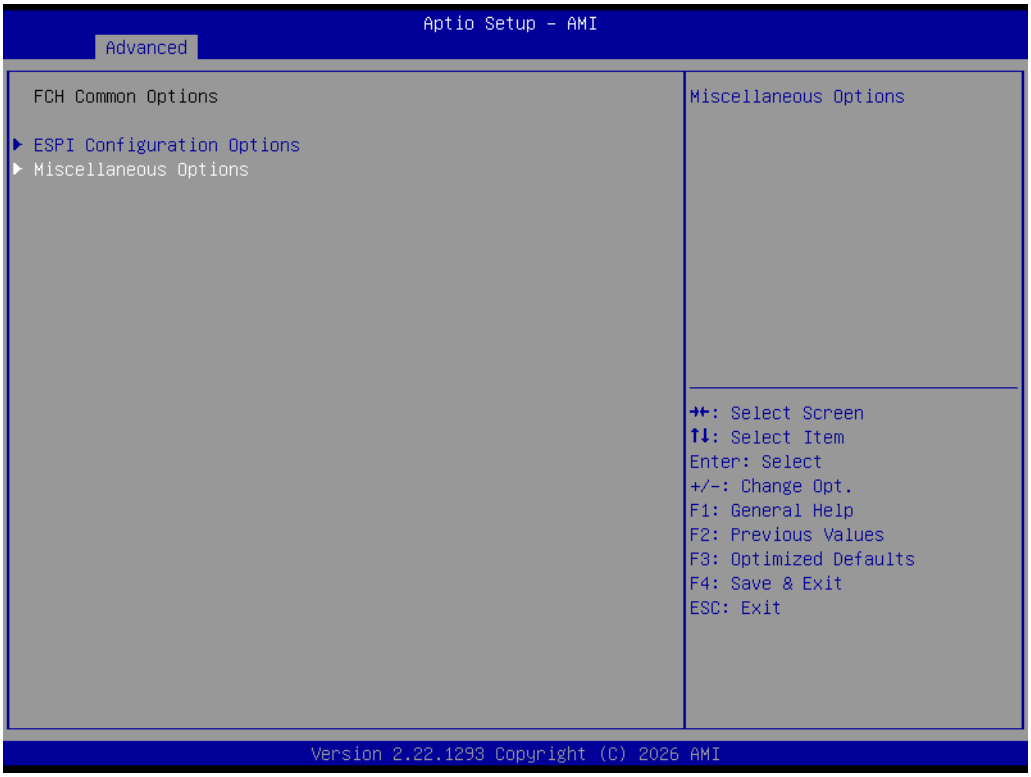

Aptio Setup – AMI
Advanced
SMU Common Options
TDP Control [Auto]
PPT Control [Auto]
Determinism Control [Auto]
APBDIS [Auto]
DfPstate Range Support [Auto]
Power Profile Selection [High Performance Mode]
BoostFmaxEn [Auto]
DF PState Frequency Optimizer [Auto]
DF Cstates [Auto]
CPPC [Auto]
HSMP Support [Auto]
SVI3 SVC Speed Control [Auto]
Diagnostic Mode [Auto]
PCIE Speed PMM Control [Auto]
Auto = Use the fused TDP
Manual = User can set customized TDP
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

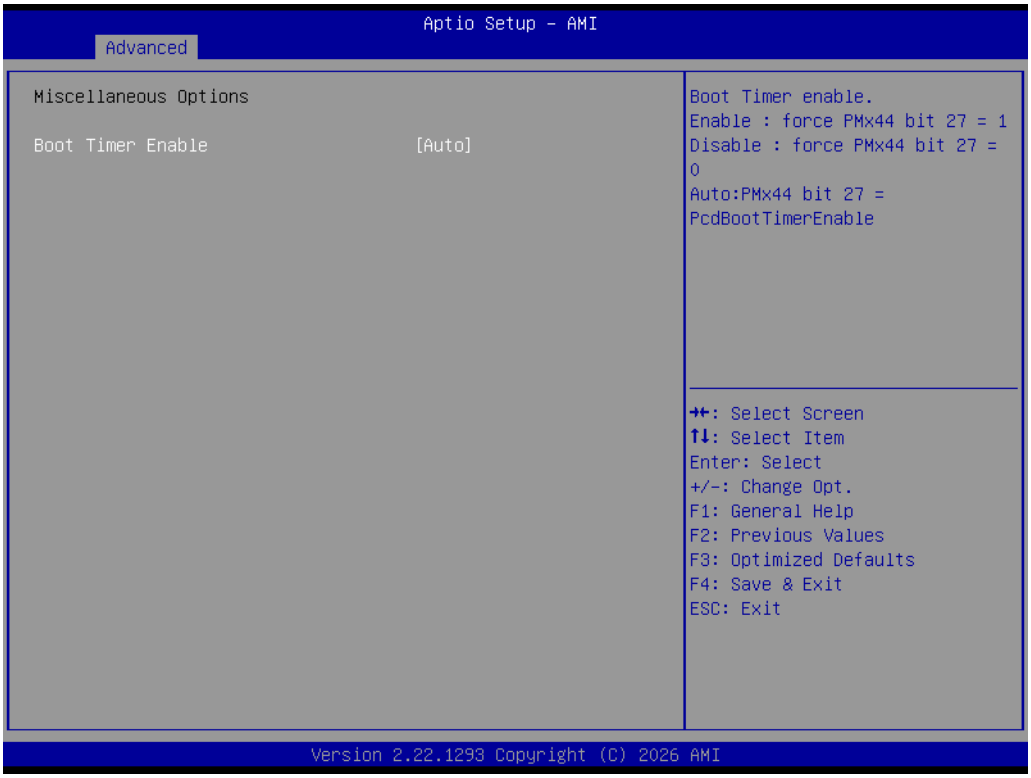

Aptio Setup – AMI
Advanced
NBIO Common Options
IOMMU [Disabled]
DMAr Support [Auto]
DMA Protection [Auto]
SMU Common Options
NBIO RAS Common Options
Enable AER Cap [Auto]
PCIE Link Speed Capability [Auto]
NBIO RAS Common Options
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

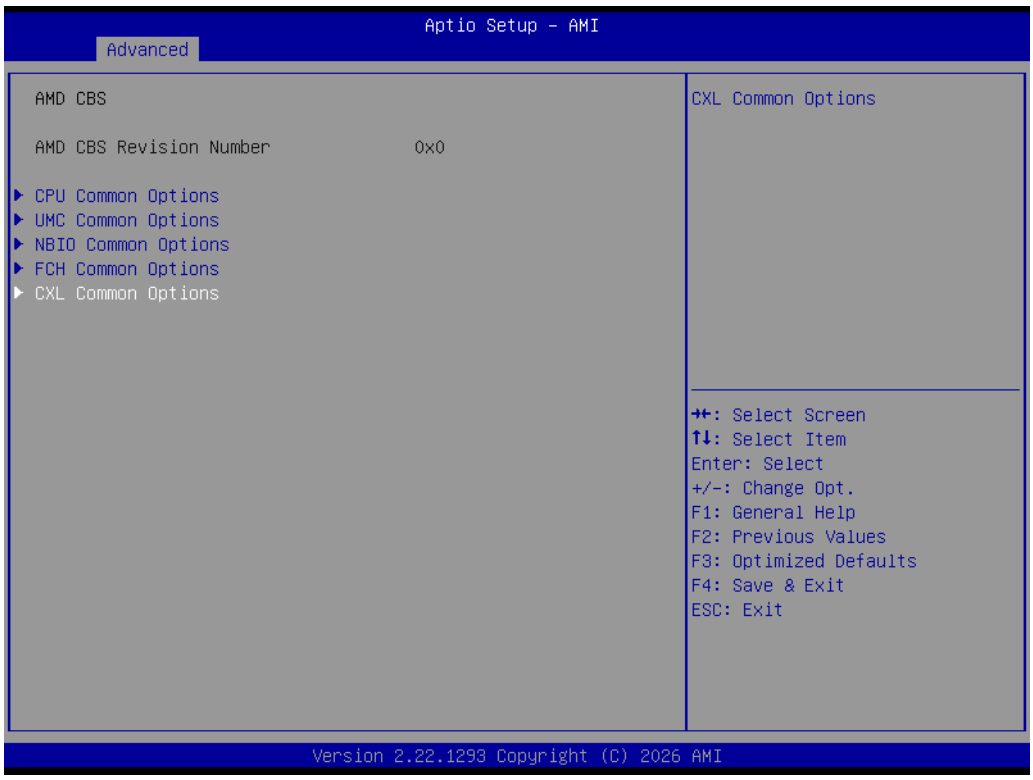

Aptio Setup – AMI
Advanced
NBIO RAS Common Options
PCIe Aer Reporting Mechanism [Auto]
This value selects the method of reporting AER errors from PCI Express. A value of 1 allows OS First handling of the errors through generation of a system control interrupt (SCI). A value of 2 provides for Firmware First handling of errors through generation of a system management interrupt (SMI).
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

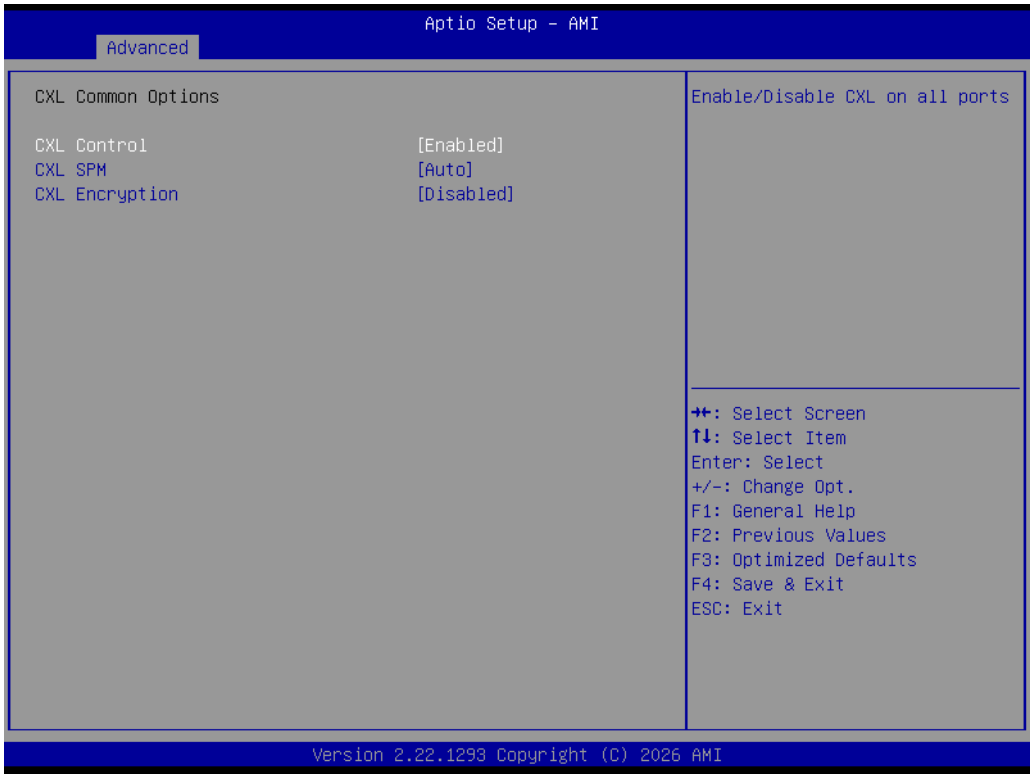

Aptio Setup – AMI
Advanced
AMD CBS
AMD CBS Revision Number 0x0
CPU Common Options
UMC Common Options
NBIO Common Options
FCH Common Options
CXL Common Options
FCH Common Options
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
ESPI Configuration Options
ESPI Enable [Enabled]
No help string
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
FCH Common Options
ESPI Configuration Options
Miscellaneous Options
Miscellaneous Options
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

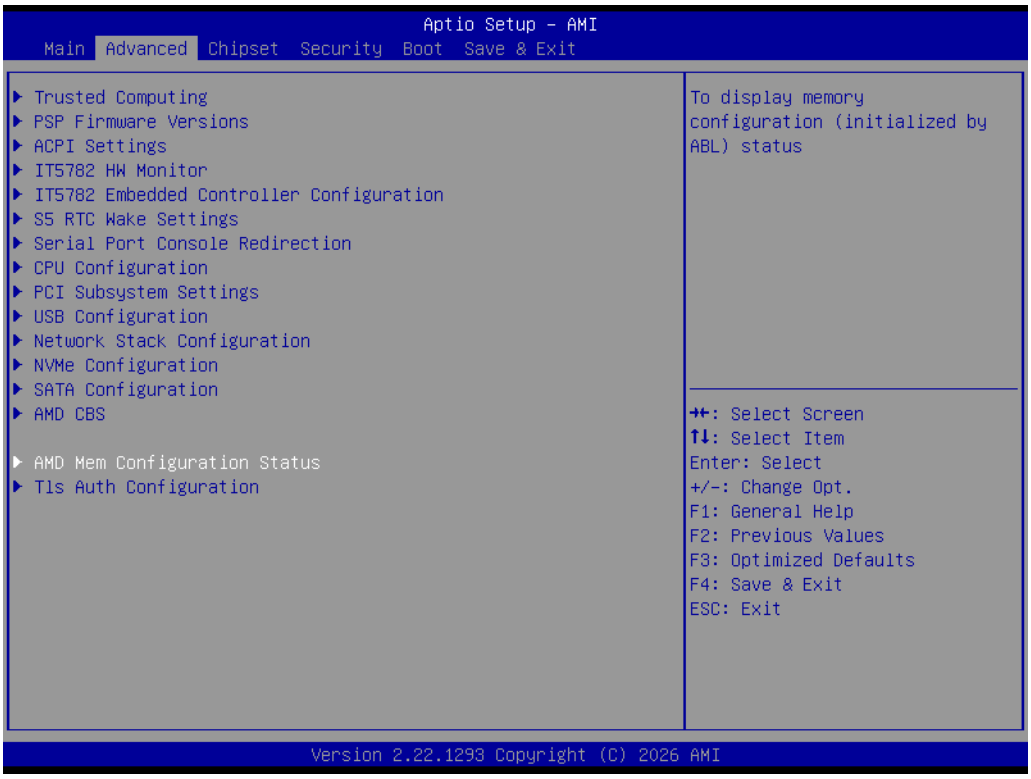

Aptio Setup – AMI
Advanced
Miscellaneous Options
Boot Timer Enable [Auto]
Boot Timer enable.
Enable : force PMx44 bit 27 = 1
Disable : force PMx44 bit 27 = 0
Auto:PMx44 bit 27 = PcdBootTimerEnable
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

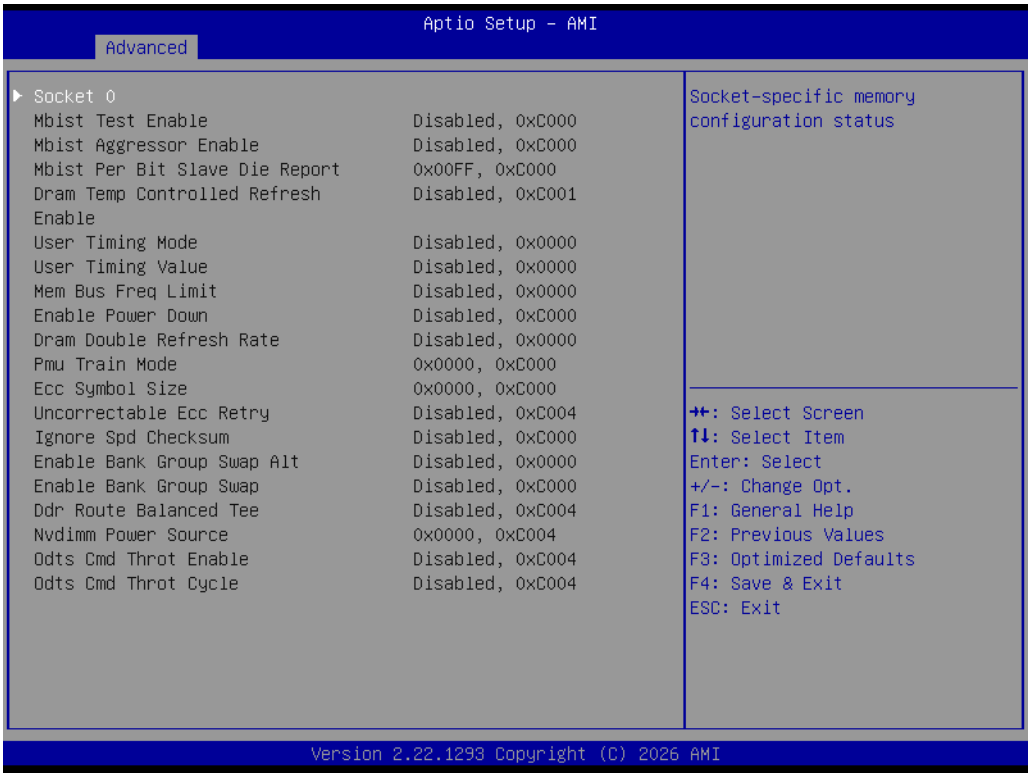

Aptio Setup – AMI
Advanced
AMD CBS
AMD CBS Revision Number 0x0
CPU Common Options
UMC Common Options
NBIO Common Options
FCH Common Options
CXL Common Options
CXL Common Options
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

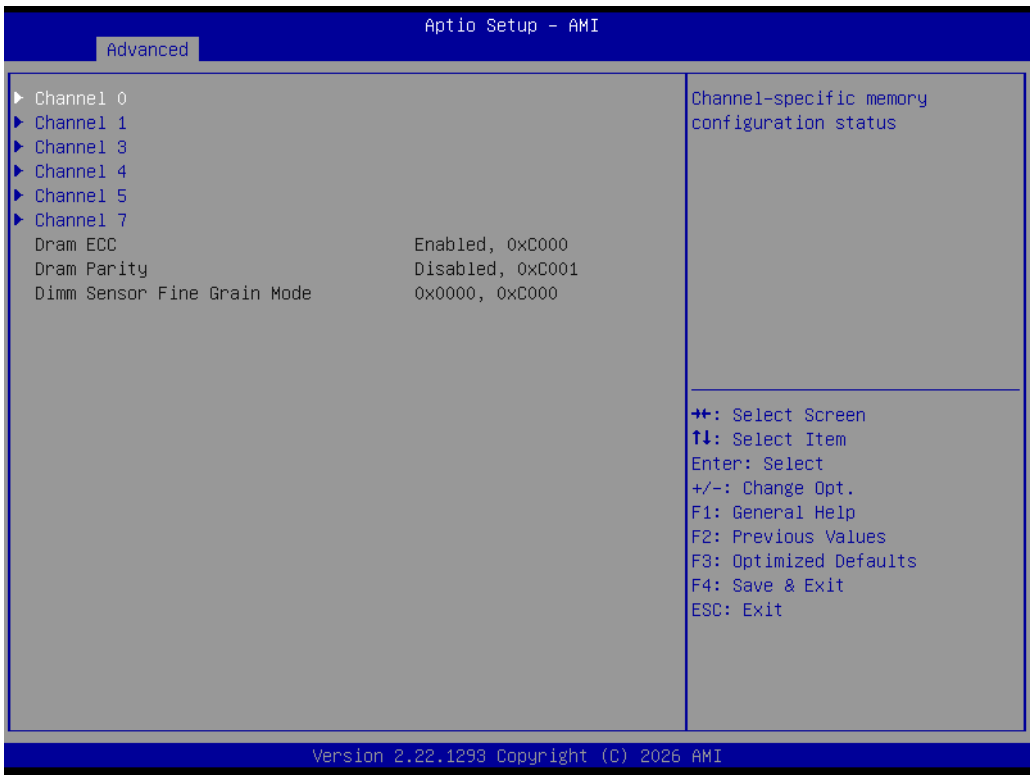

Aptio Setup – AMI
Advanced
CXL Common Options
CXL Control [Enabled]
CXL SPM [Auto]
CXL Encryption [Disabled]
Enable/Disable CXL on all ports
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

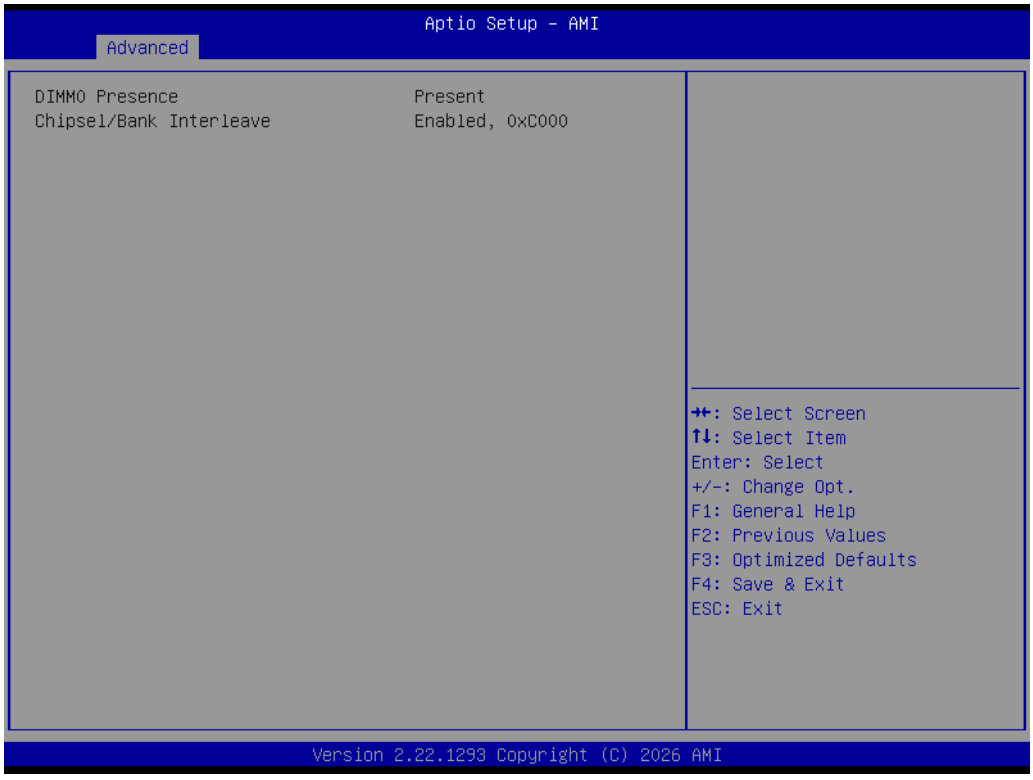
3.2.2.14 AMD Mem Configuration Status

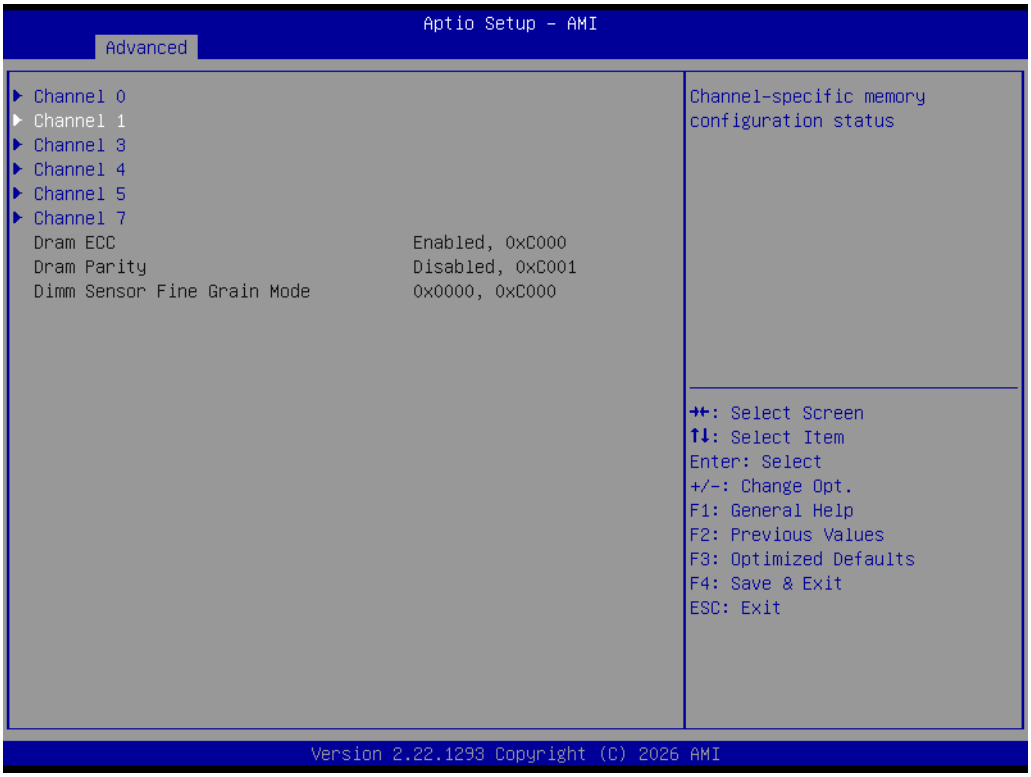
Advanced → AMD Mem Configuration Status

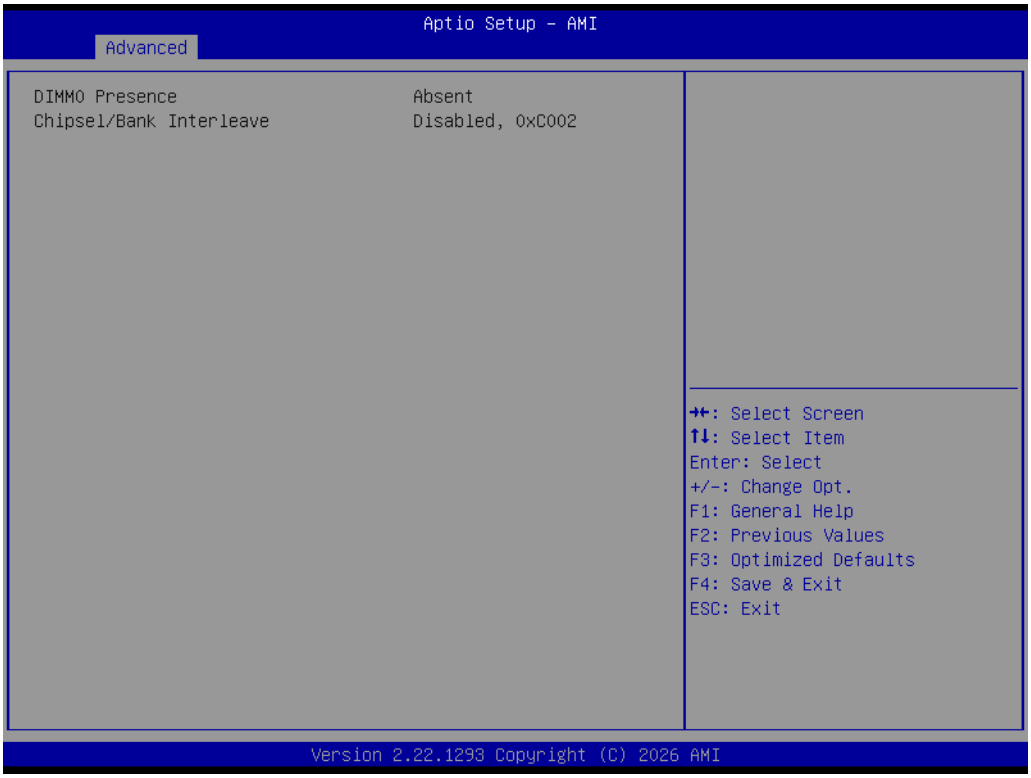


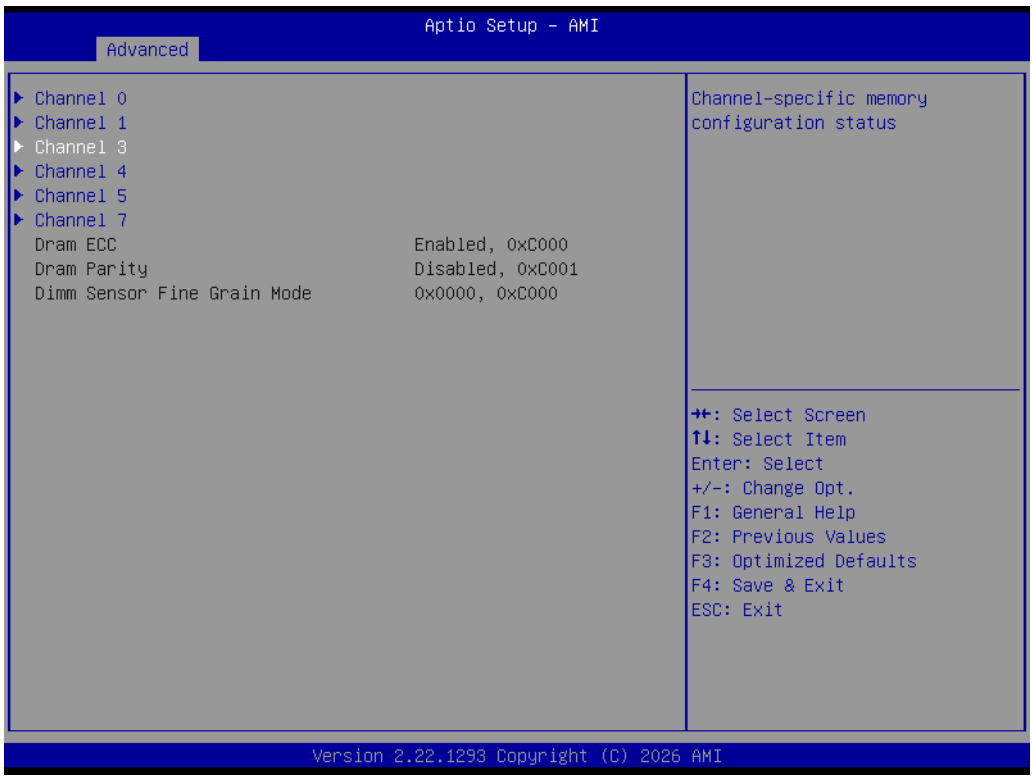


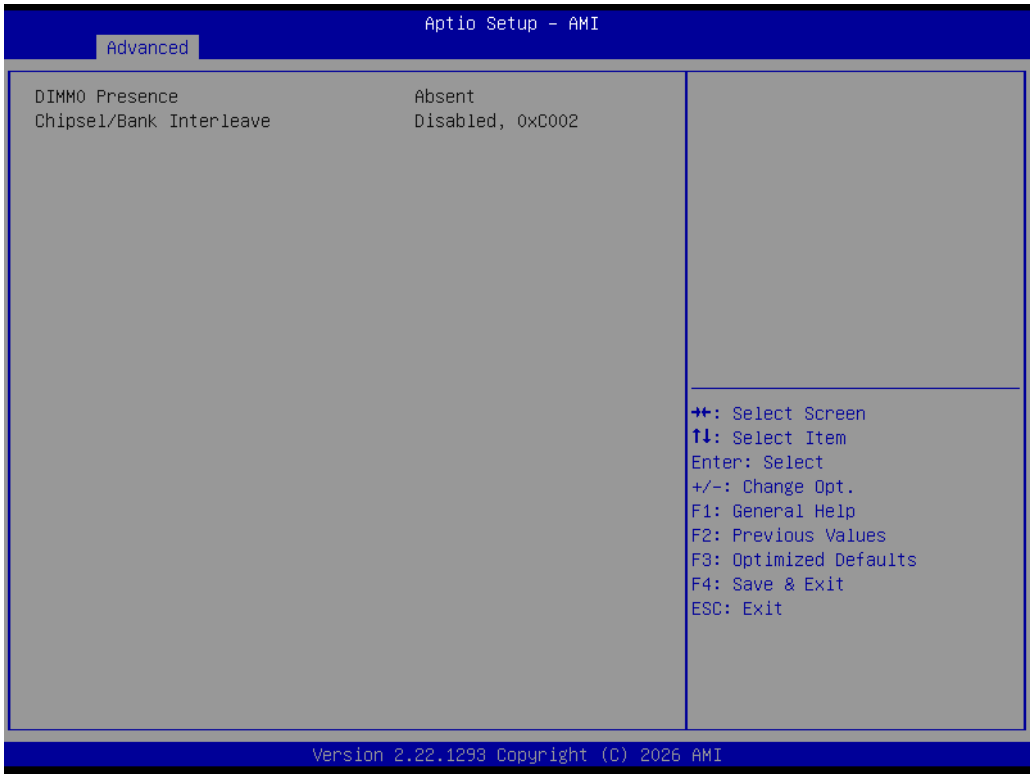

Aptio Setup – AMI
Advanced
Channel 0
Channel 1
Channel 3
Channel 4
Channel 5
Channel 7
Dram ECC Enabled, 0xC000
Dram Parity Disabled, 0xC001
Dimm Sensor Fine Grain Mode 0x0000, 0xC000
Channel-specific memory configuration status
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

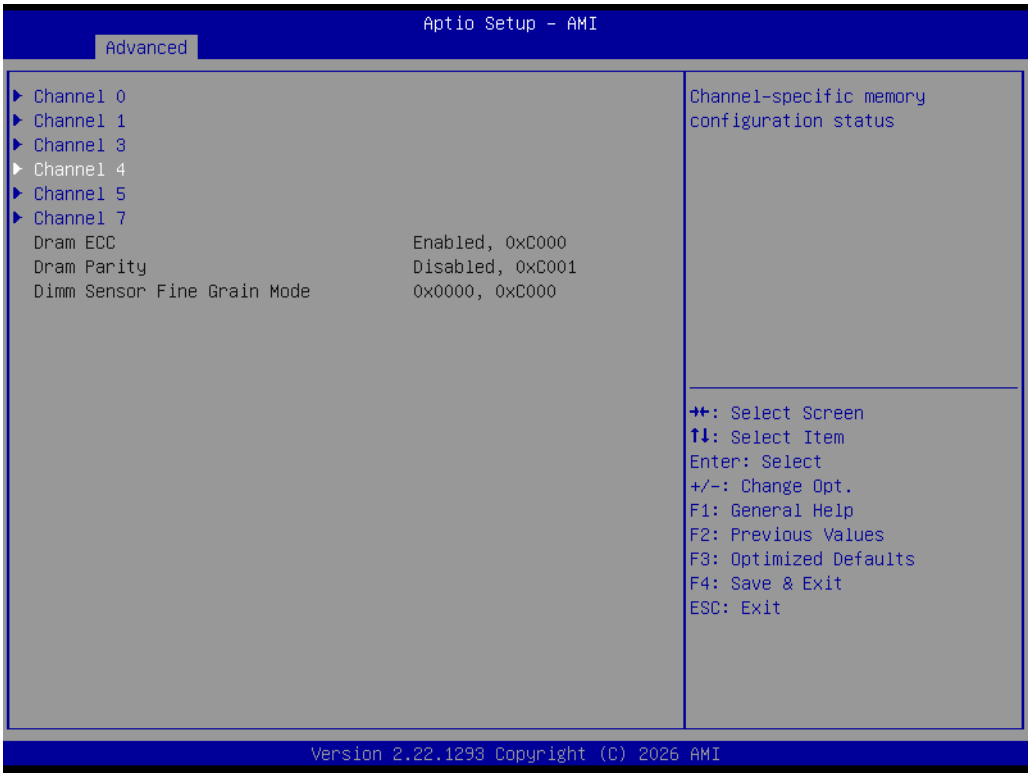

Aptio Setup – AMI
Advanced
DIMM0 Presence Present
Chipsel/Bank Interleave Enabled, 0xC000
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

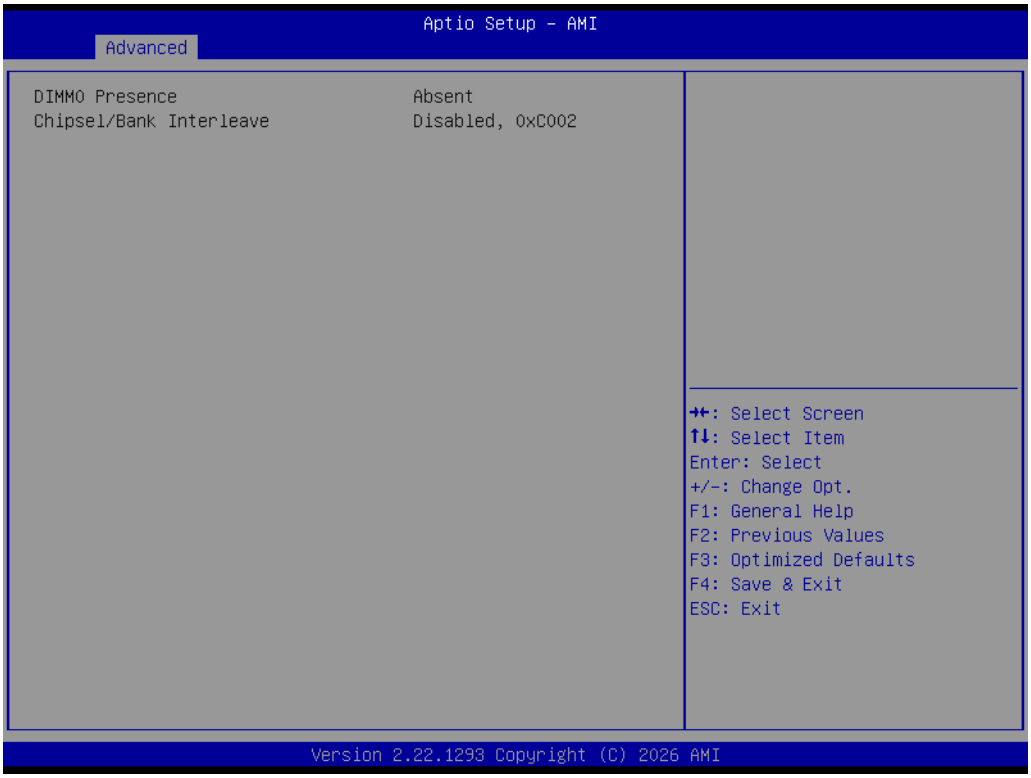

Aptio Setup – AMI
Advanced
Channel 0
Channel 1
Channel 3
Channel 4
Channel 5
Channel 7
Dram ECC
Enabled, 0xC000
Dram Parity
Disabled, 0xC001
Dimm Sensor Fine Grain Mode
0x0000, 0xC000
Channel-specific memory configuration status
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

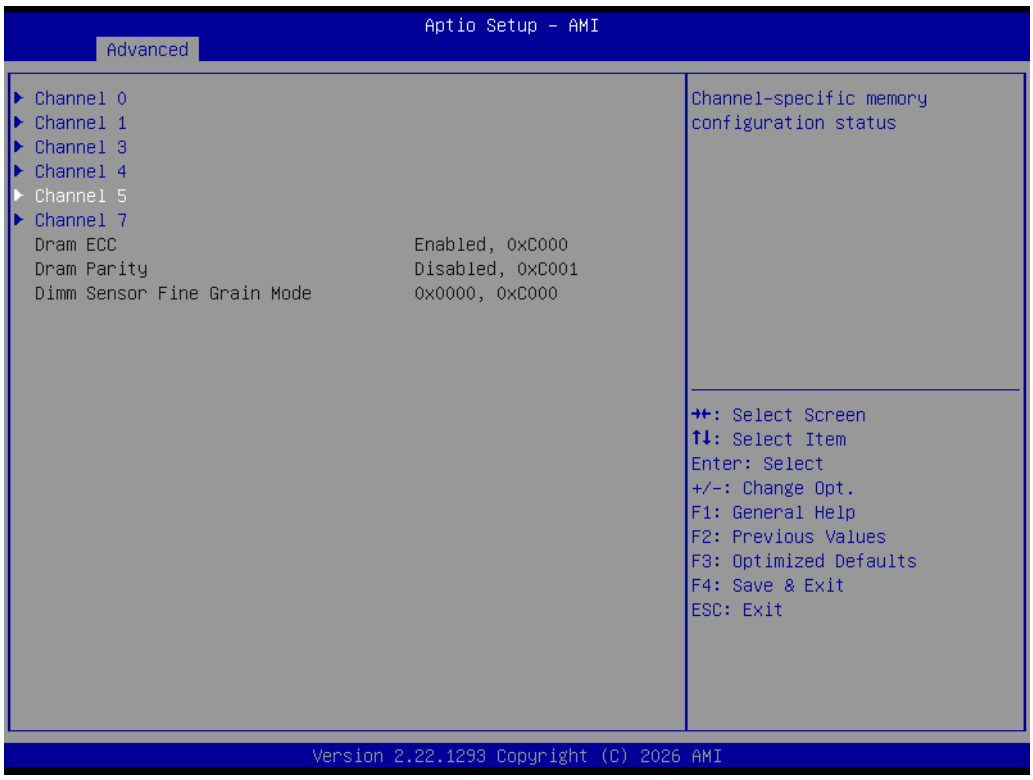

Aptio Setup – AMI
Advanced
DIMM0 Presence
Absent
Chipsel/Bank Interleave
Disabled, 0xC002
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
Channel 0
Channel 1
Channel 3
Channel 4
Channel 5
Channel 7
Dram ECC Enabled, 0xC000
Dram Parity Disabled, 0xC001
Dimm Sensor Fine Grain Mode 0x0000, 0xC000
Channel-specific memory configuration status
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
DIMM0 Presence Absent
Chipsel/Bank Interleave Disabled, 0xC002
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
Channel 0
Channel 1
Channel 3
Channel 4
Channel 5
Channel 7
Dram ECC
Enabled, 0xC000
Dram Parity
Disabled, 0xC001
Dimm Sensor Fine Grain Mode
0x0000, 0xC000
Channel-specific memory configuration status
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
DIMM0 Presence
Absent
Chipsel/Bank Interleave
Disabled, 0xC002
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
Channel 0
Channel 1
Channel 3
Channel 4
Channel 5
Channel 7
Dram ECC Enabled, 0xC000
Dram Parity Disabled, 0xC001
Dimm Sensor Fine Grain Mode 0x0000, 0xC000
Channel-specific memory configuration status
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
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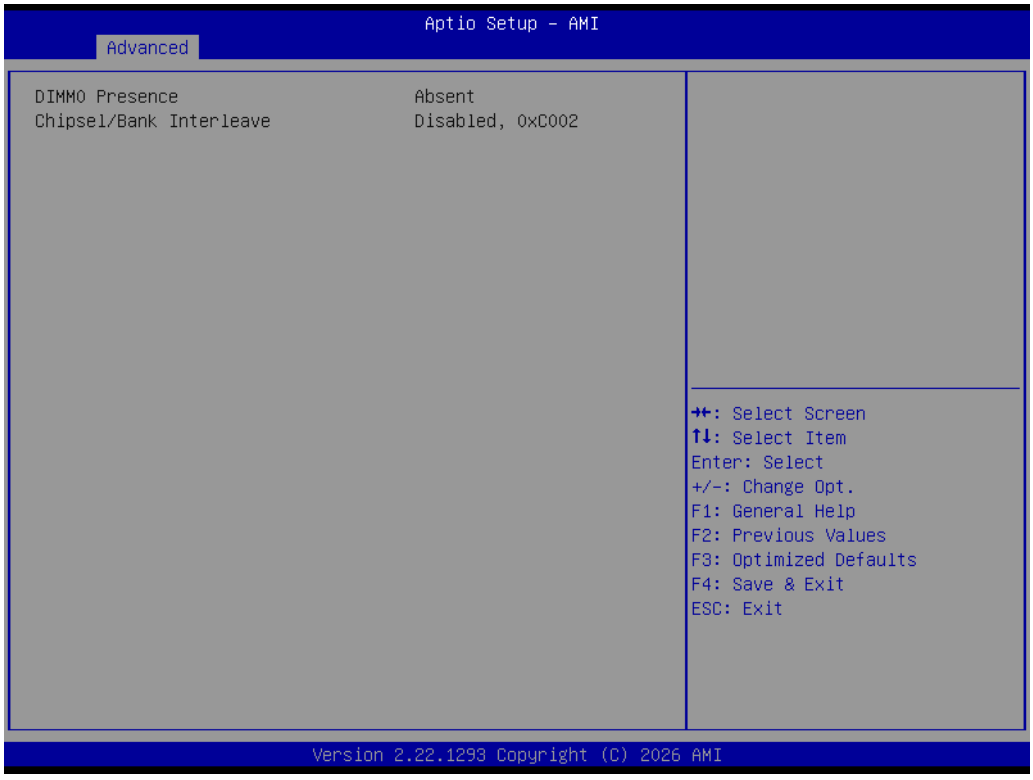
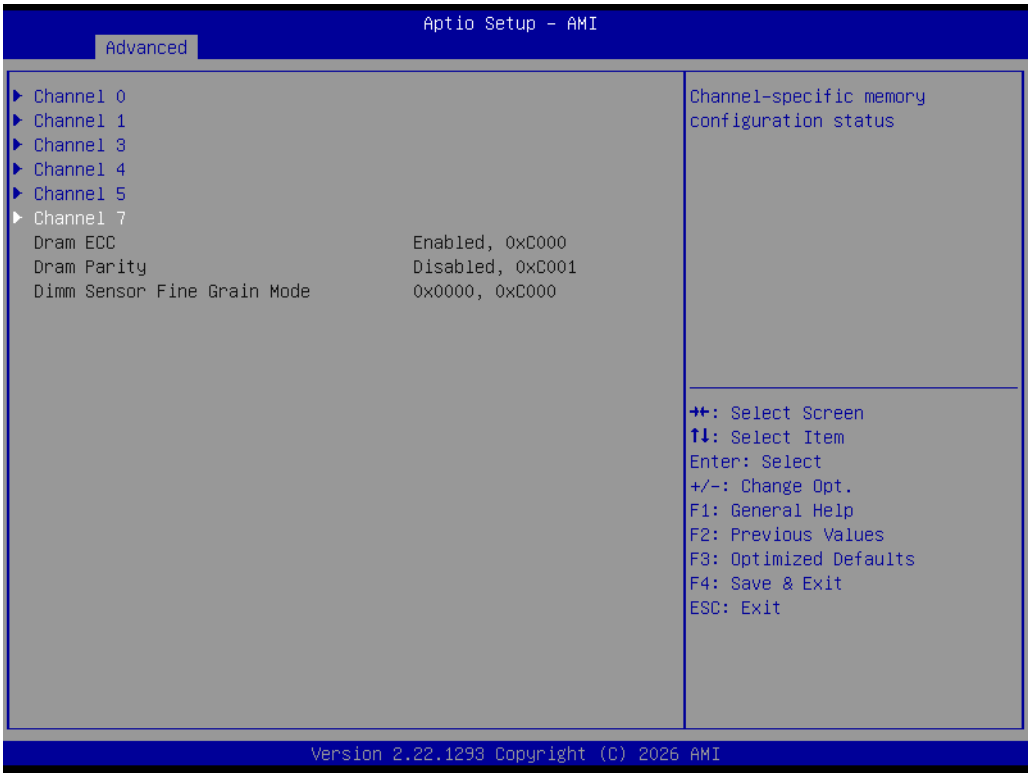
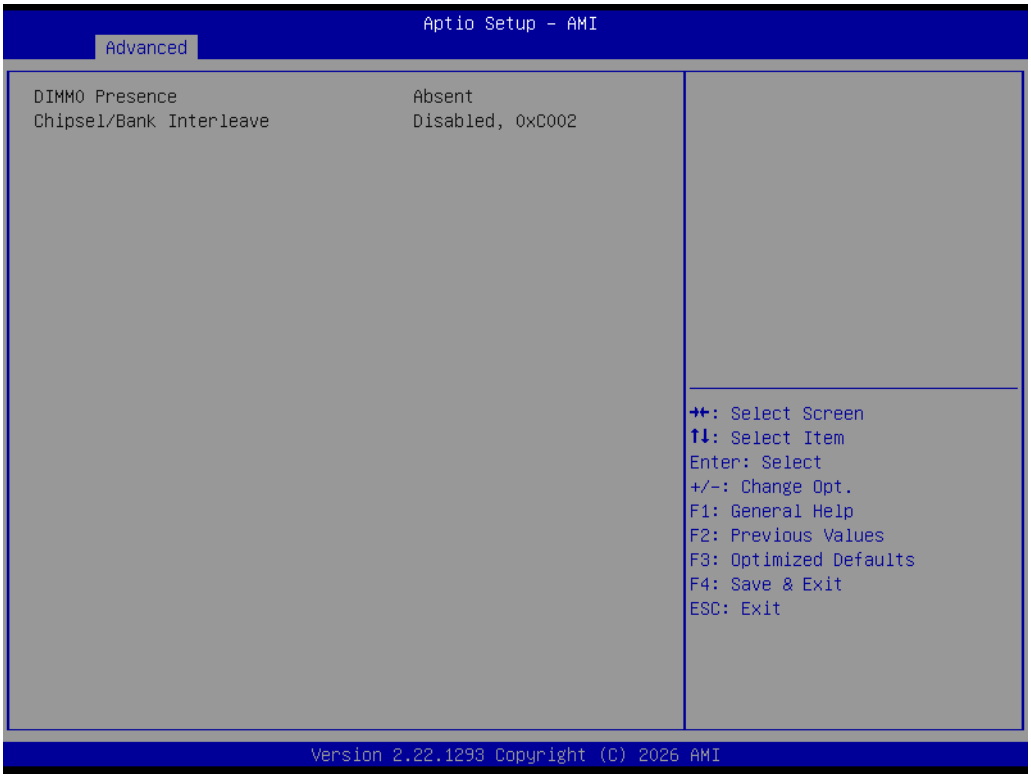

Aptio Setup – AMI
Advanced
DIMM0 Presence Absent
Chipsel/Bank Interleave Disabled, 0xC002
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
Channel 0
Channel 1
Channel 3
Channel 4
Channel 5
Channel 7
Dram ECC Enabled, 0xC000
Dram Parity Disabled, 0xC001
Dimm Sensor Fine Grain Mode 0x0000, 0xC000
Channel-specific memory configuration status
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
DIMM0 Presence Absent
Chipsel/Bank Interleave Disabled, 0xC002
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
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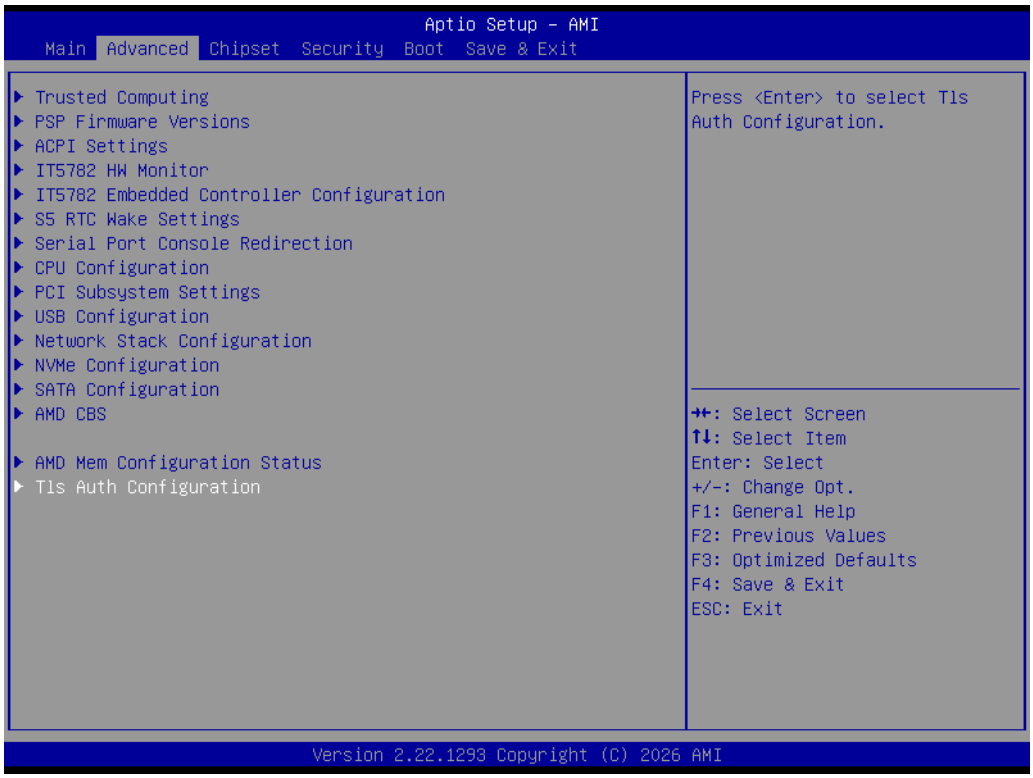
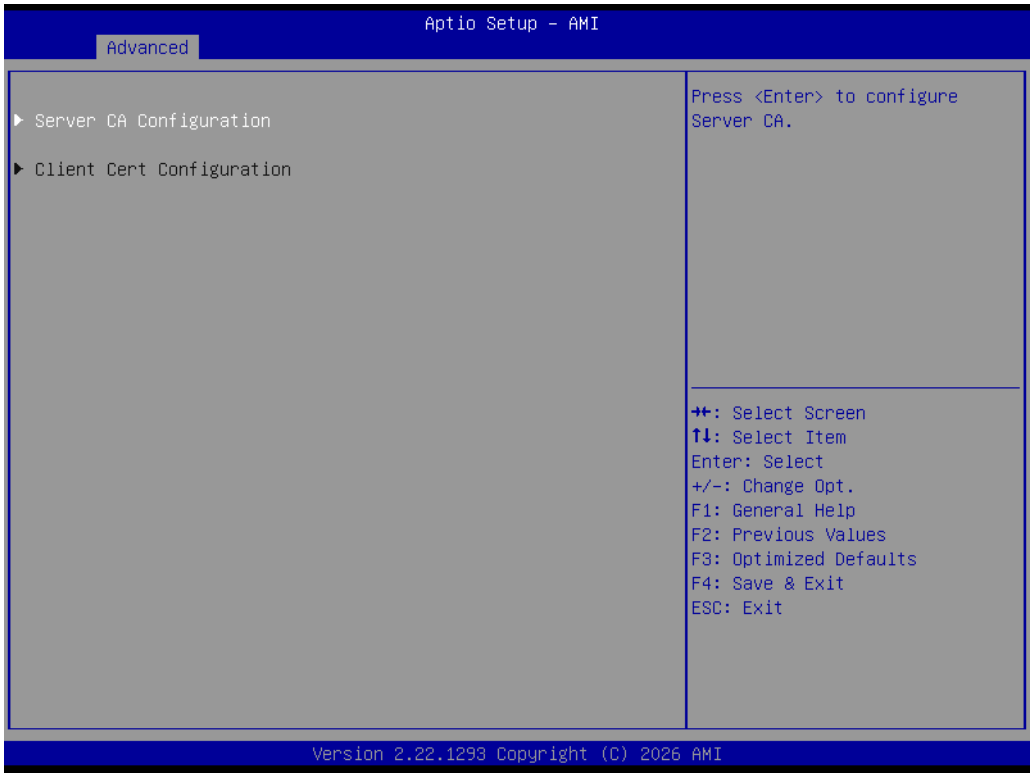
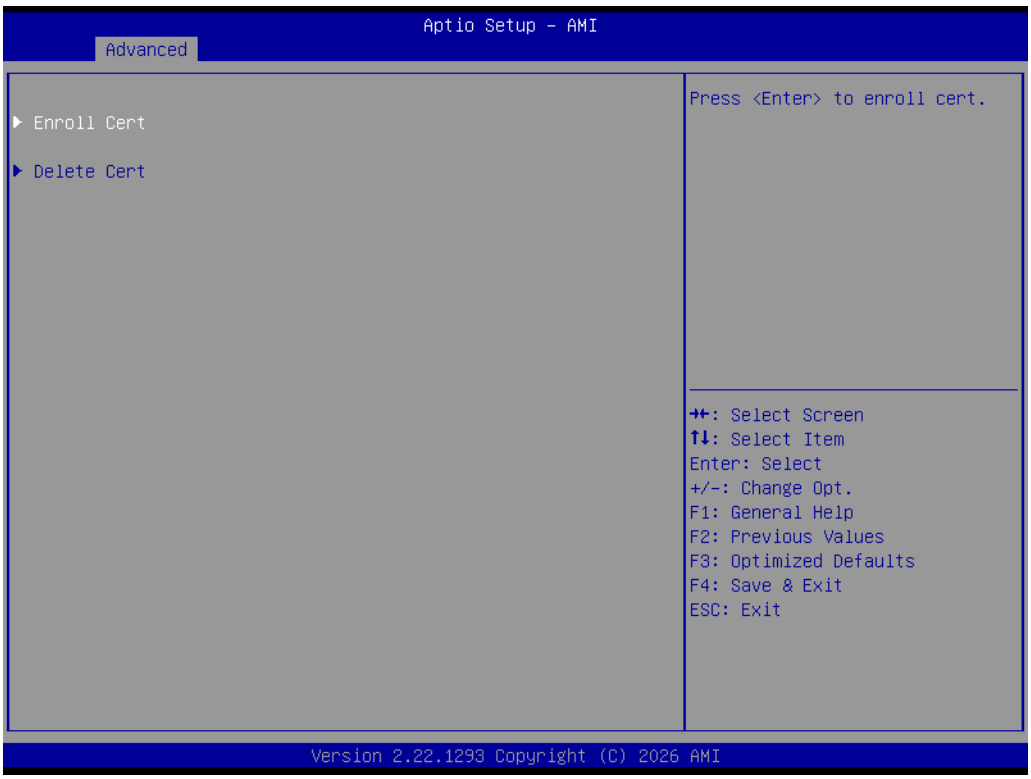
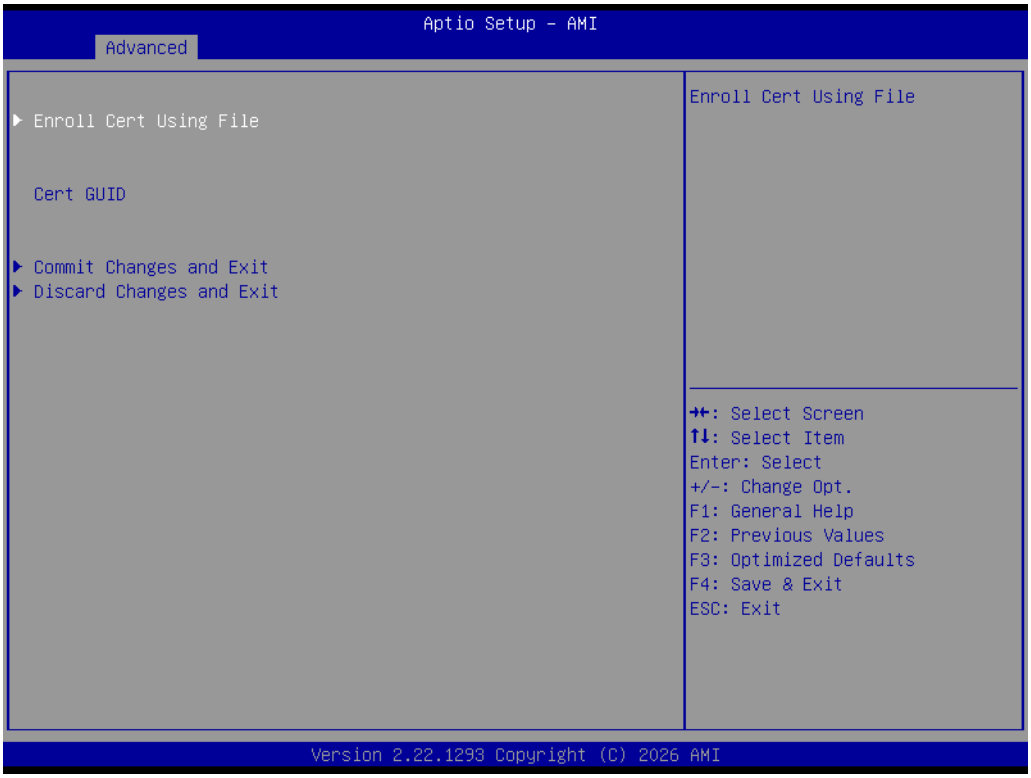
3.2.2.15 Tls Auth Configuration

Advanced → Tls Auth Configuration



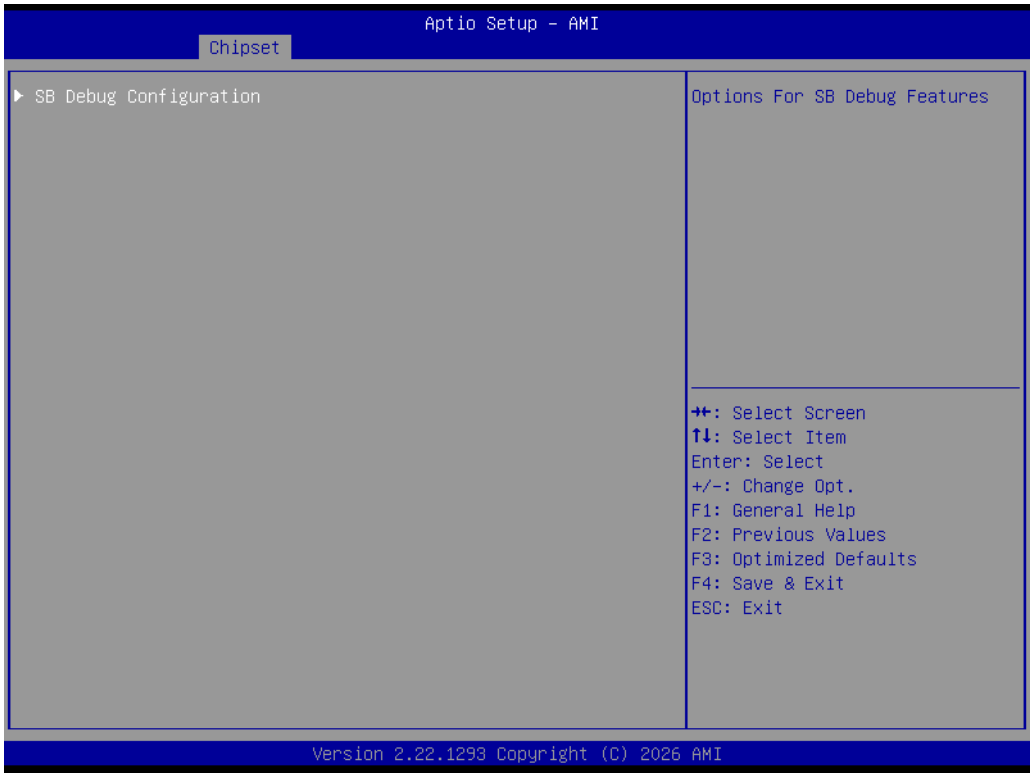



Aptio Setup – AMI
Advanced
Enroll Cert
Delete Cert
Press <Enter> to enroll cert.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

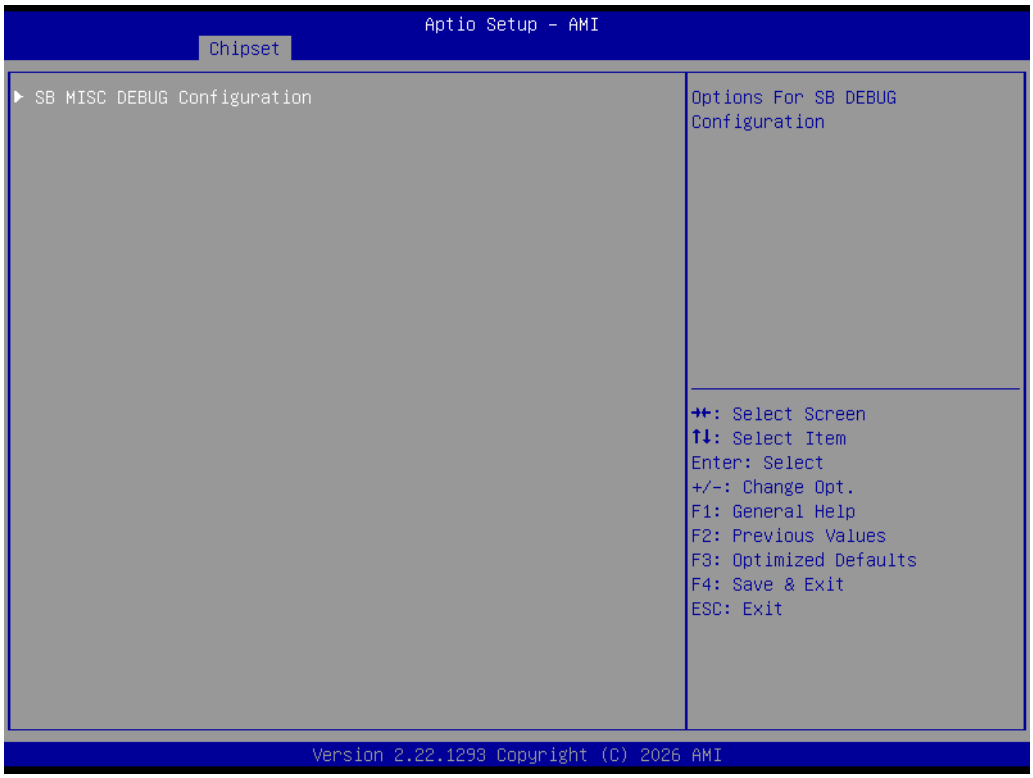

Aptio Setup – AMI
Advanced
Enroll Cert Using File
Cert GUID
Commit Changes and Exit
Discard Changes and Exit
Enroll Cert Using File
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

3.2.3 Chipset

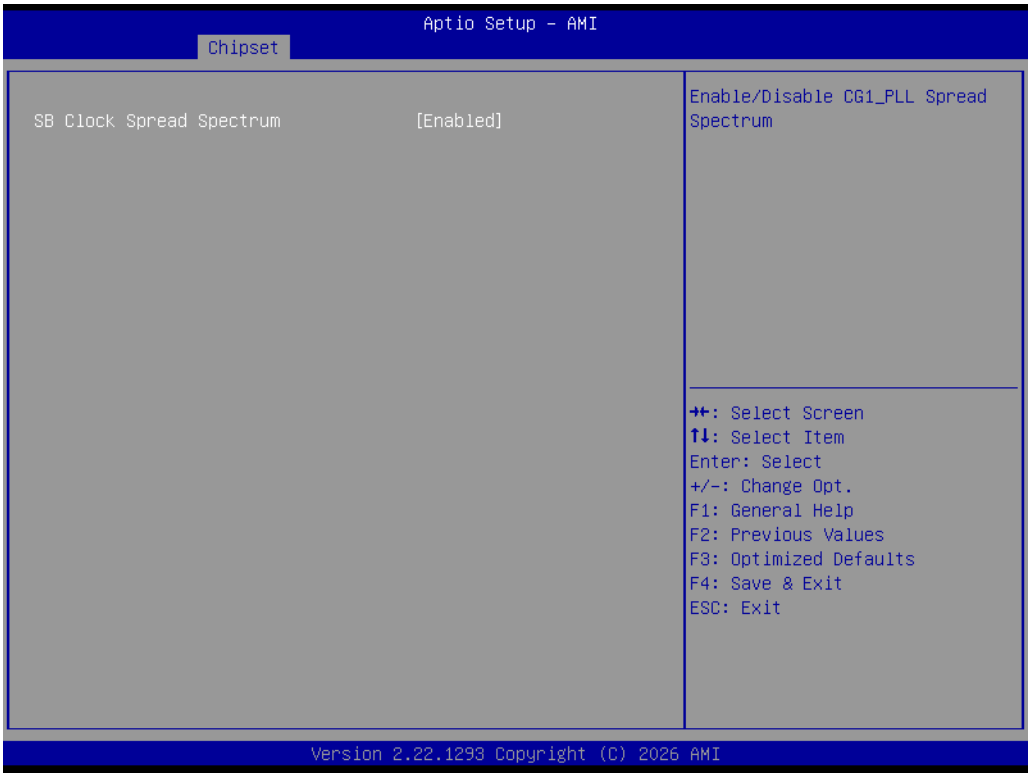
3.2.3.1 SB Debug Configuration



3.2.3.2 SB MISC DEBUG Configuration

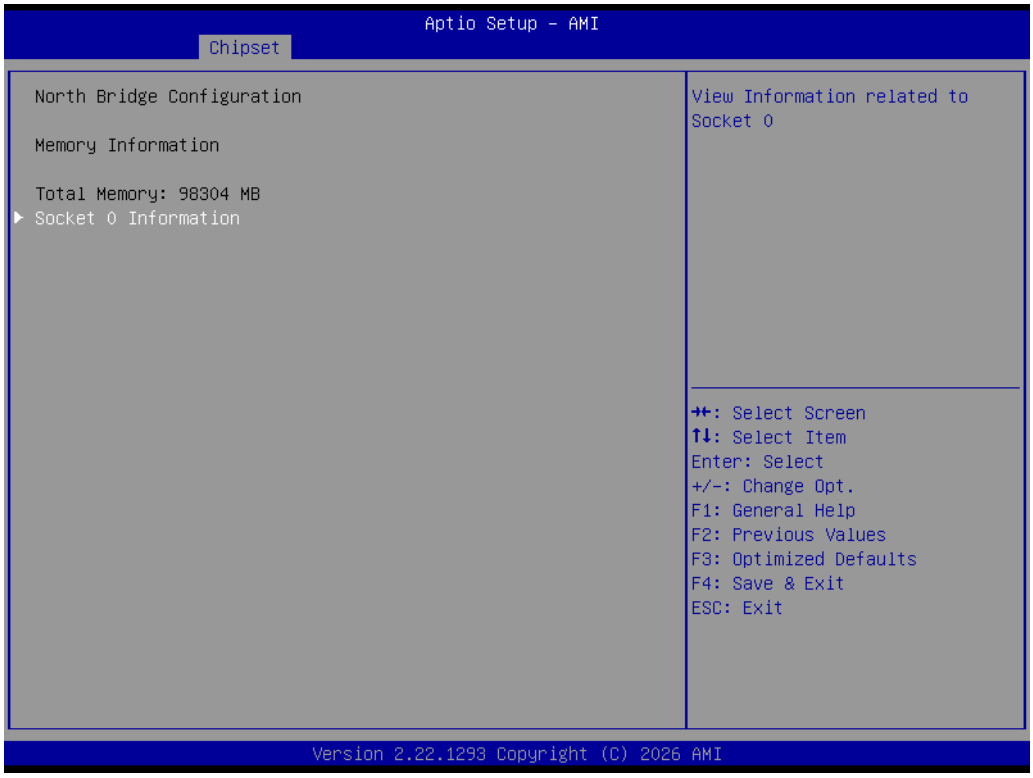


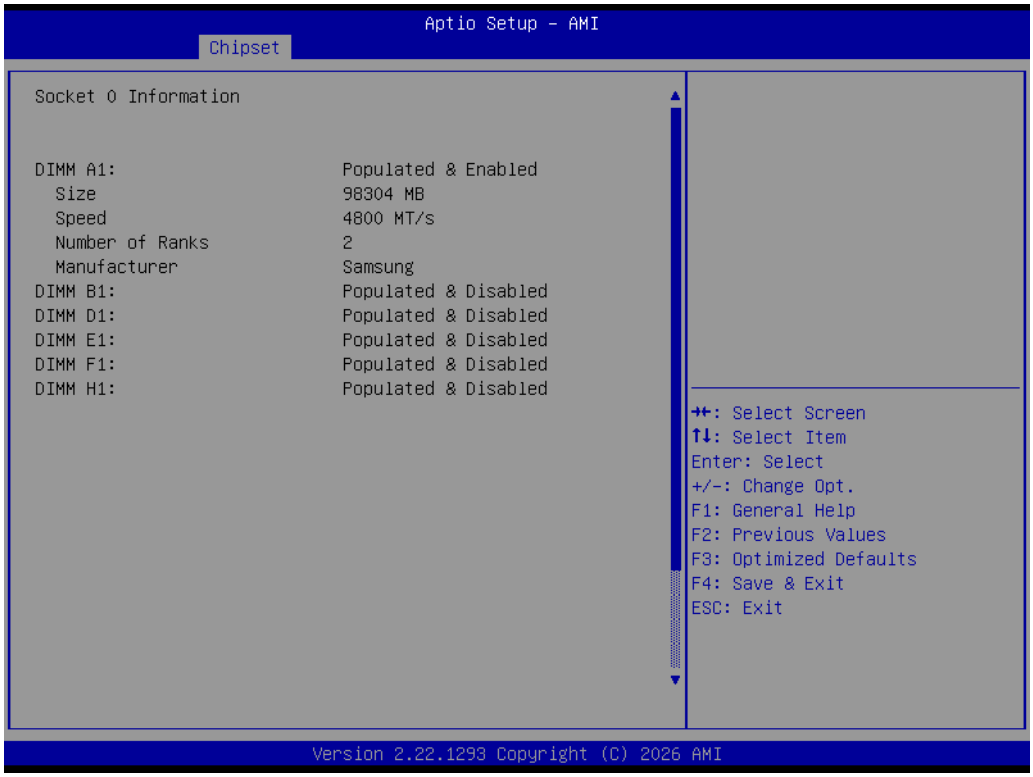
3.2.3.3 SB Clock Spread Spectrum



3.2.3.4 North Bridge

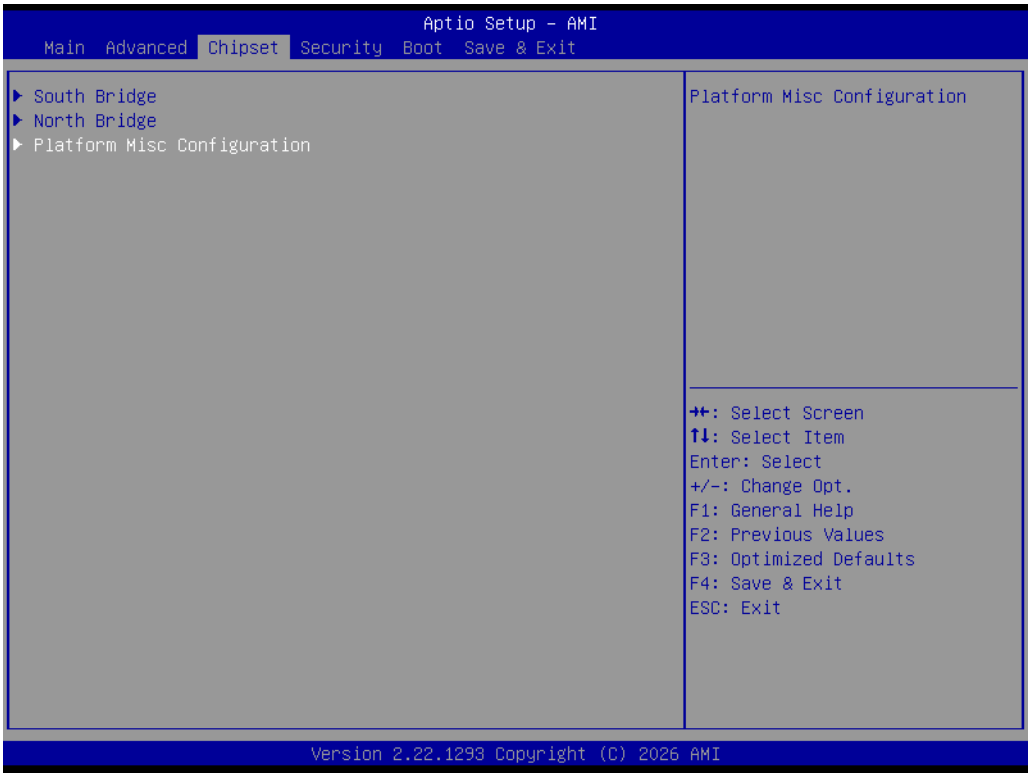
Chipset → North Bridge


Aptio Setup – AMI
Chipset
North Bridge Configuration
Memory Information
Total Memory: 98304 MB
Socket 0 Information
View Information related to Socket 0
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

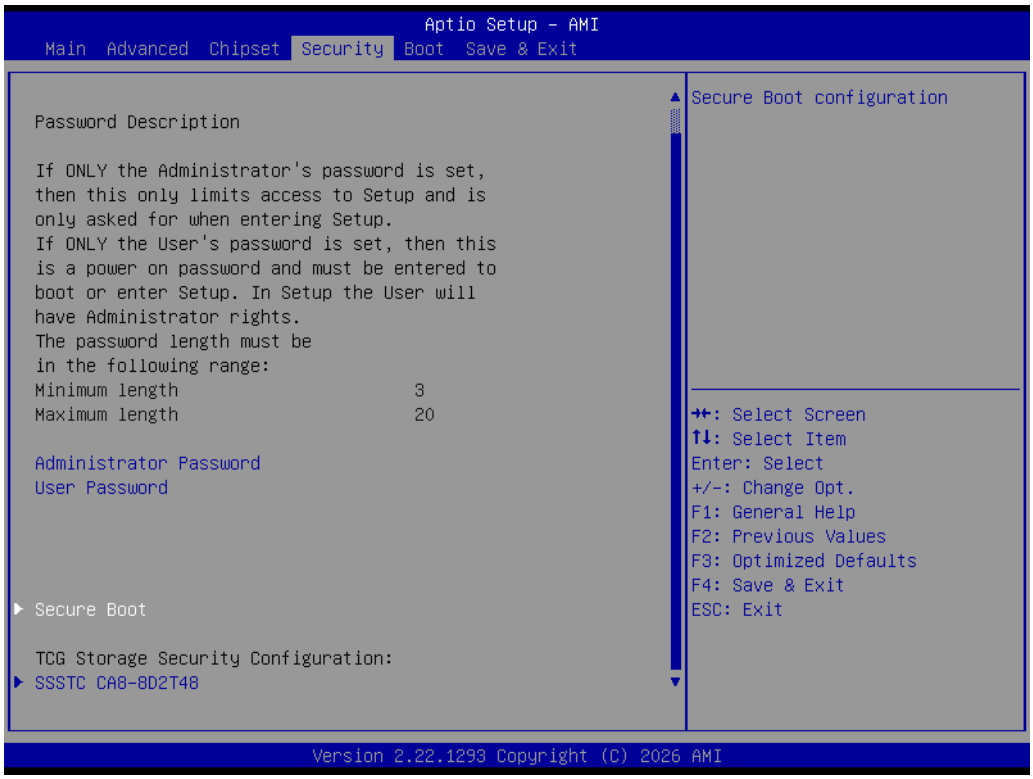

Aptio Setup – AMI
Chipset
Socket 0 Information
DIMM A1: Populated & Enabled
Size 98304 MB
Speed 4800 MT/s
Number of Ranks 2
Manufacturer Samsung
DIMM B1: Populated & Disabled
DIMM D1: Populated & Disabled
DIMM E1: Populated & Disabled
DIMM F1: Populated & Disabled
DIMM H1: Populated & Disabled
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1293 Copyright (C) 2026 AMI

3.2.3.5 North Bridge

Chipset → Platform Misc Configuration

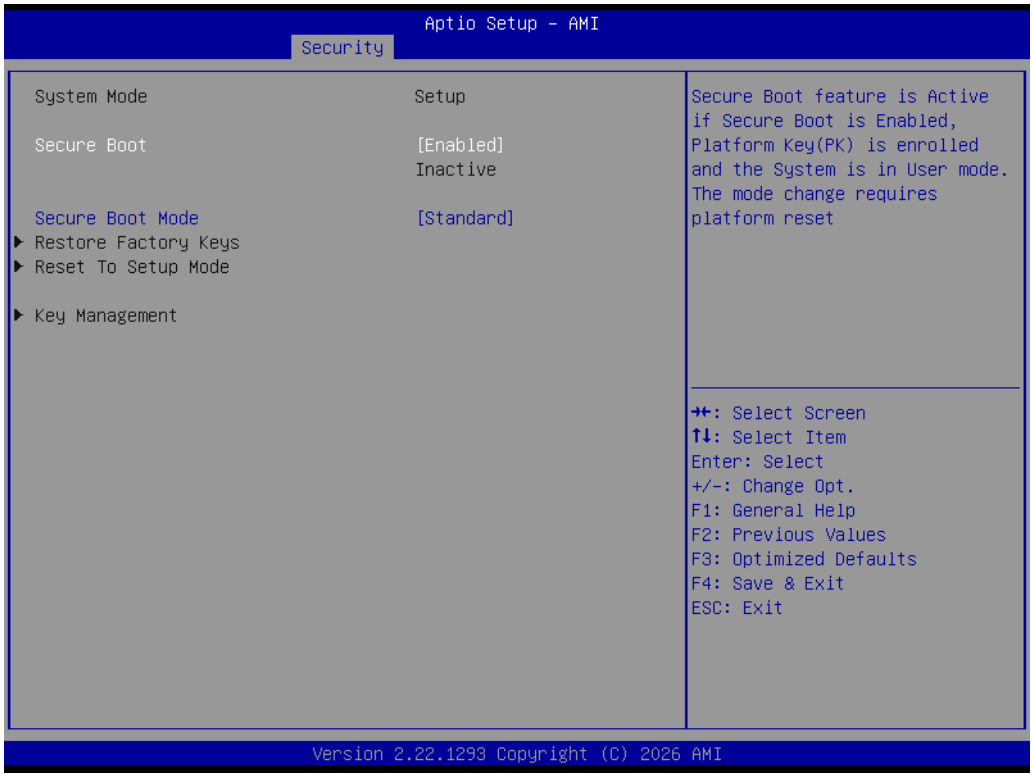


3.2.4 Security

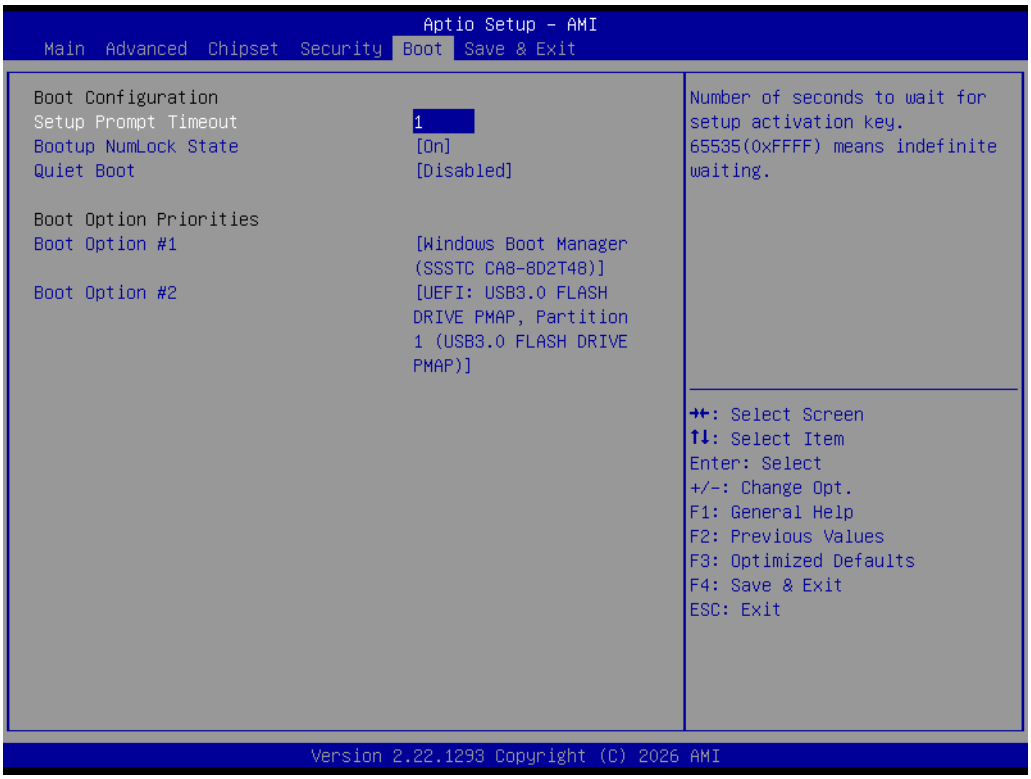


Secure Boot

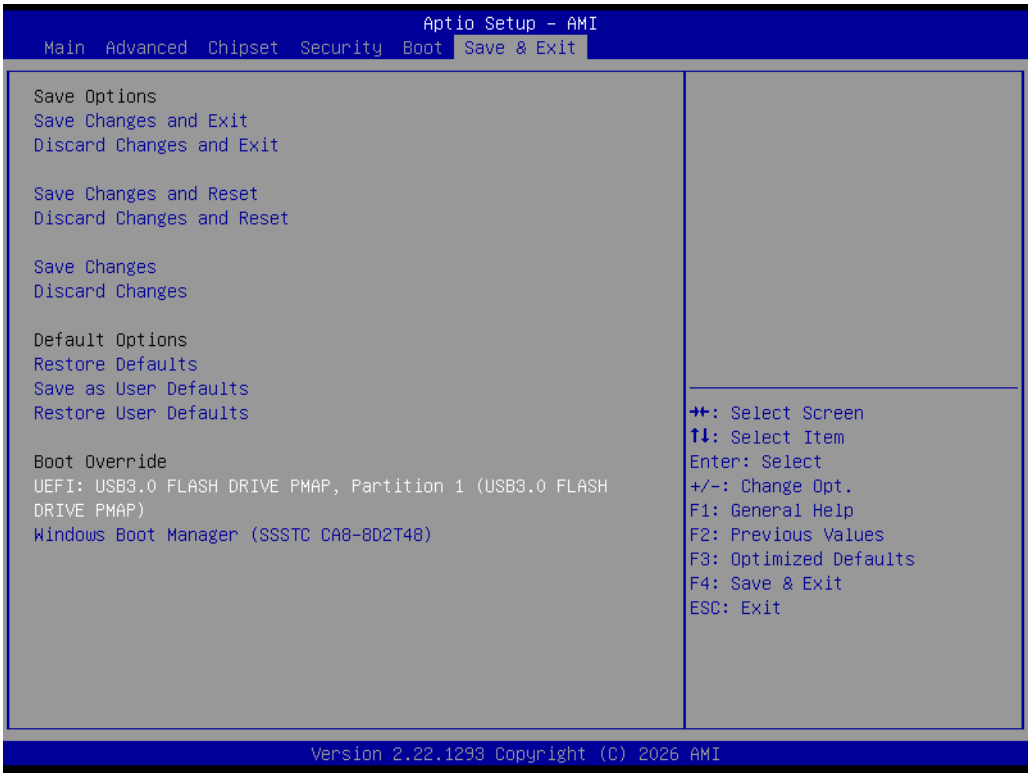
Security → Secure Boot



3.2.5 Boot Settings



3.2.6 Save & Exit Configuration



Chapter 4

Software Introduction & Service

4.1 Introduction

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft® Windows® embedded technology." We enable Windows® Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows® Embedded Software solutions easily and widely available to the embedded computing community.

4.2 Value-Added Software Services

Software API: An interface that defines the ways by which an application program may request services from libraries and/or operating systems. Provides not only the underlying drivers required but also a rich set of user-friendly, intelligent and integrated interfaces, which speeds development, enhances security and offers add-on value for Advantech platforms. It plays the role of catalyst between developer and solution, and makes Advantech embedded platforms easier and simpler to adopt and operate with customer applications.

4.2.1 Software API

4.2.1.1 Control

GP I/O

General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch on/off the device. Our API also provides Programmable GPIO, which allows developers to dynamically set the GPIO input or output status.

SMBus

SMBus is the System Management Bus defined by Intel Corporation in 1995. It is used in personal computers and servers for low-speed system management communications. The SMBus API allows a developer to interface with an embedded system environment and transfer serial messages using the SMBus protocol, allowing control of multiple devices simultaneously.

4.2.1.2 Display

Brightness Control

The Brightness Control API allows a developer to access embedded devices and easily control brightness.

Backlight

The Backlight API allows a developer to control the backlight (screen) on/off in embedded devices.

4.2.1.3 Monitor

Watchdog

A watchdog timer (WDT) is a device that automatically performs a predefined action if the system becomes unresponsive and does not recover within a specified period. A watchdog timer can be programmed to perform a warm boot (restart the system) after a specified number of seconds.

Hardware Monitor

The Hardware Monitor (HWM) API is a system health supervision API that inspects certain condition indexes, such as fan speed, temperature and voltage.

4.2.1.4 Power Saving

CPU Speed

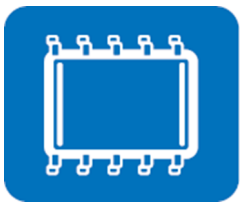
Makes use of Intel SpeedStep BIOS technology to save power consumption. The system will automatically adjust the CPU speed depending on the system loading.

System Throttling

Refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. This API allows the user to adjust the clock from 87.5% to 12.5%.

4.2.2 Software Utility

BIOS Flash



The BIOS Flash utility allows users to update the BIOS stored in the flash ROM or back up the current BIOS by copying it from the flash ROM to a file on disk. The BIOS Flash utility also provides a command-line version and an API for easy integration with customized applications.

Embedded Security ID

The embedded application is one of the most valuable assets of a system integrator. It contains valuable intellectual property, design knowledge, and innovation, making it vulnerable to unauthorized access and misuse. The Embedded Security ID utility provides reliable security features that help protect application data stored in the embedded BIOS.

Monitoring

The Monitoring utility allows users to monitor system health, including voltage, CPU and system temperature, and fan speed. These parameters are critical to system operation. If critical errors occur and are not resolved immediately, permanent damage may result.

Chapter 5

Chipset Software Installation Utility

5.1 Before You Begin

To facilitate the installation of the enhanced display drivers and utility software, read the instructions in this chapter carefully. The drivers for the AIMB-593 are located on the Advantech support website: http://support.advantech.com/Support/. The drivers on the support website will guide and link you to the utilities and drivers under a Windows system. Updates are provided via Service Packs from Microsoft*.

Note! *The driver files on the website are compressed. Do not attempt to install the drivers by copying the files manually. You must download the files and decompress them first. Also, please use the supplied SETUP program to install the drivers.*

Before you begin, it is important to note that most display drivers need to have the relevant software application already installed in the system prior to installing the enhanced display drivers. In addition, many of the installation procedures assume that you are familiar with both the relevant software applications and operating system commands. Review the relevant operating system commands and the pertinent sections of your application software's user manual before performing the installation.

5.2 Introduction

The AMD Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured. This is needed for the proper functioning of the following features:

- Core PCI PnP services
- USB support
- Identification of AMD chipset components in the Device Manager

Note! *This utility is used for the following versions of Windows, and it has to be installed before installing all the other drivers:*

- *Windows 11 (64-bit)*
- *Windows Server (64-bit)*

Chapter 6

LAN Configuration

6.1 Introduction

The AIMB-593 system features four Gigabit Ethernet LANs via dedicated PCI Express x4 lanes (Lan1/LAN2: Intel I226-LM 2.5 GbE, LAN3/LAM4: Intel X710-AT2 10 GbE) that offer a bandwidth of up to 500 MB/sec, eliminating bottlenecks in the flow of network data by incorporating Gigabit Ethernet at 1000 Mbps.

6.2 Features

- Integrated 10/100/1000/2500/10000 Mbps transceiver
- 10/100/1000/2500/10000 Mbps triple-speed MAC
- High-speed RISC core with 24-KB cache
- On-chip voltage regulation
- Wake-on-LAN (WOL) support
- PCI Express X4 host interface

6.3 Installation

Note! *Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.*

The Intel I226-LM (LAN1/LAN2), Intel X710-AT2 (LAN3/4) Gigabit integrated controllers support all major network operating systems. However, the installation procedure varies between systems. Please follow the driver setup procedure instructions specific to the operating system installed.

6.4 Windows® 11 and Windows® Server Driver Setup

Download the driver from support website on your computer and decompressed the file. Select the “Autorun” then navigate to the directory for your OS.

Note! *Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.*

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Please verify specifications before quoting. This guide is intended for reference purposes only.