



**MODEL:
PCIE-AM5**

Full-size PICMG 1.3 CPU Card supports AMD Ryzen™ 7000/Ryzen™ 9000 Series Desktop Processors, DDR5 SO-DIMM, Dual Display, Dual Intel® 2.5 GbE, USB3.2, M.2, RoHS

User Manual



Revision



Date	Version	Changes
October 24, 2025	1.00	Initial release



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Manual Conventions

**WARNING**

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.

**CAUTION**

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.

**NOTE**

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

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Chapter

1

Introduction

1.1 Introduction



Figure 1-1: PCIE-AM5

The PCIE-AM5 is a Full-size PICMG 1.3 CPU Card. It accepts AMD Ryzen™ 7000/Ryzen™ 9000 Series Desktop Processors and supports Two 288-pin Dual-Channel DDR5 SDRAM Unbuffered DIMMs, supported up to 64GB, Speeds up to 5200MHz memory. Moreover, the PCIE-AM5 includes one DP and one HDMI for dual independent display.

The PCIE-AM5 provides two 2.5GbE interfaces through the Intel® I226V controllers. Expansion and I/O include one PCIe x16 slot, four PCIe x1 slots via golden finger, four PCI slots via golden finger, four SATA, one M.2 M key, two RS-232/422/485, three USB 3.2 Gen 2 Type-A, one USB 3.2, two USB 3.2, four USB 2.0 and four USB2.0 to the backplane.

PCIE-AM5

1.2 Features

Some of the PCIE-AM5 motherboard features are listed below:

- AMD Socket AM5 for AMD Ryzen™ 7000/Ryzen™ 9000 Series Desktop Processors
- Two 288-pin 5200 MHz Dual-Channel DDR5 SDRAM Unbuffered DIMMs, supported up to 64GB
- Two 2.5GbE I226V controllers
- Dual independent display by DP and HDMI
- Four SATA 6Gb/s connectors
- Three USB 3.2 Gen 2 Type-A, one USB 3.2, two USB 3.2, four USB 2.0 and four USB2.0 to the backplane.
- One M.2 M Key slot (2242/2280, PCIe Gen4 x4) NVMe support
- 1 x PCIe Gen3 x16 signal via golden finger (Support x16, or x8 + x8, or x4 + x4 + x4 + x4) 4 x PCIe Gen3 x1 signal via golden finger (support1 x4, or 4 x1) 4 x PCI signal via golden finger
- 2 x RS-232/422/485
- Support TPM 2.0(TPM-IN03 module)
- RoHS compliant

1.3 Connectors

The connectors on the PCIE-AM5 are shown in the figure below.

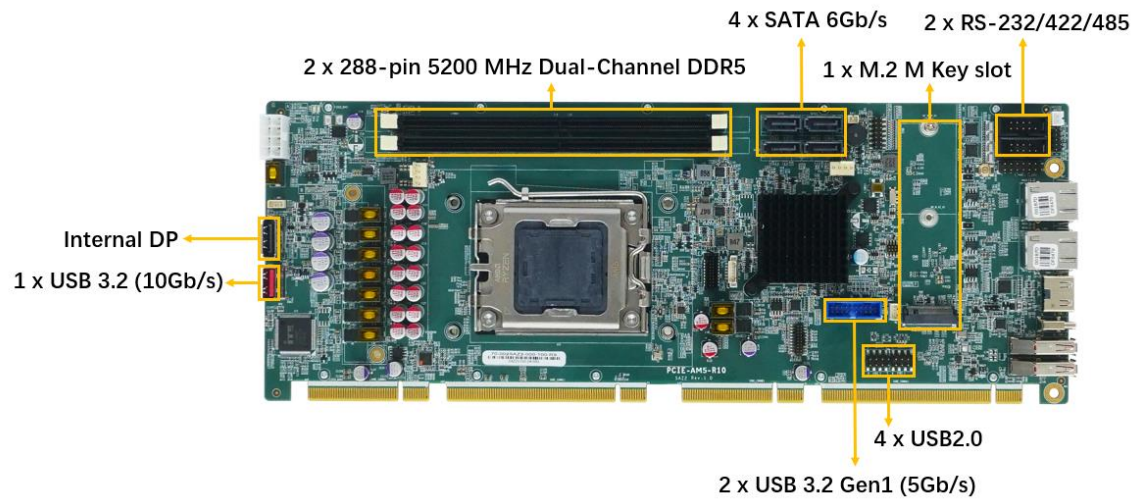


Figure 1-2: Connectors

PCIE-AM5

1.4 Dimensions

The main dimensions of the PCIE-AM5 are shown in the diagram below.

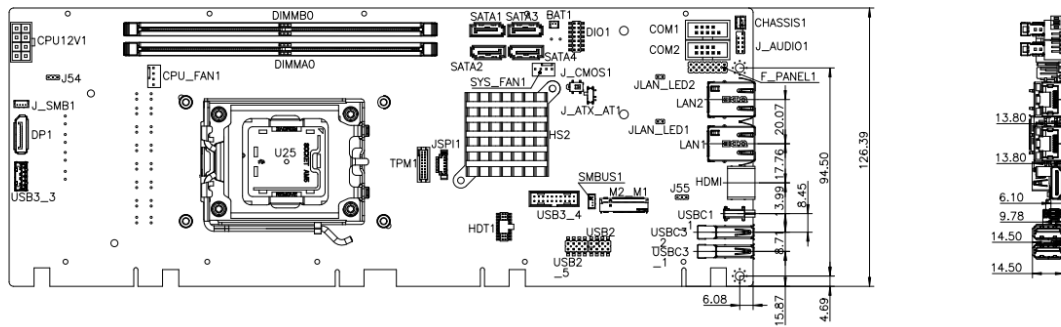


Figure 1-3: PCIE-AM5 Dimensions (mm)

1.5 Data Flow

Figure 1-4 shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

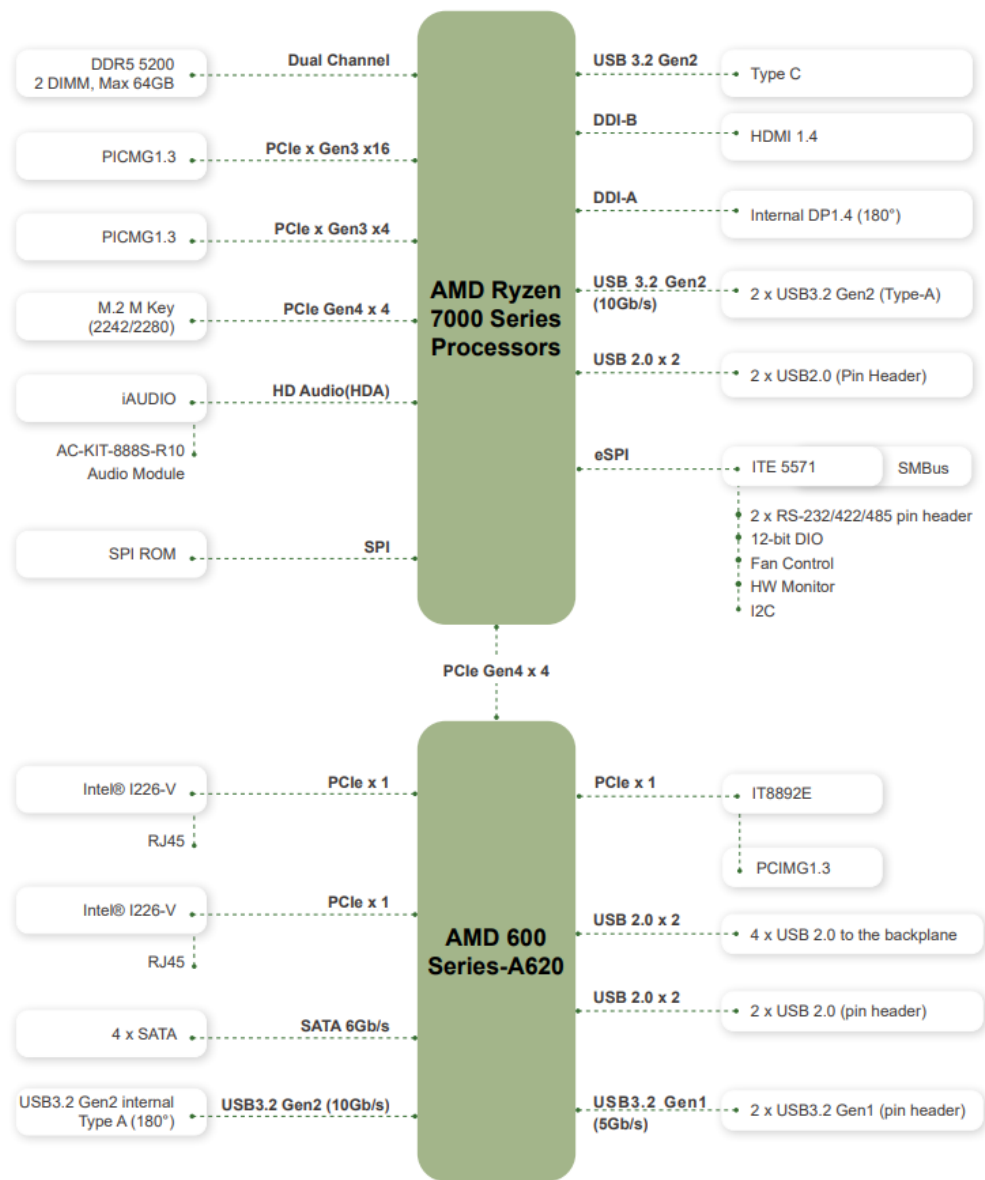


Figure 1-4: Data Flow Diagram

PCIE-AM5

1.6 Technical Specifications

The PCIE-AM5 technical specifications are listed below.

Specification/Model	PCIE-AM5
Form Factor	Full-size PICMG 1.3 CPU Card
CPU Supported	AMD Ryzen™ 7000/Ryzen™ 9000 Series Desktop Processors
Memory	Two 288-pin Dual-Channel DDR5 SDRAM Unbuffered DIMMs, supported up to 64GB, Speeds up to 5200MHz
Graphics Engine	Integrated RDNA2 GPU
Display Output	Dual independent display 1 x HDMI 1.4 (4K @30Hz) 1 x internal DP 1.4 (180°) (4K @60Hz)
Ethernet Controllers	LAN1: Intel® I226V 2.5GbE controller LAN2: Intel® I226V 2.5GbE controller
Audio	1 x iAUDIO, support IEI AC-KIT-888S Audio Module (2x5 pin)
BIOS	AMI UEFI BIOS
Watchdog Timer	Software Programmable support 1~255 sec. System reset
Expansions	1 x PCIe Gen3 x16 signal via golden finger (Support x16, or x8 + x8, or x4 + x4 + x4 + x4) 4 x PCIe Gen3 x1 signal via golden finger (support 1 x4, or 4 x1) 4 x PCI signal via golden finger 1 x M.2 M Key slot (2242/2280, PCIe Gen4 x4) NVMe support
I/O Interface Connectors	
Audio Connectors	One internal audio connector (10-pin header)
Chassis Intrusion	One 2-pin header
Digital I/O	1 x 12-bit digital I/O (2x7 pin)
Ethernet	Two RJ-45 GbE ports

Specification/Model	PCIE-AM5
Fan	1 x CPU fan connector (1x4 pin) 1 x System fan connector (1x4 pin)
Front Panel	1 x Front Panel (2x7 pin, Power LED, HDD LED, Speaker, Power button, Reset button)
I ² C	One 4-pin wafer connector
LAN LED	2 x LAN LED (1x2 pin)
Serial ATA	Four SATA 6Gb/s connectors
Serial Ports	2 x RS-232/422/485 (2x5 pin, P=2.54)
SMBus	One 4-pin wafer connector
USB Ports	2 x USB 3.2 Gen2 (Type-A) 2 x USB 3.2 Gen1 (2x10 pin P=2.00 pin wafer) (5Gb/s) 1 x USB 3.2 (10Gb/s) (internal Type A) 4x USB 2.0 (2x4 pin, P=2.54) 4 x USB2.0 to the backplane
Environmental and Power Specifications	
Power Supply	Support AT/ATX mode ErP/EuP Compliant
Power Consumption	3.3V@2.65A, 5V@11.47A, 12V@9.56A, 5VSB@0.16A (AMD Ryzen 9 7900 with Transcend DDR5 4800MT/s U-DIMM 32GB memory,EUP mode enabled)
Operating Temperature	0°C ~ 60°C
Storage Temperature	-30°C ~ 70°C
Operating Humidity	5% ~ 95% (non-condensing)
Physical Specifications	
Dimensions	338 mm x 126 mm
Weight (GW/NW)	1000g / 500g

Table 1-1: PCIE-AM5 Specifications

Packing List

2.1 Anti-static Precautions



WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

Make sure to adhere to the following guidelines:

- ***Wear an anti-static wristband:*** Wearing an anti-static wristband can prevent electrostatic discharge.
- ***Self-grounding:*** Touch a grounded conductor every few minutes to discharge any excess static buildup.
- ***Use an anti-static pad:*** When configuring any circuit board, place it on an anti-static mat.
- ***Only handle the edges of the PCB:*** Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

2.2 Unpacking Precautions

When the PCIE-AM5 is unpacked, please do the following:

- Follow the anti-static guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

PCIE-AM5

2.3 Packing List



NOTE:

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the PCIE-AM5 was purchased from or contact an IEI sales representative directly by sending an email to sales@ieiworld.com.

The PCIE-AM5 is shipped with the following components:

Quantity	Item and Part Number	Image
1	PCIE-AM5 single board computer	
1	SATA cable	
1	Quick installation guide	

Table 2-1: Packing List

2.4 Optional Items

The following are optional components which may be separately purchased:

Item and Part Number	Image
RS-232 cable, 200mm, P=2.0 (P/N: 32205-000702-100-RS)	

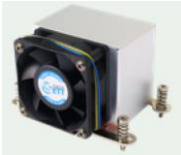
Item and Part Number	Image
Dual port USB cable with bracket, 30mm, P=2.54 (P/N: 19800-003100-100-RS)	
USB 3.0 cable 457mm with bracket (P/N:19800-010500-200-RS)	
SATA power cable, MOLEX 5264-4P to SATA15P (P/N:32102-000100-200-RS)	
Cooler module (P/N: 19100-000344-00-RS)	
Cooler module (P/N: 19100-000345-00-RS)	

Table 2-2: Optional Items

Installation

3.1 Anti-static Precautions

**WARNING:**

Failure to take ESD precautions during the installation of the PCIE-AM5 may result in permanent damage to the PCIE-AM5 and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the PCIE-AM5. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the PCIE-AM5 or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- ***Wear an anti-static wristband:*** Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- ***Self-grounding:*** Before handling the board touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- ***Use an anti-static pad:*** When configuring the PCIE-AM5, place it on an anti-static pad. This reduces the possibility of ESD damaging the PCIE-AM5.
- ***Only handle the edges of the PCB:*** When handling the PCB, hold the PCB by the edges.

3.2 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the onboard connectors.

3.2.1 SATA Drive Connection

The PCIE-AM5 is shipped with one SATA drive cables. To connect the SATA drives to the connectors, please follow the steps below.

Step 1: **Locate the connectors.** The locations of the SATA drive connectors are shown in **Chapter 3**.

PCIE-AM5

Step 2: Insert the cable connector. Insert the cable connector into the on-board SATA drive connector until it clips into place. See **Figure 3-1**.

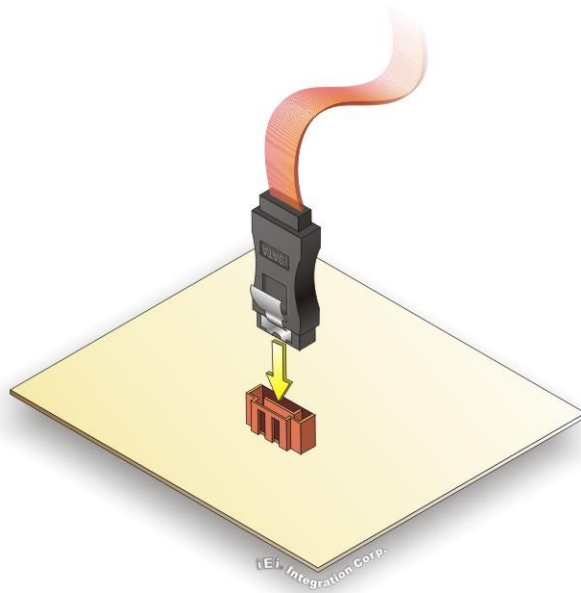


Figure 3-1: SATA Drive Cable Connection

Step 3: Connect the cable to the SATA disk. Connect the connector on the other end of the cable to the connector at the back of the SATA drive. See **Figure 3-2**.

Step 4: Connect the SATA power cable. Connect the SATA power connector to the back of the SATA drive. See **Figure 3-2**.

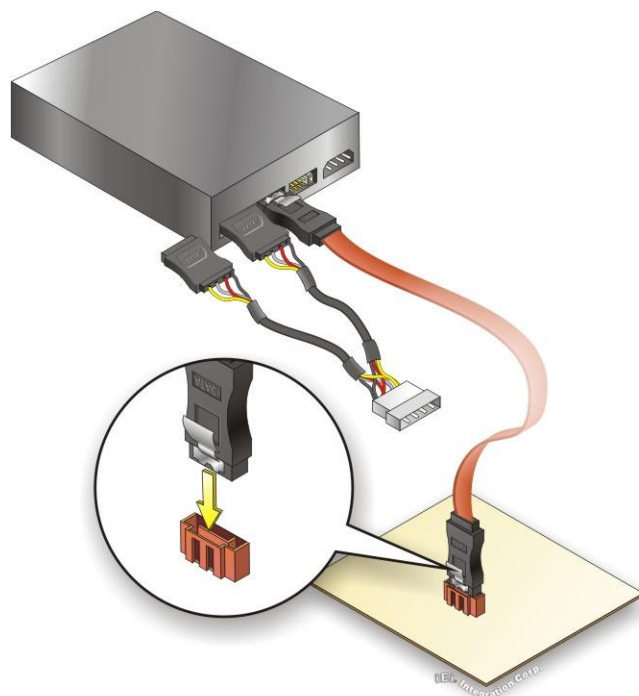


Figure 3-2: SATA Power Drive Connection

The SATA power cable can be bought from IEI. See Optional Items in Section 2.4.

3.3 Installation Considerations

**NOTE:**

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

**WARNING:**

The installation instructions described in this manual should be carefully followed in order to prevent damage to the components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
 - The user manual provides a complete description of the PCIE-AM5 installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
 - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the PCIE-AM5 on an anti-static pad:
 - When installing or configuring the motherboard, place it on an anti-static pad. This helps to prevent potential ESD damage.
- Turn all power to the PCIE-AM5 off:
 - When working with the PCIE-AM5, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the PCIE-AM5, **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

3.4 Socket AM5 CPU Installation



WARNING:

CPUs are expensive and sensitive components. When installing the CPU please be careful not to damage it in anyway. Make sure the CPU is installed properly and ensure the correct cooling kit is properly installed.

DO NOT touch the pins at the bottom of the CPU. When handling the CPU, only hold it on the sides.

To install the CPU, follow the steps below.

Step 1: **Disengage the load lever** by pressing the lever down and slightly outward to clear the retention tab. Fully open the lever. See **Figure 3-3**.

PCIE-AM5

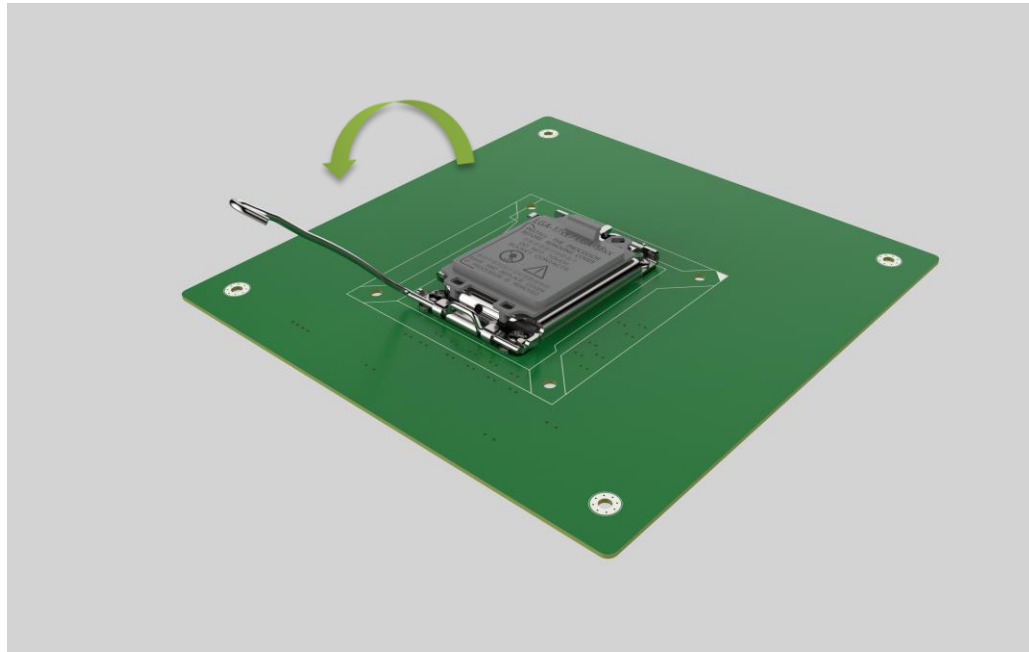


Figure 3-3: Disengage the CPU Socket Load Lever

Step 2: Open the socket and remove the protective cover. The black protective cover can be removed by pulling up on the tab labeled "Remove". See Figure 3-4.

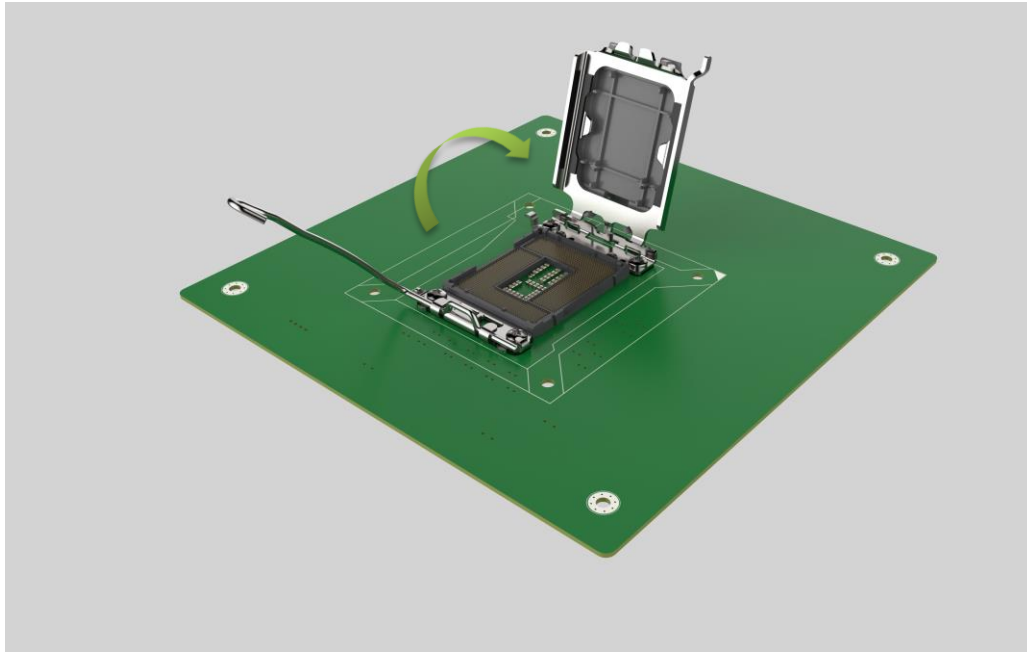


Figure 3-4: Remove Protective Cover

Step 3: Inspect the CPU socket. Make sure there are no bent pins and make sure the socket contacts are free of foreign material. If any debris is found, remove it with compressed air.

Step 4: Orientate the CPU properly. The contact array should be facing the CPU socket.



WARNING:

DO NOT touch the pins at the bottom of the CPU. When handling the CPU, only hold it on the sides.

Step 5: Correctly position the CPU. Match the Pin 1 mark with the cut edge on the CPU socket.

Step 6: Align the CPU pins. Locate pin 1 and the two orientation notches on the CPU. Carefully match the two orientation notches on the CPU with the socket alignment keys.

PCIE-AM5

Step 7: Insert the CPU. Gently insert the CPU into the socket. If the CPU pins are properly aligned, the CPU should slide into the CPU socket smoothly. See **Figure 3-5**.

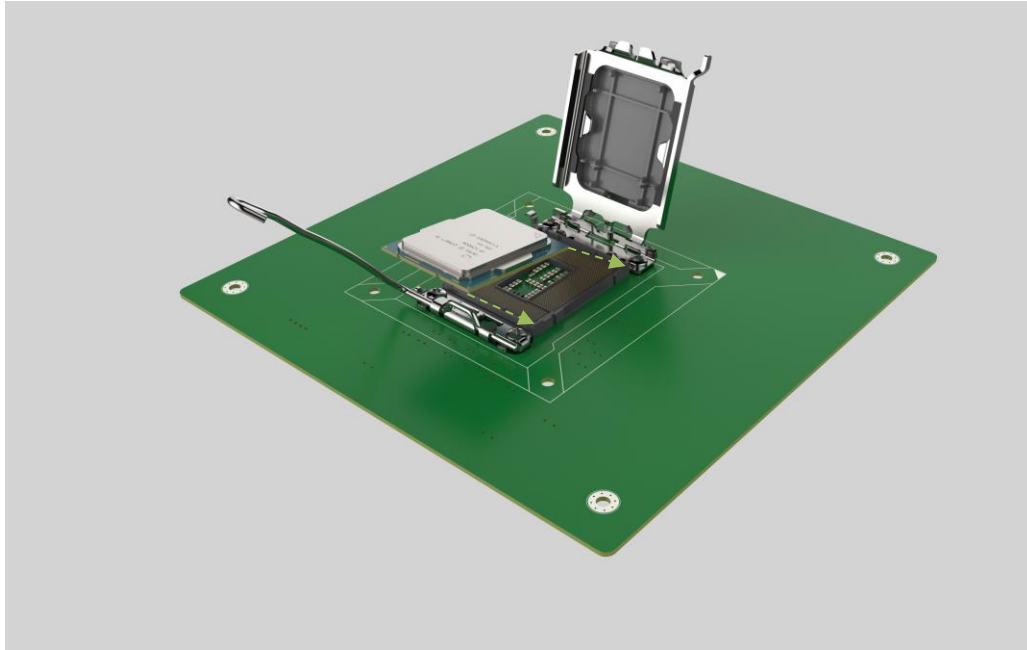


Figure 3-5: Insert the Socket AM5 CPU

Step 8: Close the CPU socket. Close the load plate and pull the load lever back a little to have the load plate be able to secure to the knob. Engage the load lever by pushing it back to its original position (**Figure 3-6**). There will be some resistance, but will not require extreme pressure.

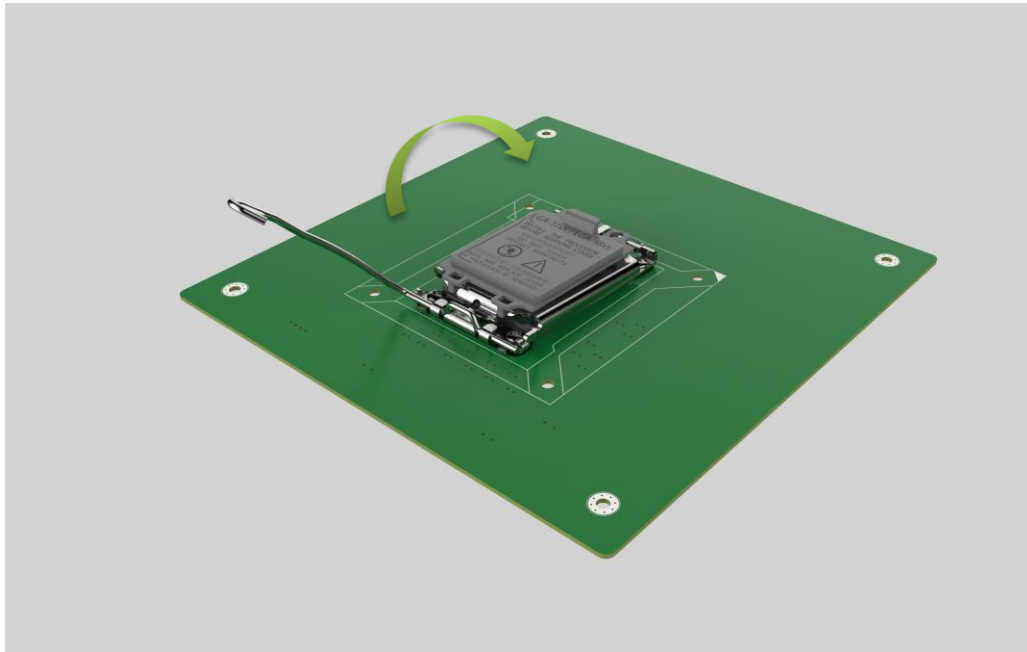


Figure 3-6: Close the Socket AM5

Step 9: Connect the 12 V power to the board. Connect the 12 V power from the power supply to the board.

3.5 Socket AM5 Cooling Kit Installation



WARNING:

DO NOT attempt to install a push-pin cooling fan.

The pre-installed support bracket prevents the board from bending and is **ONLY** compatible with captive screw type cooling fans.

The cooling kit can be bought from IEI. The cooling kit has a heat sink and fan.

PCIE-AM5

**WARNING:**

Do not wipe off (accidentally or otherwise) the pre-sprayed layer of thermal paste on the bottom of the heat sink. The thermal paste between the CPU and the heat sink is important for optimum heat dissipation.

To install the cooling kit, follow the instructions below.

Step 1: A cooling kit bracket is pre-installed on the rear of the motherboard. See **Figure 3-7**.

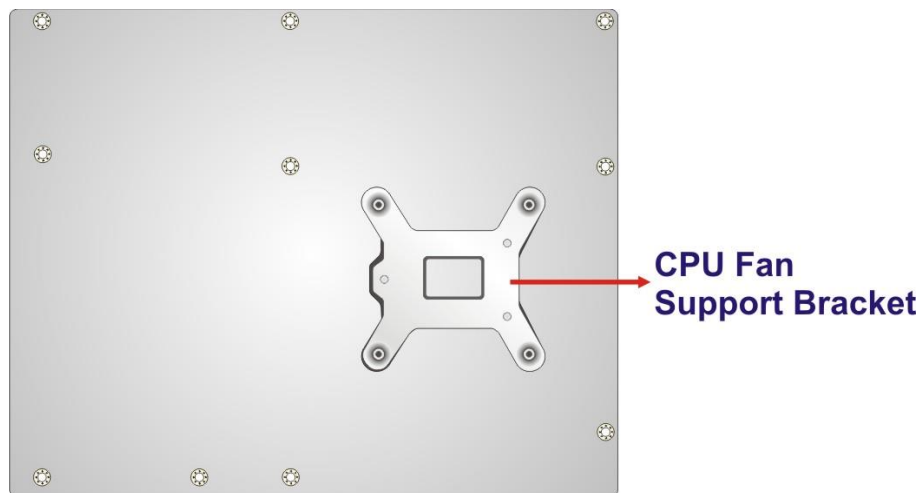


Figure 3-7: Cooling Kit Support Bracket

Step 2: Place the cooling kit onto the socket AM5 CPU. Make sure the CPU cable can be properly routed when the cooling kit is installed.

Step 3: Mount the cooling kit. Gently place the cooling kit on top of the CPU. Make sure the four threaded screws on the corners of the cooling kit properly pass through the holes of the cooling kit bracket.

Step 4: Tighten the screws. Use a screwdriver to tighten the four screws. In a diagonal pattern, tighten each screw a few turns then move to the next one, until they are all secured. Do not overtighten the screws.

Step 5: Connect the fan cable. Connect the cooling kit fan cable to the CPU fan connector on the PCIE-AM5. Carefully route the cable and avoid heat generating chips and fan blades.

3.6 DIMM Installation

To install a DIMM, please follow the steps below and refer to **Figure 3-8**.

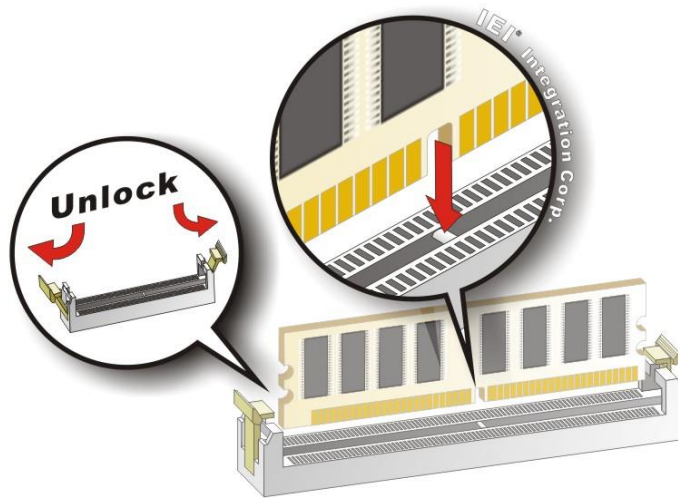


Figure 3-8: DIMM Installation

Step 1: Open the DIMM socket handles. Open the two handles outwards as far as they can. See **Figure 3-8**.

Step 2: Align the DIMM with the socket. Align the DIMM so the notch on the memory lines up with the notch on the memory socket. See **Figure 3-8**.

Step 3: Insert the DIMM. Once aligned, press down until the DIMM is properly seated. Clip the two handles into place. See **Figure 3-8**.

Step 4: Removing a DIMM. To remove a DIMM, push both handles outward. The memory module is ejected by a mechanism in the socket.

PCIE-AM5

**CAUTION:**

For quad channel configuration, install four identical memory modules that feature the same capacity, timings, voltage, number of ranks and the same brand.

3.7 M.2 Module Installation

The PCIE-AM5 provide two ways to install the M.2 expansion card. One is using screw, and the other is using the retainer. Please follow the steps below.

Mode One: Using screw

- Step 1:** Locate the M.2 module slot. See **Chapter 3**.
- Step 2:** Remove the retention screw secured on the motherboard.
- Step 3:** Line up the notch on the module with the notch on the slot. Slide the M.2 module into the socket at an angle of about 20° (**Figure 3-9**).

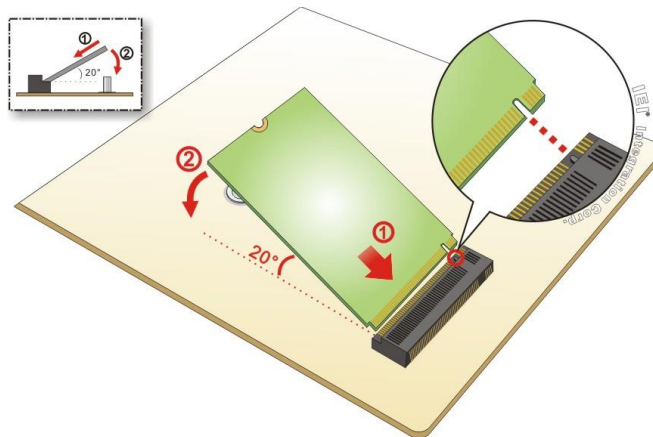


Figure 3-9: Inserting the M.2 Module into the Slot at an Angle

- Step 4:** Secure the M.2 module with the previously removed retention screw (**Figure 3-10**).

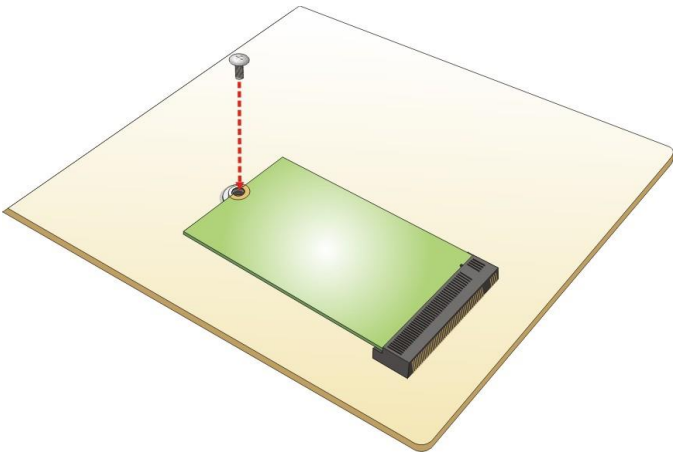


Figure 3-10: Securing the M.2 Module

Mode Two: Using the Retainer

Step 1: Press the retainer down as shown below. (See Figure 3-11)

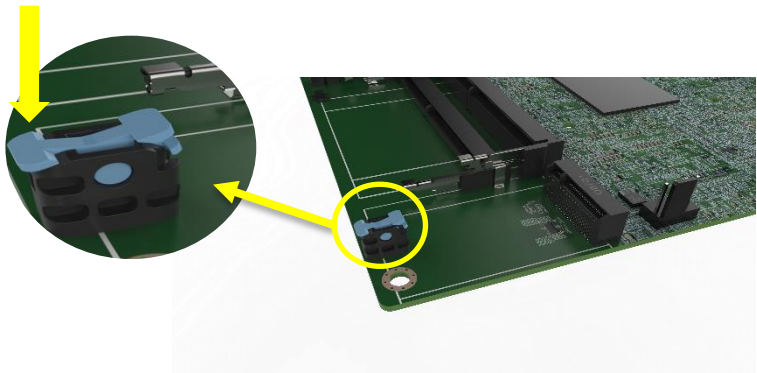


Figure 3-11: Press the Retainer

PCIE-AM5

Step 2: Line up the notch on the M.2 module with the notch on the slot. Slide the M.2 module into the socket at an angle of about 20°. (See **Figure 3-9**)

Step 3: Align the notch on the end of the M.2 module with the clip of the retainer. (See

Figure 3-12)

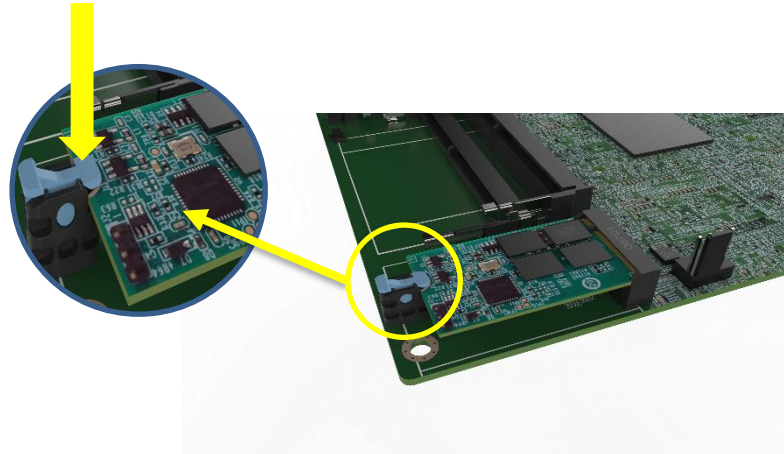


Figure 3-12: Aligning the M.2 Module with the Retainer

Step 4: Press the M.2 module down until it is secured into place by the retainer. (See **Figure 3-13**)

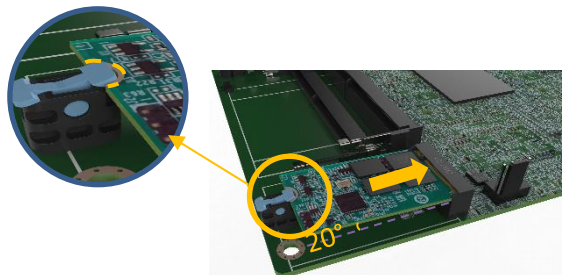


Figure 3-13: Securing the M.2 Module

Step 5: If you want to remove the M.2 module, you should press the retainer down as described in Step 1 to release the M.2 module. (See **Figure 3-11**)



3.8 Software Installation

All the drivers for the PCIE-AM5 are available on IEI Resource Download Center (<https://download.ieiworld.com>). Type PCIE-AM5 and press Enter to find all the relevant software, utilities, and documentation.

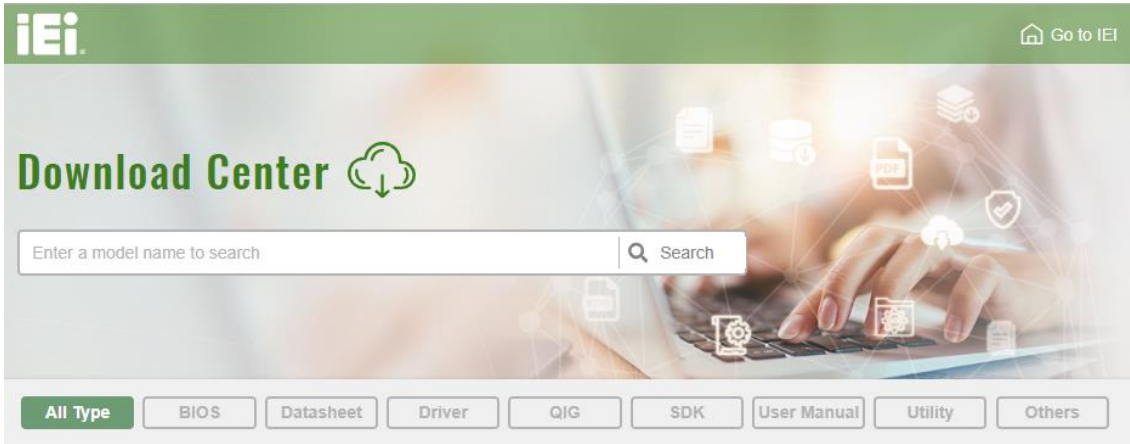
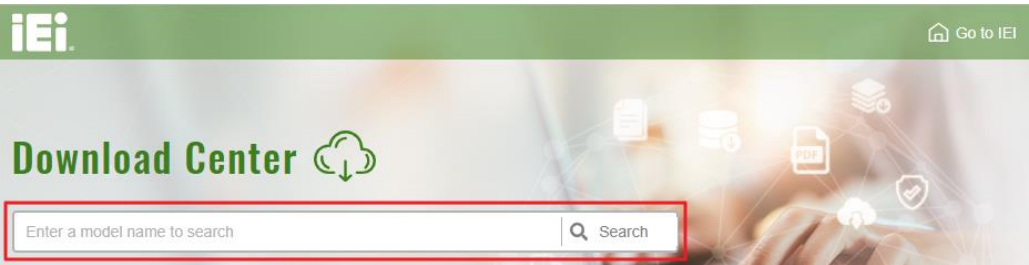


Figure 3-14: IEI Resource Download Center

3.9 Driver Download

To download drivers from IEI Resource Download Center, follow the steps below.

Step 1: Go to <https://download.ieiworld.com>. Type PCIE-AM5 and press Enter.



Step 2: All product-related software, utilities, and documentation will be listed. You can choose **Driver** to filter the result.



PCIE-AM5

[All Type](#)
[BIOS](#)
[Datasheet](#)
[Driver](#)
[QIG](#)
[SDK](#)
[User Manual](#)
[Utility](#)
[Others](#)

Keyword: "PCIE-AM5", Searching Result : 3 Records.

PCIE-AM5
[Product Info](#)

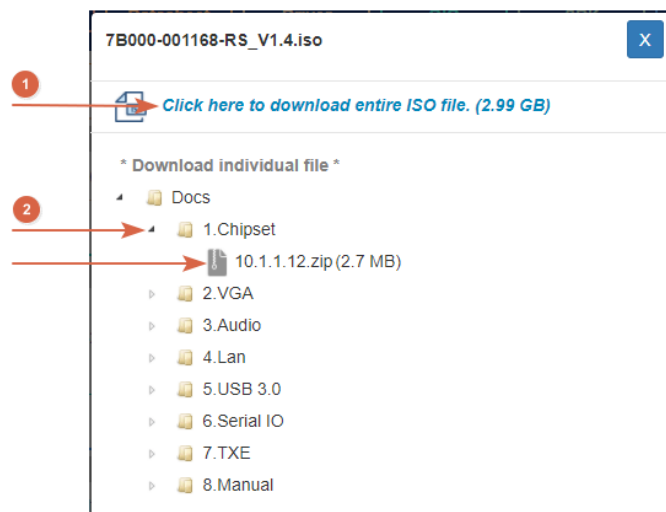
Embedded Computer ▶ Single Board Computer ▶ Full Size Single Board Computer

Full-size PICMG 1.3 CPU Card supports AMD Ryzen™ 7000/8000 Series Desktop Processors, DDR5, dual Display, Dual Intel® 2.5GbE, USB3.2, M.2, RoHS

Driver

File Name	Published	Version	File Checksum
IMBA-AM5-R10_V1.0.iso (1.09 GB)	2024-12-12	1.00	E0F30F32B817C54104D9554E8D60AC90

Step 3: Click the driver file name on the page and you will be prompted with the following window. You can download the entire ISO file (○), or click the small arrow to find an individual driver and click the file name to download (○).

**NOTE:**

To install software from the downloaded ISO image file in Windows 8, 8.1 or 10, double-click the ISO file to mount it as a virtual drive to view its content. On Windows 7 system, an additional tool (such as Virtual CD-ROM Control Panel from Microsoft) is needed to mount the file.

Chapter

4

Connectors

PCIE-AM5

4.1 Peripheral Interface Connectors

This chapter details all the peripheral interface connectors.

4.1.1 PCIE-AM5 Layout

The figures below show all the peripheral interface connectors.

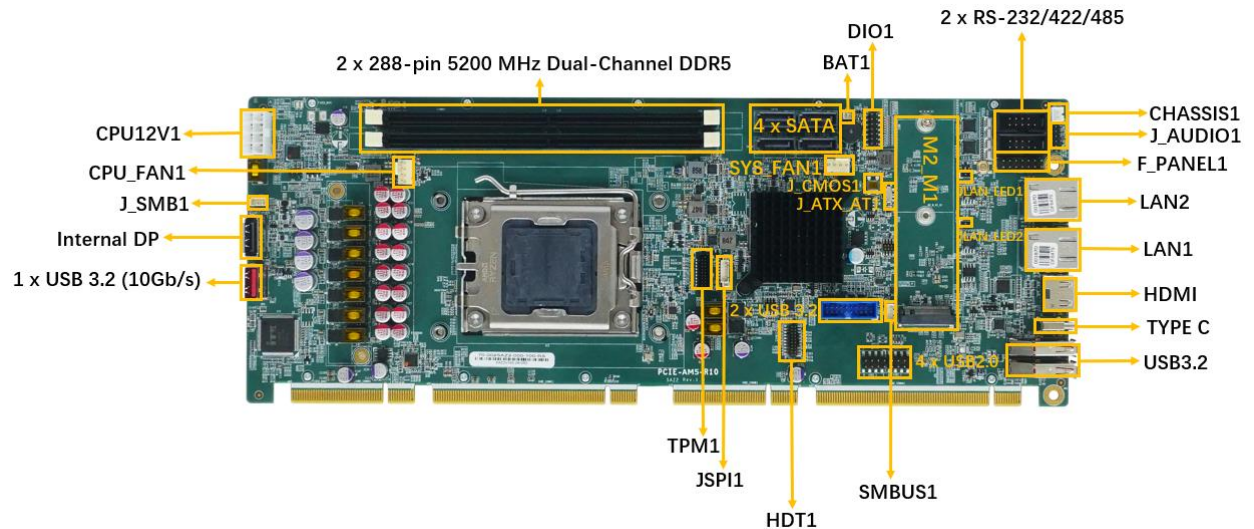


Figure 4-1: Peripheral Interface Connectors

4.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
AT/ATX power mode setting	3-pin switch	J_ATX_AT1
Clear CMOS jumper	Button	J_CMOS1
ATX CPU 12V power connector	8-pin Molex power connector	CPU12V1
RTC battery connector	2-pin header	BAT1
Chassis intrusion connector	2-pin header	CHASSIS1
DDR5 DIMM slots	288-pin socket	DIMMA0, DIMMB0

Connector	Type	Label
Digital I/O connector	14-pin header	DIO1
Trusted Platform Module Connector	20-pin header	TPM1
Fan connectors	4-pin header	CPU_FAN1, SYS_FAN1,
Front panel connector	14-pin header	F_PANEL1
LAN link LED connector	2-pin header	JLAN_LED1 JLAN_LED2
RS-232/422/485 connectors	9-pin header	COM1, COM2
SATA 6Gb/s connectors	8-pin SATA connector	SATA1, SATA2 SATA3, SATA4
SMBus connector	4-pin wafer	SMBUS1
Flash SPI ROM connector	6-pin header	JSPI1
M.2 M key slots	M-key slot	M2_M1
HDT connector	20-pin header	HDT1
USB 3.2 connector	internal Type A	USB3_3
USB 3.2 slot	2 x 10 pin header	USB3_4
USB 2.0 slot	2 x 4 pin	USB2_1, USB2_5
External audio jacks	Audio jacks	J_AUDIO
DP Connector	Display port	DP1

Table 4-1: Peripheral Interface Connectors

4.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
External dual 2.5GbE RJ-45 connector	USB 3.2, RJ45	LAN1, LAN2
External HDMI connector	HDMI	HDMI1
External USB connector	TYPE C	USBC1_1

PCIE-AM5

Connector	Type	Label
External USB Connector	USB 3.2	USB3_1, USB3_2

Table 4-2: Rear Panel Connectors

4.2 Internal Peripheral Connectors

The section describes all of the connectors on the PCIE-AM5.

4.2.1 Clear CMOS Button

- CN Label:

J_CMOS1
- CN Type:

Button
- CN Location:

See Figure 4-2
- CN Pinouts:

See Table 4-3

The J_CMOS1 is used to Clear CMOS Setup.



Figure 4-2: Clear CMOS Jumper Location

Pin	Description
NC	Keep CMOS Setup
Press button	Clear CMOS Setup

Table 4-3: Clear CMOS Jumper Pinouts

PCIE-AM5

4.2.2 AT/ATX Power Mode Setting

CN Label:	J_ATX_AT1
CN Type:	3-pin switch
CN Location:	See Figure 4-3
CN Pinouts:	See Table 4-4

The AT/ATX power mode selection is made through the AT/ATX power mode switch.

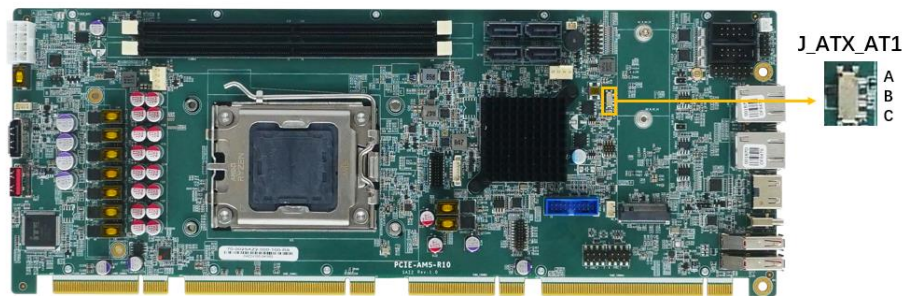


Figure 4-3: AT/ATX Power Mode Switch Locations

Pin	Description	Pin	Description
1-2(Right)	ATX Power Mode (default)	2-3(Left)	AT Power Mode

Table 4-4: AT/ATX Power Mode Switch Settings

4.2.3 Front Panel Connector

CN Label:	F_PANEL1
CN Type:	14-pin header, p=2.54 mm
CN Location:	See Figure 4-4
CN Pinouts:	See Table 4-5

The front panel connector connects to the indicator LEDs and buttons on the computer's front panel.

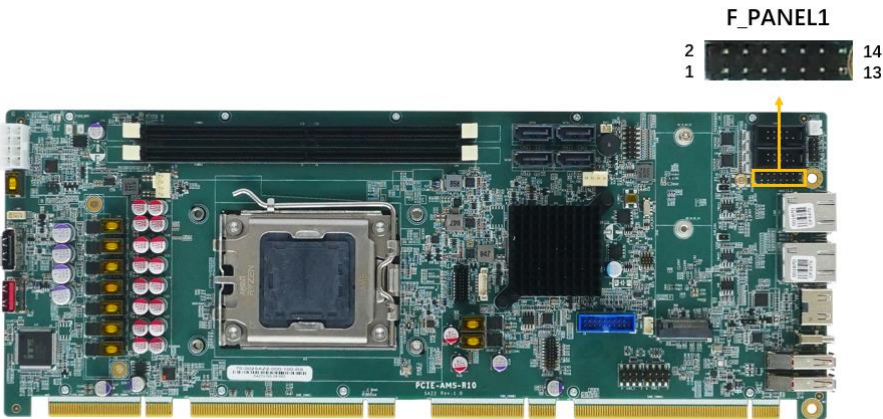


Figure 4-4: Front Panel Connector Location

Function	Pin	Description	Function	Pin	Description
PWR LED	1	+5V	SPKR	2	SPKR+
	3	NC	IPMI LED	4	NC
	5	GND		6	NC
PWR BTN	7	PWR_BTN_N	SPKR	8	SPKR-
	9	GND		10	NC
HDD LED	11	HD_LED_P	RESET	12	Reset+
	13	HD_LED_N		14	Reset-

Table 4-5: Front Panel Connector Pinouts

PCIE-AM5**4.2.4 Serial ATA 3.0 Connectors**

CN Label: SATA1, SATA2, SATA3, SATA4

CN Type: 8-pin SATA connector

CN Location: See **Figure 4-5**

CN Pinouts: See **Table 4-6**

The SATA drive connectors can be connected to SATA drives and support up to 6Gb/s data transfer rate.

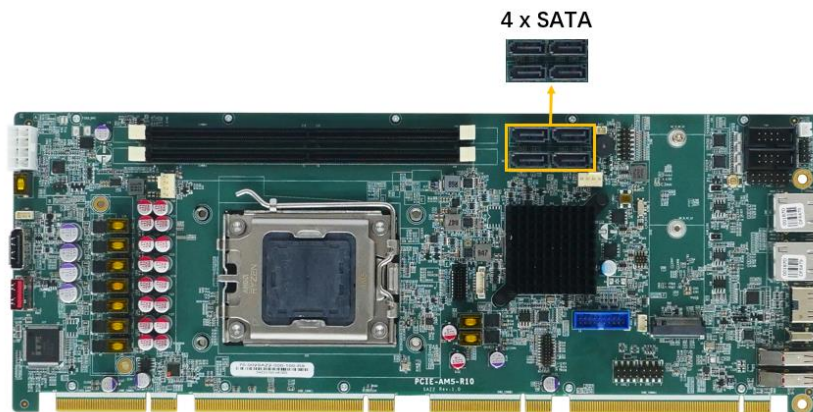


Figure 4-5: SATA 6Gb/s Connector Locations

Pin	Description
1	GND
2	SATA_TXP
3	SATA_TXN
4	GND
5	SATA_RXN
6	SATA_RXP
7	GND
8	NC
9	NC

Table 4-6: SATA 6Gb/s Connector Pinouts

4.2.5 Extend Audio Module Connector

- CN Label:

J_AUDIO1
- CN Type:

10-pin header, p=2.00 mm
- CN Location:

See Figure 4-6
- CN Pinouts:

See Table 4-7

This connector connects to speakers, a microphone and an audio input.

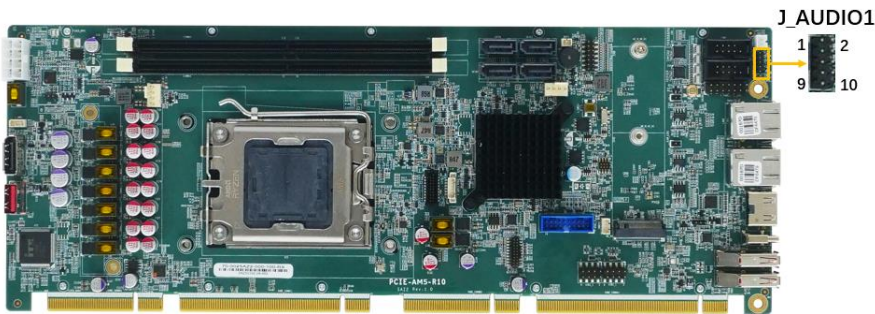


Figure 4-6: Audio Connector Location

Pin	Description	Pin	Description
1	HDA_SYNC_R	2	HDA_BCLK_R
3	HDA_SDO_R	4	HDA_PCBEEPC
5	HDA_SDI_0_R	6	HDA_RST_R
7	+5V	8	GND
9	+12V	10	GND

Table 4-7: Audio Connector Pinouts

PCIE-AM5**4.2.6 Fan Connector (CPU)**

- CN Label:** CPU_FAN1
- CN Type:** 4-pin header, p=2.54 mm
- CN Location:** See **Figure 4-7**
- CN Pinouts:** See **Table 4-8**

The fan connector attaches to a CPU cooling fan.



Figure 4-7: CPU Fan Connector Location

Pin	Description	Pin	Description
1	GND	2	+12V
3	FANIN	4	PWM (+5V)

Table 4-8: CPU Fan Connector Pinouts

4.2.7 Fan Connectors (System)

- CN Label:

SYS_FAN1
- CN Type:

4-pin header, p=2.54 mm
- CN Location:

See Figure 4-8
- CN Pinouts:

See Table 4-9

Fan connector attaches to a system cooling fan. The fan connector provides smart fan function.

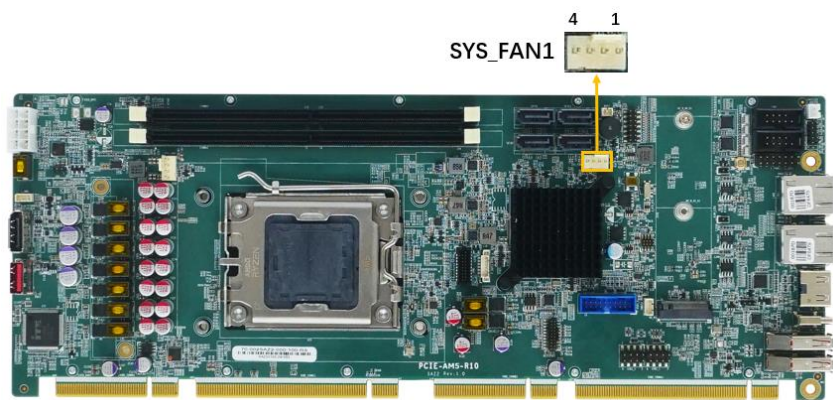


Figure 4-8: System Fan Connector Locations

Pin	Description	Pin	Description
1	GND	2	+12V
3	FANIN	4	PWM (+5V)

Table 4-9: System Fan Connector Pinouts

PCIE-AM5

4.2.8 Hardware Debug Tool Connector

- CN Label:** HDT1
- CN Type:** 20-pin connector, p=1.27mm
- CN Location:** See **Figure 4-9**
- CN Pinouts:** See **Table 4-10**

This connector provides hardware functional testing.

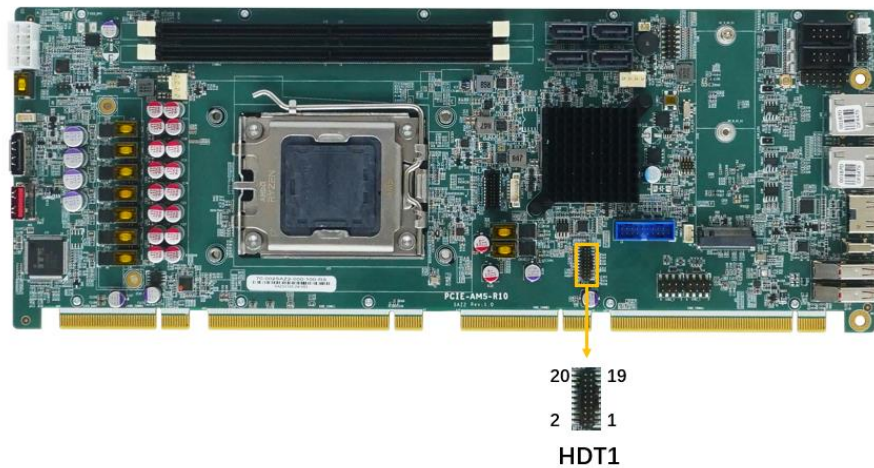


Figure 4-9: HDT Connector Location

Pin	Description	Pin	Description
1	+1.8V HDT	2	APU_TCK
3	GND	4	APU_TMS
5	GND	6	APU_TDI
7	GND	8	APU_TDO
9	APU_TRST#	10	APU_PWROK
11	GND	12	APU_RST_L
13	GND	14	APU_DBRDY
15	GND	16	HDT_DBREQ_L
17	GND	18	HDT_PLLTEST0
19	+1.8V HDT	20	HDT_PLLTEST1

Table 4-10: HDT Connector Pinouts

4.2.9 CPU 12V Power Connector

- CN Label:

CPU12V1
- CN Type:

8-pin Molex power connector, p=4.2mm
- CN Location:

See Figure 4-10
- CN Pinouts:

See Table 4-11

This connector provides power to the CPU.



Figure 4-10: CPU 12V Power Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	5	+12V
2	GND	6	+12V
3	GND	7	+12V
4	GND	8	+12V

Table 4-11: CPU 12V Power Connector Pinouts

PCIE-AM5

4.2.10 SMBus Connector

CN Label:	SMBUS1
CN Type:	4-pin wafer, p=1.25 mm
CN Location:	See Figure 4-11
CN Pinouts:	See Table 4-12

The SMBus (System Management Bus) connector provides low-speed system management communications.

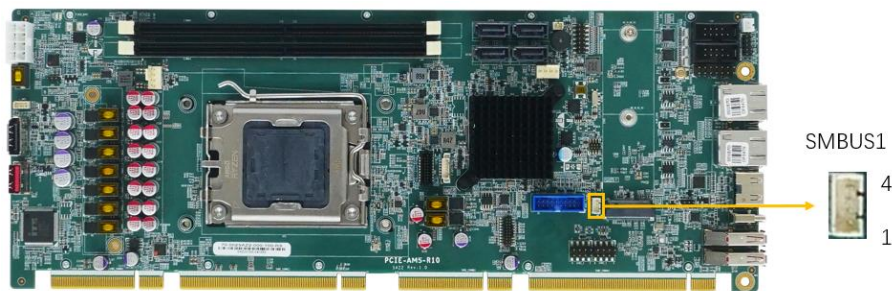


Figure 4-11: SMBus Connector Location

Pin	Description
1	GND
2	SMB_DATA_MAIN
3	SMB_CLK_MAIN
4	+5V

Table 4-12: SMBus Connector Pinouts

4.2.11 Chassis Intrusion Connector

- CN Label:

CHASSIS1
- CN Type:

2-pin header, p=2.00 mm
- CN Location:

See Figure 4-12
- CN Pinouts:

See Table 4-13

The chassis intrusion connector is for a chassis intrusion detection sensor or switch that detects if a chassis component is removed or replaced.

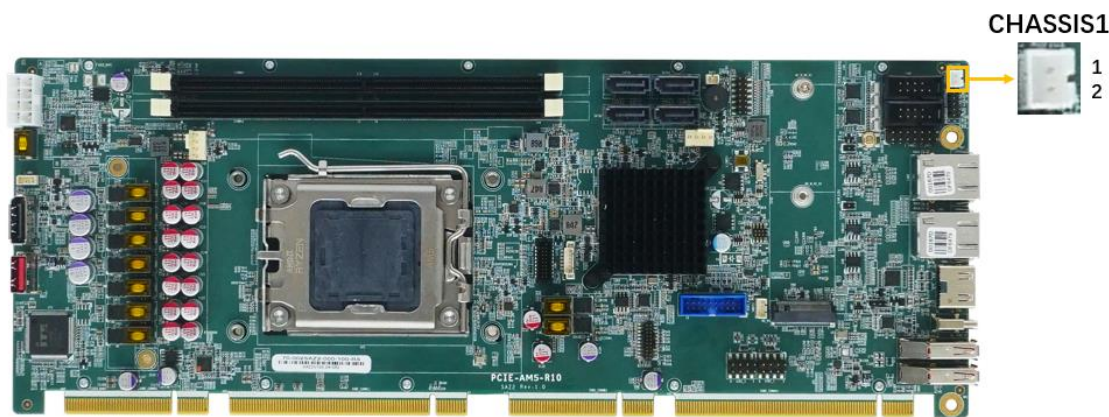


Figure 4-12: Chassis Intrusion Connector Location

Pin	Description	Pin	Description
1	CASEOPEN_N	2	GND

Table 4-13: Chassis Intrusion Connector Pinouts

PCIE-AM5

4.2.12 M.2 M-key Slot

CN Label:	M2_M1
CN Type:	M-key slot
CN Location:	See Figure 4-13
CN Pinouts:	See Table 4-14

The M.2 2242/2280 slot is keyed in the M position.

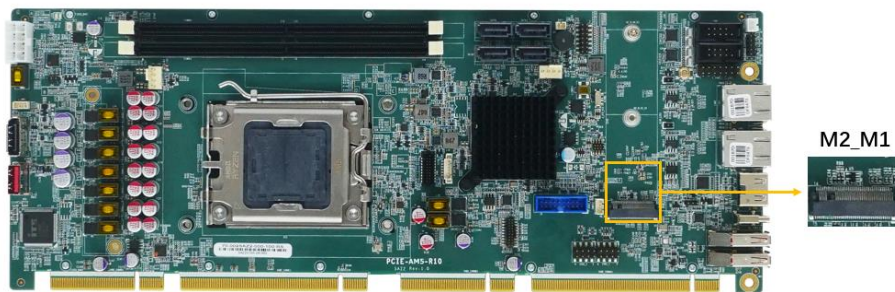


Figure 4-13: M.2 M-key Slot Location

Pin	Description	Pin	Description
1	GND	2	+3.3V
3	GND	4	+3.3V
5	PCIE_20_RX_DN	6	N/C
7	PCIE_20_RX_DP	8	N/C
9	GND	10	NGFF1 ACT_N
11	PCIE_TX_DN20	12	+3.3V
13	PCIE_TX_DP20	14	+3.3V
15	GND	16	+3.3V
17	PCIE_19_RX_DN	18	+3.3V
19	PCIE_19_RX_DP	20	N/C
21	GND	22	N/C
23	PCIE_TX_DN19	24	N/C
25	PCIE_TX_DP19	26	N/C
27	GND	28	N/C
29	PCIE_18_RX_DN	30	N/C



Pin	Description	Pin	Description
31	PCIE_18_RX_DP	32	N/C
33	GND	34	N/C
35	PCIE_TX_DN18	36	N/C
37	PCIE_TX_DP18	38	M_2 SSD SLP
39	GND	40	N/C
41	PCIE_17_RX_DN	42	N/C
43	PCIE_17_RX_DP	44	N/C
45	GND	46	N/C
47	PCIE_TX_DN17	48	N/C
49	PCIE_TX_DP17	50	PLT_RST_N
51	GND	52	SRCCLKREQB_17_N
53	PCIE_CLK_DN17	54	NC
55	PCIE_CLK_DP17	56	N/C
57	GND	58	N/C
59	N/C	60	N/C
61	N/C	62	N/C
63	N/C	64	N/C
65	N/C	66	N/C
67	N/C	68	NC
69	N/C	70	+3.3V
71	GND	72	+3.3V
73	GND	74	+3.3V
75	GND		
N1	N/C		
N2	N/C		

Table 4-14: M.2 M-key Connector Pinouts



PCIE-AM5

4.2.13 Digital I/O Connector

CN Label:	DIO1
CN Type:	14-pin header, p=2.00 mm
CN Location:	See Figure 4-14
CN Pinouts:	See Table 4-15

The Digital I/O connector provides programmable input and output for external devices.

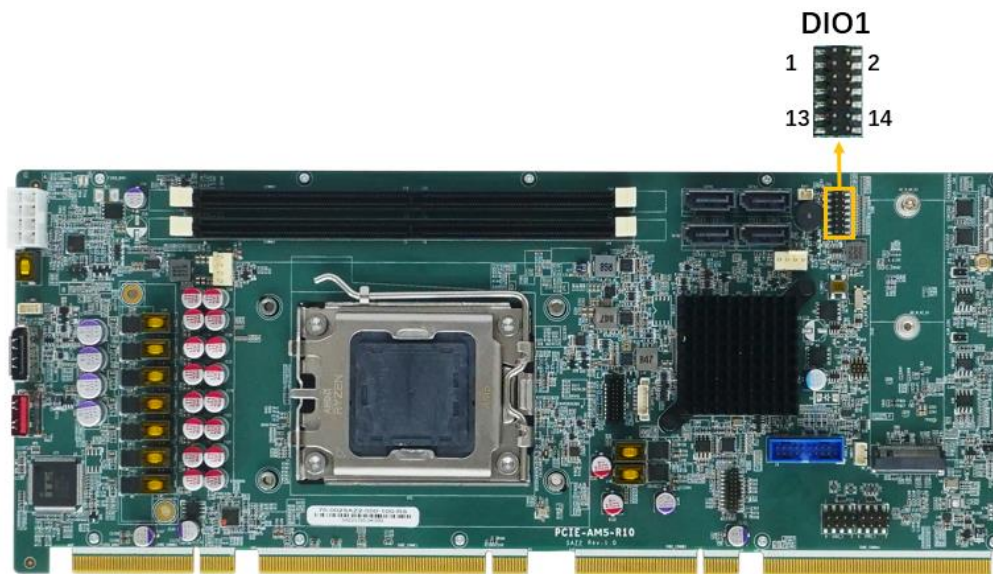


Figure 4-14: Digital I/O Connector Location

Pin	Description	Pin	Description
1	GND	2	+5V
3	DOUT5	4	DOUT4
5	DOUT3	6	DOUT2
7	DOUT1	8	DOUT0
9	DIN5	10	DIN4
11	DIN3	12	DIN2
13	DIN1	14	DIN0

Table 4-15: Digital I/O Connector Pinouts

4.2.14 Trusted Platform Module Connector

- CN Label:

TPM1
- CN Type:

20-pin header, p=1.27 mm
- CN Location:

See Figure 4-15
- CN Pinouts:

See Table 4-16

The TPM1 connector is used to the trusted platform module.

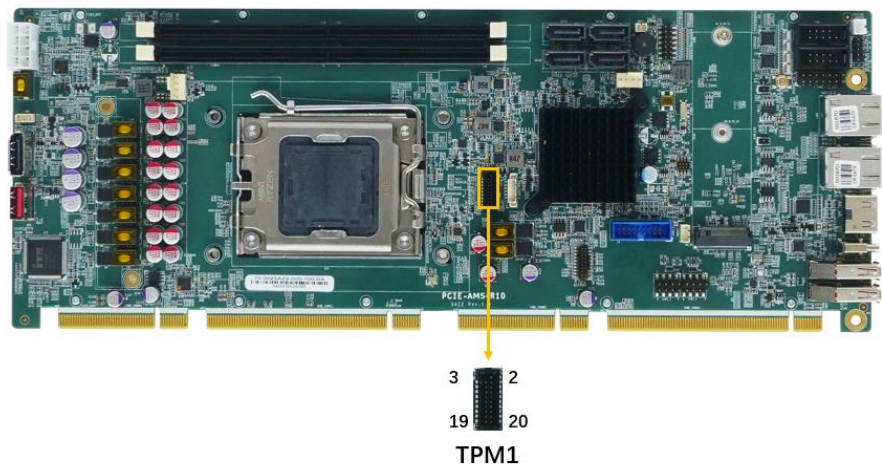


Figure 4-15: Trusted Platform Module Connector Location

Pin	Description	Pin	Description
1	N/C	2	N/C
3	TPM_GPIO	4	N/C
5	GND	6	+1.8V_ALW
7	SPI_CLK_TPM_R	8	N/C
9	N/C	10	SPI_MISO_TPM_R
11	N/C	12	SPI_MOSI_TPM_R
13	TPM_SPI_CS2_N	14	GND
15	N/C	16	N/C
17	TPM_IRQ#	18	+1.8V_ALW
19	TPM_R_N	20	+1.8V_ALW

Table 4-16: Trusted Platform Module Connector Pinouts

PCIE-AM5**4.2.15 LAN Link LED Connector**

CN Label: JLAN_LED1, JLAN_LED2

CN Type: 2-pin header, p=2.00 mm

CN Location: See **Figure 4-16**

CN Pinouts: See **Table 4-17**

The LAN LED connectors are used to connect to the LAN LED indicators on the chassis to indicate users the link activities of the two LAN ports.

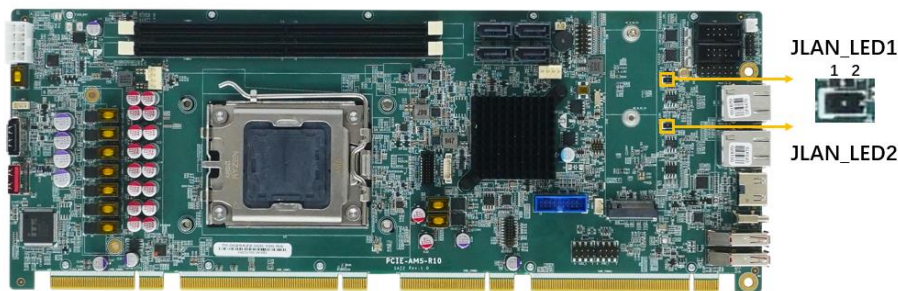


Figure 4-16: LAN LED Connector Location

Pin	Description
1	+3.3V
2	LAN_LED_LINK#_ACT

Table 4-17: LAN LED Connector Pinouts

4.2.16 Flash SPI ROM Connector

- CN Label:

JSPI1
- CN Type:

6-pin header, p=1.25 mm
- CN Location:

See Figure 4-17
- CN Pinouts:

See Table 4-18

The Flash SPI ROM connector is used to flash the SPI ROM.

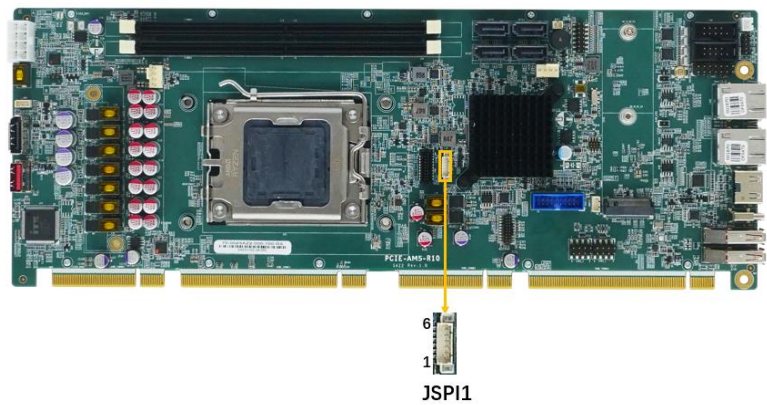


Figure 4-17: Flash SPI ROM Connector Location

Pin	Description	Pin	Description
1	SPI_POWER	4	SPI_F_CLK
2	SPI_F_CS_L	5	SPI_F_MOSI
3	SPI_F_MISO	6	GND

Table 4-18: Flash SPI ROM Connector Pinouts

PCIE-AM5**4.2.17 USB 3.2 Connector**

CN Label: USB3_3

CN Type: USB 3.2

CN Location: See **Figure 4-18**

The USB3_3 connector includes one USB 3.2 Gen 2 (10Gb/s).



Figure 4-18: USB 3.2 Locations

4.2.18 DP Connector

CN Label: DP1

CN Type: DP++ Connector

CN Location: See **Figure 4-19**

The DP++ connector connects to a display device with DisplayPort interface.



Figure 4-19: DP Locations

PCIE-AM5

4.2.19 USB 3.2 slots

CN Label:	USB3_4
CN Type:	USB 3.2 slot
CN Pinouts:	See Table 4-19
CN Location:	See Figure 4-20

The USB3_4 connector includes dual USB 3.2 Gen 2 (10Gb/s).

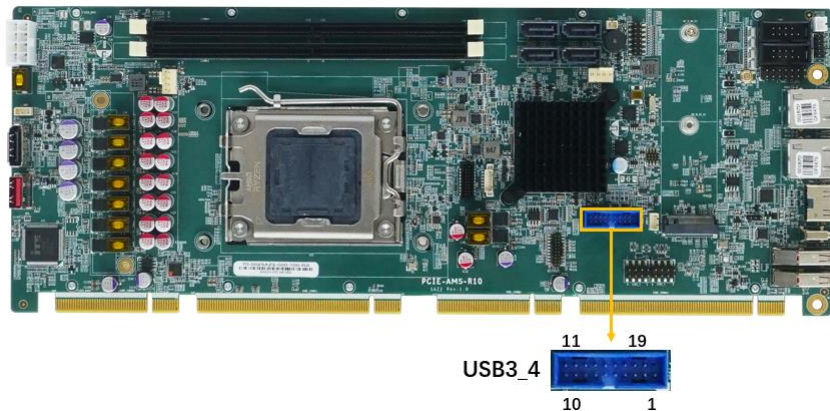


Figure 4-20: USB 3.2 Slot Locations

Pin	Description	Pin	Description
1	VCC1	11	SBD1+
2	USB3_RX1_DN	12	SBD1-
3	USB3_RX1_DP	13	GND
4	GND	14	USB3_TX2_DP
5	USB3_TX1_DN	15	USB3_TX2_DN
6	USB3_TX1_PD	16	GND
7	GND	17	USB3_RX2_DP
8	SBD0-	18	USB3_RX2_DN
9	SBD0+	19	VCC2
10	N/C		

Table 4-19: USB 3.2 Slot Pinouts

4.2.20 USB 2.0 Connector

- CN Label:USB2_1, USB2_5
- CN Type:USB 2.0
- CN Location:See Figure 4-21
- CN Pinouts:See Table 4-20

The USB2_1, USB2_5 connector includes dual USB 2.0.

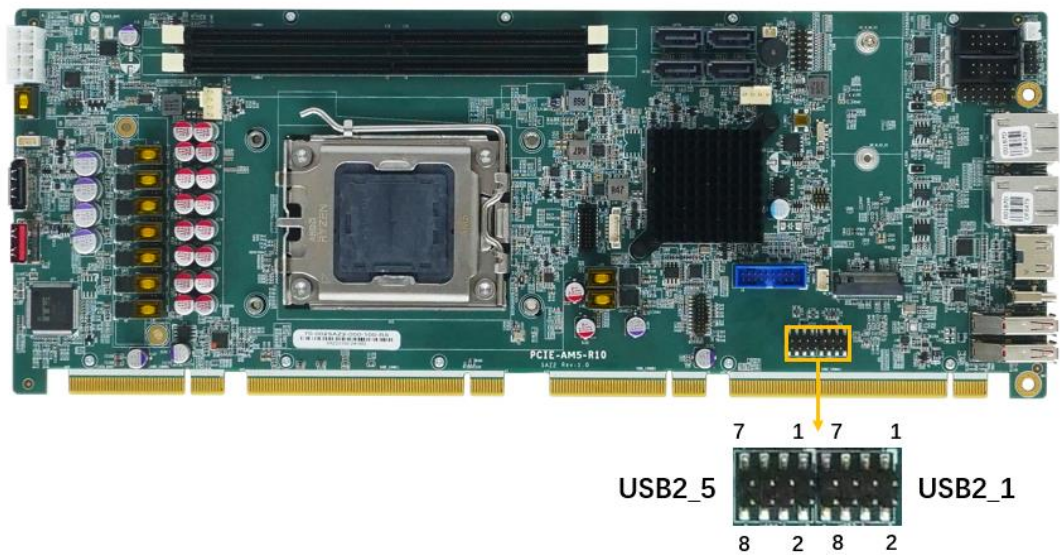


Figure 4-21: USB 2.0 Connector Locations

Pin	Description
1	+5V
2	USB_D2N
3	USB_D2P
4	GND
G3	GND
G4	USB_D2P
	USB_D2N
	+5V

Table 4-20: USB 2.0 Connector Pinouts

PCIE-AM5

4.2.21 DDR5 DIMM sockets

CN Label: DIMMA0, DIMMB0

CN Type: 288-pin socket

CN Location: See **Figure 4-22**

The DIMM slots are for DDR5 DIMM memory modules

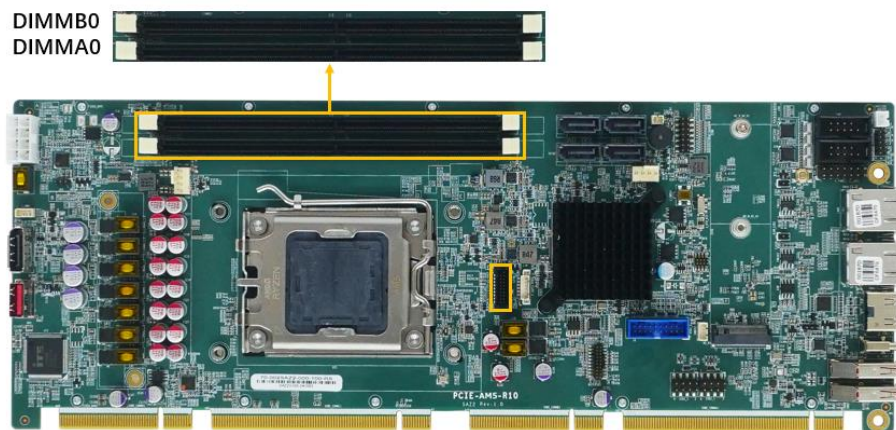


Figure 4-22: DDR5 DIMM Sockets Location

4.2.22 RS-232/422/485 Serial Port Connectors

- CN Label:

COM1, COM2
- CN Type:

9-pin header, p=2.54 mm
- CN Location:

See Figure 4-23
- CN Pinouts:

See Table 4-21

Each of these connectors provides RS-232/422/485 communications.

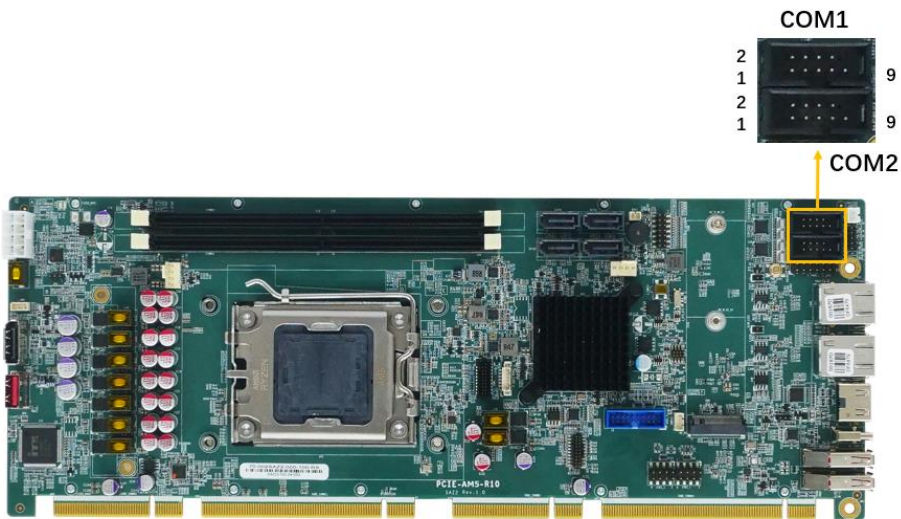


Figure 4-23: RS-232/422/485 Connector Location

PIN NO.	RS-232	RS-422	RS-485
1	DCD	TXD422	TXD485
2	RXD	TXD422+	TXD485+
3	TXD	RXD422+	
4	DTR	RXD422-	
5	GND		
6	DSR		
7	RTS		
8	CTS		

Table 4-21: RS-232/422/485 Connector Pinouts

4.3 External Peripheral Interface Connector Panel

The figure below shows the external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

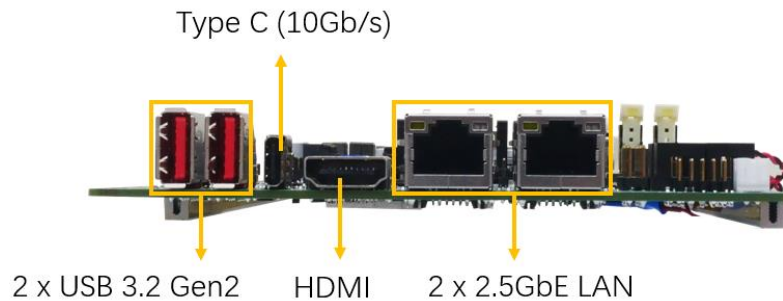


Figure 4-24: External Peripheral Interface Connector

4.3.1 External dual 2.5GbE RJ-45 connector

CN Label: LAN1, LAN2
CN Type: RJ45
CN Location: See Figure 4-25
CN Pinouts: See Table 4-22

The LAN1 and LAN2 is 2.5GbE RJ-45.



Figure 4-25: RJ45 Connector

Pin	Description	Pin	Description
R1	LAN_MDI0+	R2	LAN_MDI0-
R3	LAN_MDI1+	R4	LAN_MDI1-
R5	NC	R6	NC
R7	LAN_MDI2+	R8	LAN_MDI2-
R9	LAN_MDI3+	R10	LAN_MDI3-
L1	LAN_2.5G	L2	LAN_1G

Pin	Description	Pin	Description
L3	LAN_ACT-	L4	LAN_ACT+

Table 4-22: RJ45 Pinouts

4.3.2 External HDMI Connector

- CN Label: HDMI1
- CN Type: HDMI
- CN Location: See Figure 4-26
- CN Pinouts: See Table 4-23

The HDMI connector can connect to an HDMI device.

Pin	Description	Pin	Description
1	HDMI_DATA2	13	NC
2	GND	14	NC
3	HDMI_DATA2#	15	HDMI_SCL
4	HDMI_DATA1	16	HDMI_SDA
5	GND	17	GND
6	HDMI_DATA1#	18	+5V
7	HDMI_DATA0	19	HDMI_HPD
8	GND		
9	HDMI_DATA0#		
10	HDMI_CLK		
11	GND		

Table 4-23: HDMI Connector Pinouts



Figure 4-26: HDMI Connector

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4.3.3 External USB Connector

CN Label: UCBC1

CN Type: TYPEC

CN Location: See **Figure 4-27**

CN Pinouts: See **Table 4-24**

The USB connector connects to a TYPEC.



Figure 4-27: External USB Locations

PIN	Description	PIN	Description
A1	GND_A1	B1	GND_B1
A2	TX0_P	B2	TX1_P
A3	TX0_N	B3	TX1_N
A4	VBUS_A4	B4	VBUS_B4
A5	CC1	B5	CC2
A6	USB2_P_T	B6	USB2_P_B
A7	USB2_N_T	B7	USB2_N_B
A8	RFU1	B8	RFU2
A9	VBUS_A9	B9	VBUS_B9
A10	RX1_N	B10	RX0_N
A11	RXI_P	B11	RX0_P
A12	GND/-A12	B12	

Table 4-24: External USB Pinouts

4.3.4 External Dual USB 3.2 Gen 2 Connector

- CN Label:USB3_1
- CN Type:USB 3.2 Gen 2
- CN Location:See Figure 4-28
- CN Pinouts:See Table 4-25

The USB3_1 connector includes dual USB 3.2 Gen 2 (10Gb/s).



Figure 4-28: USB 3.2 Connector

Pin	Description	Pin	Description
1	+5V	G3	GND
2	USB_D1N	G4	GND
3	USB_D1P		
4	GND		
5	USB3_RX1_N		
6	USB3_RX1_P		
7	GND		
8	USB3_TX1_N		
9	USB3_TX1_P		
10	NC		
G1	GND		
G2	GND		

Table 4-25: USB 3.2 Connector Pinouts

Chapter

5

BIOS

5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.



NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. **Using keyboard:** Press the **DEL** or **F2** as soon as the system is turned on.
2. **Using touchscreen:** Press the **Setup** button on the upper right corner of the BIOS Starting Menu.

If the message disappears before the **DEL** or **F2** key is pressed, restart the computer and try again, then the BIOS Starting Menu will appear. Select "Setup" and press Enter to get into the BIOS Setup.

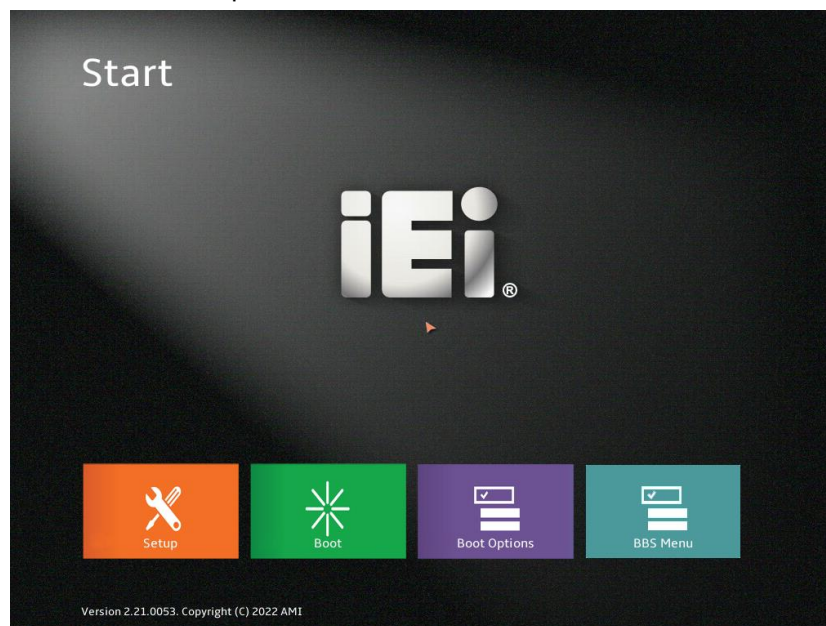


Figure 5-1: BIOS Starting Menu

PCIE-AM5

5.1.2 Using Setup

The BIOS Setup menu can be navigated by using a keyboard or a touchscreen.

5.1.2.1 Keyboard Navigation

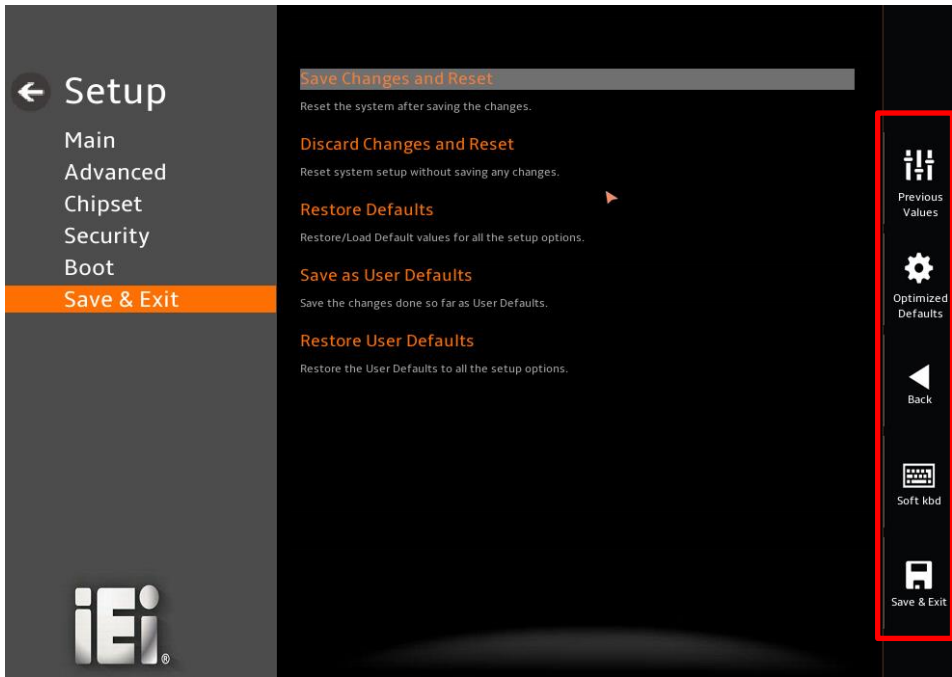
For keyboard navigation, use the navigation keys shown in **Table 5-1**.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes
-	Decrease the numeric value or make changes
Page Up	Move to the previous page
Page Dn	Move to the next page
Esc	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
F1	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2	Load previous values
F3	Load optimized defaults
F4	Save changes and Exit BIOS
<K>	Scroll help area upwards
<M>	Scroll help area downwards

Table 5-1: BIOS Navigation Keys

5.1.2.2 Touch Navigation

For touchscreen navigation, use the on-screen navigation keys shown below.



On-screen Button	Function
Previous Values	Load the last value you set.
Optimized Defaults	Load the factory default values in order to achieve the best performance.
Back	Return to the previous menu.
Soft kbd	Display the on-screen keyboard.
Save & Exit	Save the changes made to the BIOS options and reset the system.

Table 5-2: BIOS On-screen Navigation Keys

PCIE-AM5

5.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window, press the **Esc** key.

5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the clear CMOS button described in **Chapter 4**.

5.1.5 BIOS Menu Bar

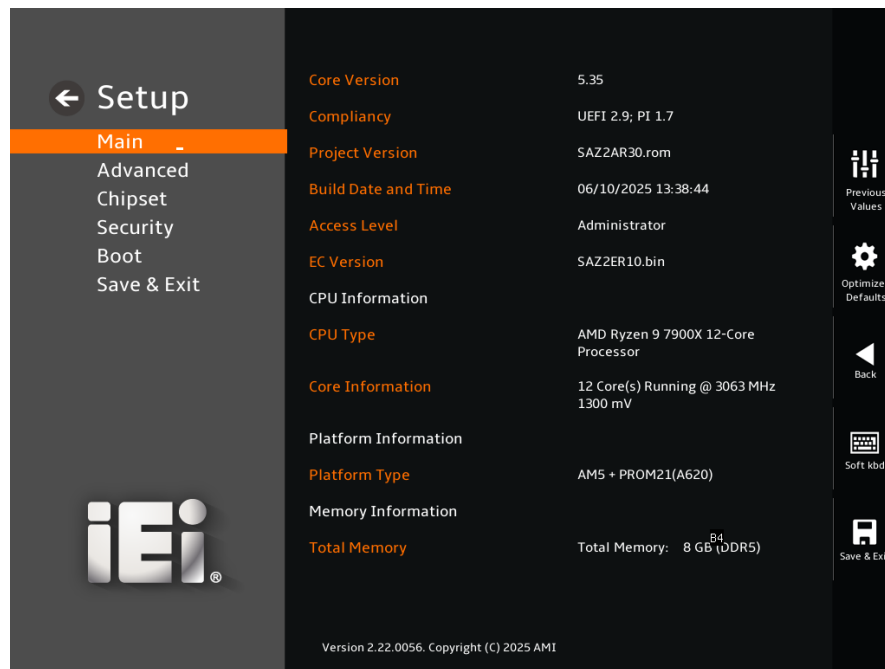
The **menu bar** on top of the BIOS screen has the following main items:

- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Security – Sets User and Supervisor Passwords.
- Boot – Changes the system boot configuration.
- Save & Exit – Selects exit options and loads default settings

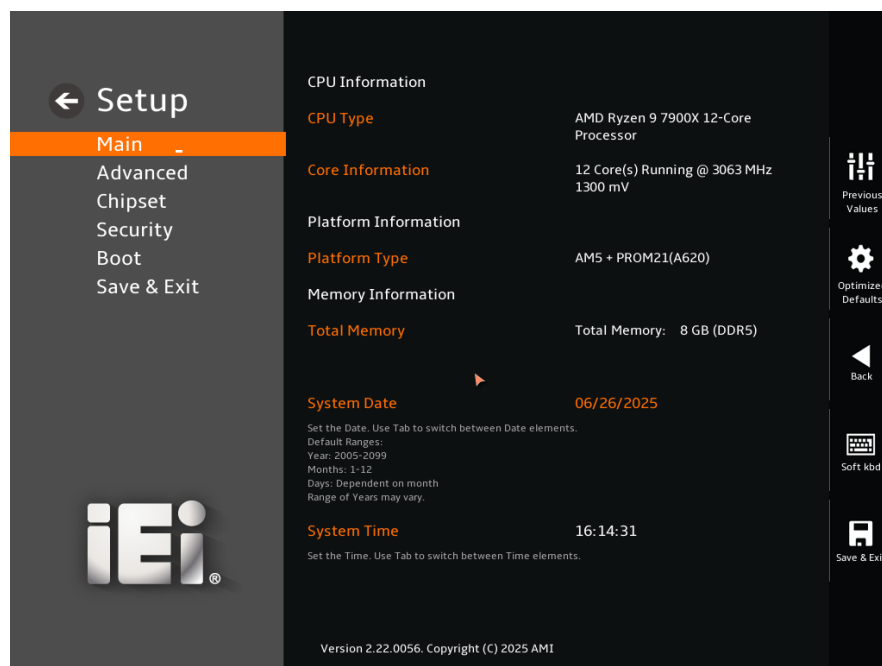
The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

5.2 Main

The **Main** BIOS menu (**BIOS Menu 1**) appears when the **BIOS Setup** program is entered. The **Main** menu gives an overview of the basic system information.



BIOS Menu 1: Main (1/2)



BIOS Menu 2: Main (2/2)

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➔ BIOS Information

The **BIOS Information** lists a brief summary of the BIOS. The fields in **BIOS Information** cannot be changed. The items shown in the system overview include:

- **BIOS Vendor:** Installed BIOS vendor
- **Core Version:** Current BIOS version
- **Compliance:** Current UEFI & PI version
- **Project Version:** the board version
- **Build Date and Time:** Date the current BIOS version was made
- **Access Level:** Administrator
- **EC Version:** Current EC version

➔ CPU Information

The **CPU Information** lists a brief summary of the CPU. The fields in **CPU Information** cannot be changed. The items shown in the system overview include:

- **CPU Type:** Displays the CPU Type
- **Core Information:** Displays the CPU Core Information

➔ Platform Information

The **Platform Information** lists a brief summary of the Platform. The fields in **Platform Information** cannot be changed. The items shown in the system overview include:

- **Platform Type:** Displays the PCH Name

➔ Memory Information

- **Total Memory:** Displays the Total Memory

➔ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

➔ **System Time [xx:xx:xx]**

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

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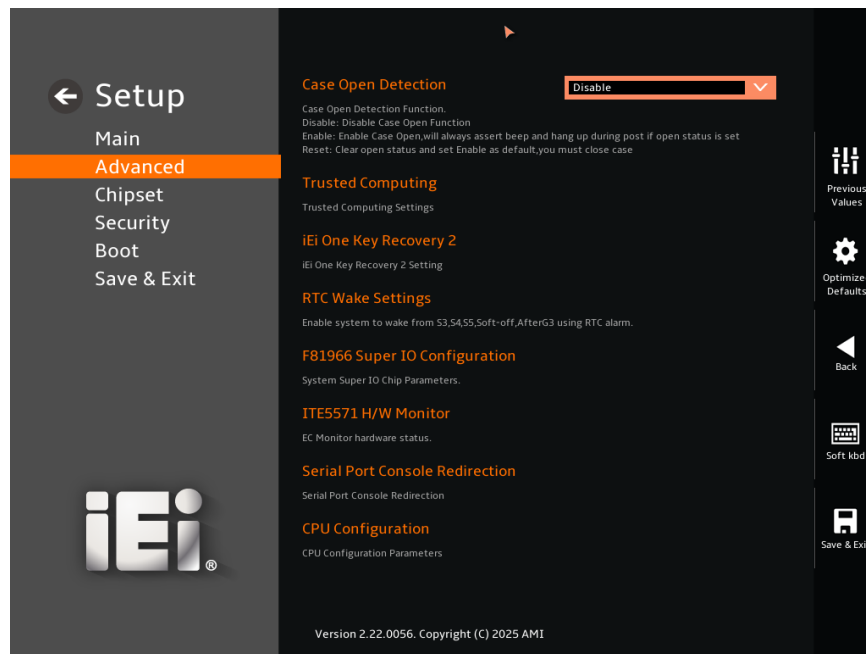
5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 3**) to configure the CPU and peripheral devices through the following sub-menus:

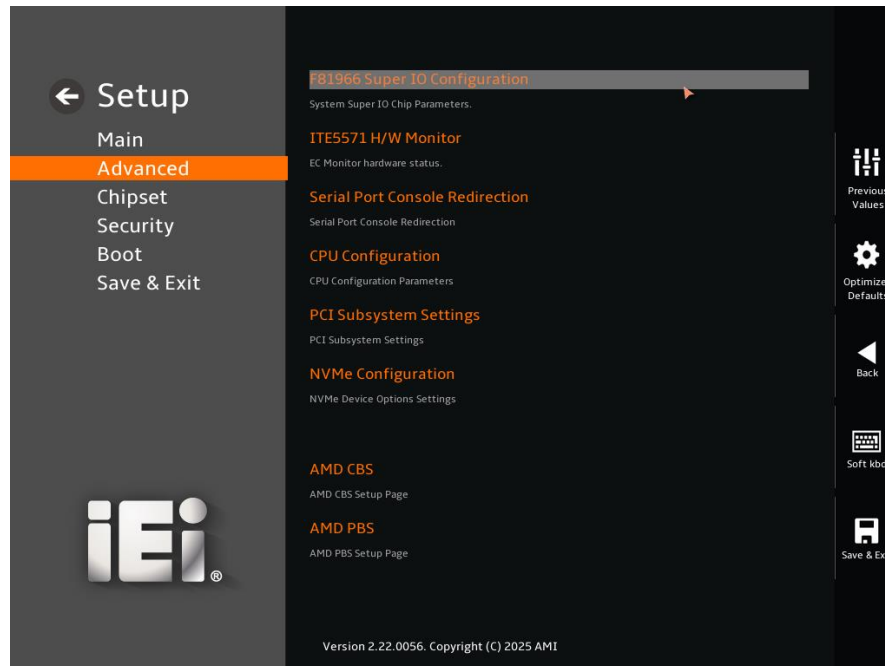


WARNING!

Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.



BIOS Menu 3: Advanced (1/2)

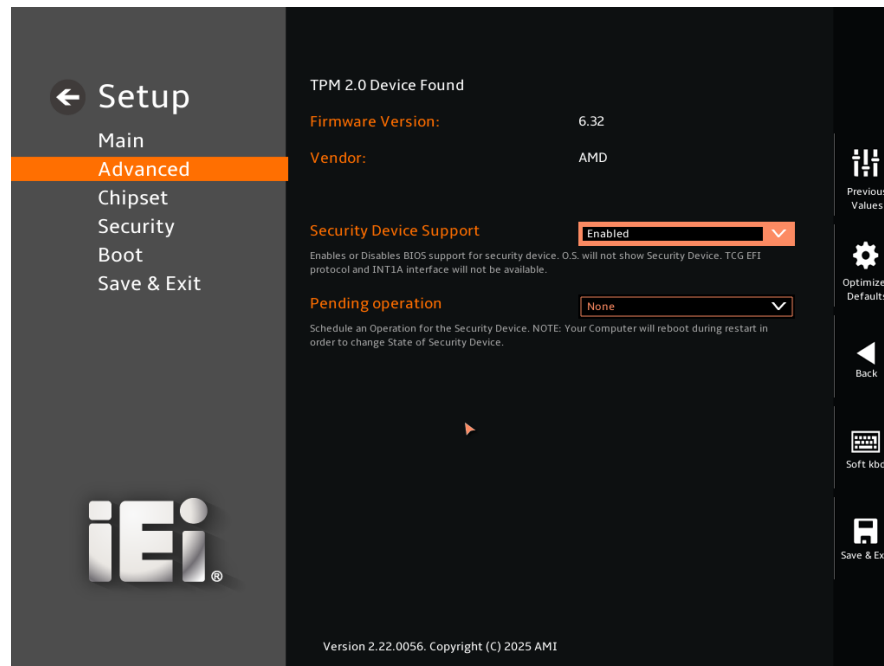


BIOS Menu 4: Advanced (2/2)

PCIE-AM5

5.3.1 Trusted Computing

Use the **Trusted Computing** menu (**BIOS Menu 5**) to configure settings related to the Trusted Computing Group (TCG) Trusted Platform Module (TPM).



BIOS Menu 5: Trusted Computing Configuration

➔ Security Device Support [Enable]

Use the **Security Device Support** option to enable or disable BIOS support for security device.

- ➔ **Disable** TPM support is disabled.
- ➔ **Enable** **DEFAULT** TPM support is enabled.

➔ Pending Operation [None]

Use the **Pending Operation** option to schedule an operation for the security device.

- ➔ **None** **DEFAULT** TPM information is previous.S
- ➔ **TPM Clear** TPM information is cleared

5.3.2 iEi One Key Recovery2

Use the **iEi One Key Recovery2** menu (**BIOS Menu 6**) to configure settings related to the iEi One Key Recovery2.



BIOS Menu 6: iEi One Key Recovery2

➔ **Auto Recovery Function [Enabled]**

Use the **Auto Recovery Function** option to enable or disable watch dog function, when OS crashes, it will automatically recover system.

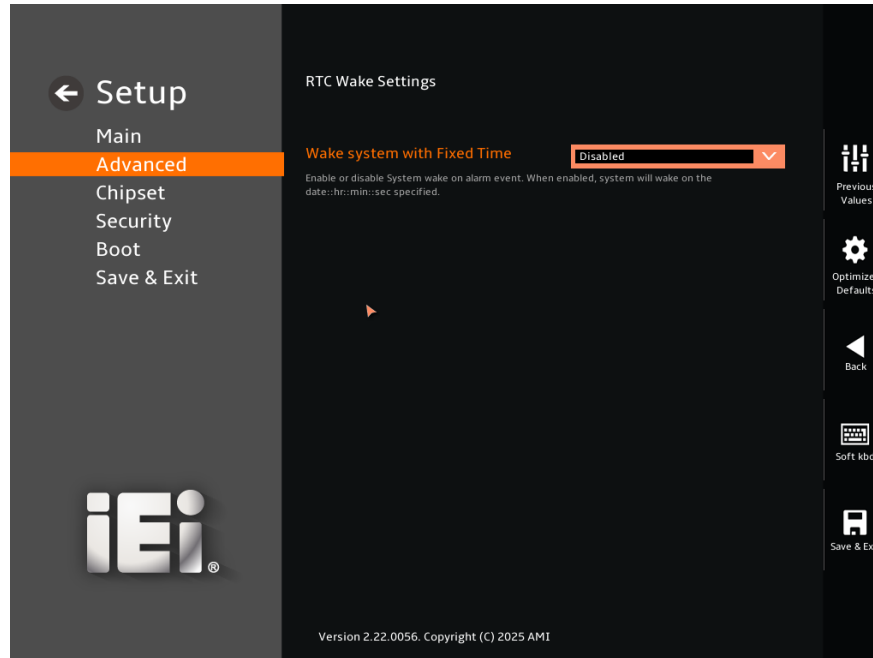
➔ **Disabled** Watch dog function is disabled.

➔ **Enabled** **DEFAULT** Watch dog function t is enabled.

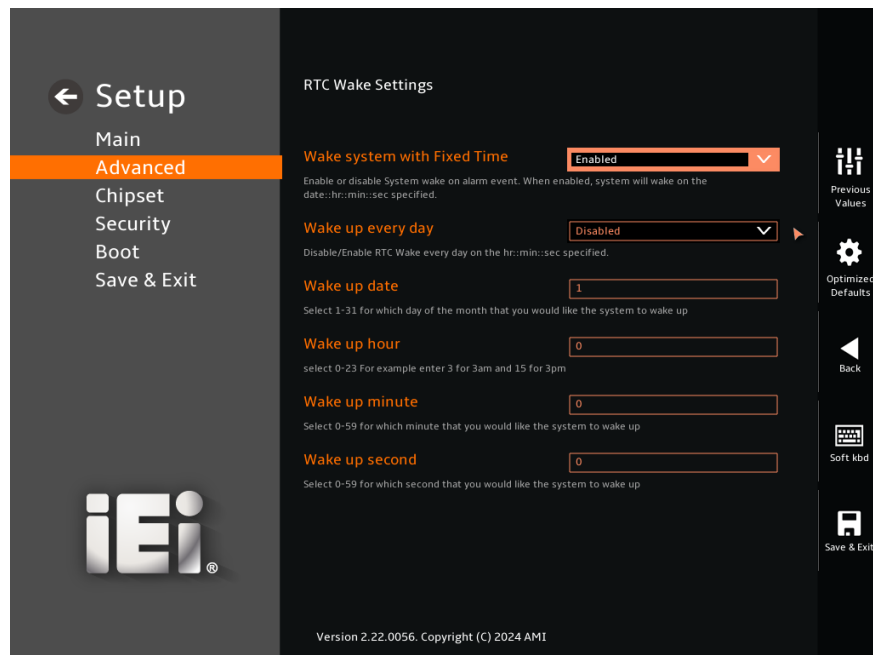
PCIE-AM5

5.3.3 RTC Wake Settings

The **RTC Wake Settings** menu (**BIOS Menu 7**) configures RTC wake event.



BIOS Menu 7: RTC Wake Settings (1/2)



BIOS Menu 8: RTC Wake Settings (2/2)

➔ **Wake system with Fixed Time [Enabled]**

Use the **Wake system with Fixed Time** option to enable or disable the system wake on alarm event.

➔ **Disabled**

The real time clock (RTC) cannot generate a wake event

➔ **Enabled DEFAULT**

If selected, the **Wake up every day** option appears allowing you to enable to disable the system to wake every day at the specified time. Besides, the following options appear with values that can be selected:

Wake up date

Wake up hour

Wake up minute

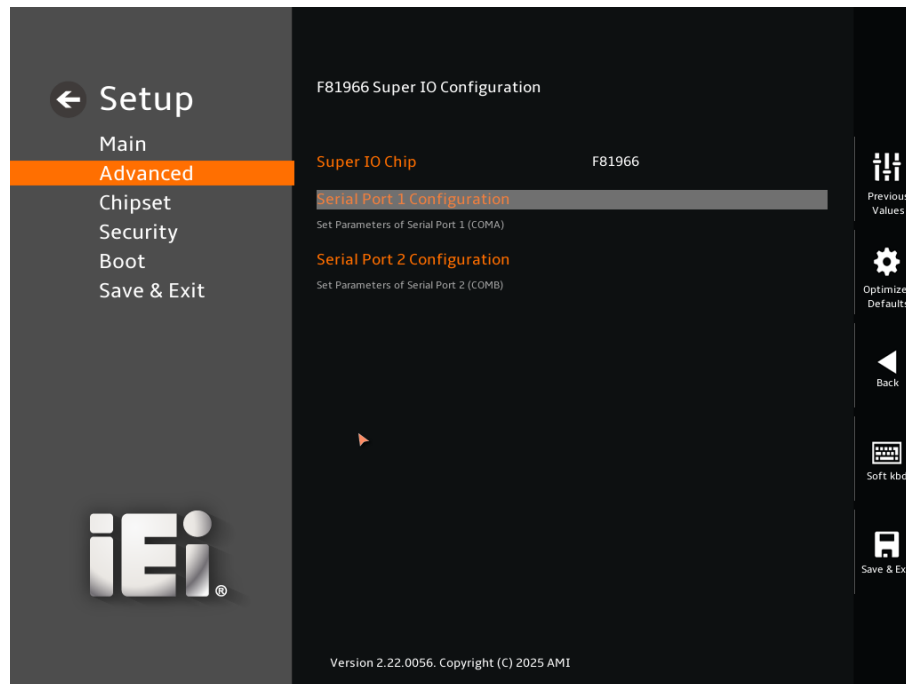
Wake up second

After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

PCIE-AM5

5.3.4 F81966 Super IO Configuration

Use the **F81966 Super IO Configuration** menu (**BIOS Menu 9**) to set or change the configurations for serial ports.

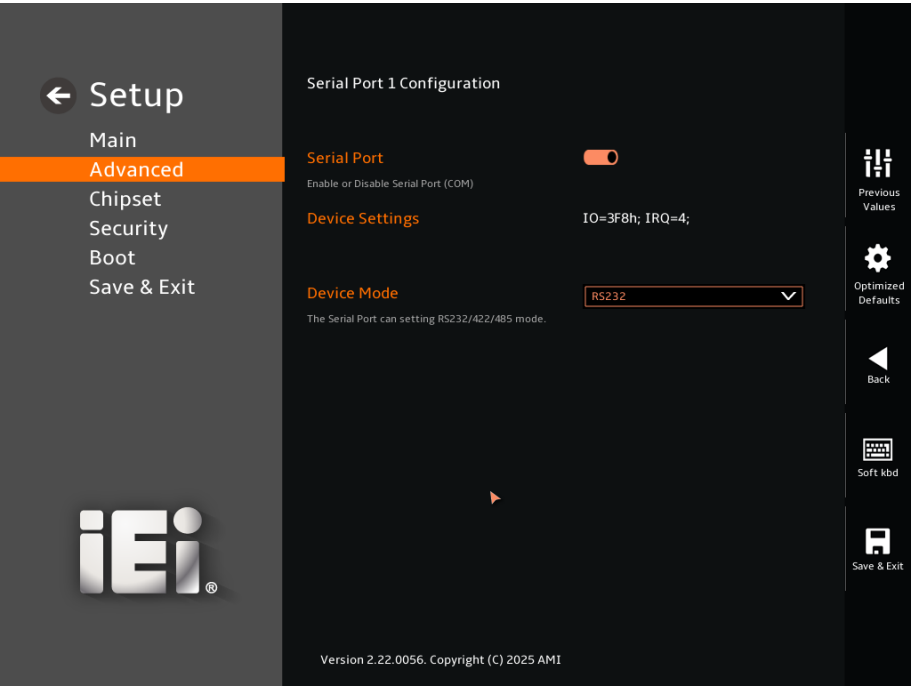


BIOS Menu 9: F81966 Super IO Configuration



5.3.4.1 Serial Port 1 Configuration

Use the **Serial Port 1 Configuration** menu (**BIOS Menu 10**) to configure the serial port.



BIOS Menu 10: Serial Port 1 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

- ➔ **Disabled** Disable the serial port
- ➔ **Enabled DEFAULT** Enable the serial port

➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

- ➔ **IO=3F8h; Serial Port I/O port address is 3F8h and the interrupt**
IRQ=4 address is IRQ4

➔ **Device Mode [RS232]**

Use the **Device Mode** option to change the serial port mode.

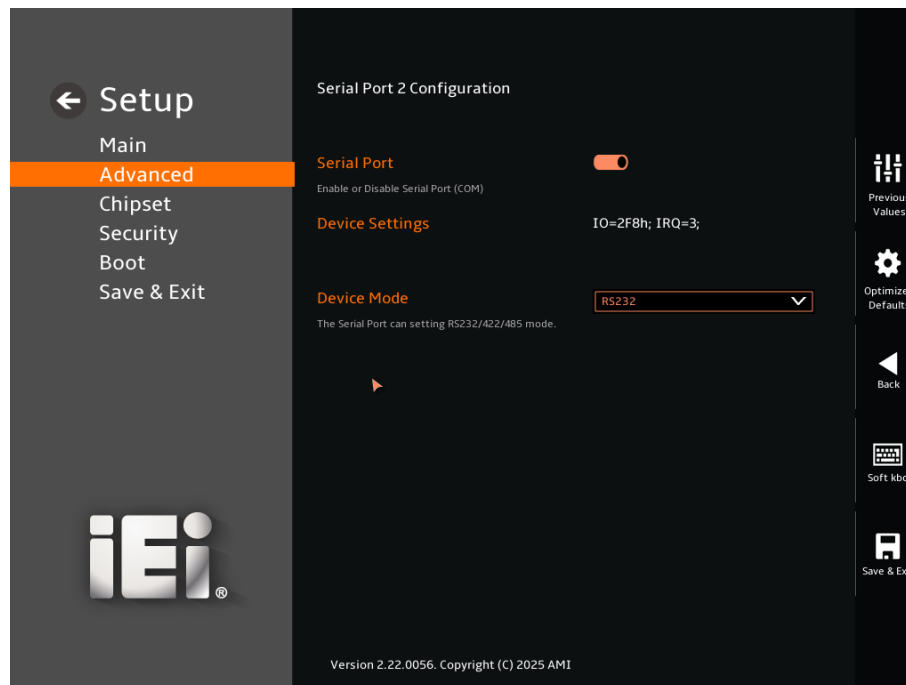


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- ➔ **RS232** **DEFAULT** The serial port mode is RS-232
- RS422 with Register** The serial port mode is RS-422
- RS485 with Register** The serial port mode is RS-485

5.3.4.2 Serial Port 2 Configuration

Use the **Serial Port 2 Configuration** menu (**BIOS Menu 11**) to configure the serial port.



BIOS Menu 11: Serial Port 2 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

- ➔ **Disabled** Disable the serial port
- ➔ **Enabled** **DEFAULT** Enable the serial port

➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.



➔ IO=2F8h; Serial Port I/O port address is 2F8h and the interrupt
IRQ=3 address is IRQ3

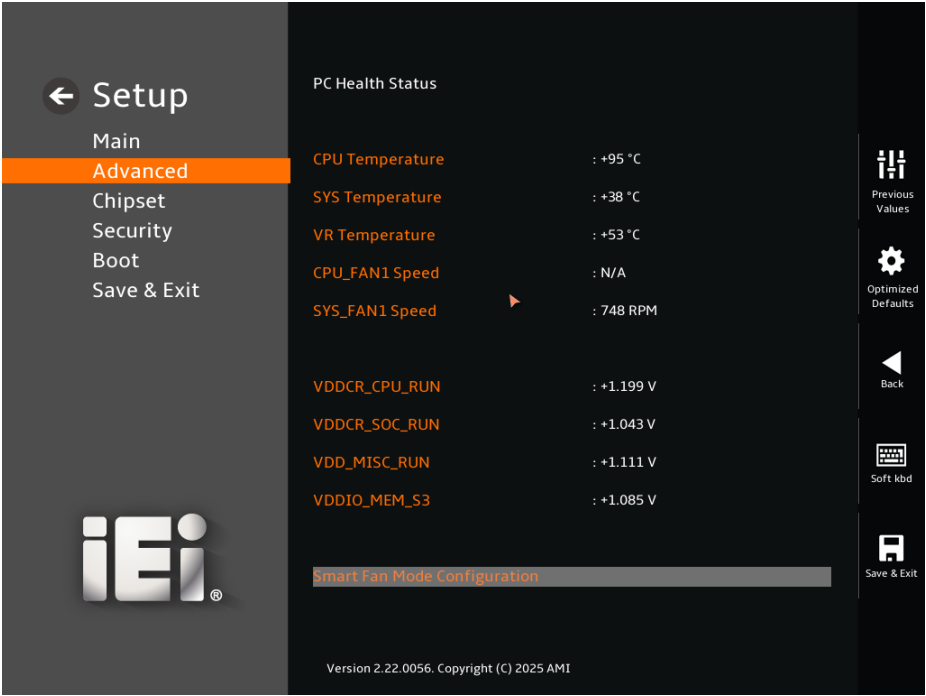
➔ Device Mode [RS232]

Use the **Device Mode** option to change the serial port mode.

➔ RS232	DEFAULT	The serial port mode is RS-232
RS422 with Register		The serial port mode is RS-422
RS485 with Register		The serial port mode is RS-485

5.3.5 ITE5571 H-W Monitor

The **ITE5571 H-W Monitor** menu (**BIOS Menu 12**) contains the smart fan mode configuration submenu and shows the state of H/W real-time operating temperature, fan speeds and system voltages.



BIOS Menu 12: ITE5571 H-W Monitor



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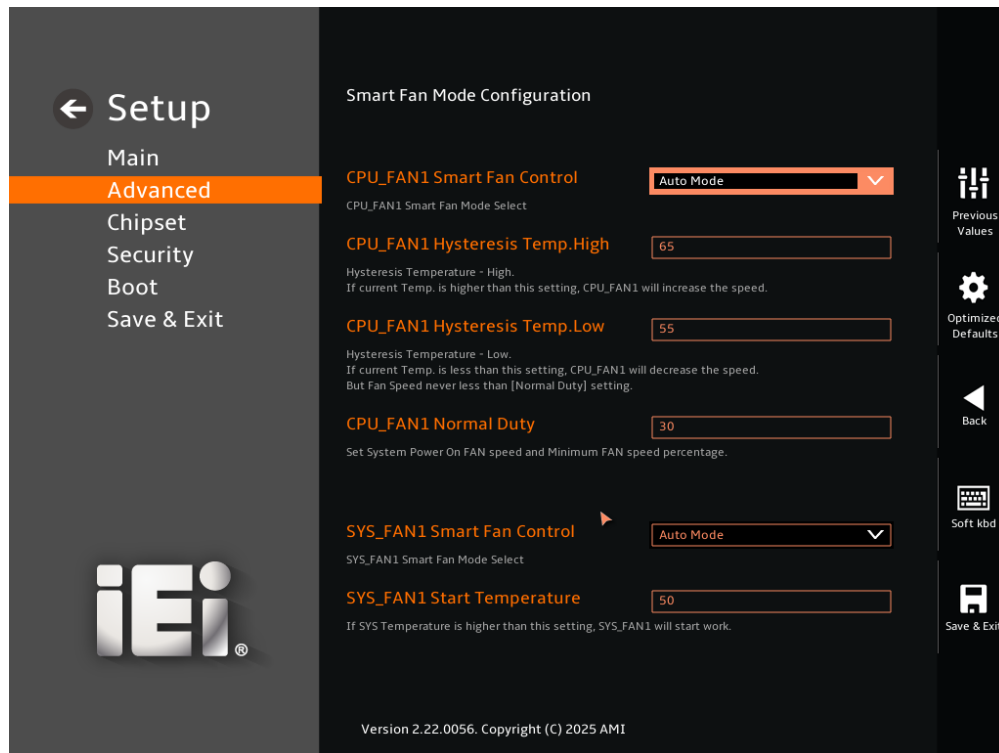
➔ PC Health Status

The following system parameters and values are shown. The system parameters that are monitored are:

- System Temperatures:
 - CPU Temperature
 - System Temperature
 - VR Temperature
- Fan Speeds:
 - CPU_Fan1 Speed
 - SYS_Fan1 Speed
- Voltages:
 - VDDCR_CPU_RUN
 - VDDCR_SOC_RUN
 - VDDCR_MISC_RUN
 - VDDCR_MEM_S3

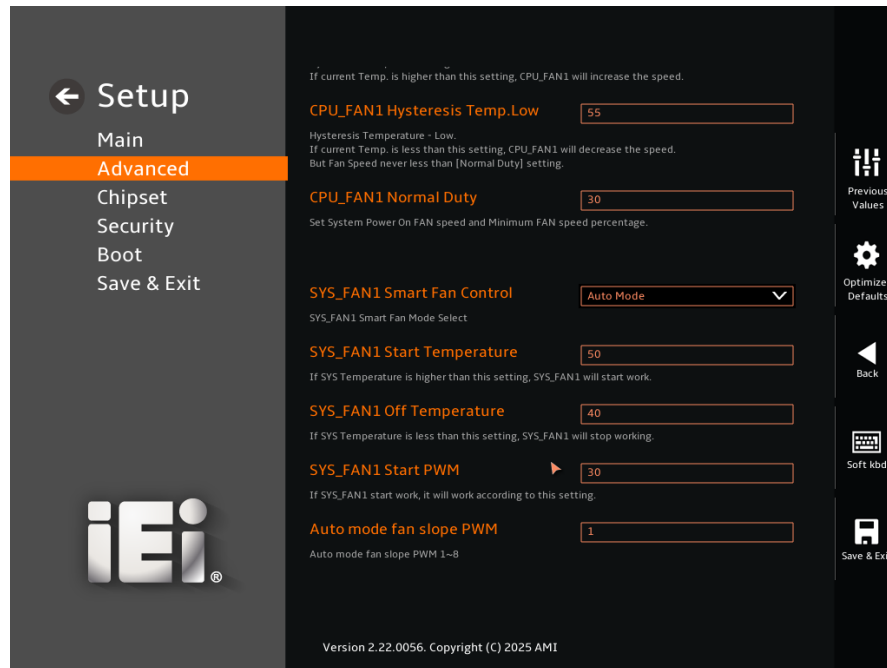
5.3.5.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 13**) to configure the CPU/system fan start/off temperature and control mode.



BIOS Menu 13: Smart Fan Mode Configuration (1/2)

PCIE-AM5



BIOS Menu 14: Smart Fan Mode Configuration (2/2)

→ CPU_FAN1 Smart Fan Control [Auto Mode]

Use the **CPU_FAN1 Smart Fan Control** option to configure the CPU Smart Fan.

- **Manual Mode** The fan spins at the speed set in Manual Mode settings.
- **Auto Mode** **DEFAULT** The fan adjusts its speed using Auto Mode settings.

→ CPU_FAN1 Hysteresis Temp.High [65]

Use the **CPU_FAN1 Hysteresis Temp.High** option to set value. If current temperature is higher than this setting, CPU_FAN1 will increase the speed.

→ CPU_FAN1 Hysteresis Temp.Low [55]

Use the **CPU_FAN1 Hysteresis Temp. Low** option to set value. If current temperature is lower than this setting, CPU_FAN1 will decrease the speed.



➔ CPU_FAN1 Normal Duty [30]

Use the **CPU_FAN1 Normal Duty** option to set system power on fan speed and minimum fan speed percentage.

➔ SYS_FAN1 Smart Fan Control [Auto Mode]

Use the **SYS_FAN1 Smart Fan Control** option to configure the System Smart Fan.

- ➔

Manual Mode

The fan spins at the speed set in Manual Mode settings.
- ➔

Auto Mode

DEFAULTThe fan adjusts its speed using Auto Mode settings.

➔ SYS_FAN1 Start Temperature [50]

If the SYS temperature is high than the value, the SYS_FAN1will start working. To set a value, Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ SYS_FAN1 Off Temperature

If the SYS temperature is lower than the value, the SYS_FAN1will stop working. To set a value, Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ SYS_FAN1 Start PWM

Use the **SYS_FAN1 Start PWM** option to set the PWM start value. Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ Auto mode fan slope PWM

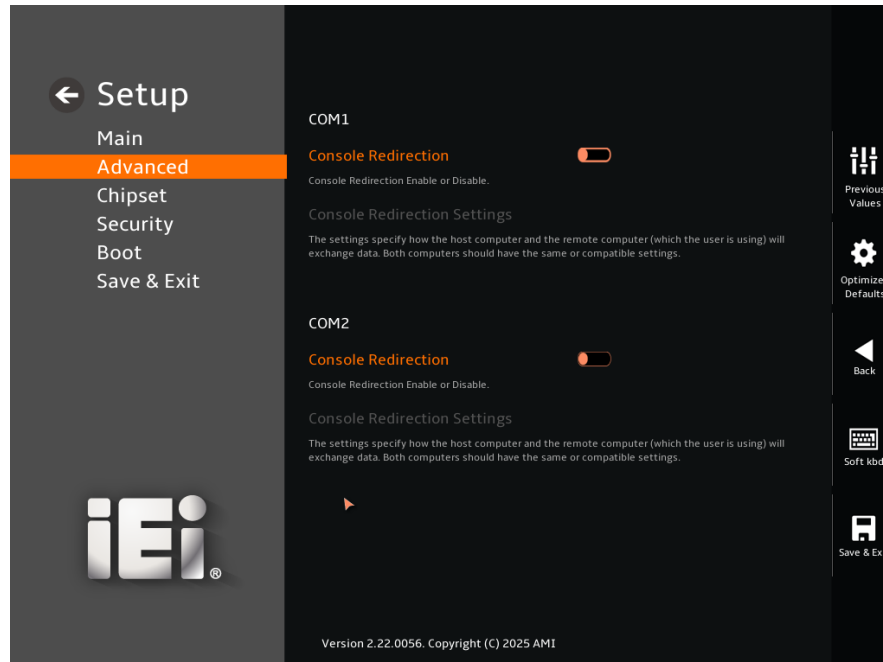
Use the **Auto mode fan slope PWM** option to set the PWM start value. Use the + or – key to change the value or enter a decimal number between 1 and 100.



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5.3.6 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 15**) allows the console redirection options to be configured. Console Redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.



BIOS Menu 15: Serial Port Console Redirection

➔ **Console Redirection [Disabled]**

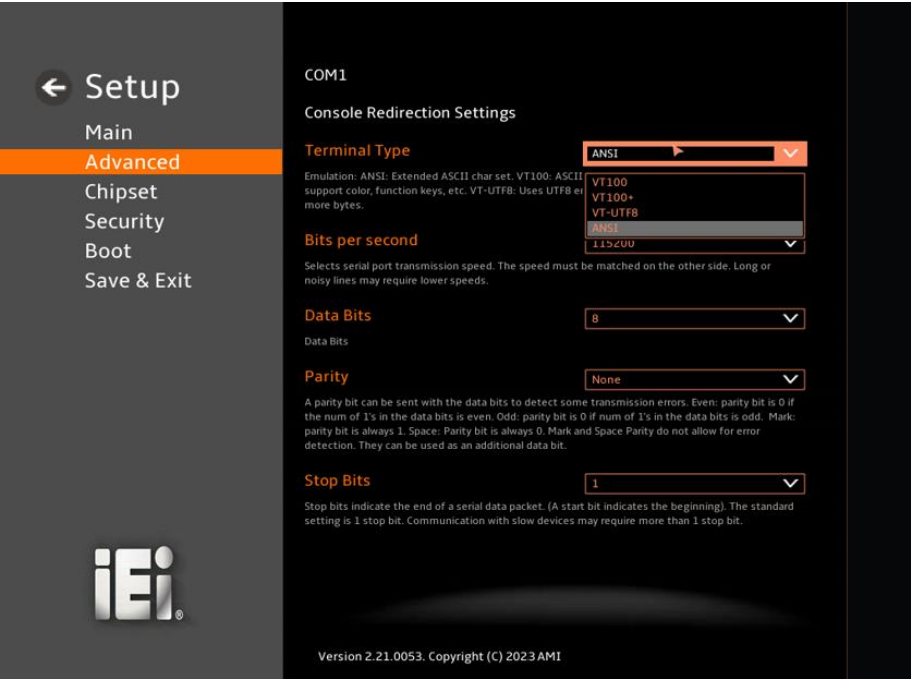
Use **Console Redirection** option to enable or disable the console redirection function.

- ➔ **Disabled** **DEFAULT** Disabled the console redirection function
- ➔ **Enabled** Enabled the console redirection function

The **Console Redirection Settings** submenu will be available when the **Console Redirection** option is enabled.

5.3.6.1 Console Redirection Settings

The following options are available in the **Console Redirection Settings** submenu (**BIOS Menu 16**) when the **COM Console Redirection** (for COM1 to COM6) option is enabled.



BIOS Menu 16: COM Console Redirection Settings

➔ Terminal Type [ANSI]

Use the **Terminal Type** option to specify the remote terminal type.

- ➔

VT100

The target terminal type is VT100
- ➔

VT100+

The target terminal type is VT100+
- ➔

VT-UTF8

The target terminal type is VT-UTF8
- ➔

ANSI

DEFAULT

The target terminal type is ANSI

➔ Bits per second [115200]

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match on the other side. Long or noisy lines may require lower speeds.

PCIE-AM5

- ➔ **9600** Sets the serial port transmission speed at 9600.
- ➔ **19200** Sets the serial port transmission speed at 19200.
- ➔ **38400** Sets the serial port transmission speed at 38400.
- ➔ **57600** Sets the serial port transmission speed at 57600.
- ➔ **115200** **DEFAULT** Sets the serial port transmission speed at 115200.

➔ **Data Bits [8]**

Use the **Data Bits** option to specify the number of data bits.

- ➔ **7** Sets the data bits at 7.
- ➔ **8** **DEFAULT** Sets the data bits at 8.

➔ **Parity [None]**

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

- ➔ **None** **DEFAULT** No parity bit is sent with the data bits.
- ➔ **Even** The parity bit is 0 if the number of ones in the data bits is even.
- ➔ **Odd** The parity bit is 0 if the number of ones in the data bits is odd.
- ➔ **Mark** The parity bit is always 1. This option does not allow for error detection.
- ➔ **Space** The parity bit is always 0. This option does not allow for error detection.

➔ **Stop Bits [1]**

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

- ➔ **1** **DEFAULT** Sets the number of stop bits at 1.



➔ 2

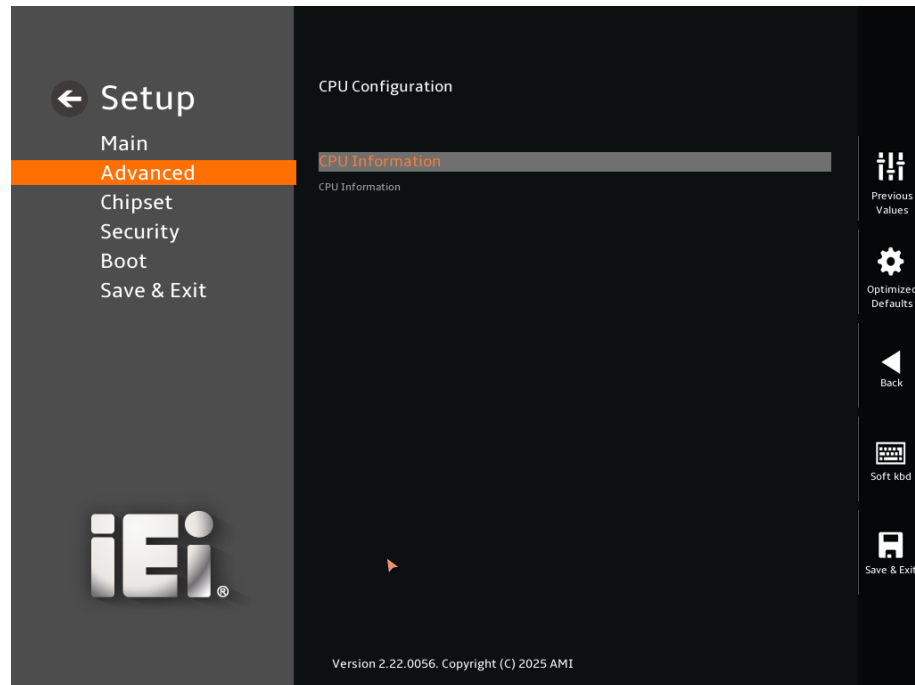
Sets the number of stop bits at 2.



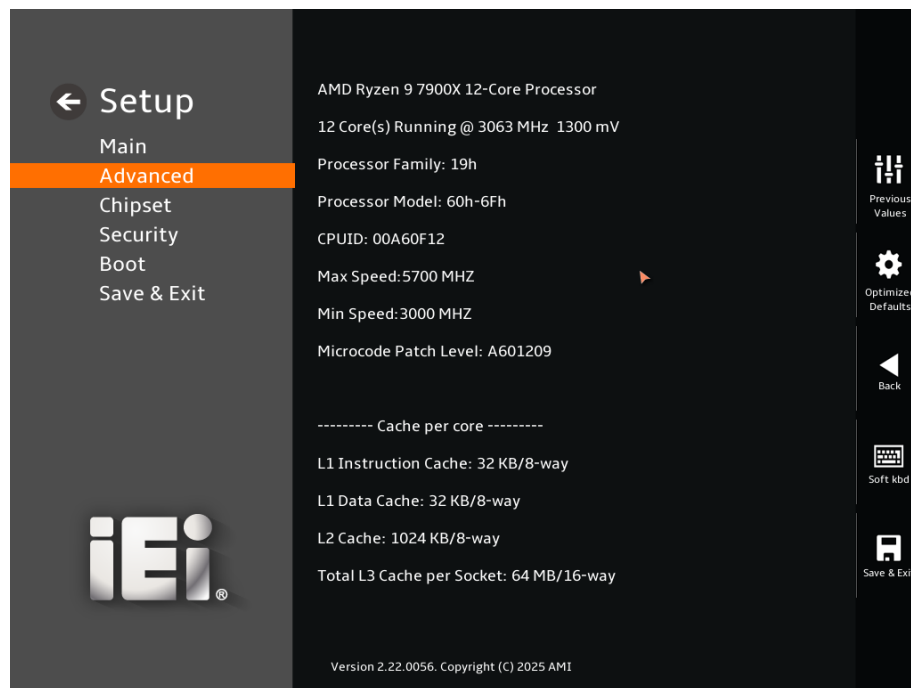
PCIE-AM5

5.3.7 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 18**) to view detailed CPU specifications.



BIOS Menu 17: CPU Configuration (1/2)

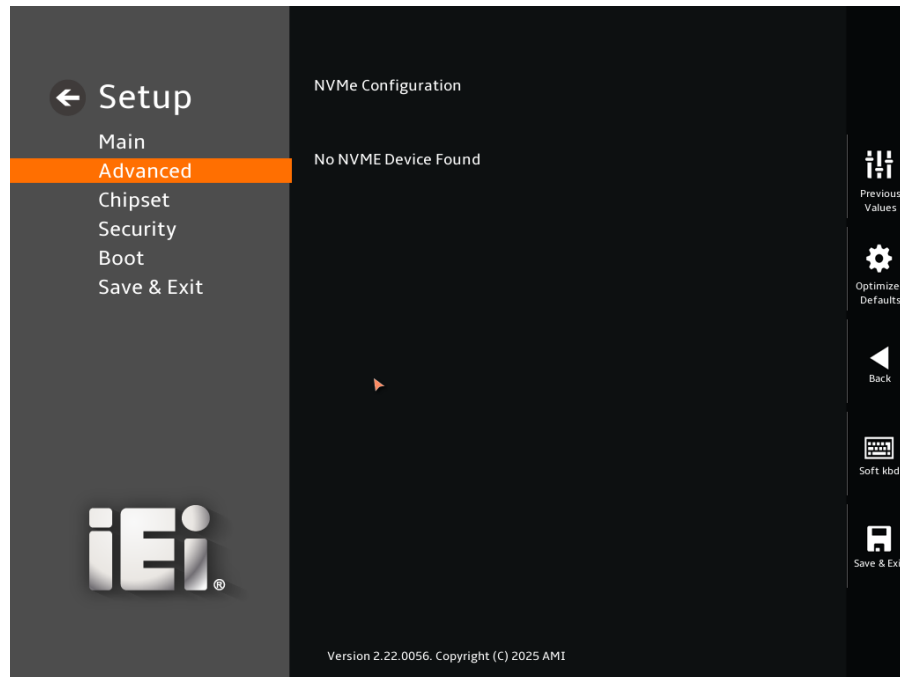


BIOS Menu 18: CPU Configuration (2/2)

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5.3.8 NVMe Configuration

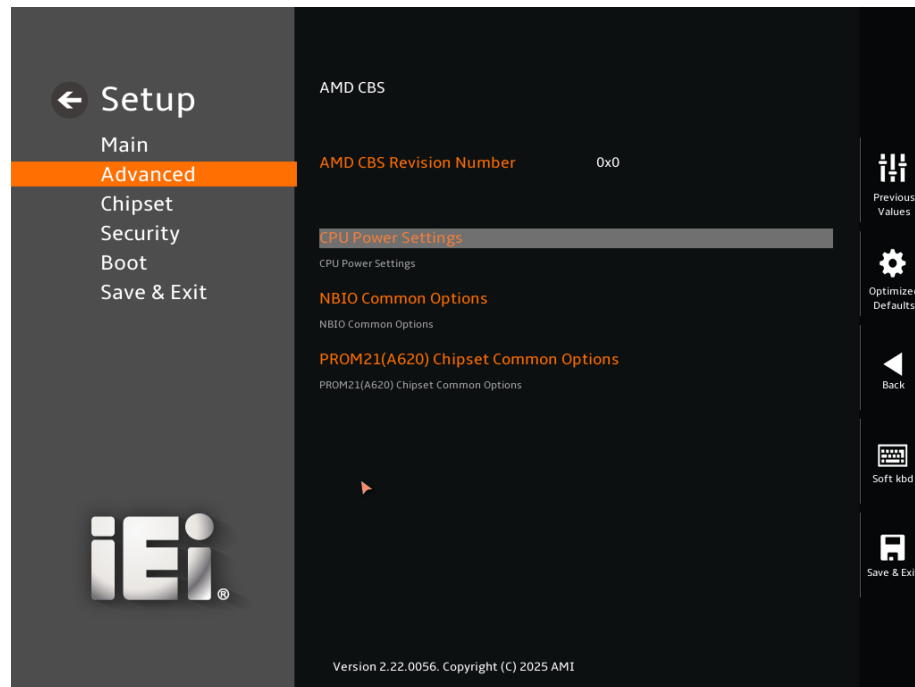
Use the **NVMe Configuration (BIOS Menu 19)** menu to display the NVMe controller and device information.



BIOS Menu 19: NVMe Configuration

5.3.9 AMD CBS

Use the **AMD CBS (BIOS Menu 20)** menu to display the AMD Core BIOS Settings.

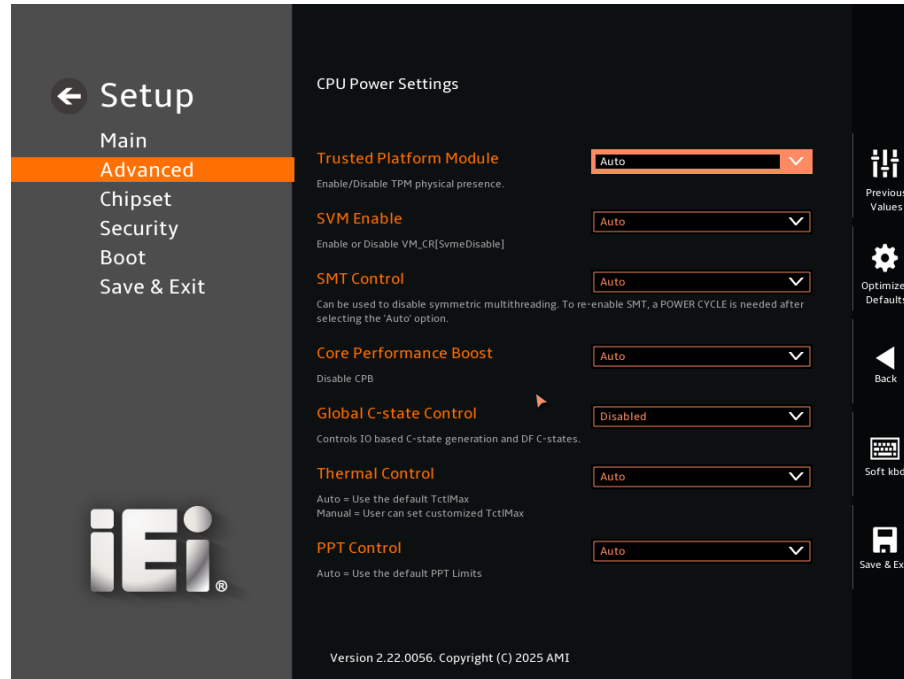


BIOS Menu 20: AMD CBS

PCIE-AM5

5.3.9.1 CPU Power Settings

Use the **CPU Power Settings (BIOS Menu 21)** menu to display the CPU Power Settings.



BIOS Menu 21: CPU Power Settings

➔ **Trusted Platform Module [Auto]**

Use the **Trusted Platform Module** option to enable or disable the TPM.

- ➔ **Auto** **DEFAULT** Enable the TPM.
- ➔ **Disable** Disable the TPM.

➔ **SVM Enable [Auto]**

Use the **SVM Enable** option to enable or disable the SVM.

- ➔ **Auto** **DEFAULT** Enable the SVM.
- ➔ **Disable** Disable the SVM.

→ SMT Control [Auto]

Use the **SMT Control** option to enable or disable the symmetric multithreading.

- | | | | |
|---|----------------|----------------|---------------------------------------|
| → | Auto | DEFAULT | Enable the symmetric multithreading. |
| → | Disable | | Disable the symmetric multithreading. |

→ Core Performance Boost [Auto]

Use the **Core Performance Boost** option to enable or disable the CPB.

- | | | | |
|---|----------------|----------------|------------------|
| → | Auto | DEFAULT | Enable the CPB. |
| → | Disable | | Disable the CPB. |

→ Global C-state Control [Auto]

Use the **Global C-state Control** option to enable or disable the IO based C-state generation and DF C-states.

- | | | | |
|---|----------------|----------------|--|
| → | Auto | DEFAULT | Enable the IO based C-state generation and DF C-states. |
| → | Disable | | Disable the IO based C-state generation and DF C-states. |

→ Thermal Control [Auto]

Use the **Thermal Control** option to use the TctlMax.

- | | | | |
|---|---------------|----------------|--------------------------|
| → | Auto | DEFAULT | Use the default TctlMax. |
| → | Manual | | Customized the TctlMax. |

→ PPT Control [Auto]

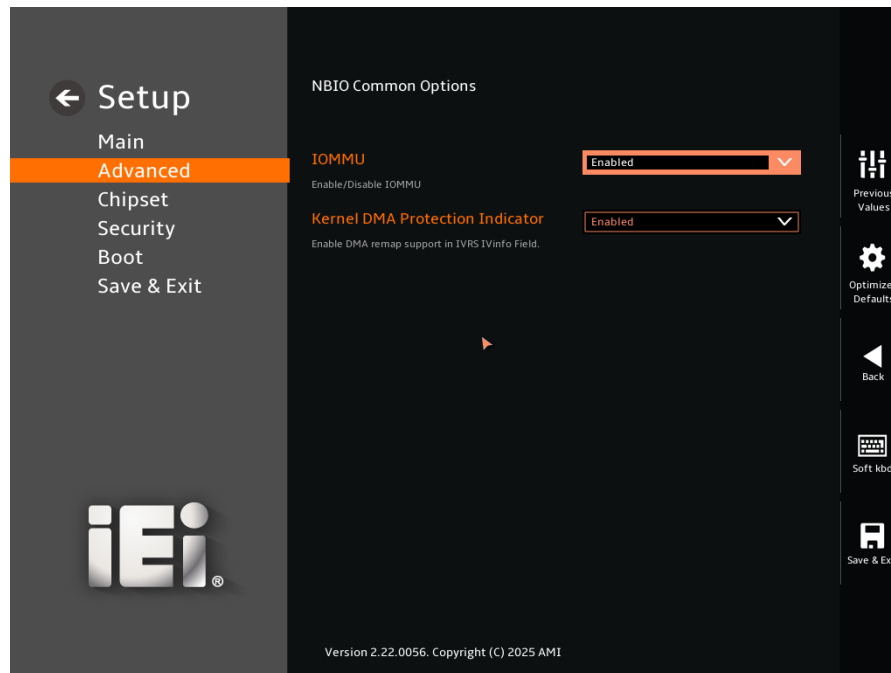
Use the **PPT Control** option to use the PPT Limits.

- | | | | |
|---|---------------|----------------|-----------------------------|
| → | Auto | DEFAULT | Use the default PPT Limits. |
| → | Manual | | Customized the PPT Limits. |

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5.3.9.2 NBIO Common Options

Use the **NBIO Common Options (BIOS Menu 22)** menu to display the NBIO Common Options.



BIOS Menu 22: NBIO Common Options

→ IOMMU [Enabled]

Use the **IOMMU** option to enable or disable the IOMMU.

- **Enabled** **DEFAULT** Enable the IOMMU.
- **Disable** Disable the IOMMU.
- **Auto** Automatically enable or disable IOMMU.

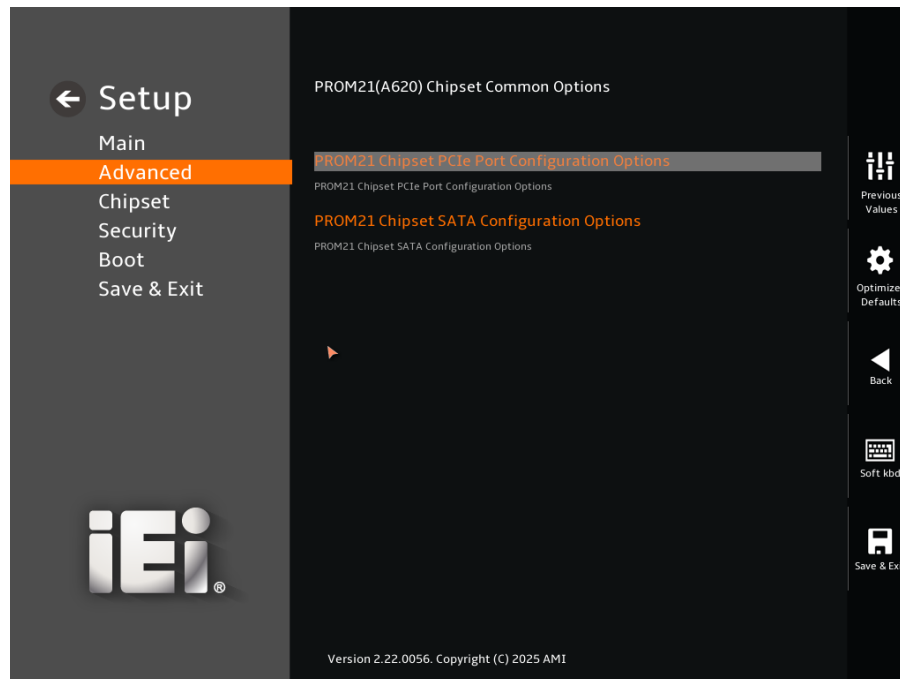
→ Kernel DMA Protection Indicator [Enabled]

Use the **Kernel DMA Protection Indicator** option to enable or disable the DMA remap support in IVRS IVinfo field.

- **Enabled** **DEFAULT** Enable the DMA remap support in IVRS IVinfo field.
- **Disable** Disable the DMA remap support in IVRS IVinfo field.

5.3.9.3 PROM21(A620) Chipset Common Options

Use the **PROM21(A620) Chipset Common Options (BIOS Menu 23)** menu to display the PROM21(A620) Chipset Common Options.

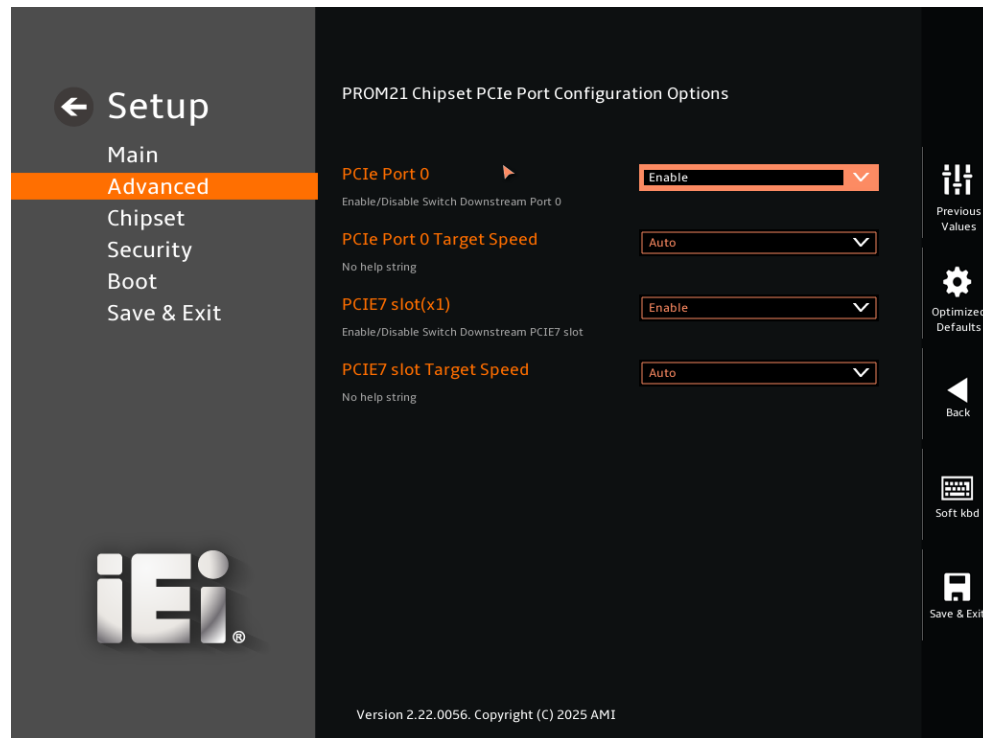


BIOS Menu 23: PROM21(A620) Chipset Common Options

PCIE-AM5

5.3.9.3.1 PROM21 Chipset PCIe Port Configuration Options

Use the **PROM21 Chipset PCIe Port Configuration Options (BIOS Menu 24)** menu to display the PROM21 Chipset PCIe Port Configuration Options.

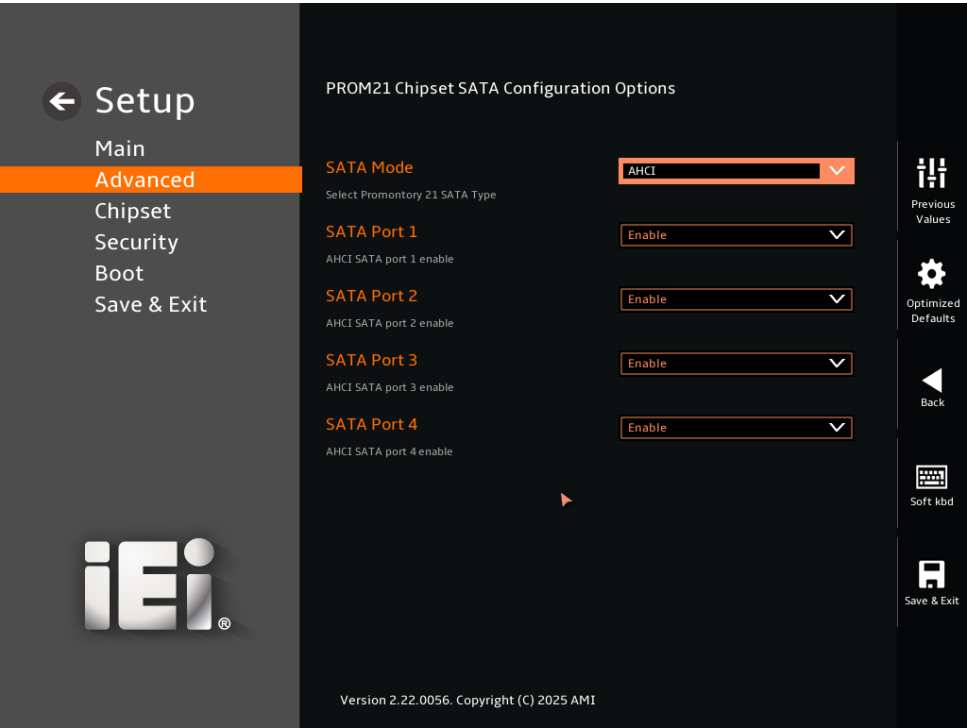


BIOS Menu 24: PROM21 Chipset PCIe Port Configuration Options



5.3.9.3.2 PROM21 Chipset SATA Configuration Options

Use the **PROM21 Chipset SATA Configuration Options (BIOS Menu 25)** menu to display the PROM21 Chipset SATA Configuration Options.



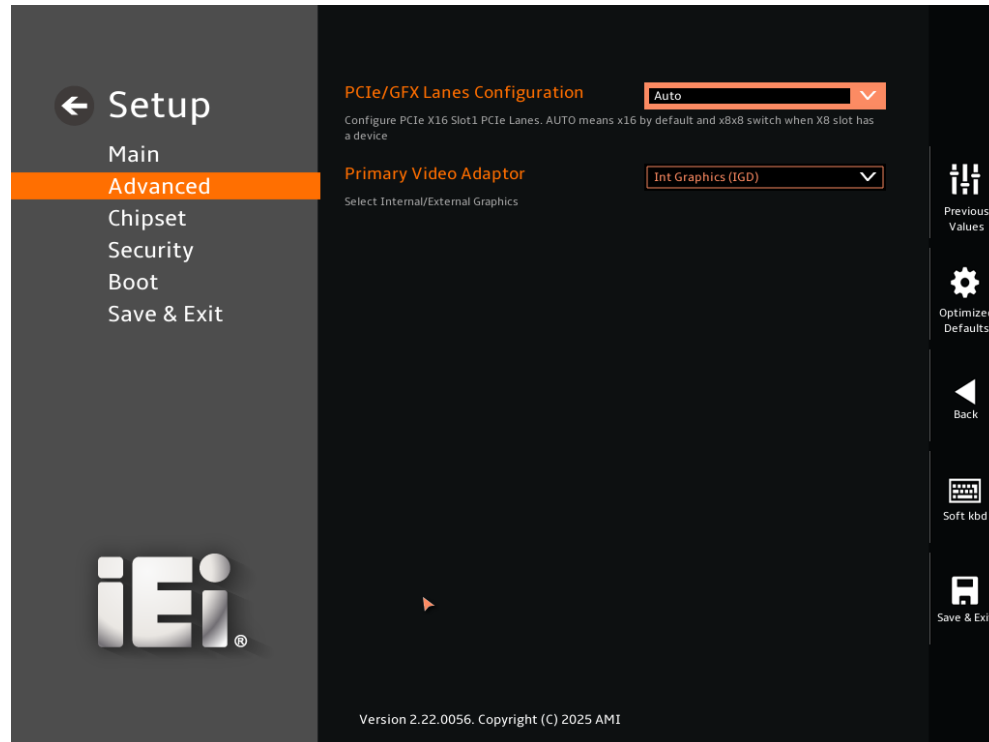
BIOS Menu 25: PROM21 Chipset SATA Configuration Options



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5.3.10 AMD PBS

Use the **AMD PBS (BIOS Menu 26)** menu to set AMD PBS.



BIOS Menu 26: AMD PBS

➔ PCie/GFX Lanes Configuration [Auto]

Use the **PCie/GFX Lanes Configuration** option to configure PCIe x16 slot.

- | | | | |
|---|-----------------|----------------|---|
| ➔ | Auto | DEFAULT | Default x16 and auto switches to x8/x8 when x8 slot is populated. |
| ➔ | x16 | | One x16 slot. |
| ➔ | x8x8 | | Two x8 slots. |
| ➔ | x8x4x4 | | One x8 and two x4 slots. |
| ➔ | x4x4x8 | | Two x4 and one x8 slots. |
| ➔ | x4x4x4x4 | | Four x4 slots. |

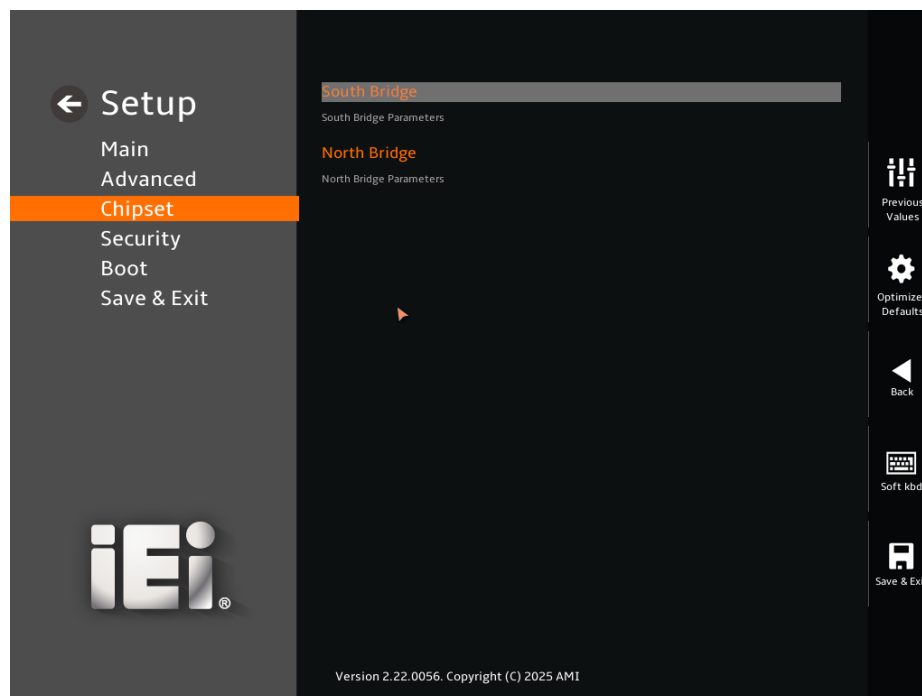
5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 27**) to access the South Bridge and North Bridge configuration menus.



WARNING!

Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.



BIOS Menu 27: Chipset

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5.4.1 South Bridge

Use the **South Bridge** menu (**BIOS Menu 28**) to configure the parameters.



BIOS Menu 28: South Bridge Configuration

➔ Power Saving Function (EUP) [Disabled]

Use the **Power Saving Function (EUP)** BIOS option to enable or disable the power saving function.

- ➔ **Disabled** **DEFAULT** Power saving function is disabled.
- ➔ **Enabled** Power saving function is enabled. It will reduce power consumption when the system is off.

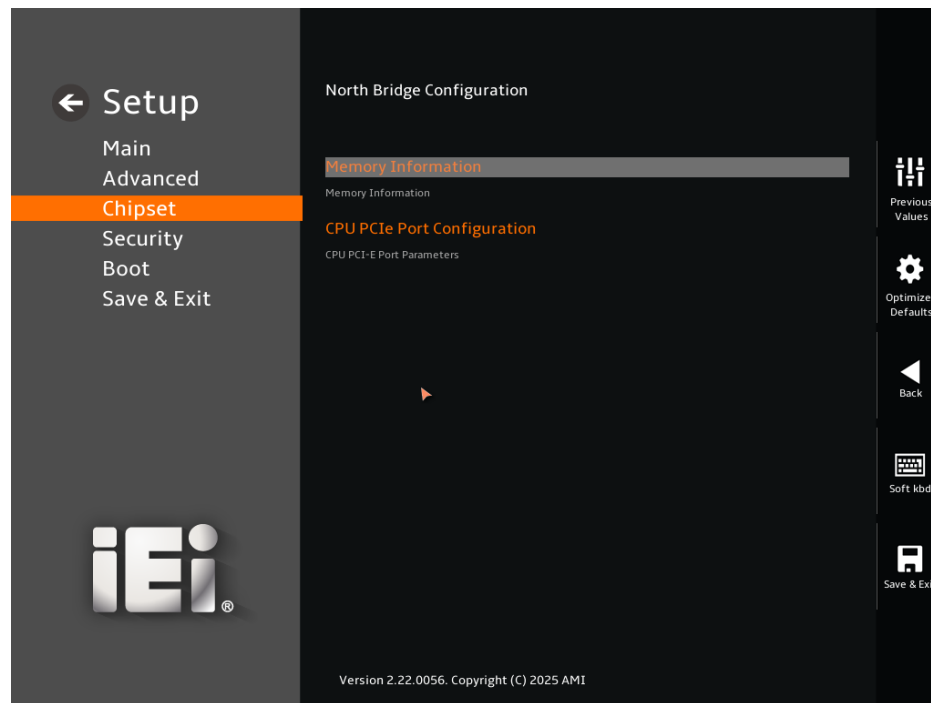
➔ USB Power [+5VDUAL]

Use the **USB Power** option to enable or disable the USB Power.

- ➔ **+5VDUAL** **DEFAULT** USB Power is on.
- ➔ **+5V** USB Power is off.

5.4.2 Nouth Bridge

Use the **Nouth Bridge** menu (**BIOS Menu 29**) to configure the parameters.

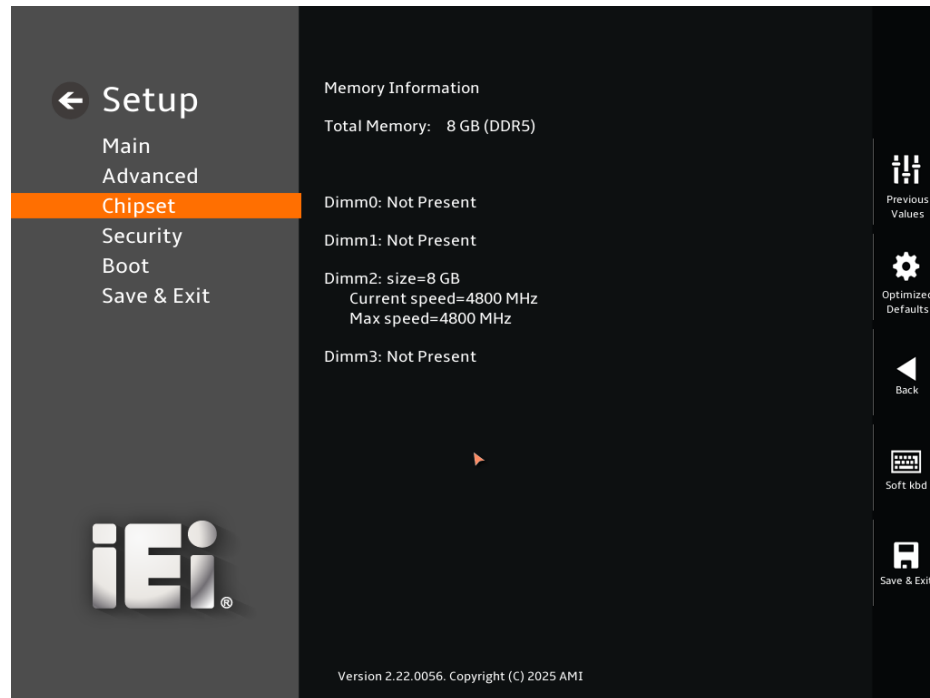


BIOS Menu 29: Nouth Bridge

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5.4.2.1 Memory Information

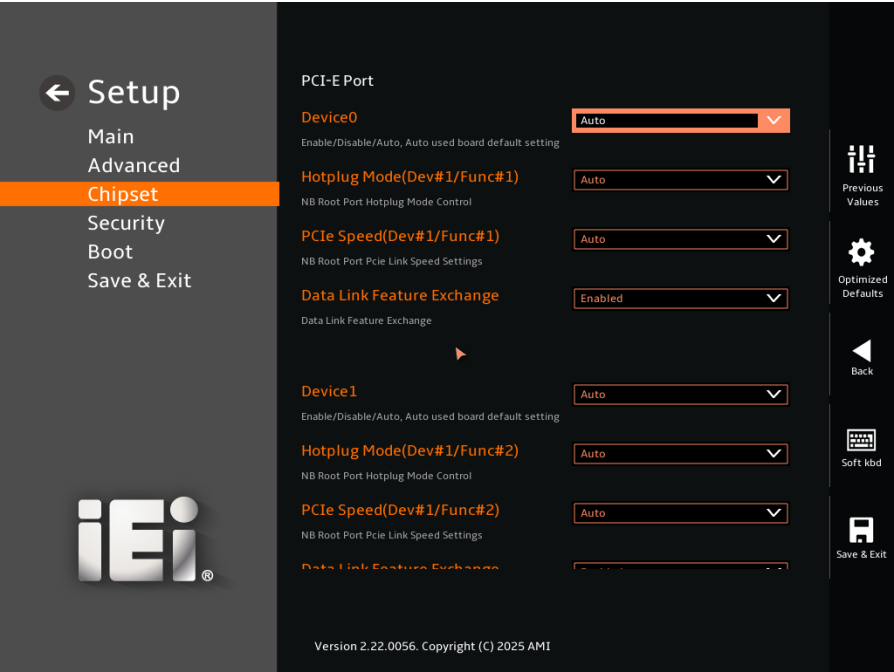
Use the **Memory Configuration** submenu (**BIOS Menu 30**) to view memory information.



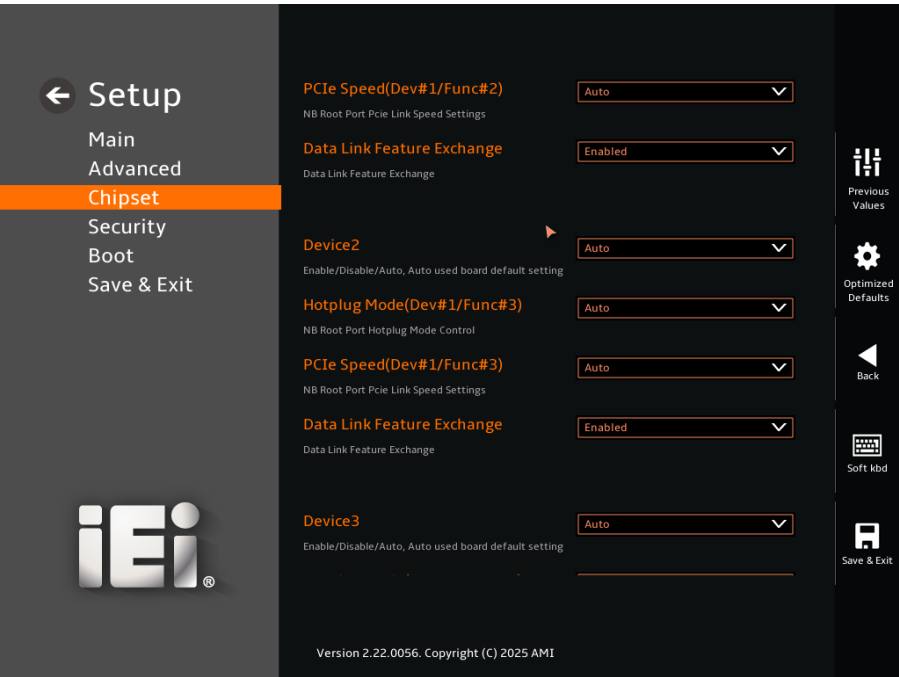
BIOS Menu 30: Memory Configuration

5.4.2.2 CPU PCIe Port Configuration

Use the **CPU PCIe Port Configuration (BIOS Menu 31)** menu to configure the PCIe Port.

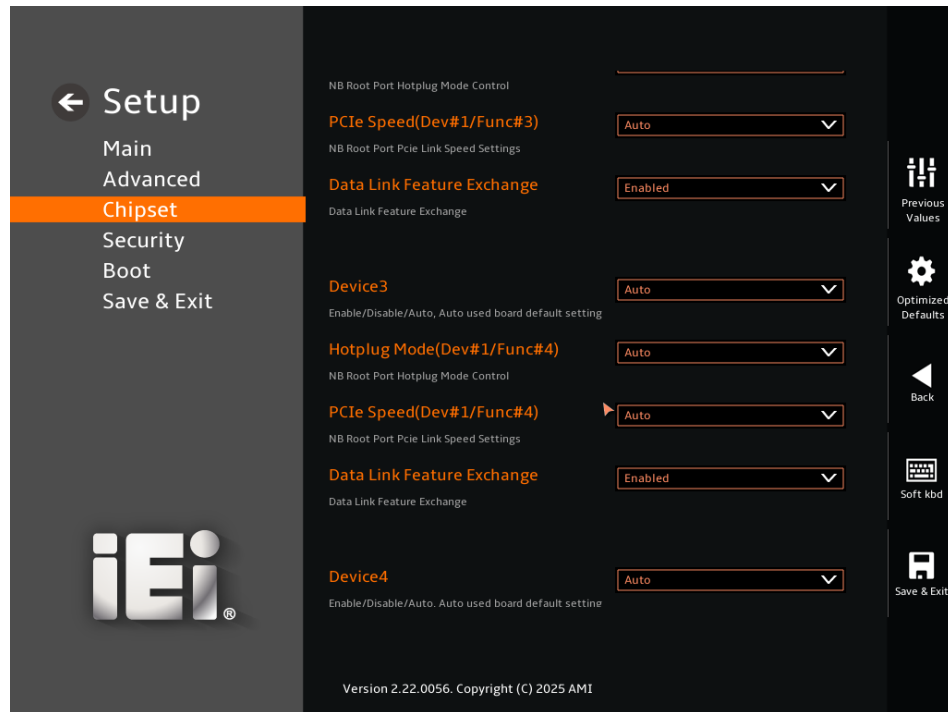


BIOS Menu 31: CPU PCIe Port Configuration (1/6)

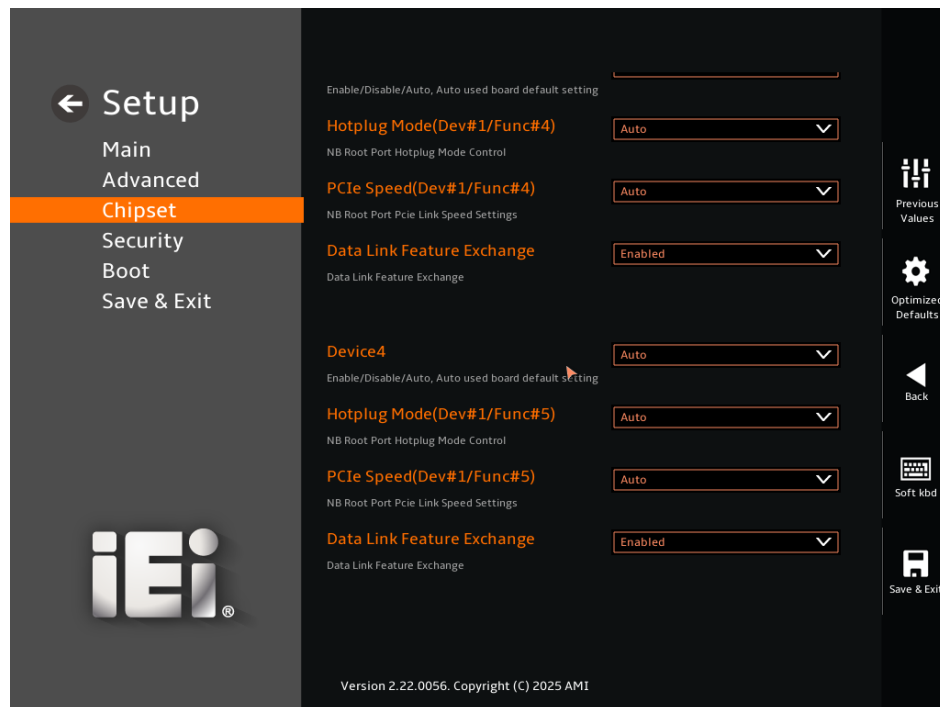


BIOS Menu 32: CPU PCIe Port Configuration (2/6)

PCIE-AM5



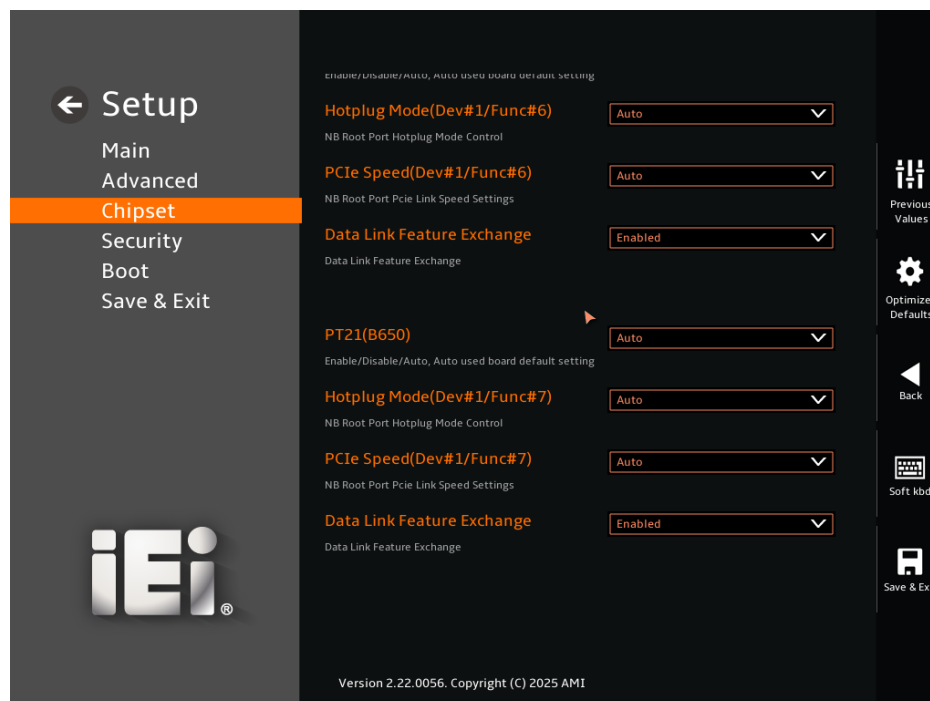
BIOS Menu 33: CPU PCIe Port Configuration (3/6)



BIOS Menu 34: CPU PCIe Port Configuration (4/6)



BIOS Menu 35: CPU PCIe Port Configuration (5/6)



BIOS Menu 36: CPU PCIe Port Configuration (6/6)

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→ **Device1 [Auto]**

Use the **Device1** option to configure the board setting.

- **Auto** **DEFAULT** The board setting is auto.
- **Disabled** The board setting is disabled.
- **Enable** The board setting is enabled.

→ **Hotplug Mode [Auto]**

Use the **Hotplug Mode** option to configure the Hotplug Mode.

- **Auto** **DEFAULT** Automatically selects the suitable hotplug mode
- **Hotplug Inboard** Enables basic hotplug support
- **Hotplug Enhanced** Provides extended hotplug functions
- **Hotplug Server** Enables server-grade hotplug control
- **Hotplug Basic** Enables standard PCIe hotplug
- **Disabled** Disables PCIe hotplug function

→ **PCIe Speed [Auto]**

Use the **PCIe Speed** option to configure the PCIe generation.

- **Auto** **DEFAULT** Automatically selects the highest PCIe generation
- **Gen1** PCIe operate at PCIe Gen1
- **Gen2** PCIe operate at PCIe Gen2
- **Gen3** PCIe operate at PCIe Gen3
- **Gen4** PCIe operate at PCIe Gen4

→ **Data Link Feature Exchange [Enabled]**

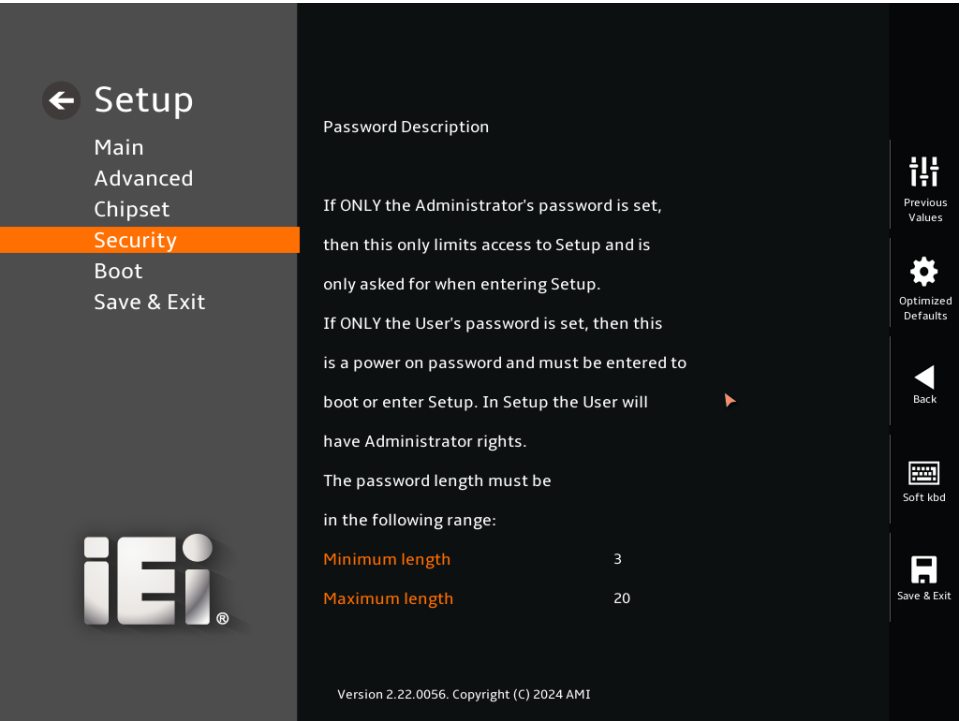
Use the **Data Link Feature Exchange** option to enable or disable the Data Link Feature Exchange.

- **Enabled** **DEFAULT** Enables PCIe link to exchange
- **Disabled** Disables PCIe link to exchange



5.5 Security

Use the **Security** menu (**BIOS Menu 37**) to set system and user passwords.



BIOS Menu 37: Security (1/2)



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BIOS Menu 38: Security (2/2)

➔ Administrator Password

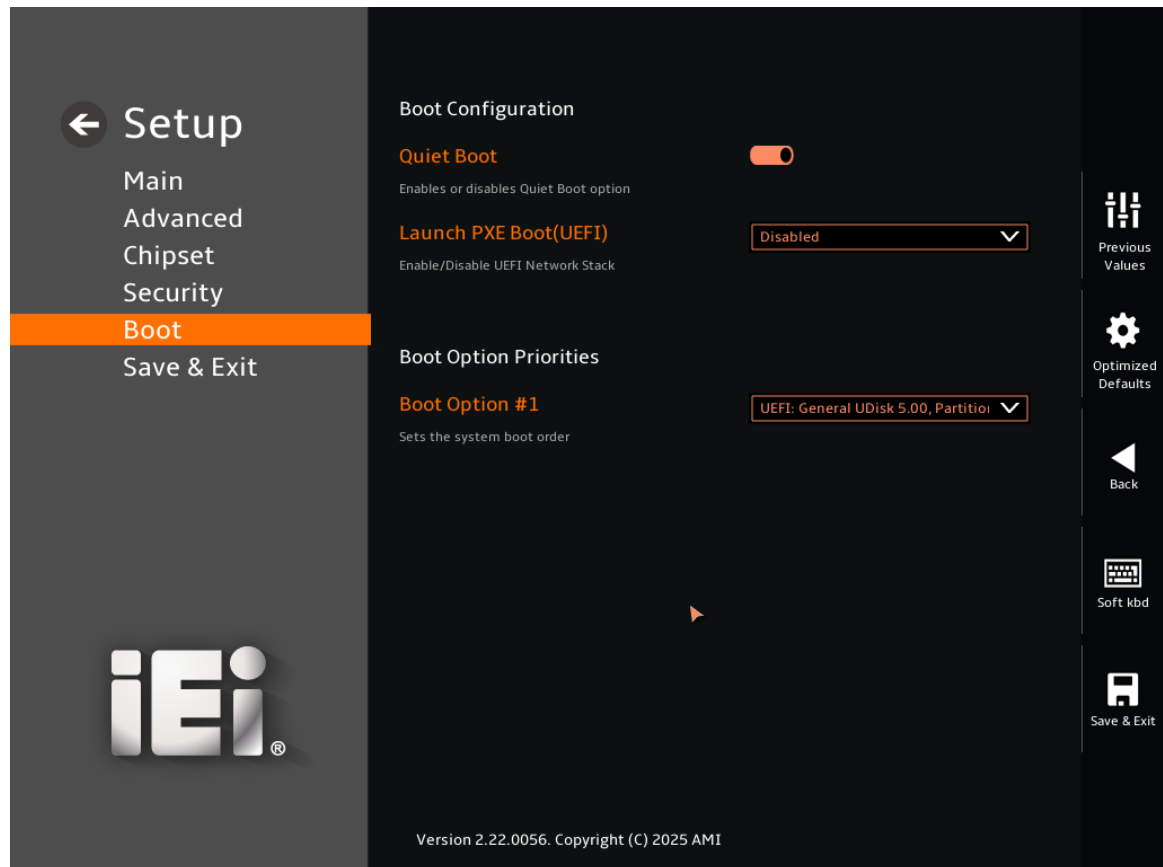
Use the **Administrator Password** to set or change an administrator password.

➔ User Password

Use the **User Password** to set or change a user password.

5.6 Boot

Use the **Boot** menu (**BIOS Menu 39**) to configure system boot options.



BIOS Menu 39: Boot

5.6.1 Boot Configuration

→ Quiet Boot [Enabled]

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

- | | | | |
|---|-----------------|----------------|---|
| → | Disabled | | Normal POST messages displayed |
| → | Enabled | DEFAULT | OEM Logo displayed instead of POST messages |

PCIE-AM5

→ Launch PXE OpROM [Disabled]

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

- **Disabled** **DEFAULT** Ignore all PXE Option ROMs
- **Enabled** Load PXE Option ROMs.

→ Option ROM Messages [Force BIOS]

Use the **Option ROM Messages** option to set the Option ROM display mode.

- **Force BIOS** **DEFAULT** Sets display mode to force BIOS.
- **Keep Current** Sets display mode to current.

5.6.2 Boot Option Priorities

Use the Boot Option # N to choose the system boots from the peripherals you selected. The following Boot Options are listed as an example.

→ Boot Option #1

Sets the system boot order **ADATA SP580** as the first priority.

- **Windows Boot Manager (P1: ADATA SSD SP580 240GB)**
- **Disabled**

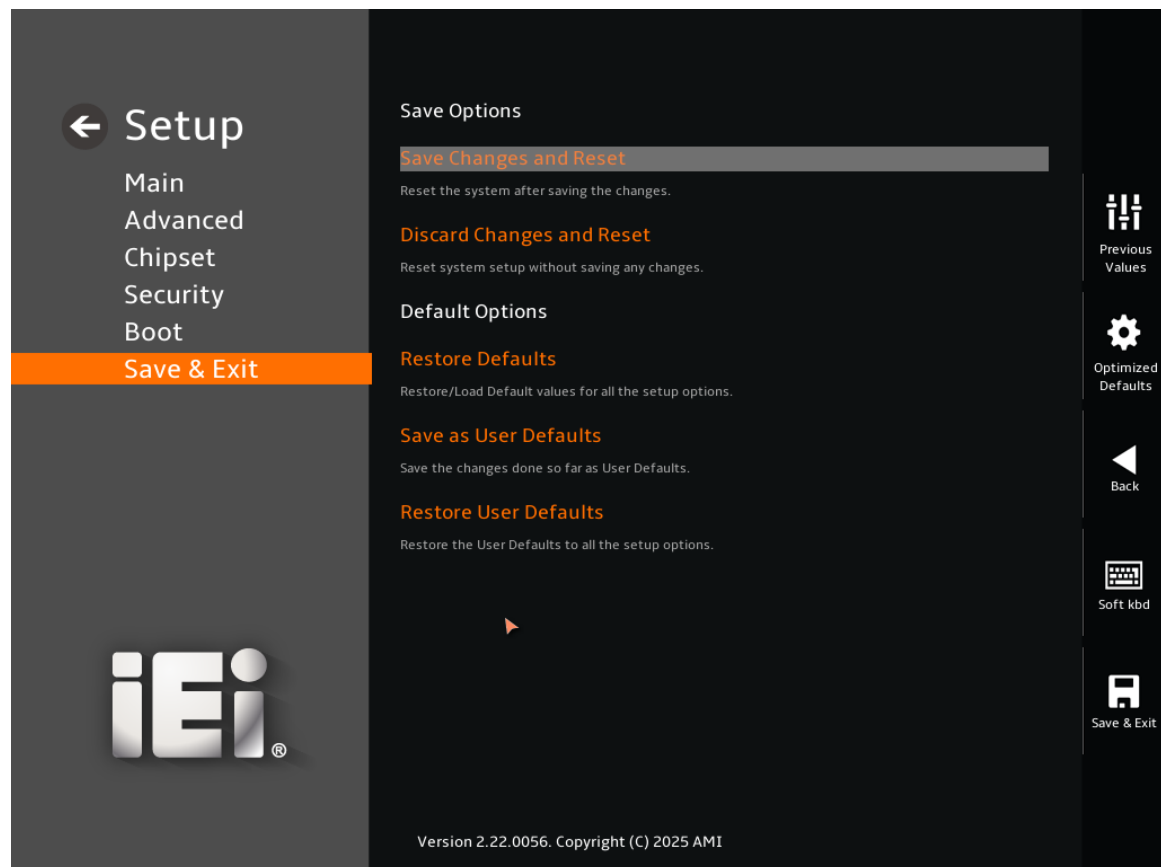
→ Boot Option #2

Sets the system boot order **USB Partition 1** as the second priority.

- **UEFI: USB, Partition 1**
- **Disabled**

5.7 Save & Exit

Use the **Save & Exit** menu (**BIOS Menu 40**) to load default BIOS values, optimal failsafe values and to save configuration changes.



BIOS Menu 40: Save & Exit

➔ Save Changes and Reset

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and reset the system.

➔ Discard Changes and Reset

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

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➔ Restore Defaults

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

➔ Save as User Defaults

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

➔ Restore User Defaults

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Appendix

A

Regulatory Compliance

DECLARATION OF CONFORMITY

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

FCC WARNING

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

Product Disposal

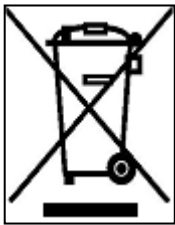
PCIE-AM5

**CAUTION:**

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- Outside the European Union—If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the correct disposal method.
- Within the European Union—The device that produces less waste and is easier to recycle is classified as electronic device in terms of the European Directive 2012/19/EU (WEEE), and must not be disposed of as domestic garbage.



EU-wide legislation, as implemented in each Member State, requires that waste electrical and electronic products carrying the mark (left) must be disposed of separately from normal household waste. This includes monitors and electrical accessories, such as signal cables or power cords. When you need to dispose of your device, please follow the guidance of your local authority, or ask the shop where you purchased the product. The mark on electrical and electronic products only applies to the current European Union Member States.

Please follow the national guidelines for electrical and electronic product disposal.

Appendix

C

BIOS Options

PCIE-AM5

Below is a list of BIOS configuration options in the BIOS chapter.

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Appendix

D

Watchdog Timer



NOTE:

The following discussion applies to DOS environment. Contact IEI support or visit the IEI website for specific drivers for other operating systems.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMIs or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer’s period.
BL:	Time-out value (Its unit-second is dependent on the item “Watchdog Timer unit select” in CMOS setup).

Table D-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

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**NOTE:**

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

EXAMPLE PROGRAM:

; INITIAL TIMER PERIOD COUNTER

;

W_LOOP:

;

```

MOV      AX, 6F02H      ;setting the time-out value
MOV      BL, 30          ;time-out value is 48 seconds
INT      15H

```

;

; ADD THE APPLICATION PROGRAM HERE

;

```

CMP      EXIT_AP, 1      ;is the application over?
JNE      W_LOOP          ;No, restart the application

MOV      AX, 6F02H      ;disable Watchdog Timer
MOV      BL, 0           ;
INT      15H

```

;

; EXIT ;

Appendix

E

Error Beep Code

PCIE-AM5**E.1 PEI Beep Codes**

Number of Beeps	Description
4	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXE IPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

E.2 DXE Beep Codes

Number of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

**NOTE:**

If you have any question, please contact IEI for further assistance.

Appendix

F

Hazardous Materials Disclosure

PCIE-AM5

F.1 RoHS Directive (2015/863/EU)

The details provided in this appendix are to ensure that the product is compliant with the RoHS Directive (2015/863/EU). The table below acknowledges the presences of small quantities of certain substances in the product, and is applicable to RoHS Directive (2015/863/EU).

Please refer to the following table.

Part Name	Toxic or Hazardous Substances and Elements									
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)	Bis(2-ethylhexyl) phthalate (DEHP)	Butyl benzyl phthalate (BBP)	Dibutyl phthalate (DBP)	Diisobutyl phthalate (DIBP)
Housing	O	O	O	O	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O	O	O	O	O
Battery	O	O	O	O	O	O	O	O	O	O
O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in Directive (EU) 2015/863. X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in Directive (EU) 2015/863.										



F.2 China RoHS

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有“环境友好使用期限”的标签，此期限是估算这些物质“不会有泄漏或突变”的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	O	O	O	O	O	O
印刷电路板	O	O	O	O	O	O
金属螺帽	O	O	O	O	O	O
电缆组装	O	O	O	O	O	O
风扇组装	O	O	O	O	O	O
电力供应组装	O	O	O	O	O	O
电池	O	O	O	O	O	O
O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求以下。 X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求。						

