

AIMB-219 B1

**Mini-ITX Motherboard
Intel® Core™ i3 and Core™ 3
Processor
Intel Atom® x7000E/x7000RE
Processor
(Twin Lake/Amston Lake/Alder
Lake-N)**

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- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

Initial Inspection

Before installing the motherboard, please ensure that the following items are included in your shipment:

- 1 x AIMB-219 B1 Mini-ITX motherboard
- 1 x SATA HDD cable
- 1 x SATA power cable
- 1 x Serial port cable
- 1 x I/O port bracket
- 1 x Startup Manual
- 1 x Warranty Card
- 1 x Onboard CPU heatsink

If any of these items are missing or damaged, contact your distributor or sales representative immediately. All AIMB-219 B1 devices are mechanically and electrically inspected before shipment. Thus, your product should be free of marks and scratches and in perfect working order upon receipt. While unpacking AIMB-219 B1, check the product for signs of shipping damage (for example, a damaged box, scratches, dents, etc.). If the device is damaged or fails to meet the specifications, notify our service department or your local sales representative immediately. Please also notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After this inspection, we will make arrangements to repair or replace the unit.

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Chapter 1

General Information

1.1 Introduction

The AIMB-219 B1 with Intel® Core™ i3 and Core™ 3 and Atom® x7000E/x7000RE Processor is designed for industrial applications that require enhanced computing performance and power management capabilities. The motherboard features an onboard Intel® Core™ i3 and Core™ 3 and Atom® x7000E/x7000RE Processor with DDR5 4800 MT/s up to 16GB. The AIMB-219 B1 offers rich I/O connectivity with one USB 3.2 Gen2 x1 Type-C, three USB 3.2 Gen2 x1, and five USB 2.0 ports, as well as 6 x COM ports integrated in a standard 170 x 170 mm form factor. The system also supports triple independent displays for HDMI, DP, LVDS (or eDP). AIMB-219 B1 also features numerous connectivity and expansion options, including PCIe x1 Gen3, 8-bit GPIO, SATA III 6GB/s connectors, an optional TPM security feature, and two M.2 (E-Key for 2230 type, B-Key for 2242/3042/2280 type) expansion slots for easy integration. A dual Realtek chipset and 10/100/1000/2500 Mbps Ethernet port are also provided to deliver high-speed networking. Intel® UHD Graphics engines provide extremely high display resolution. All the features described above are incorporated into a space-saving, power-efficient, and cost-effective Mini-ITX form factor.

1.2 Features

- **I/O Expansion:** 6 x serial ports, 3 x USB 3.2 Gen2 x1, 5 x USB 2.0, 1 x USB 3.2 Gen2 x1 Type-C, 2 x SATA III, 1 x M.2 B-Key, 1 x M.2 E-Key, 2 x GbE LAN (co-lay 2.5GbE).
- **Standard Mini-ITX form factor with industrial features:** The AIMB-219 B1 is a full-featured Mini-ITX motherboard with balanced expandability and performance.

1.3 Specifications

1.3.1 System

- **CPU:** Supports Intel® Core™ i3 and Core™ 3 and Atom® x7000E/x7000RE Processor (up to 15W)
- **BIOS:** AMI EFI 256 Mbit SPI BIOS.
- **Storage interface:** One onboard Serial ATA III connector with a data transmission rate of up to 6GB/s supporting Advanced Host Controller Interface (AHCI) technology. One M.2 (B-Key) supports SSD/LTE and M.2 (E-Key) for wireless modules.

1.3.2 Memory

- **RAM:** 1 x 262-pin SODIMM socket supporting one-channel DDR5 4800 MT/s SODIMM, up to 16GB

1.3.3 Input/Output

- **Serial ports:** 6 x serial ports; COM1 and COM2 support RS-232 by default; COM3 supports RS-232/422/485 (BOM option), auto flow control by BIOS; COM4 supports RS-232 by default, CCtalk by BOM option; COM5 supports RS-232 by default, TTL by BOM option; COM6 supports RS-232 by default, Ring-in 5V/12V is selected by jumper.
- **USB port:** Supports up to 3 x USB 3.2 Gen2 x1, 5 x USB 2.0, and 1 x USB 3.2 Gen2 x1 Type-C.
- **GPIO connector:** 8-bit general purpose Input/Output.

1.3.4 Graphics

- **Controller:** Intel® UHD Graphics
- **eDP:** Supports max. resolution 4096 x 2304 @ 60Hz.
- **DP:** Supports max. resolution 4096 x 2304 @ 60Hz (via USB Type-C)
- **HDMI:** Supports max. resolution 4K x 2K @ 60Hz.
- **LVDS (default):** Supports 1 x LVDS maximum resolution up to 1920 x 1200 @ 60 Hz (eDP co-design with LVDS)

1.3.5 Ethernet LAN

- Supports dual 10/100/1000/2500 Mbps Ethernet port(s)
- **Controller:**
 - GbE LAN1: RTL8111K (1GbE) co-lay RTL8125BG (2.5GbE)
 - GbE LAN2: RTL8111K (1GbE) co-lay RTL8125BG (2.5GbE)

1.3.6 Industrial Features

- **Watchdog timer:** Generates a system reset and is programmable with each unit equal to one second or one minute (255 levels).

1.3.7 Mechanical and Environmental Specifications

- **Operating temperature:** 0 ~ 60°C (32 ~ 140°F), depending on CPU speed and cooler solution
- **Storage temperature:** -40 ~ 85°C (-40 ~ 185°F)
- **Humidity:** 5 ~ 95% non-condensing
- **Power supply voltage:** 12V DC-in
- **Power consumption:** Boost 43.1W; Typical 21.2W (configuration: Intel® Core™ 3 N355, 1pcs 16GB DDR5 4800 MT/s SODIMM)
- **Board size:** 170 x 170 mm (6.69" x 6.69")
- **Board weight:** 0.365 kg

1.4 Jumpers and Connectors

Connectors on the AIMB-219 B1 motherboard link it to devices such as hard disk drives and a keyboard. In addition, the board has a number of jumpers used to configure the system for your application.

The tables below list the function of each of the board jumpers and connectors. Later sections in this chapter give instructions on setting jumpers. Chapter 2 gives instructions for connecting external devices to your motherboard.

Table 1.1: I/O Connector

	Description	Part Reference
1	USB Type-C Connector	USBC1
2	HDMI Connector	HDMI1
3	RJ-45 Dual LAN ports	LAN1_LAN2
4	USB 3.1 Stack Connector * 2 Ports	USB12
5	Internal USB 3.1 Vertical Connector	USB8
6	M.2 E-Key Connector	M2_E1
7	M.2 B-Key Connector	M2_B1
8	SIM Card Connector	SIM1
9	DDR5 SODIMM Socket	DIMMA1
10	12V Power Supply Connector	DCIN1
11	SATA Connector	SATA1
12	PCIe x1 Connector	PCIEX1_1
13	HD Analog Audio Interface Line-Out	AUDIO1
14	HD Analog Audio Interface Mic-In	AUDIO2
15	RJ-45 Single LAN port	LAN1

Table 1.2: Box Header

	Description	Part Reference
1	EDP Connector / LVDS Connector	EDP1_LVDS1
2	Internal USB 2.0 Connector * 2 Ports	USB34
3	Internal USB 2.0 Connector * 2 Ports	USB56
4	Internal USB 2.0 Connector * 1 Port	USB7
5	COM1 Connector	COM1
6	COM2 Connector	COM2
7	COM3 Connector	COM3
8	COM4 Connector	COM4
9	COM5 Connector	COM5
10	COM6 Connector	COM6
11	CMOS Battery Connector	BAT1
12	EDP/LVDS Backlight Inverter Power Connector	INV1
13	ATX 4-Pin Power Connector (180D)	ATX12V1
14	ATX 5V/PSON Connector	ATX_5VSB1
15	SATA Power Connector	SATA_PWR1

Table 1.3: Pin Header

	Description	Part Reference
1	Power LED Pin Header	JFP2
2	SPI BIOS Flash Socket 1	SPI1
3	SPI BIOS Debug Header	SPI_CN1
4	8-bit General Purpose I/O Pin Header	GPIO1
5	CPU FAN Connector	CPUFAN1
6	System Fan Connector	SYSFAN1
7	Case Open Connector	JCASE1
8	Programming Header	VR_PMB1
9	HD Digital Audio Interface S/PDIF Out	SPDIF1
10	Audio Amplifier Output Pin Header	AMP1
11	HD Analog Audio Interface Front Panel	FPAUD1
12	LED Port 80 Connector	LED_P80

Table 1.4: Jumper Settings

	Description	Part Reference
1	COM6 RI# Selection Pin Header	JSETCOM6_V1
2	COM4 CCTALK Voltage Select Header	JCCT_VCON1
3	Watchdog Timer Output and OBS Beep	JWDT1+JOBS1
4	EDP Panel/LVDS Panel Voltage Selection	JEDP1_LVDS1
5	PWRBTN#/RESET#/HDD LED/Serial Bus from HW Monitor IC/Internal Buzzer/External Speaker Header	JFP1
6	Case Open Signal Reverse Header	JCASEOP_SW1
7	CMOS Reset Header	JCMOS1
8	AT/ATX Mode Selection	PSON1
9	VESA & JEIDA Support Select	SW_LVDS_VCON1

1.5 Board Layout: Jumper and Connector Locations

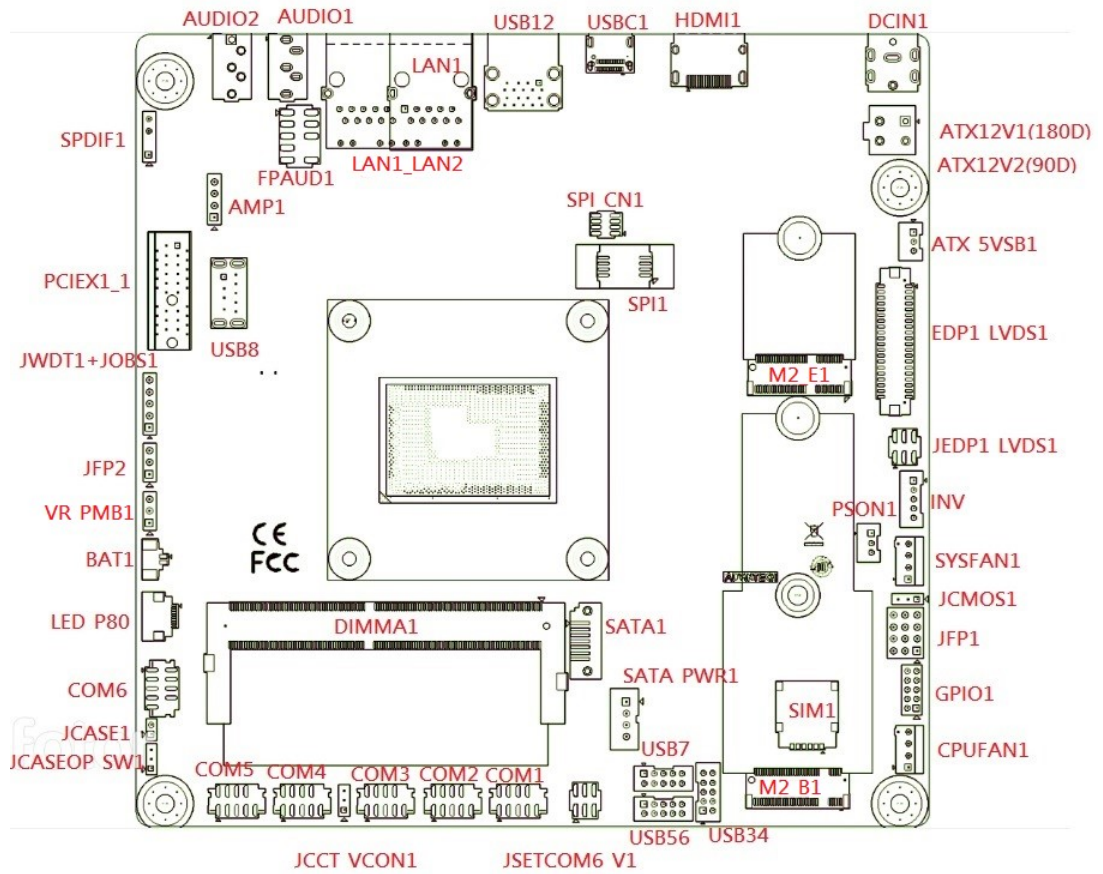


Figure 1.1 Jumper and Connector Locations (Top Side)

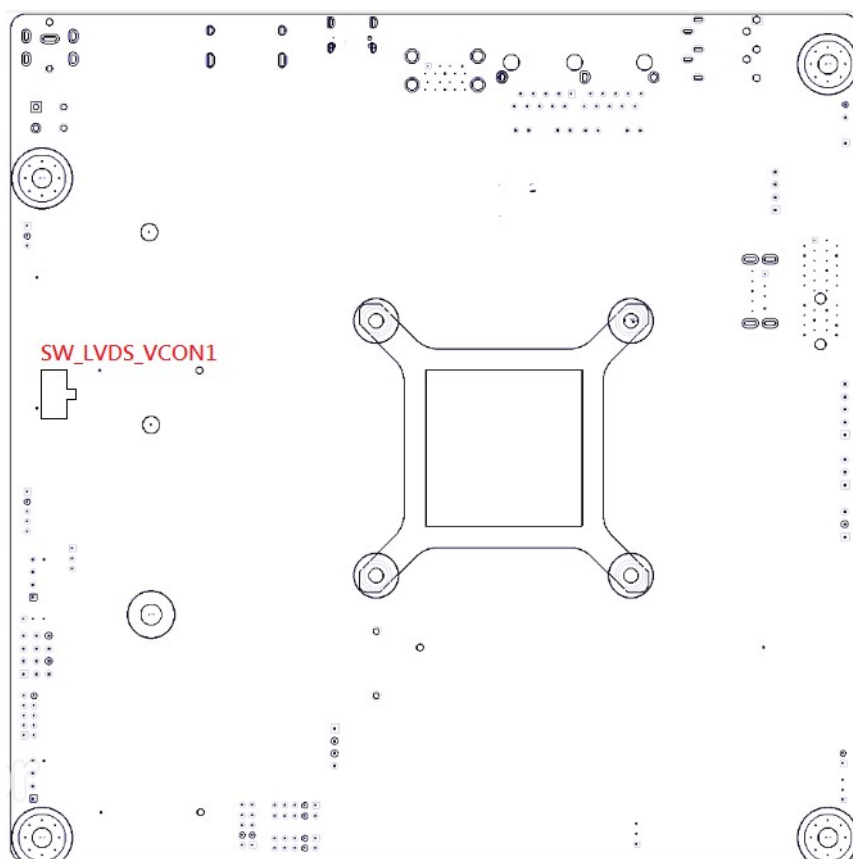


Figure 1.2 Jumper and Connector Locations (Bottom Side)

1.6 AIMB-219 B1 Board Diagram

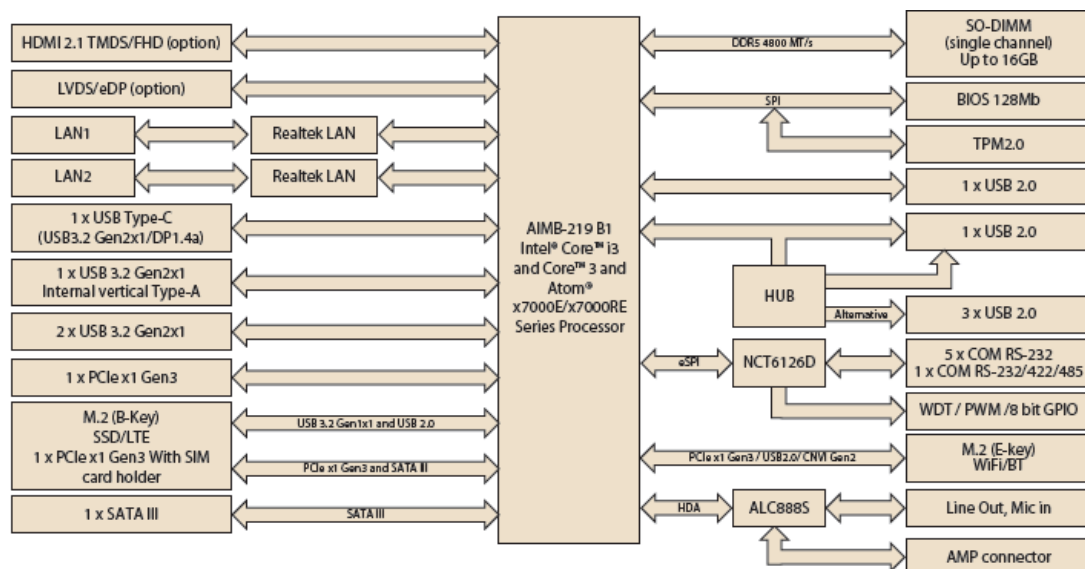


Figure 1.3 AIMB-219 B1 Board Diagram

1.7 Safety Precautions

Warning! *Always completely disconnect the power cord from the chassis when working with the hardware. Do not connect devices while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.*



Caution! *Always ground yourself to remove any static charge before touching the motherboard. Modern electronic devices are very sensitive to electrostatic discharges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when not in the chassis.*



Caution! *The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*



Caution! *There is danger of a new battery exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*



1.8 Jumper Options

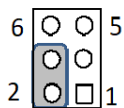
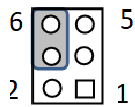
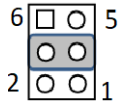
This section provides instructions on how to configure your motherboard by setting the jumpers. It also includes the motherboard's default settings and your options for each jumper.

1.8.1 Setting Jumpers

You can configure your motherboard to match the needs of your application by setting the jumpers. A jumper is a metal bridge that closes an electrical circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” (or turn ON) a jumper, you connect the pins with the clip. To “open” (or turn OFF) a jumper, you remove the clip. Sometimes a jumper consists of a set of three pins, labeled 1, 2, and 3. In this case you connect either pins 1 and 2, or 2 and 3. A pair of needle-nose pliers may be useful when setting jumpers.

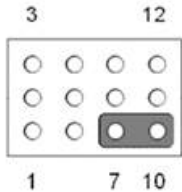
1.8.2 EDP Panel/LVDS Panel Voltage Selection (JEDP1_LVDS1)

Table 1.5: JEDP1_LVDS1

Function	Jumper Setting
Jumper position for 5V	
Jumper position for 3.3V (default)	
Jumper position for 12V	

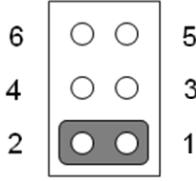
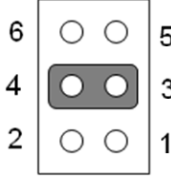
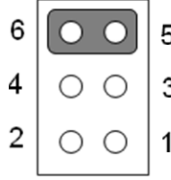
1.8.3 PWRBTN#/RESET#/HDD LED/Internal Buzzer/External Speaker Header (JFP1)

Table 1.6: JFP1

Function	Jumper Setting
Internal buzzer (default)	

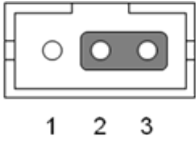
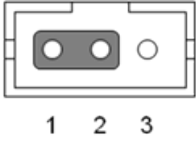
1.8.4 COM6_RI# Pin RI#/5V/12V Selection (JSETCOM6_V1)

Table 1.7: JSETCOM6_V1

Function	Jumper Setting
Jumper position for RI# (default)	
Jumper position for +5V	
Jumper position for +12V	

1.8.5 AT/ATX Mode Selection (PSON1)

Table 1.8: PSON1

Function	Jumper Setting
ATX Mode (default) PSON1(2-3)	
AT Mode PSON1(1-2)	

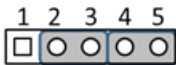
1.8.6 Case Open State (NC/NO) Pin Header (JCASEOP_SW1)

Table 1.9: JCASEOP_SW1

Function	Jumper Setting
N.C. (Normal Close) (default) JCASEOP_SW1(2-3)	

1.8.7 Watchdog Output and OBS Beep (JWDT1+JOBS1)

Table 1.10: JWDT1+JOBS1

Function	Jumper Setting
Watchdog Timer Output (2-3) (Default) OBS BEEP (4-5) (Default)	 (4 and 6)+(8 and 9)
Watchdog Timer Disable (1-2) OBS BEEP (4-5) (Default)	 (1 and 2)+(8 and 9)

1.8.8 CMOS Clear Jumper (JCMOS1)

Table 1.11: JCMOS1

Function	Jumper Setting
Normal (default) JCMOS1(1-2)	
Clear CMOS JCMOS1(2-3)	

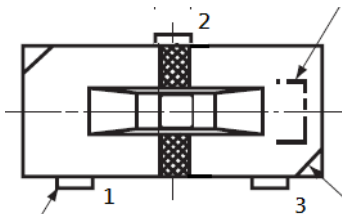
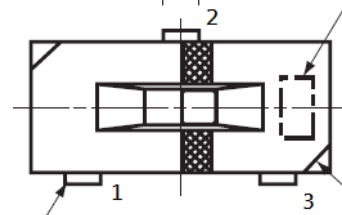
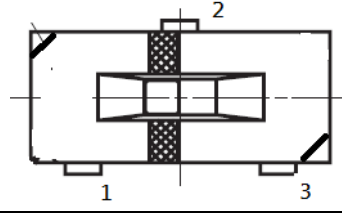
1.8.9 COM4 CCTALK Voltage Select Header (JCCT_VCON1)

Table 1.12: JCCT_VCON1

Function	Jumper Setting
+V12 (default) JCCT_VCON1 (1-2)	
+V5 JCCT_VCON1 (2-3)	

1.8.10 VESA & JEIDA Support Select (SW_LVDS_VCON1)

Table 1.13: SW_LVDS_VCON1

Function	Jumper Setting
OPEN (default) SW_LVDS_VCON1 (2) SW Switch Center	
GND SW_LVDS_VCON1 (2-3) SW Switch Right	
100 ohm pull high +V3.3 SW_LVDS_VCON1 (1-2) SW Switch Left	

1.9 System Memory

AIMB-219 B1 features a single socket designed for a 262-pin DDR5 SODIMM. This socket uses a 1.2V unbuffered double data rate synchronous DRAM (DDR SDRAM) module. DRAM is available in capacities of 4GB, 8GB and 16GB. The socket can be filled using SODIMM of any size, giving a total memory size of 4GB, 8GB, up to a max of 16GB. AIMB-219 B1 does NOT support error checking and correction (ECC).

1.10 Memory Installation Procedures

To install the SODIMM, first make sure the two handles of the SODIMM socket are in the “open” position, i.e., the handles lean outward. Slowly slide the SODIMM module along the plastic guides on both ends of the socket. Then firmly but gently (avoid pushing down too hard) press the SODIMM module well down into the socket, until you hear a click when the two handles have automatically locked the memory module into the correct position of the SODIMM socket. To remove the memory module, just push both handles outward, and the memory module will be ejected by the mechanism.

1.11 Cache Memory

The AIMB-219 B1 supports a CPU with one of the following built-in full-speed last-level caches:

6MB for Intel® Core™ i3, Core™ 3 Processor and Atom® x7000E/x7000RE Processor.

The built-in second-level cache in the processor yields much higher performance than conventional external cache memory.

1.12 Processor Installation

The AIMB-219 B1 is designed to support Intel® Core™ i3, Core™ 3 Processor and Atom® x7000E/x7000RE Processor.

Chapter 2

Connecting
Peripherals

2.1 Introduction

You can access most of the connectors from the top of the board as it is being installed in the chassis. If you have a number of cards installed or have a packed chassis, you may need to partially remove the card to make all the connections.

2.2 I/O Connector

2.2.1 USB Type-C Connector (USBC1)

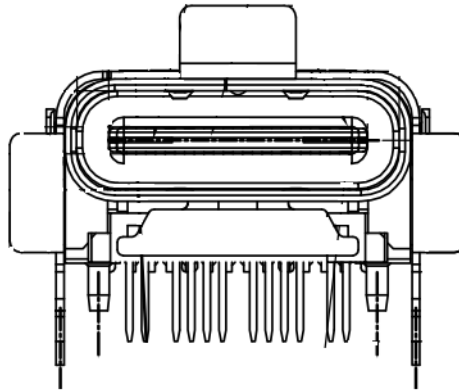


Table 2.1: USB Type-C Connector (USBC1)

Pin	Signal	Pin	Signal
A1	GND1	B1	GND3
A2	SSTXP1_1	B2	SSTXP2_2
A3	SSTXN1_1	B3	SSTXN2_2
A4	VUSB_1	B4	VUSB_3
A5	CC1	B5	CC2
A6	DP1	B6	DP2
A7	DN1	B7	DN2
A8	SBU1	B8	SBU2
A9	VUSB_2	B9	VUSB_4
A10	SSRXN2_1	B10	SSRXN1_2
A11	SSRXP2_1	B11	SSRXP1_2
A12	GND2	B12	GND4

2.2.2 HDMI Connector (HDMI1)

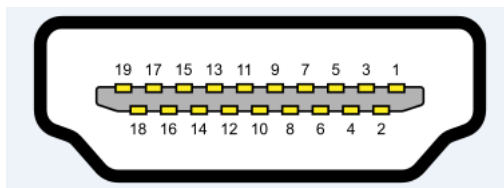


Table 2.2: HDMI Connector (HDMI1)

Pin	Signal	Pin	Signal
1	TMDS Data2+	2	GND
3	TMDS Data2-	4	TMDS Data1+
5	GND	6	TMDS Data1-
7	TMDS Data0+	8	GND
9	TMDS Data0-	10	TMDS Clock+
11	GND	12	TMDS Clock-
13	NC	14	NC
15	SCL	16	SDA
17	GND	18	+5V Power
19	Hot Plug Detect		

2.2.3 RJ-45 Dual LAN Ports (LAN1_LAN2)

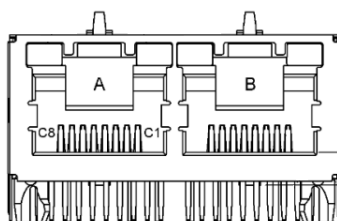


Table 2.3: RJ-45 Dual LAN Ports (LAN1_LAN2)

Pin	Signal	Pin	Signal
AL1	LAN1_LED1_ACT#_R	BL1	LAN2_LED1_ACT#_R
AL2	+V3.3_DUAL	BL2	+V3.3_DUAL
AL3	LAN1_LED2_1G#_R	BL3	LAN2_LED2_1G#_R
AL4	LAN1_LED0_100M#_R	BL4	LAN2_LED0_100M#_R
AR6	LAN1_CT	BR6	LAN2_CT
AR5	LAN1_CONN	BR5	LAN2_CONN
AR1	LAN1_MDI0+	BR1	LAN2_MDI0+
AR2	LAN1_MDI0-	BR2	LAN2_MDI0-
AR3	LAN1_MDI1+	BR3	LAN2_MDI1+
AR4	LAN1_MDI1-	BR4	LAN2_MDI1-
AR7	LAN1_MDI2+	BR7	LAN2_MDI2+
AR8	LAN1_MDI2-	BR8	LAN2_MDI2-
AR9	LAN1_MDI3+	BR9	LAN2_MDI3+
AR10	LAN1_MDI3-	BR10	LAN2_MDI3-
H3	GND	H4	GND

2.2.4 USB 3.1 Stack Connector * 2 Ports (USB12)

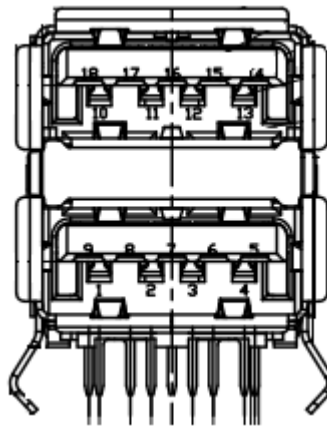


Table 2.4: USB 3.1 Stack Connector * 2 Ports (USB12)

Pin	Signal	Pin	Signal
1	+5V	10	+5V
2	USB2_D0-	11	USB2_D1-
3	USB2_D0+	12	USB2_D1+
4	GND	13	GND
5	USB31_P0_z_RX-	14	USB31_P1_z_RX-
6	USB31_P0_z_RX+	15	USB31_P1_z_RX+
7	GND	16	GND
8	USB31_P0_z_TX-	17	USB31_P1_z_TX-
9	USB31_P0_z_TX+	18	USB31_P1_z_TX+

2.2.5 Internal USB 3.1 Vertical Connector (USB8)

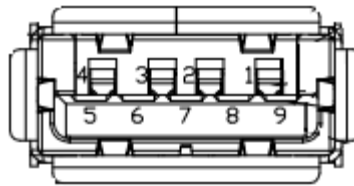


Table 2.5: Internal USB 3.1 Vertical Connector (USB8)

Pin	Signal
1	+5V
2	USB2_D0-
3	USB2_D0+
4	GND
5	USB31_P0_z_RX-
6	USB31_P0_z_RX+
7	GND
8	USB31_P0_z_TX-
9	USB31_P0_z_TX+

2.2.6 M.2 E-Key Connector (M2_E1)

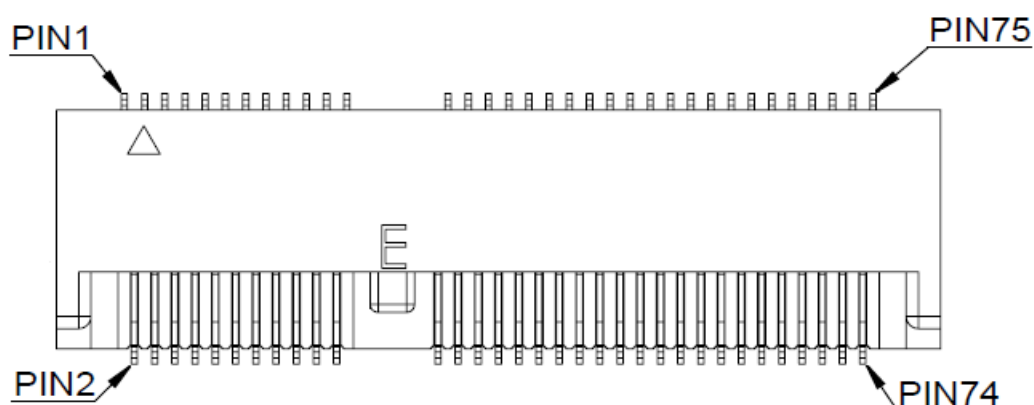


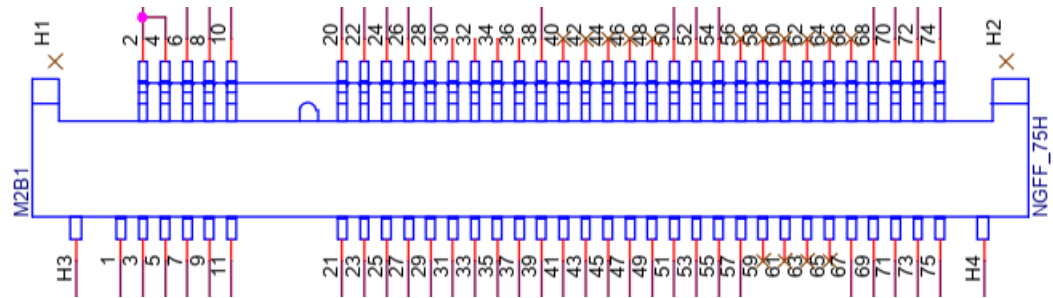
Table 2.6: M.2 E-Key Connector (M2_E1)

Pin	Signal	Pin	Signal
1	GND	2	+3.3V
3	USB_D+	4	+3.3V
5	USB_D-	6	WLAN_LED1#
7	GND	8	BT_PCMCLK
9	CNV_WR_D1-	10	BT_PCMFRM
11	CNV_WR_D1+	12	BT_PCMIN
13	GND	14	BT_PCMOUT
15	CNV_WR_D0-	16	BT_LED#
17	CNV_WR_D0+	18	GND
19	GND	20	UART_WAKE#
21	CNV_WR_CLK-	22	CNV_BRI_RSP
23	CNV_WR_CLK+	24	Connector Key
25	Connector Key	26	Connector Key
27	Connector Key	28	Connector Key
29	Connector Key	30	Connector Key
31	Connector Key	32	CNV_RGI_DT_R
33	GND	34	CNV_RGI_RSP
35	PETp0	36	CNV_BRI_DT_R
37	PETn0	38	CL_RST#
39	GND	40	CL_DAT
41	PERp0	42	CL_CLK
43	PERn0	44	CNV_GNSS_PA_BLANKING
45	GND	46	CNV_MFUART2_TXD
47	REFCLKp0	48	CNV_MFUART2_RXD
49	REFCLKn0	50	SUSCLK
51	GND	52	WLAN_RST#
53	CLKREQ0#	54	BT_RF_KILL#
55	PEWAKE0#	56	WIFI_RF_KILL#
57	GND	58	NC
59	CNV_WT_D1-	60	NC
61	CNV_WT_D1+	62	NC
63	GND	64	NC

Table 2.6: M.2 E-Key Connector (M2_E1)

65	CNV_WT_D0-	66	NC
67	CNV_WT_D0+	68	NC
69	GND	70	NC
71	CNV_WT_CLK-	72	+3.3V
73	CNV_WT_CLK+	74	+3.3V
75	GND		

2.2.7 M.2 B-Key Connector (M2_B1)

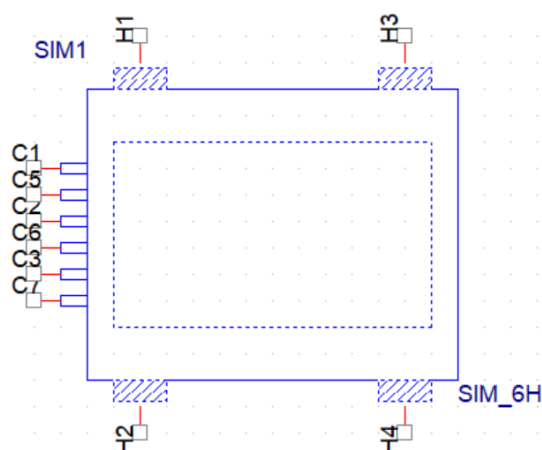
**Table 2.7: M.2 B-Key Connector (M2_B1)**

Pin	Signal	Pin	Signal
1	M2B1_CONFIG_3	2	+V3.3_M2B1_S0
3	GND	4	+V3.3_M2B1_S0
5	GND	6	M2B1_POWER_OFF#_R
7	USB2_M2B1_P4+	8	M2B1_W_DISABLE#_R
9	USB2_M2B1_P4-	10	M2B1_LED1#
11	GND	20	M2B1_I2S_SCLK
21	M2B1_CONFIG_0	22	M2B1_I2S_TXD
23	M2B1_WAKE_WWAN#	24	M2B1_I2S_RXD
25	M2B1_SAR_DPR_WWAN	26	M2B1_GNSS_DISABLE#_R
27	GND	28	M2B1_I2S_SFRM_R
29	M2B1_USB3_RX-	30	NC
31	M2B1_USB3_RX+	32	NC
33	GND	34	NC
35	M2B1_USB3_TX-	36	NC
37	M2B1_USB3_TX+	38	M2B1_SATA_DEVSLP_R
39	GND	40	NC
41	M2PCIE_M2SATA_RX-	42	NC
43	M2PCIE_M2SATA_RX+	44	NC
45	GND	46	NC
47	M2PCIE_M2SATA_TX-	48	NC
49	M2PCIE_M2SATA_TX+	50	M2B1_PLTRST#
51	GND	52	M2B1_CLKREQ2#_R
53	M2B1_CLK-	54	M2B1_PCIE_WAKE#
55	M2B1_CLK+	56	NC
57	GND	58	NC
59	NC	60	NC

Table 2.7: M.2 B-Key Connector (M2_B1)

61	NC	62	NC
63	NC	64	NC
65	NC	66	NC
67	M2B1_RESET#_R	68	M2B1_SUSCLK
69	M2B1_CONFIG_1	70	+V3.3_M2B1_S0
71	GND	72	+V3.3_M2B1_S0
73	GND	74	+V3.3_M2B1_S0
75	M2B1_CONFIG_2		

2.2.8 SIM Card Connector (SIM1)

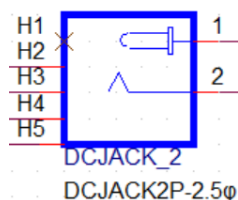
**Table 2.8: SIM Card Connector (SIM1)**

Pin	Signal	Pin	Signal
C1	VCC	C5	GND
C2	RST	C6	VPP
C3	CLK	C7	IO

2.2.9 DDR5 SODIMM Socket (DIMMA1)

Please refer to JEDEC STANDARD.

2.2.10 12V Power Supply Connector (DCIN1)

**Table 2.9: 12V Power Supply Connector (DCIN1)**

Pin	Signal
1	+12V
2	GND

2.2.11 SATA Connector (SATA1)

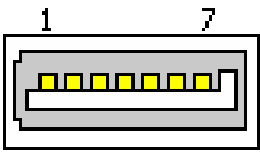


Table 2.10: SATA Connector (SATA1)

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

2.2.12 PCIe x1 Connector (PCIEX1_1)

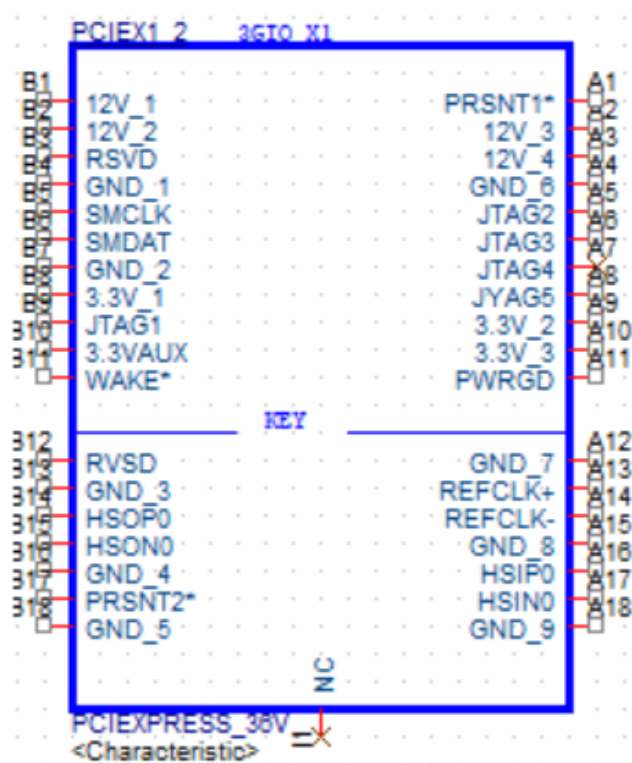


Table 2.11: PCIe x1 Connector (PCIEX1_1)

Pin	Signal	Pin	Signal
A1	PRSNT	B1	12V
A2	12V	B2	12V
A3	12V	B3	RSVD
A4	GND	B4	GND
A5	JTAG	B5	SMCLK
A6	JTAG	B6	SMDAT
A7	JTAG	B7	GND
A8	JTAG	B8	3.3V
A9	3.3V	B9	JTAG
A10	3.3V	B10	3.3V_AUX
A11	PWRGD	B11	WAKE#
A12	GND	B12	RSVD
A13	REFCLK+	B13	GND
A14	REFCLK-	B14	HSOP0
A15	GND	B15	HSON0
A16	HSIP0	B16	GND
A17	HSIN0	B17	PRSNT
A18	GND	B18	GND

2.2.13 HD Analog Audio Interface Line-Out (AUDIO1)

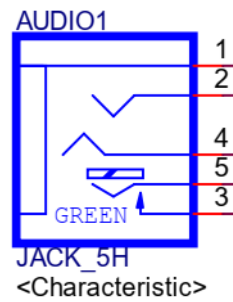


Table 2.12: HD Analog Audio Interface Line-Out (AUDIO1)

Pin	Signal
1	GND_A
2	A_Z_LINEO-L
3	GND_A
4	A_Z_LINEO-R
5	A_FRONT-JD

2.2.14 HD Analog Audio Interface Mic-In (AUDIO2)

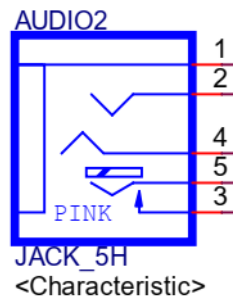


Table 2.13: HD Analog Audio Interface Mic-In (AUDIO2)

Pin	Signal
1	GND_A
2	A_Z_MIC1-L
3	GND_A
4	A_Z_MIC1-R
5	A_MIC1-JD

2.2.15 RJ-45 Single LAN Port (LAN1)

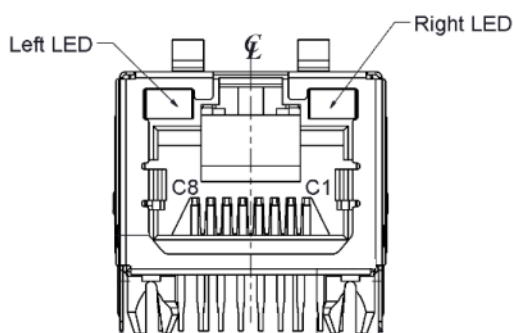


Table 2.14: RJ-45 Single LAN Port (LAN1)

Pin	Signal
L1	LAN1_LED1_ACT#_R
L2	+V3.3_DUAL
L3	LAN1_LED2_1G#_R
L4	LAN1_LED0_100M#_R
R1	LAN1_MDI0+
R2	LAN1_MDI0-
R3	LAN1_MDI1+
R4	LAN1_MDI1-
R5	LAN1_CONN
R6	LAN1_CT
R7	LAN1_MDI2+
R8	LAN1_MDI2-
R0	LAN1_MDI3+
R10	LAN1_MDI3-
H1	NC
H2	NC
H3	GND
H4	GND

2.3 Box Header

2.3.1 EDP Connector / LVDS Connector (EDP1_LVDS1)

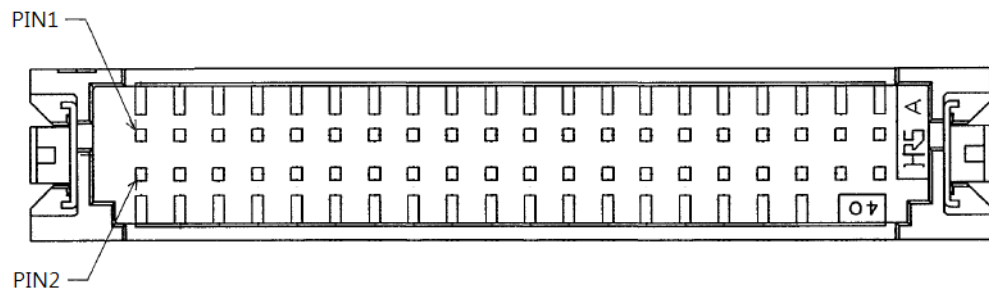


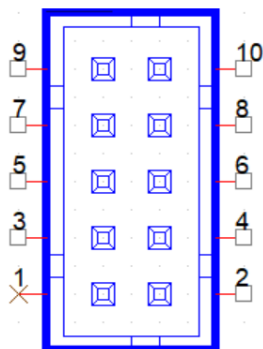
Table 2.15: LVDS1

Pin	Signal	Pin	Signal
1	VDD	2	VDD
3	LVDS_DETECT#	4	GND
5	VDD	6	VDD
7	LVDS_OD0-	8	LVDS_ED0-
9	LVDS_OD0+	10	LVDS_ED0+
11	GND	12	GND
13	LVDS_OD1-	14	LVDS_ED1-
15	LVDS_OD1+	16	LVDS_ED1+
17	GND	18	GND
19	LVDS_OD2-	20	LVDS_ED2-
21	LVDS_OD2+	22	LVDS_ED2+
23	GND	24	GND
25	LVDS_OCK-	26	LVDS_ECK-
27	LVDS_OCK+	28	LVDS_ECK+
29	GND	30	GND
31	N.C	32	N.C
33	GND	34	GND
35	LVDS_OD3-	36	LVDS_ED3-
37	LVDS_OD3+	38	LVDS_ED3+
39	N.C	40	LVDS_VCON

Table 2.16: EDP1

Pin	Signal	Pin	Signal
1	VDD	2	VDD
3	LVDS DETECT#	4	GND
5	VDD	6	VDD
7	EDP_TX2-	8	N.C
9	EDP_TX2+	10	N.C
11	GND	12	GND
13	EDP_TX1-	14	N.C
15	EDP_TX1+	16	N.C
17	GND	18	GND
19	EDP_TX0-	20	N.C
21	EDP_TX0+	22	N.C
23	GND	24	GND
25	EDP_TX3-	26	N.C
27	EDP_TX3+	28	N.C
29	GND	30	GND
31	EDP_AUX+	32	EDP_AUX-
33	GND	34	EDP_HPD
35	N.C	36	N.C
37	N.C	38	N.C
39	N.C	40	GND

2.3.2 Internal USB 2.0 Connector * 2 Ports (USB34)

**Table 2.17: Internal USB 2.0 Connector * 2 Ports (USB34)**

Pin	Signal	Pin	Signal
1	N.C	2	GND
3	GND	4	GND
5	D+	6	D+
7	D-	8	D-
9	VBUS	10	VBUS

2.3.3 Internal USB 2.0 Connector * 2 Ports (USB56)

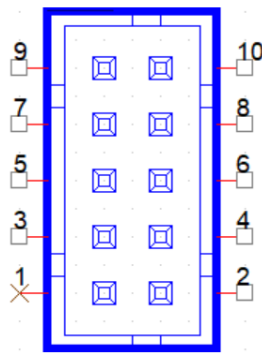


Table 2.18: Internal USB 2.0 Connector * 2 Ports (USB56)

Pin	Signal	Pin	Signal
1	N.C	2	GND
3	GND	4	GND
5	D+	6	D+
7	D-	8	D-
9	VBUS	10	VBUS

2.3.4 Internal USB 2.0 Connector * 1 Port (USB7)

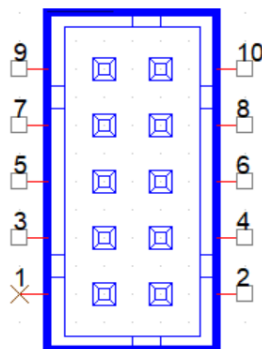


Table 2.19: Internal USB 2.0 Connector * 1 Port (USB7)

Pin	Signal	Pin	Signal
1	N.C	2	N.C
3	GND	4	N.C
5	D+	6	N.C
7	D-	8	N.C
9	VBUS	10	N.C

2.3.5 COM1 Connector (COM1)

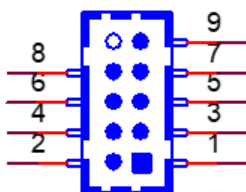


Table 2.20: COM1 Connector (COM1)

Pin	Signal	Pin	Signal
1	DCD#	2	SIN
3	SOUT	4	DTR
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI		

2.3.6 COM2 Connector (COM2)

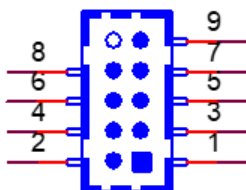


Table 2.21: COM2 Connector (COM2)

Pin	Signal	Pin	Signal
1	DCD#	2	SIN
3	SOUT	4	DTR
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI		

2.3.7 COM3 Connector (COM3)

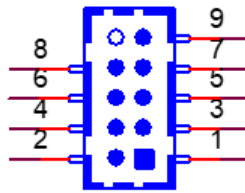


Table 2.22: COM2 Connector (COM3)

Pin	Signal	Pin	Signal
1	DCD#	2	SIN
3	SOUT	4	DTR
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI		

2.3.8 COM4 Connector (COM4)

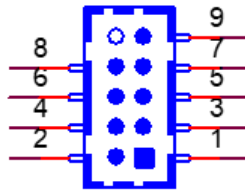


Table 2.23: COM2 Connector (COM4)

Pin	Signal	Pin	Signal
1	DCD#	2	SIN
3	SOUT	4	DTR
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI		

2.3.9 COM5 Connector (COM5)

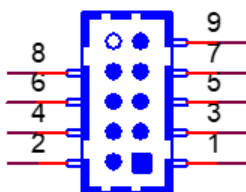


Table 2.24: COM2 Connector (COM5)

Pin	Signal	Pin	Signal
1	DCD#	2	SIN
3	SOUT	4	DTR
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI		

2.3.10 COM6 Connector (COM6)

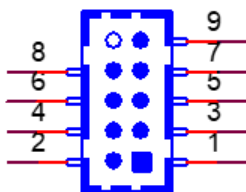


Table 2.25: COM2 Connector (COM6)

Pin	Signal	Pin	Signal
1	DCD#	2	SIN
3	SOUT	4	DTR
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI		

2.3.11 CMOS Battery Connector (BAT1)

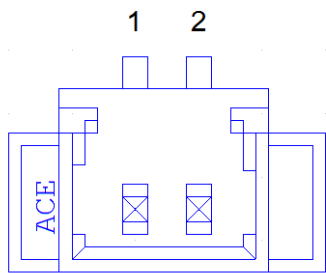


Table 2.26: CMOS Battery Connector (BAT1)

Pin	Signal
1	+VBAT
2	GND

2.3.12 EDP/LVDS Backlight Inverter Power Conn. (INV1)

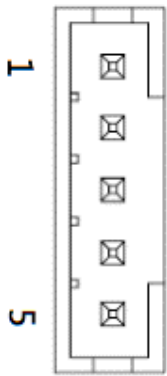


Table 2.27: EDP/LVDS Backlight Inverter Power Conn. (INV1)

Pin	Signal
1	+12V
2	GND
3	BKL EN
4	BKL CTRL
5	+5V

2.3.13 ATX 4-Pin Power Connector (180D) (ATX12V1)

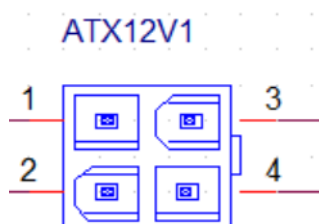


Table 2.28: ATX 4-Pin Power Connector (180D) (ATX12V1)

Pin	Signal	Pin	Signal
1	GND	2	GND
3	+12V	4	+12V

2.3.14 ATX 5V/PSON Connector (ATX_5VSB1)

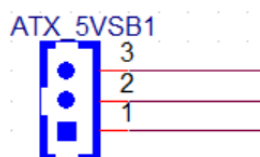


Table 2.29: ATX 5V/PSON Connector (ATX_5VSB1)

Pin	Signal
1	ATX_5V
2	GND
3	PS_ON#

2.3.15 SATA Power Connector (SATA_PWR1)

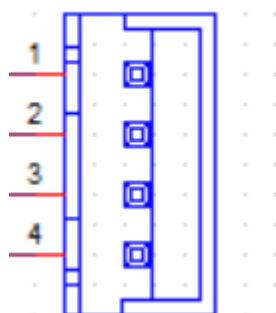


Table 2.30: SATA Power Connector (SATA_PWR1)

Pin	Signal
1	+V5
2	GND
3	GND
4	+V12

2.4 Pin Header

2.4.1 Power LED Pin Header (JFP2)

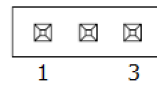


Table 2.31: Power LED Pin Header (JFP2)

Pin	Signal
1	Power LED+
2	NC
3	Power LED-

2.4.2 SPI BIOS Flash Socket (SPI1)

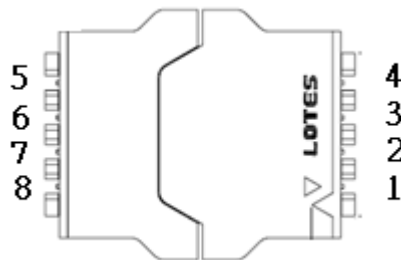


Table 2.32: SPI BIOS Flash Socket (SPI1)

Pin	Signal	Pin	Signal
1	CS#	5	MOSI
2	MISO	6	SCLK
3	WP# / IO2	7	HOLD# / IO3
4	GND	8	+V3.3_SPI

2.4.3 SPI BIOS Debug Header (SPI_CN1)

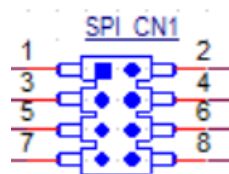


Table 2.33: SPI BIOS Debug Header (SPI_CN1)

Pin	Signal	Pin	Signal
1	CS#	5	WP
2	+V3.3_SPI	6	CLK
3	MISO	7	GND
4	HOLD	8	MOSI

2.4.4 8-Bit General Purpose I/O Pin Header (GPIO1)

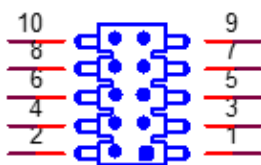


Table 2.34: 8-Bit General Purpose I/O Pin Header (GPIO1)

Pin	Signal	Pin	Signal
1	GPIO0	2	GPIO4
3	GPIO1	4	GPIO5
5	GPIO2	6	GPIO6
7	GPIO3	8	GPIO7
9	VCC_GPIO	10	GND

2.4.5 CPU FAN Connector (CPUFAN1)

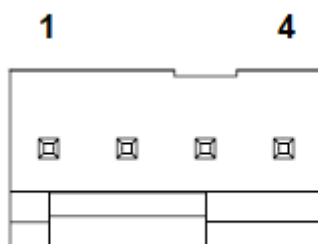


Table 2.35: CPU FAN Connector (CPUFAN1)

Pin	Signal
1	GND
2	CPU FAN VCC
3	CPU FAN SPEED
4	CPU FAN PWM

2.4.6 System Fan Connector (SYSFAN1)

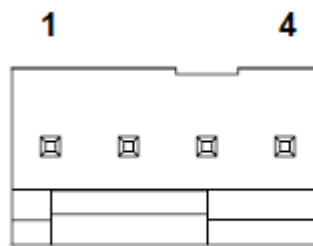


Table 2.36: System Fan Connector (SYSFAN1)

Pin	Signal
1	GND
2	CPU FAN VCC
3	CPU FAN SPEED
4	CPU FAN PWM

2.4.7 Case Open Connector (JCASE1)

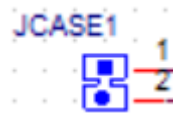


Table 2.37: Case Open Connector (JCASE1)

Pin	Signal
1	CASEOP
2	GND

2.4.8 Programming Header (VR_PMB1)

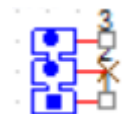


Table 2.38: Programming Header (VR_PMB1)

Pin	Signal
1	VR_SDATA
2	GND
3	VR_SCLK

2.4.9 HD Digital Audio Interface S/PDIF Out (SPDIF1)

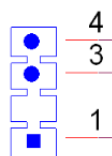


Table 2.39: HD Digital Audio Interface S/PDIF Out (SPDIF1)

Pin	Signal Pin Definition
1	+5V
2	NA
3	SPDIF OUT
4	GND

2.4.10 Audio Amplifier Output Pin Header (AMP1)

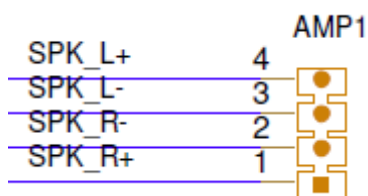


Table 2.40: Audio Amplifier Output Pin Header (AMP1)

Pin	Signal
1	AMP OUT – R+
2	AMP OUT – R-
3	AMP OUT – L-
4	AMP OUT – L+

2.4.11 HD Analog Audio Interface Front Panel (FPAUD1)

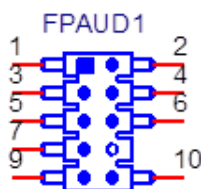


Table 2.41: HD Analog Audio Interface Front Panel (FPAUD1)

Pin	Signal	Pin	Signal
1	VCC_USB0	5	VCC_USB1
2	USB-0_B	6	USB-1_B
3	USB+0_B	7	USB+1_B
4	GND_1	8	GND_2

2.4.12 LED Port 80 Connector (LED_P80)

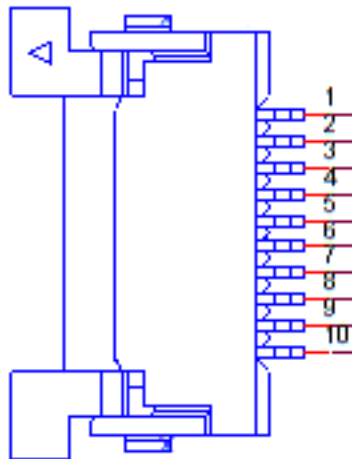


Table 2.42: LED Port 80 Connector (LED_P80)

Pin	Signal
1	GND
2	LED_A
3	LED_B
4	LED_C
5	LED_D
6	LED_E
7	LED_F
8	LED_G
9	DGH0#
10	DGL0#

2.5 Jumper Settings

2.5.1 COM6 RI# Selection Pin Header (JSETCOM6_V1)

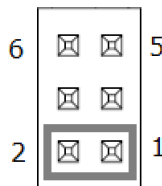


Table 2.43: COM6 RI# Selection Pin Header (JSETCOM6_V1)

Pin	Signal	Pin	Signal
1	RI# [1]	2	COM6_RI_VA#
3	COM6_RI_VA#	4	+5V
5	+12V	6	COM6_RI_VA#

2.5.2 COM4 CCTALK Voltage Select Header (JCCT_VCON1)

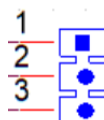


Table 2.44: COM4 CCTALK Voltage Select Header (JCCT_VCON1)

Pin	Signal
1	+12V
2	COM4_SOUT
3	+5V

2.5.3 Watchdog Timer Output and OBS Beep (JWDT1+JOBS1)

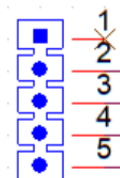


Table 2.45: Watchdog Timer Output and OBS Beep (JWDT1+JOBS1)

Pin	Signal
1	NC
2	SIO_WG#
3	SYS_RESET#
4	SIO_ERR_BEEP
5	FRP_BEEP

2.5.4 EDP Panel/LVDS Panel Voltage Selection (JEDP1_LVDS1)

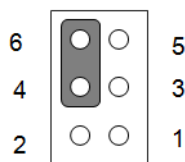


Table 2.46: EDP Panel / LVDS Panel Voltage Selection (JEDP1_LVDS1)

Pin	Signal	Pin	Signal
1	NC	2	+5V
3	+12V	4	VDD
5	NC	6	+3.3V

2.5.5 PWRBTN#/RESET#/HDD LED/Serial Bus from HW Monitor IC/ Internal Buzzer/External Speaker Header (JFP1)

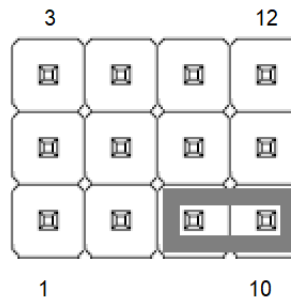


Table 2.47: PWRBTN#/RESET#/HDD LED/Serial Bus from HW Monitor IC /Internal Buzzer/External Speaker Header (JFP1)

Pin	Signal	Pin	Signal
1	+5V	2	HDD LED+
3	Power Button+	4	SPK_P2
5	HDD LED-	6	Power Button-
7	SPK_P3	8	SMB_DATA
9	System Reset+	10	SPK_P4
11	SMB_CLK	12	System Reset-

2.5.6 Case Open Signal Reverse Header (JCASEOP_SW1)

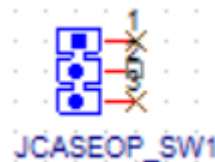


Table 2.48: Case Open Signal Rev. Header (JCASEOP_SW1)

Pin	Signal
1	CASEOP#
2	HWM_CASEOP#
3	CASEOP

2.5.7 CMOS Reset Header (JCMOS1)

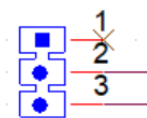


Table 2.49: CMOS Reset Header (JCMOS1)

Pin	Signal
1	NC
2	RTCRST#
3	RTCRST#_PD

2.5.8 AT/ATX Mode Selection (PSON1)

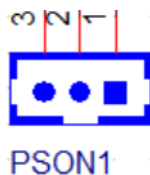


Table 2.50: AT/ATX Mode Selection (PSON1)

Pin	Signal
1	VCCAT
2	+V3_Pull High
3	VCCATX

2.5.9 VESA & JEIDA Support Select (SW_LVDS_VCON1)

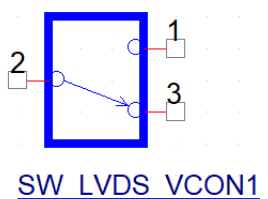


Table 2.51: VESA & JEIDA Support (SW_LVDS_VCON1)

Pin	Signal
1	100 ohm to +V3.3
2	LVDS1_VCON
3	GND

Chapter 3

BIOS Operation

3.1 Introduction

With the AMI BIOS Setup program, you can modify BIOS settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning special features on or off. This chapter describes the basic navigation of the AIMB-219 setup screens.

3.2 BIOS Setup

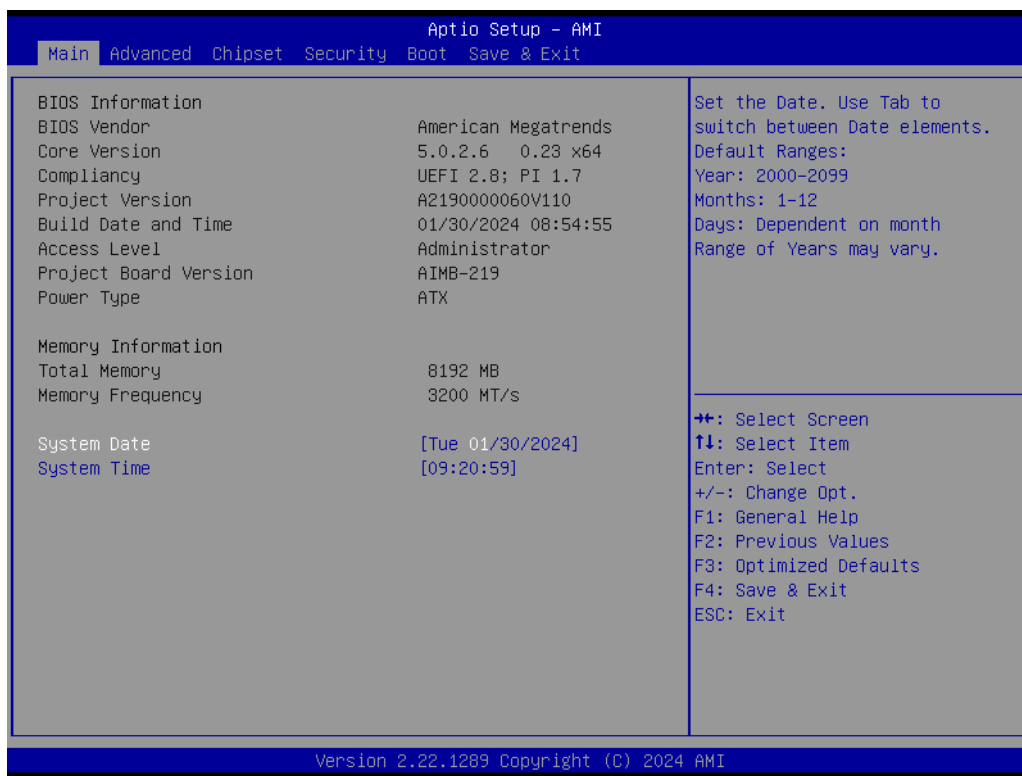
The AIMB-219 Series system has AMI BIOS built in, with a CMOS SETUP utility that allows users to configure required settings or to activate certain system features. The CMOS SETUP saves the configuration in the CMOS RAM of the motherboard. When the power is turned off, the battery on the board supplies the necessary power to preserve the CMOS RAM. When the power is turned on, press the key during the BIOS POST (Power-On Self-Test) to access the CMOS SETUP screen.

Table 3.1: Control Keys

< ↑ >< ↓ >< ← >< → >	Move to select item
<Enter>	Select item
<Esc>	Main Menu - Quit and do not save changes into CMOS Sub-Menu - Exit current page and return to the Main Menu
<Page Up/+>	Increase the numeric value or make changes
<Page Down/->	Decrease the numeric value or make changes
<F1>	General help, for the Setup Sub-Menu
<F2>	Item Help
<F5>	Load Previous Values
<F7>	Load Setup Defaults
<F10>	Save all CMOS changes

3.2.1 Main Menu

Press to enter the AMI BIOS CMOS Setup Utility. The Main Menu will appear on the screen. Use the arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.



The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the legend. Above the legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

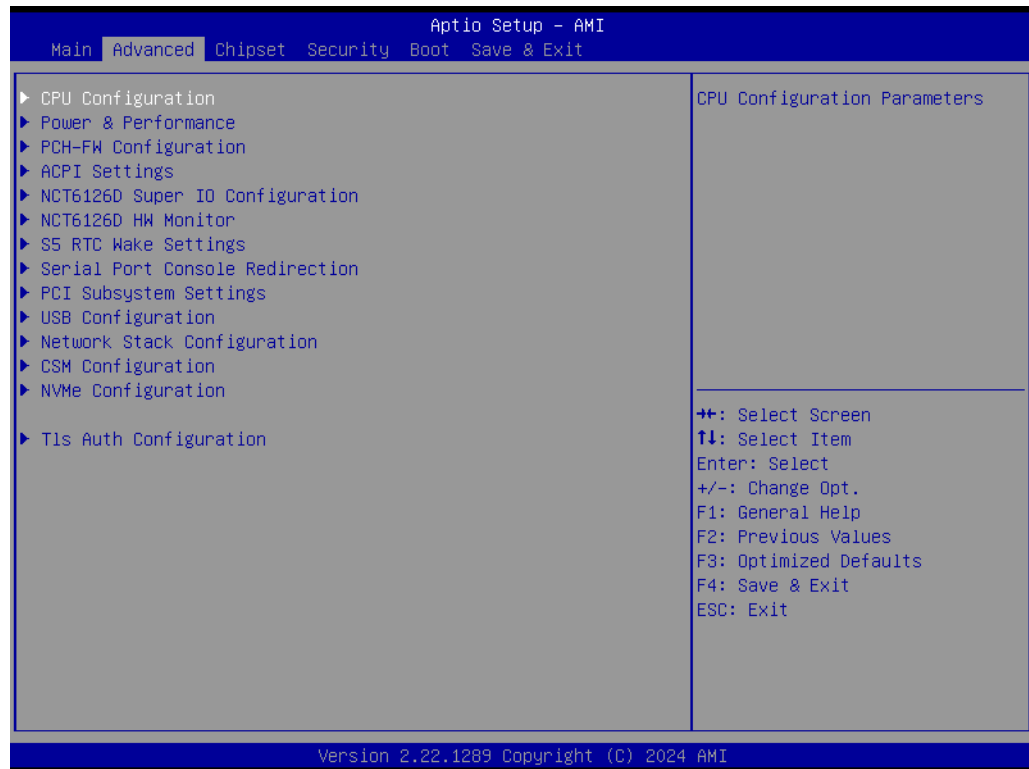
- **System Time/System Date:** Use this option to change the system time and date. Highlight the System Time or System Date using the keys. Enter new values via the keyboard. Press the <Tab> or <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

3.2.2 Advanced BIOS Features

Select the Advanced tab from the AIMB-219 setup menu to enter the Advanced BIOS setup page. Users can select any item in the left frame of the screen, such as CPU configuration. Select an Advanced BIOS setup option by highlighting the text using the <Arrow> keys. All Advanced BIOS setup options are described in this section. The Advanced BIOS setup menu screen is shown below. The sub-menus are described in the following pages.

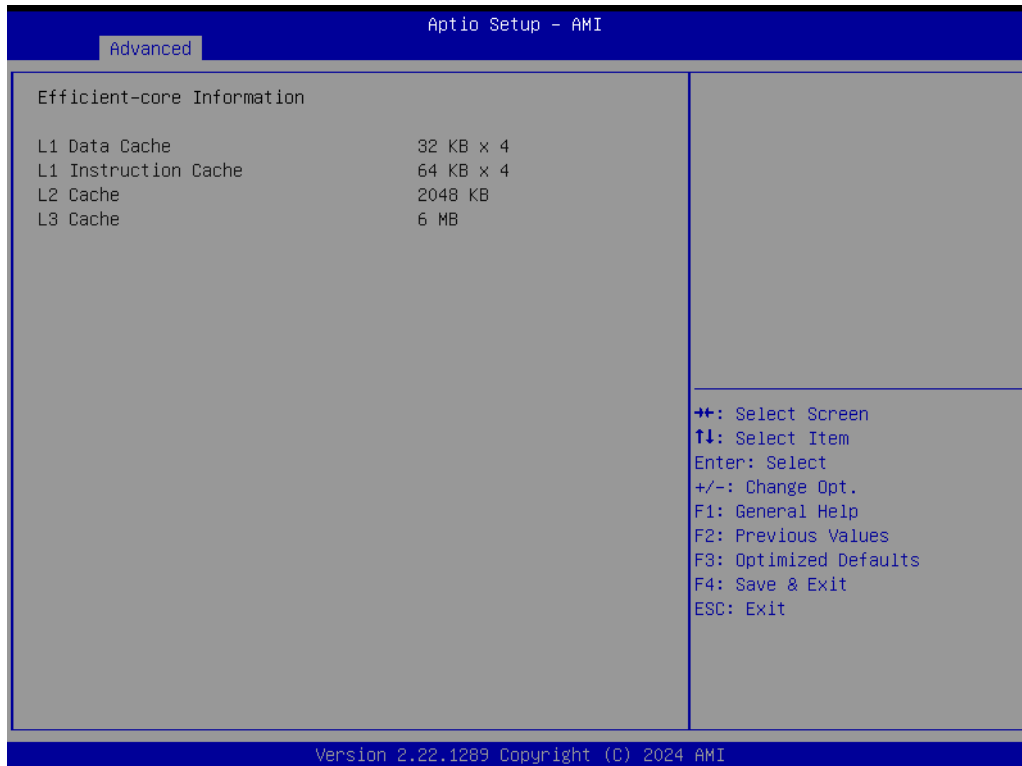
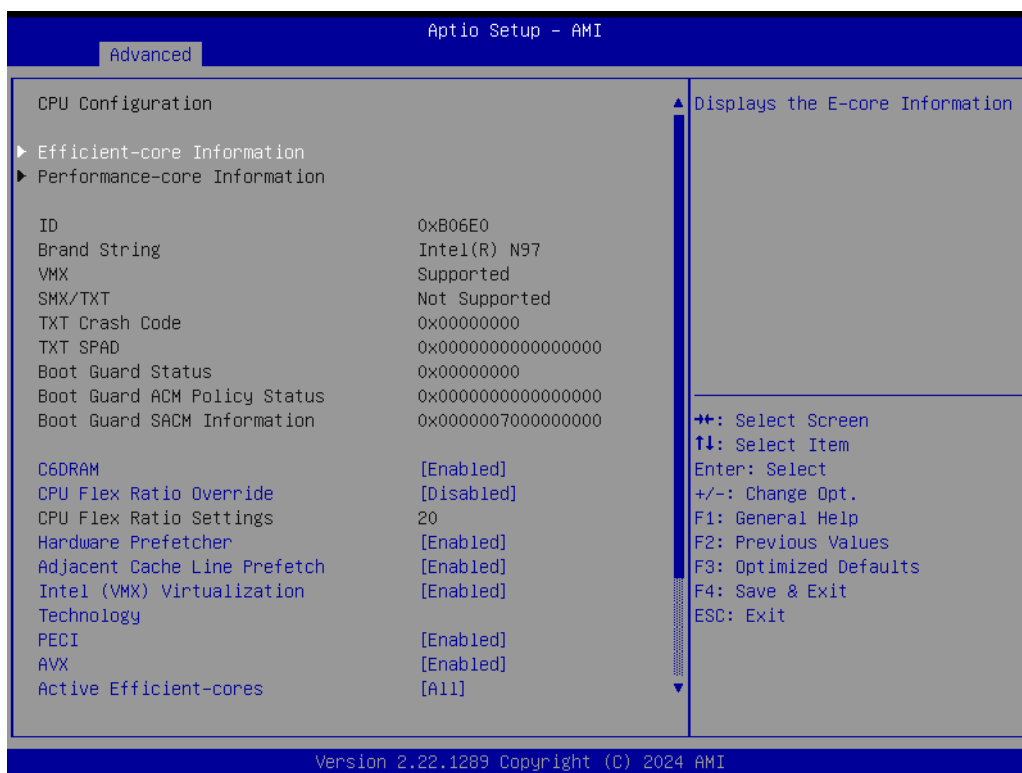
3.2.2.1 CPU Configuration

Advanced → CPU Configuration



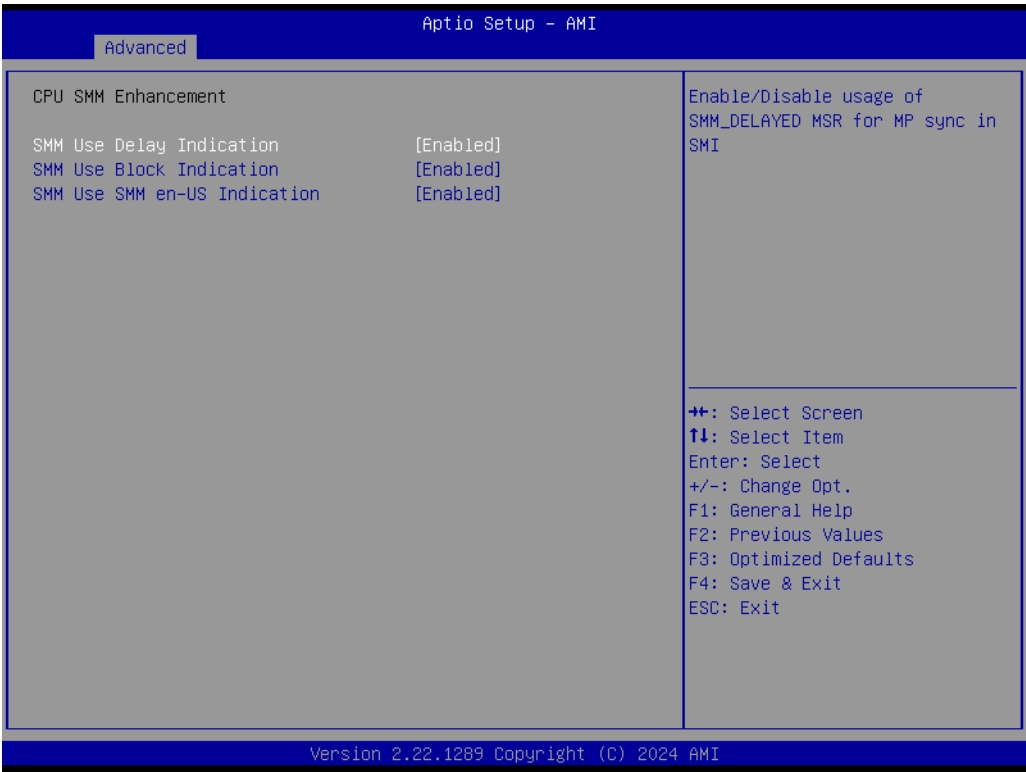
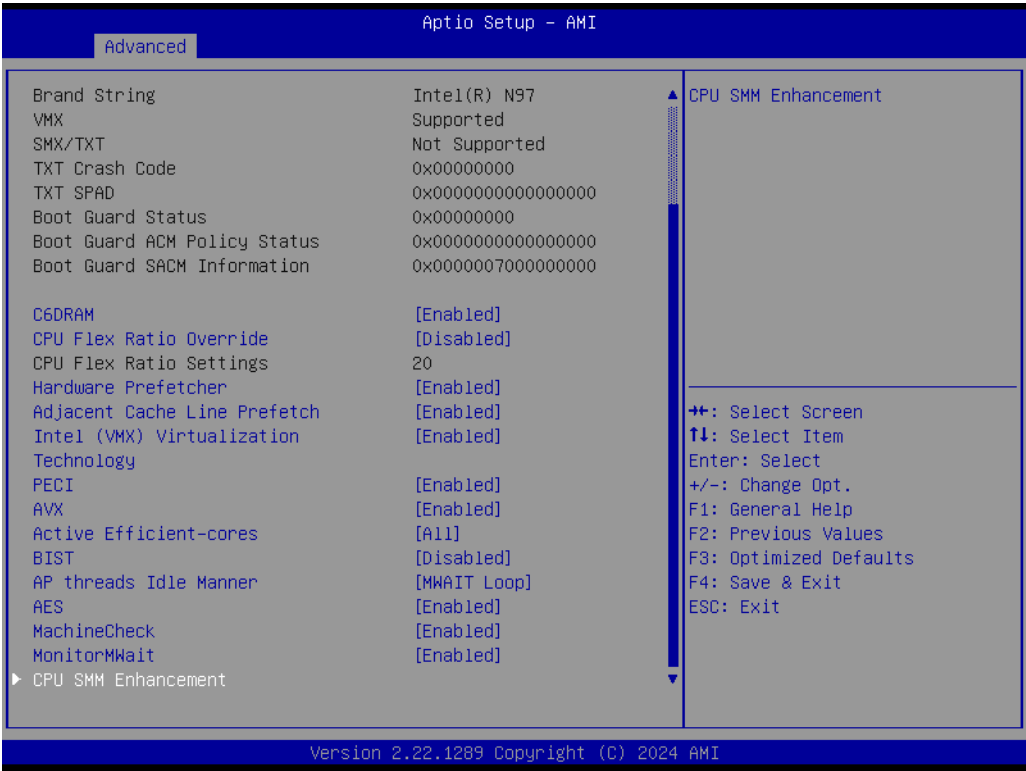
Efficient-core Information

Advanced → CPU Configuration → Efficient-core Information



CPU SMM Enhancement

Advanced → CPU SMM Enhancement



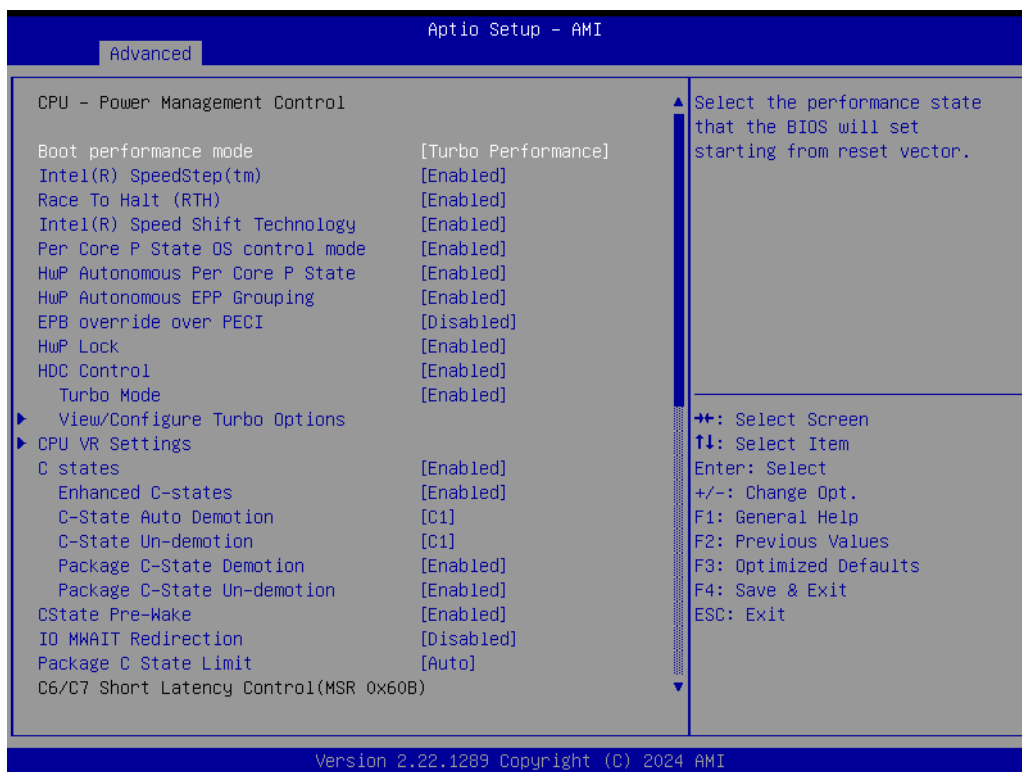
3.2.2.2 Power & Performance

Advanced → Power & Performance



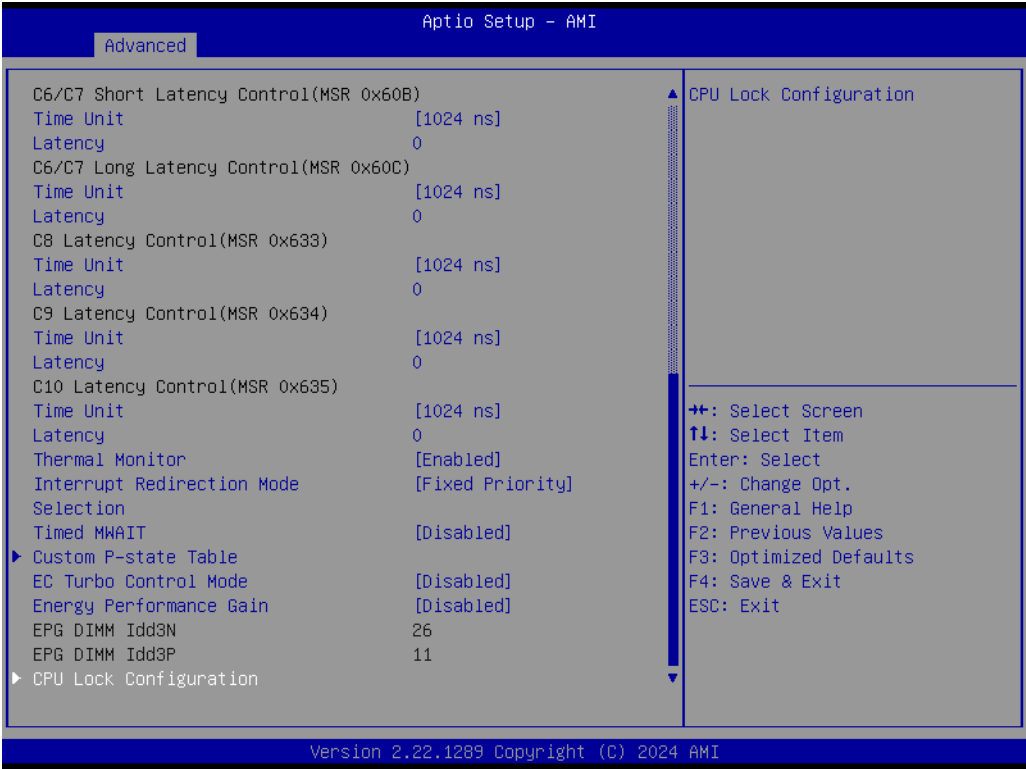
CPU – Power Management Control

Advanced → Power & Performance → CPU – Power Management Control



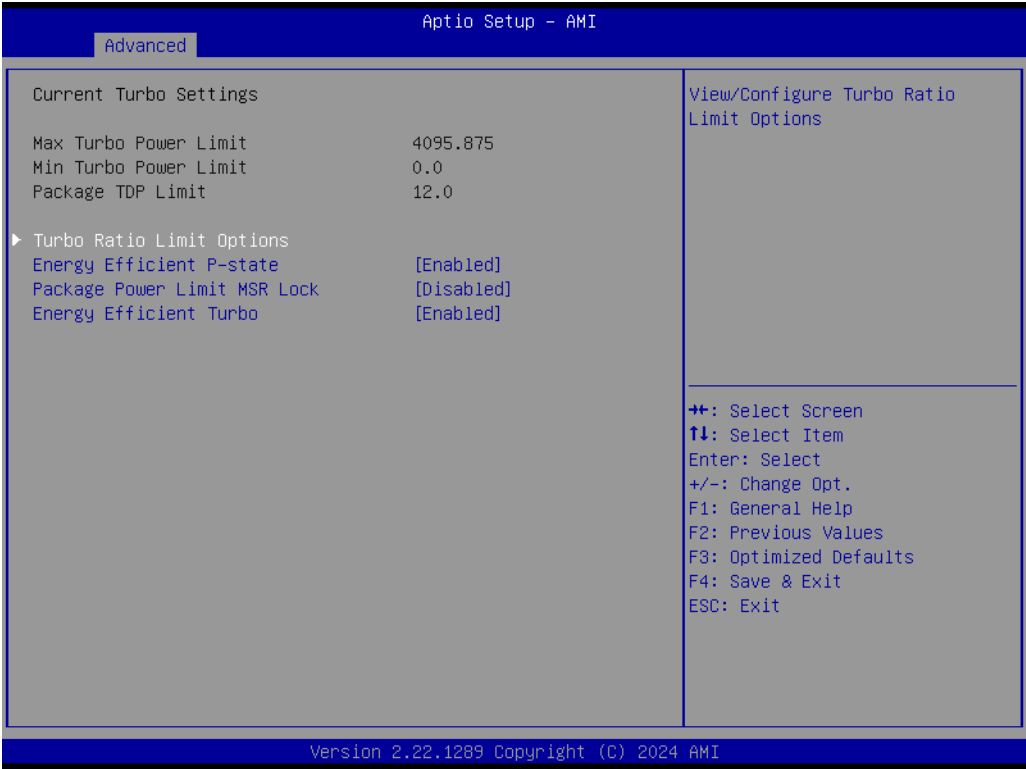
Current Turbo Settings

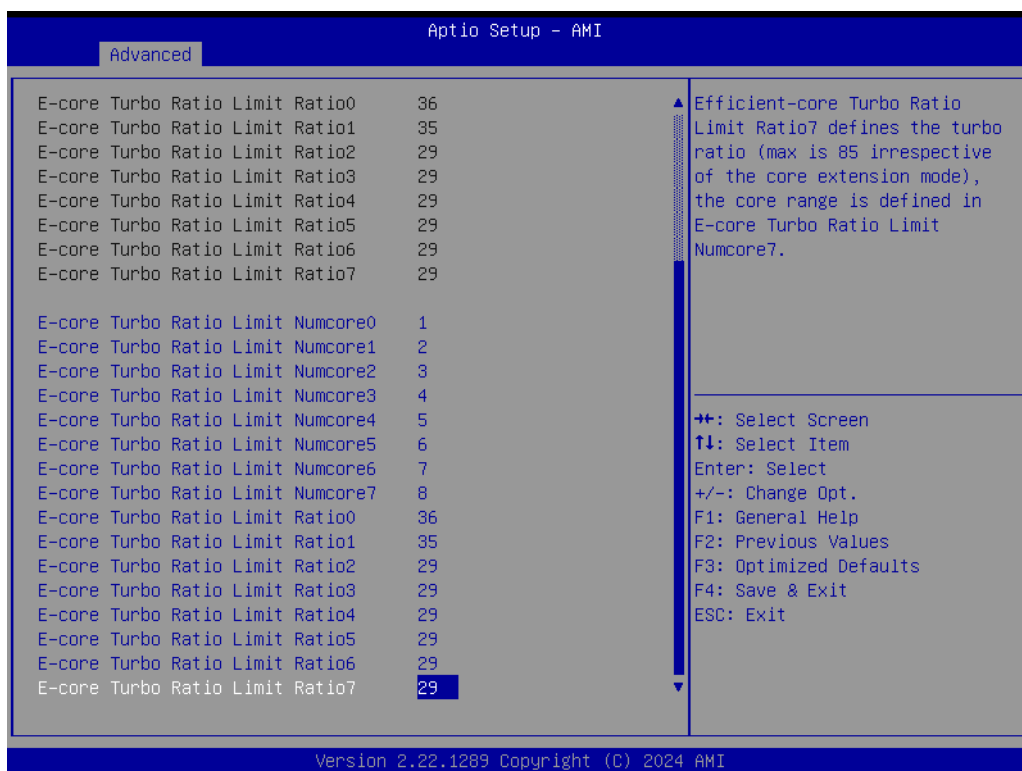
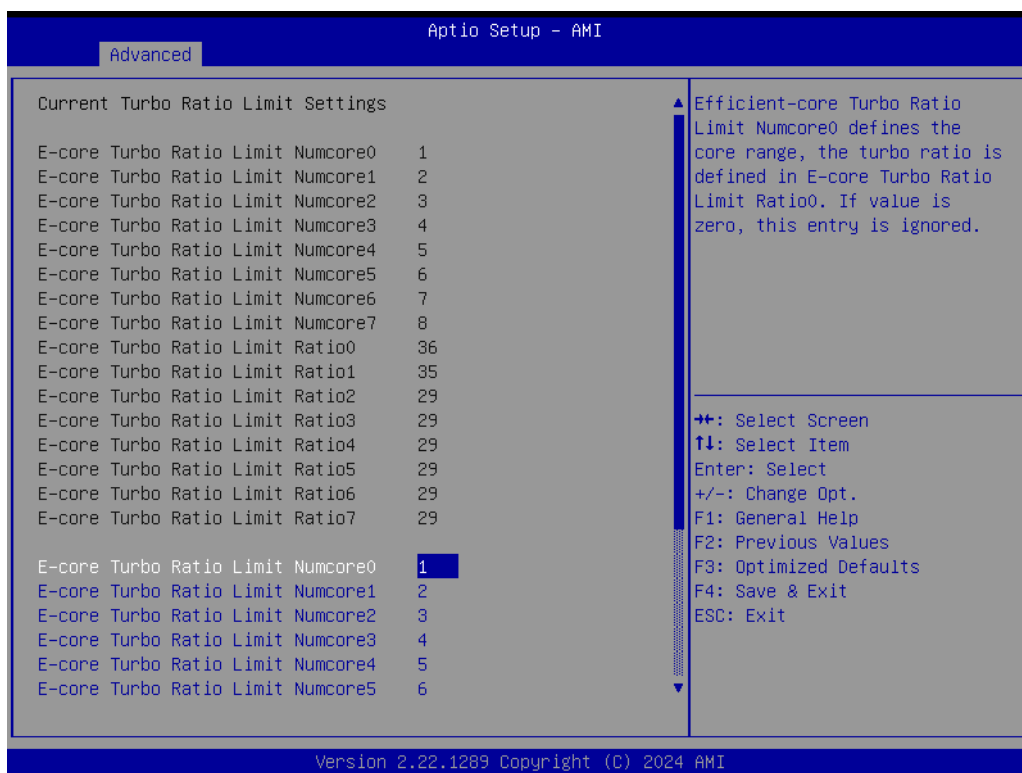
Advanced → Power & Performance → CPU – Power Management Control → View/Configure Turbo Ratio



Turbo Ratio Limit Options

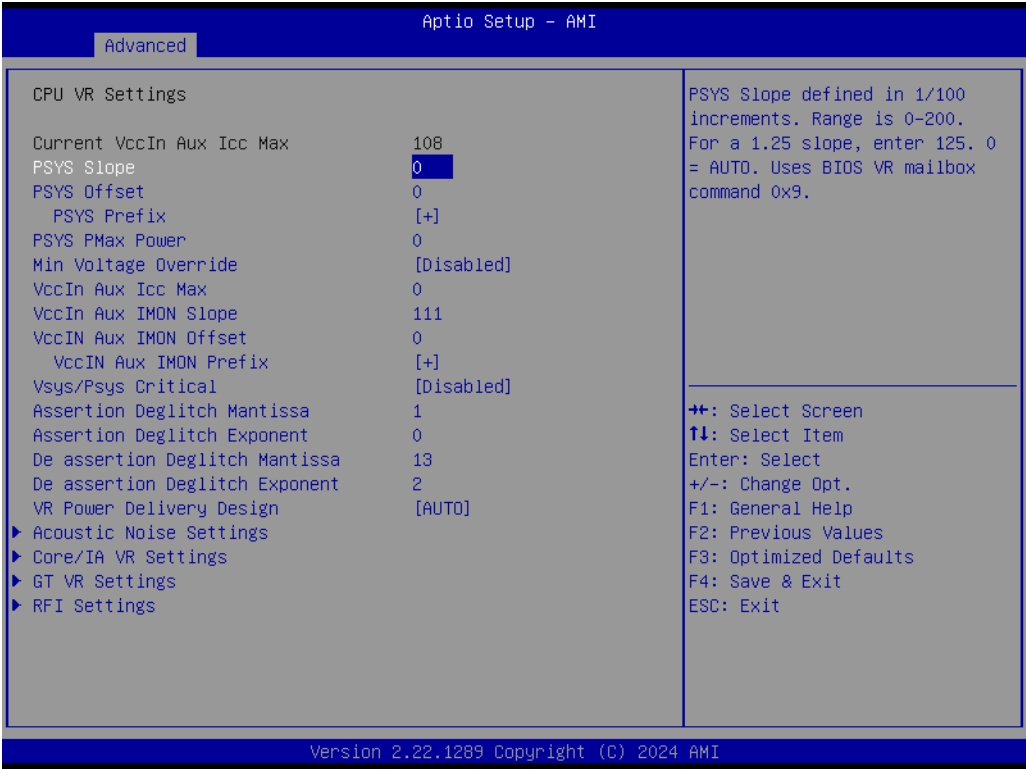
Advanced → Power & Performance → CPU – Power Management Control → View/Configure Turbo Ratio → Turbo Ratio Limit Options





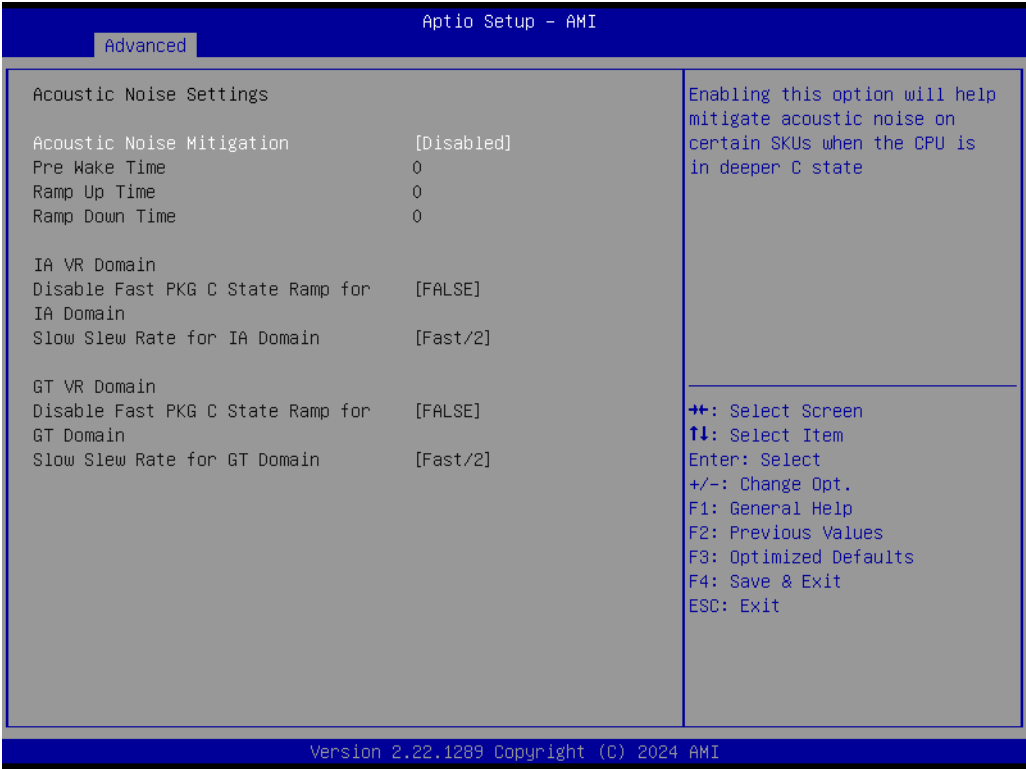
CPU VR Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings



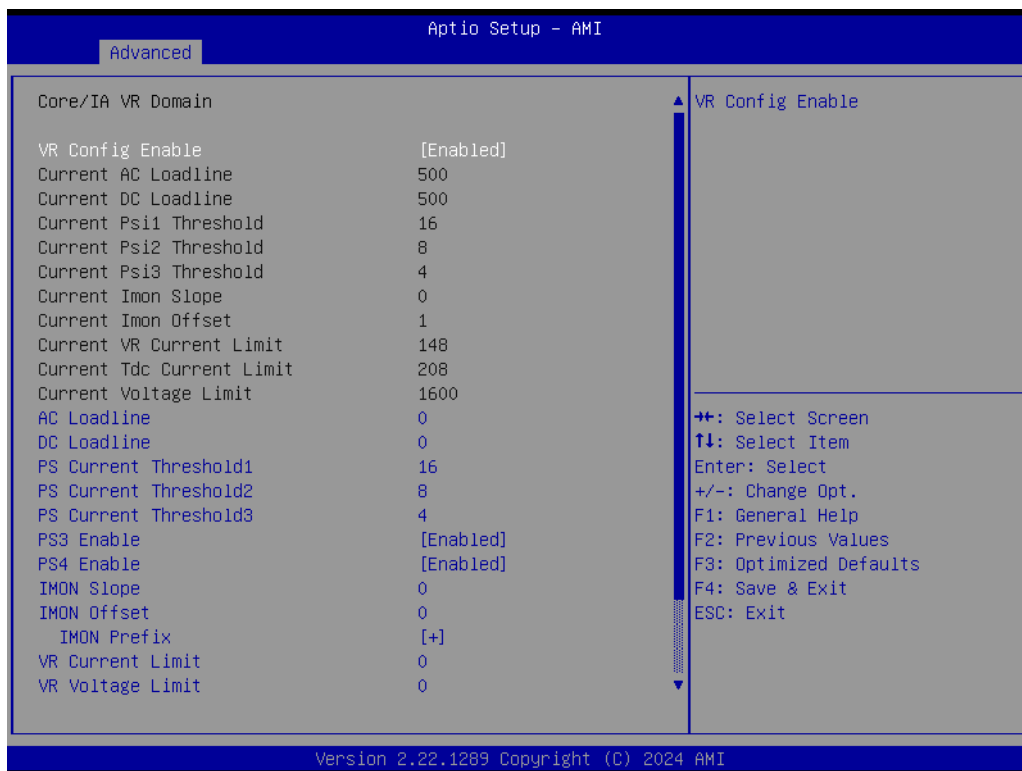
Acoustic Noise Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → Acoustic Noise Settings



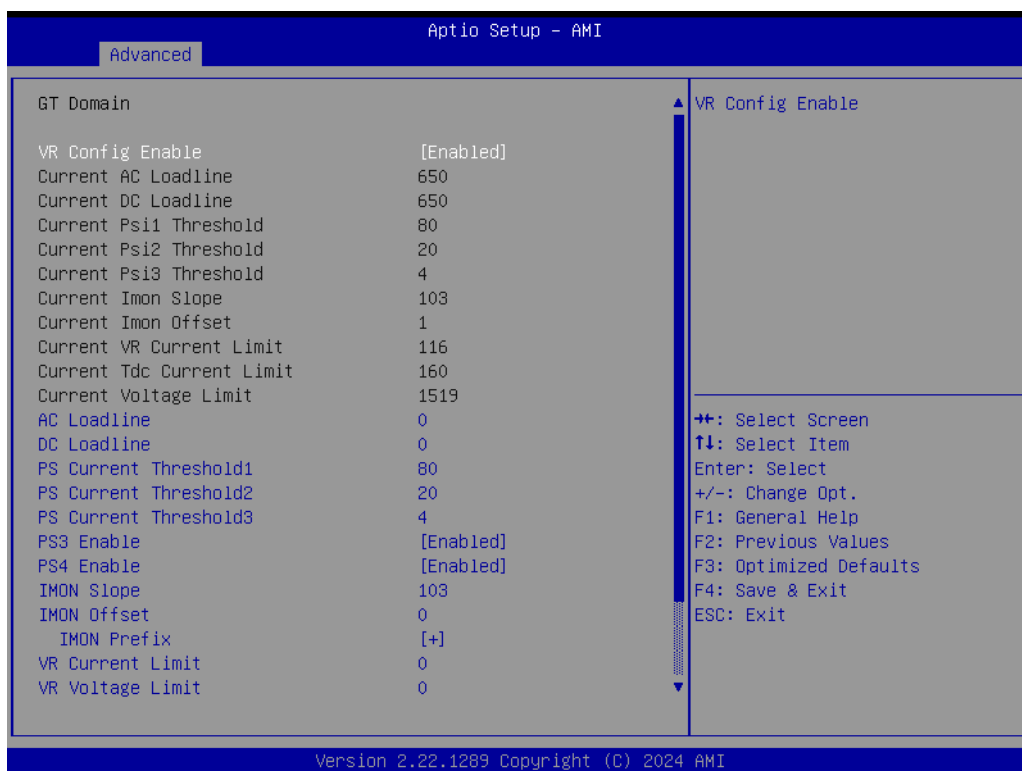
Core/IA VR Settings

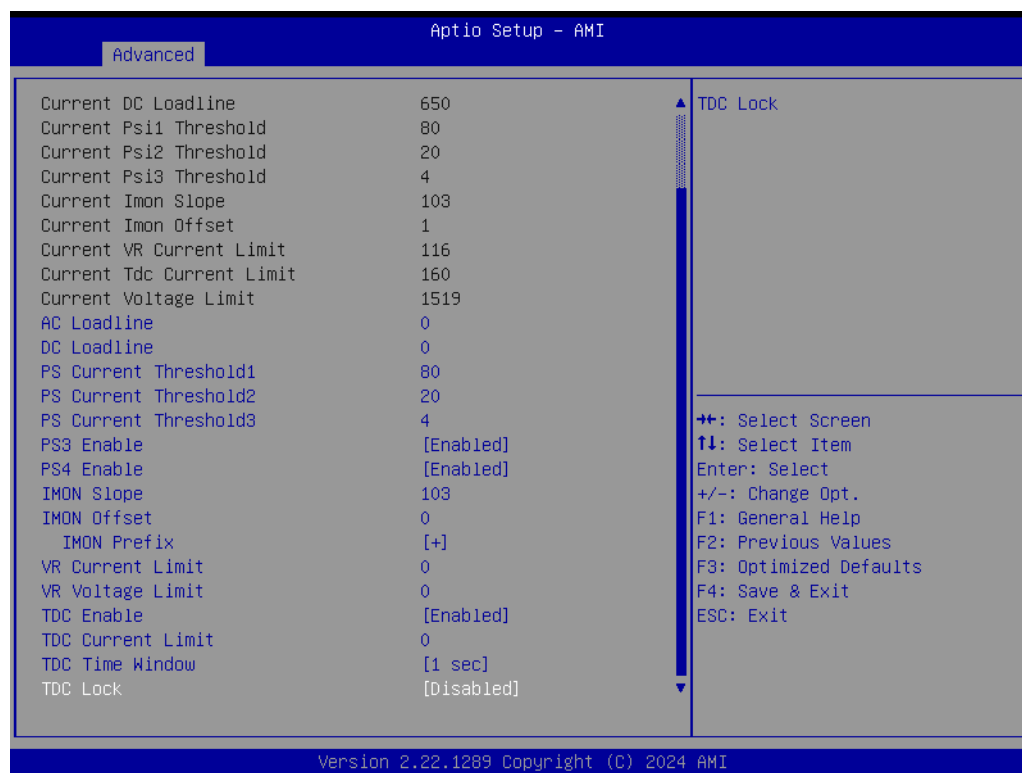
Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → Core/IA Settings



GT Domain

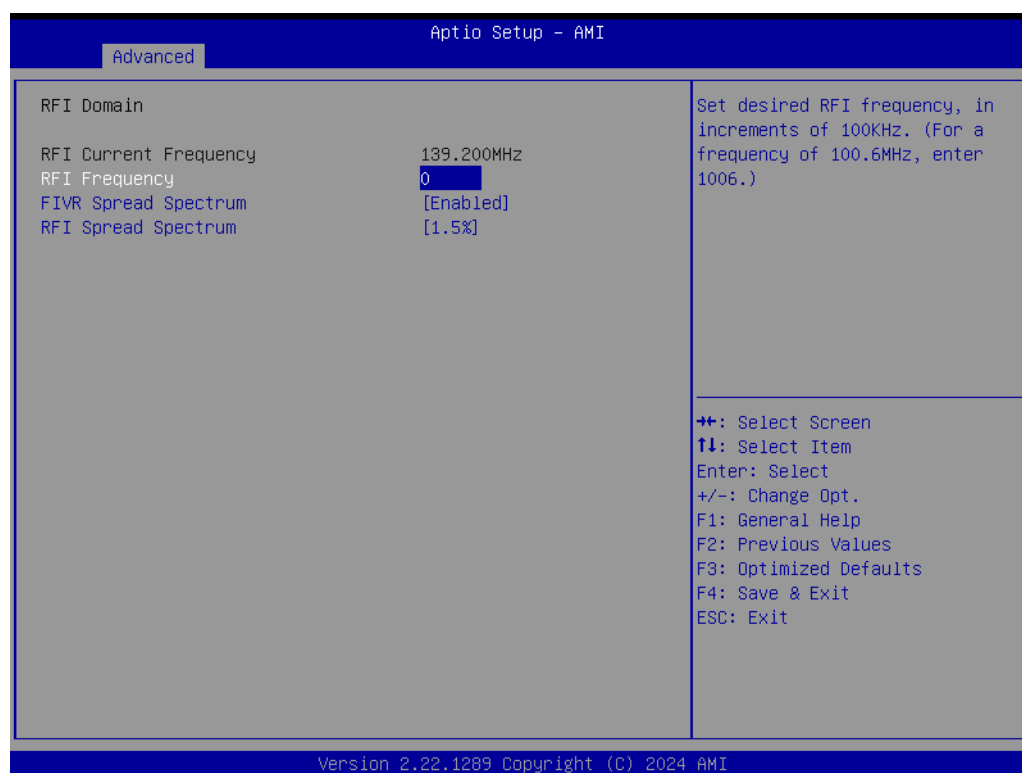
Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → GT Domain





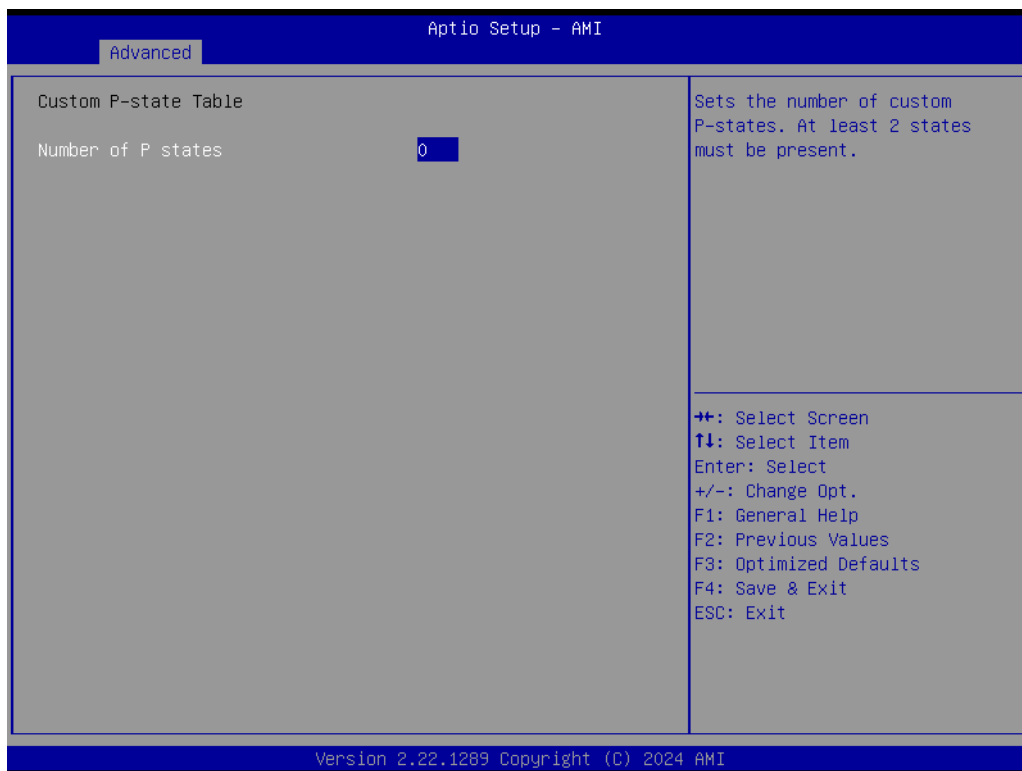
RFI Domain

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → RFI Domain



Custom P-state Table

Advanced → Power & Performance → CPU – Power Management Control → Custom P-state Table



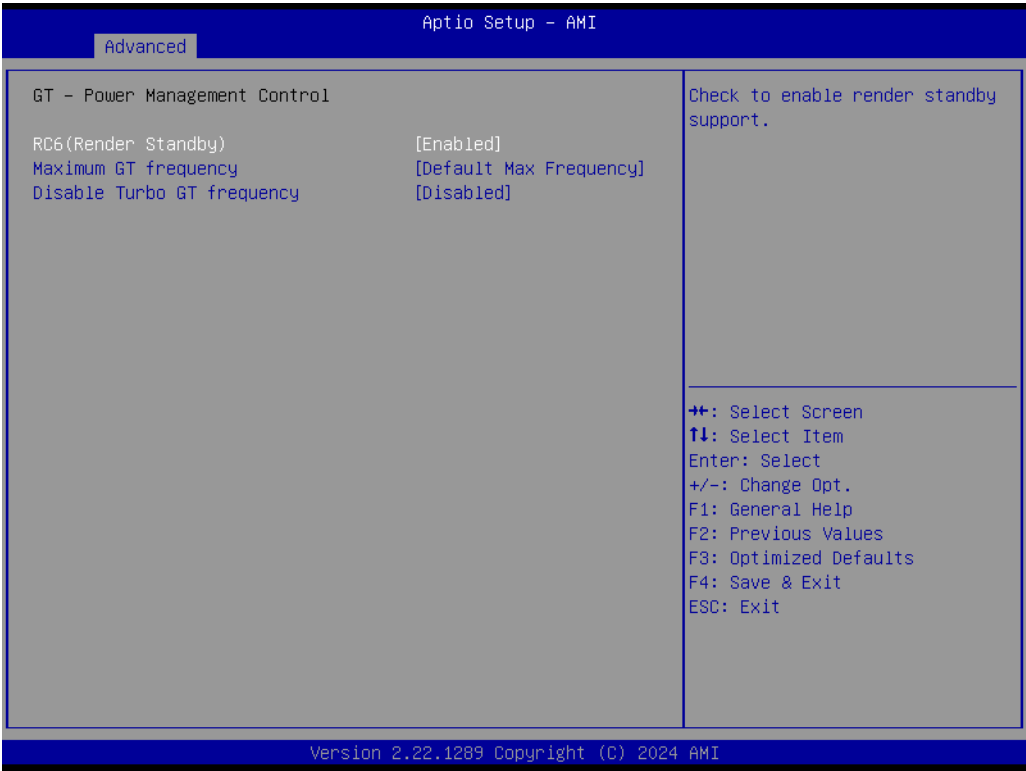
CFG Lock

Advanced → Power & Performance → CPU – Power Management Control → CFG Lock



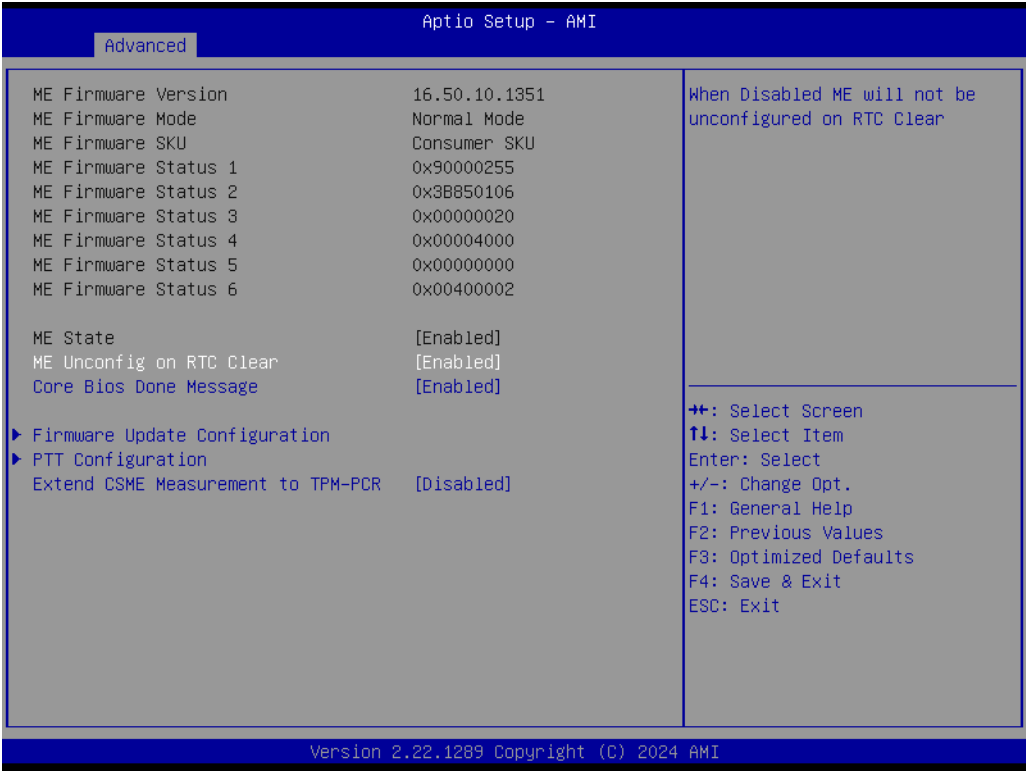
GT – Power Management Control

Advanced → Power & Performance → GT – Power Management Control



3.2.2.3 PCH-FW Configuration

Advanced → PCH-FW Configuration



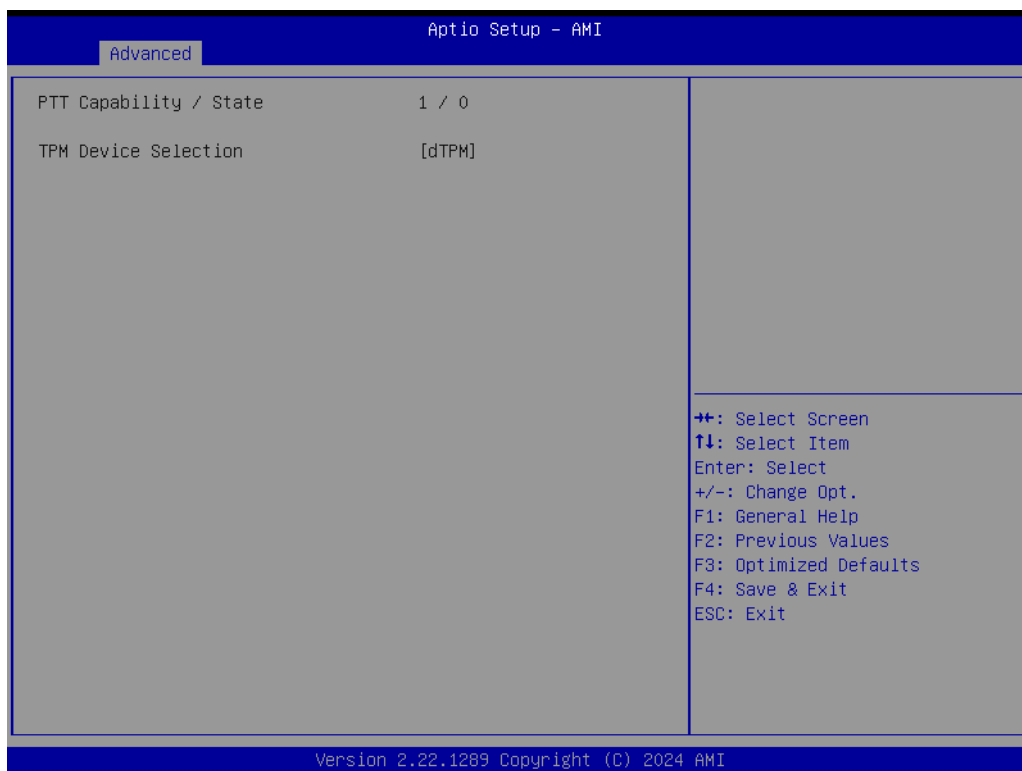
Firmware Update Configuration

Advanced → PCH-FW Configuration → Firmware Update Configuration

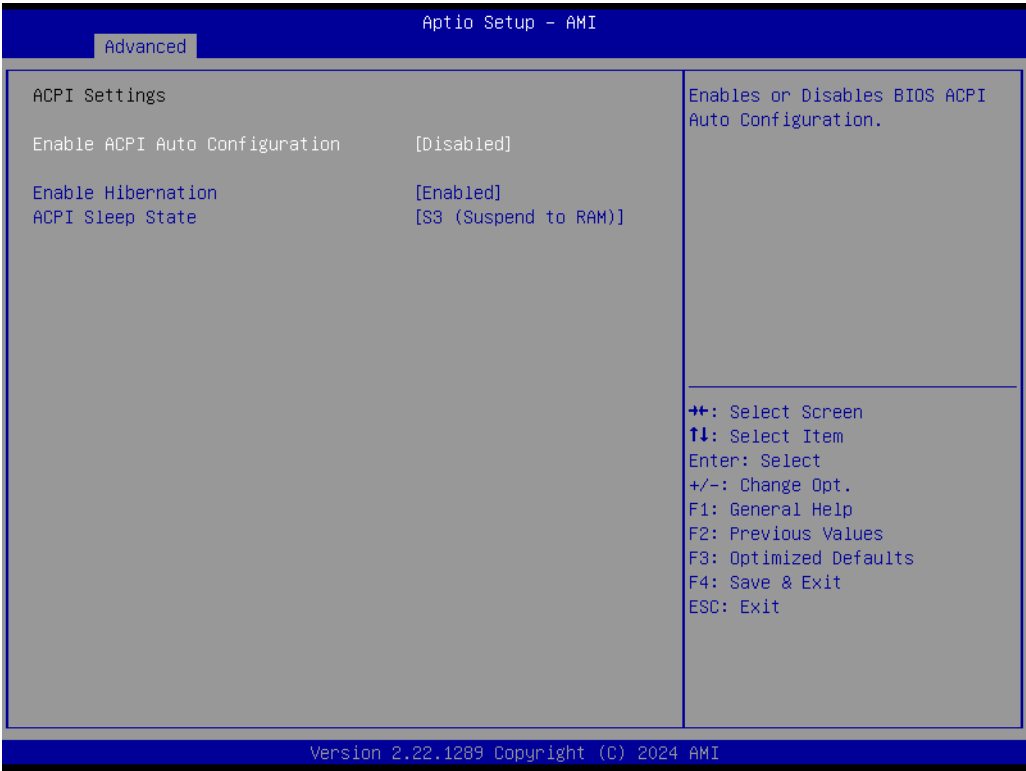


PTT Configuration

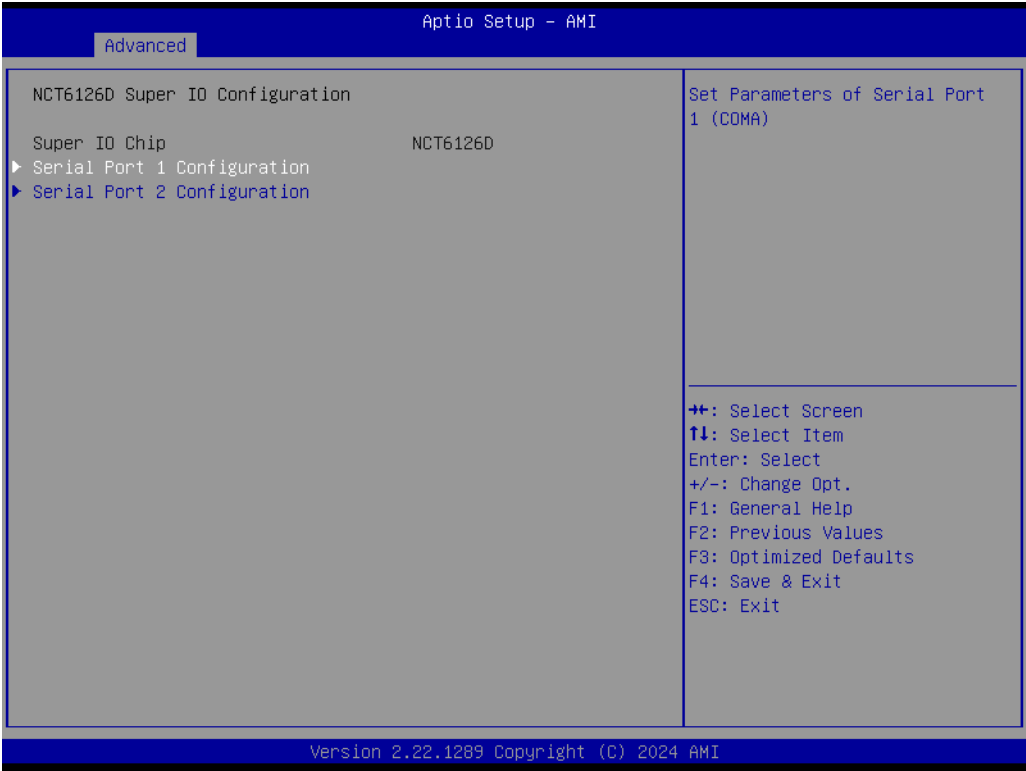
Advanced → PCH-FW Configuration → PTT Configuration



3.2.2.4 **ACPI Settings**
Advanced → ACPI Settings

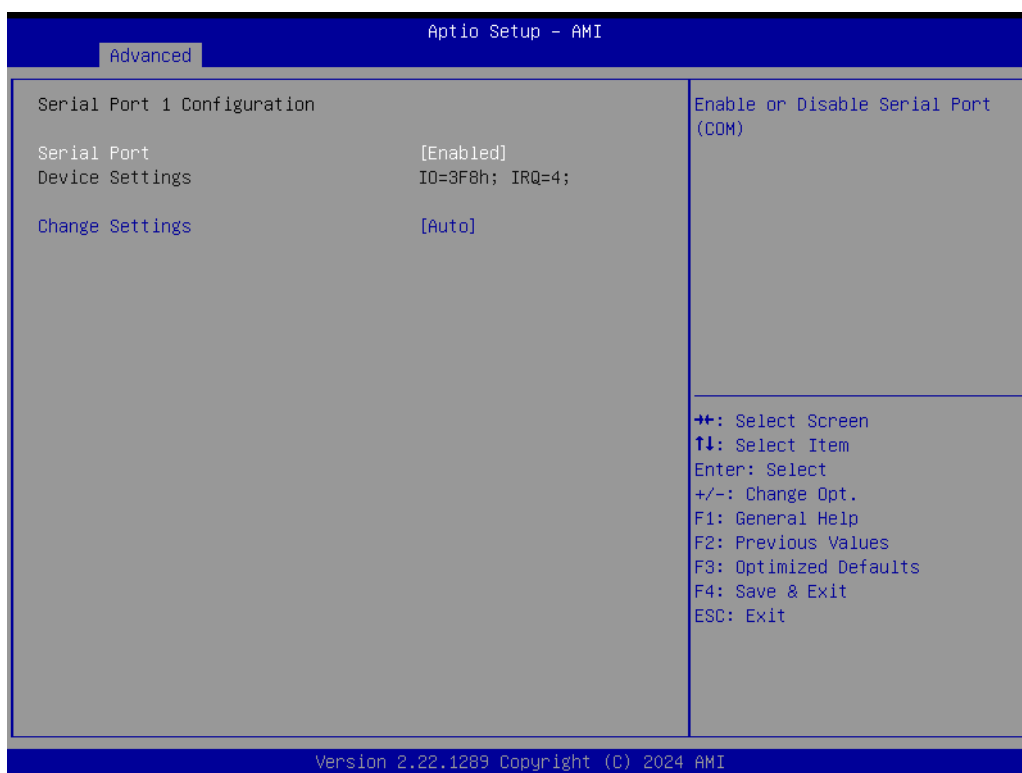


3.2.2.5 **NCT6126D Super IO configuration**
Advanced → NCT6126D Super IO Configuration



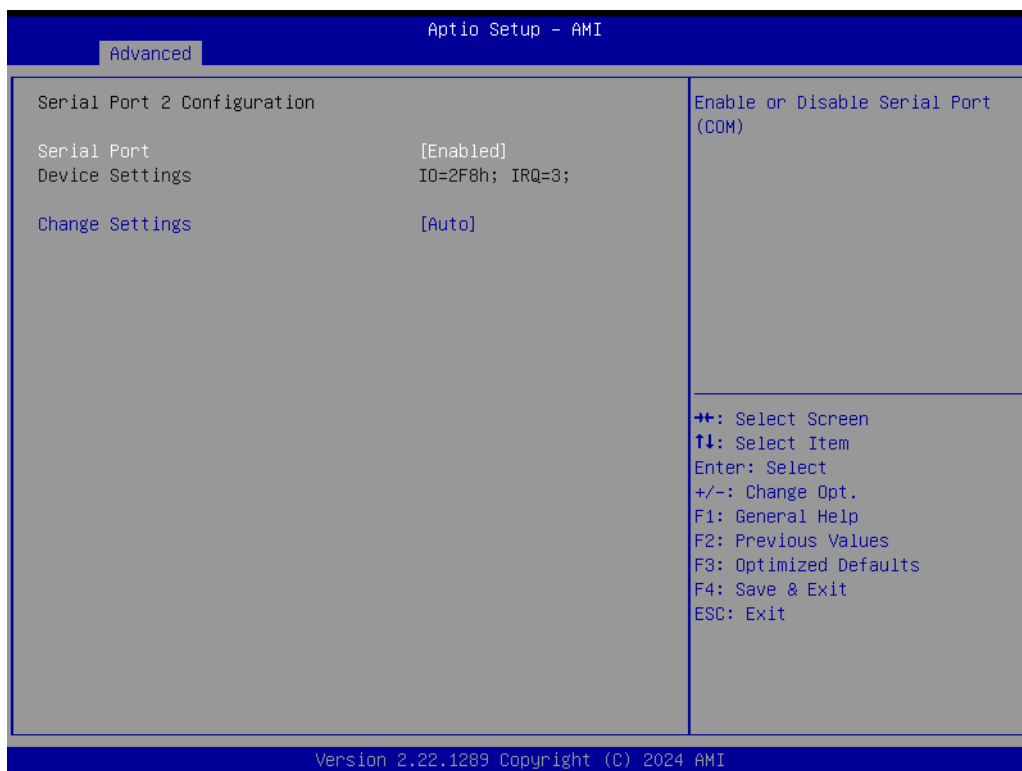
Serial Port 1 Configuration

Advanced → NCT6126D Super IO Configuration → Serial Port 1 Configuration



Serial Port 2 Configuration

Advanced → NCT6126D Super IO Configuration → Serial Port 2 Configuration

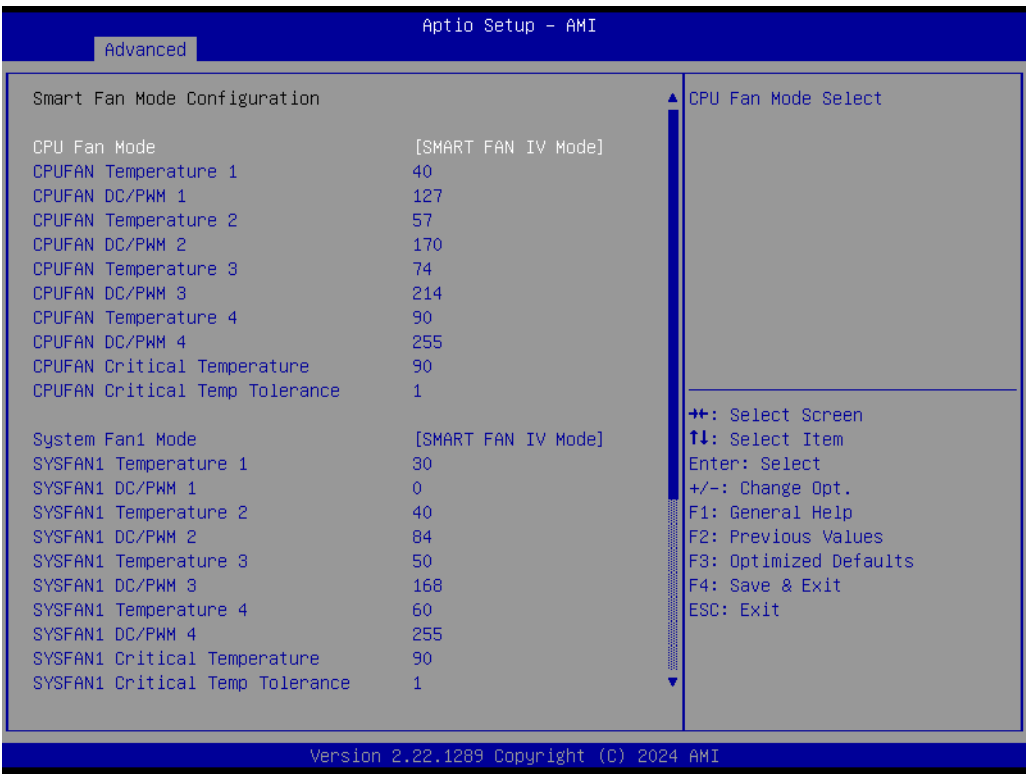
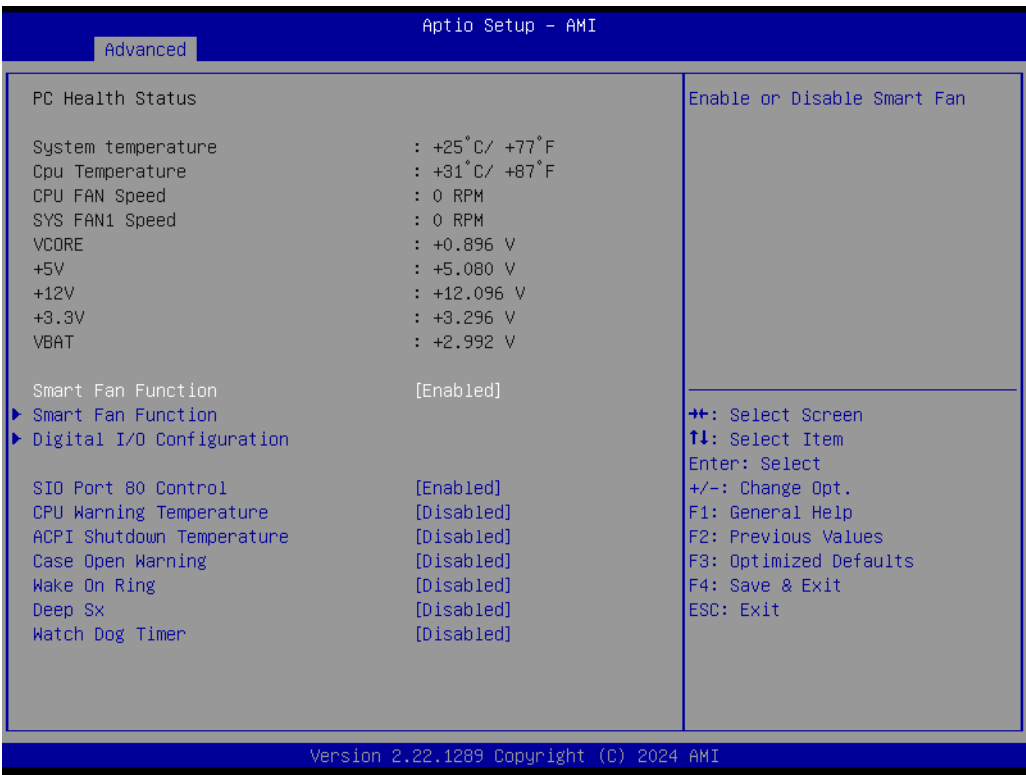


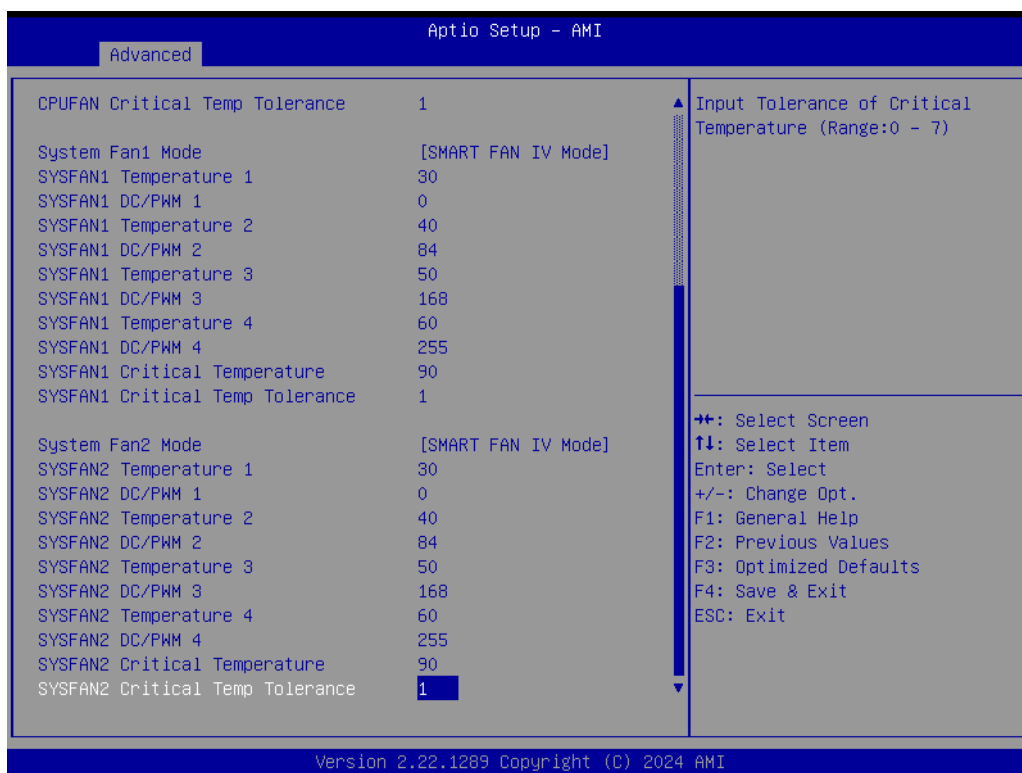
3.2.2.6 NCT6126D HW Monitor

Advanced → NCT6126D HW Monitor

Smart Fan Function

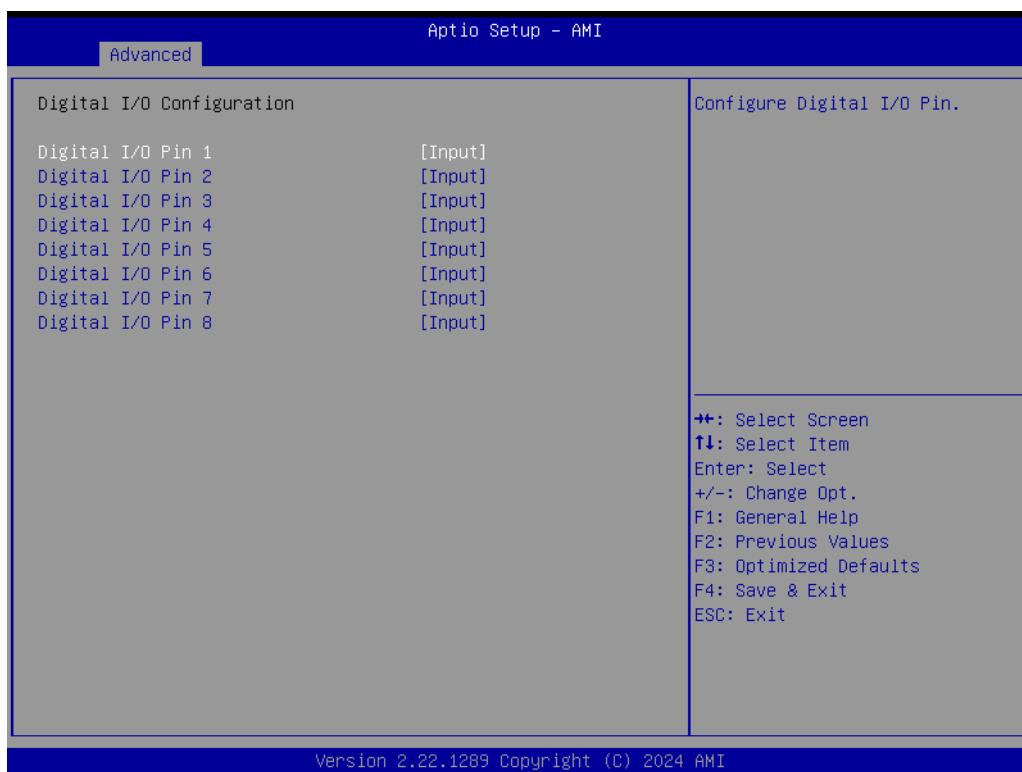
Advanced → NCT6126D HW Monitor → Smart Fan Function





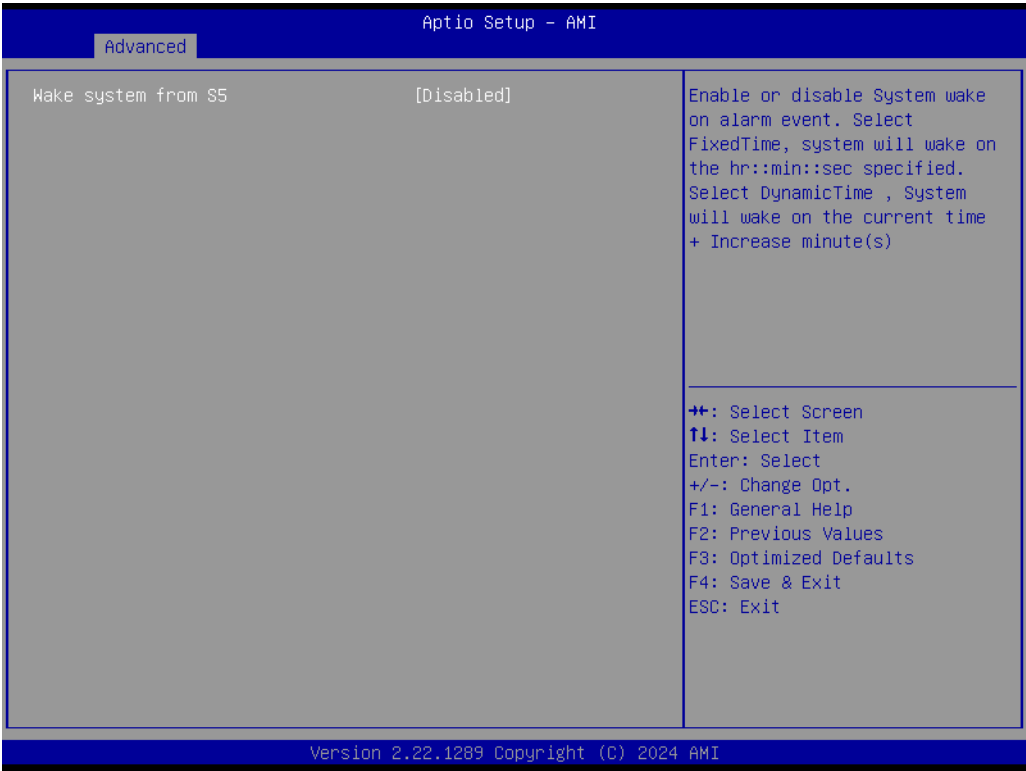
Digital I/O Configuration

Advanced → NCT6126D HW Monitor → Digital I/O Configuration

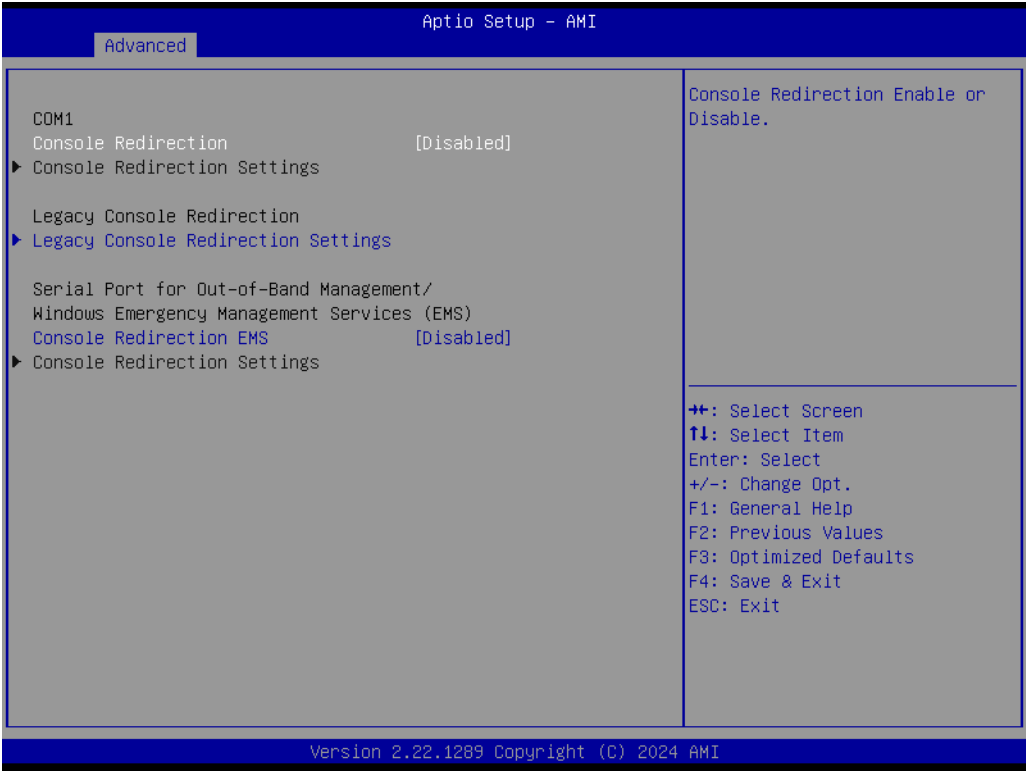


3.2.2.7 S5 RTC Wake Settings

Advanced → S5 RTC Wake Settings

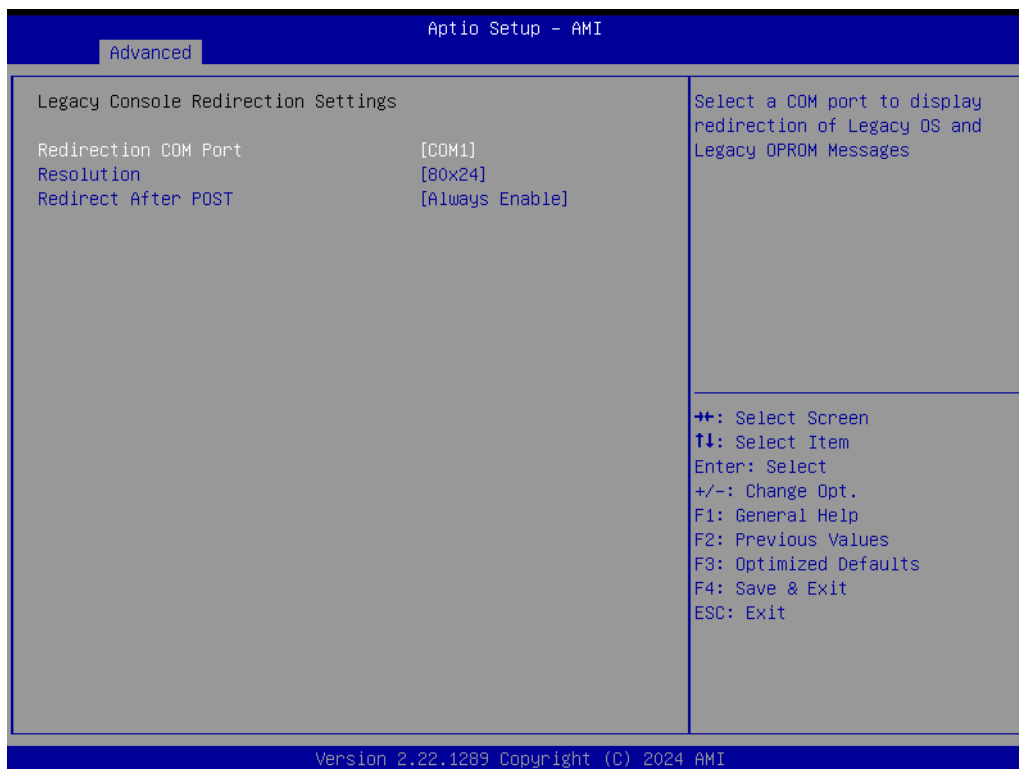


3.2.2.8 Serial Port Console Redirection



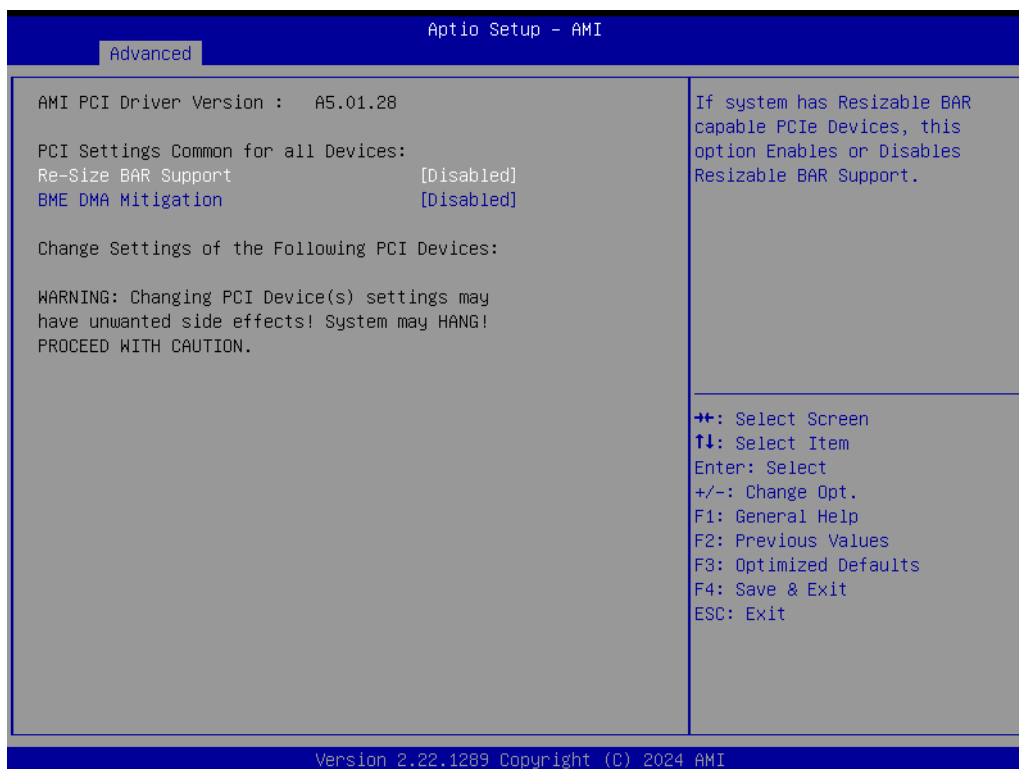
Legacy Console Redirection Settings

Advanced → Serial Port Console Redirection → Legacy Console Redirection Settings

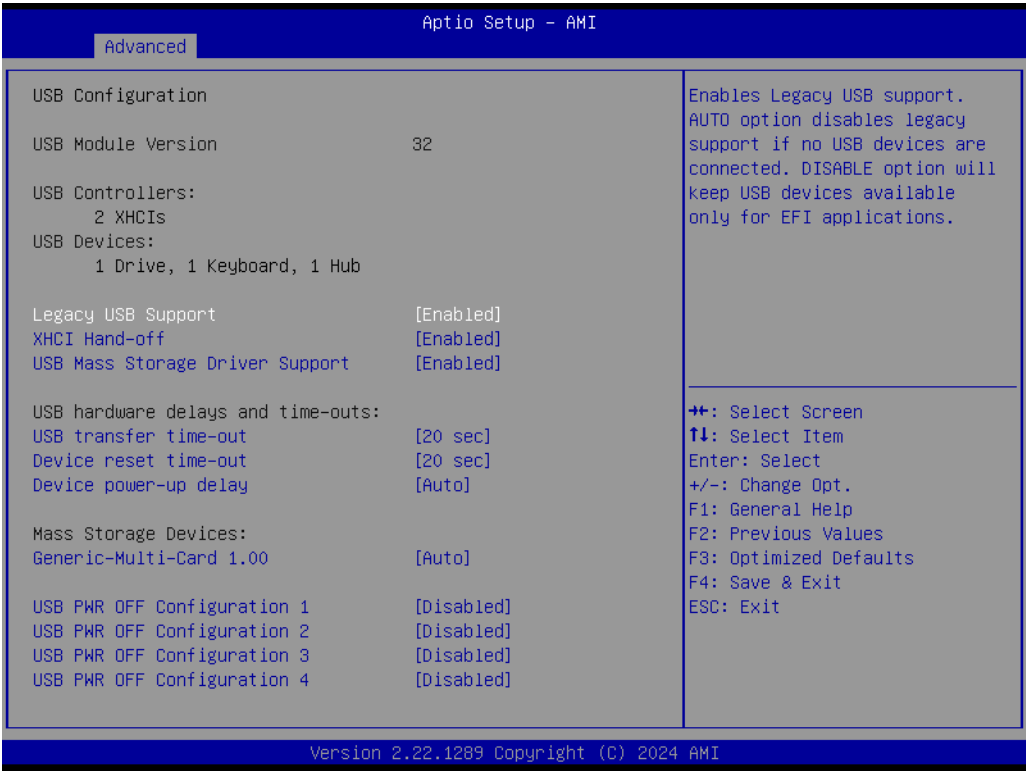


3.2.2.9 PCI Subsystem Settings

Advanced → PCI Subsystem Settings



3.2.2.10 USB Configuration
Advanced → USB Configuration



3.2.2.11 Network Stack Configuration
Advanced → Network Stack Configuration



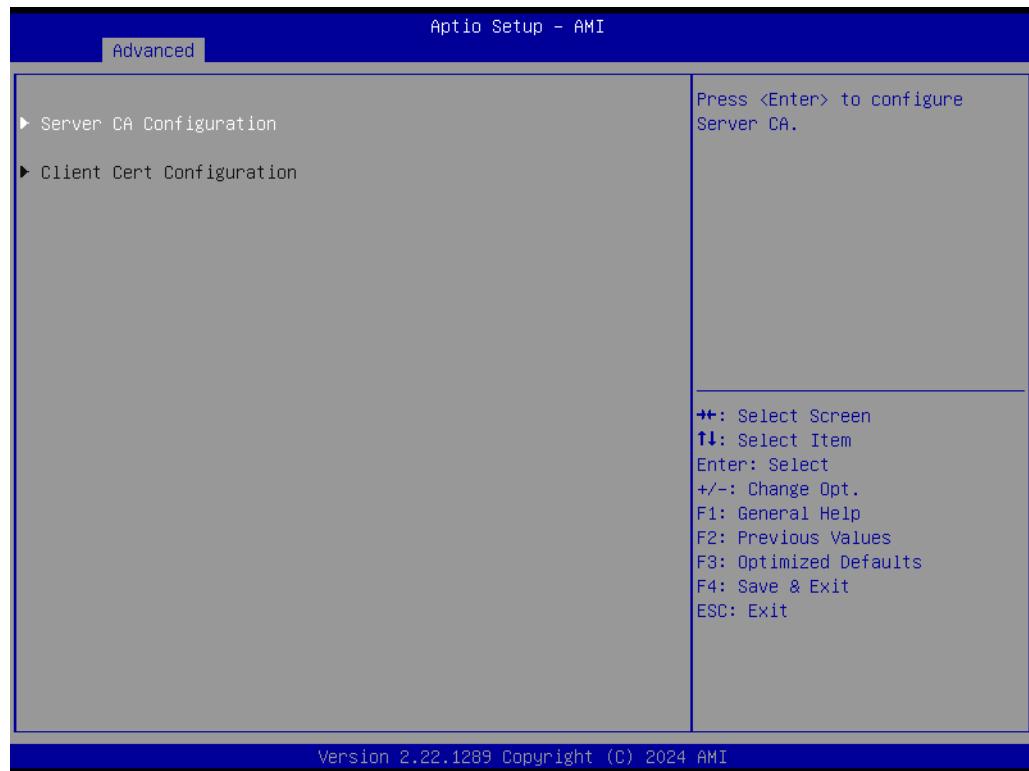
3.2.2.12 NVMe Configuration

Advanced → NVMe Configuration



3.2.3 Chipset Configuration Settings

Select the chipset tab from the BIOS setup screen to enter the Chipset Setup screen. Users can select any item in the left frame of the screen, such as PCI Express Configuration, to go to the sub-menu for that item. Users can display a Chipset Setup option by highlighting it using the <Arrow> keys. All Chipset Setup options are described in this section. The Chipset Setup screens are shown below. The sub-menus are described on the following pages.



3.2.3.1 System Agent (SA) Configuration

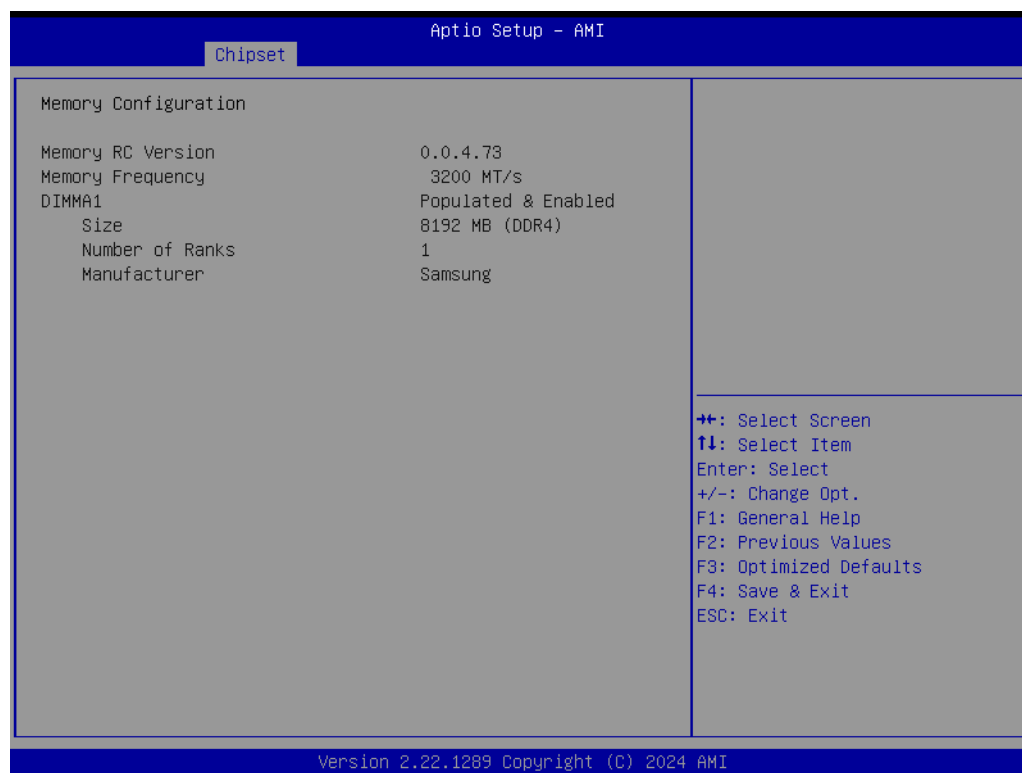
Chipset → System Agent (SA) Configuration



Memory Configuration

Chipset → System Agent (SA) Configuration → Memory Configuration





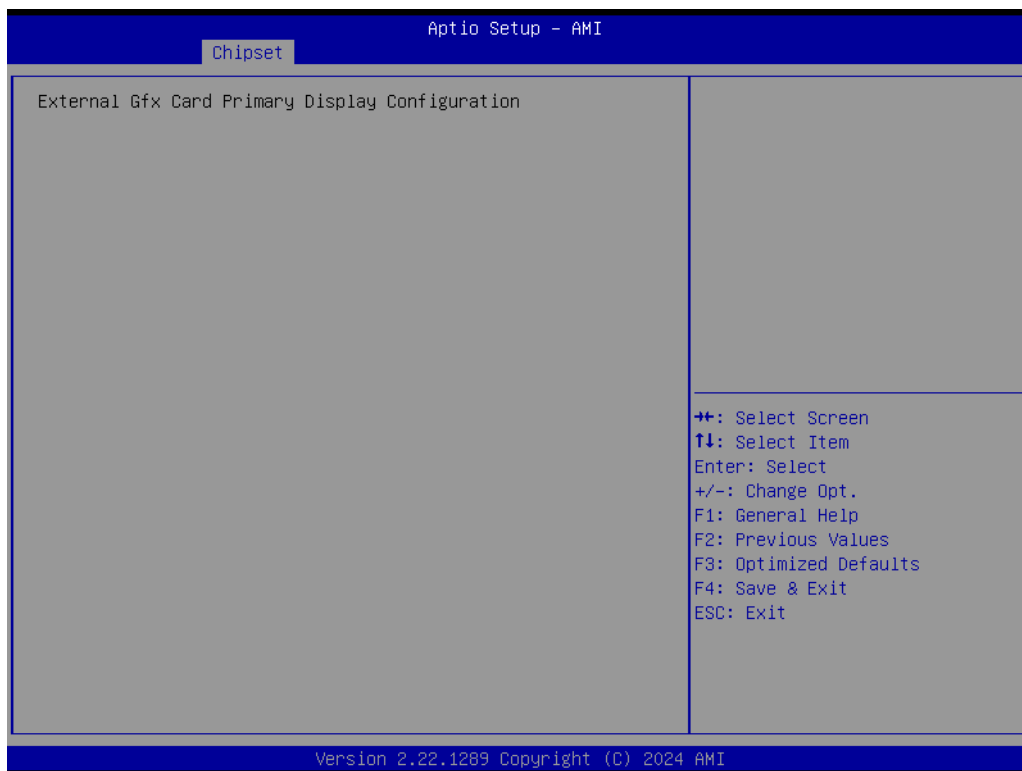
Graphics Configuration

Chipset → System Agent (SA) Configuration → Graphics Configuration



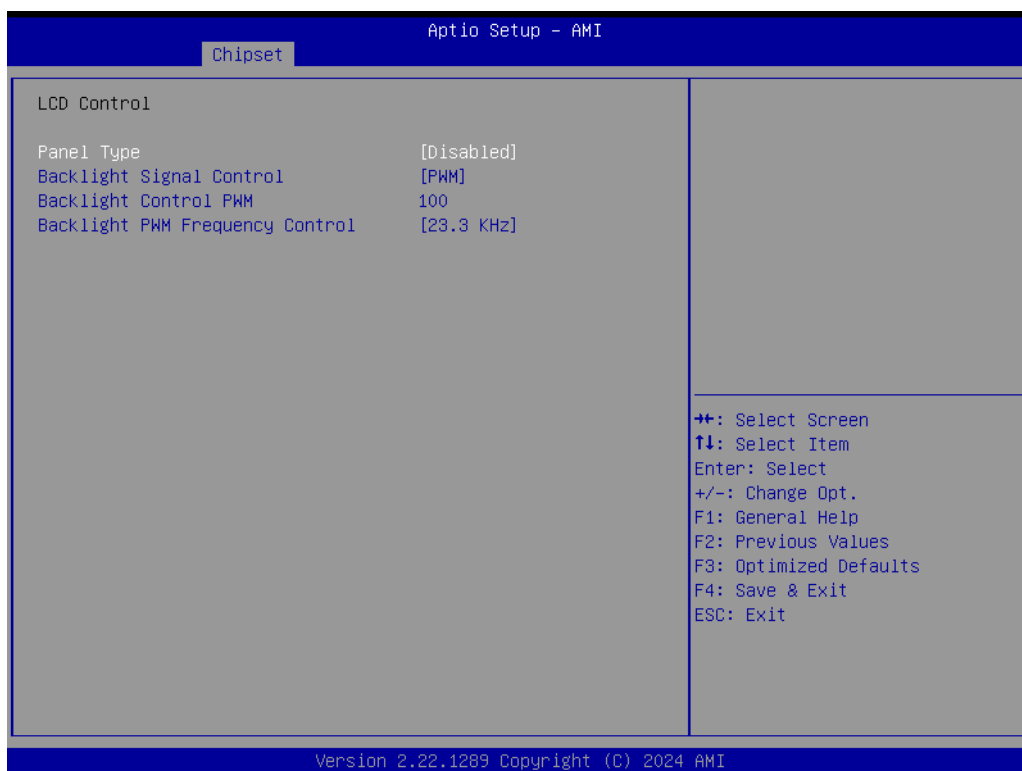
External Gfx Card Primary Display Configuration

Chipset → System Agent (SA) Configuration → Graphics Configuration → External Gfx Card Primary Display Configuration



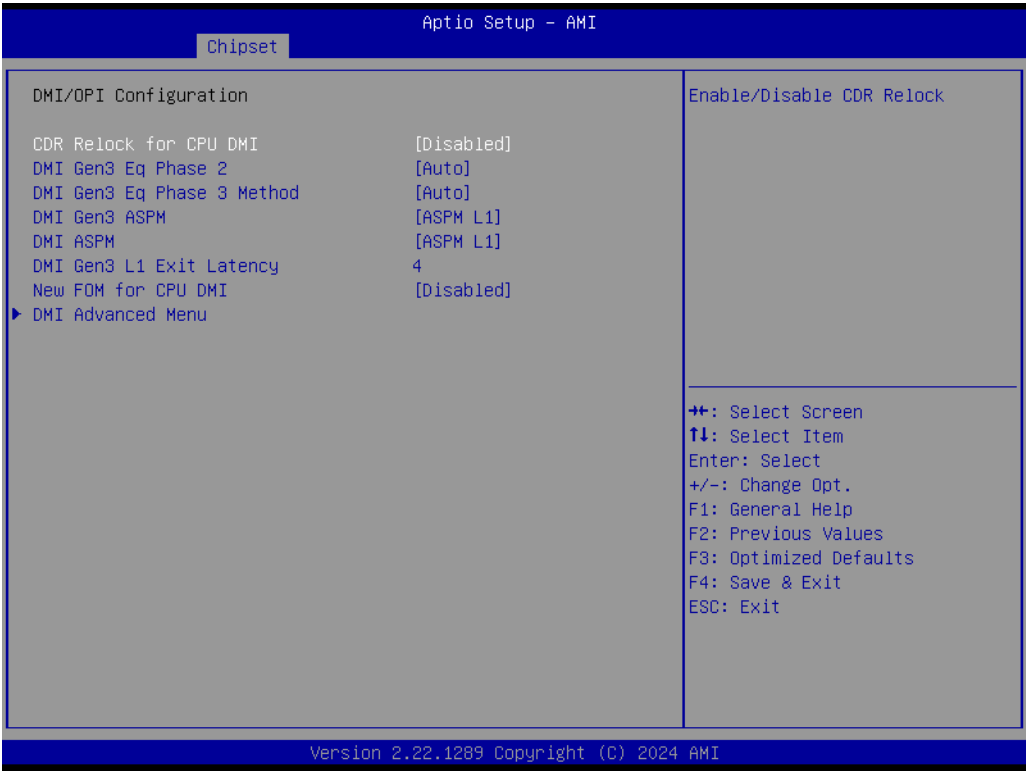
LCD Control

Chipset → System Agent (SA) Configuration → Graphics Configuration → LCD Control



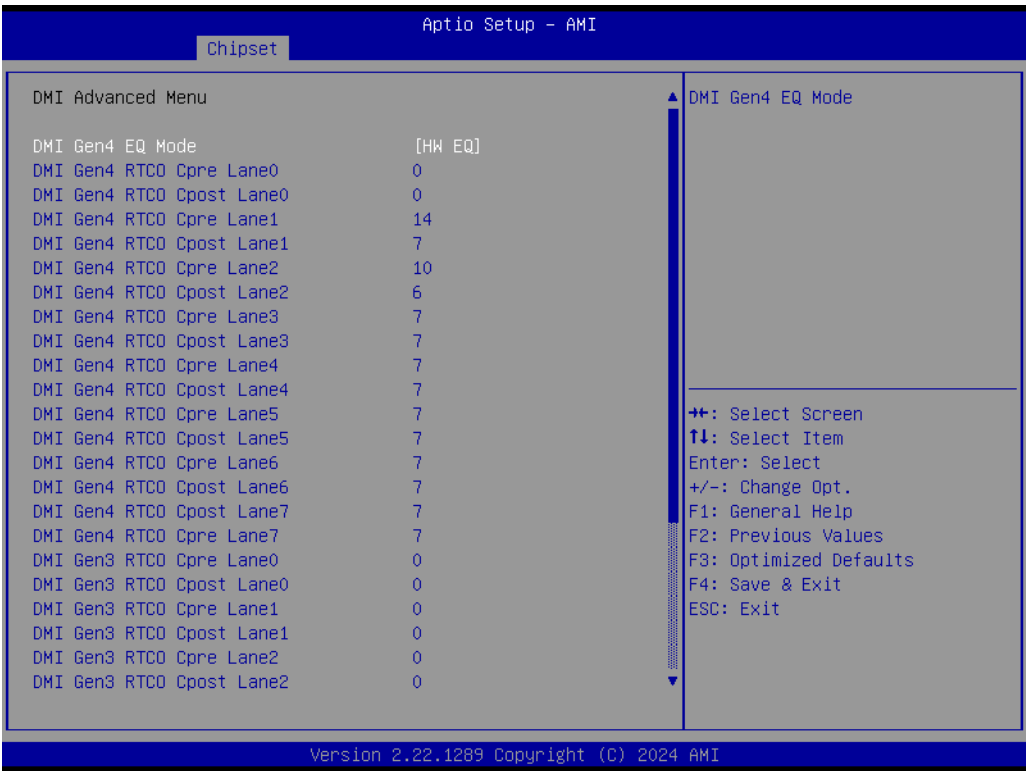
DMI/OPI Configuration

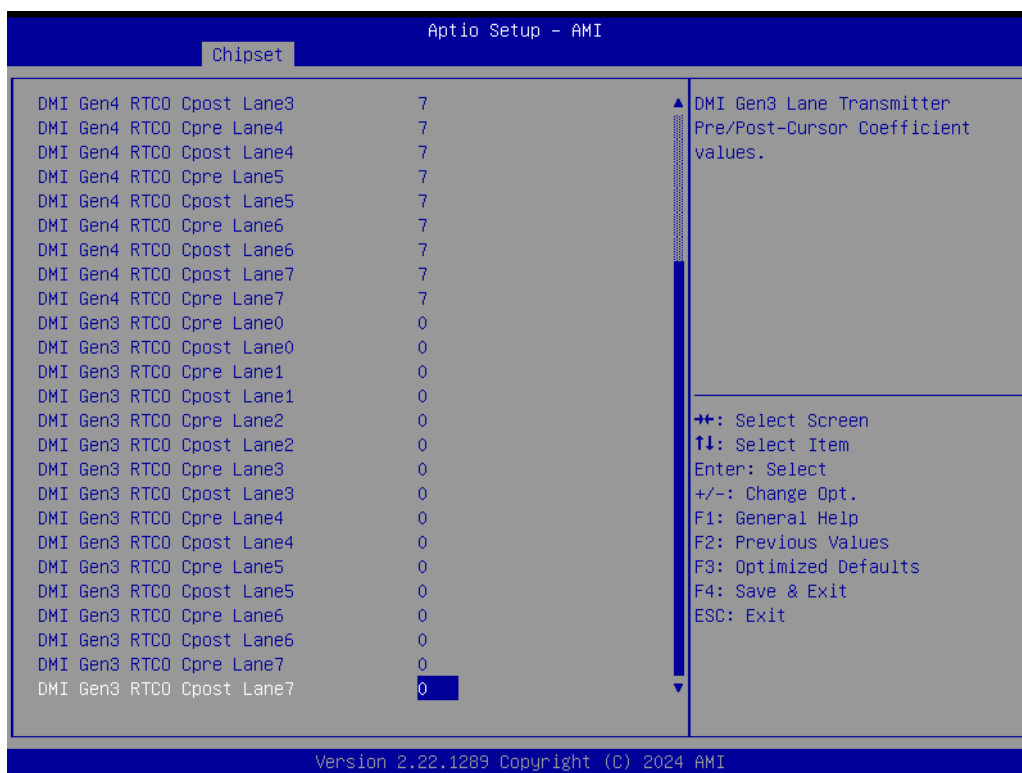
Chipset → System Agent (SA) Configuration → DMI/OPI Configuration



DMI Advanced Menu

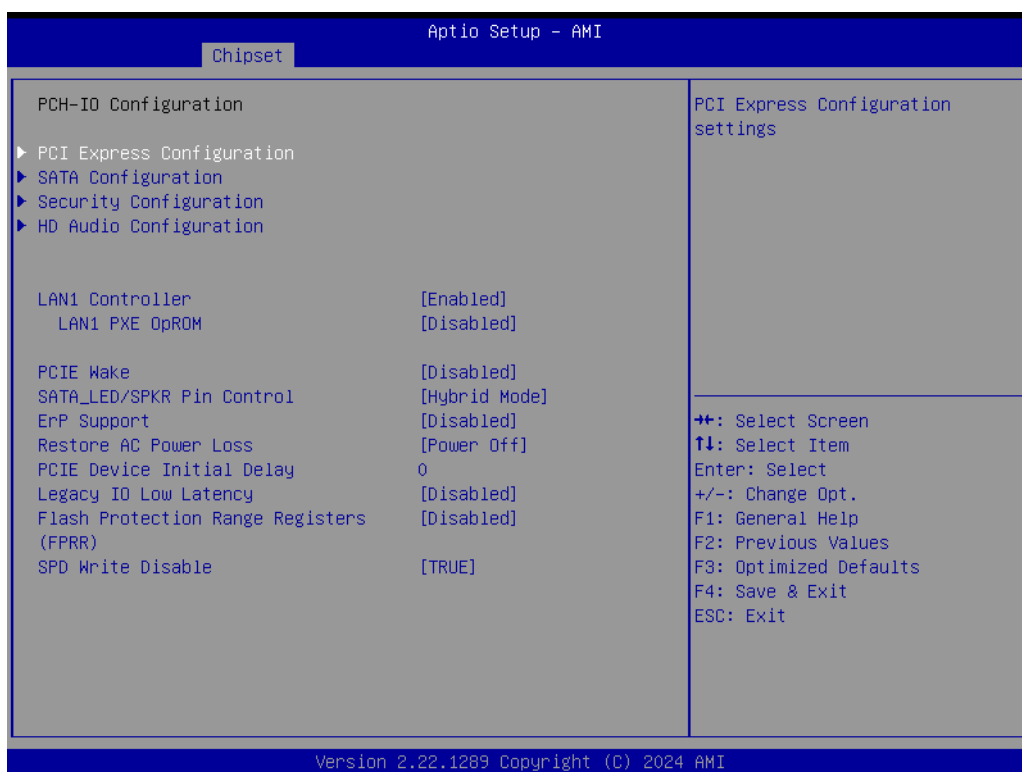
Chipset → System Agent (SA) Configuration → DMI/OPI Configuration → DMI Advanced Menu





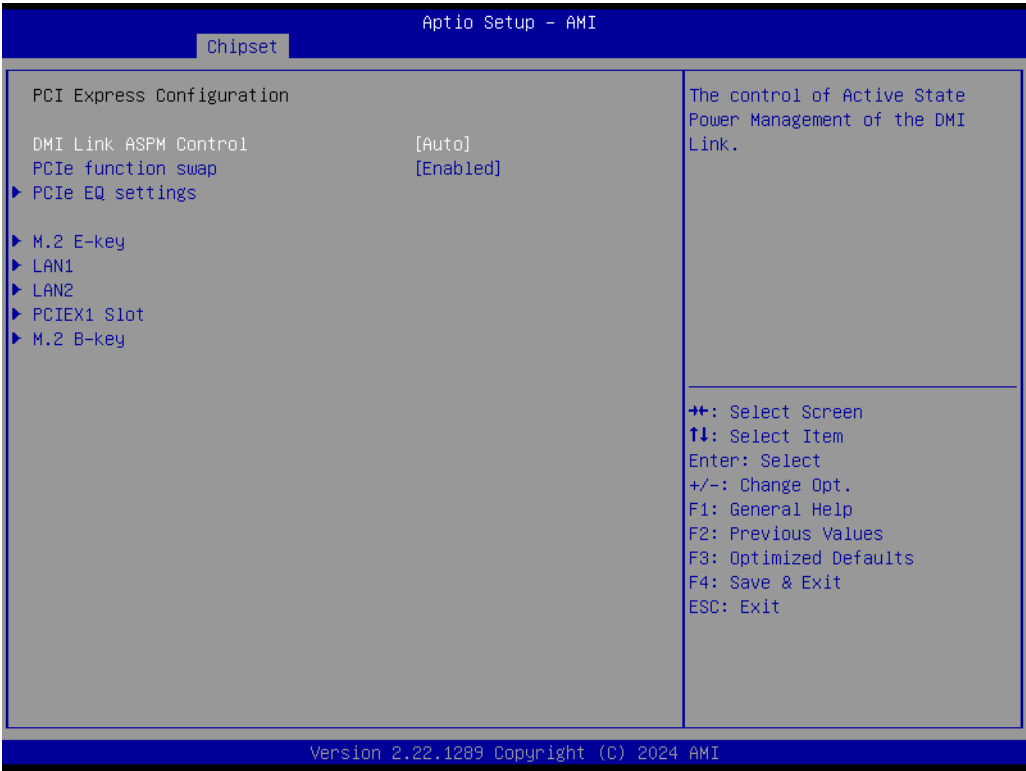
3.2.3.2 PCH-I/O Configuration

Chipset → PCH-IO Configuration



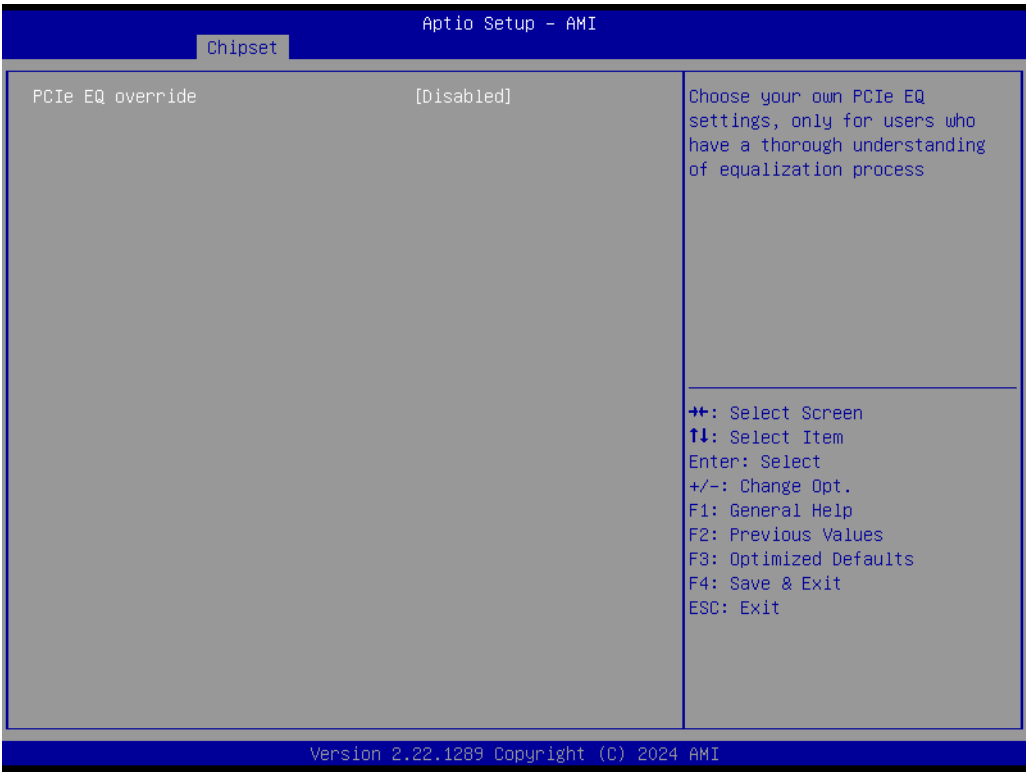
PCI Express Configuration

Chipset → PCH-IO Configuration → PCI Express Configuration



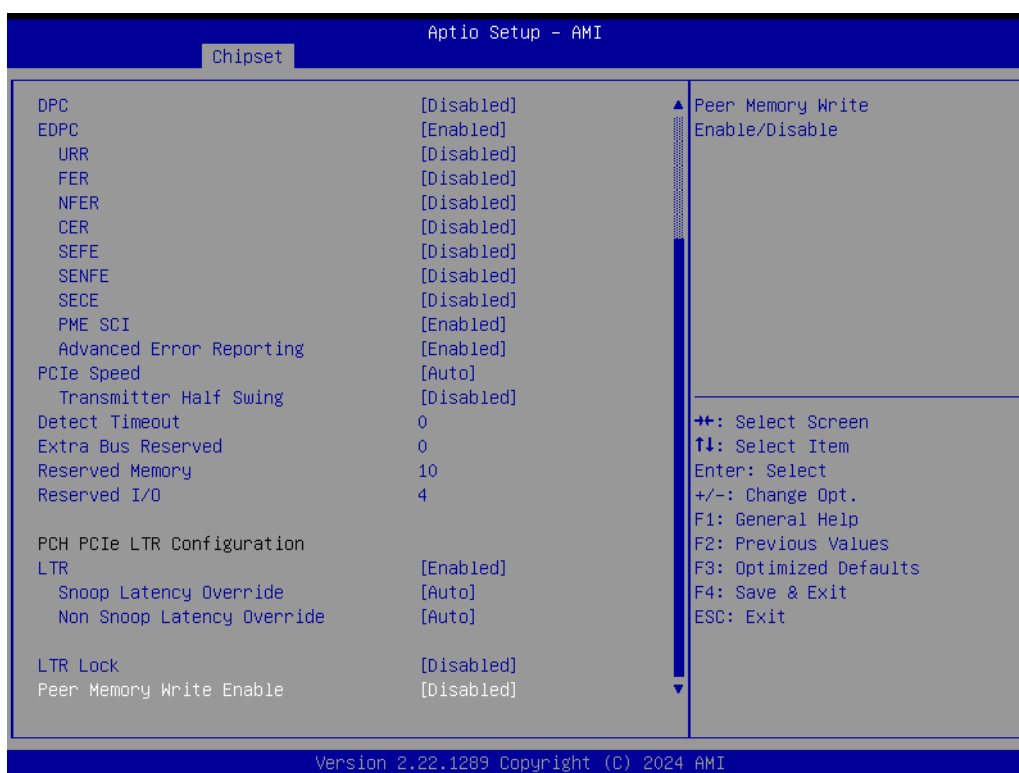
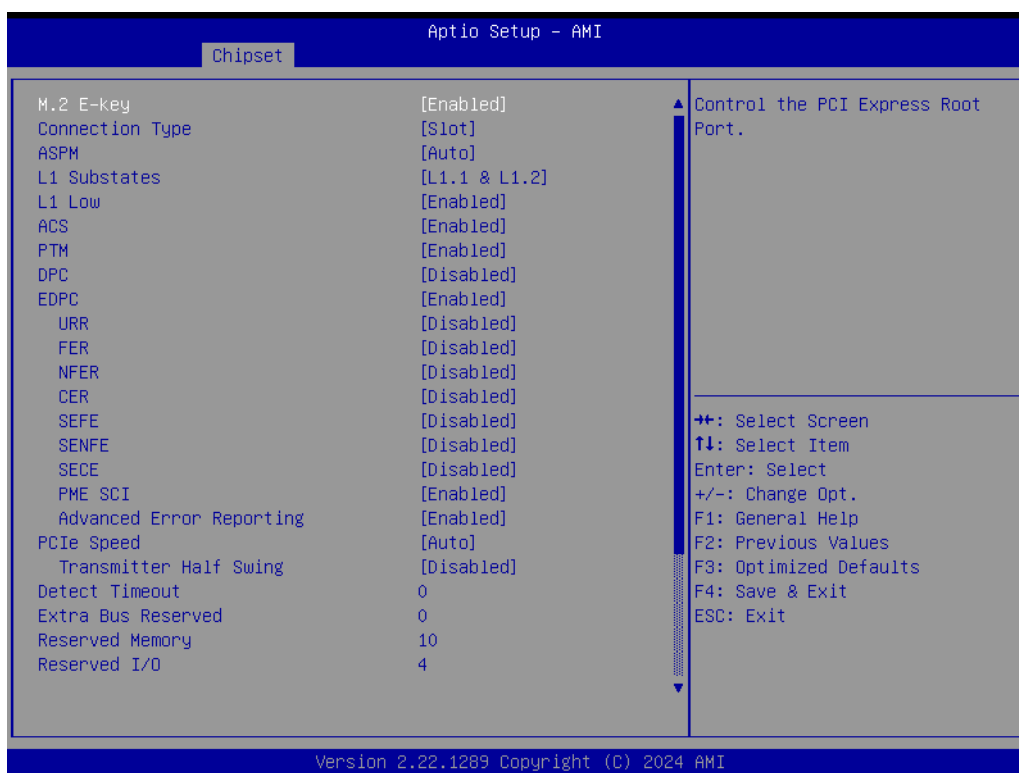
PCIe EQ Settings

Chipset → PCH-IO Configuration → PCI Express Configuration → PCIe EQ Settings



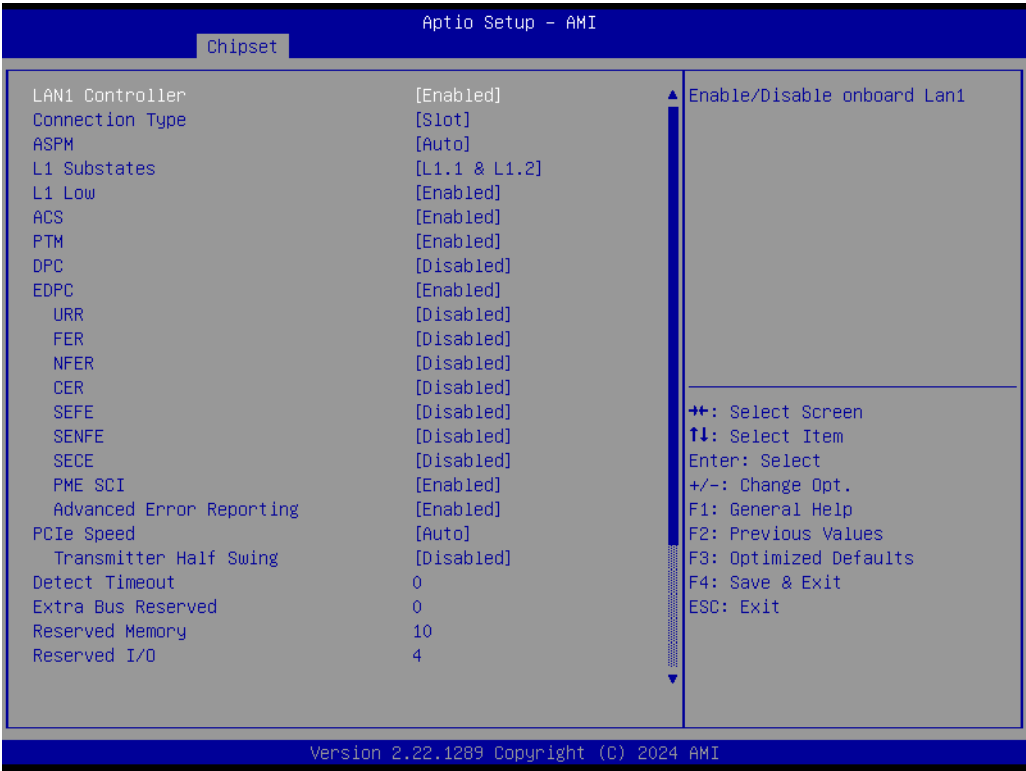
M.2 E-Key

Chipset → PCH-IO Configuration → PCI Express Configuration → M.2 E-Key



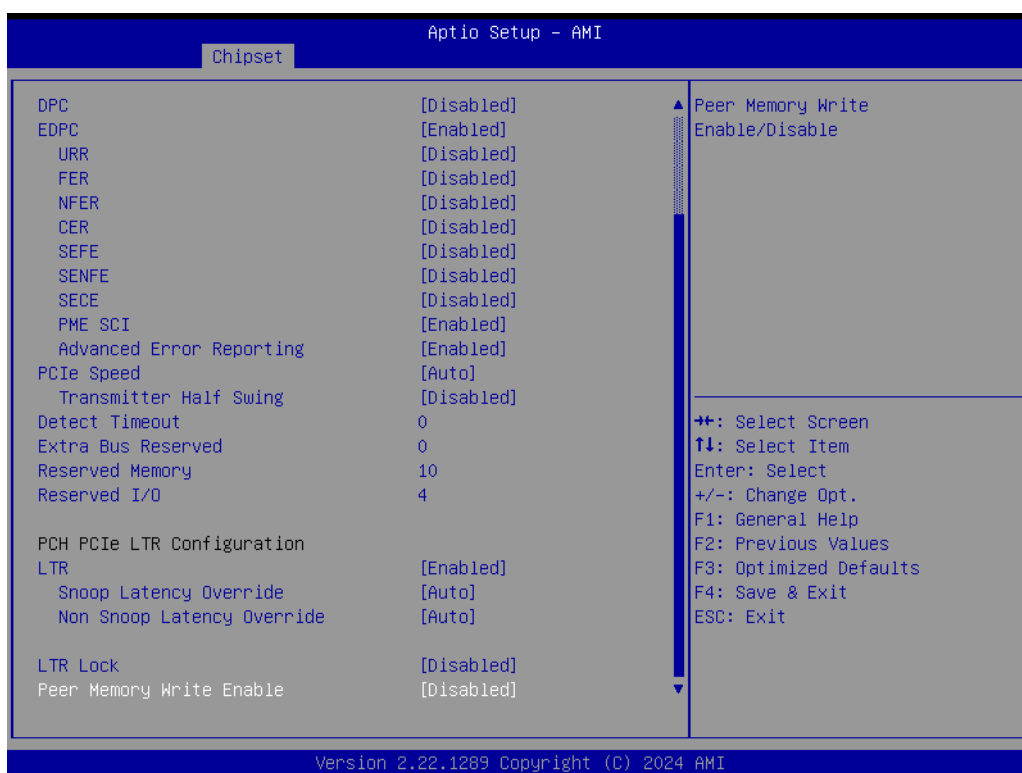
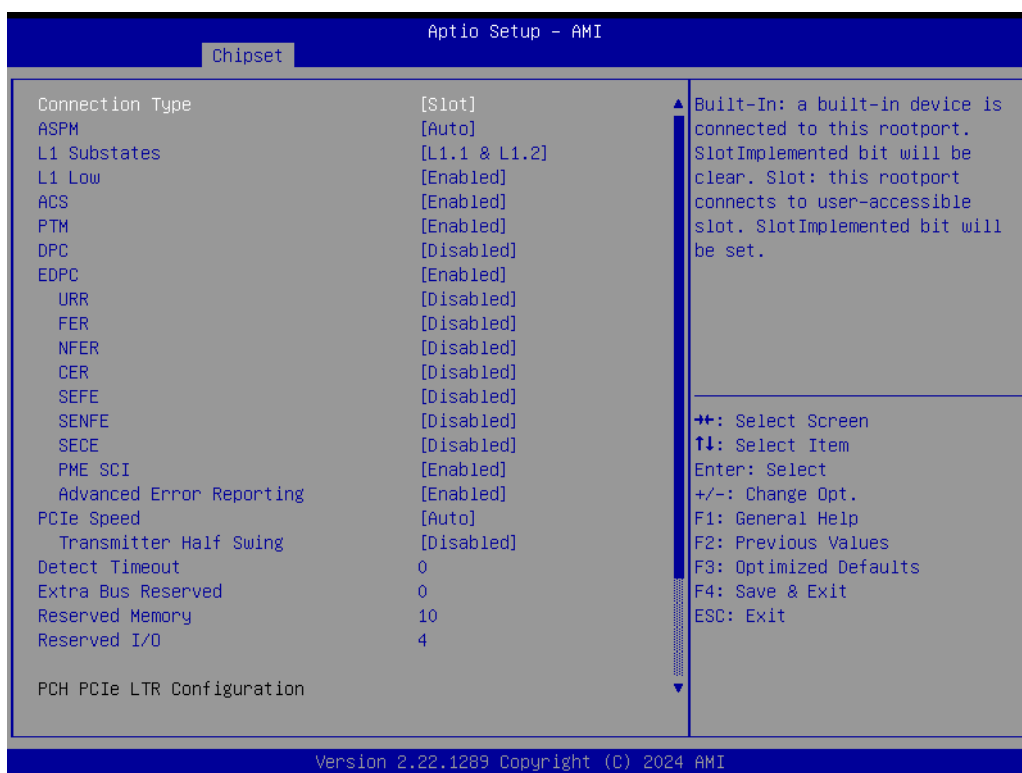
LAN 1

Chipset → PCH-IO Configuration → PCI Express Configuration → LAN1



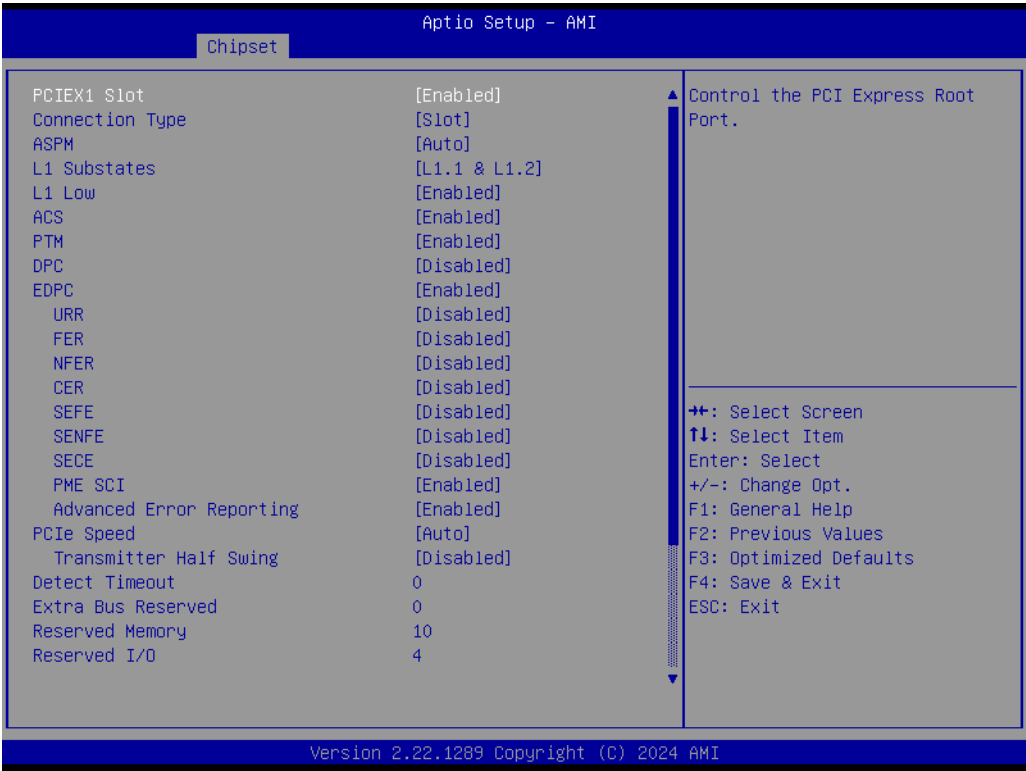
LAN 1

Chipset → PCH-IO Configuration → PCI Express Configuration → LAN2



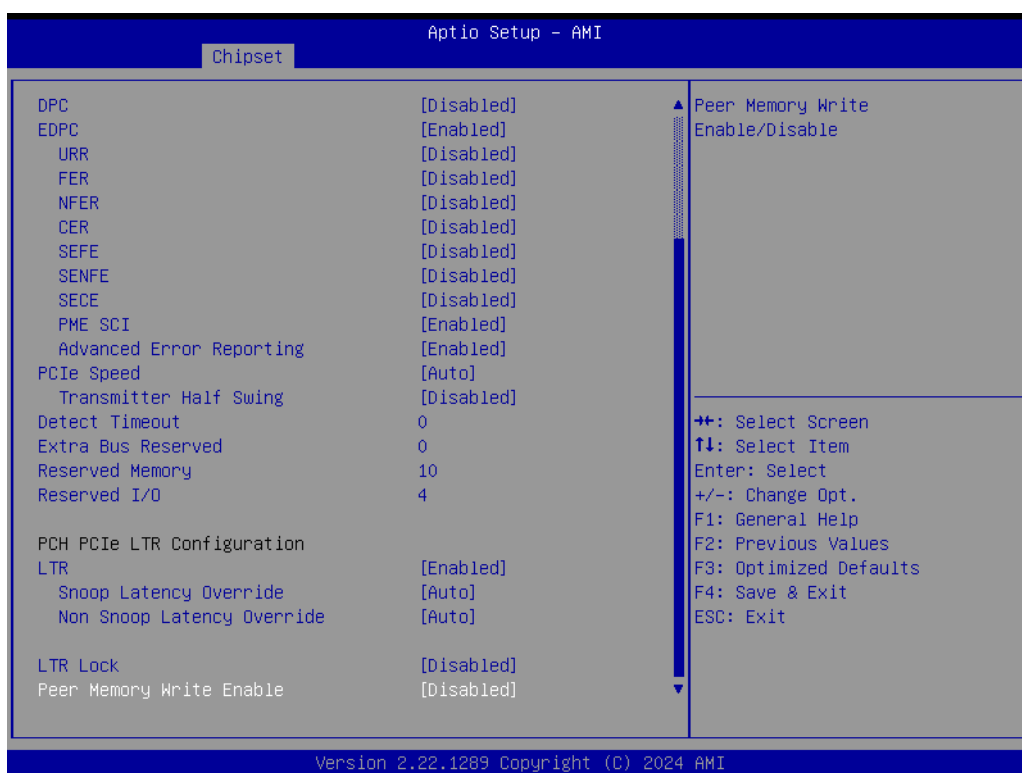
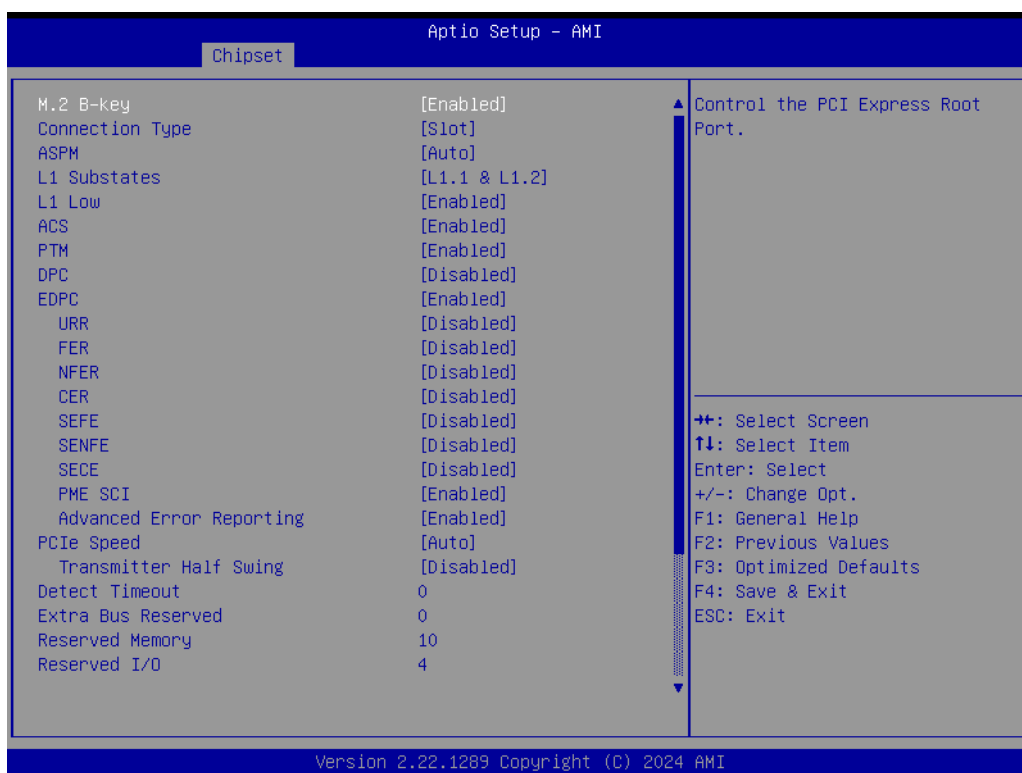
PCle x1 Slot

Chipset → PCH-IO Configuration → PCI Express Configuration → PCIe x1 Slot



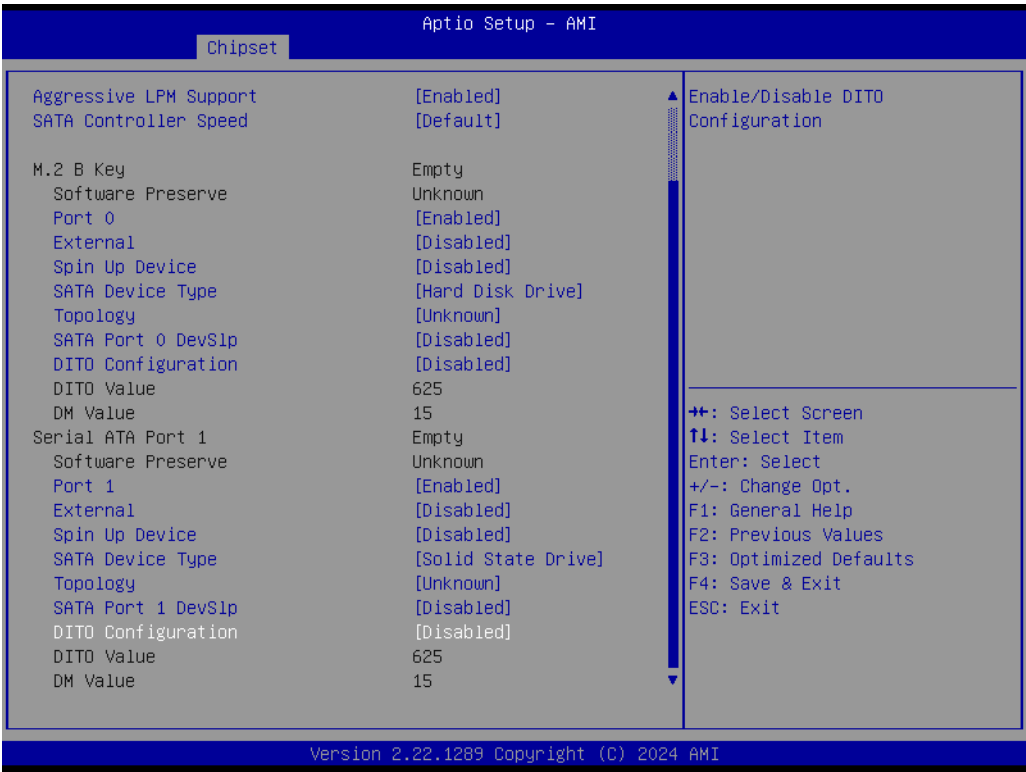
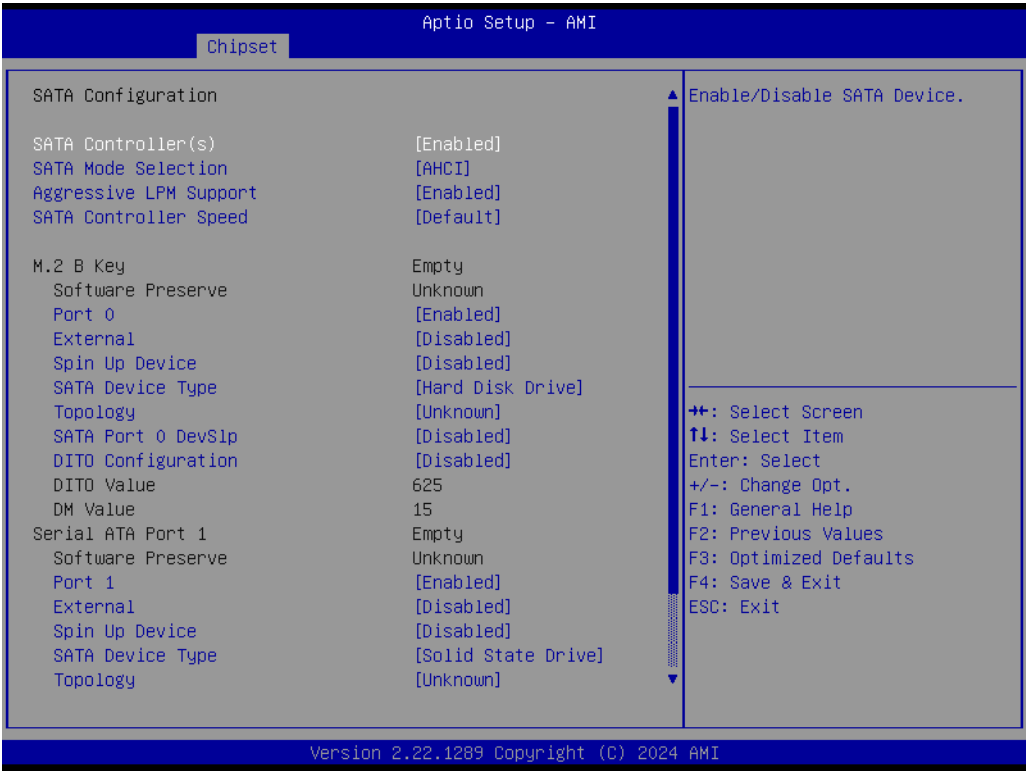
M.2 B-Key

Chipset → PCH-IO Configuration → PCI Express Configuration → M.2 B-Key



SATA Configuration

Chipset → PCH-IO Configuration → SATA Configuration



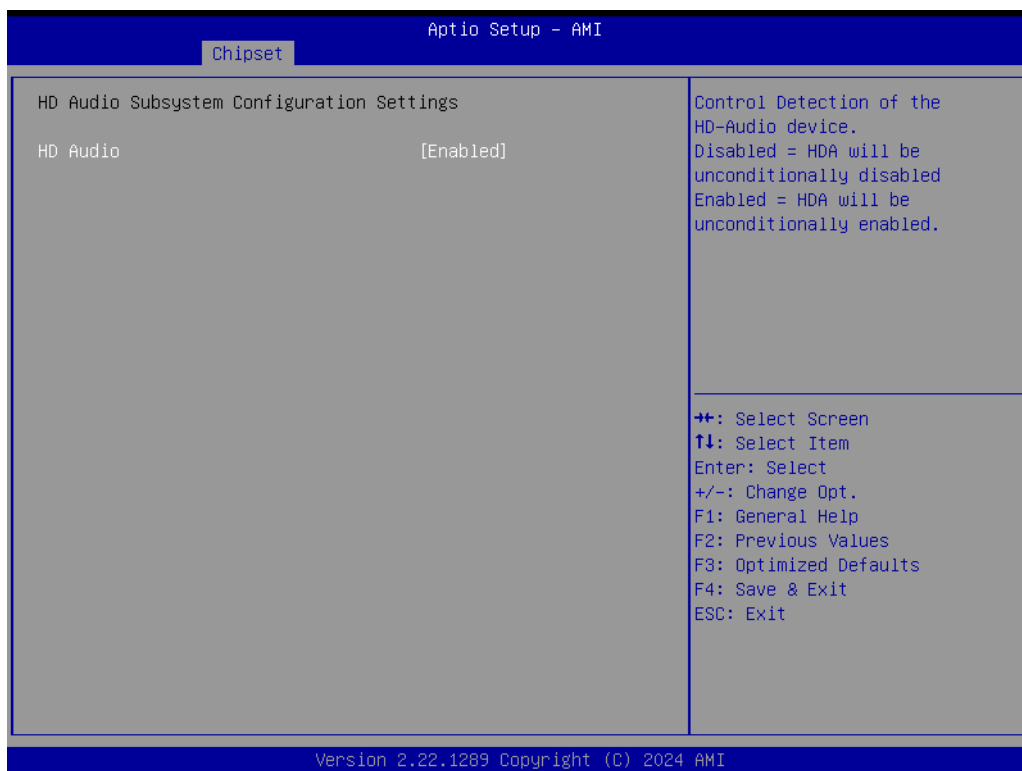
Security Configuration

Chipset → PCH-IO Configuration → Security Configuration

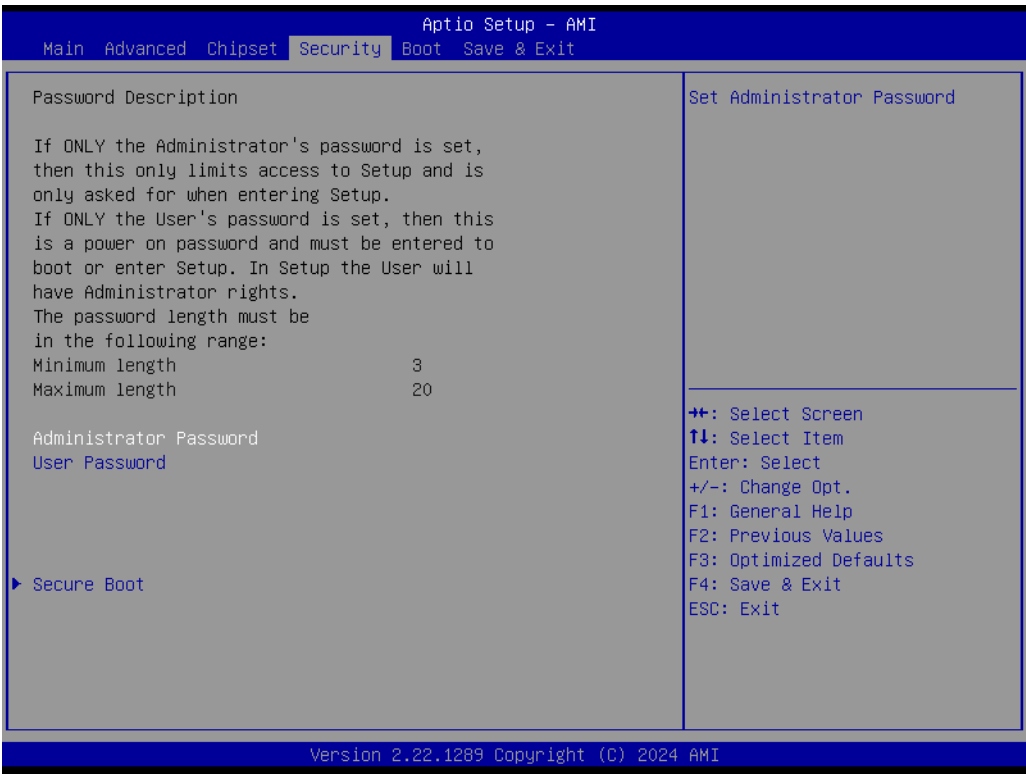


HD Audio Subsystem Configuration Settings

Chipset → PCH-IO Configuration → HD Audio Subsystem Configuration Settings

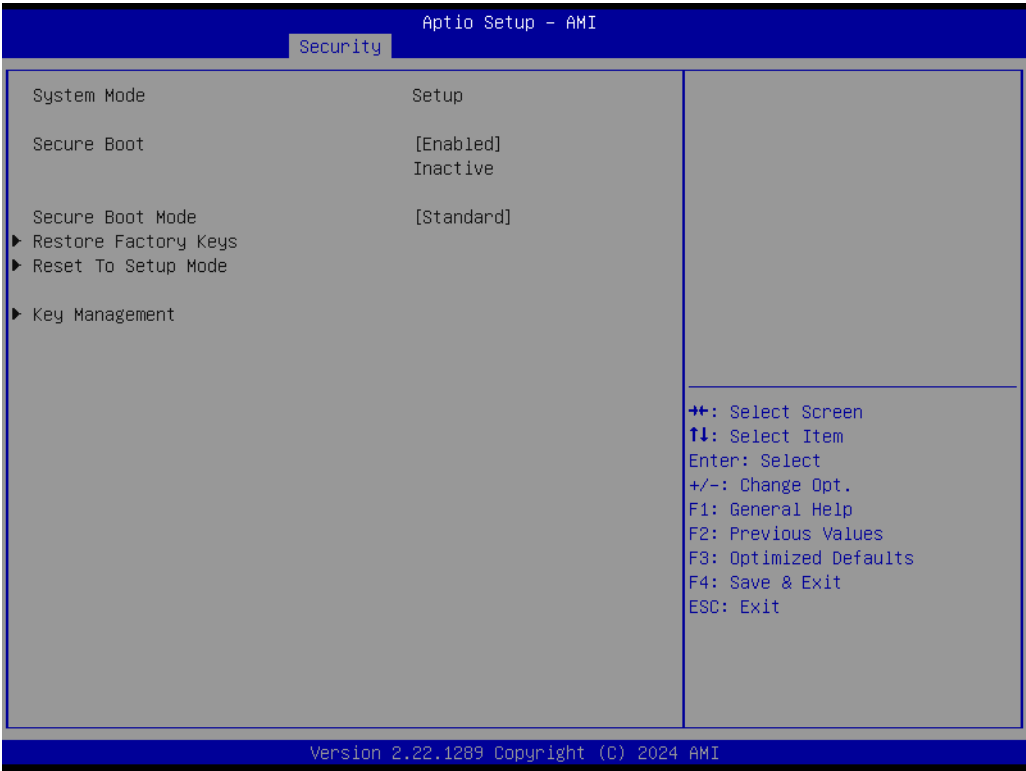


3.2.4 Security

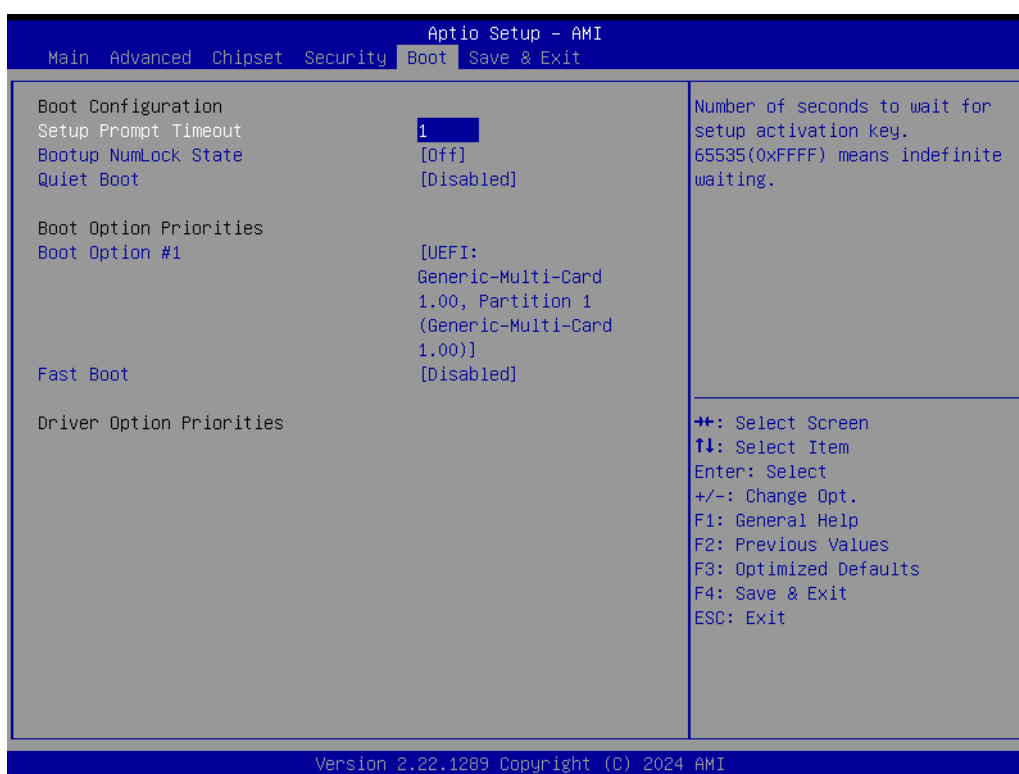


Secure Boot

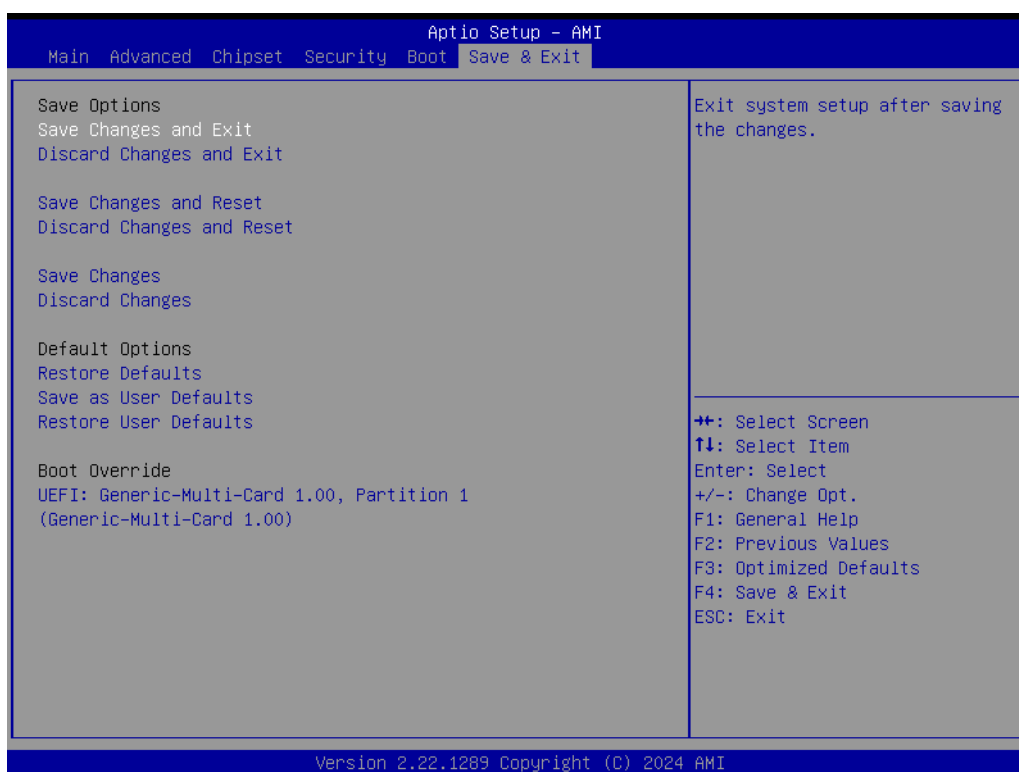
Security → Secure Boot



3.2.5 Boot Settings



3.2.6 Save & Exit Configuration



Chapter 4

Software Introduction
& Services

4.1 Introduction

The mission of Advantech Embedded Software Services is to “Enhance quality of life with Advantech platforms and Microsoft® Windows® embedded technology.” We enable Windows Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows Embedded Software solutions easily and widely available to the embedded computing community.

4.2 Value-Added Software Services

Software API: An interface that defines the ways by which an application program may request services from libraries and/or operating systems. It provides not only the underlying drivers required but also a rich set of user-friendly, intelligent and integrated interfaces, which speeds development, enhances security and offers add-on value for Advantech platforms. It plays the role of catalyst between developer and solution, and makes Advantech embedded platforms easier and simpler to adopt and operate with customer applications.

4.2.1 Software API

4.2.1.1 Control

GP I/O



General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch the device on/off. Our API also provides programmable GPIO which allows developers to dynamically set the GPIO input or output status.

SMBus



SMBus is the System Management Bus which was defined by Intel Corporation in 1995. It is used in personal computers and servers for low-speed system management communications. The SMBus API allows a developer to interface with an embedded system environment and transfer serial messages using the SMBus protocols, allowing simultaneous control of multiple devices.

4.2.1.2 Display

Brightness Control



The Brightness Control API allows a developer to access embedded devices and easily control brightness.

Backlight



The Backlight API allows a developer to control the backlight (screen) on/off in embedded devices.

4.2.1.3 Monitor

Watchdog



A watchdog timer (WDT) is a device that performs a specific operation after a certain period of time if something goes wrong and the system does not recover on its own. A watchdog timer can be programmed to perform a warm boot (restarting the system) after a certain number of seconds.

Hardware Monitor



The Hardware Monitor (HWM) API is a system health supervision API that inspects certain condition indexes, such as fan speed, temperature, and voltage.

4.2.1.4 Power Saving

CPU Speed



This makes use of Intel® SpeedStep® BIOS technology to save power. The system will automatically adjust the CPU speed depending on the system loading.

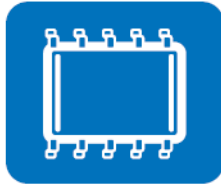
System Throttling



This refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. This API allows the user to adjust the clock from 87.5% to 12.5%.

4.2.2 Software Utilities

BIOS Flash



The BIOS Flash utility allows customers to update the flash ROM BIOS version or use it to back up the current BIOS by copying it from the flash chip to a file on the customer's disk. The BIOS Flash utility also provides a command line version and an API for fast implementation into customized applications.

Embedded Security ID



The embedded application is the most important property of a system integrator. It contains valuable intellectual property, design knowledge, and innovation, but this makes it vulnerable! The Embedded Security ID utility provides reliable security functions for customers to secure their application data within the embedded BIOS.

Monitoring



Monitoring is a utility for customers to monitor system health parameters such as voltage, CPU and system temperature, and fan speed. These items are important to a device. If critical errors occur and are not solved immediately, permanent damage may be caused.

Chapter 5

Chipset Software
Installation Utility

5.1 Before You Begin

To facilitate the installation of the enhanced display drivers and utility software, read the instructions in this chapter carefully. The drivers for the AIMB-219 are located on the Advantech support website: <http://support.advantech.com/support>. The drivers on the support website will guide and link you to the utilities and drivers under a Windows system. Updates are provided via Service Packs from Microsoft.

Note! *The driver files on the website are compressed. Do not attempt to install the drivers by copying the files manually. You must download the files and decompress them first. Also, please use the supplied Setup program to install the drivers.*



Before you begin, it is important to note that most display drivers need to have the relevant software application already installed in the system prior to installing the enhanced display drivers. In addition, many of the installation procedures assume that you are familiar with both the relevant software applications and operating system commands. Review the relevant operating system commands and the pertinent sections of your application software's user manual before performing the installation.

5.2 Introduction

The Intel® Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured. This is needed for the proper functioning of the following features:

- Core PCI PnP services
- Serial ATA interface support
- USB support
- Identification of Intel® chipset components in the Device Manager

Note! *This utility is used for the following versions of Windows, and it has to be installed before installing all the other drivers:*



- Windows 10 (64-bit)

Chapter 6

LAN Configuration

6.1 Introduction

The AIMB-219 B1 system features dual Gigabit Ethernet LAN via dedicated PCI Express x1 lanes (Realtek RTL8111K (LAN1) and Realtek RTL8111K (LAN2)) that offer bandwidth of up to 500 MB/sec, eliminating bottlenecks in the flow of network data by incorporating Gigabit Ethernet at 1000 Mbps. Both LAN1 and LAN2 colay RTL8125BG (2.5GbE), offering bandwidth of up to 500 MB/sec, eliminating bottlenecks in the flow of network data by incorporating Gigabit Ethernet at 2500 Mbps.

6.2 Features

- Integrated 10/100/1000/2500 Mbps transceiver
- 10/100/1000/2500 Mbps triple-speed MAC
- High-speed RISC core with 24KB cache
- On-chip voltage regulation
- Wake-on-LAN (WOL) support
- PCI Express x1 host interface

6.3 Installation

Note! *Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.*



The Realtek 8111K (LAN1) and Realtek 8111K (LAN2) Gigabit integrated controllers support all major network operating systems. However, the installation procedure varies between systems. Please follow the driver setup procedure instructions specific to the operating system installed.

6.4 Windows 10 Driver Setup (Realtek 8111K)

Download the driver from support website on your computer and decompress the file. Select "Autorun", then navigate to the directory for your OS.

Note! *Note! Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.*





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