Approval Sheet

Customer	
Product Number	**MM1AP-NNNNNA2NDB00**
Type	**CXL 2.0 Add-In-Card**
Capacity	**N/A**
Operating temperature	**Tc=0 to 70°C**
Date	**21st Apr 2026**

The Total Solution For Industrial Flash Storage

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1. CXL FEATURES

- Compliant with PCI Express® Base Specification Rev. 5.0
- Compliant with CXL™ 1.1 & CXL™ 2.0
- PCIe / CXL io Base
  - Single link with x8 lanes
  - Up to 32GT/S data rate
- CXL DVSEC (Designated Vendor-Specific Extended Capability)
  - CXL device
  - Flex Port
  - Register Locator
  - No Data Response NDR (ECN)
- Type-3 Single Logical Device (SDL)
- Vendor Defined Message (VDM) for CXL power management
- CXL Memory Mapped IO (MMIO) register
  - Component registers
  - Device registers
- Mailbox
- Three Data Object Exchange (DOE) instances :
  - CDAT DOE
  - Compliance DOE
  - Security DOE
- Datapath protection for RAS
- Metadata storage
- CXL Performance Monitoring Unit (CPMU)
- Media Side I2C/I3C Master ; Host Side SMBUS Slave
- RoHS/Halogen-free
- *CXL Device Speed : 1 Slot : 6400 MT/S (Max)
- 2 Slots : 5200 MT/S only (Controller Limitation)

*Note : The device speed is not the same as the speed transmitted through PCIe

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2. RAS FEATURES

- CXL Link CRC and Retry
- CXL Link Retrain and Recovery
- Data Poison
- Viral
- Memory ECC SEC/DED
- Automatic data scrubbing of correctable errors
- DDR Read CRC / Write CRC and Retry
- DDR CA Parity and Retry
- Errors Logging and Injection
- Patrol and Demand Scrub
- hPPR & sPPR
- Memory data scrambling
- Memory sparing
- Memory mirroring

3. DEVICE PERFORMANCE[1] @ PCI Express® Gen.5 x8

- Data Transfer Rate (64Byte Cache line size) (full loading 128GB*2=256GB)
-

- All Read	26.5 GB/S
- 1Read/ 1Write	33.4 GB/S
- 2Read/ 1Write	32.9 GB/S
- 3Read/ 1Write	31.9 GB/S
- Stream-triad like	31.1 GB/S

- Latency

- Idle Latency	314.5 ns
- Device Latency (Pin to Pin)	< 150 ns
- QoS of Latency (99.9%)	< 450 ns

1) Based on PCI Express® Gen.5 x8, All performance (bandwidth/Latency) is measured by using Intel® MLC in Ubuntu 20.04.6 LTS with all threads operated by all activated cores. Data size of read / write is 64Byte with random address, aligned with cache line size. Actual performance may vary depending on use conditions and environment.

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4. Environmental Specifications

- Temperature – Operating 0~70°C

5. Power Requirements

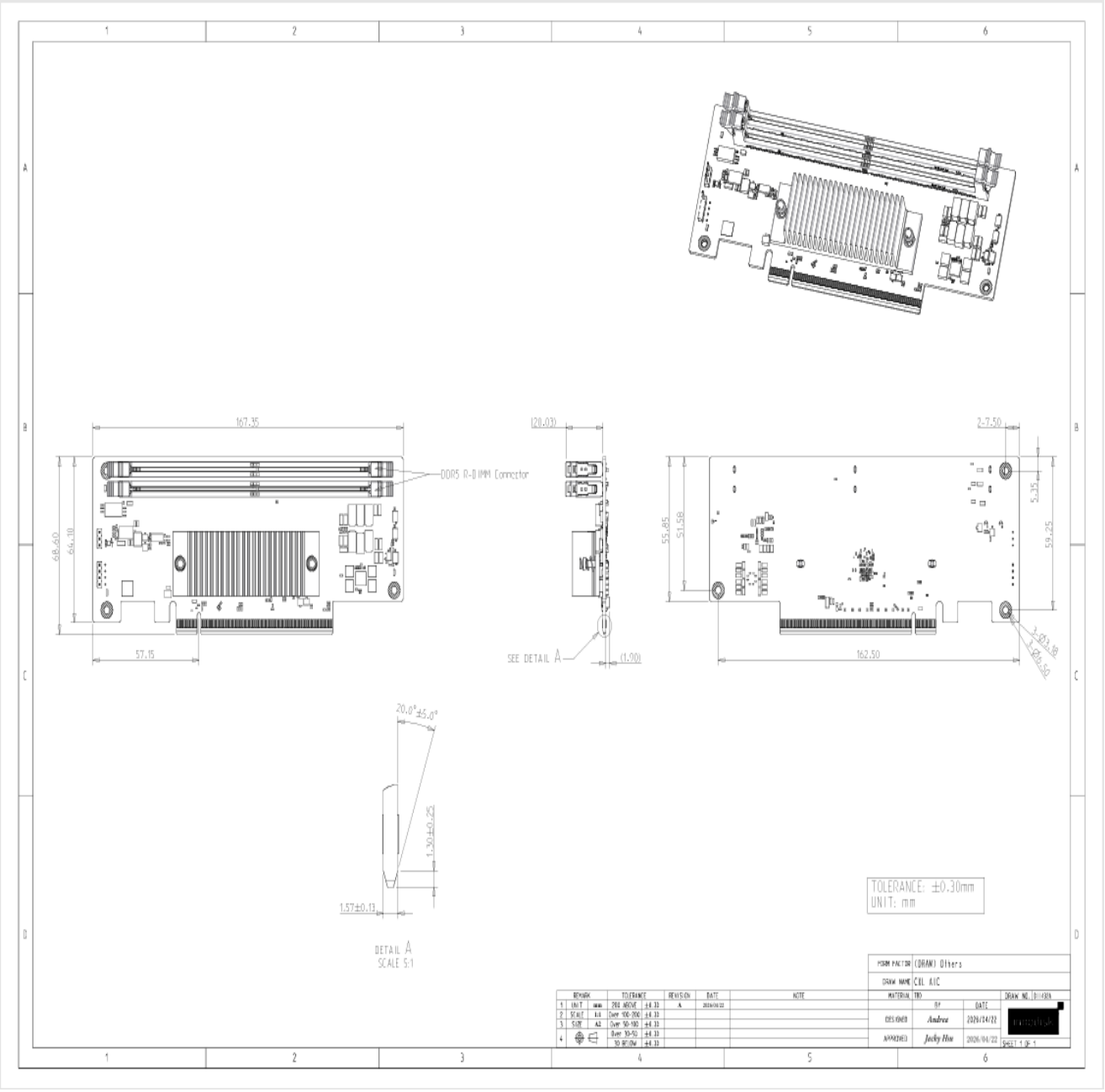
- Supply Voltage / Tolerance 12V±10%
- Power Consumption – Active Power 24.3W

6. Physical Dimension

- Width 20.03±0.30mm
- Length 167.35±0.30mm
- Height 68.6±0.30mm
- Weight (without Bracket) 108 g

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7. Mechanical Specifications



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Parameter	Unit	Description
Width	mm	20.03±0.30
Length	mm	167.35±0.30
Height	mm	68.6±0.30
Weight	g	Up to 108

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8. Pin Descriptions

- **The pin assignments and description follows PCIe Gen5**

PCI Express connector pinout (×1, ×4, ×8 and ×16 variants)							
Pin	**Side B**	**Side A**	**Description**	**Pin**	**Side B**	**Side A**	**Description**
1	+12 V	PRSNT1#	Must connect to farthest PRSNT2# pin	50	HSOp(8)	Reserved	Lane 8 transmit data, + and −
2	+12 V	+12 V	Main power pins	51	HSOn(8)	Ground	
3	+12 V	+12 V		52	Ground	HSIp(8)	Lane 8 receive data, + and −
4	Ground	Ground		53	Ground	HSIn(8)	
5	SMCLK	TCK	SMBus and JTAG port pins	54	HSOp(9)	Ground	Lane 9 transmit data, + and −
6	SMDAT	TDI		55	HSOn(9)	Ground	
7	Ground	TDO		56	Ground	HSIp(9)	Lane 9 receive data, + and −
8	+3.3 V	TMS		57	Ground	HSIn(9)	
9	TRST#	+3.3 V		58	HSOp(10)	Ground	Lane 10 transmit data, + and −
10	+3.3 V aux	+3.3 V	Aux power & standby power	59	HSOn(10)	Ground	
11	WAKE#	PERST#	Link reactivation; fundamental reset[26]	60	Ground	HSIp(10)	Lane 10 receive data, + and −
Key notch				61	Ground	HSIn(10)	
12	CLKREQ#	Ground	Clock request signal[27]	62	HSOp(11)	Ground	Lane 11 transmit data, + and −
13	Ground	REFCLK+	Reference clock differential pair	63	HSOn(11)	Ground	
14	HSOp(0)	REFCLK−	Lane 0 transmit data, + and −	64	Ground	HSIp(11)	Lane 11 receive data, + and −
15	HSOn(0)	Ground		65	Ground	HSIn(11)	
16	Ground	HSIp(0)	Lane 0 receive data, + and −	66	HSOp(12)	Ground	Lane 12 transmit data, + and −
17	PRSNT2#	HSIn(0)		67	HSOn(12)	Ground	
18	Ground	Ground		68	Ground	HSIp(12)	Lane 12 receive data, + and −
PCI Express ×1 cards end at pin 18				69	Ground	HSIn(12)	
19	HSOp(1)	Reserved	Lane 1 transmit data, + and −	70	HSOp(13)	Ground	Lane 13 transmit data, + and −
20	HSOn(1)	Ground		71	HSOn(13)	Ground	
21	Ground	HSIp(1)	Lane 1 receive data, + and −	72	Ground	HSIp(13)	Lane 13 receive data, + and −
22	Ground	HSIn(1)		73	Ground	HSIn(13)	
23	HSOp(2)	Ground	Lane 2 transmit data, + and −	74	HSOp(14)	Ground	Lane 14 transmit data, + and −
24	HSOn(2)	Ground		75	HSOn(14)	Ground	
25	Ground	HSIp(2)	Lane 2 receive data, + and −	76	Ground	HSIp(14)	Lane 14 receive data, + and −
26	Ground	HSIn(2)		77	Ground	HSIn(14)	
27	HSOp(3)	Ground	Lane 3 transmit data, + and −	78	HSOp(15)	Ground	Lane 15 transmit data, + and −
28	HSOn(3)	Ground		79	HSOn(15)	Ground	
29	Ground	HSIp(3)	Lane 3 receive data, + and −	80	Ground	HSIp(15)	Lane 15 receive data, + and −
30	PWRBRK#	HSIn(3)	"Power brake", active-low to reduce device power	81	PRSNT2#	HSIn(15)	
31	PRSNT2#	Ground		82	Reserved	Ground	
32	Ground	Reserved					
PCI Express ×4 cards end at pin 32							
33	HSOp(4)	Reserved	Lane 4 transmit data, + and −				
34	HSOn(4)	Ground					
35	Ground	HSIp(4)	Lane 4 receive data, + and −				
36	Ground	HSIn(4)					
37	HSOp(5)	Ground	Lane 5 transmit data, + and −				
38	HSOn(5)	Ground					
39	Ground	HSIp(5)	Lane 5 receive data, + and −				
40	Ground	HSIn(5)					
41	HSOp(6)	Ground	Lane 6 transmit data, + and −				
42	HSOn(6)	Ground					
43	Ground	HSIp(6)	Lane 6 receive data, + and −				
44	Ground	HSIn(6)					
45	HSOp(7)	Ground	Lane 7 transmit data, + and −				
46	HSOn(7)	Ground					
47	Ground	HSIp(7)	Lane 7 receive data, + and −				
48	PRSNT2#	HSIn(7)					
49	Ground	Ground					
PCI Express ×8 cards end at pin 49							

Legend	
Power	Supplies power to the card
Sense	Tied together on card
Ground	Zero volt reference
Open drain	May be pulled low or sensed by multiple cards[28]
Host-to-card	Signal from the motherboard to the card
Card-to-host	Signal from the card to the motherboard
Reserved	Not presently used

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9. References

- This document leverages and references the below standards specification.

Item	Website
• PCI Express® Base Specification Revision 5.0	• https://www.pcisig.com/specifications
• PCI Express® Card Electromechanical Specification	• https://www.pcisig.com/specifications
• CXL™ 1.1 & 2.0 Specification.	• https://www.computeexpresslink.org
• SFF-TA-1002 & SFF-TA-1008 & SFF-TA-1009	• https://www.snia.org/sff/specifications
• SNIA / SFF-TA-1023 - Specification for Thermal	• https://www.snia.org/sff/specifications
• JEDEC® CXL Memory Module Label - JESD405 - 1A , January 2024	• https://www.jedec.org/
• JEDEC® CXL Memory Module Reference Base Standard – JESD317A, January 2024	
• JEDEC® CXL Memory Controller Standard – JESD319, September 2024	
• JEDEC® CXL Memory Device Management Standard – JESD325, September 2024	

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10. RoHS Declaration

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Innodisk Corporation

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Tel:(02)7703-3000 Internet: https://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Products: All Innodisk EM FLASH, DRAM and EP products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及(EU) 2015/863 關於 RoHS 之規範要求。
Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

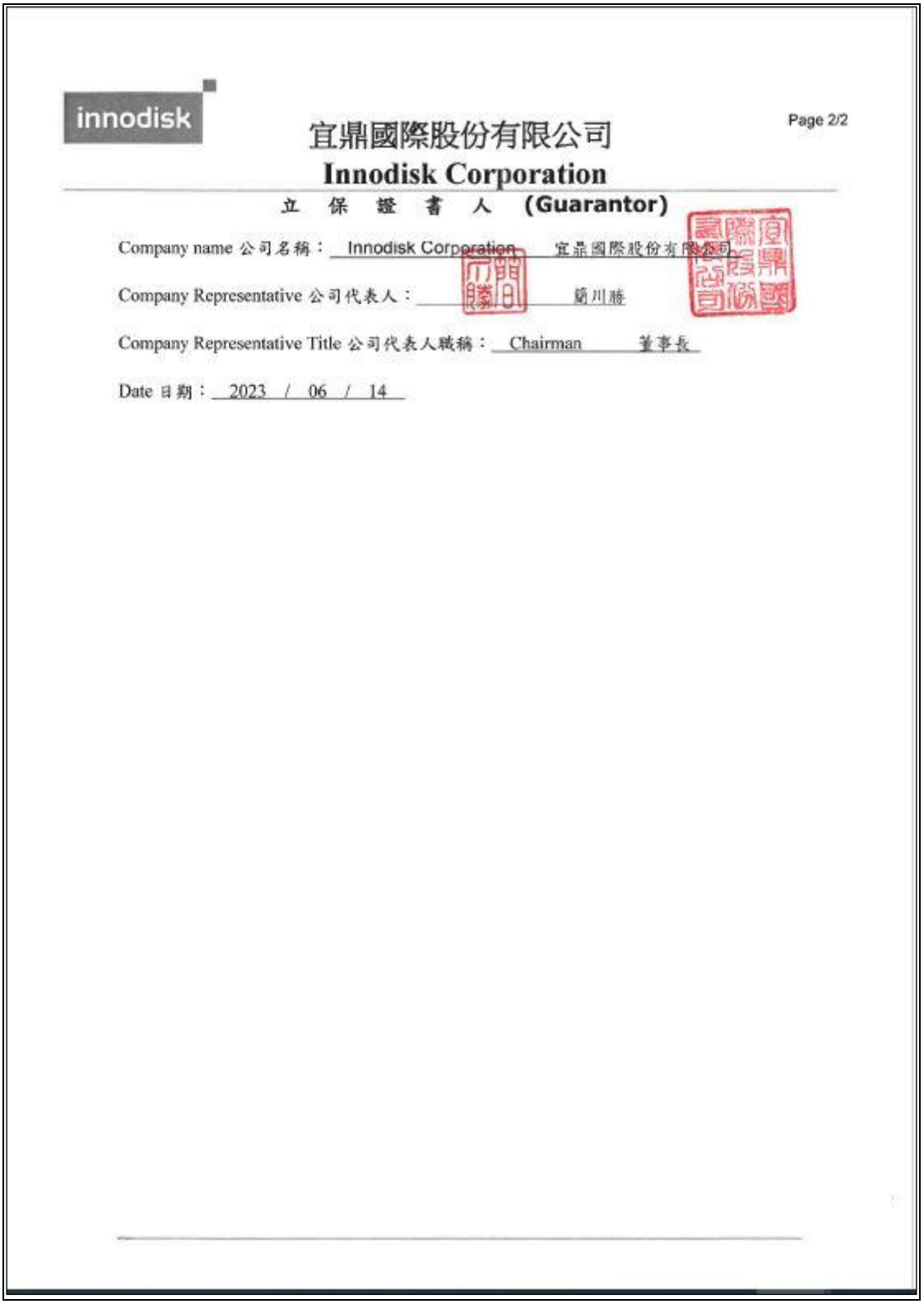
二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。
Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

三、 本公司聲明我們的產品符合 RoHS 指令的附件中 7(a)、7(c)-I、6(c)允許豁免。
We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.

※ 7(a) Lead in high melting temperature type solders(i.e. lead-based alloys containing 85% by weight or more lead).
※ 7(c)-I Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.
※ 6(c) Copper alloy containing up to 4% lead by weight. (This exemption applies to products that use antennas)

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
鉛（Pb）	< 1000 ppm
汞（Hg）	< 1000 ppm
鎘（Cd）	< 100 ppm
六價鉻（Cr 6+）	< 1000 ppm
多溴聯苯（PBBs）	< 1000 ppm
多溴二苯醚（PBDEs）	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯（DEHP）	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯（BBP）	< 1000 ppm
鄰苯二甲酸二丁酯（DBP）	< 1000 ppm
鄰苯二甲酸二異丁酯（DIBP）	< 1000 ppm

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Innodisk Corporation

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立 保 證 書 人 **(Guarantor)**

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2023 / 06 / 14

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11. REACH Declaration

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Innodisk Corporation
REACH Declaration

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: https://www.innodisk.com/

Innodisk Corporation pursues its social responsibility for global environmental preservation by committing to be compliant with REACH regulation (REGULATION (EC) No 1907/2006).
We hereby confirm that the product(s),

Scope: Flash Memory, DRAM Module and Embedded Peripherals Products.

■ The standard products of **not listed in** the ***Appendix2*** meet the requirements of REACH SVHC regulations(SVHCs < 0.1% in Article), as described in the candidate list table currently including 240 substances (release date: 23-JAN-2024) and shown on the ECHA website. https://echa.europa.eu/candidate-list-table

■ The standard products listed in the ***Appendix2*** contain(s) one or more hazardous substances or constituents exceeding 0.1 % by weight in article if not otherwise specified in candidate list table.
Where the threshold value is exceeded, the substances in question are to be declared in accompanying. (SVHCs > 0.1% in Article).

■ Comply with REACH Annex XVII.

Guarantor

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Yichuan Chen 陳怡全

Company Representative Title 公司代表人職稱：Quality Assurance Div. SR. Manager 品保處經理

Date 日期：2024 / 02 / 19

1

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Revision Log

Rev	Date	Modification
0.1	23th May 2024	Preliminary Edition
0.2	16th Sep 2025	Revised by more Function
0.3	21st Apr 2026	Revised by more datas

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