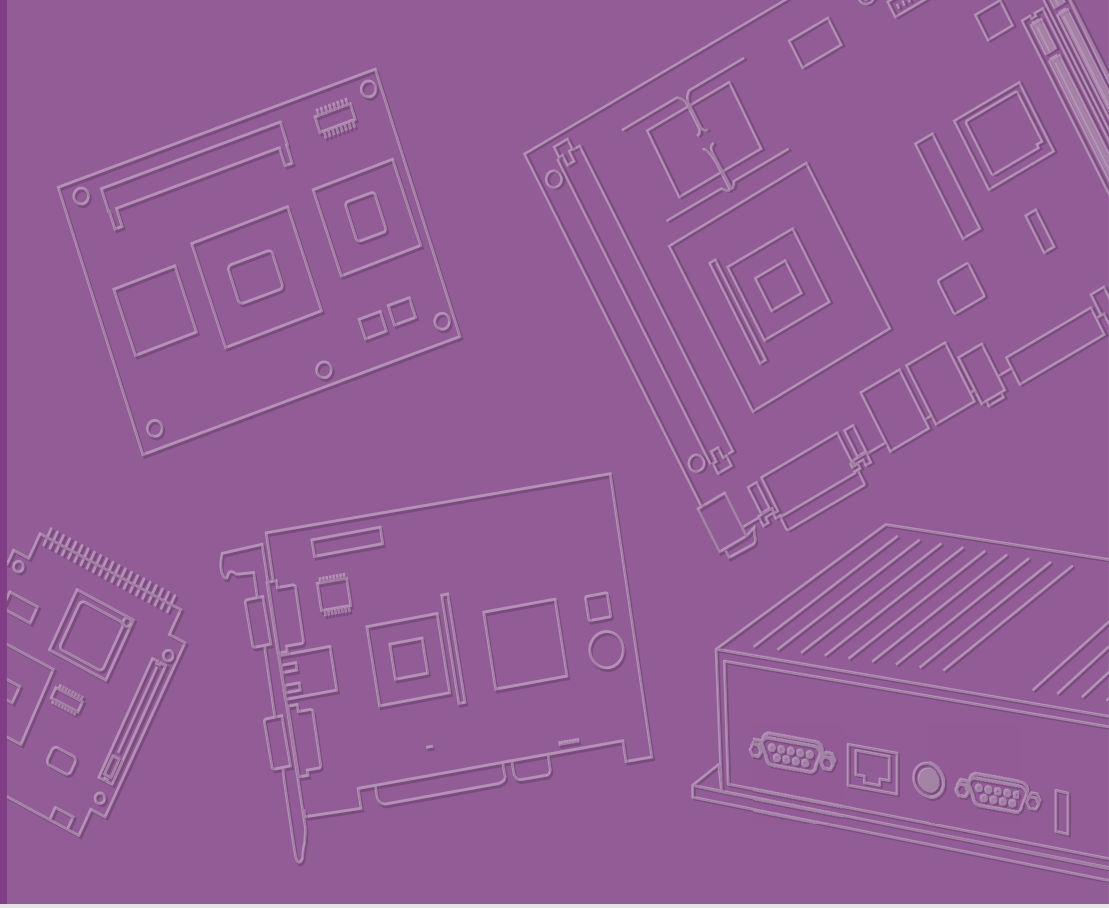


User Manual

AIMB-234

Mini-ITX motherboard
15th Gen Intel® Core™ Ultra Processor, LGA1851

ADVANTECH

Enabling an Intelligent Planet

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Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

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1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
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5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

Part No. 2006023400 Edition 1

Printed in China October 2026

Declaration of Conformity

FCC Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

Initial Inspection

Before you begin installing your motherboard, please make sure that the following materials have been shipped:

- AIMB-234 Mini-ITX motherboard
- 1 x cooler for CPU
- 1 x SATA HDD cable
- 1 x SATA power cable
- 1 x 1-to-1 serial port cable
- 1 x ATX 2x10P-4.2/1x3P-2.0 15cm cable
- 1 x I/O port bracket
- 1 x startup manual
- 1 x warranty card
- 3 x screws (M3*4L)

If any of these items are missing or damaged, contact your distributor or sales representative immediately. We have carefully inspected the AIMB-234 mechanically and electrically before shipment. It should be free of marks and scratches and in perfect working order upon receipt. As you unpack the AIMB-234, check it for signs of shipping damage. (For example, damaged box, scratches, dents, etc.) If it is damaged or it fails to meet the specifications, notify our service department or your local sales representative immediately. Also notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After inspection, we will make arrangements to repair or replace the unit.

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Chapter 1

General Information

1.1 Introduction

The AIMB-234 features an onboard Intel® Core™ Ultra Series 3 Processor and is designed for industrial applications requiring enhanced computing performance and power management. It supports up to 128GB of dual-channel DDR5 7200 MT/s memory via two 262-pin CSODIMM slots.

The AIMB-234 provides rich I/O connectivity, including one USB 4.0 Type-C port, four USB 3.2 ports, two USB 2.0 ports, and four COM ports, all integrated into a standard 170 x 170 mm form factor. It supports up to four independent displays via HDMI, DP, LVDS (or eDP), and USB4 Type-C with Alternate Mode (Alt Mode).

Additional connectivity and expansion features include PCIe x8 Gen 5 (SKU-dependent), 8-bit GPIO, SATA III 6 Gb/s connectors, TPM 2.0 security, and three M.2 expansion slots: M-Key (2280/2242), B+M-Key (3042), and E-Key (2230). Dual Intel Ethernet controllers and 10/100/1000/2500 Mbps Ethernet connectivity provide high-speed networking.

All these features are integrated into a space-saving, power-efficient, and cost-effective Mini-ITX motherboard.

1.2 Features

- Intel® Core™ Ultra Series 3 processors, up to 16 cores.
- Supports dual channel DDR5, up to 7200 MT/s CSODIMM, up to 128GB Max.
- 1 x M.2 M-Key 2280/2242 for NVMe SSD (PCIe x4 Gen5)
- 1 x M.2 B+M-Key 3042. a. PCIe x2 Gen4 + USB2.0 b. USB3.2 Gen1 + USB2.0 + SIM1 Slot for 4G Module c. SATAIII for Storage d. Colay with 2nd M-key 2242 PCIe x4 Gen 4.
- 1 x M.2 E-key 2230 for wireless module (WiFi/BT)
- 1 x PCIe x8 Gen5 by SKU
- Dual 2.5GbE LAN with Intel® I226-LM & I226-V

1.3 Specifications

1.3.1 System

- **CPU:** Intel® Core™ Ultra Series 3 processors (BGA up to 25W TDP)
- **BIOS:** AMI EFI 512 Mbit SPI BIOS
- **Storage Interface:** one M.2 M-Key 2280/2242 for NVMe SSD (PCIe x4 Gen5); one SATA III 6.0 Gb/s

1.3.2 Memory

- **RAM:** Dual 262-pins CSODIMM sockets support channel DDR5, up to 7200 MT/s CSODIMM, up to 128GB Max.

1.3.3 Input/Output

- **Serial Ports:** Supports 3 x RS-232, 1 x RS-232/422/485, by BOM option
- **USB port:** Supports two USB3.2 Gen1, two USB3.2 Gen2, two USB2.0, one USB Type-C
- **GPIO connector:** 8-bit general purpose Input/Output

1.3.4 Graphics

- **Controller:** Intel® Arc™ Graphics (Xe3)
- **LVDS or eDP:** 1 LVDS with maximum resolution up to 1920x1200 @ 60Hz or 1 eDP with maximum resolution up to 1920x1080 @ 60Hz by pass mode.
- **DP:** Supports 2 DP (1 via USB Type-C with ALT mode) up to 4096 x 2160 @120Hz.
- **HDMI:** Supports 1 HDMI 2.1 TMDS up to 4096 x 2160 @60Hz

1.3.5 Ethernet LAN

- Supports dual 10/100/1000/2500 Mbps Ethernet port (s)
- **Controller:**
  - LAN1: Intel I226-LM 2.5 GbE
  - LAN2: Intel I226-V 2.5 GbE

1.3.6 Industrial Features

- **Watchdog Timer:** Generates a system reset. The watchdog timer is programmable, with each unit equal to one second or one minute (255 levels).

1.3.7 Mechanical and Environmental Specifications

- **Operating Temperature:** 0 ~ 60°C (32 ~ 140°F)
- **Storage Temperature:** -40 ~ 85°C (-40 ~ 185°F).
- **Humidity:** 5 ~ 95% non-condensing.
- **Power Supply Voltage:** 12-24V
- **Power Consumption:**

Status	Total Watt (W)
S0 (TAT Turbo CPU + GPU 100%)	82
S0 (Burn-in)	36

(configuration: Intel® Core™ Ultra Series 3 X7 358H, 2pcs 64 GB DDR5 6400 MT/s)

- **Board Size:** 170 x 170 mm (6.69 x 6.69").
- **Board Weight:** 0.5 kg

1.4 Jumpers and Connectors

Connectors on the AIMB-234 motherboard link it to devices such as hard disk drives and a keyboard. In addition, the board has a number of jumpers used to configure the system for your application.

Later sections in this chapter give instructions on setting jumpers. Chapter 2 gives instructions for connecting external devices to your motherboard.

Table 1.1: I/O Connector

Item	Description	Part Reference
1	Direct current input connector	DCIN1
2	Display Port / HDMI connector	DP1+HDMI1
3	TBT4 / USB4 Type C connector	USB-C1
4	USB 3.2 Gen2 connector #1 / #2	USB3_12
5	RJ45 connector #1	LAN1
6	RJ45 connector #2	LAN2
7	HD audio interface (LINE-OUT)	AUDIO1
8	HD audio interface (MIC-IN)	AUDIO2
9	Audio amplifier output pin header	AMP1
10	ATX 12V 4-pin power connector	ATX12V1(ATX12V2)
11	ATX supported 3-pin header on board	ATX_5VSB1
12	PD external 100W power connector	PD_SPR1
13	PD external 100W I2C connector	PD_SPR2
14	PCI Express x8 slot	PCIEX8_1
15	DDR5 SO-DIMM socket A1	DIMMA1
16	DDR5 SO-DIMM socket B1	DIMMB1
17	USB2.0 front panel header	USB2_56
18	USB3.2 Gen1 front panel header	USB3_34
19	Serial ATA interface connector #1	SATA1
20	Serial ATA interface power connector	SATA_PWR1
21	M.2 E-KEY connector	M2_E1
22	M.2 B-KEY connector	M2_B1
23	M.2 M-KEY connector	M2_M2
24	M.2 M-KEY connector	M2_M1
25	COM1 connector	COM1
26	COM2 connector	COM2
27	COM3 connector	COM3
28	COM4 connector	COM4
29	COM4 RI# selection pin header	JSETCOM4_V1
30	8-bit general purpose I/O pin header	GPIO1
31	CPU FAN connector	CPUFAN1
32	System Fan #1 connector	SYSFAN1
33	EDP connector / LVDS connector	EDP1_LVDS1
34	EDP panel / LVDS panel voltage selection	JEDP1_LVDS1
35	EDP / LVDS backlight inverter power connector	INV1
36	PWRBTN#/ RESET#/HDD LED/ SM bus pin header	JFP1
37	PWRBTN# pin connector	JFP1_1
38	Power LED pin header	JFP2 (JFP2_1)

Table 1.1: I/O Connector		
39	CMOS mode selection	JCMOS1
40	Case open connector	JCASE1
41	LED port 80 connector	LED_P80
42	CAN bus connector	CANBUS1
43	AT / ATX mode selection	PSON1
44	CMOS battery connector	BAT1
45	SIM card connector	SIM1
46	Flash description security override switch	SW_ME1
47	SPI BIOS flash socket	SPI1
48	IT5782VG programming header	JSMBUS1

1.5 Board layout: Jumper and Connector Locations

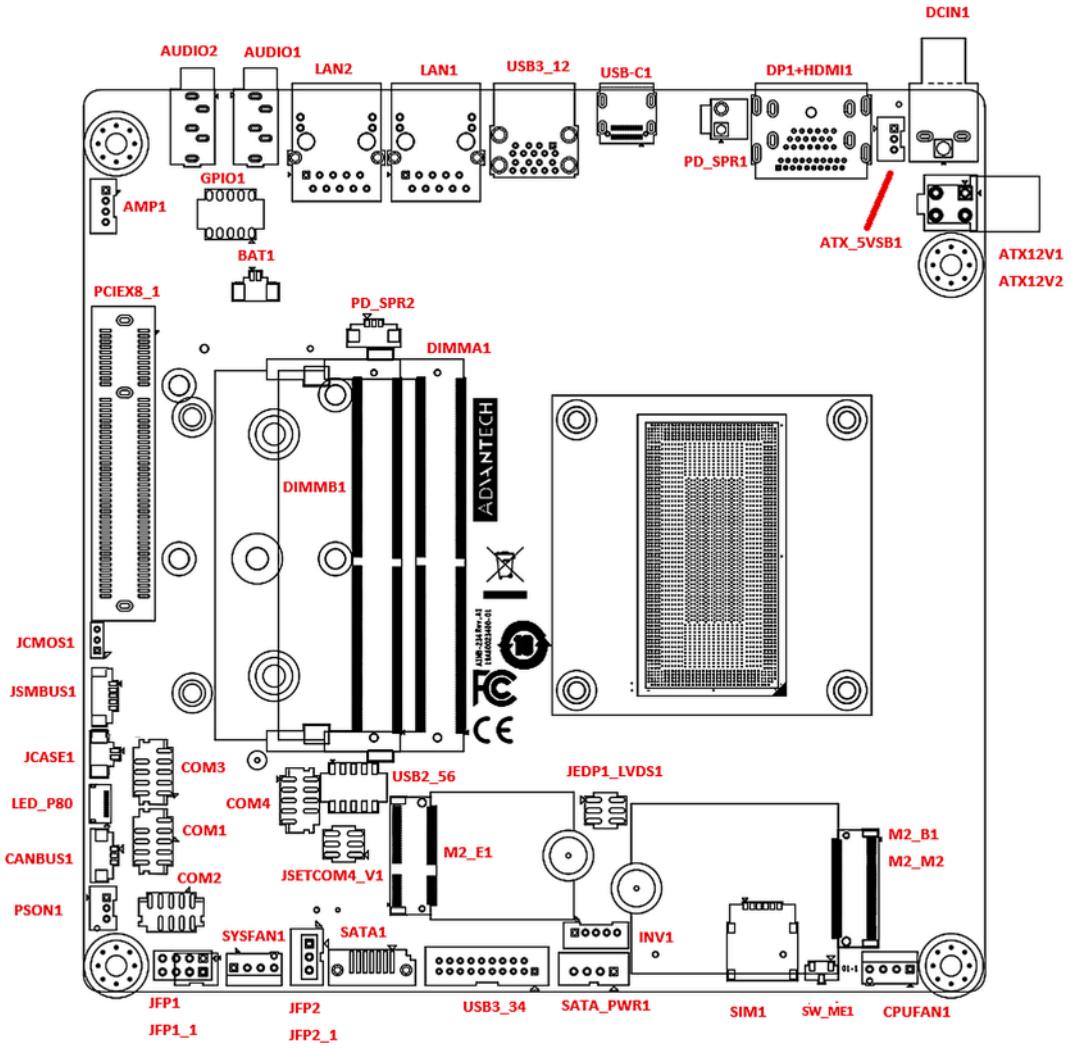


Figure 1.1 Jumper and Connector Location (Top Side)

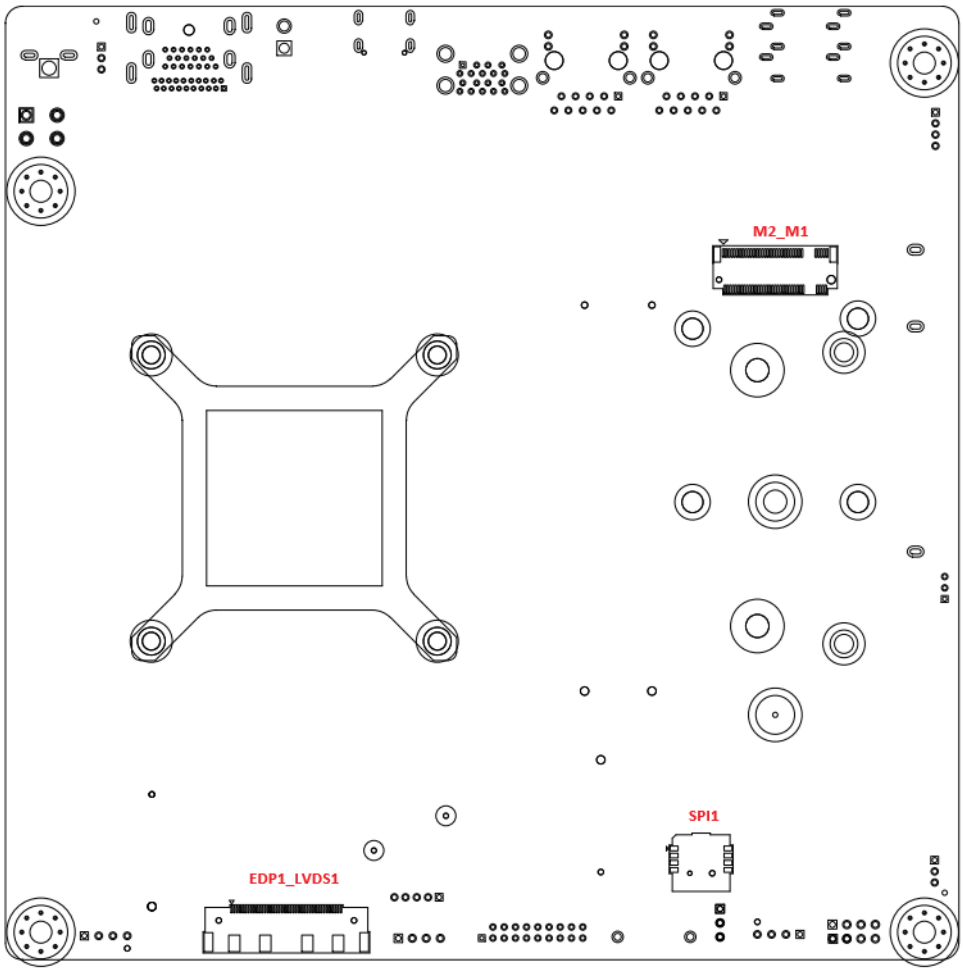


Figure 1.2 Jumper and Connector Location (Bottom Side)

Table 1.2: Connector / Header List

Item	Description	Part Reference
1	Direct current input connector	DCIN1
2	Display Port / HDMI connector	DP1+HDMI1
3	TBT4 / USB4 Type C connector	USB-C1
4	USB 3.2 Gen2 connector #1 / #2	USB3_12
5	RJ45 connector #1	LAN1
6	RJ45 connector #2	LAN2
7	HD audio interface (LINE-OUT)	AUDIO1
8	HD audio interface (MIC-IN)	AUDIO2
9	Audio amplifier output pin header	AMP1
10	ATX 12V 4-pin power connector	ATX12V1(ATX12V2)
11	ATX supported 3-pin header on board	ATX_5VSB1
12	PD external 100W power connector	PD_SPR1
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14	PCI Express x8 slot	PCIEX8_1
15	DDR5 SO-DIMM socket A1	DIMMA1
16	DDR5 SO-DIMM socket B1	DIMMB1
17	USB2.0 front panel header	USB2_56
18	USB3.2 Gen1 front panel header	USB3_34

Table 1.2: Connector / Header List		
19	Serial ATA interface connector #1	SATA1
20	Serial ATA interface power connector	SATA_PWR1
21	M.2 E-KEY connector	M2_E1
22	M.2 B-KEY connector	M2_B1
23	M.2 M-KEY connector	M2_M2

1.6 AIMB-234 Board Diagram

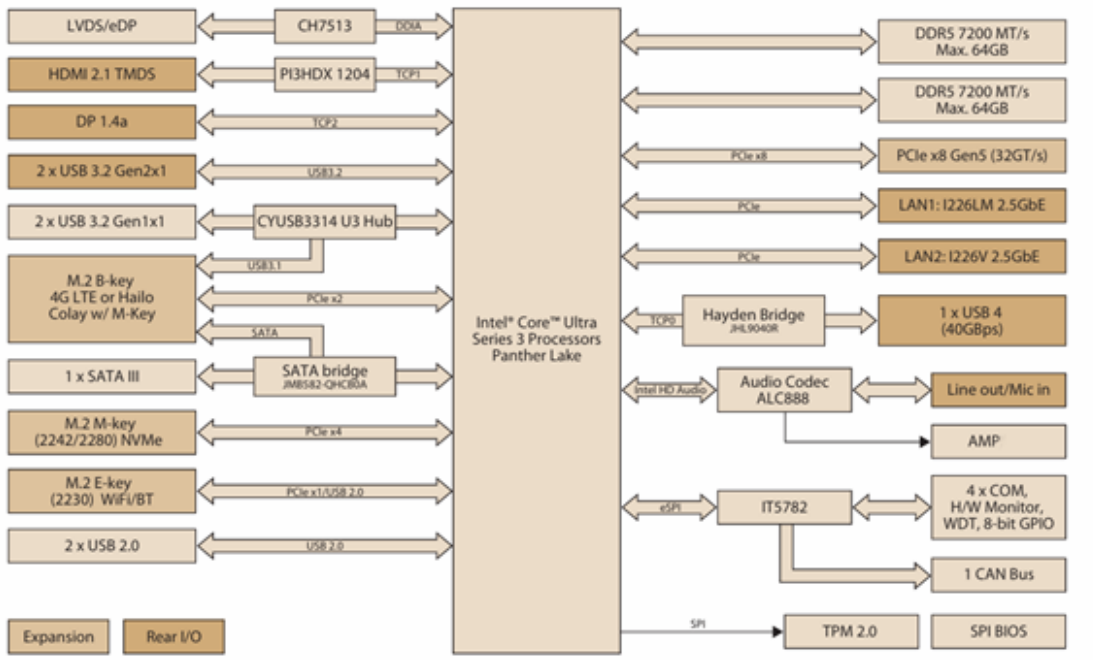


Figure 1.3 AIMB-234 Block Diagram

1.7 Safety Precautions

Warning! *Always completely disconnect the power cord from chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.*



Caution! *Always ground yourself to remove any static charge before touching the motherboard. Modern electronic devices are very sensitive to electro-static discharges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis.*



Caution! *The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by the manufacturer. Discard used batteries according to manufacturer's instructions.*



Caution! *There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*



1.8 Jumper Settings

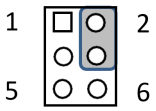
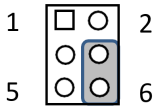
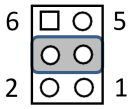
This section provides instructions on how to configure your motherboard by setting the jumpers. It also includes the motherboard's default settings and your options for each jumper.

1.8.1 How to Set Jumpers

Users can configure your motherboard to match the needs of your application by setting the jumpers. A jumper is a metal bridge that closes an electrical circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" (or turn ON) a jumper, you connect the pins with the clip. To "open" (or turn OFF) a jumper, you remove the clip. Sometimes a jumper consists of a set of three pins, labeled 1, 2, and 3. In this case you connect either pins 1 and 2, or 2 and 3. A pair of needle-nose pliers may be useful when setting jumpers.

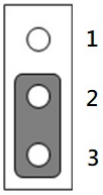
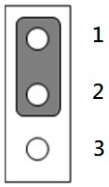
1.8.2 EDP Panel / LVDS Panel Voltage Selection (JEDP1_LVDS1)

Table 1.3: JEDP1_LVDS1

Function	Jumper Setting
Jumper position for 5V	
Jumper position for 3.3V (default)	
Jumper position for 12V	

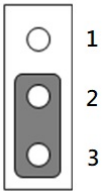
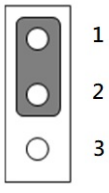
1.8.3 AT/ATX Mode Selection (PSON1)

Table 1.4: PSON1

Function	Jumper Setting
ATX Mode (default) PSON1(2-3)	
AT Mode PSON(1-2)	

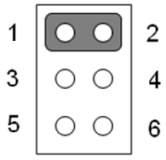
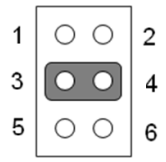
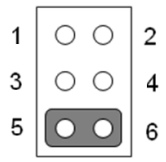
1.8.4 CMOS Clear (JCMOS1)

Table 1.5: JCMOS1

Function	Jumper Setting
Normal (default) JCMOS1(1-2)	
Clear CMOS JCMOS(2-3)	

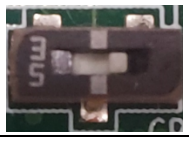
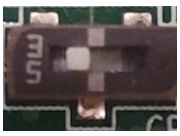
1.8.5 COM4 RI# Selection Pin Header (JSETCOM4_V1)

Table 1.6: JSETCOM4_V1

Function	Jumper Setting
Jumper position for RI# (default)	
Jumper position for +5V	
Jumper position for +12V	

1.8.6 Flash Descriptor Security Override Switch (SW_ME1)

Table 1.7: SW_ME1

Function	Jumper Setting
Enable Flash Descriptor Security (default)	
Disable Flash Descriptor Security	

1.9 System Memory

The AIMB-234 has two 262-pin CSODIMM sockets for DDR5 memory. These sockets support 1.2 V unbuffered DDR5 SDRAM. Supported memory module capacities are 8GB, 16GB, 32GB, 48GB, and 64GB. The sockets support different combinations of module capacities, allowing a total memory capacity of 8GB, 16GB, 32GB, 48GB, 64GB, 80GB, 96GB, 112GB, or up to 128GB. The AIMB-234 does not support Error-Correcting Code (ECC) memory.

1.10 Memory Installation Procedures

To install DIMMs, make sure the two socket latches are in the open position, tilted outward. Align the DIMM with the guides at both ends of the socket and insert it evenly. Press down firmly and gently until both latches click into place, securing the DIMM. To remove a DIMM, push both latches outward to release it. The DIMM will then be ejected from the socket.

Chapter 2

Pin Assignments

2.1 Introduction

You can access most of the connectors from the top of the board as it is being installed in the chassis. If you have a number of cards installed or have a packed chassis, you may need to partially remove the card to make all the connections.

2.2 I/O Connector

2.2.1 Direct Current Input Connector (DCIN1)

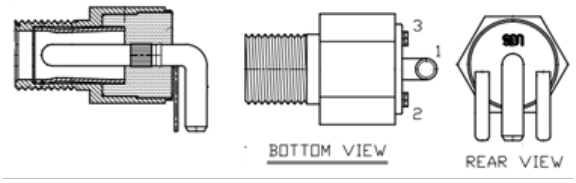


Table 2.1: DCIN1

Pin	Signal
1	12V ~ 24V
2	GND
3	GND

2.2.2 DisplayPort / HDMI Connector (DP1 + HDMI1)

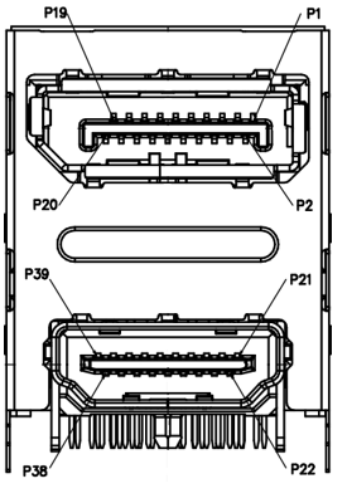


Table 2.2: DP1 + HDMI1

Pin	Signal	Pin	Signal
P1	DP1_TX0+	P21	TMDS Data2+
P2	GND	P22	GND
P3	DP1_TX0-	P23	TMDS Data2-
P4	DP1_TX1+	P24	TMDS Data1+
P5	GND	P25	GND
P6	DP1_TX1-	P26	TMDS Data1-
P7	DP1_TX2+	P27	TMDS Data0+
P8	GND	P28	GND

Table 2.2: DP1 + HDMI1			
P9	DP1_TX2-	P29	TMDS Data0-
P10	DP1_TX3+	P30	TMDS Clock+
P11	GND	P31	GND
P12	DP1_TX3-	P32	TMDS Clock-
P13	DP1_HDMI_DNG_DET	P33	NC
P14	GND	P34	NC
P15	AUX+	P35	SCL
P16	GND	P36	SDA
P17	AUX-	P37	GND
P18	HPD	P38	HDMI_PWR
P19	GND	P39	HPD
P20	DP_PWR		

2.2.3 TBT4 / USB4 Type Connector (USB-C1)

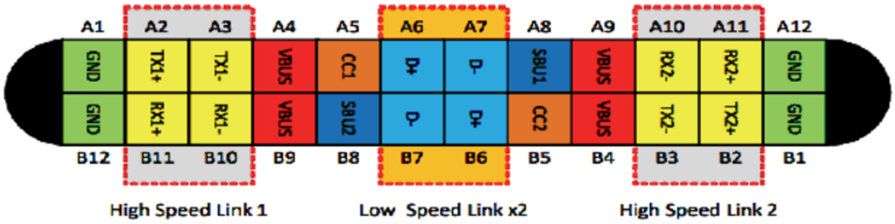


Table 2.3: USB-C1			
Pin	**Signal**	**Pin**	**Signal**
A1	GND1	B1	GND3
A2	SSTXP1_1	B2	SSTXP2_2
A3	SSTXN1_1	B3	SSTXN2_2
A4	VUSB_1	B4	VUSB_3
A5	CC1	B5	CC2
A6	DP1	B6	DP2
A7	DN1	B7	DN2
A8	SBU1	B8	SBU2
A9	VUSB_2	B9	VUSB_4
A10	SSRXN2_1	B10	SSRXN1_2
A11	SSRXP2_1	B11	SSRXP1_2
A12	GND2	B12	GND4

2.2.4 USB 3.2 Gen2 Connector #1 / #2 (USB3_12)

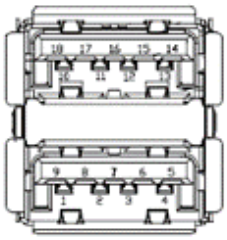


Table 2.4: USB3_12

Pin	Signal	Pin	Signal
1	VBUS	2	D- [1]
3	D+ [1]	4	GND
5	RX- [1]	6	RX+ [1]
7	GND	8	TX- [1]
9	TX+ [1]	10	VBUS
11	D- [2]	12	D+ [2]
13	GND	14	RX- [2]
15	RX+ [2]	16	GND
17	TX- [2]	18	TX+ [2]

2.2.5 RJ45 Connector #1 (LAN1)

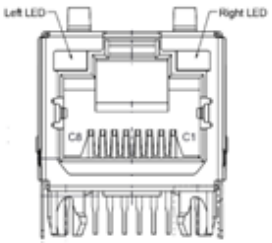


Table 2.5: LAN1

Pin	Signal
C1	MDI0+
C2	MDI0-
C3	MDI1+
C4	MDI2+
C5	MDI2-
C6	MDI1-
C7	MDI3+
C8	MDI3-

2.2.6 RJ45 Connector #2 (LAN2)

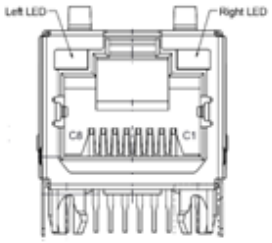


Table 2.6: LAN2	
Pin	**Signal**
C1	MDI0+
C2	MDI0-
C3	MDI1+
C4	MDI2+
C5	MDI2-
C6	MDI1-
C7	MDI3+
C8	MDI3-

2.2.7 HD Analog Audio Interface Line-Out (AUDIO1)



Table 2.7: AUDIO1	
Pin	**Signal Pin Definition**
1	GND_A
2	A_Z_LINEO-L
3	GND_A
4	A_Z_LINEO-R
5	A_FRONT-JD

2.2.8 HD Analog Audio Interface MIC-IN (AUDIO2)



Table 2.8: AUDIO2	
Pin	**Signal Pin Definition**
1	GND_A
2	A_Z_MIC1-L
3	GND_A
4	A_Z_MIC1-R
5	A_MIC1-JD

2.2.9 Audio Amplifier Output Pin Header (AMP1)

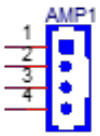


Table 2.9: AMP1	
Pin	**Signal**
1	AMP OUT - R+
2	AMP OUT - R-
3	AMP OUT - L-
4	AMP OUT - L+

2.2.10 ATX 12V 4 Pin Power Connector (ATX12V1/ ATX12V2)

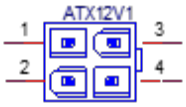


Table 2.10: ATX12V1/ ATX12V2			
Pin	**Signal**	**Pin**	**Signal**
1	GND	3	POWER
2	GND	4	POWER

2.2.11 ATX Supported 3-pin Header on Board (ATX_5VSB1)

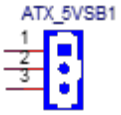


Table 2.11: ATX_5VSB1	
Pin	**Signal**
1	+5V_A_ATX
2	GND
3	SPS_PS_ON#

2.2.12 PD External 100W Power Connector (PD_SPR1)

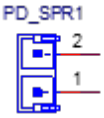


Table 2.12: PD_SPR1	
Pin	**Signal**
1	+V_CHGR_VIN
2	GND

2.2.13 PD External 100W I2C Connector (PD_SPR2)

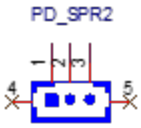


Table 2.13: PD_SPR2	
Pin	**Signal**
1	EE_+VDCIN_SCLK
2	EE_+VDCIN_SDATA
3	GND

2.2.14 PCI Express x8 Slot (PCIX8_1)

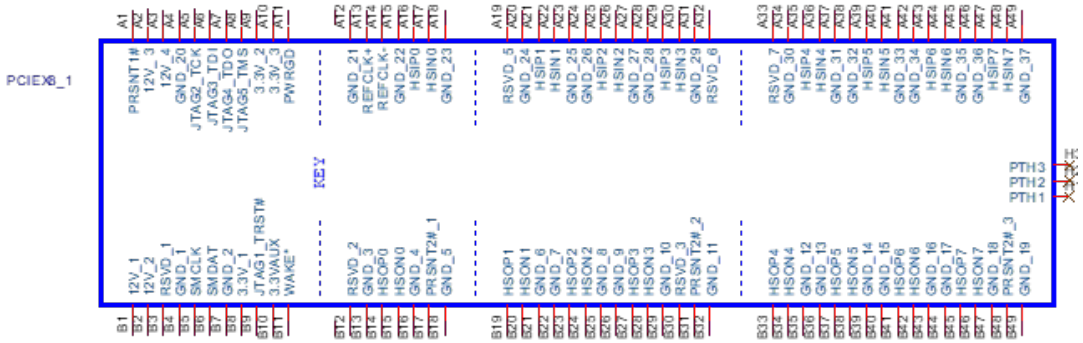


Table 2.14: PCIX8_1

Pin	Signal	Pin	Signal
B1	+12V	A1	PRSNT1#
B2	+12V	A2	+12V
B3	+12V	A3	+12V
B4	GND	A4	GND
B5	SMB_CLK	A5	Reserved
B6	SMB_DATA	A6	Reserved
B7	GND	A7	Reserved
B8	+3.3V	A8	Reserved
B9	Reserved	A9	+3.3V
B10	+3.3VAUX	A10	+3.3V
B11	WAKE#	A11	PWRGD
B12	Reserved	A12	GND
B13	GND	A13	REFCLK+
B14	TX0+	A14	REFCLK-
B15	TX0-	A15	GND
B16	GND	A16	RX0+
B17	Reserved	A17	RX0-
B18	GND	A18	GND
B19	TX1+	A19	NC
B20	TX1-	A20	GND
B21	GND	A21	RX1+
B22	GND	A22	RX1-
B23	TX2+	A23	GND
B24	TX2-	A24	GND
B25	GND	A25	RX2+
B26	GND	A26	RX2-
B27	TX3+	A27	GND
B28	TX3-	A28	GND
B29	GND	A29	RX3+
B30	Reserved	A30	RX3-
B31	Reserved	A31	GND
B32	GND	A32	NC
B33	TX4+	A33	NC

Table 2.14: PCIX8_1			
B34	TX4-	A34	GND
B35	GND	A35	RX4+
B36	GND	A36	RX4-
B37	TX5+	A37	GND
B38	TX5-	A38	GND
B39	GND	A39	RX5+
B40	GND	A40	RX5-
B41	TX6+	A41	GND
B42	TX6-	A42	GND
B43	GND	A43	RX6+
B44	GND	A44	RX6-
B45	TX7+	A45	GND
B46	TX7-	A46	GND
B47	GND	A47	RX7+
B48	Reserved	A48	RX7-
B49	GND	A49	GND

2.2.15 DDR5 SO-DIMM Socket A1 (DIMMA1)

Please refer to JEDEC STANDARD.

2.2.16 DDR5 SO-DIMM Socket B1 (DIMMB1)

Please refer to JEDEC STANDARD.

2.2.17 USB2.0 Front Panel Header (USB2_56)

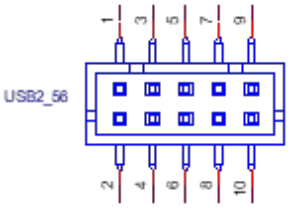


Table 2.15: USB2_56			
Pin	**Signal**	**Pin**	**Signal**
1	N.C	2	N.C
3	GND	4	GND
5	D5+	6	D6+
7	D5-	8	D6-
9	VBUS	10	VBUS

2.2.18 USB3.2 Gen1 Front Panel Header (USB3_34)

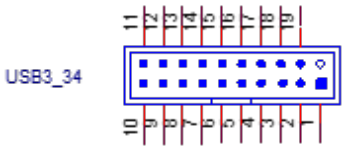


Table 2.16: USB3_34

Pin	Signal	Pin	Signal
1	VBUS		
2	RX3-	19	VBUS
3	RX3+	18	RX4-
4	GND	17	RX4+
5	TX3-	16	GND
6	TX3+	15	TX4-
7	GND	14	TX4+
8	D3-	13	GND
9	D3+	12	D4-
10	NC	11	D4+

2.2.19 Serial ATA Interface Connector #1 (SATA1)

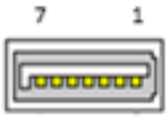


Table 2.17: SATA1

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

2.2.20 Serial ATA Interface Power Connector (SATA_PWR1)



Table 2.18: SATA_PWR1	
Pin	**Signal**
1	+V5
2	GND
3	GND
4	+V12

2.2.21 M.2 E-KEY Connector (M2_E1)

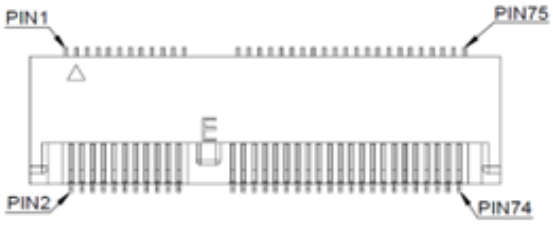


Table 2.19: M2_E1			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	+3.3V
3	USB_D+	4	+3.3V
5	USB_D-	6	WLAN_LED1#
7	GND	8	NC
9	NC	10	NC
11	NC	12	NC
13	GND	14	NC
15	NC	16	BT_LED#
17	NC	18	GND
19	GND	20	NC
21	NC	22	NC
23	NC	24	Connector Key
25	Connector Key	26	Connector Key
27	Connector Key	28	Connector Key
29	Connector Key	30	Connector Key
31	Connector Key	32	NC
33	GND	34	NC
35	PETp0	36	NC
37	PETn0	38	CL_RST#
39	GND	40	CL_DAT
41	PERp0	42	CL_CLK
43	PERn0	44	NC

Table 2.19: M2_E1			
45	GND	46	NC
47	REFCLKp0	48	NC
49	REFCLKn0	50	SUSCLK
51	GND	52	WLAN_RST#
53	CLKREQ0#	54	BT_RF_KILL#
55	PEWAKE0#	56	WIFI_RF_KILL#
57	GND	58	NC
59	NC	60	NC
61	NC	62	NC
63	GND	64	NC
65	NC	66	NC
67	NC	68	NC
69	GND	70	NC
71	NC	72	+3.3V
73	NC	74	+3.3V
75	GND		

2.2.22 M.2 B-KEY Connector (M2_B1)

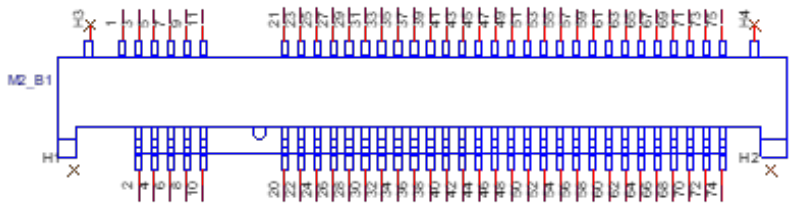


Table 2.20: M2_B1			
Pin	**Signal**	**Pin**	**Signal**
1	M2B1_CFG2	2	+3.3V
3	GND	4	+3.3V
5	GND	6	M2B1_PWR_OFF#
7	USB_D+	8	M2B1_WDISABLE1#
9	USB_D-	10	M2B1_LED1#
11	GND	12	Connector Key
13	Connector Key	14	Connector Key
15	Connector Key	16	Connector Key
17	Connector Key	18	Connector Key
19	Connector Key	20	NC
21	M2B1_CFG0	22	NC
23	NC	24	NC
25	NC	26	M2B1_W_DISABLE2#
27	GND	28	NC
29	USB3_RX-	30	M2B1_UIM_RESET
31	USB3_RX+	32	M2B1_UIM_CLK
33	GND	34	M2B1_UIM_DATA
35	USB3_TX-	36	M2B1_UIM_PWR
37	USB3_TX+	38	NC

Table 2.20: M2_B1			
39	GND	40	NC
41	PERn0	42	NC
43	PERp0	44	NC
45	GND	46	NC
47	PETn0	48	NC
49	PETp0	50	M2B1_a_PERST#
51	GND	52	M2B1_a_CLKREQ#
53	REFCLKn0	54	M2B1_PCIEWAKE#
55	REFCLKp0	56	NC
57	GND	58	NC
59	NC	60	NC
61	NC	62	NC
63	NC	64	NC
65	NC	66	NC
67	M2B1_a_WWAN_RESET#	68	SUSCLK
69	M2B1_CFG1	70	+3.3V
71	GND	72	+3.3V
73	GND	74	+3.3V
75	M2B1_CFG2		

2.2.23 M.2 M-KEY Connector (M2_M2)

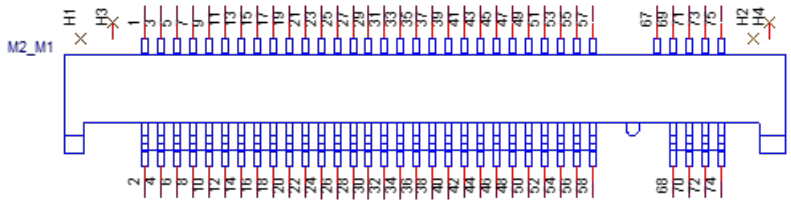


Table 2.21: M2_M2			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	+3.3V
3	GND	4	+3.3V
5	PERn3	6	NC
7	PERp3	8	NC
9	GND	10	M.2_M_LED1#
11	PETn3	12	+3.3V
13	PETp3	14	+3.3V
15	GND	16	+3.3V
17	PERn2	18	+3.3V
19	PERp2	20	NC
21	GND	22	NC
23	PETn2	24	NC
25	PETp2	26	NC
27	GND	28	NC
29	PERn1	30	NC
31	PERp1	32	NC

Table 2.21: M2_M2			
33	GND	34	NC
35	PETn1	36	NC
37	PETp1	38	NC
39	GND	40	NC
41	PERn0	42	NC
43	PERp0	44	NC
45	GND	46	NC
47	PETn0	48	NC
49	PETp0	50	PLTRST_a_M2#
51	GND	52	M2M_CLKREQ#_3.3
53	REFCLKn0	54	M2M_PCIE_WAKE#
55	REFCLKp0	56	NC
57	GND	58	NC
59	Connector Key	60	Connector Key
61	Connector Key	62	Connector Key
63	Connector Key	64	Connector Key
65	Connector Key	66	Connector Key
67	NC	68	SUSCLK
69	NC	70	+3.3V
71	GND	72	+3.3V
73	GND	74	+3.3V
75	GND		

2.2.24 M.2 M-KEY Connector (M2_M1)

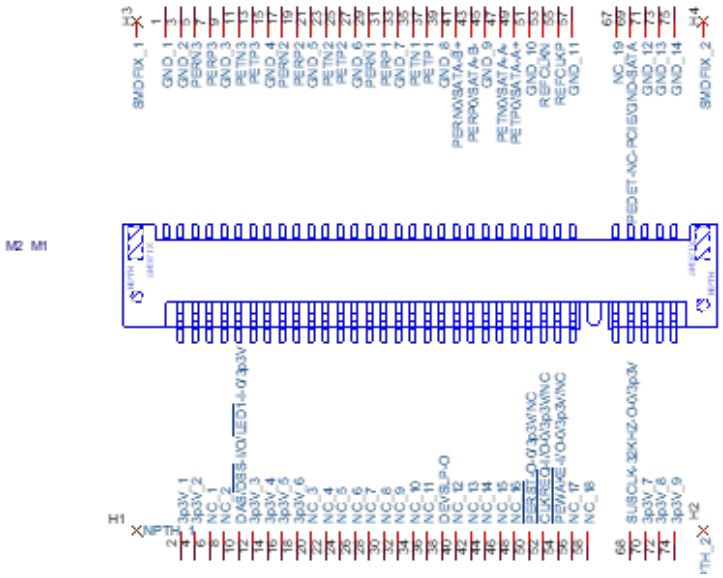


Table 2.22: M2_M1

Pin	Signal	Pin	Signal
1	GND	2	+3.3V
3	GND	4	+3.3V
5	PERn3	6	NC
7	PERp3	8	NC
9	GND	10	M.2_M_LED1#
11	PETn3	12	+3.3V
13	PETp3	14	+3.3V
15	GND	16	+3.3V
17	PERn2	18	+3.3V
19	PERp2	20	NC
21	GND	22	NC
23	PETn2	24	NC
25	PETp2	26	NC
27	GND	28	NC
29	PERn1	30	NC
31	PERp1	32	NC
33	GND	34	NC
35	PETn1	36	NC
37	PETp1	38	NC
39	GND	40	NC
41	PERn0	42	NC
43	PERp0	44	NC
45	GND	46	NC
47	PETn0	48	NC
49	PETp0	50	PLTRST_a_M2#
51	GND	52	M2M_CLKREQ#_3.3
53	REFCLKn0	54	M2M_PCIE_WAKE#
55	REFCLKp0	56	NC
57	GND	58	NC
59	Connector Key	60	Connector Key
61	Connector Key	62	Connector Key
63	Connector Key	64	Connector Key
65	Connector Key	66	Connector Key
67	NC	68	SUSCLK
69	NC	70	+3.3V
71	GND	72	+3.3V
73	GND	74	+3.3V
75	GND		

2.2.25 COM1 Connector (COM1)

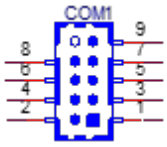


Table 2.23: COM1			
Pin	**Signal**	**Pin**	**Signal**
1	DCD#	2	SIN
3	SOUT	4	DTR#
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI#	10	

2.2.26 COM2 Connector (COM2)

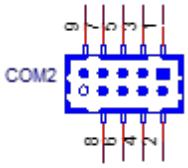


Table 2.24: COM2			
Pin	**Signal**	**Pin**	**Signal**
1	DCD#	2	SIN
3	SOUT	4	DTR#
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI#	10	

2.2.27 COM3 Connector (COM3)

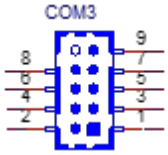


Table 2.25: COM3			
Pin	**Signal**	**Pin**	**Signal**
1	DCD#	2	SIN
3	SOUT	4	DTR#
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI#	10	

2.2.28 COM4 Connector (COM4)

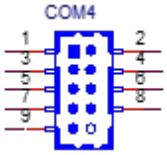


Table 2.26: COM4

Pin	Signal	Pin	Signal
1	DCD#	2	SIN
3	SOUT	4	DTR#
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI#	10	

2.2.29 COM4 RI# Selection Pin Header (JSETCOM4_V1)



Table 2.27: JSETCOM4_V1

Pin	Signal	Pin	Signal
1	RI# [1]	2	Advantech define
3	Advantech define	4	+5V
5	+12V	6	Advantech define

2.2.30 8-bit General Purpose I/O Pin Header (GPIO1)

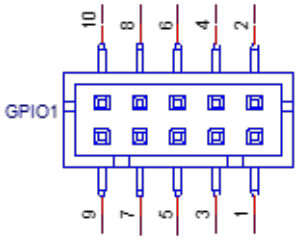


Table 2.28: GPIO1

Pin	Signal	Pin	Signal
1	GPIO4	2	GPIO0
3	GPIO5	4	GPIO1
5	GPIO6	6	GPIO2
7	GPIO7	8	GPIO3
9	GND	10	VCC_GPIO

2.2.31 CPU FAN Connector (CPUFAN1)

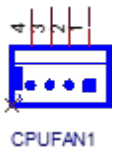


Table 2.29: CPUFAN1

Pin	Signal
1	GND
2	CPU FAN VCC
3	CPU FAN SPEED
4	CPU FAN PWM

2.2.32 System FAN Connector (SYSFAN1)

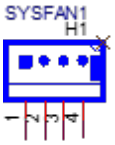


Table 2.30: SYSFAN1

Pin	Signal
1	GND
2	SYSTEM FAN VCC
3	SYSTEM FAN SPEED
4	SYSTEM FAN PWM

2.2.33 EDP Connector / LVDS Connector (EDP1_LVDS1)

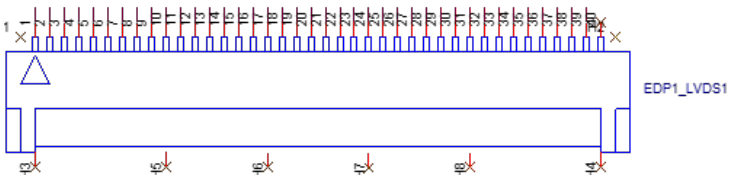


Table 2.31: LVDS1

Pin	Signal	Pin	Signal
1	VDD	2	VDD
3	VDD	4	VDD
5	N.C	6	N.C.
7	LVDS1_A4P	8	LVDS1_A4N
9	GND	10	LVDS1_A5P
11	LVDS1_A5N	12	GND
13	LVDS1_A6P	14	LVDS1_A6N
15	GND	16	LVDS1_A7P
17	LVDS1_A7N	18	GND

Table 2.31: LVDS1			
19	LVDS1_CLK2P	20	LVDS1_CLK2N
21	GND	22	LVDS1_A3P
23	LVDS1_A3N	24	GND
25	N.C.	26	N.C.
27	GND	28	LVDS1_A2P
29	LVDS1_A2N	30	GND
31	LVDS1_A1P	32	LVDS1_A1N
33	GND	34	LVDS1_A0P
35	LVDS1_A0N	36	GND
37	LVDS1_CLK1P	38	LVDS1_CLK1N
39	GND	40	LVDS CTRL

Table 2.32: EDP1			
Pin	**Signal**	**Pin**	**Signal**
1	VDD	2	VDD
3	VDD	4	VDD
5	N.C	6	N.C
7	N.C	8	N.C
9	GND	10	N.C
11	N.C	12	GND
13	N.C	14	N.C
15	GND	16	N.C
17	N.C	18	GND
19	N.C	20	N.C
21	GND	22	N.C
23	N.C	24	GND
25	N.C	26	N.C
27	GND	28	LANE0_P
29	LANE0_N	30	GND
31	LANE1_P	32	LANE1_N
33	N.C	34	GND
35	HPD	36	N.C
37	AUX_P	38	AUX_N
39	GND	40	LVDS CTRL

2.2.34 EDP / LVDS Backlight Inverter Power Connector (INV1)

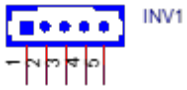


Table 2.33: INV1	
Pin	**Signal**
1	+12V
2	GND
3	BKL EN
4	BKL CTRL
5	+5V

2.2.35 EDP Panel / LVDS Panel Voltage Selection (JEDP1_LVDS1)

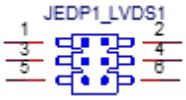


Table 2.34: JEDP1_LVDS1			
Pin	**Signal**	**Pin**	**Signal**
1	NC	2	+5V
3	+12V	4	VDD
5	NC	6	+3.3V

2.2.36 PWRBTN#/ RESET#/HDD LED/ Serial Bus Pin Header (JFP1)

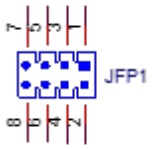


Table 2.35: JFP1			
Pin	**Signal**	**Pin**	**Signal**
1	HDD_LED+	2	PWRBTN#
3	HDD_LED-	4	GND
5	SMB_DAT	6	SYS_RESET#
7	SMB_CLK	8	GND

2.2.37 PWRBTN# Pin Connector (JFP1_1)

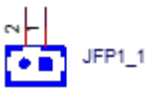


Table 2.36: JFP1_1			
Pin	**Signal**	**Pin**	**Signal**
1	SYS_RESET#	2	GND

2.2.38 Power LED Pin Header (JFP2, JFP2_1)

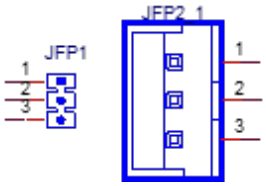


Table 2.37: JFP2, JFP2_1	
Pin	**Signal**
1	Power LED+
2	N.C.
3	Power LED-

2.2.39 CMOS Mode Selection (JCMOS1)

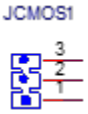


Table 2.38: JCMOS1	
Pin	**Signal**
1	NC
2	RTC_RESET#
3	GND

2.2.40 Case Open Connector (JCASE1)

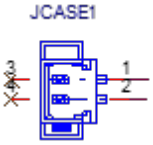


Table 2.39: JCASE1	
Pin	**Signal**
1	Case Open
2	GND

2.2.41 LED Port 80 Connector (LED_P80)

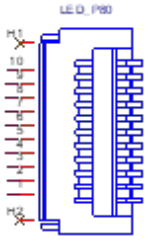


Table 2.40: LED_P80

Pin	Signal
1	GND
2	LED_A
3	LED_B
4	LED_C
5	LED_D
6	LED_E
7	LED_F
8	LED_G
9	DGH0#
10	DGL0#

2.2.42 CAN Bus Connector (CANBUS1)

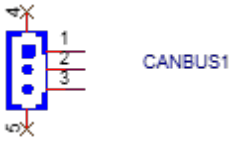


Table 2.41: CANBUS1

Pin	Signal
1	CAN_D+
2	CAN_D-
3	GND

2.2.43 AT / ATX Mode Selection (PSON1)

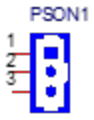


Table 2.42: PSON1

Pin	Signal
1	AT
2	+3.3V
3	ATX

2.2.44 CMOS Battery Connector (BAT1)

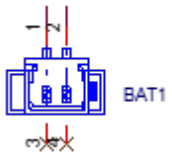


Table 2.43: BAT1	
Pin	**Signal**
1	+VBAT
2	GND

2.2.45 SIM Card Connector (SIM1)

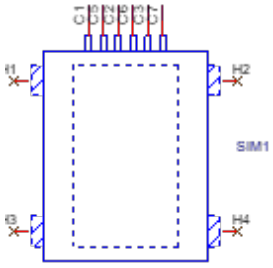


Table 2.44: SIM1	
Pin	**Signal**
C1	UIM_PWR
C5	GND
C2	UIM_RESET
C6	N.C.
C3	UIM_CLK
C7	UIM_DATA

2.2.46 Flash Descriptor Security Override Switch (SW_ME1)

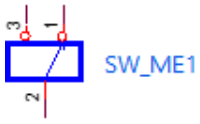


Table 2.45: SW_ME1	
Pin	**Signal**
1	N.C
2	Enable security measures defined in flash descriptor.(default)
3	Disable flash descriptor security (override)

2.2.47 SPI BIOS Flash Socket (SPI1)

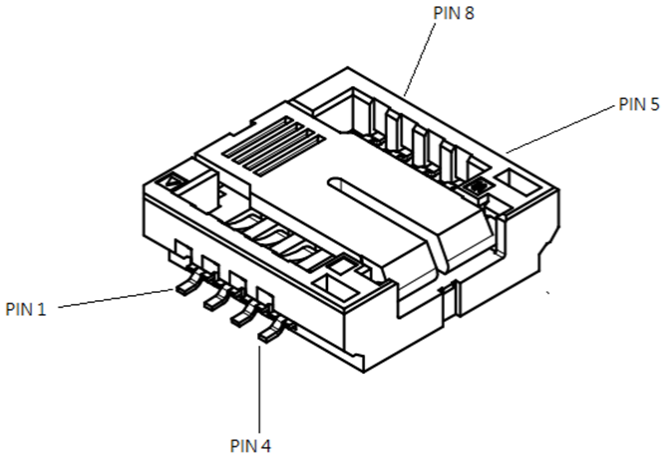


Table 2.46: SPI1

Pin	Signal	Pin	Signal
1	CS#	5	MOSI
2	MISO	6	SCLK
3	WP# / IO2	7	HOLD# / IO3
4	GND	8	+V3.3_SPI

2.2.48 IT5782VG Programming Header (JSMBUS1)

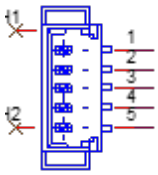


Table 2.47: JSMBUS1

Pin	Signal
1	Advantech defined
2	+V3.3_A_SIO
3	SMB_CLK_EC
4	SMB_DAT_EC
5	GND

Chapter 3

BIOS Operation

3.1 Introduction

With the AMI BIOS Setup program, you can modify BIOS settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning special features on or off. This chapter describes the basic navigation of the AIMB-234 setup screens.

3.2 BIOS Setup

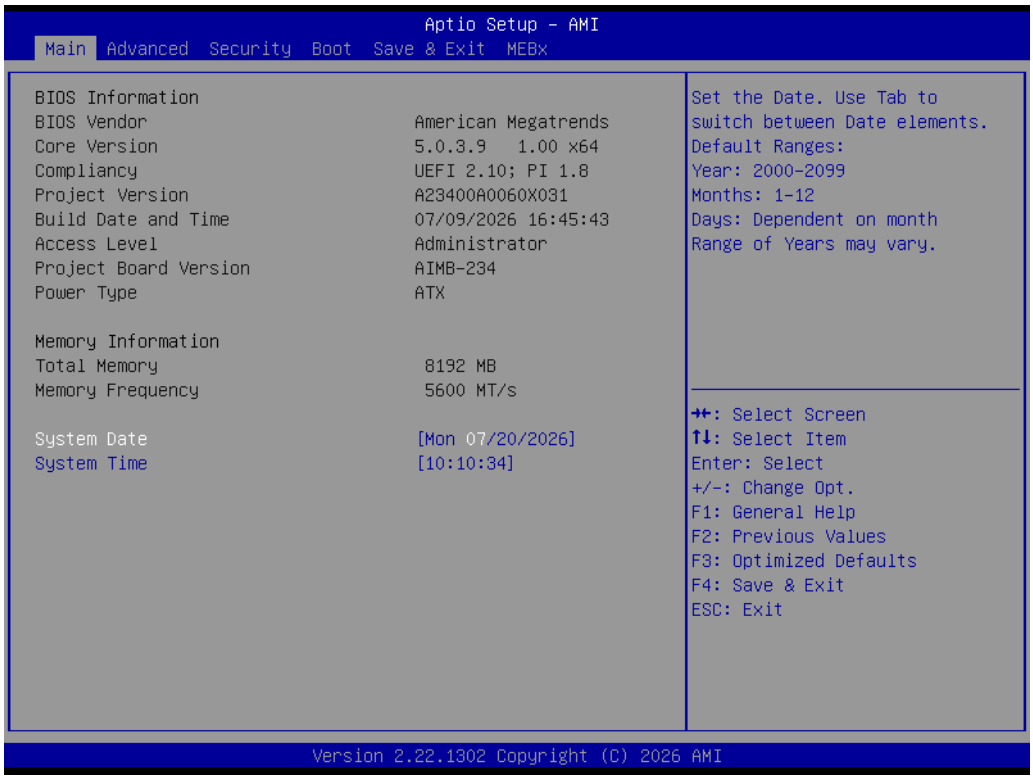
The AIMB-234 Series system has AMI BIOS built in, with a CMOS SETUP utility that allows users to configure required settings or to activate certain system features. The CMOS SETUP saves the configuration in the CMOS RAM of the motherboard. When the power is turned off, the battery on the board supplies the necessary power to preserve the CMOS RAM.

When the power is turned on, press the <Del> button during the BIOS POST (Power-On Self-Test) to access the CMOS SETUP screen.

Control Keys	
< ↑ >< ↓ >< ← >< → >	Move to select item
<Enter>	Select item
<Esc>	Main Menu - Quit and do not save changes into CMOS sub menu - Exit current page and return to main menu
<Page Up/+>	Increase the numeric value or make changes
<Page Down/->	Decrease the numeric value or make changes
<F1>	General help, for setup sub menu
<F2>	Item help
<F5>	Load previous values
<F7>	Load setup defaults
<F10>	Save all CMOS changes

3.2.1 Main Menu

Press <Del> to enter the AMI BIOS CMOS Setup Utility. The Main Menu will appear on the screen. Use the arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.



The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the legend. Above the legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

- **System time / System date**

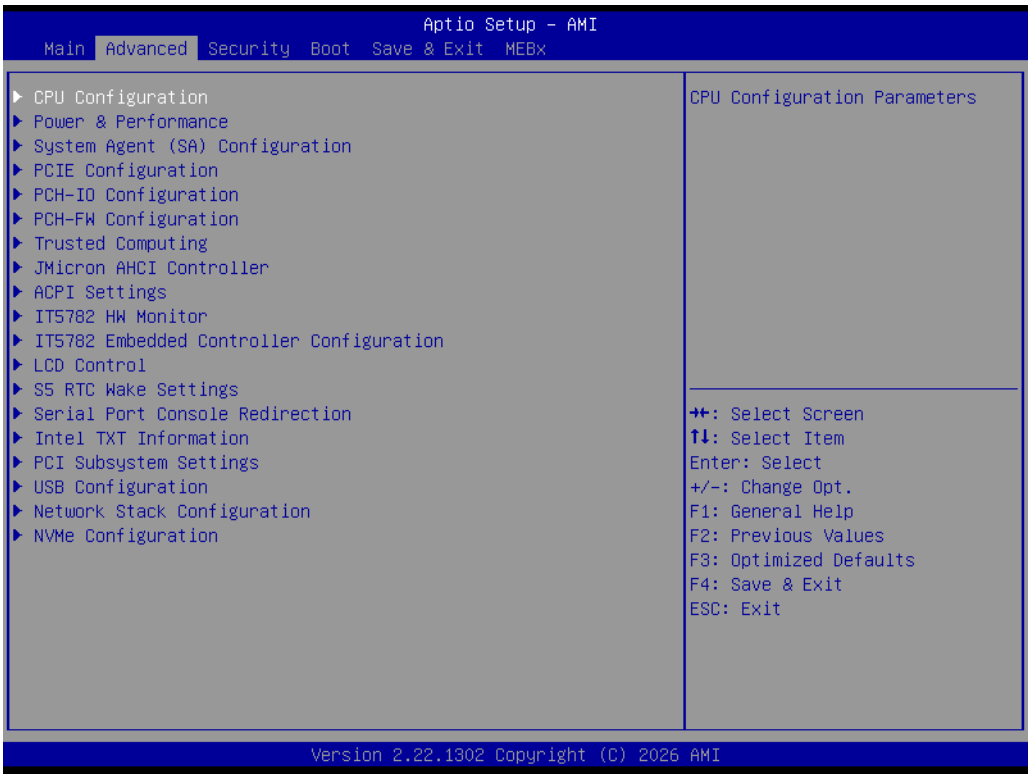
  Use this option to change the system time and date. Highlight the System Time or System Date using the keys. Enter new values via the keyboard. Press the or keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

3.2.2 Advanced BIOS Features

Select the Advanced tab from the AIMB-234 setup menu to enter the Advanced BIOS setup page. Users can select any item in the left frame of the screen, such as CPU configuration. Select an Advanced BIOS setup option by highlighting the text using the keys. All Advanced BIOS setup options are described in this section. The Advanced BIOS setup menu screen is shown below. The sub-menus are described in the following pages.

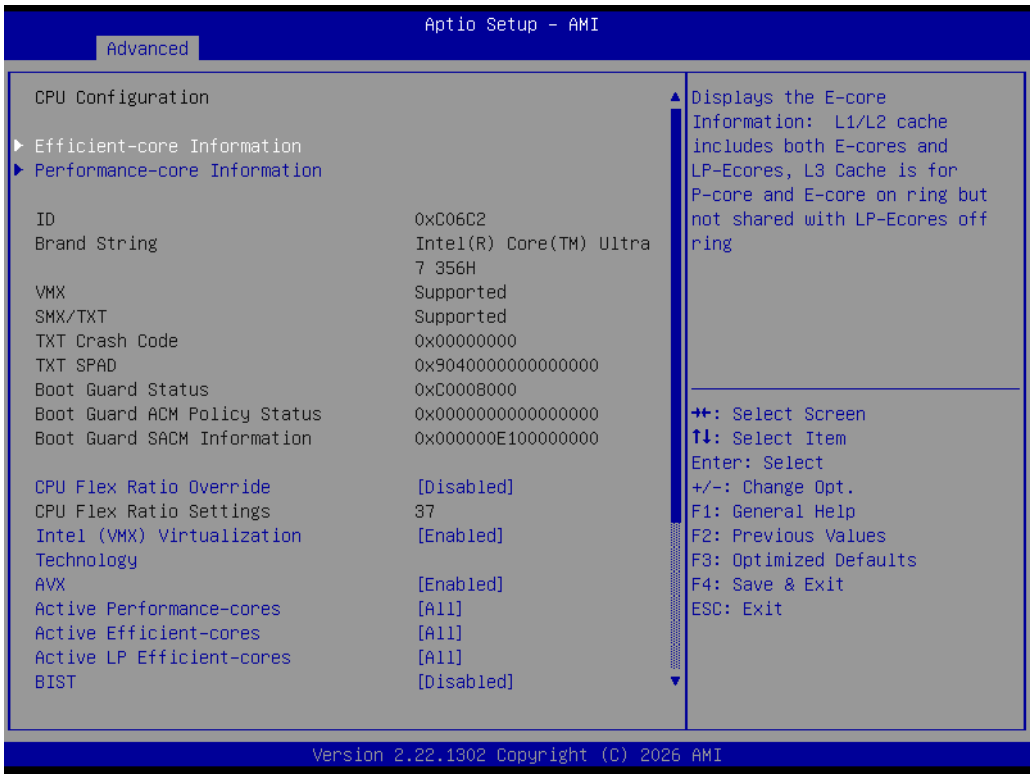
3.2.2.1 CPU Configuration

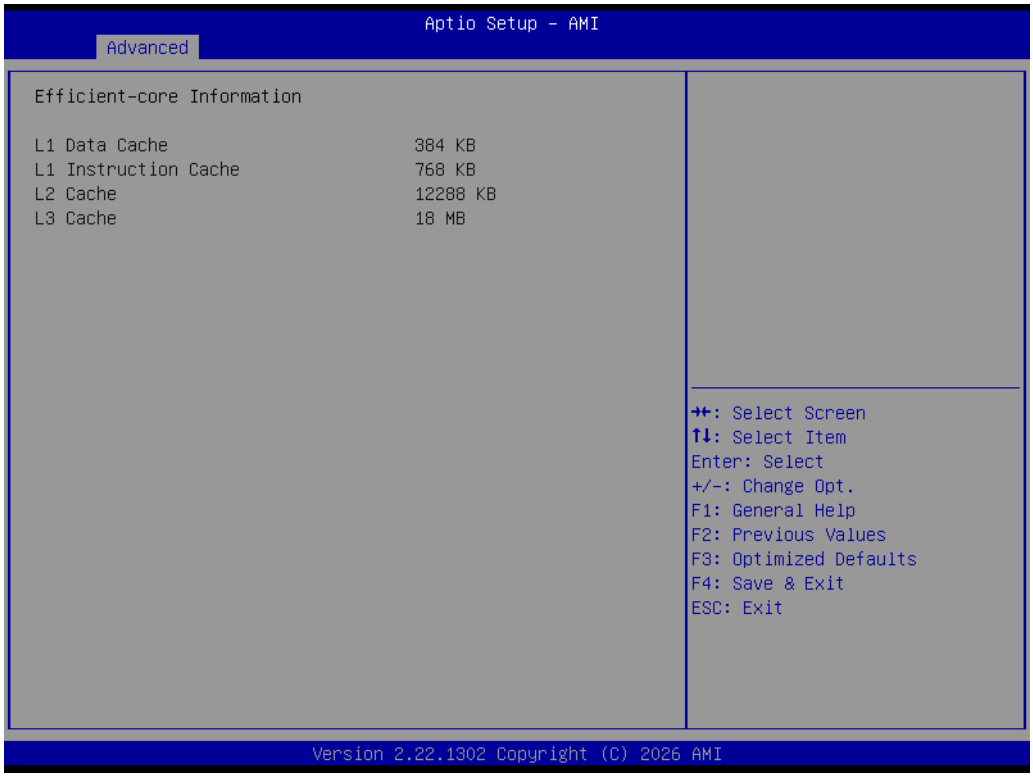
Advanced → CPU Configuration



Efficient-core Information

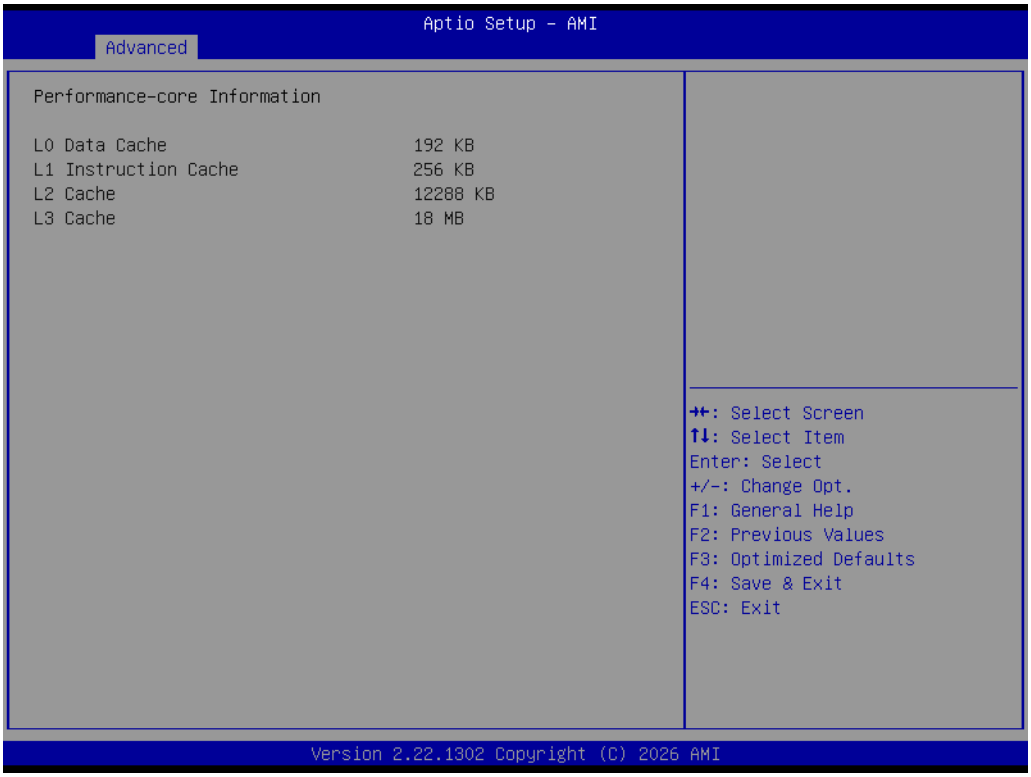
Advanced → CPU Configuration → Efficient-core Information





Performance-core Information

Advanced → CPU Configuration → Performance-core Information



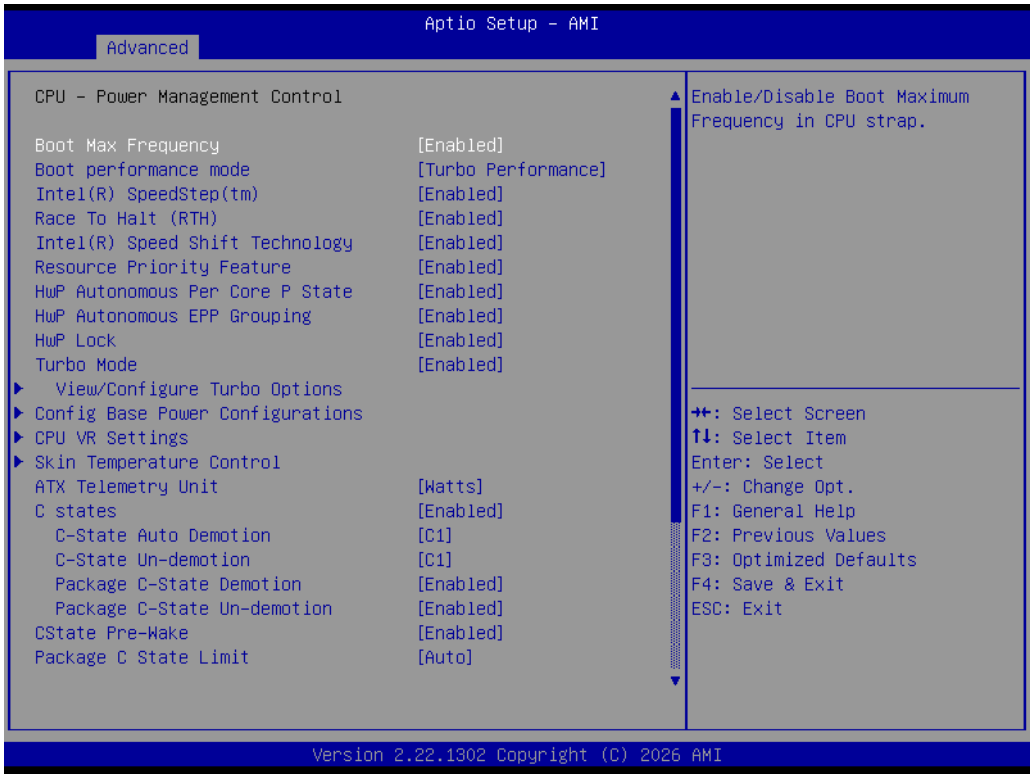
3.2.2.2 Power & Performance

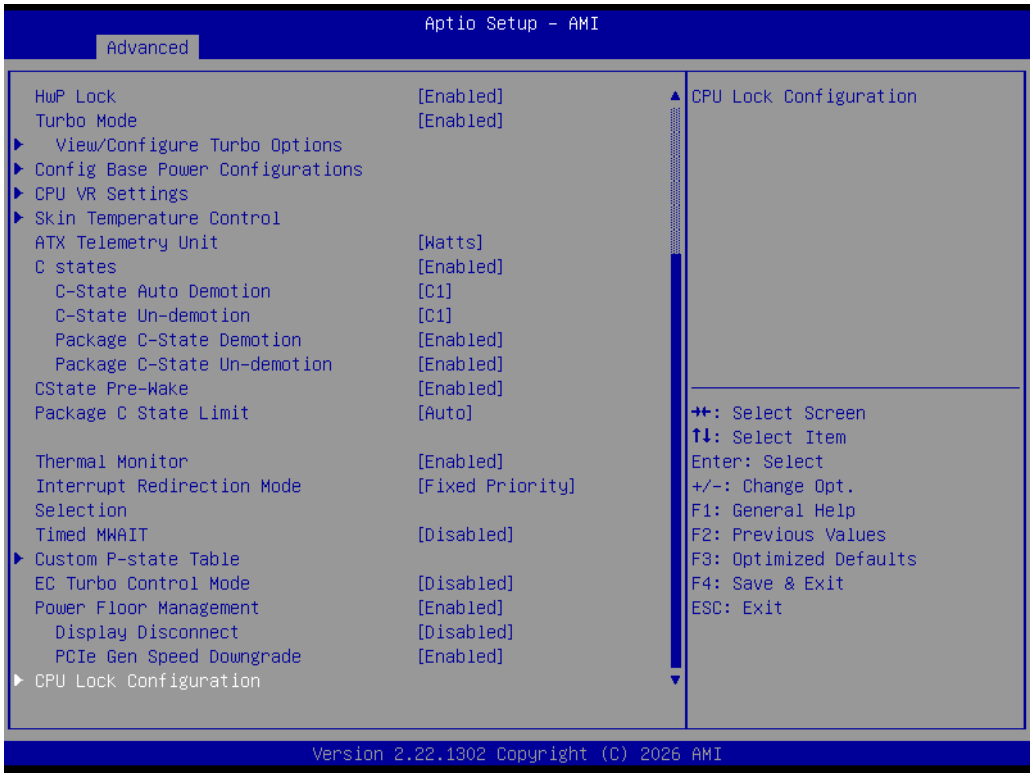
Advanced → Power & Performance



CPU – Power Management Control

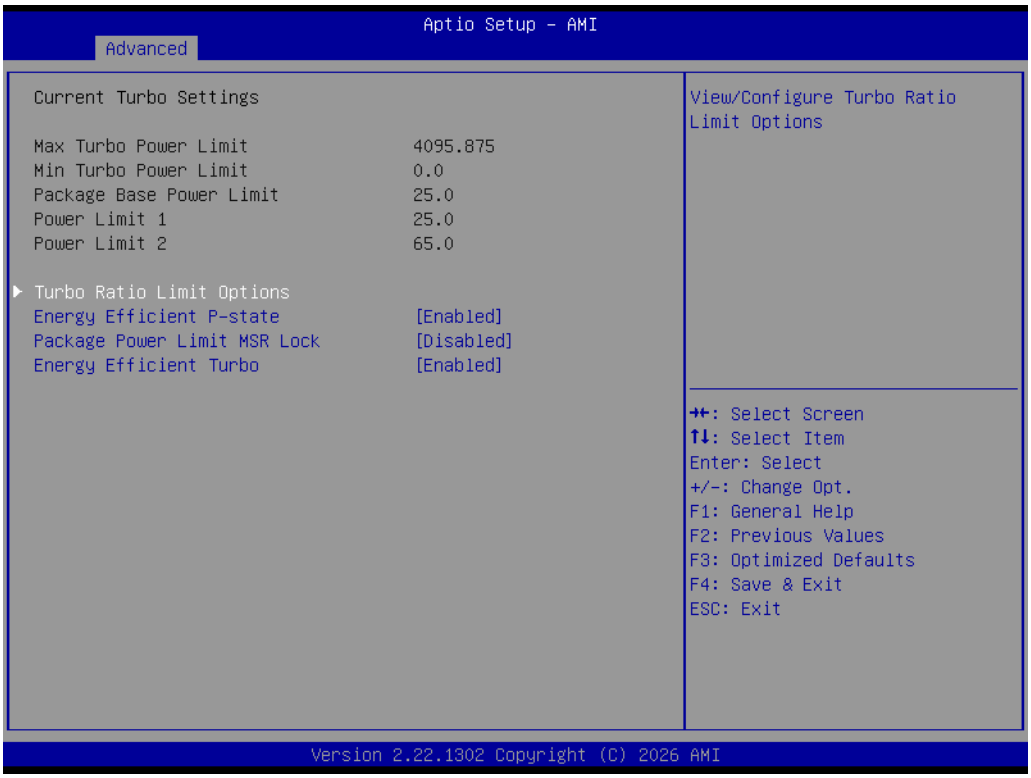
Advanced → Power & Performance → CPU – Power Management Control

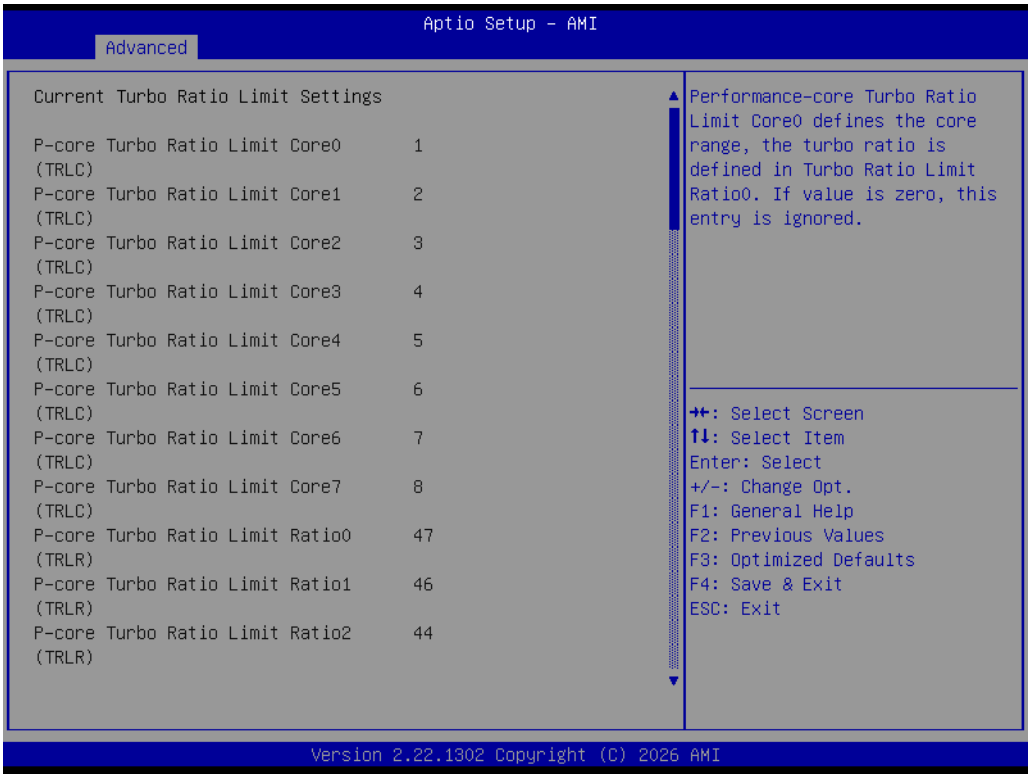


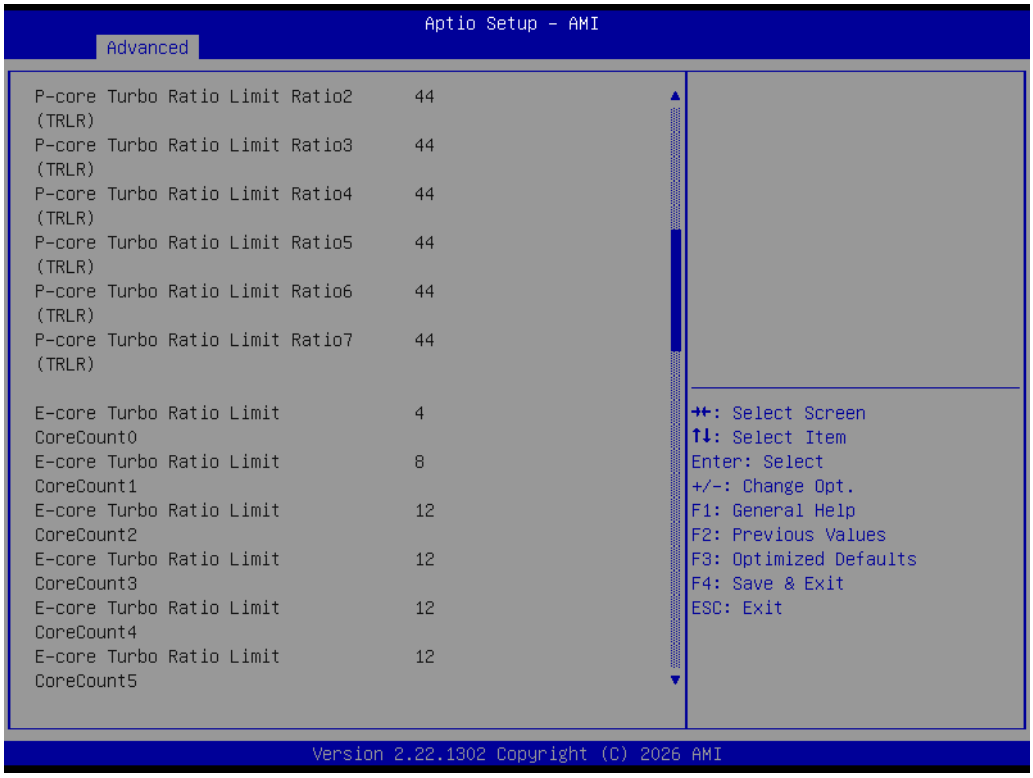


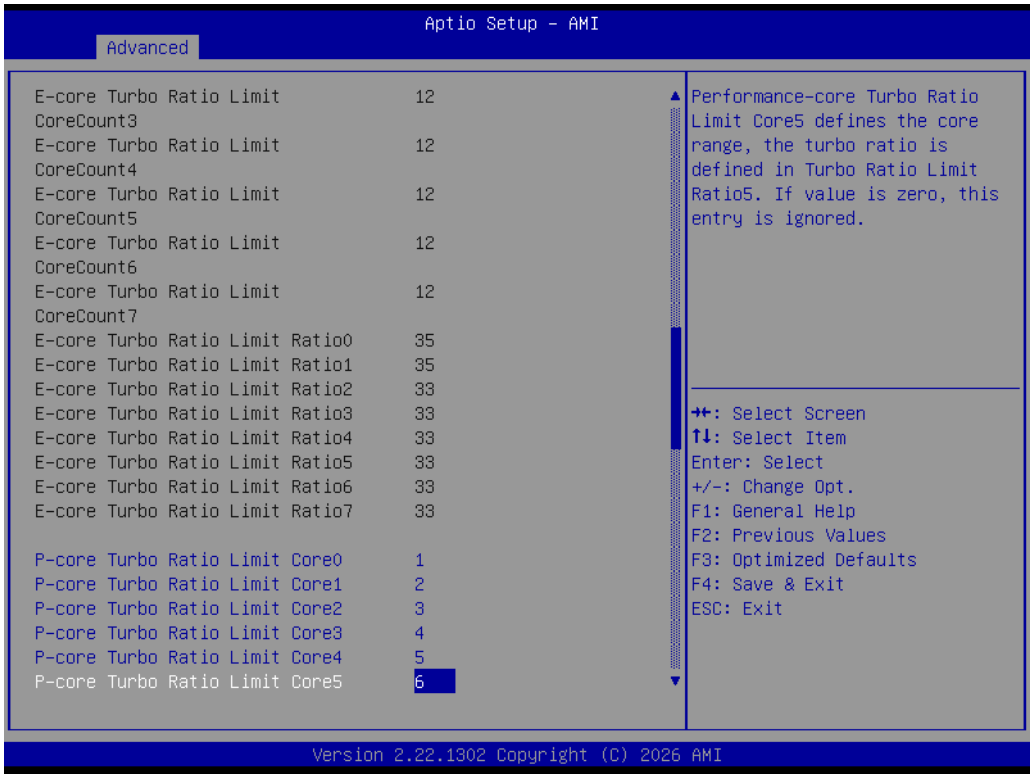
Turbo Ratio Limit Options

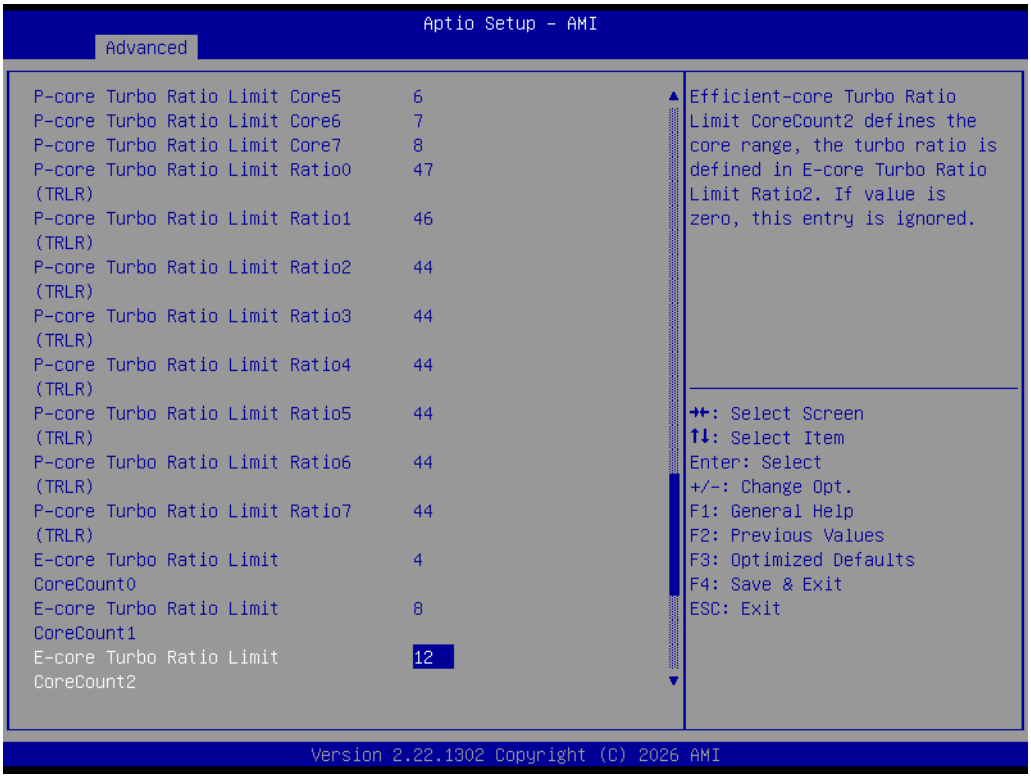
Advanced → Power & Performance → CPU – Power Management Control → View/ Configure Turbo Ratio → Turbo Ratio Limit Options

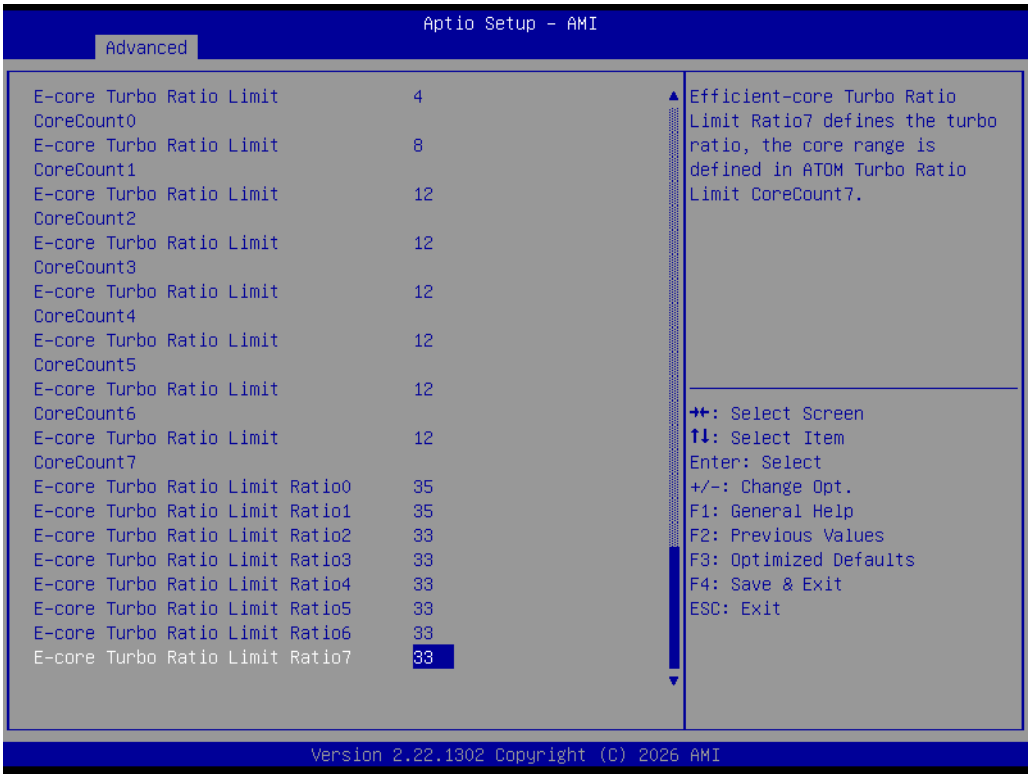


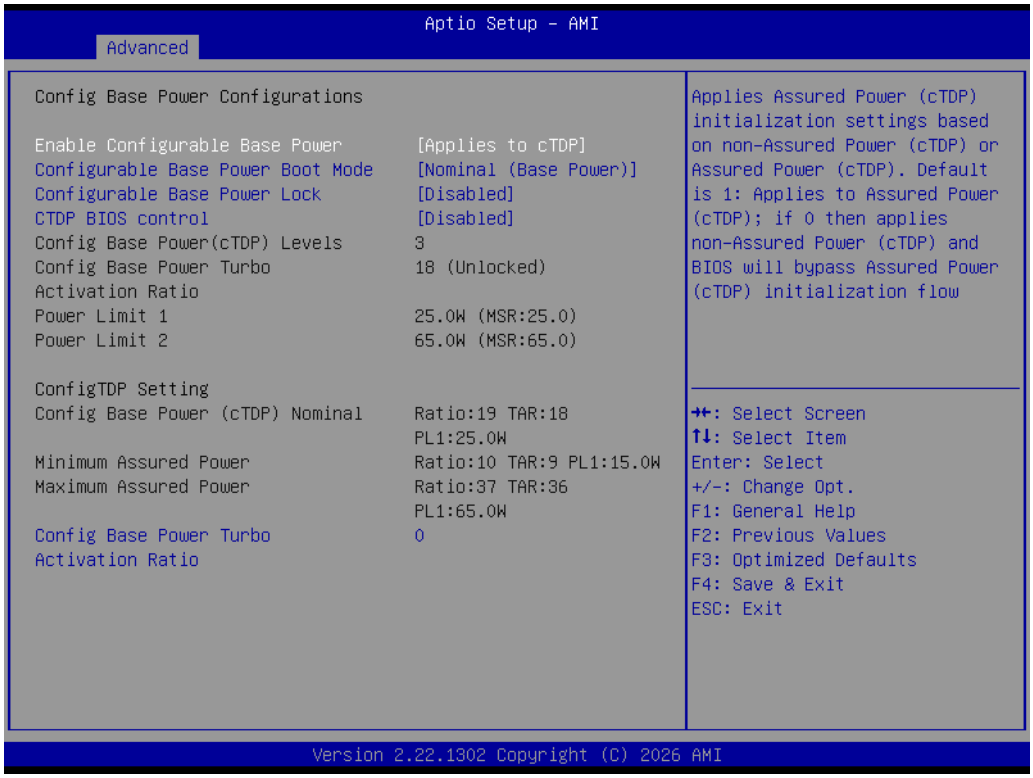



Aptio Setup – AMI
Advanced
P-core Turbo Ratio Limit Ratio2 (TRLR) 44
P-core Turbo Ratio Limit Ratio3 (TRLR) 44
P-core Turbo Ratio Limit Ratio4 (TRLR) 44
P-core Turbo Ratio Limit Ratio5 (TRLR) 44
P-core Turbo Ratio Limit Ratio6 (TRLR) 44
P-core Turbo Ratio Limit Ratio7 (TRLR) 44
E-core Turbo Ratio Limit CoreCount0 4
E-core Turbo Ratio Limit CoreCount1 8
E-core Turbo Ratio Limit CoreCount2 12
E-core Turbo Ratio Limit CoreCount3 12
E-core Turbo Ratio Limit CoreCount4 12
E-core Turbo Ratio Limit CoreCount5 12
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
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Aptio Setup – AMI
Advanced
E-core Turbo Ratio Limit CoreCount3 12
E-core Turbo Ratio Limit CoreCount4 12
E-core Turbo Ratio Limit CoreCount5 12
E-core Turbo Ratio Limit CoreCount6 12
E-core Turbo Ratio Limit CoreCount7 12
E-core Turbo Ratio Limit Ratio0 35
E-core Turbo Ratio Limit Ratio1 35
E-core Turbo Ratio Limit Ratio2 33
E-core Turbo Ratio Limit Ratio3 33
E-core Turbo Ratio Limit Ratio4 33
E-core Turbo Ratio Limit Ratio5 33
E-core Turbo Ratio Limit Ratio6 33
E-core Turbo Ratio Limit Ratio7 33
P-core Turbo Ratio Limit Core0 1
P-core Turbo Ratio Limit Core1 2
P-core Turbo Ratio Limit Core2 3
P-core Turbo Ratio Limit Core3 4
P-core Turbo Ratio Limit Core4 5
P-core Turbo Ratio Limit Core5 6
Performance-core Turbo Ratio Limit Core5 defines the core range, the turbo ratio is defined in Turbo Ratio Limit Ratio5. If value is zero, this entry is ignored.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
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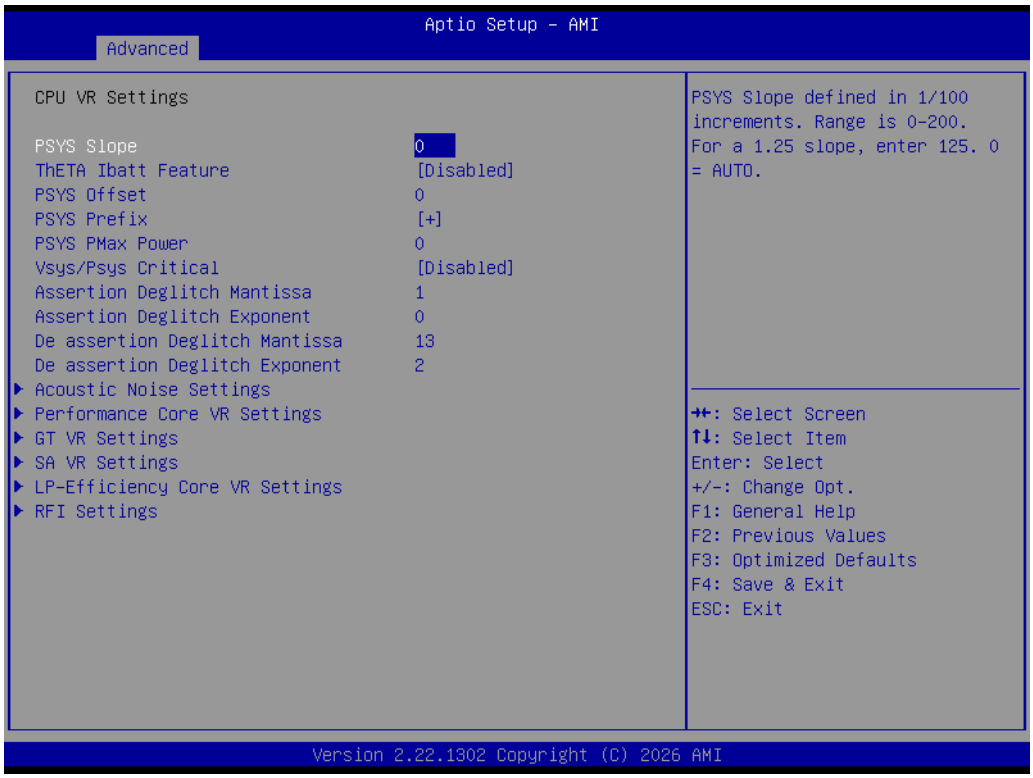

Aptio Setup – AMI
Advanced
P-core Turbo Ratio Limit Core5 6
P-core Turbo Ratio Limit Core6 7
P-core Turbo Ratio Limit Core7 8
P-core Turbo Ratio Limit Ratio0 (TRLR) 47
P-core Turbo Ratio Limit Ratio1 (TRLR) 46
P-core Turbo Ratio Limit Ratio2 (TRLR) 44
P-core Turbo Ratio Limit Ratio3 (TRLR) 44
P-core Turbo Ratio Limit Ratio4 (TRLR) 44
P-core Turbo Ratio Limit Ratio5 (TRLR) 44
P-core Turbo Ratio Limit Ratio6 (TRLR) 44
P-core Turbo Ratio Limit Ratio7 (TRLR) 44
E-core Turbo Ratio Limit CoreCount0 4
E-core Turbo Ratio Limit CoreCount1 8
E-core Turbo Ratio Limit CoreCount2 12
Efficient-core Turbo Ratio Limit CoreCount2 defines the core range, the turbo ratio is defined in E-core Turbo Ratio Limit Ratio2. If value is zero, this entry is ignored.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1302 Copyright (C) 2026 AMI


Aptio Setup – AMI
Advanced
E-core Turbo Ratio Limit CoreCount0 4
E-core Turbo Ratio Limit CoreCount1 8
E-core Turbo Ratio Limit CoreCount2 12
E-core Turbo Ratio Limit CoreCount3 12
E-core Turbo Ratio Limit CoreCount4 12
E-core Turbo Ratio Limit CoreCount5 12
E-core Turbo Ratio Limit CoreCount6 12
E-core Turbo Ratio Limit CoreCount7 12
E-core Turbo Ratio Limit Ratio0 35
E-core Turbo Ratio Limit Ratio1 35
E-core Turbo Ratio Limit Ratio2 33
E-core Turbo Ratio Limit Ratio3 33
E-core Turbo Ratio Limit Ratio4 33
E-core Turbo Ratio Limit Ratio5 33
E-core Turbo Ratio Limit Ratio6 33
E-core Turbo Ratio Limit Ratio7 33
Efficient-core Turbo Ratio Limit Ratio7 defines the turbo ratio, the core range is defined in ATOM Turbo Ratio Limit CoreCount7.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
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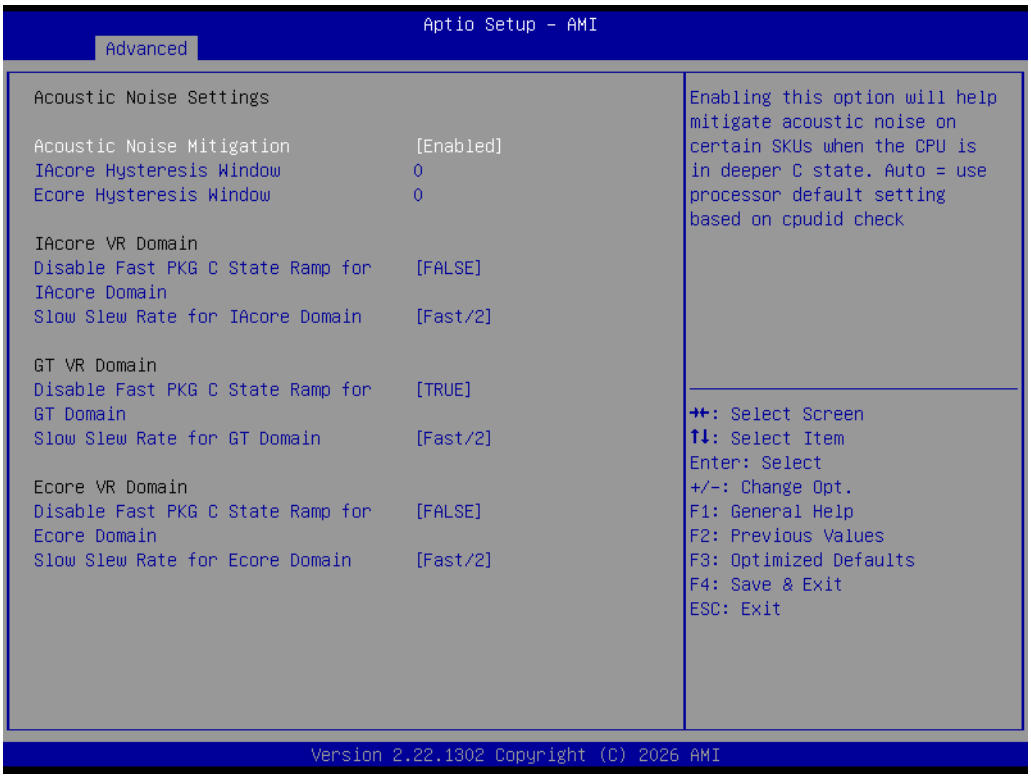
CPU VR Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings



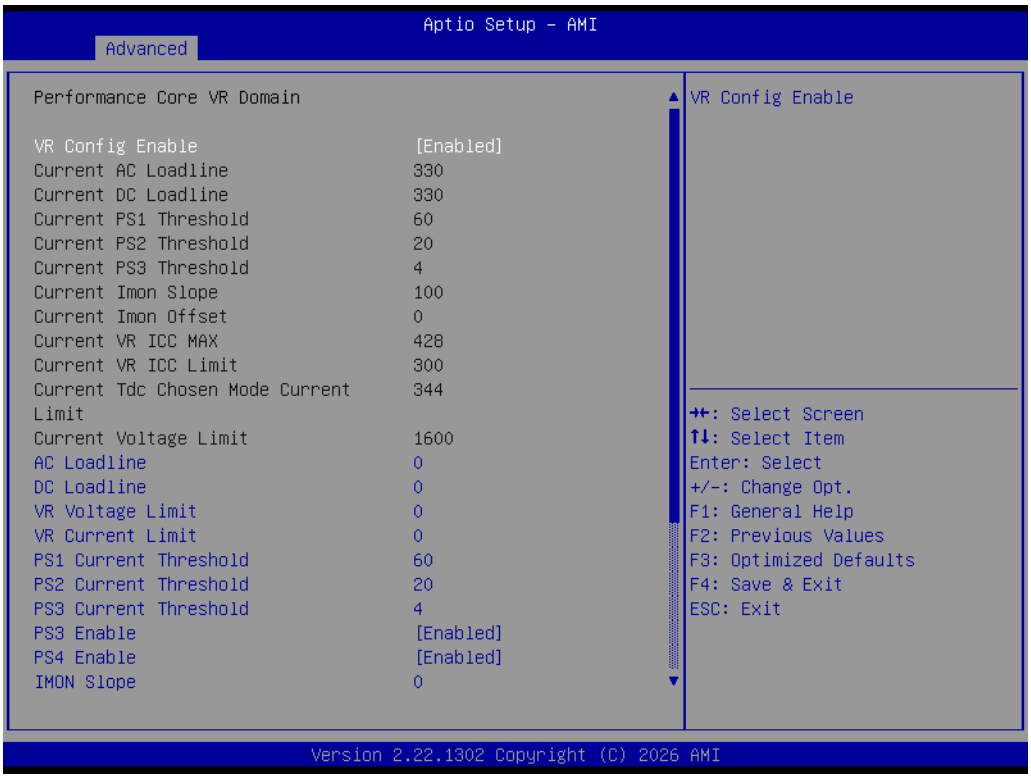
Acoustic Noise Settings

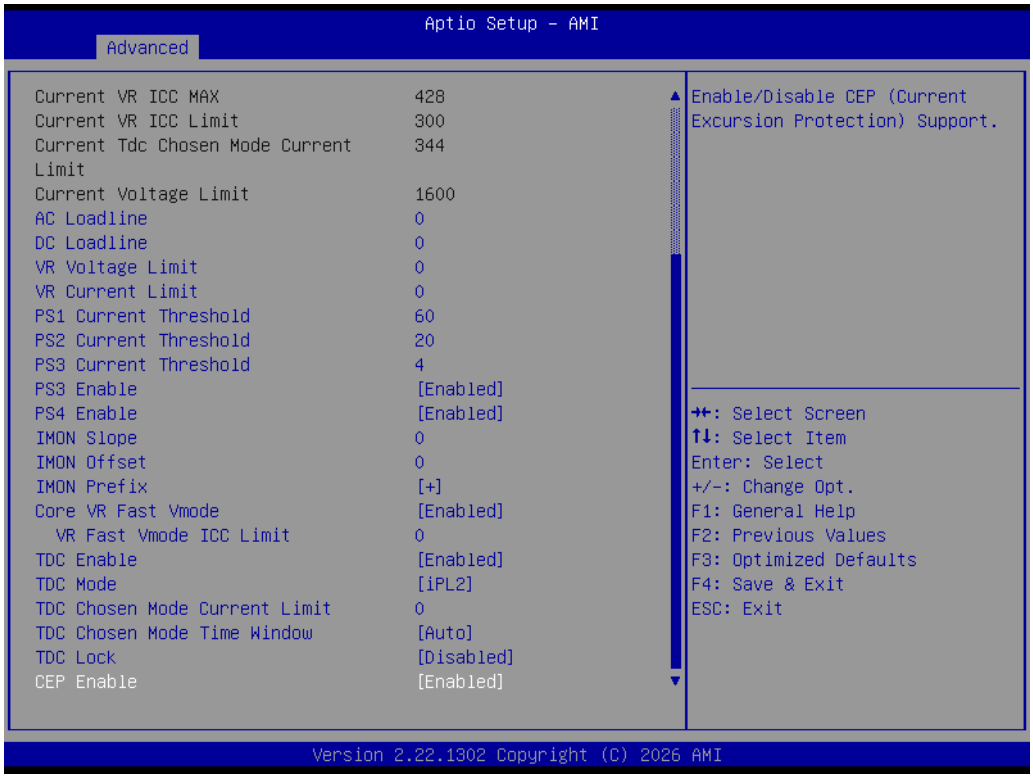
Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → Acoustic Noise Settings



Efficiency/Performance VR Settings

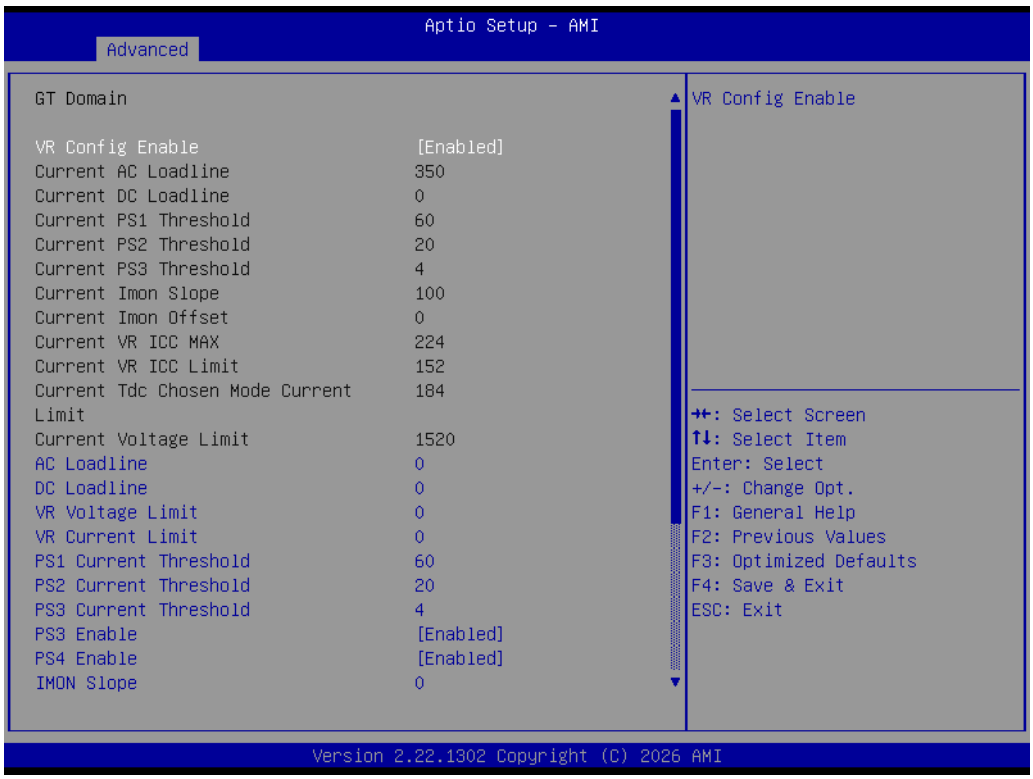
Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → Efficiency/Performance VR Settings





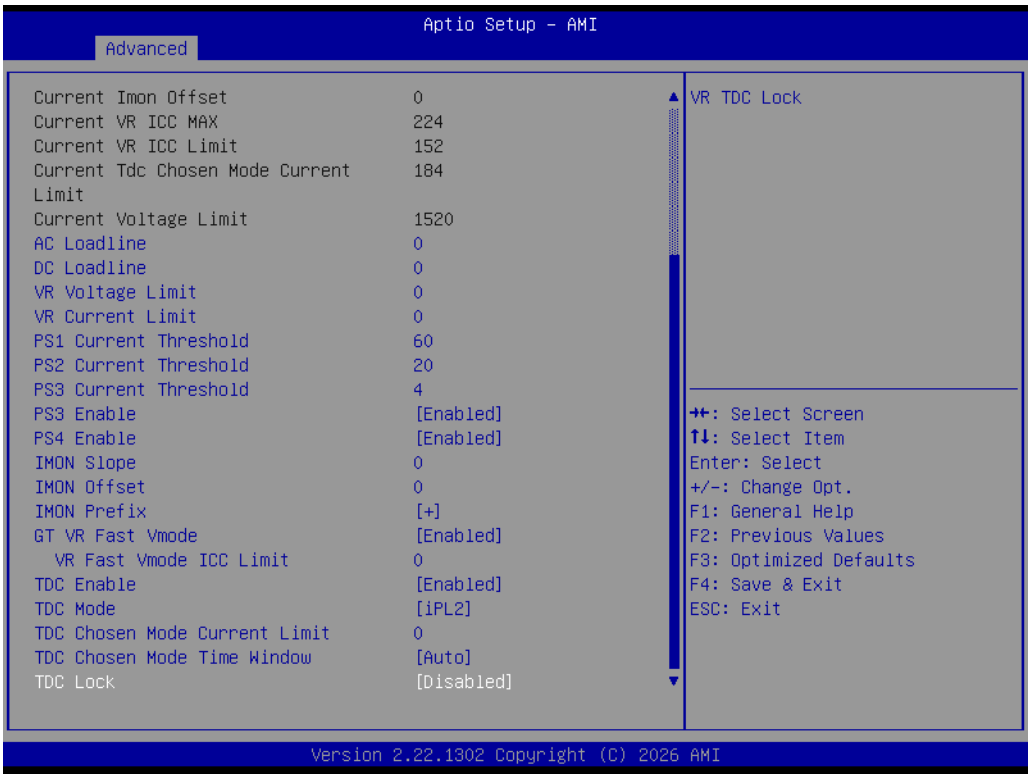
GT VR Settings

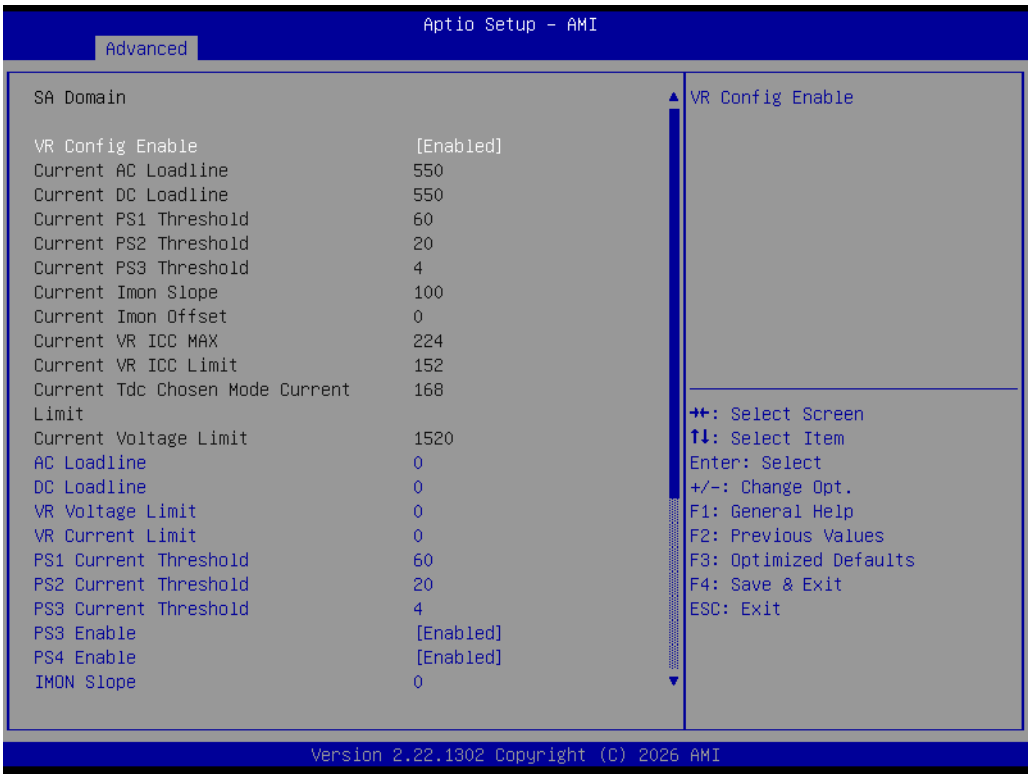
Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → GT VR Settings

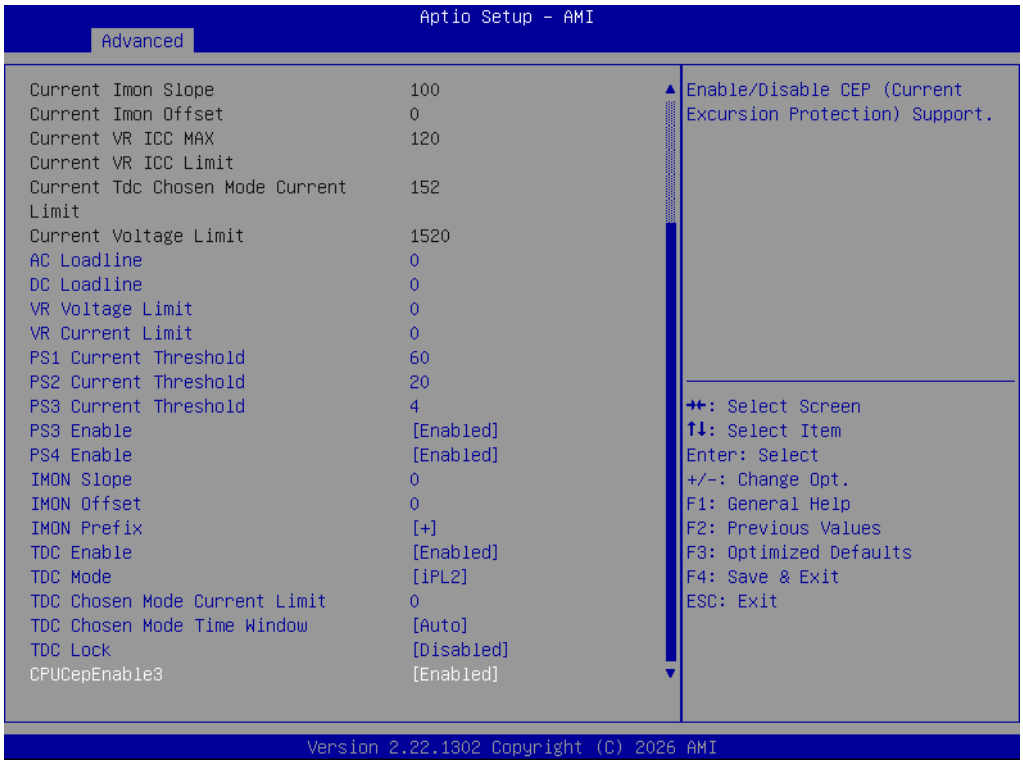


SA VR Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → SA VR Settings

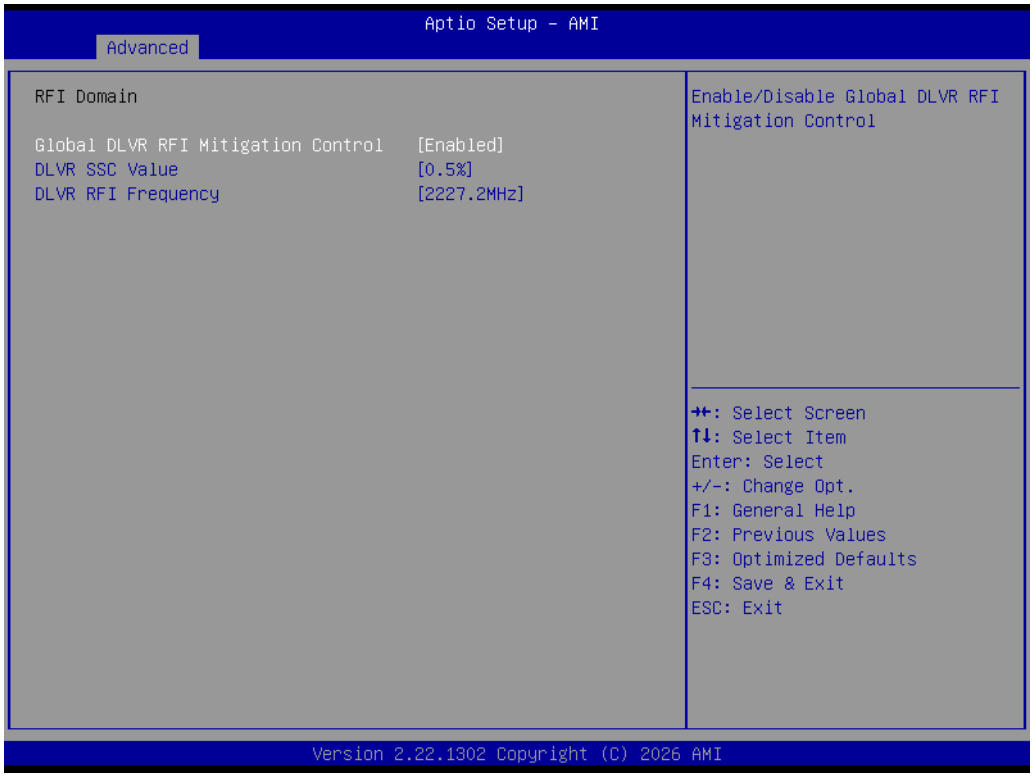






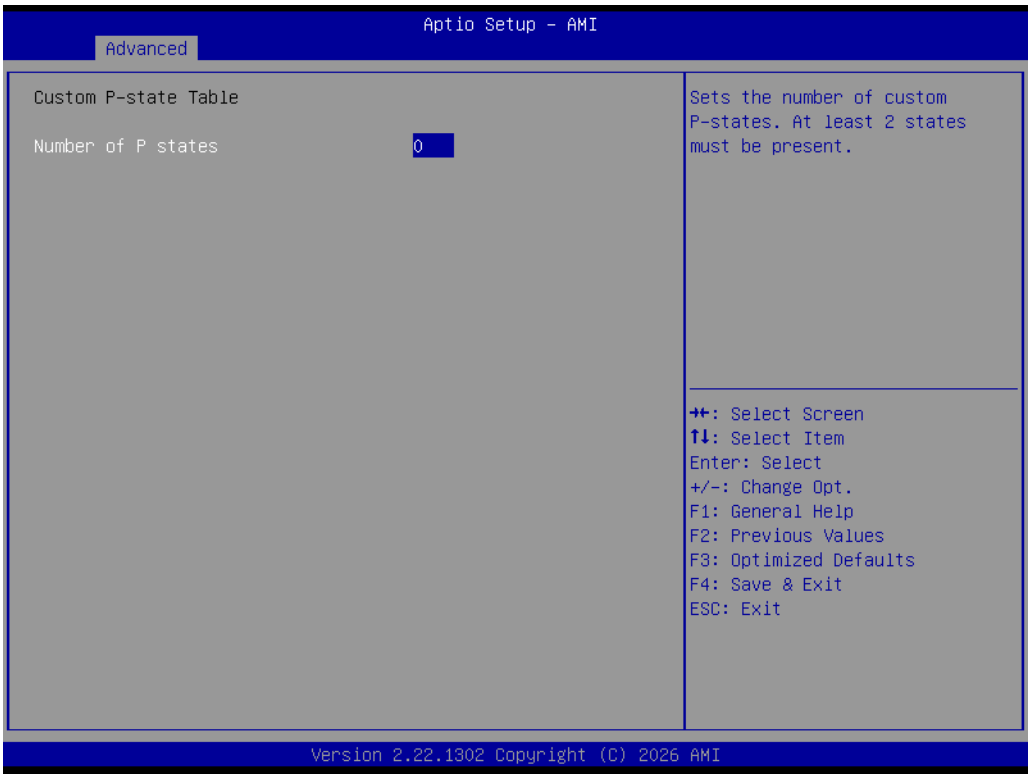
RFI Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → RFI Settings



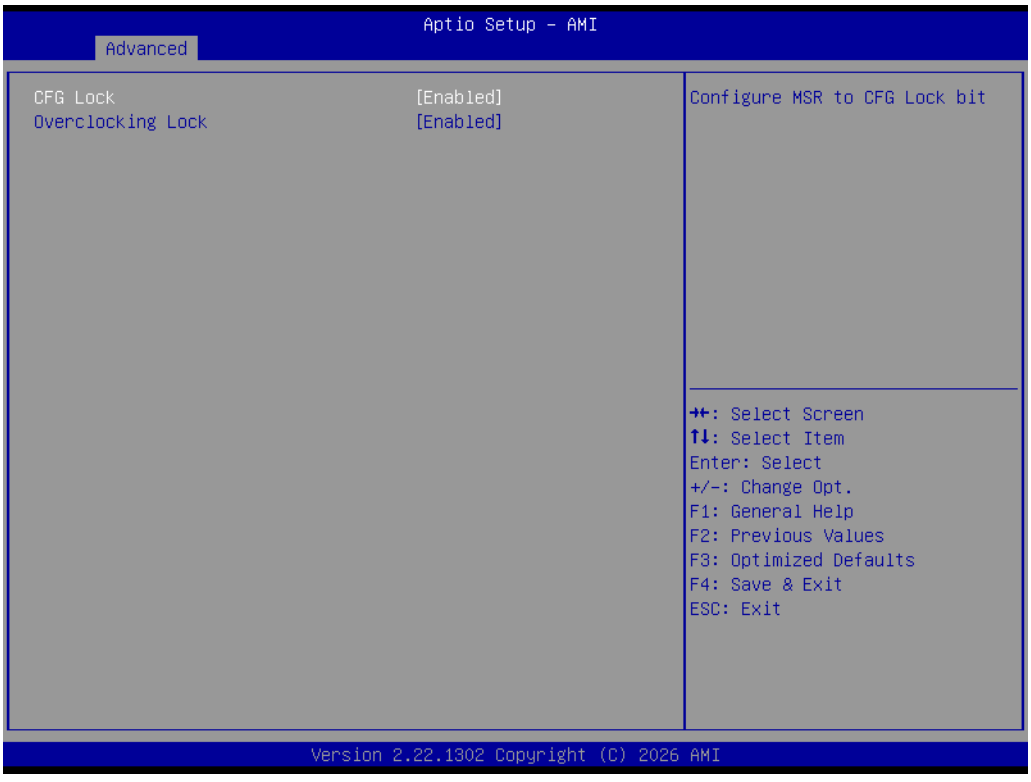
Custom P-state Table

Advanced → Power & Performance → CPU – Power Management Control → Custom P-state Table



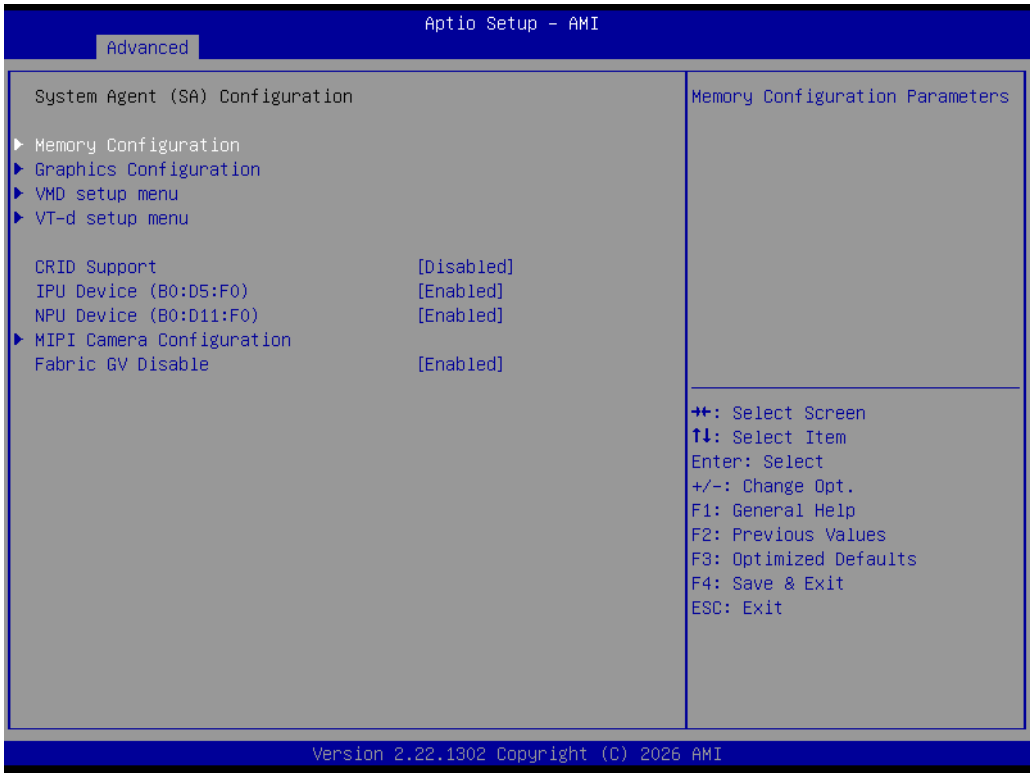
CFG Lock

Advanced → Power & Performance → CPU – Power Management Control → CFG Lock



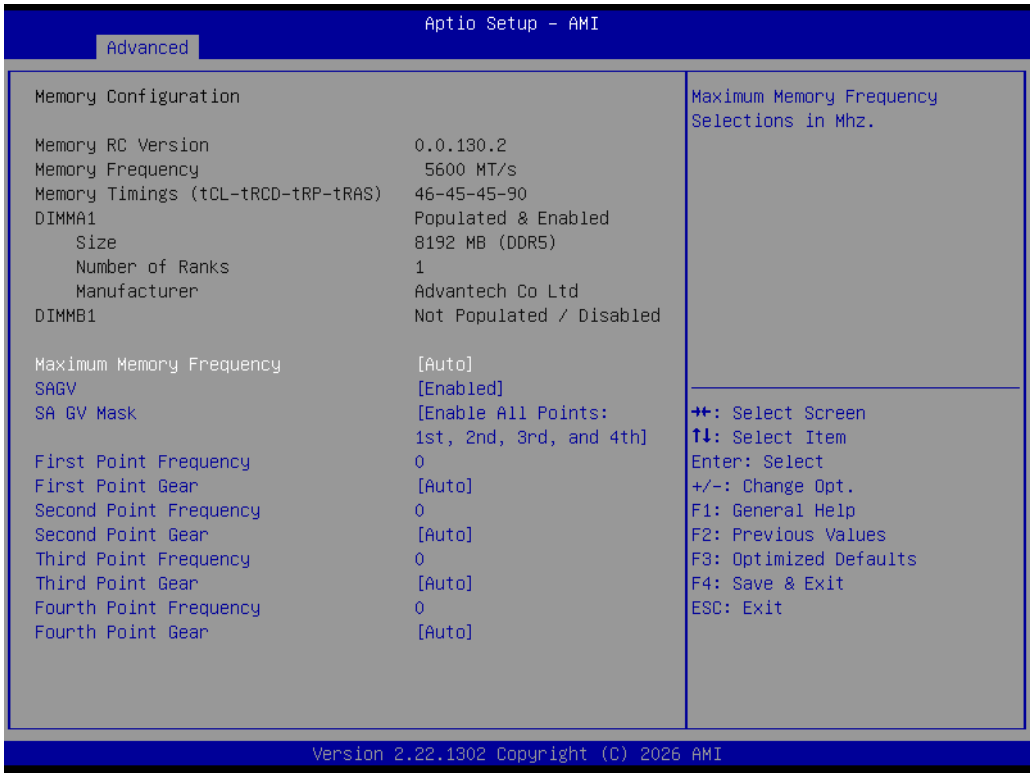
3.2.2.3 System Agent (SA) Configuration

Advanced → System Agent (SA) Configuration



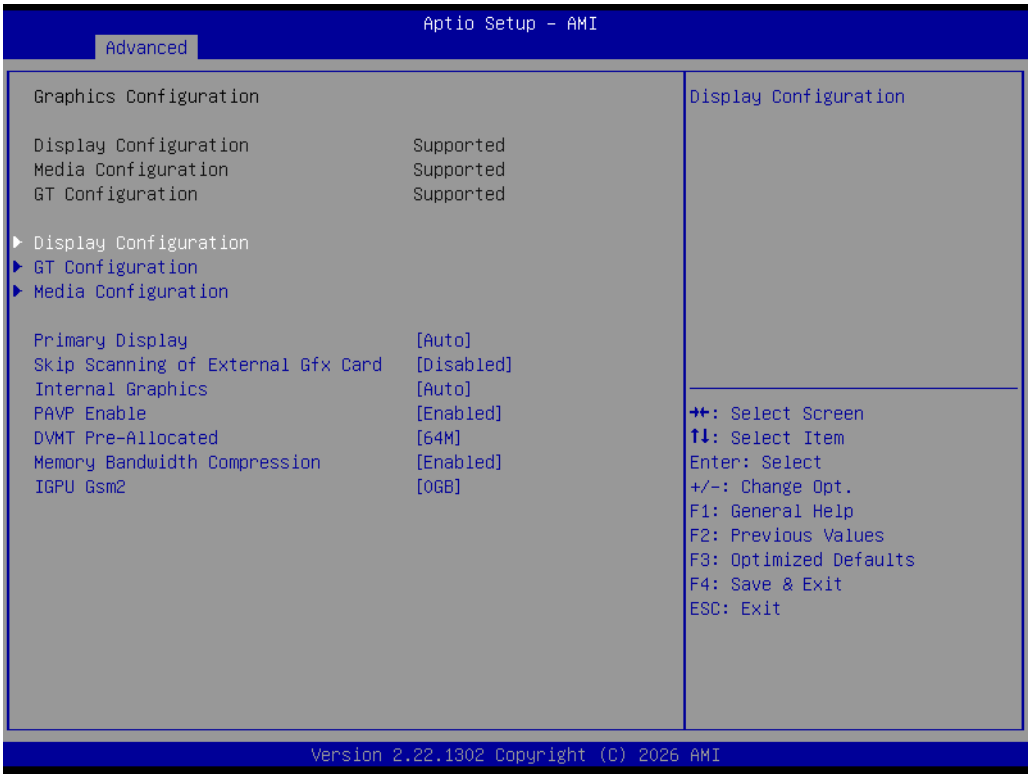
Memory Configuration

Advanced → System Agent (SA) Configuration → Memory Configuration

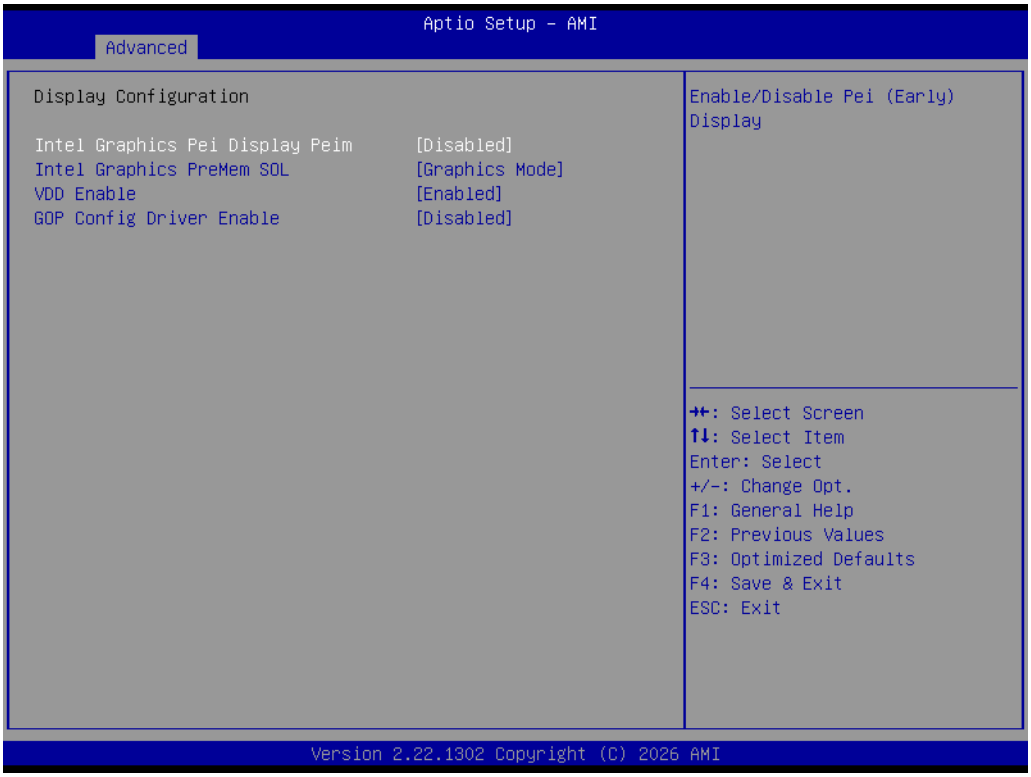


Graphics Configuration

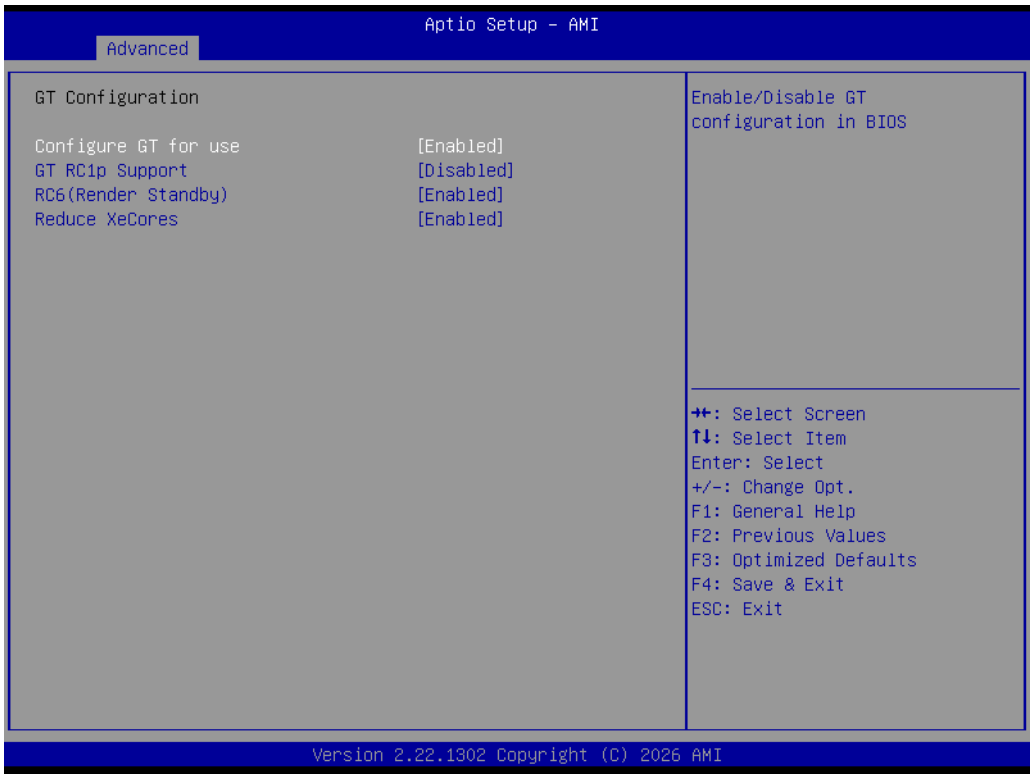
Advanced → System Agent (SA) Configuration → Graphics Configuration



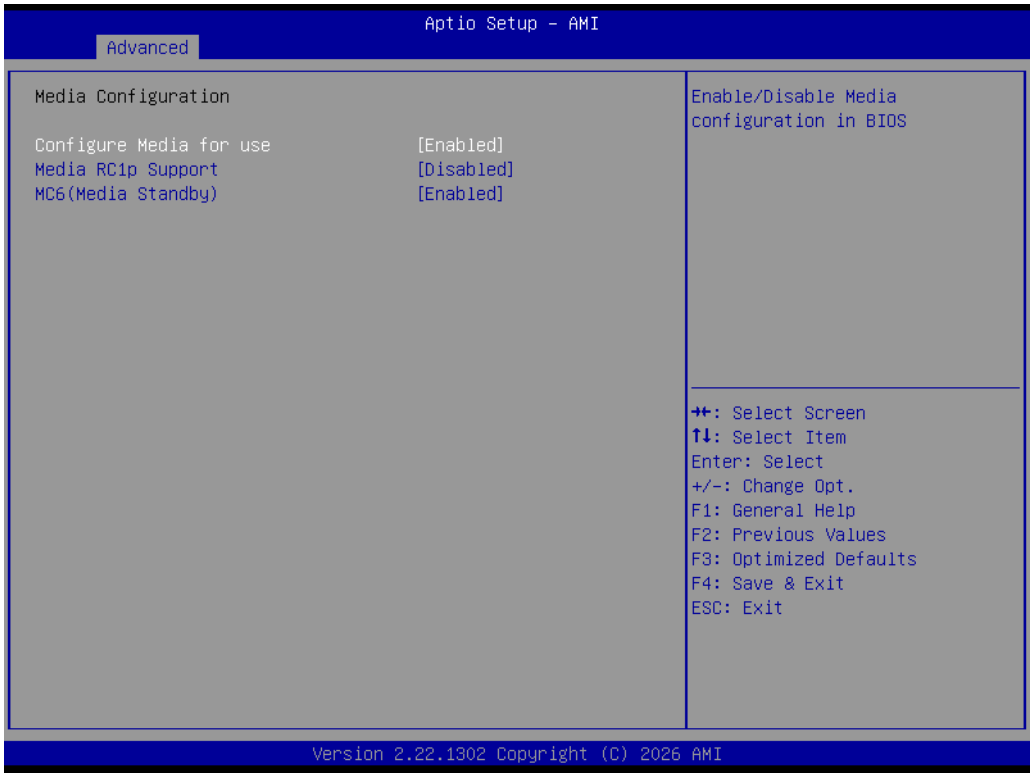
Advanced → System Agent (SA) Configuration → Graphics Configuration → Display Configuration



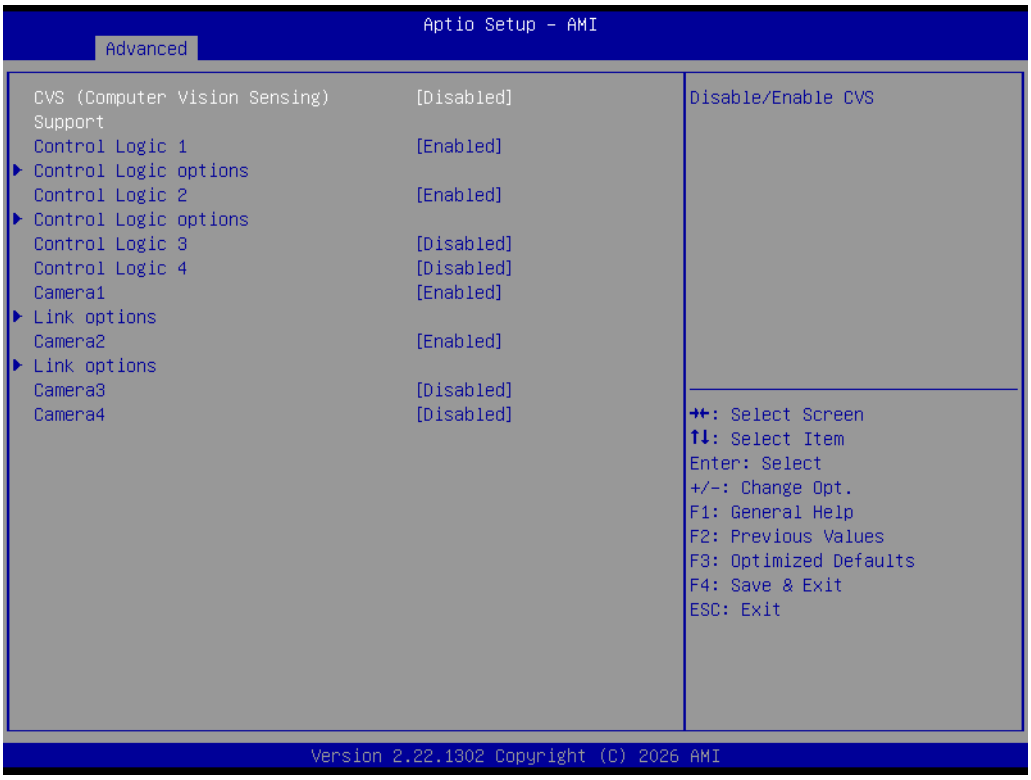
Advanced → System Agent (SA) Configuration → Graphics Configuration → GT Configuration

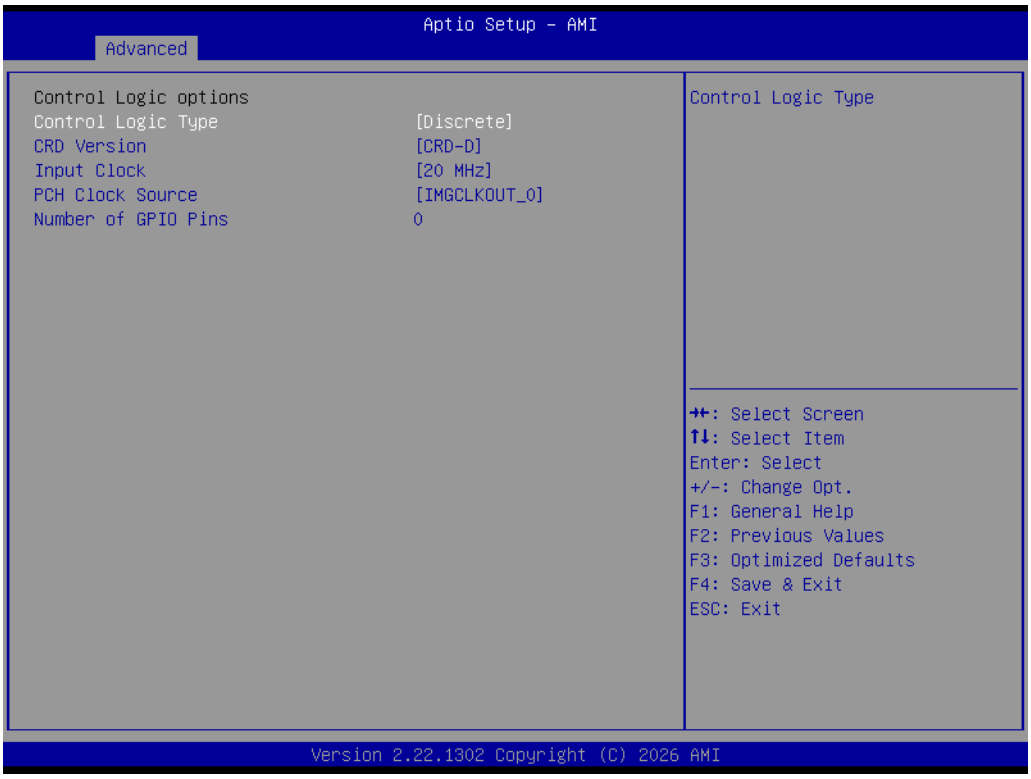


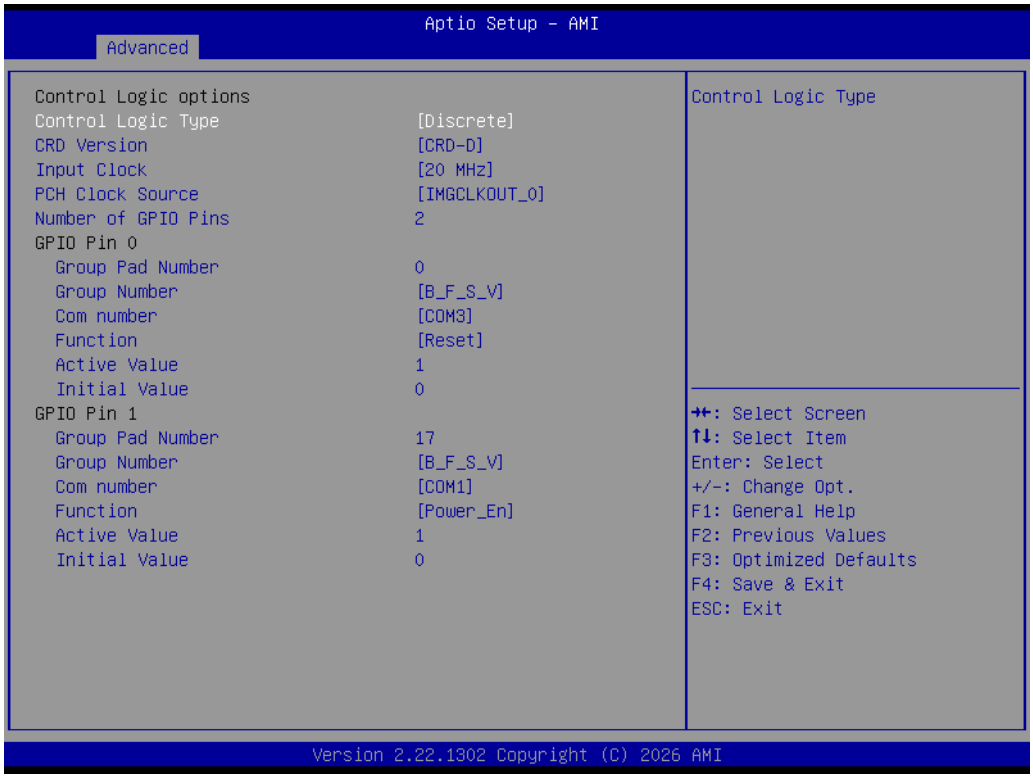
Advanced → System Agent (SA) Configuration → Graphics Configuration → Media Configuration



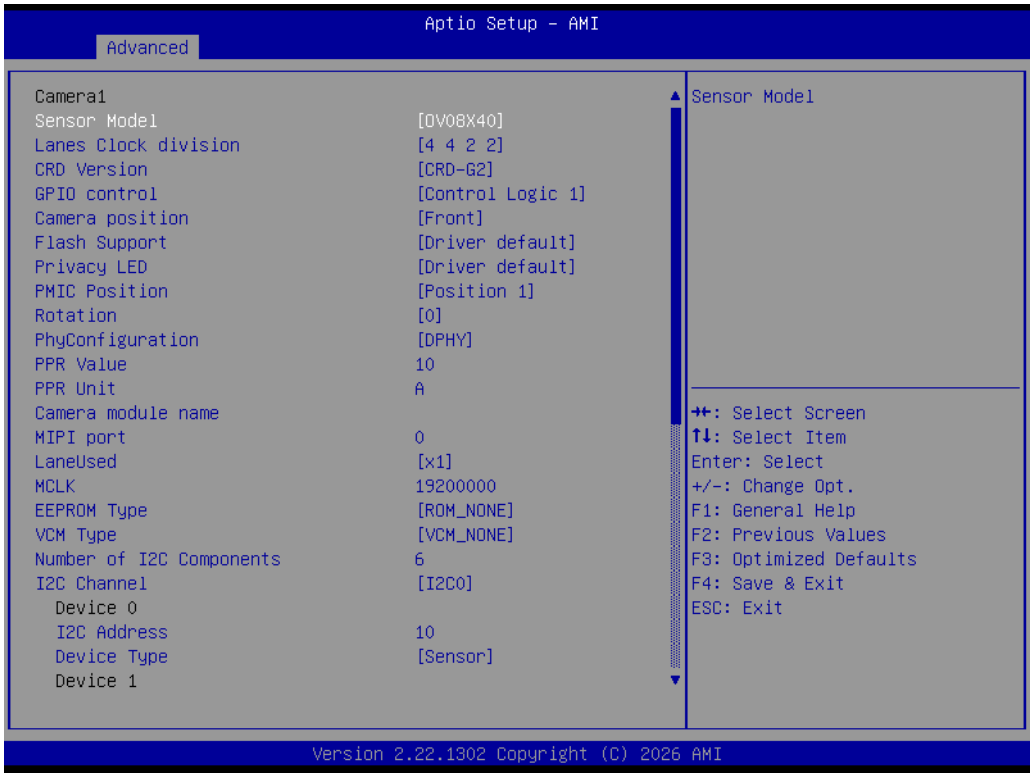
Advanced → System Agent (SA) Configuration → CSV (Computer Vision Sensing)





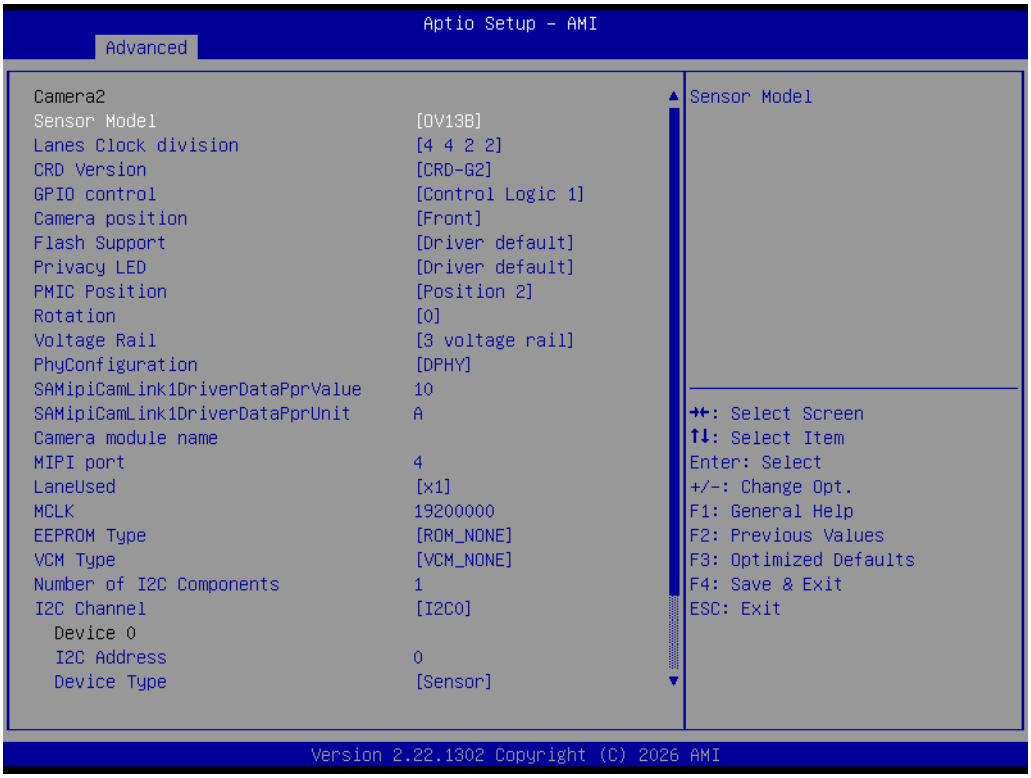


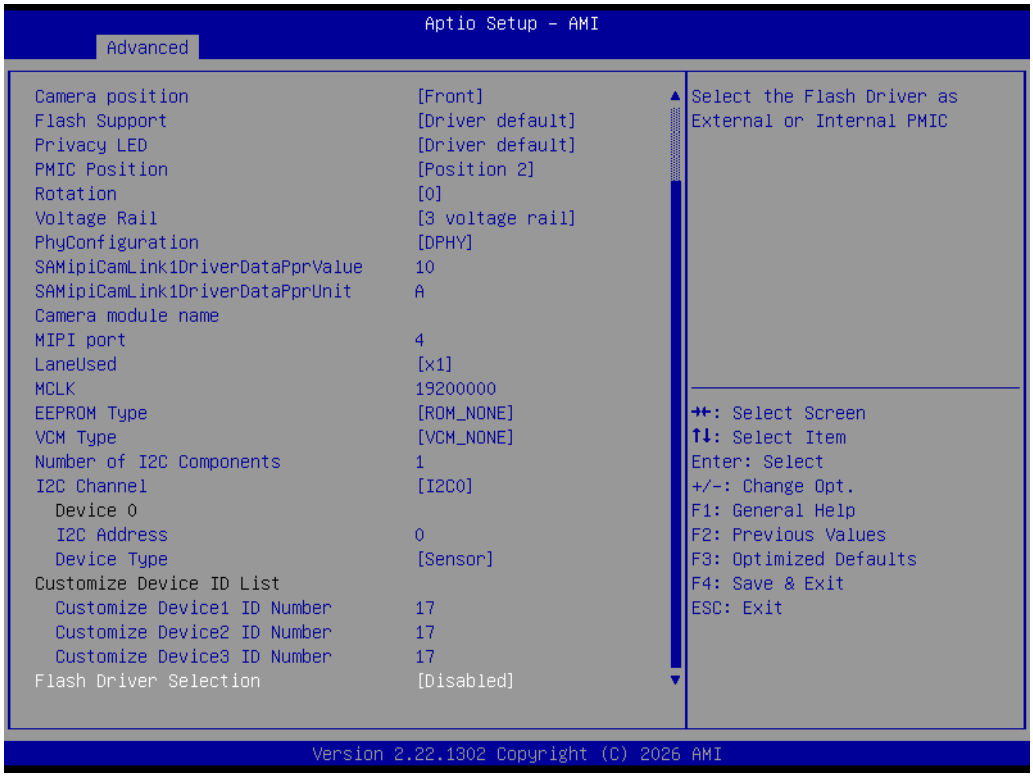
Advanced → System Agent (SA) Configuration → CSV (Computer Vision Sensing) → Camera 1





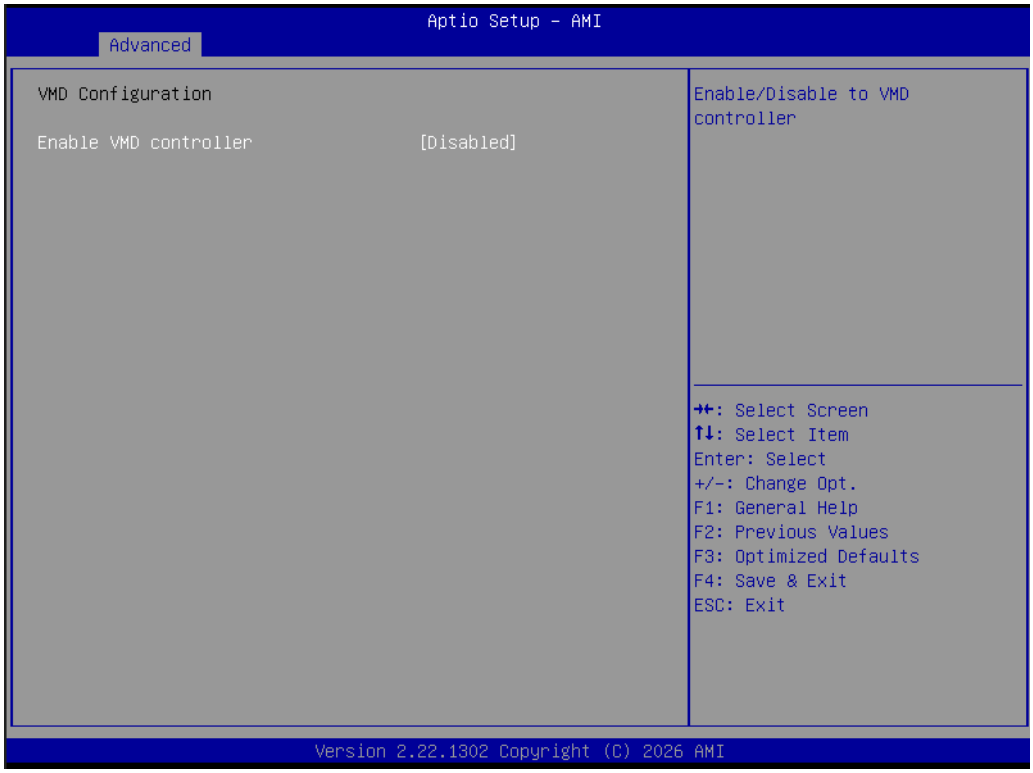
Advanced → System Agent (SA) Configuration → CSV (Computer Vision Sensing) → Camera 2





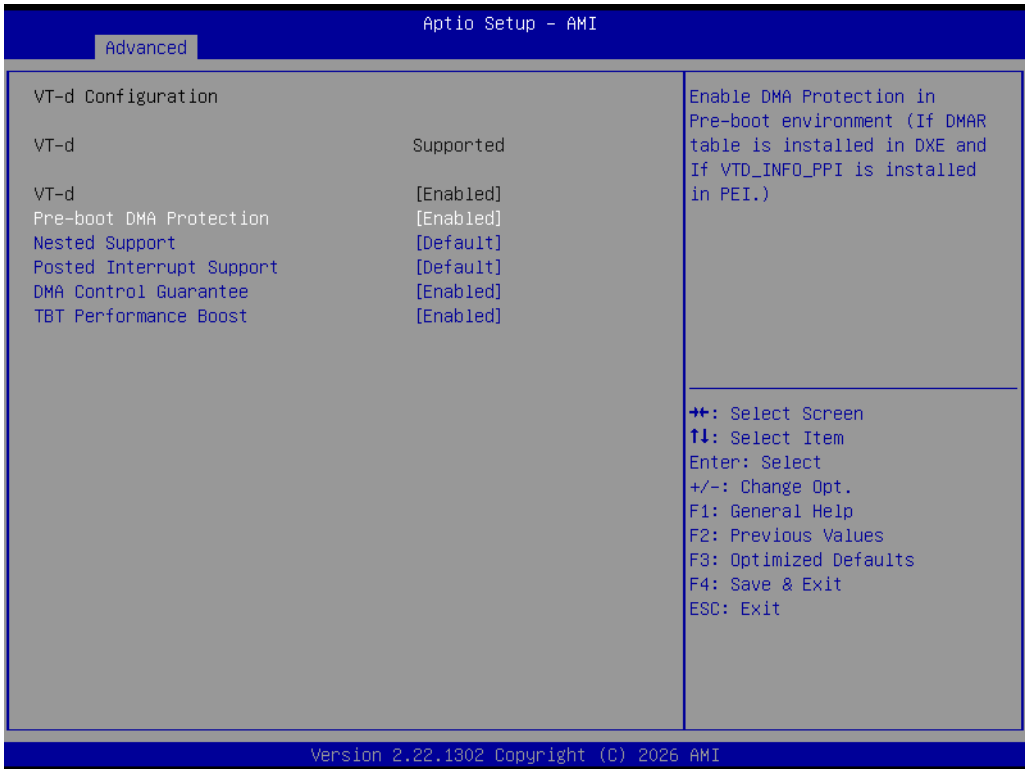
VMD Configuration

Advanced → System Agent (SA) Configuration → VMD Configuration



VT-d Configuration

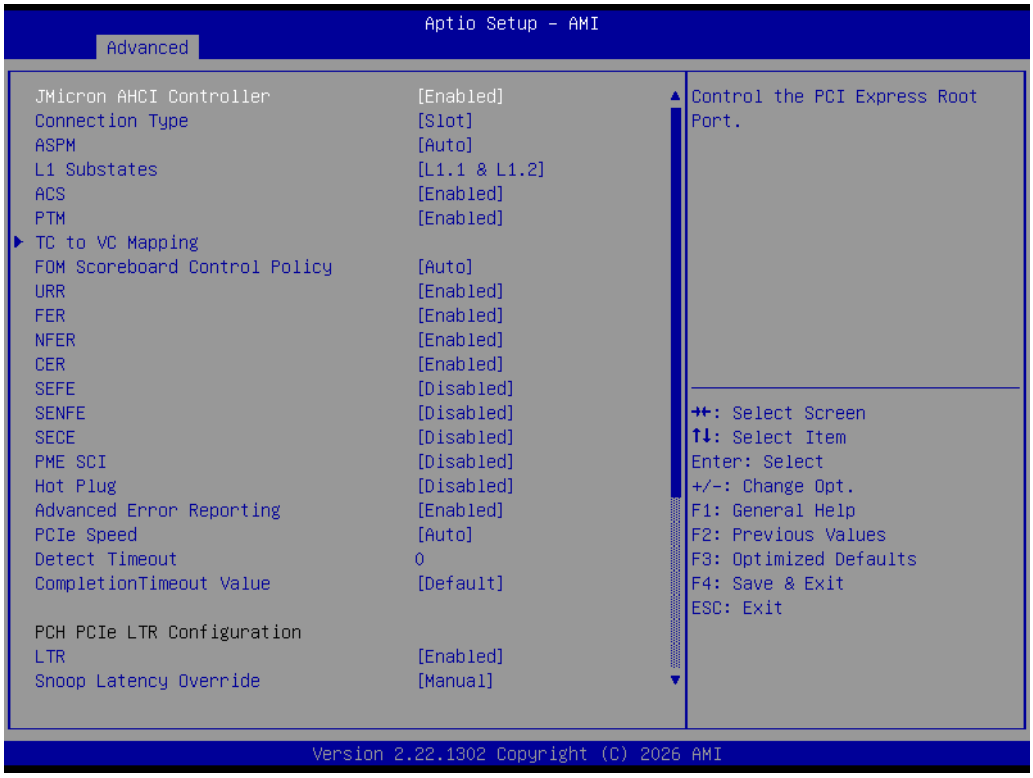
Advanced → System Agent (SA) Configuration → VT-d Configuration



3.2.2.4 PCIE Configuration

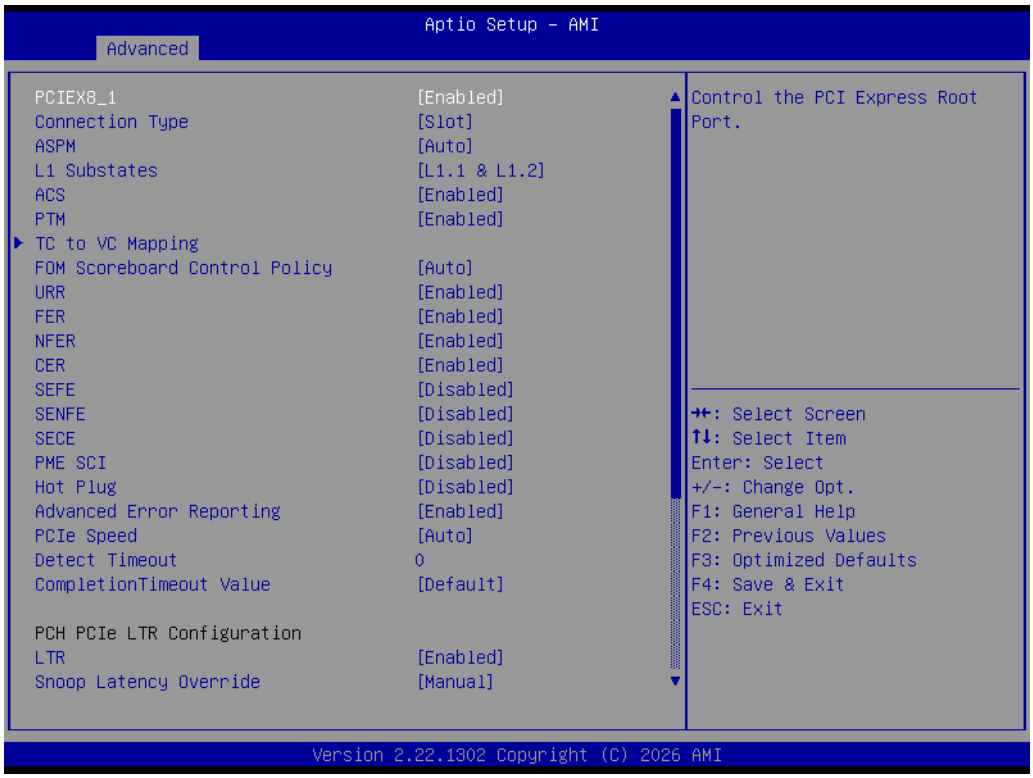
Advanced → PCIE Configuration → JMicron AHCI Controller

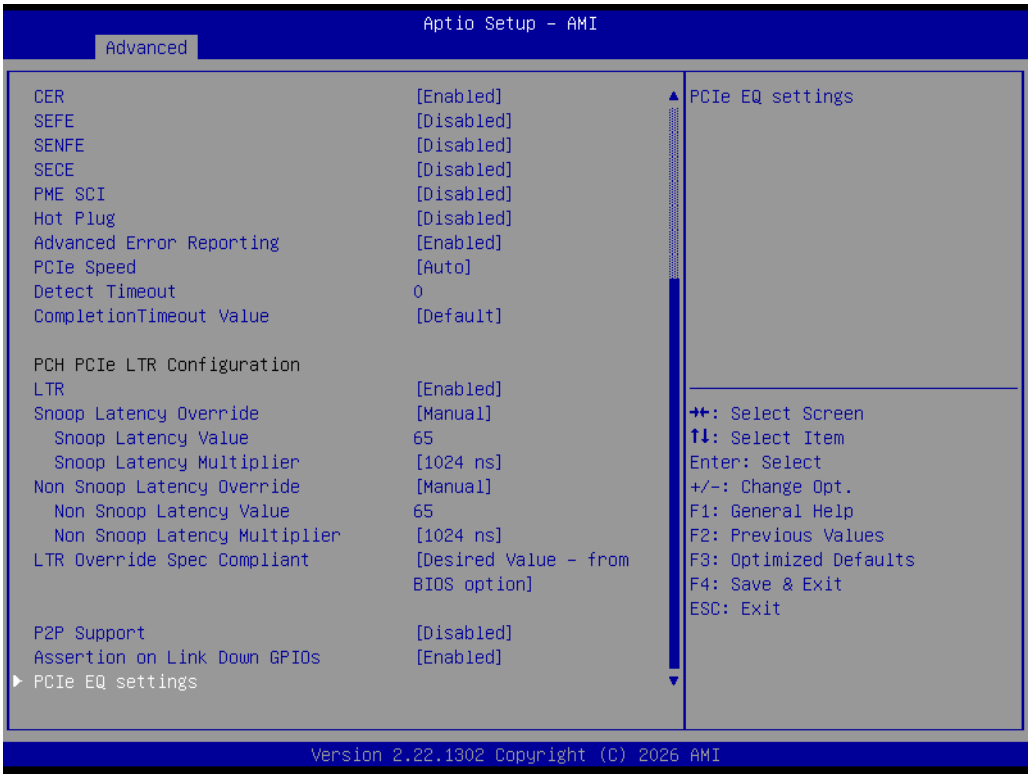


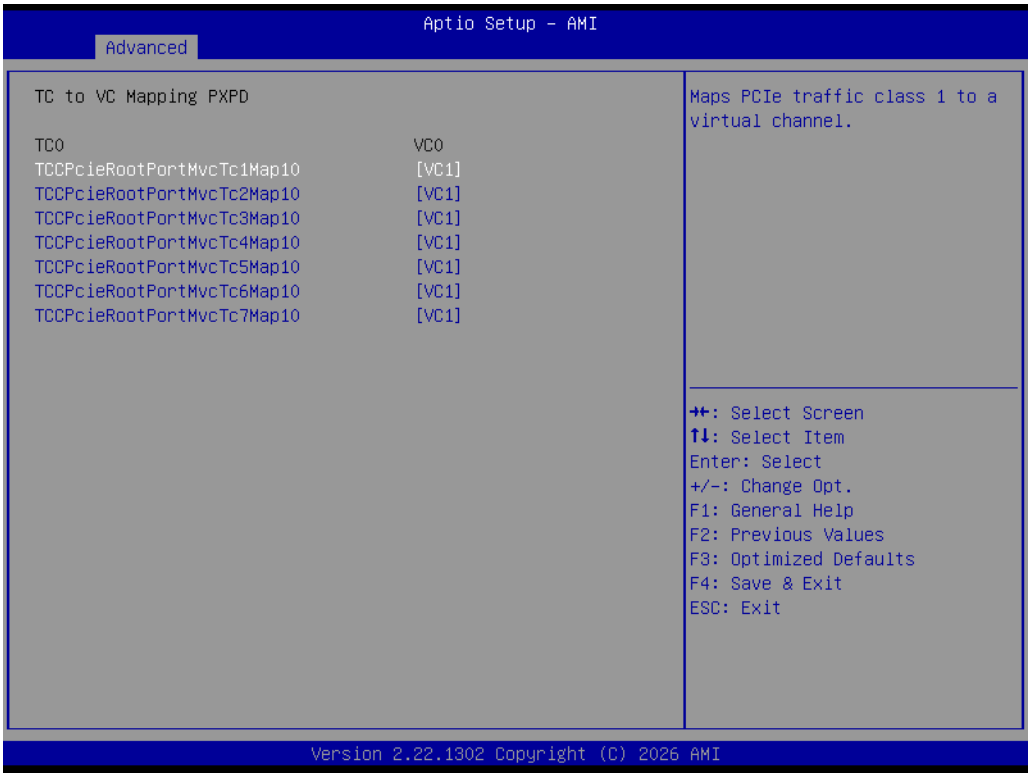


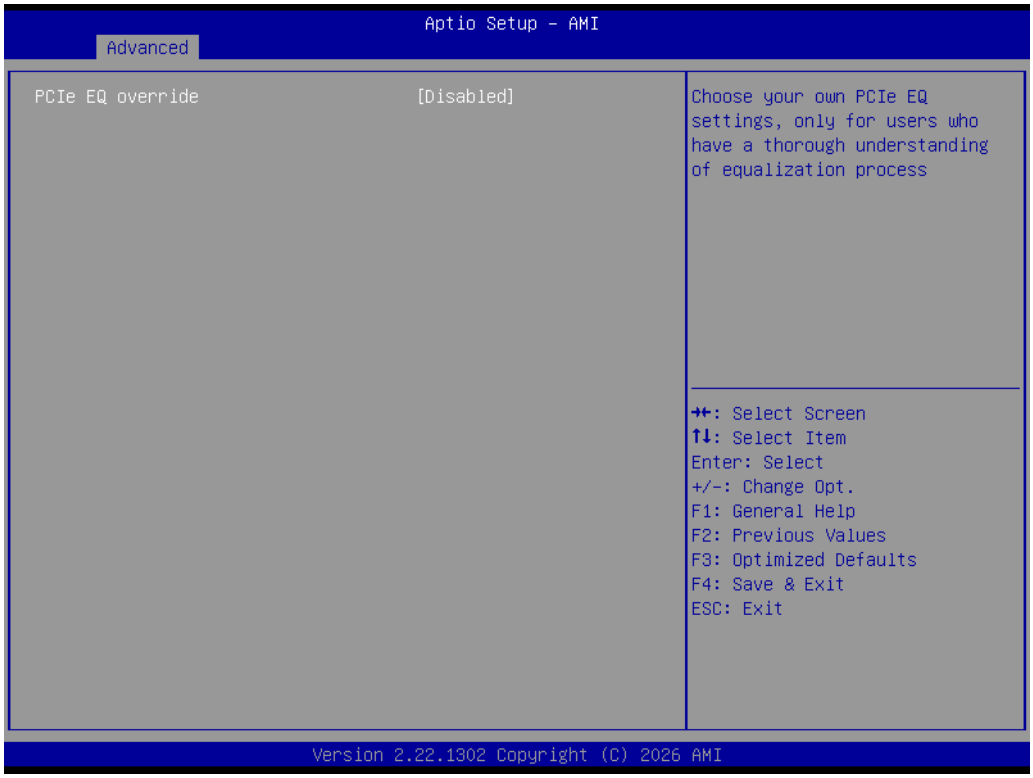
PCIE X8

Advanced → PCIE Configuration → PCIEX8_1




Aptio Setup – AMI
Advanced
CER [Enabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Disabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Detect Timeout 0
CompletionTimeout Value [Default]
PCH PCIe LTR Configuration
LTR [Enabled]
Snoop Latency Override [Manual]
Snoop Latency Value 65
Snoop Latency Multiplier [1024 ns]
Non Snoop Latency Override [Manual]
Non Snoop Latency Value 65
Non Snoop Latency Multiplier [1024 ns]
LTR Override Spec Compliant [Desired Value - from BIOS option]
P2P Support [Disabled]
Assertion on Link Down GPIOs [Enabled]
PCIe EQ settings
PCIe EQ settings
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
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Aptio Setup – AMI
Advanced
TC to VC Mapping PXPD
TC0 VC0
TCCPcieRootPortMvcTc1Map10 [VC1]
TCCPcieRootPortMvcTc2Map10 [VC1]
TCCPcieRootPortMvcTc3Map10 [VC1]
TCCPcieRootPortMvcTc4Map10 [VC1]
TCCPcieRootPortMvcTc5Map10 [VC1]
TCCPcieRootPortMvcTc6Map10 [VC1]
TCCPcieRootPortMvcTc7Map10 [VC1]
Maps PCIe traffic class 1 to a virtual channel.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1302 Copyright (C) 2026 AMI

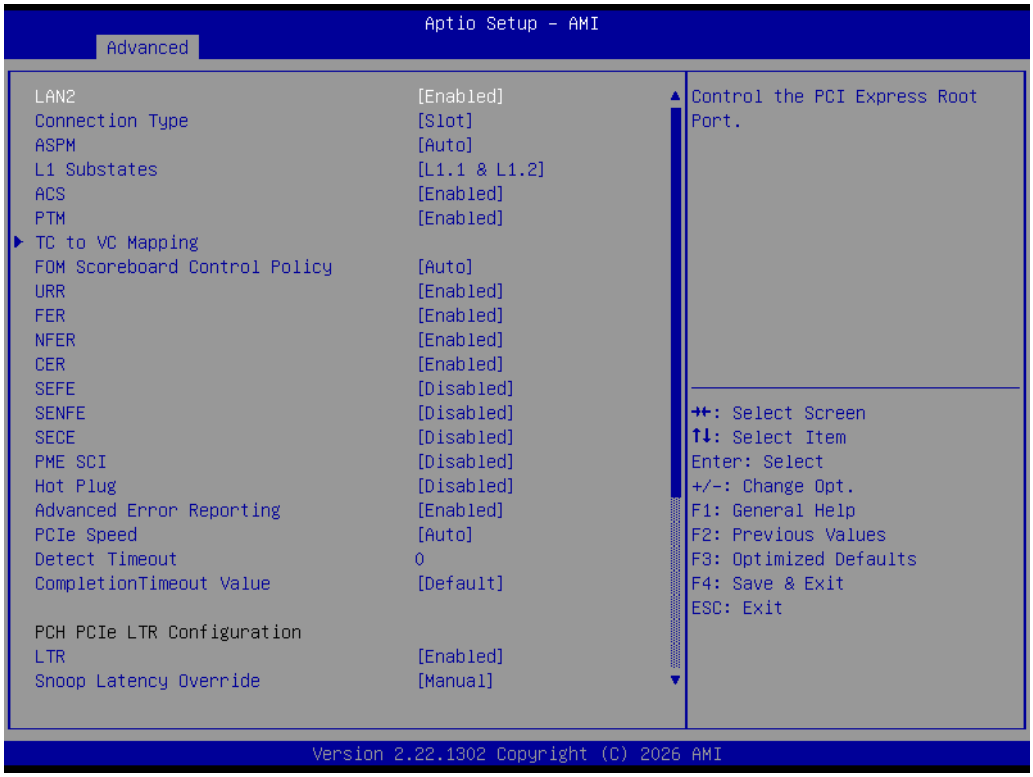


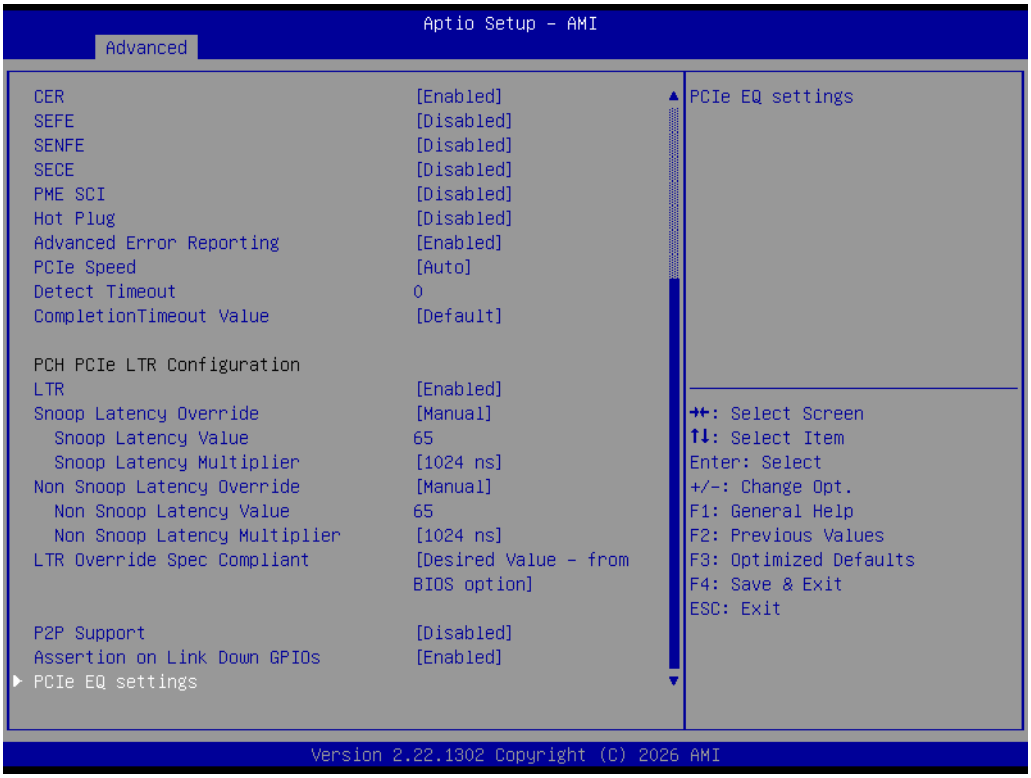
PCH Configuration

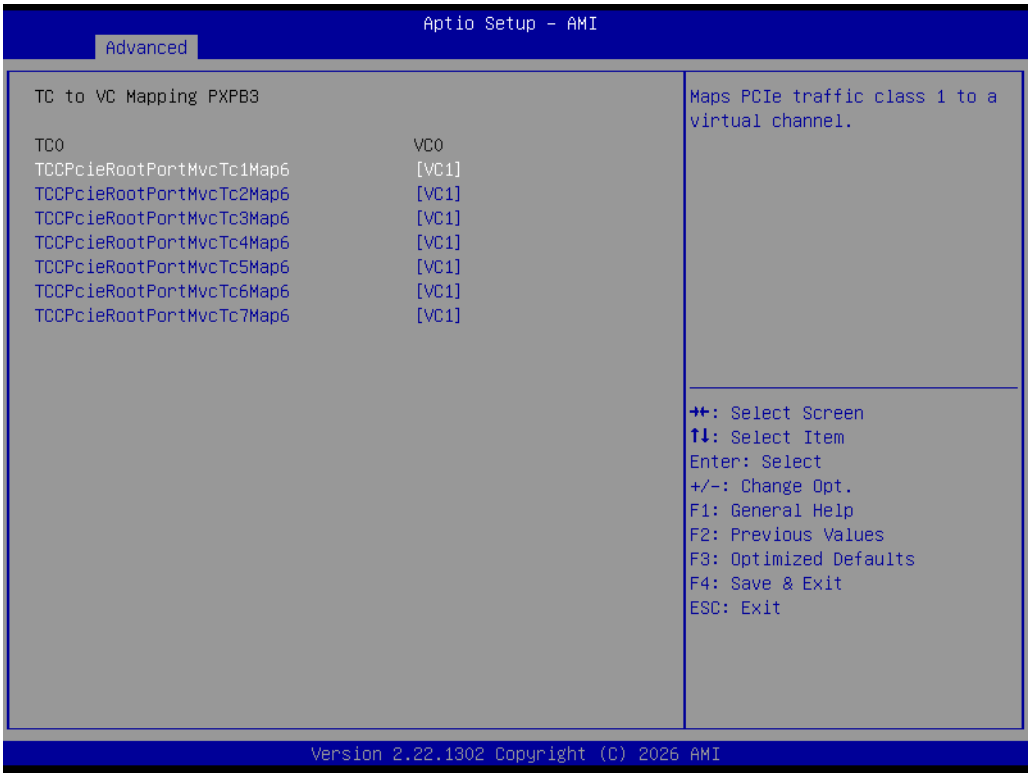
Advanced → PCIE Configuration → PCH Configuration

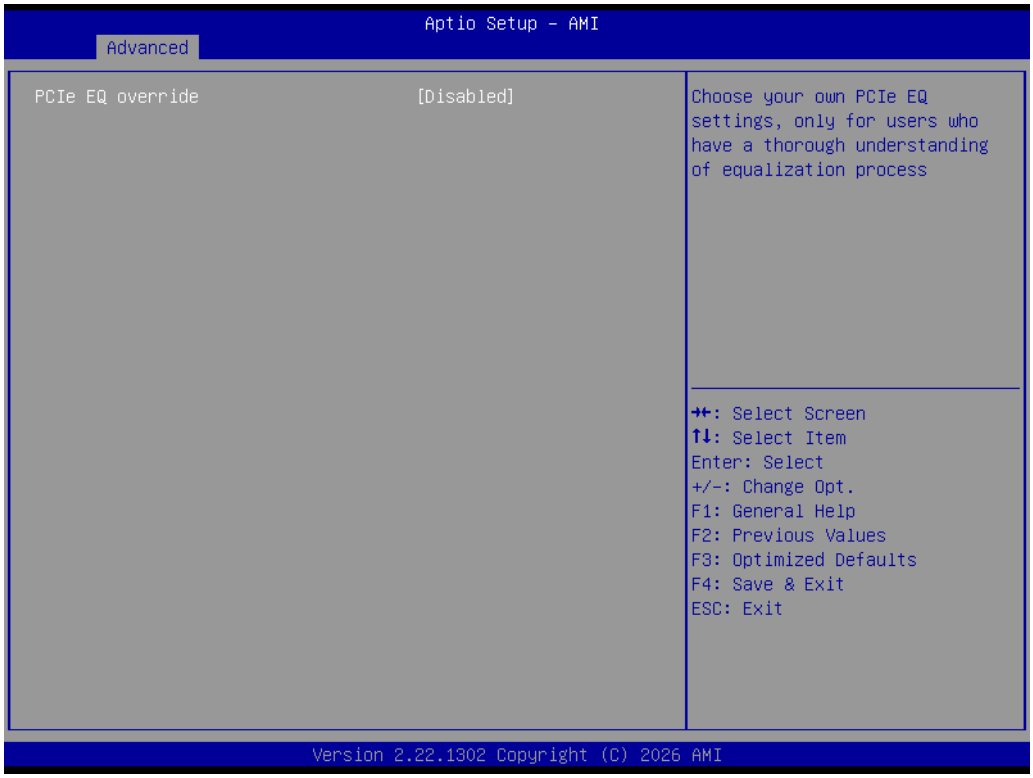
LAN2

Advanced → PCIE Configuration → PCH Configuration → LAN2



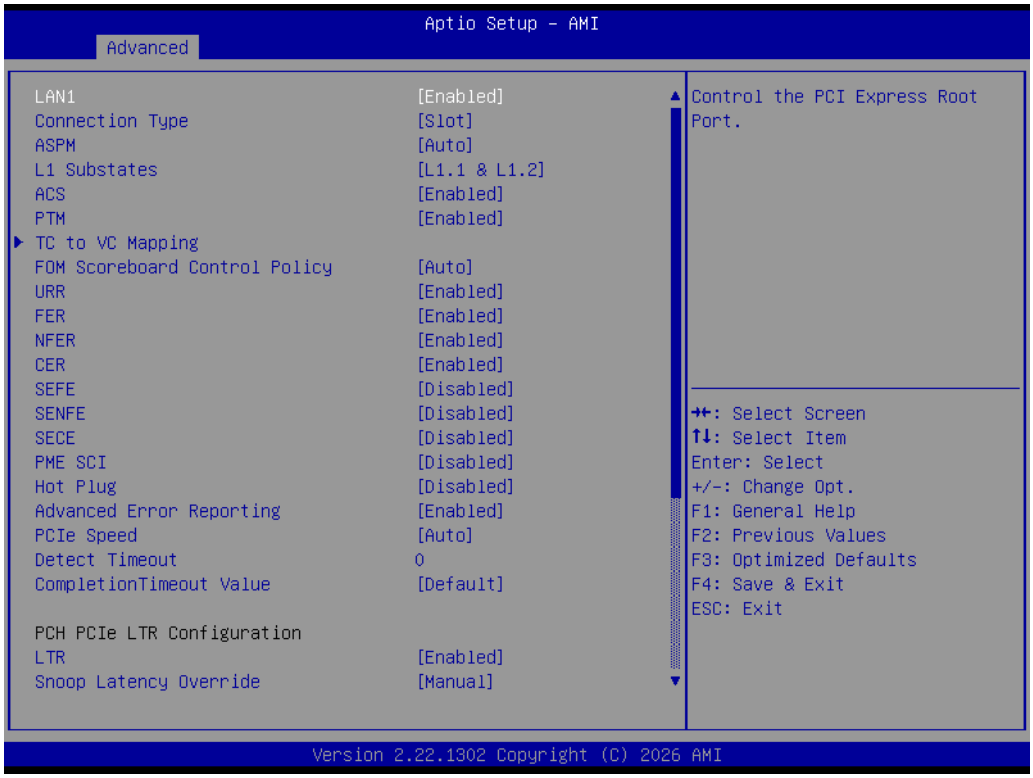

Aptio Setup – AMI
Advanced
CER [Enabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Disabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Detect Timeout 0
CompletionTimeout Value [Default]
PCH PCIe LTR Configuration
LTR [Enabled]
Snoop Latency Override [Manual]
Snoop Latency Value 65
Snoop Latency Multiplier [1024 ns]
Non Snoop Latency Override [Manual]
Non Snoop Latency Value 65
Non Snoop Latency Multiplier [1024 ns]
LTR Override Spec Compliant [Desired Value - from BIOS option]
P2P Support [Disabled]
Assertion on Link Down GPIOs [Enabled]
PCIe EQ settings
PCIe EQ settings
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
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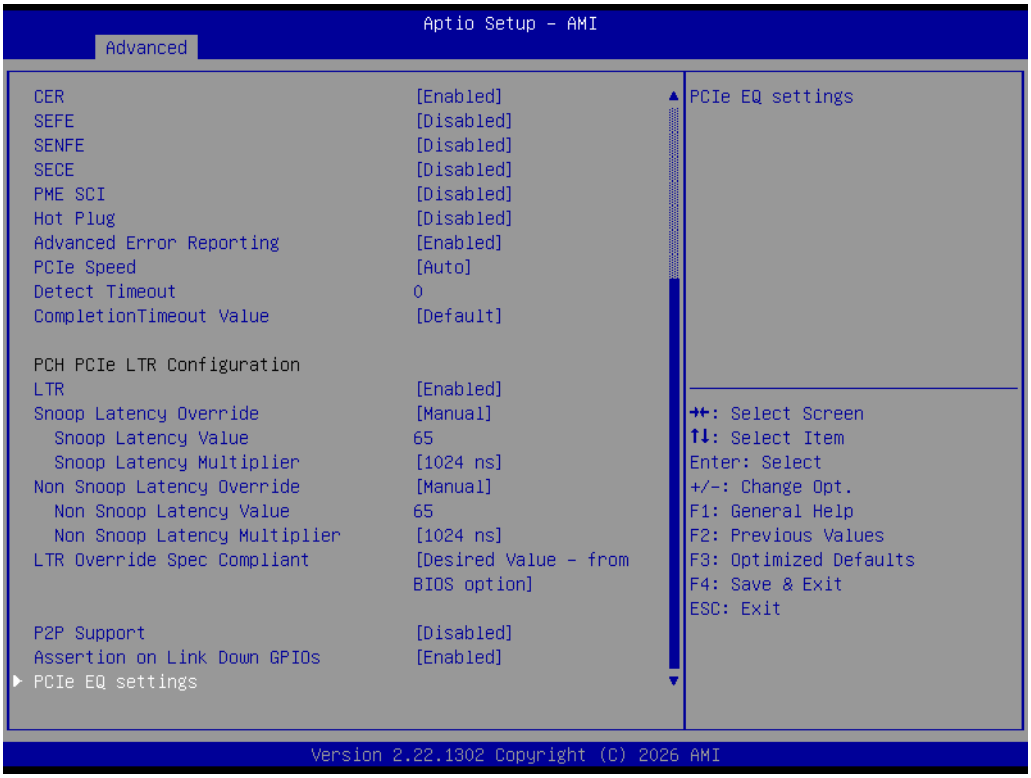

Aptio Setup – AMI
Advanced
TC to VC Mapping PXPB3
TC0 VC0
TCCPcieRootPortMvcTc1Map6 [VC1]
TCCPcieRootPortMvcTc2Map6 [VC1]
TCCPcieRootPortMvcTc3Map6 [VC1]
TCCPcieRootPortMvcTc4Map6 [VC1]
TCCPcieRootPortMvcTc5Map6 [VC1]
TCCPcieRootPortMvcTc6Map6 [VC1]
TCCPcieRootPortMvcTc7Map6 [VC1]
Maps PCIe traffic class 1 to a virtual channel.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1302 Copyright (C) 2026 AMI

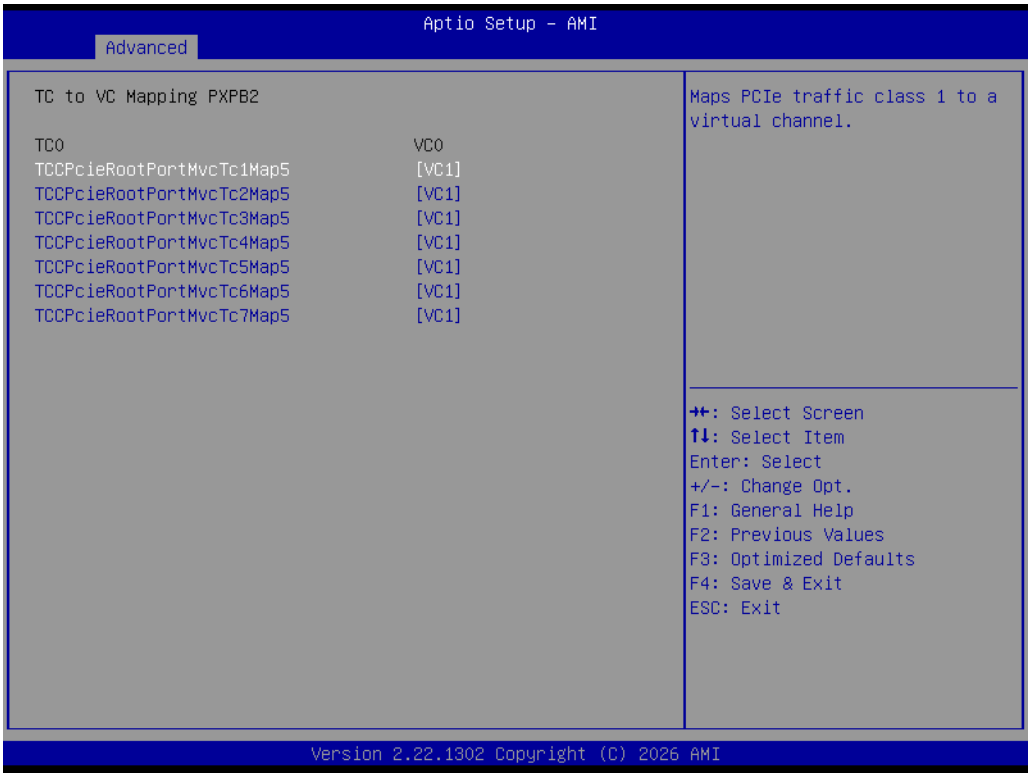


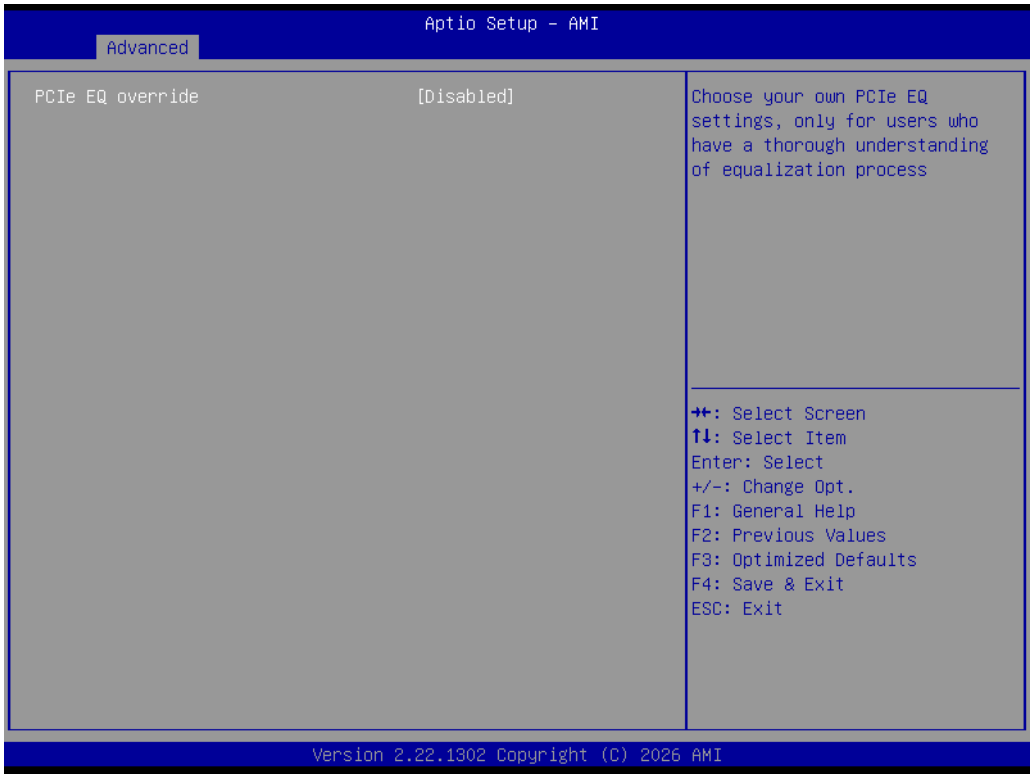
LAN1

Advanced → PCIE Configuration → PCH Configuration → LAN1



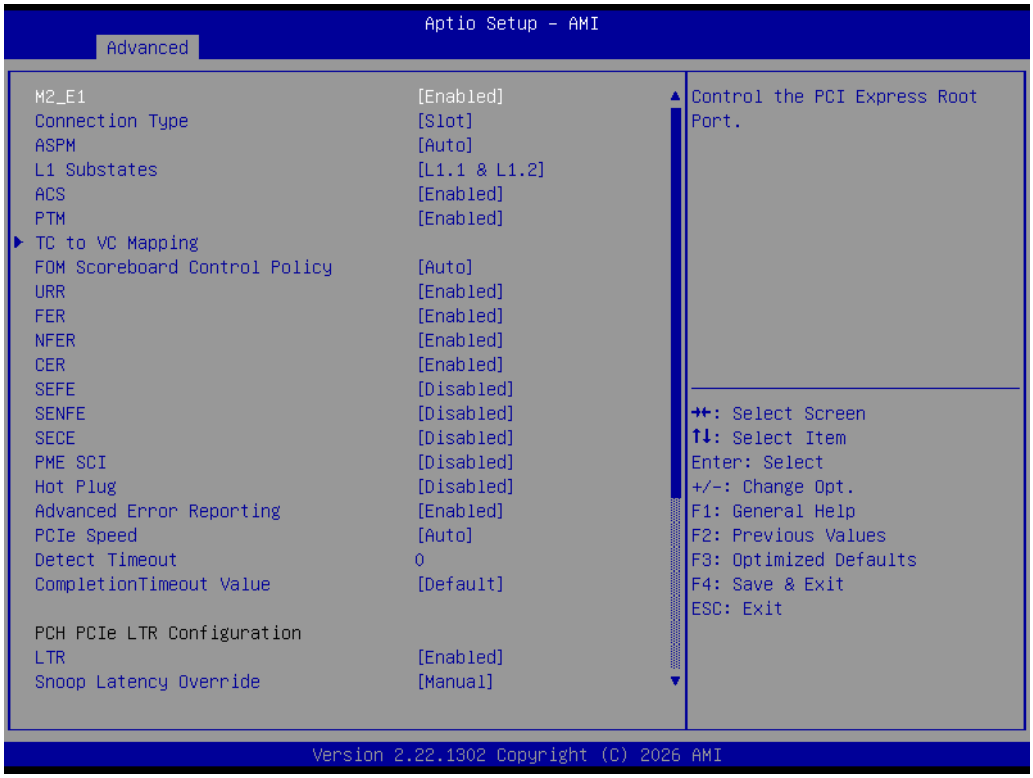

Aptio Setup – AMI
Advanced
CER [Enabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Disabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Detect Timeout 0
CompletionTimeout Value [Default]
PCH PCIe LTR Configuration
LTR [Enabled]
Snoop Latency Override [Manual]
Snoop Latency Value 65
Snoop Latency Multiplier [1024 ns]
Non Snoop Latency Override [Manual]
Non Snoop Latency Value 65
Non Snoop Latency Multiplier [1024 ns]
LTR Override Spec Compliant [Desired Value - from BIOS option]
P2P Support [Disabled]
Assertion on Link Down GPIOs [Enabled]
PCIe EQ settings
PCIe EQ settings
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1302 Copyright (C) 2026 AMI

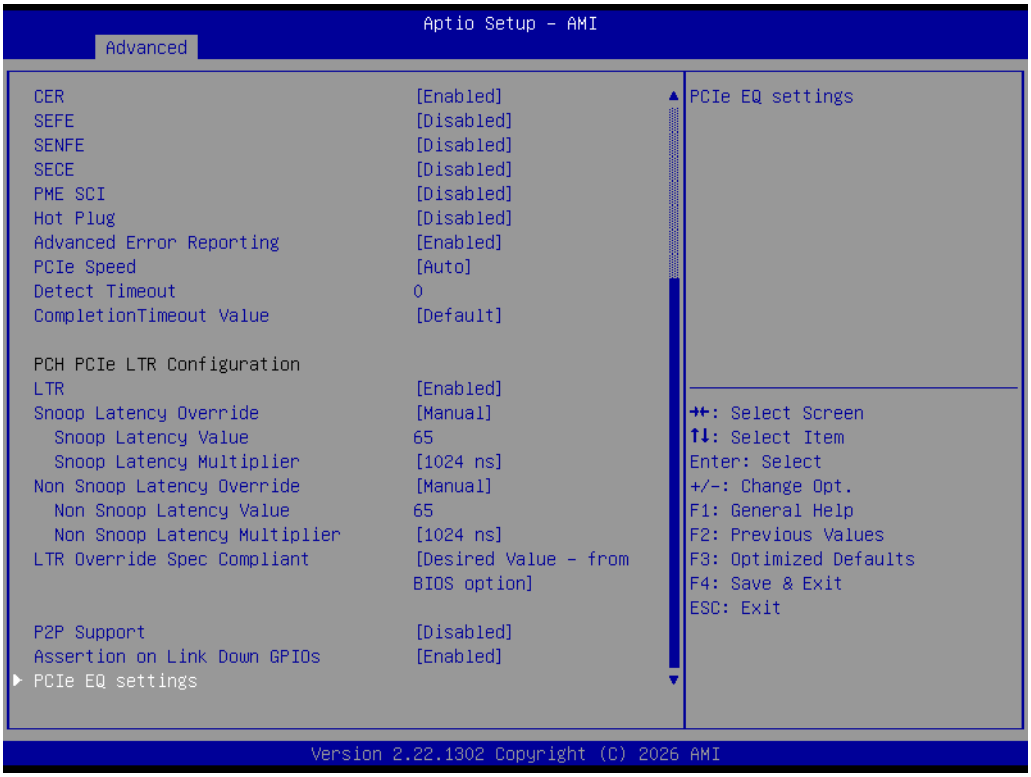

Aptio Setup – AMI
Advanced
TC to VC Mapping PXPB2
TC0 VC0
TCCPcieRootPortMvcTc1Map5 [VC1]
TCCPcieRootPortMvcTc2Map5 [VC1]
TCCPcieRootPortMvcTc3Map5 [VC1]
TCCPcieRootPortMvcTc4Map5 [VC1]
TCCPcieRootPortMvcTc5Map5 [VC1]
TCCPcieRootPortMvcTc6Map5 [VC1]
TCCPcieRootPortMvcTc7Map5 [VC1]
Maps PCIe traffic class 1 to a virtual channel.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1302 Copyright (C) 2026 AMI

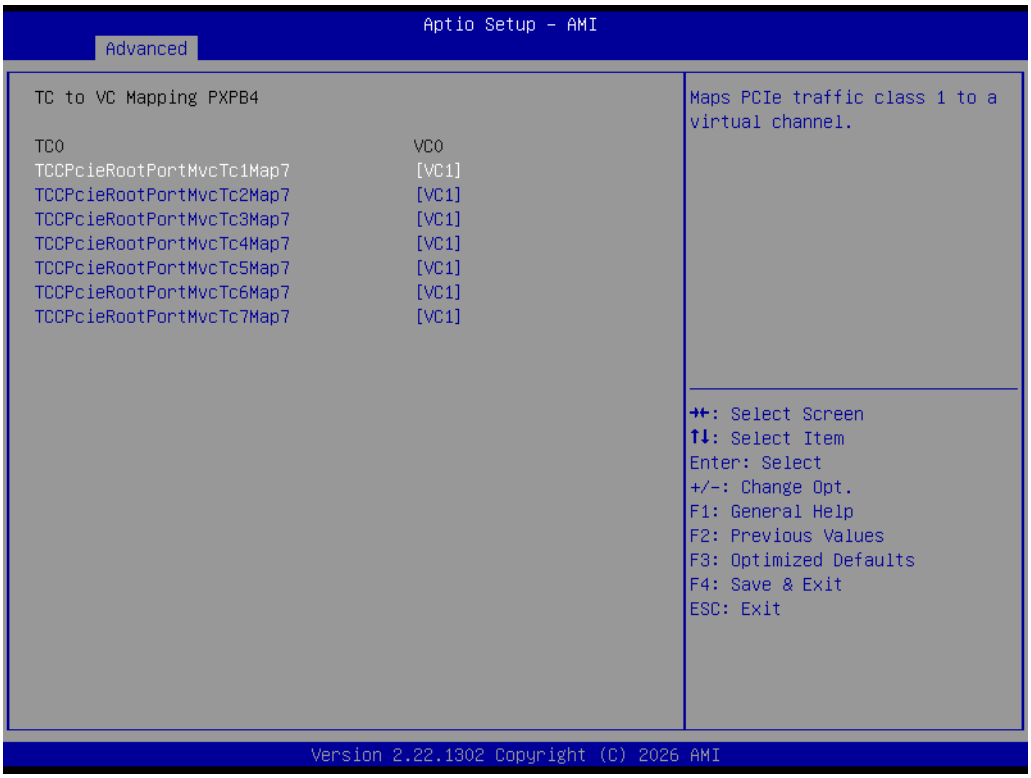


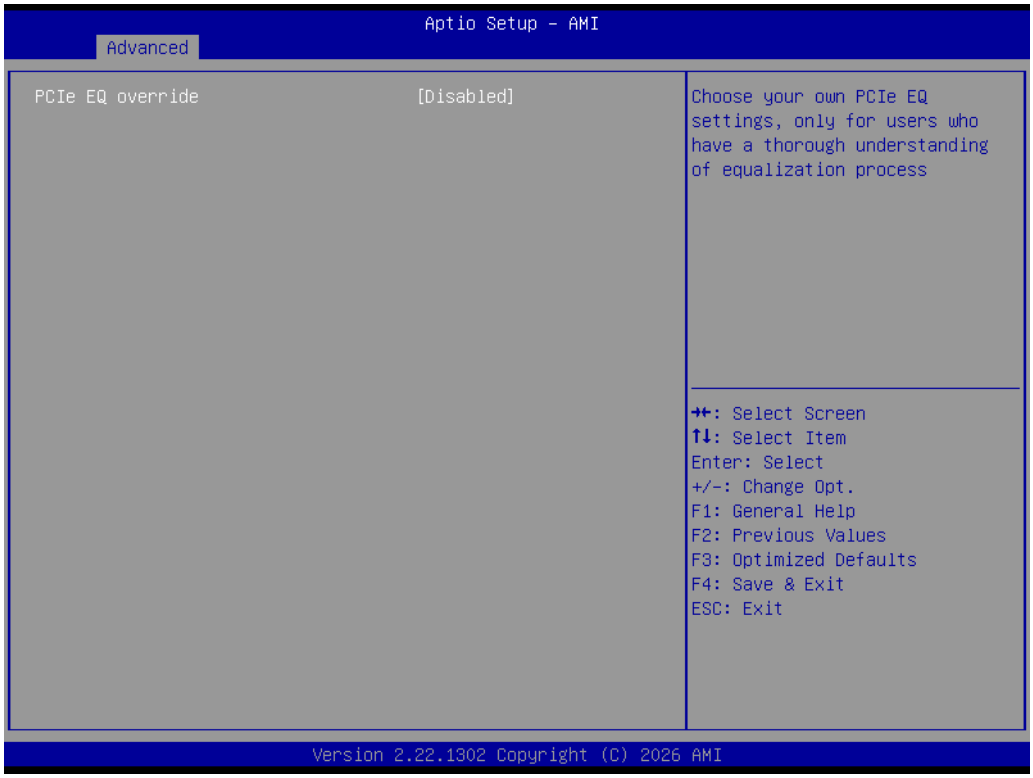
M.2 E-Key

Advanced → PCIE Configuration → PCH Configuration → M.2_E1



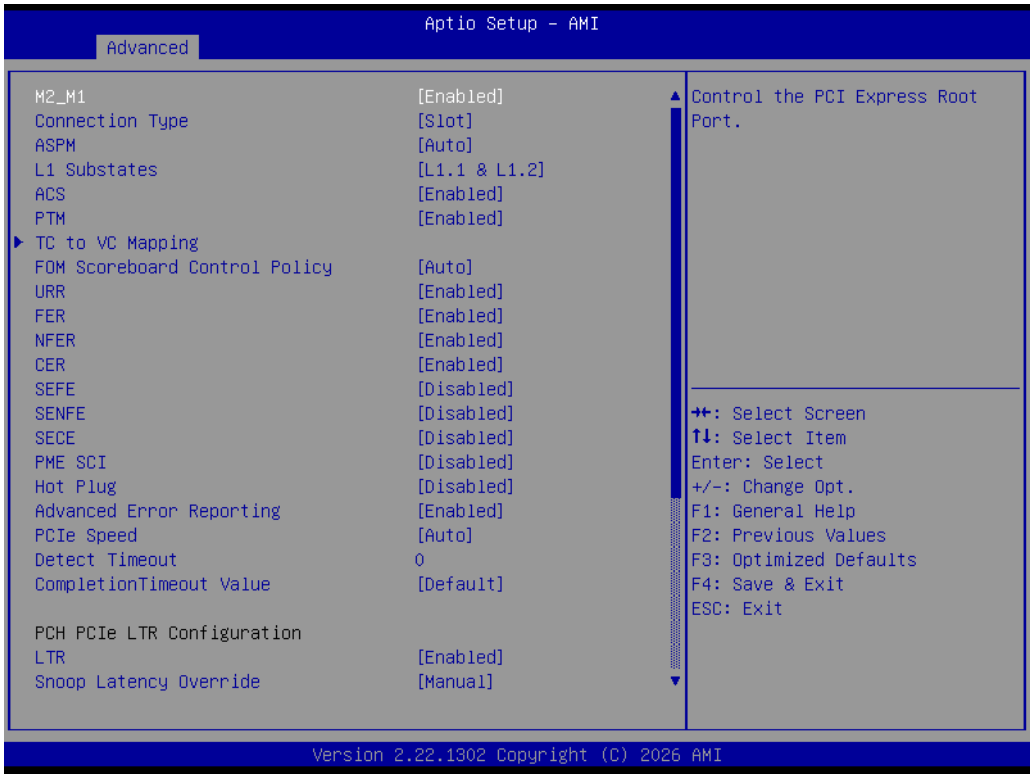

Aptio Setup – AMI
Advanced
CER [Enabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Disabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Detect Timeout 0
CompletionTimeout Value [Default]
PCH PCIe LTR Configuration
LTR [Enabled]
Snoop Latency Override [Manual]
Snoop Latency Value 65
Snoop Latency Multiplier [1024 ns]
Non Snoop Latency Override [Manual]
Non Snoop Latency Value 65
Non Snoop Latency Multiplier [1024 ns]
LTR Override Spec Compliant [Desired Value - from BIOS option]
P2P Support [Disabled]
Assertion on Link Down GPIOs [Enabled]
PCIe EQ settings
PCIe EQ settings
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1302 Copyright (C) 2026 AMI

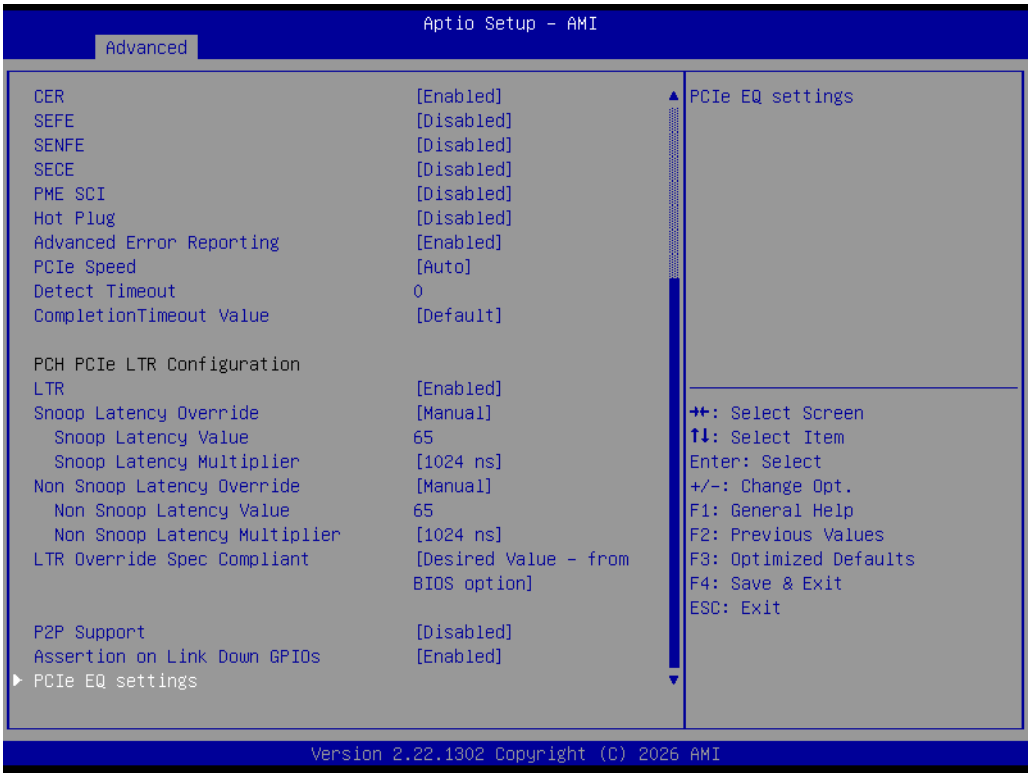

Aptio Setup – AMI
Advanced
TC to VC Mapping PXPB4
TC0 VC0
TCCPcieRootPortMvcTc1Map7 [VC1]
TCCPcieRootPortMvcTc2Map7 [VC1]
TCCPcieRootPortMvcTc3Map7 [VC1]
TCCPcieRootPortMvcTc4Map7 [VC1]
TCCPcieRootPortMvcTc5Map7 [VC1]
TCCPcieRootPortMvcTc6Map7 [VC1]
TCCPcieRootPortMvcTc7Map7 [VC1]
Maps PCIe traffic class 1 to a virtual channel.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1302 Copyright (C) 2026 AMI

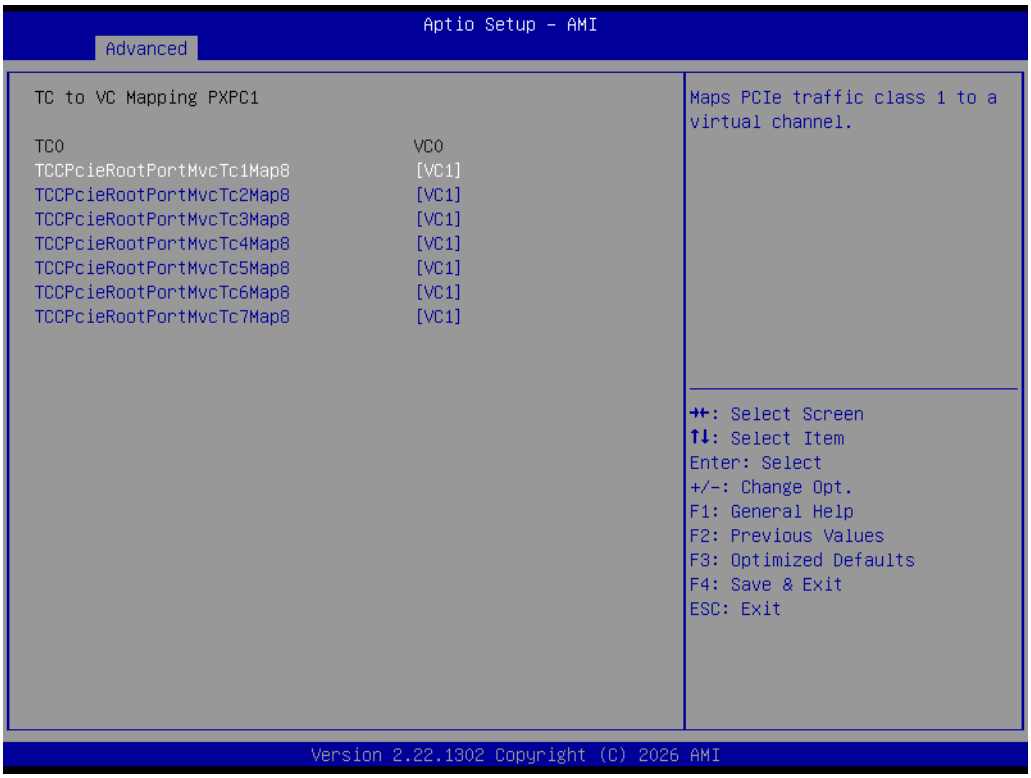


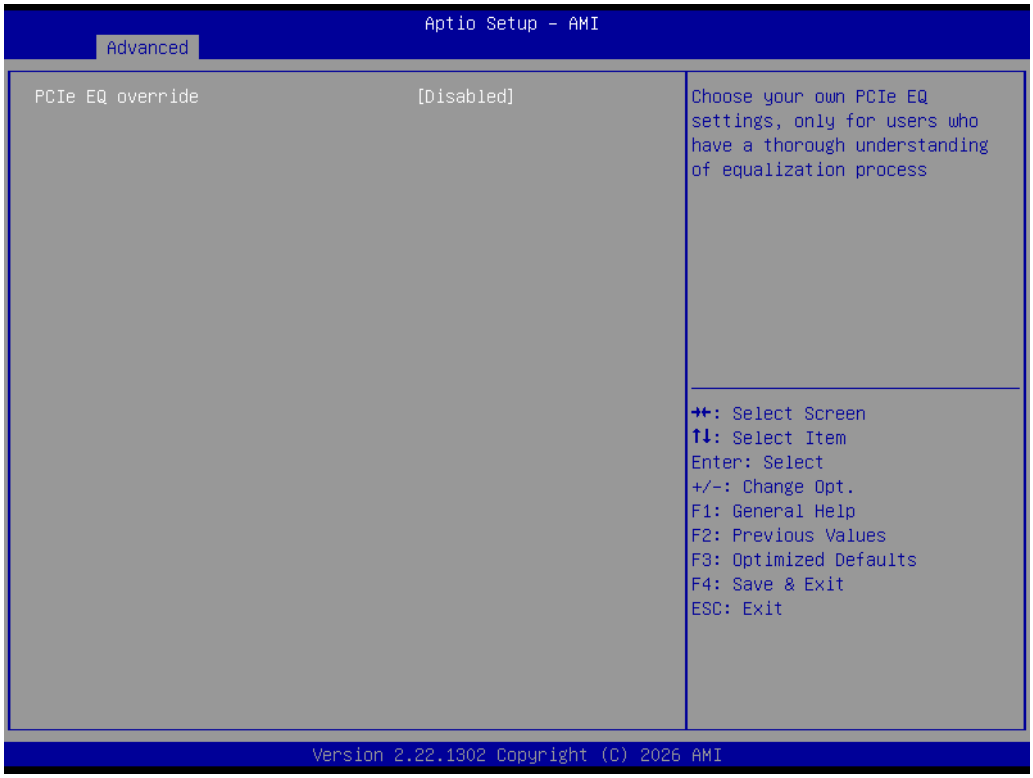
M.2 M-KEY

Advanced →PCIE Configuration → PCH Configuration → M2_M1



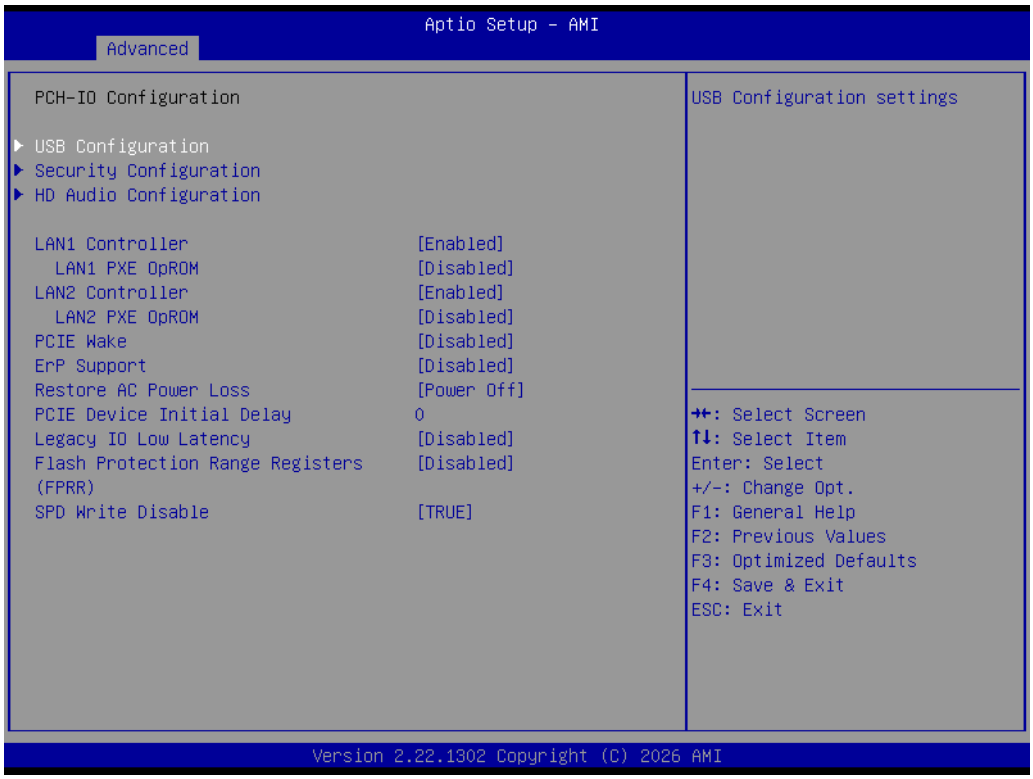

Aptio Setup – AMI
Advanced
CER [Enabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Disabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Detect Timeout 0
CompletionTimeout Value [Default]
PCH PCIe LTR Configuration
LTR [Enabled]
Snoop Latency Override [Manual]
Snoop Latency Value 65
Snoop Latency Multiplier [1024 ns]
Non Snoop Latency Override [Manual]
Non Snoop Latency Value 65
Non Snoop Latency Multiplier [1024 ns]
LTR Override Spec Compliant [Desired Value - from BIOS option]
P2P Support [Disabled]
Assertion on Link Down GPIOs [Enabled]
PCIe EQ settings
PCIe EQ settings
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1302 Copyright (C) 2026 AMI

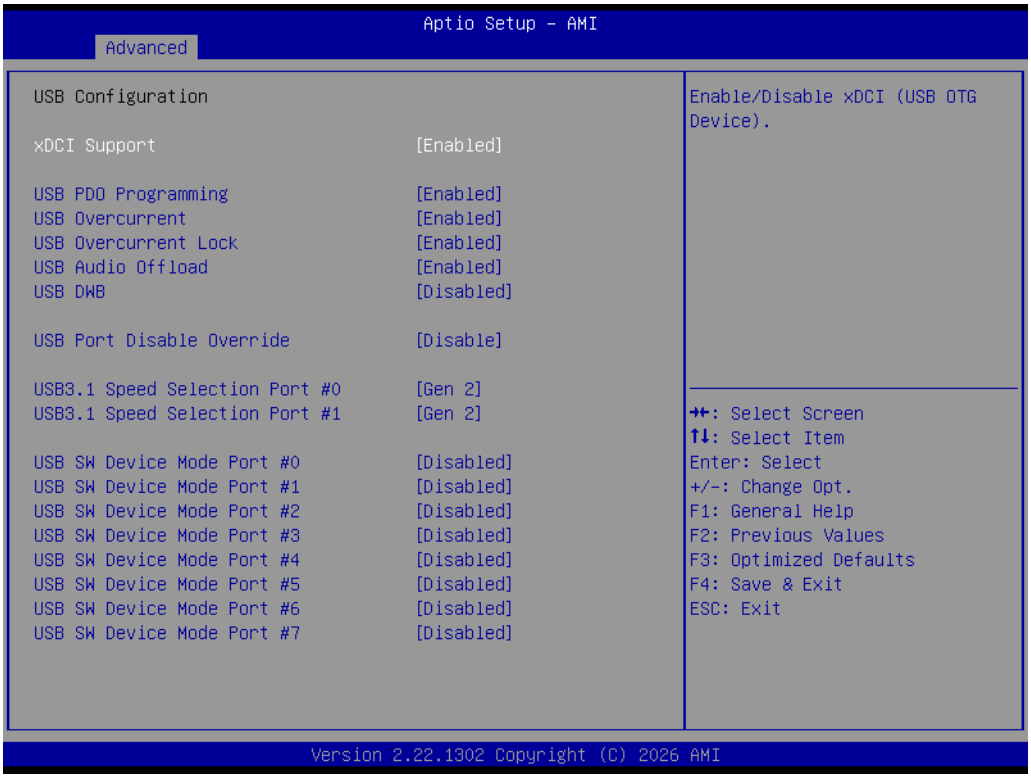

Aptio Setup – AMI
Advanced
TC to VC Mapping PXPC1
TC0 VC0
TCCPcieRootPortMvcTc1Map8 [VC1]
TCCPcieRootPortMvcTc2Map8 [VC1]
TCCPcieRootPortMvcTc3Map8 [VC1]
TCCPcieRootPortMvcTc4Map8 [VC1]
TCCPcieRootPortMvcTc5Map8 [VC1]
TCCPcieRootPortMvcTc6Map8 [VC1]
TCCPcieRootPortMvcTc7Map8 [VC1]
Maps PCIe traffic class 1 to a virtual channel.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.22.1302 Copyright (C) 2026 AMI



3.2.2.5 PCH-IO Configuration

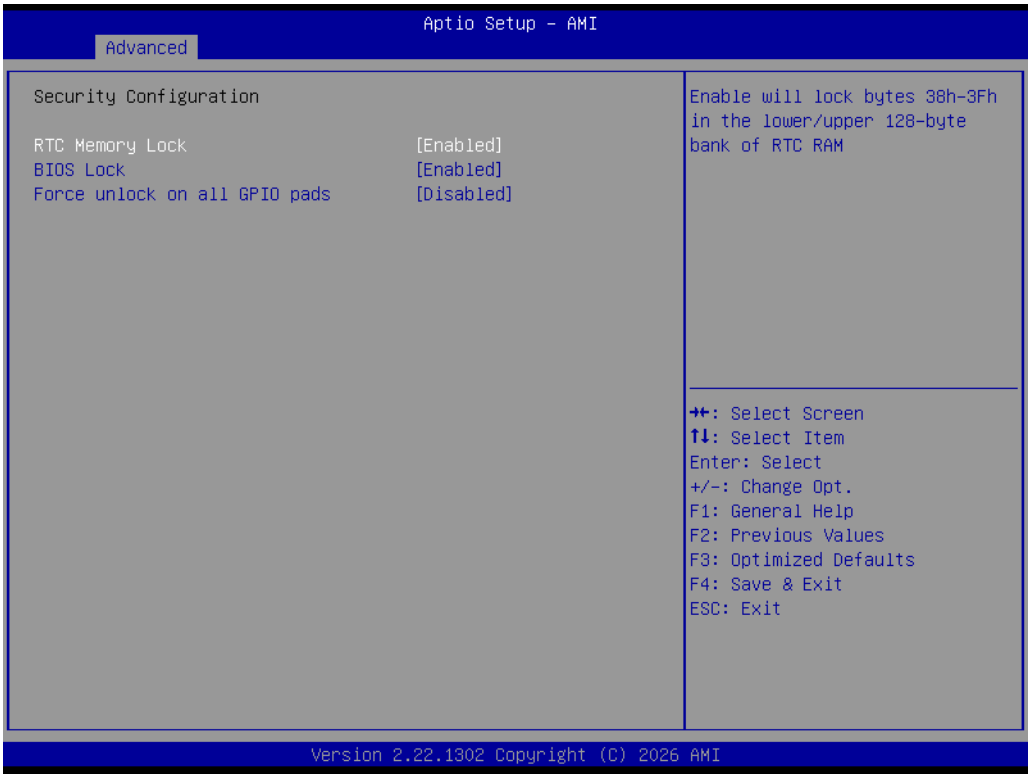
Advanced → PCH-IO Configuration





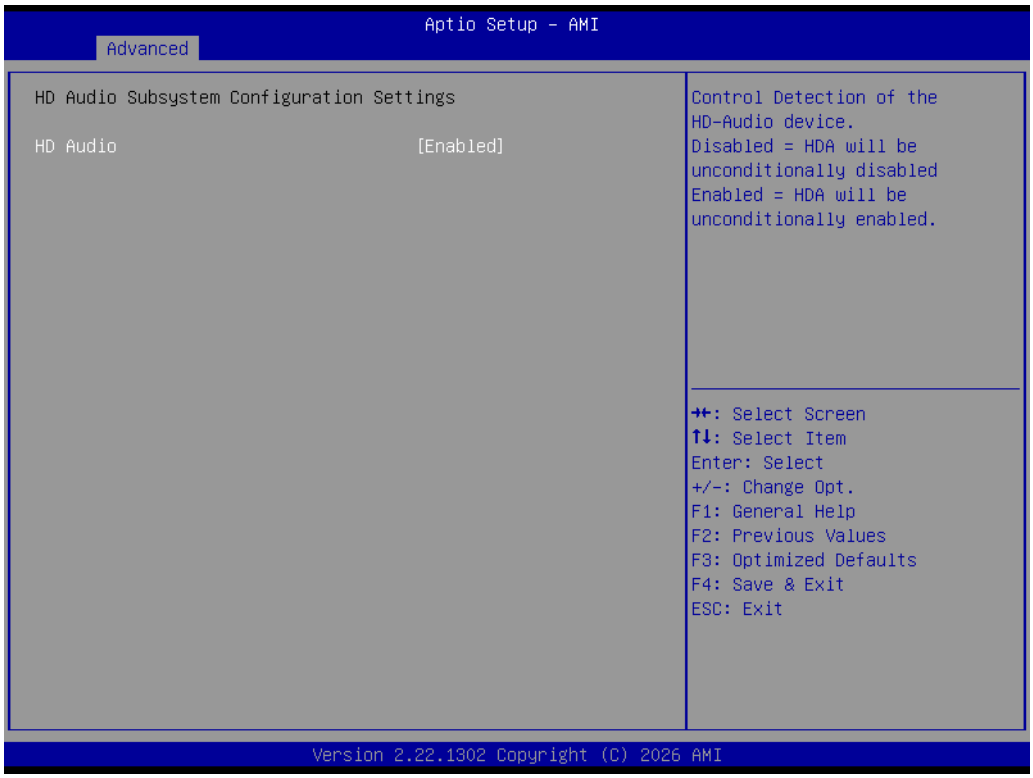
Security Configuration

Advanced → PCH-IO Configuration → Security Configuration



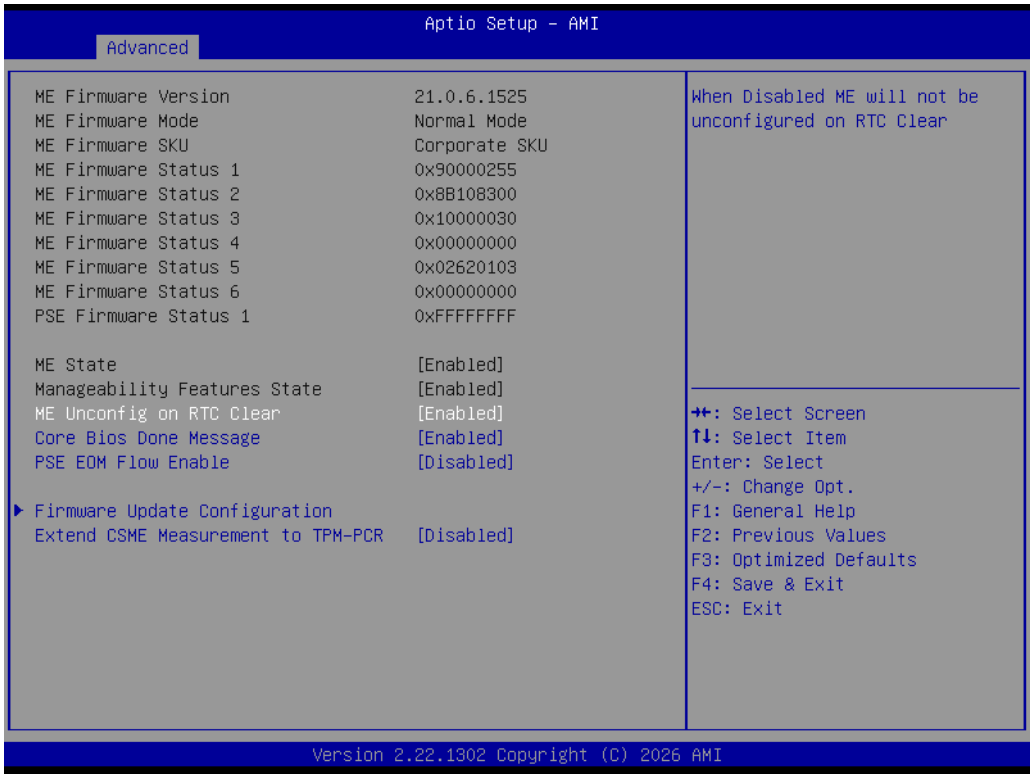
HD Audio Subsystem Configuration Settings

Advanced → PCH-IO Configuration → HD Audio Subsystem Configuration Settings



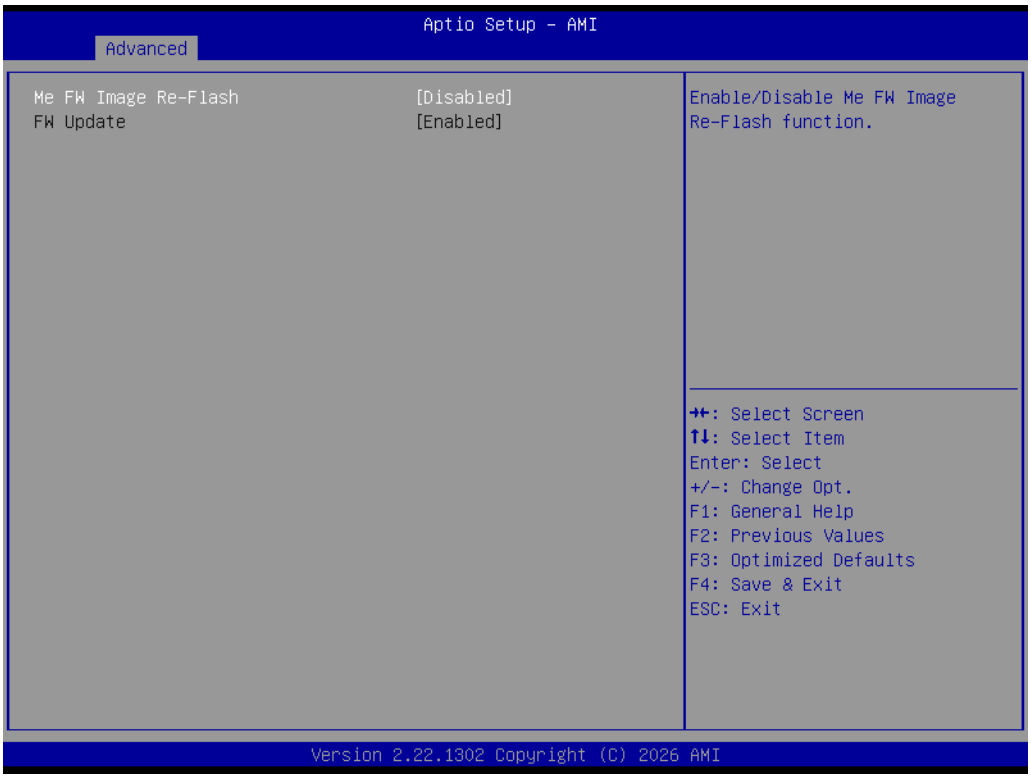
3.2.2.6 PCH-FW Configuration

Advanced → PCH-FW Configuration



Firmware Update Configuration

Advanced → PCH-FW Configuration → Firmware Update Configuration



3.2.2.7 DMI Configuration

Advanced DMI Configuration

Advanced → DMI Configuration → Advanced DMI Configuration

Gen3 Root Port Preset value for each Lane

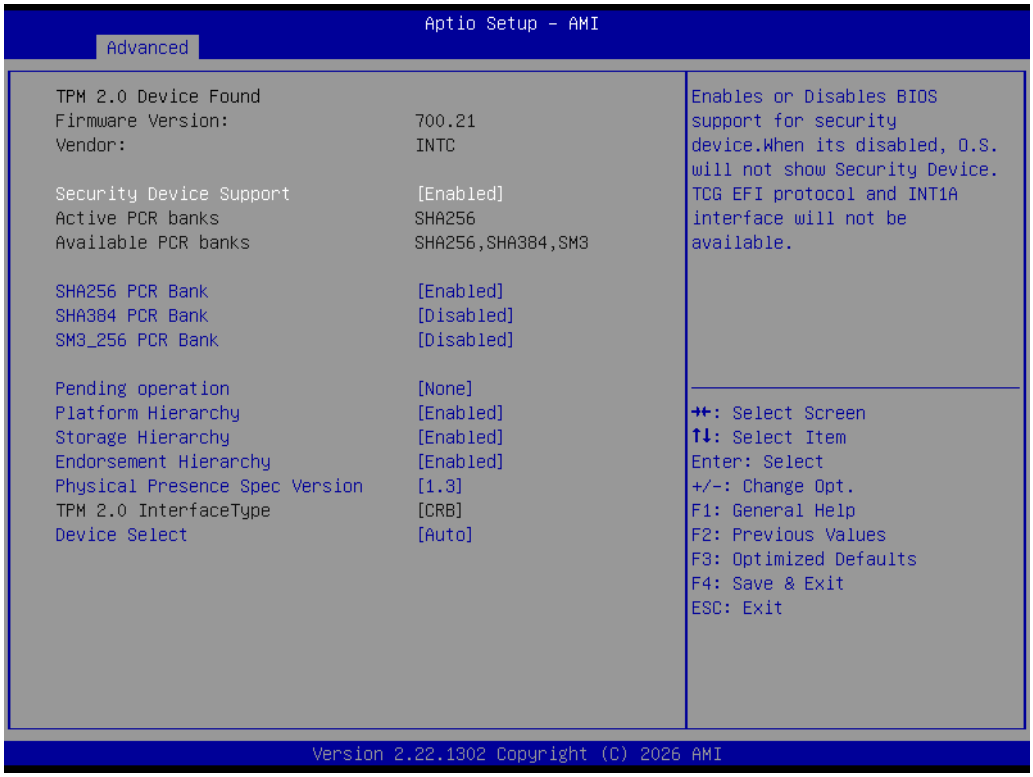
Advanced → DMI Configuration → Advanced DMI Configuration → Gen3 Root Port Preset value for each Lane

Gen3 Endpoint Preset value for each Lane

Advanced → DMI Configuration → Advanced DMI Configuration → Gen3 Endpoint

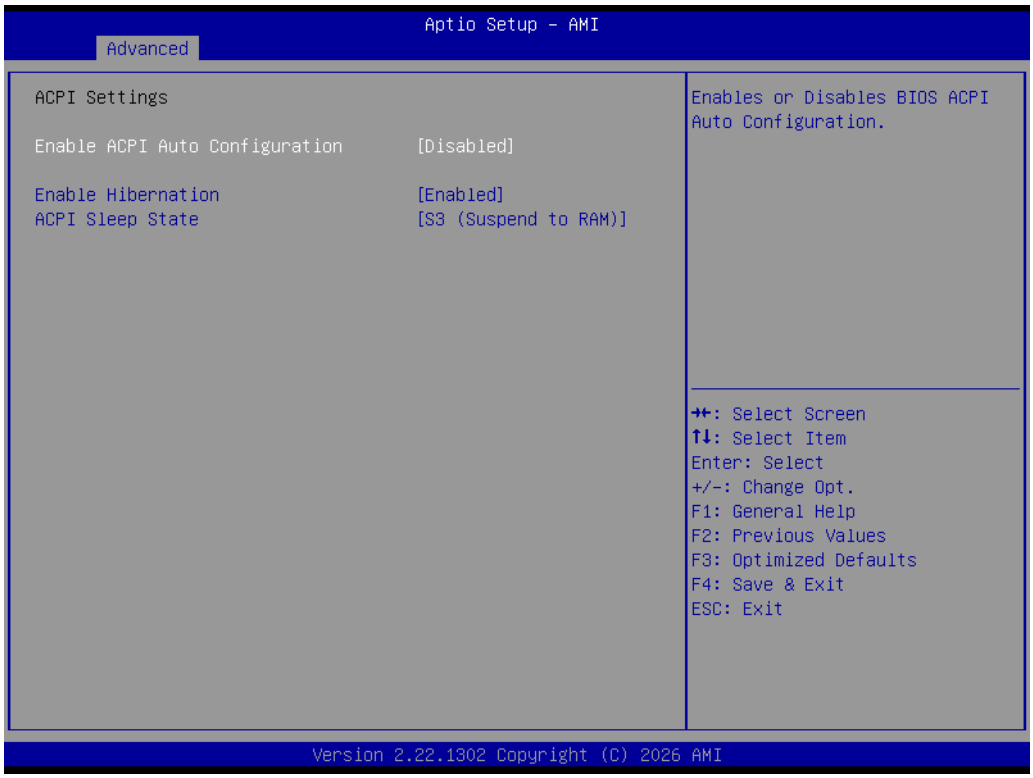
3.2.2.8 Trusted Computing

Advanced → Trusted Computing



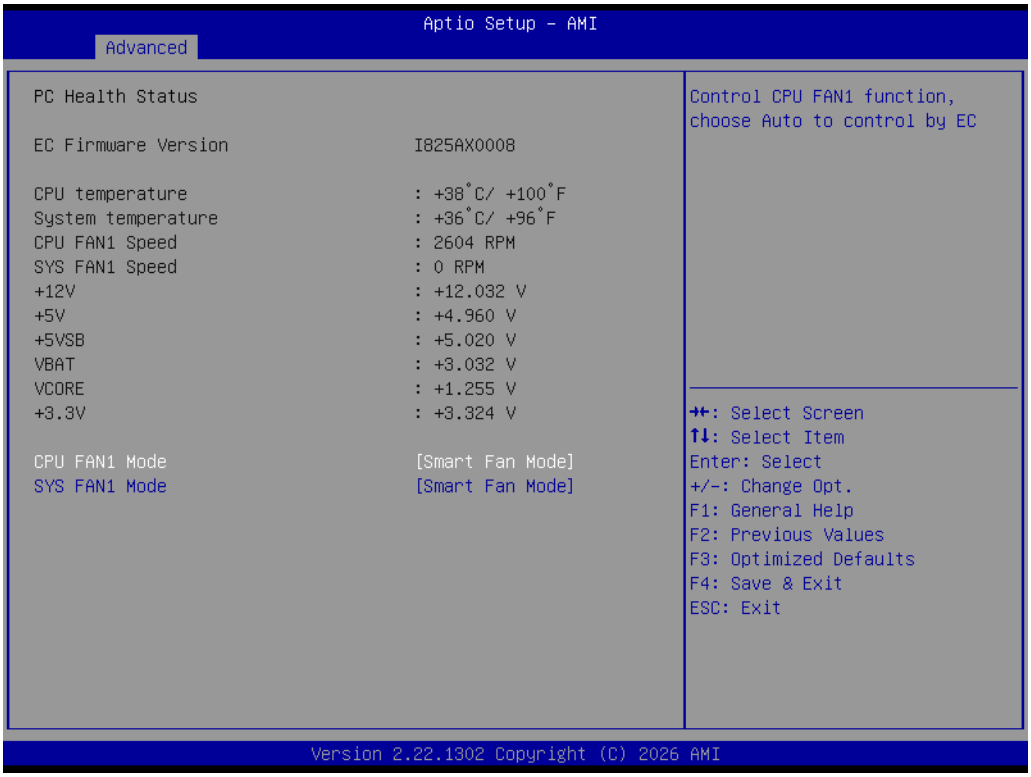
3.2.2.9 ACPI Settings

Advanced → ACPI Settings



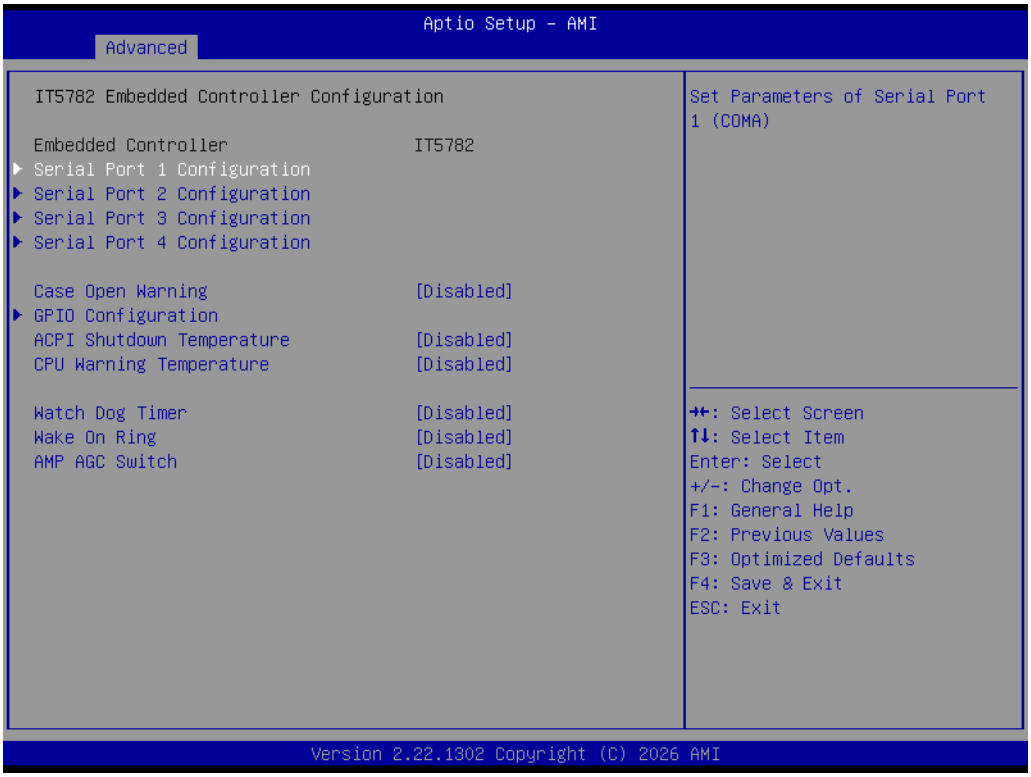
3.2.2.10 IT5782 HW Monitor

Advanced → IT5782 HW Monitor



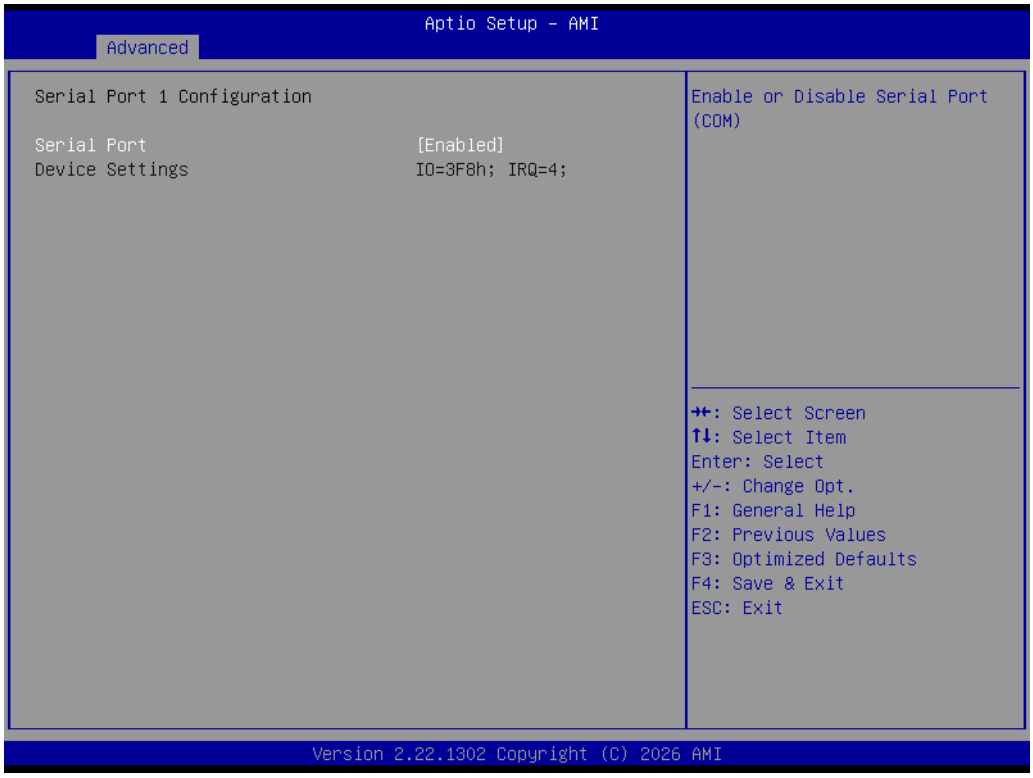
3.2.2.11 IT5782 Embedded Controller Configuration

Advanced → IT5782 Embedded Controller Configuration



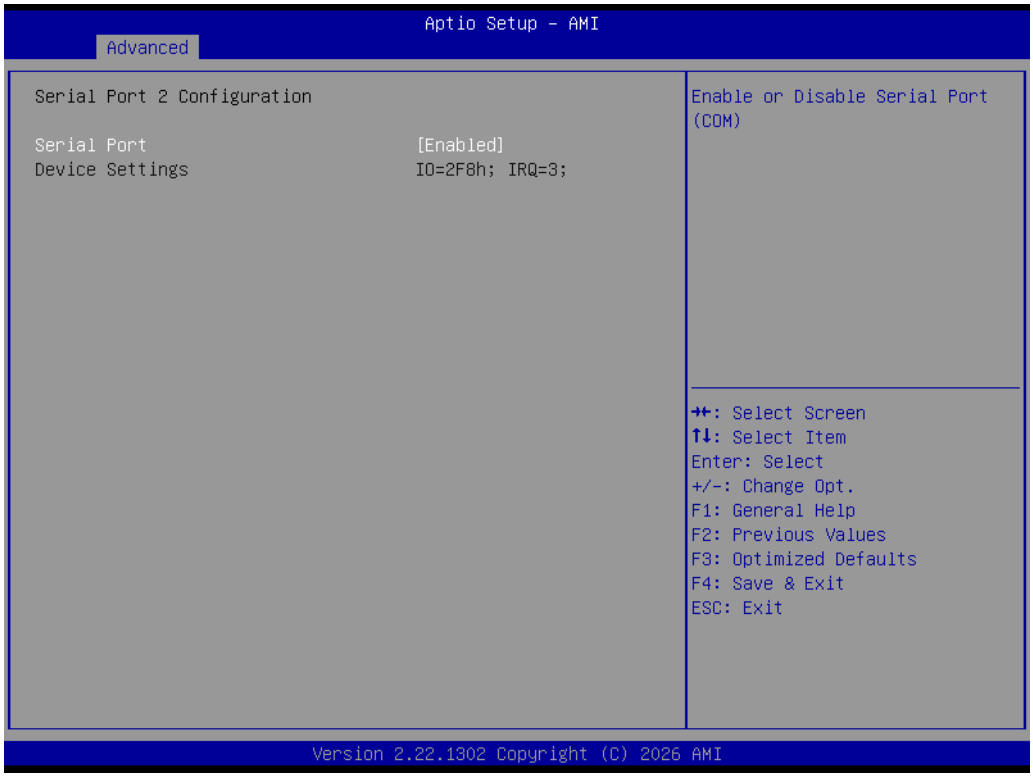
Serial Port 1 Configuration

Advanced → IT5782 Embedded Controller Configuration → Serial Port 1 Configuration



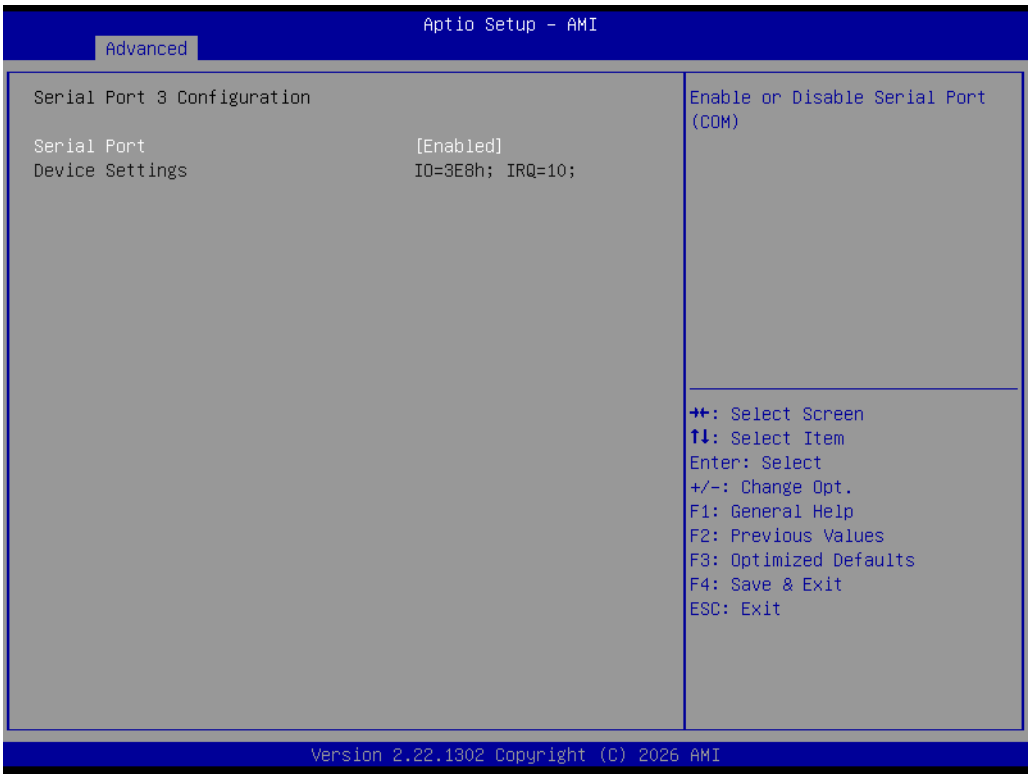
Serial Port 2 Configuration

Advanced → IT5782 Embedded Controller Configuration → Serial Port 2 Configuration



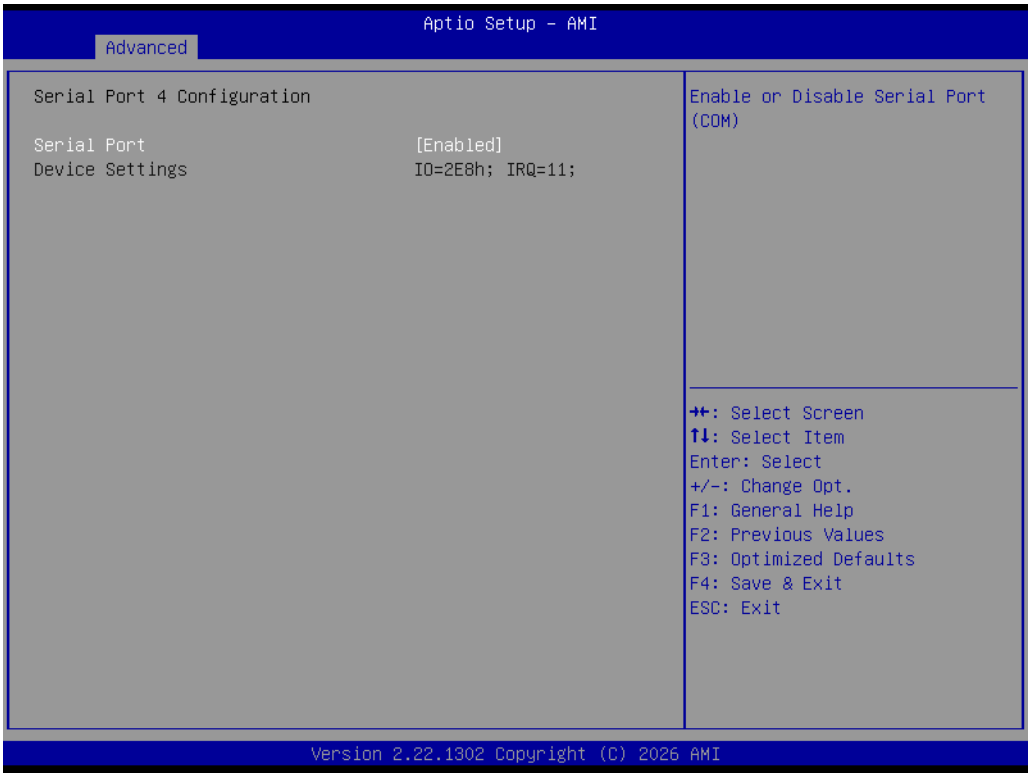
Serial Port 3 Configuration

Advanced → IT5782 Embedded Controller Configuration → Serial Port 3 Configuration



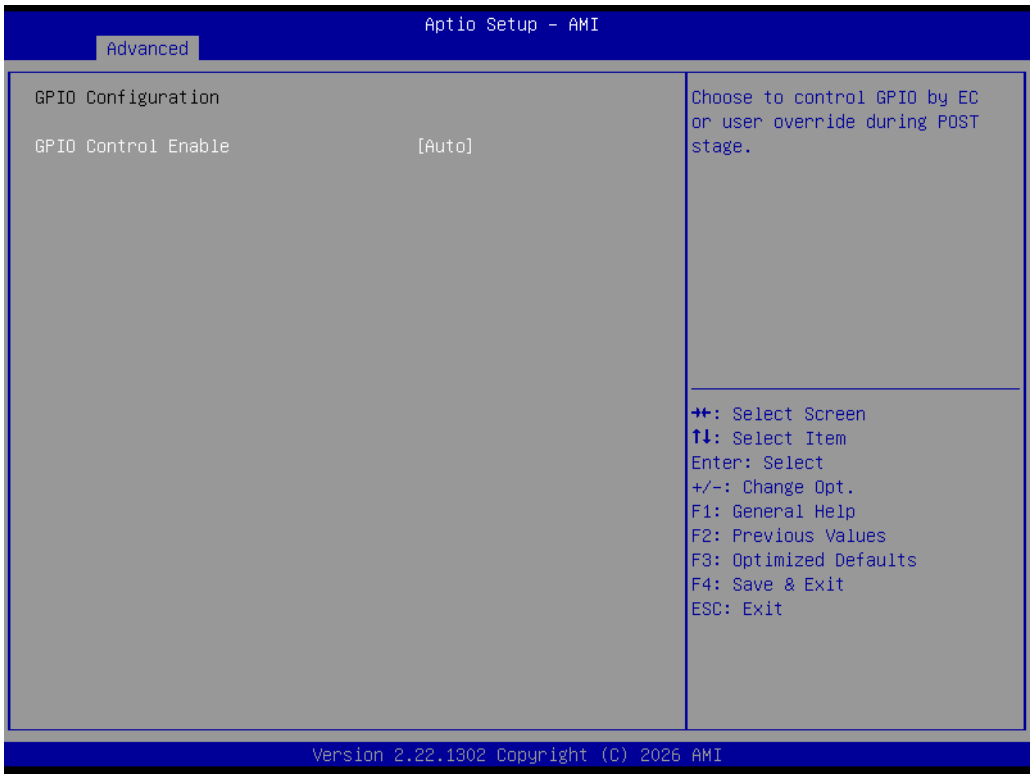
Serial Port 4 Configuration

Advanced → IT5782 Embedded Controller Configuration → Serial Port 4 Configuration



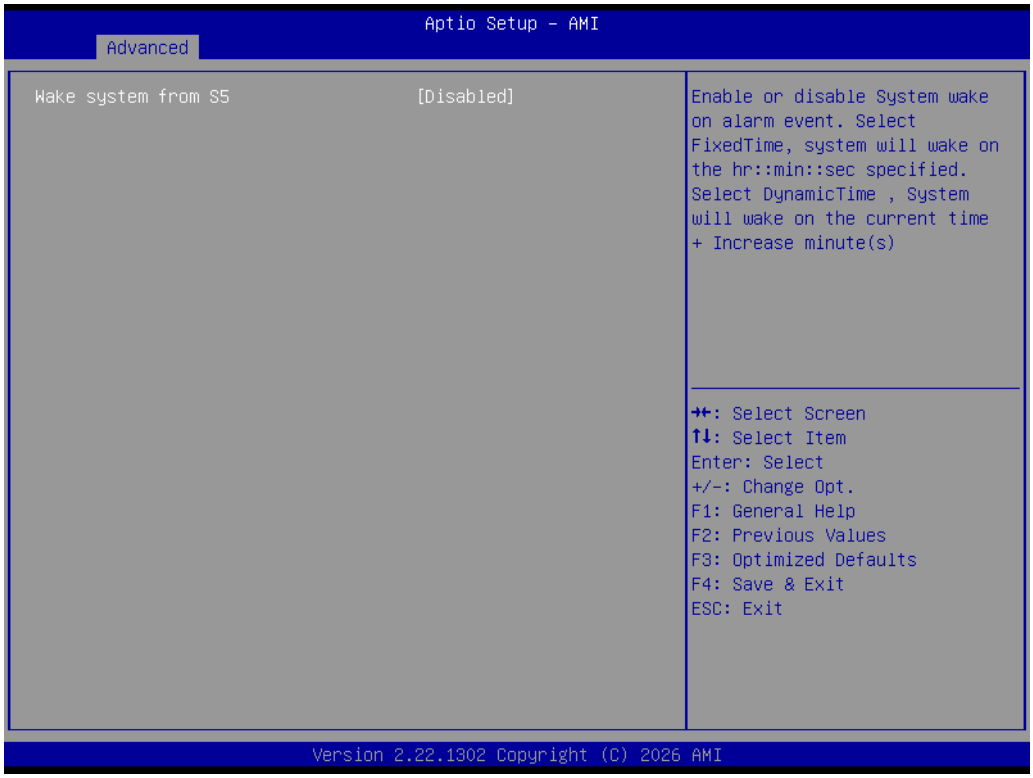
GPIO Configuration

Advanced → IT5782 Embedded Controller Configuration → GPIO Configuration



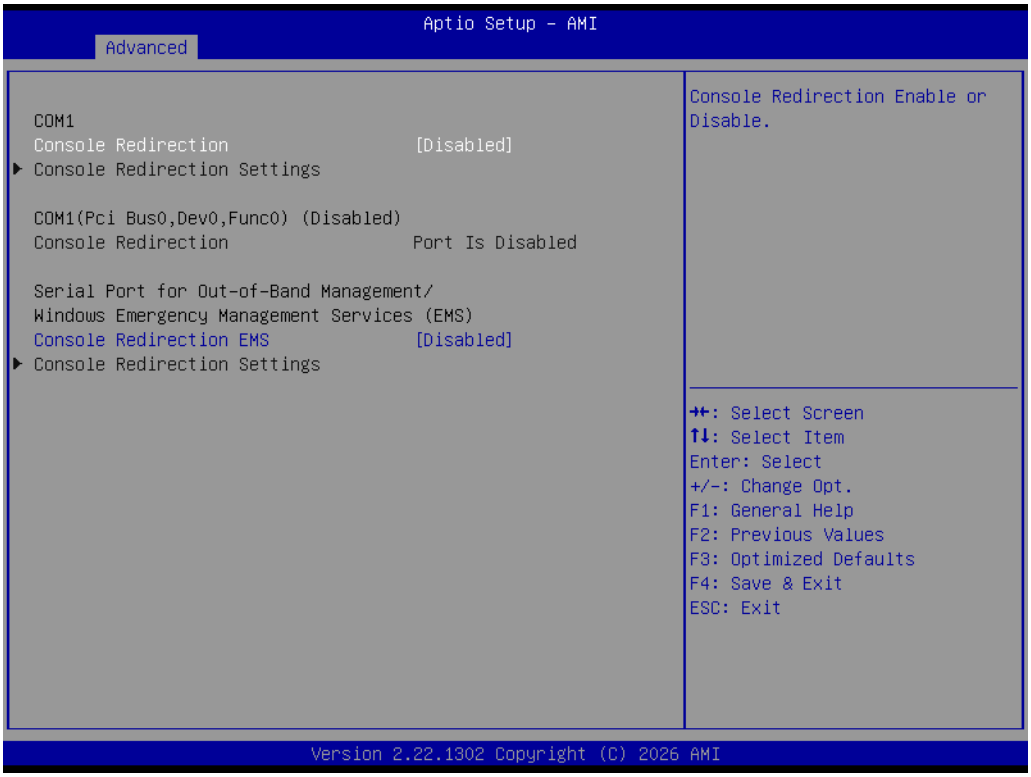
3.2.2.12 S5 RTC Wake Settings

Advanced → S5 RTC Wake Settings



3.2.2.13 Serial Port Console Redirection

Advanced → Serial Port Console Redirection



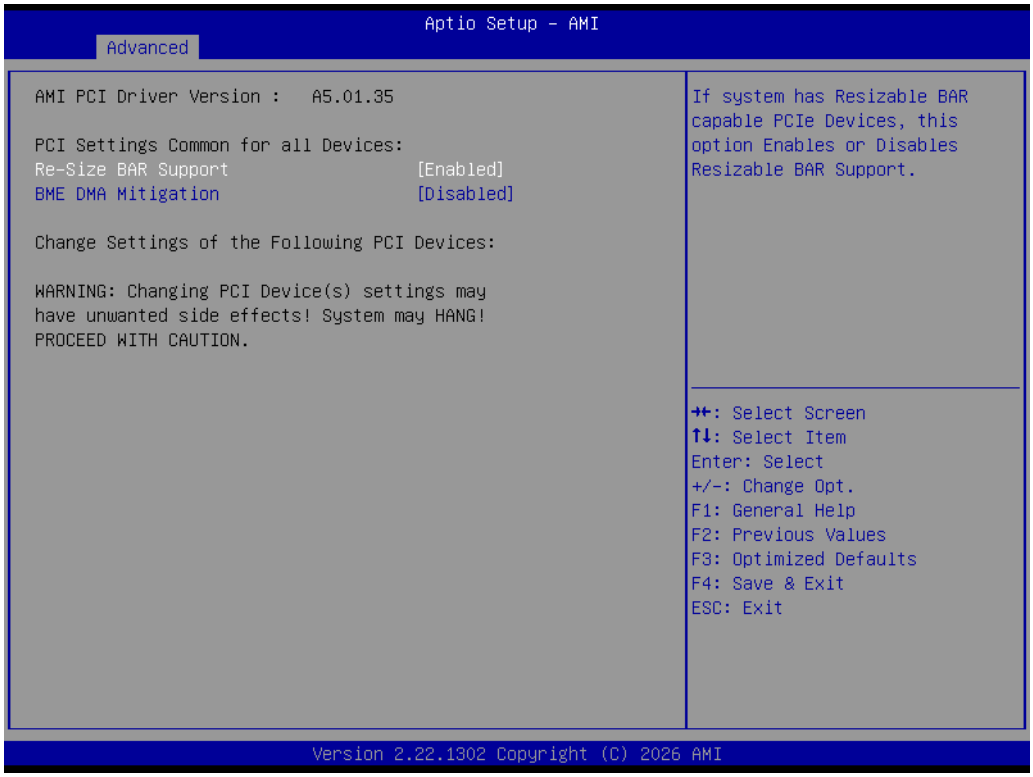
3.2.2.14 Intel TXT Information

Advanced → Intel TXT Information



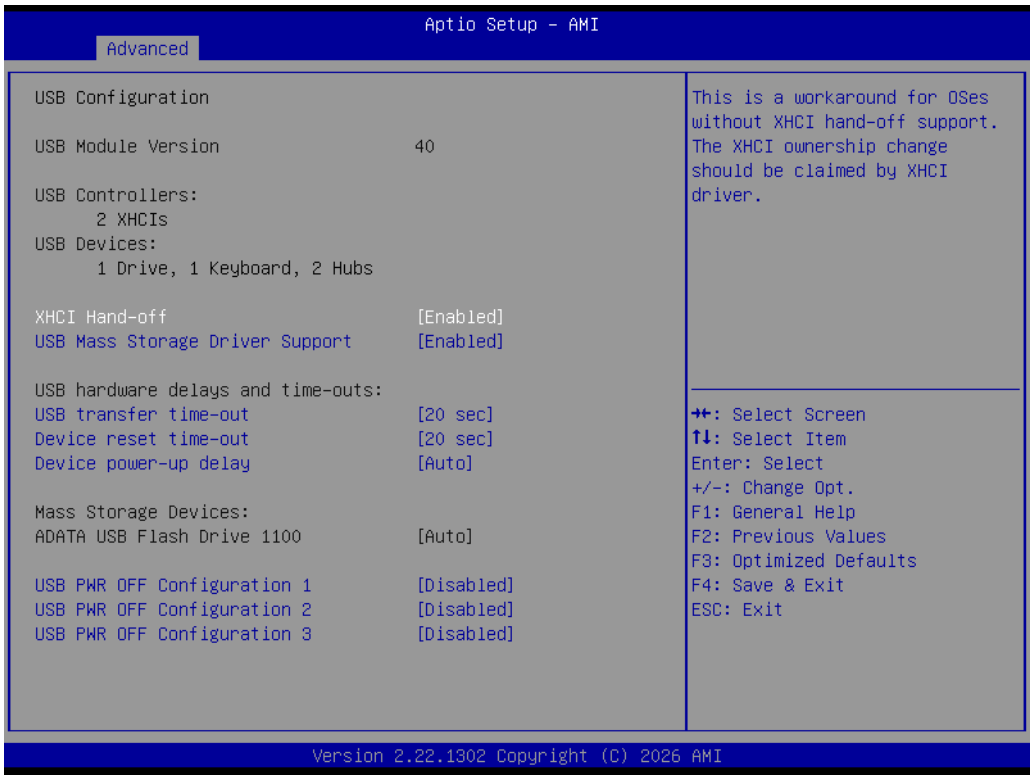
3.2.2.15 PCI Subsystem Settings

Advanced → PCI Subsystem Settings



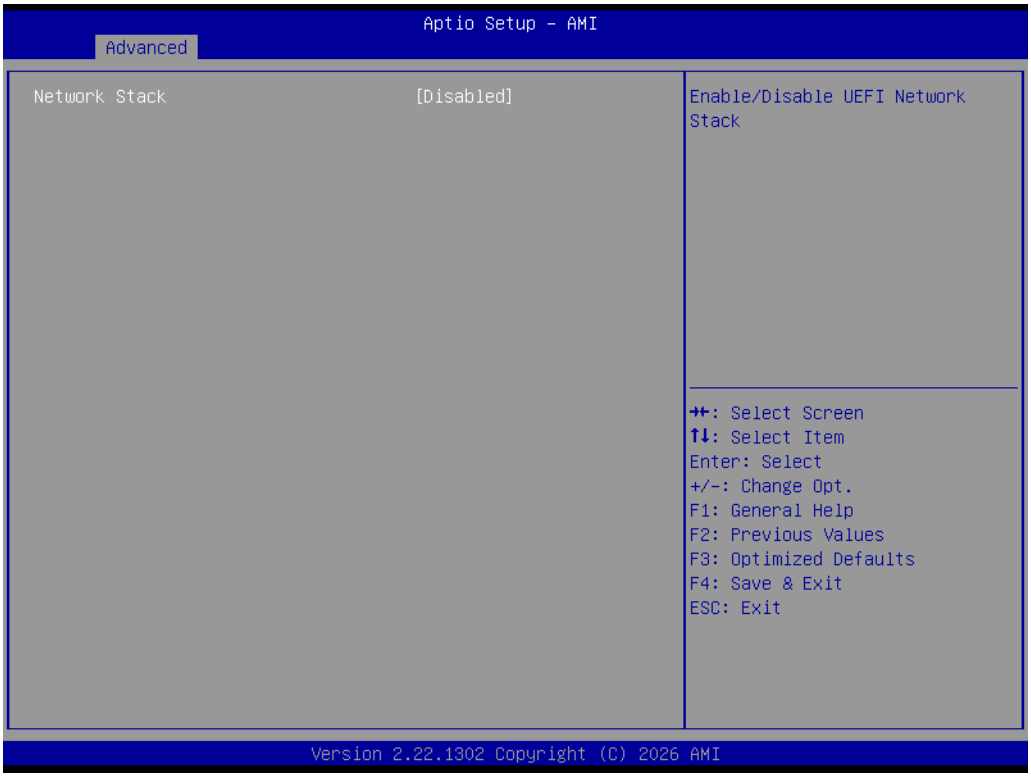
3.2.2.16 USB Configuration

Advanced → USB Configuration



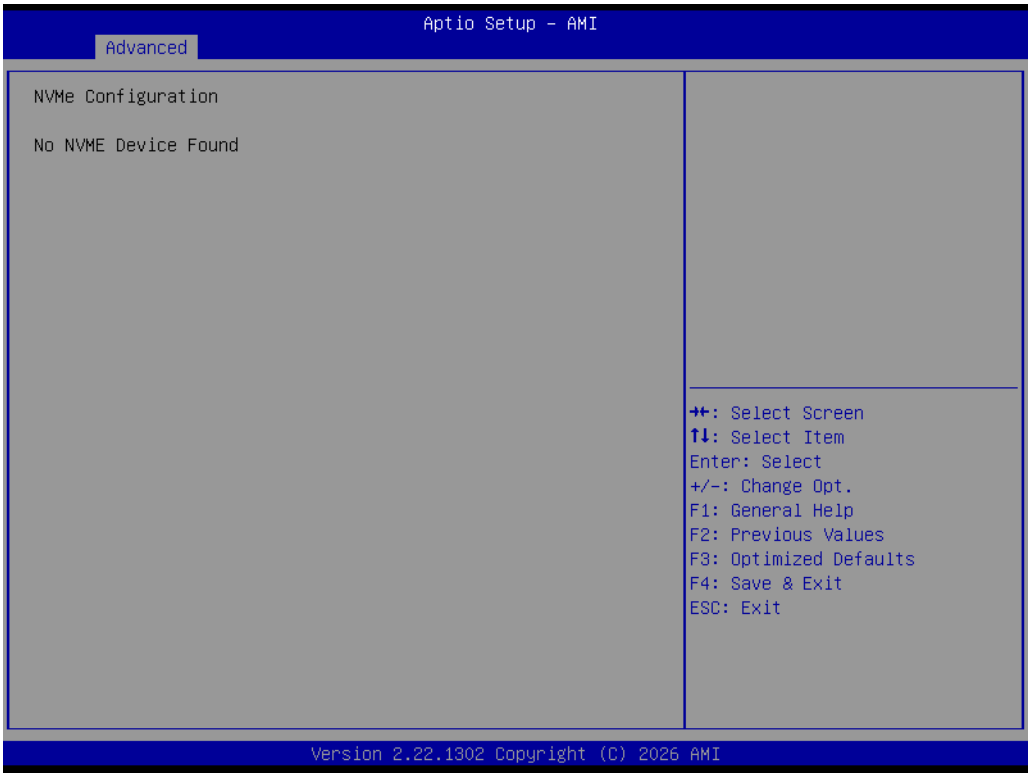
3.2.2.17 Network Stack Configuration

Advanced → Network Stack Configuration

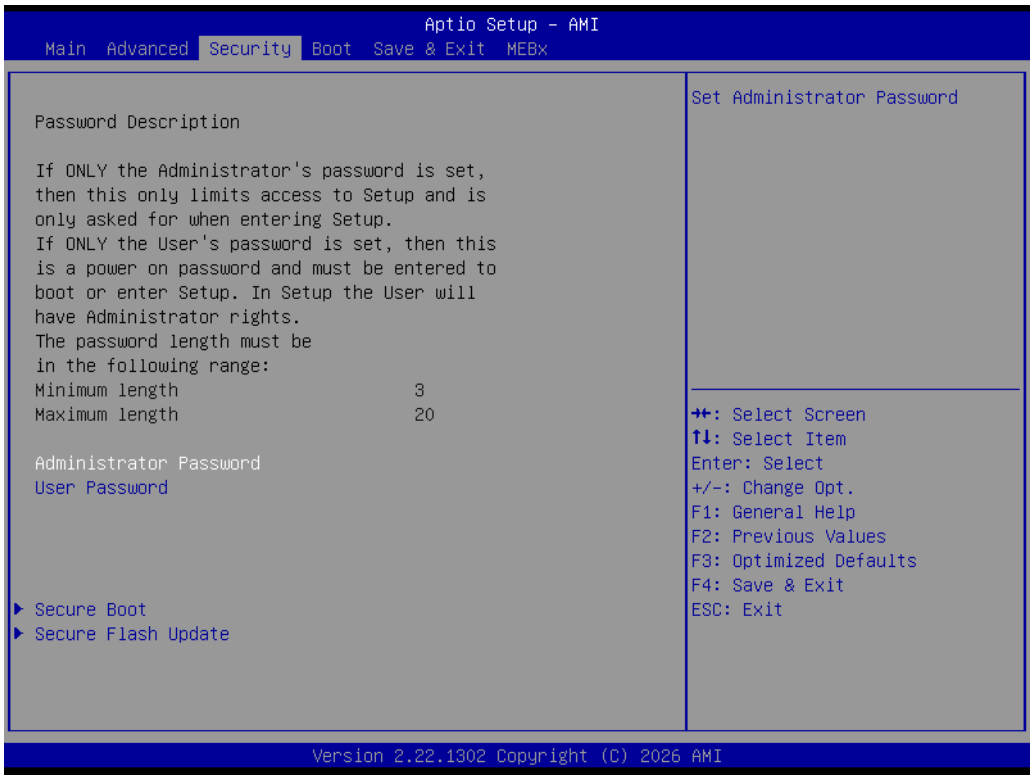


3.2.2.18 NVMe Configuration

Advanced → NVMe Configuration

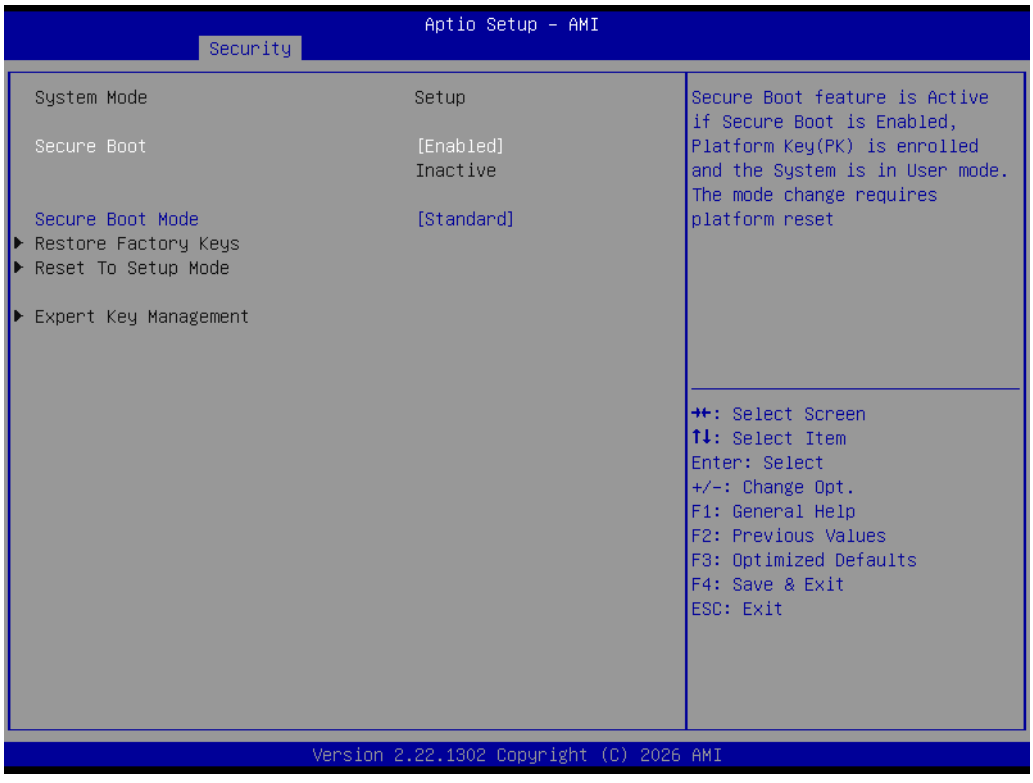


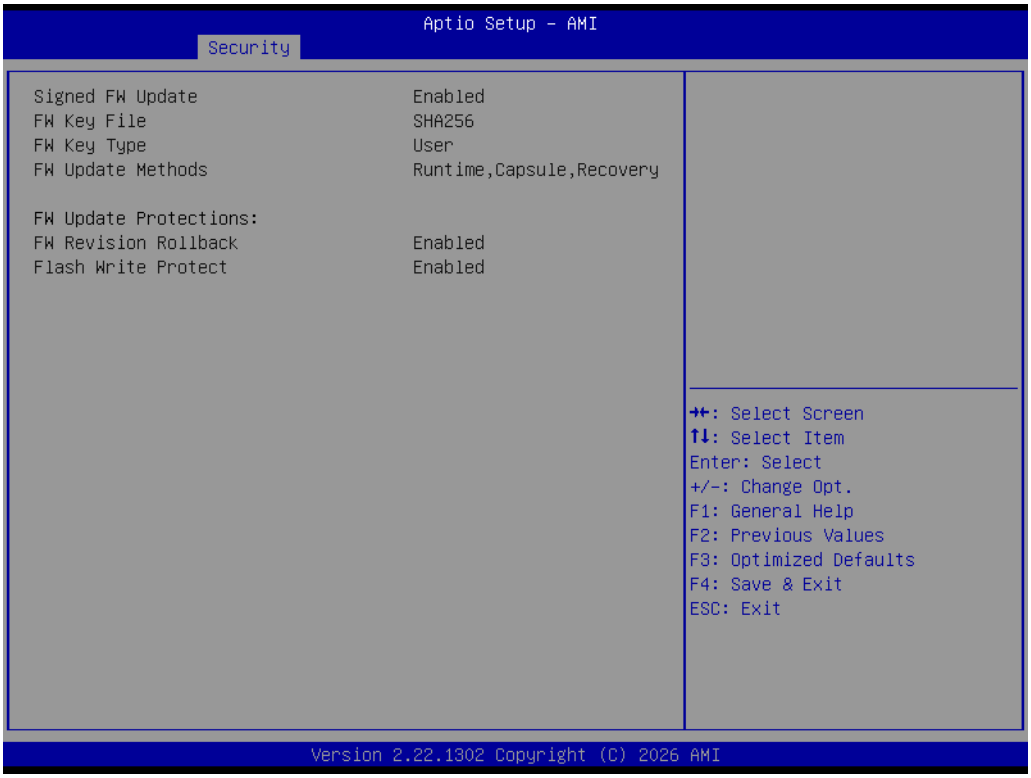
3.2.3 Security



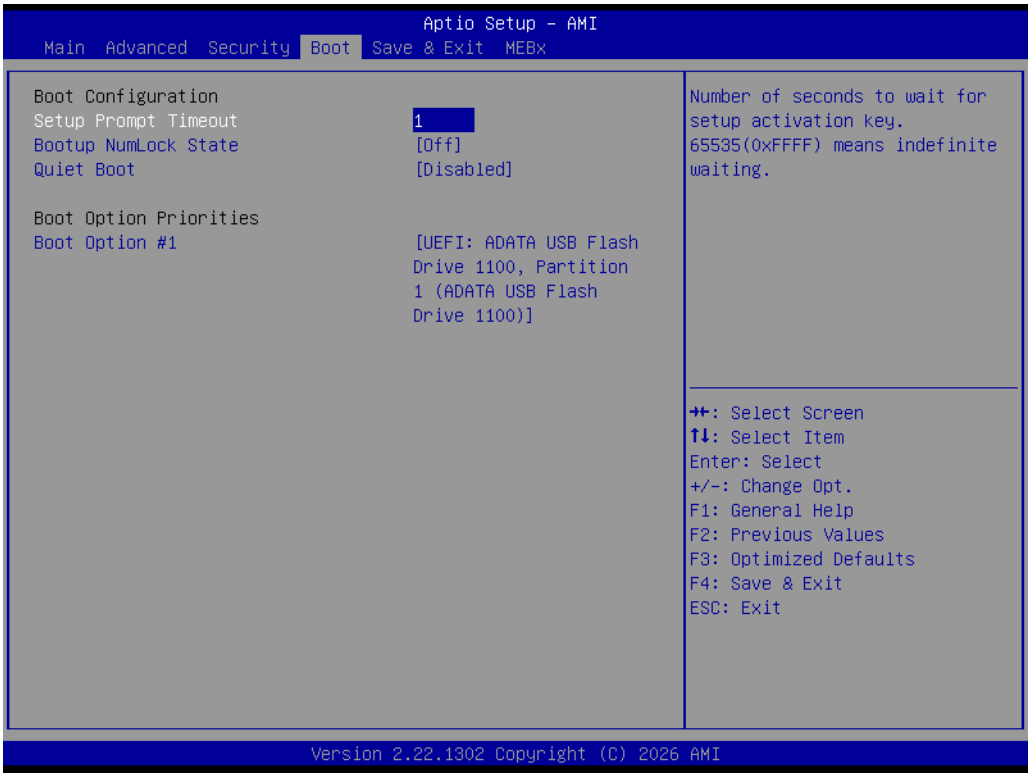
Secure Boot

Security → Secure Boot

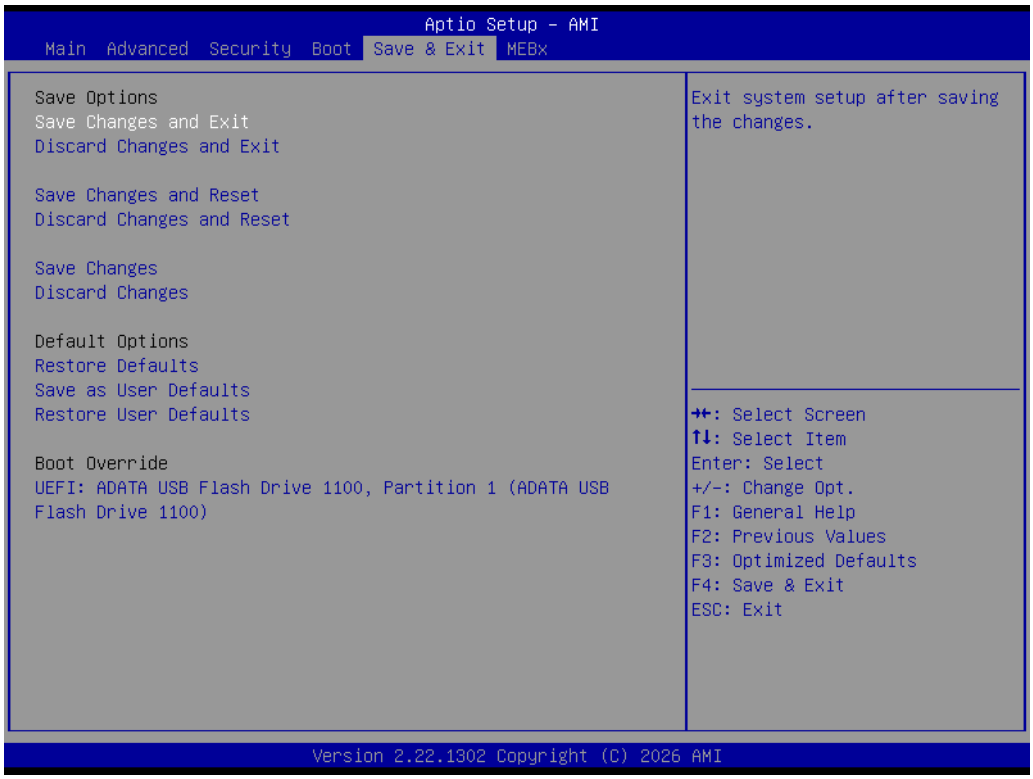




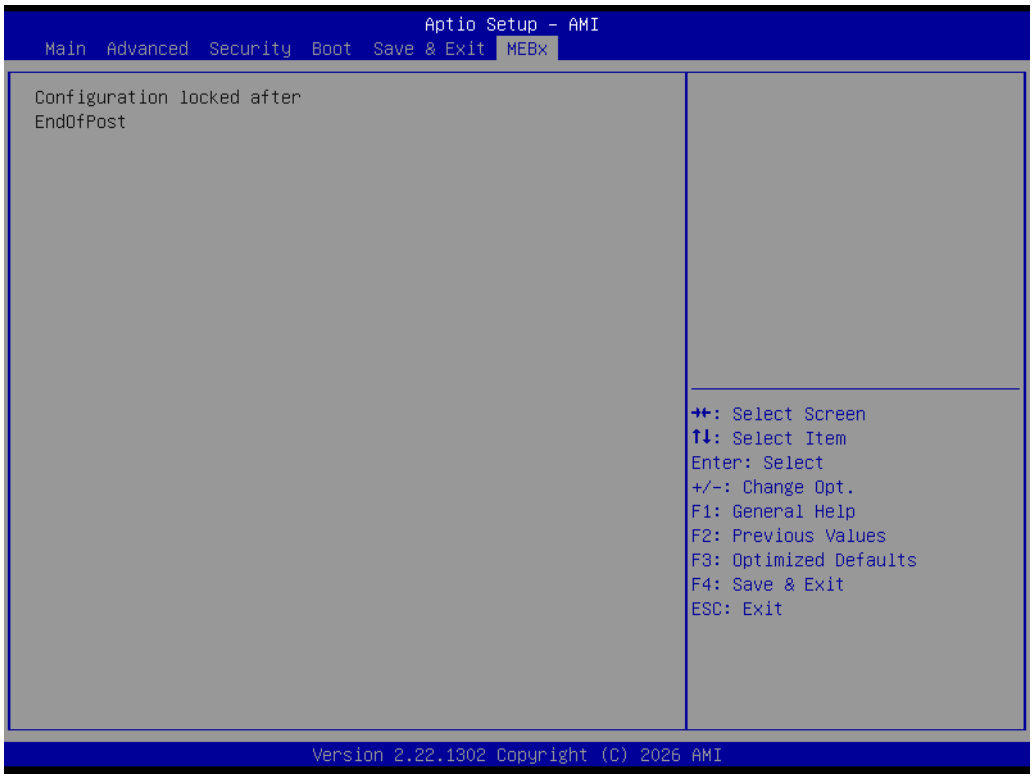
3.2.4 Boot Settings



3.2.5 Save & Exit Configuration



3.2.6 MEBx



Chapter 4

Software Introduction & Service

4.1 Introduction

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft® Windows® embedded technology." We enable Windows® Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows® Embedded Software solutions easily and widely available to the embedded computing community.

4.2 Value-Added Software Services

Software API: An interface that defines the ways by which an application program may request services from libraries and/or operating systems. Provides not only the underlying drivers required but also a rich set of user-friendly, intelligent and integrated interfaces, which speeds development, enhances security and offers add-on value for Advantech platforms. It plays the role of catalyst between developer and solution, and makes Advantech embedded platforms easier and simpler to adopt and operate with customer applications.

4.2.1 Software API

4.2.1.1 Control

GPIO



General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch on/off the device. Our API also provides Programmable GPIO, which allows developers to dynamically set the GPIO input or output status.

SMBus



SMBus is the System Management Bus defined by Intel Corporation in 1995. It is used in personal computers and servers for low-speed system management communications. The SMBus API allows a developer to interface a embedded system environment and transfer serial messages using the SMBus protocols, allowing multiple simultaneous device control.

4.2.1.2 Display

Brightness Control



The Brightness Control API allows a developer to access embedded devices and easily control brightness.

Backlight



The Backlight API allows a developer to control the backlight (screen) on/off in embedded devices.

4.2.1.3 Monitor

Watchdog



A watchdog timer (WDT) is a device that performs a specific operation after a certain period of time if something goes wrong and the system does not recover on its own. A watchdog timer can be programmed to perform a warm boot (restarting the system) after a certain number of seconds.

Hardware Monitor



The Hardware Monitor (HWM) API is a system health supervision API that inspects certain condition indexes, such as fan speed, temperature and voltage.

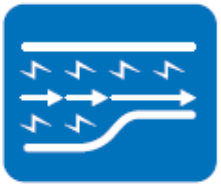
4.2.1.4 Power Saving

CPU Speed



Makes use of Intel SpeedStep technology to save power consumption. The system will automatically adjust the CPU speed depending on the system loading.

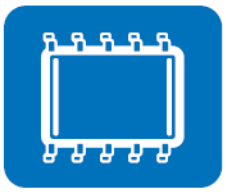
System Throttling



Refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. This API allows the user to adjust the clock from 87.5% to 12.5%.

4.2.2 Software Utility

BIOS Flash



The BIOS Flash utility allows customers to update the flash ROM BIOS version, or use it to back up current BIOS by copying it from the flash chip to a file on the customers' disk. The BIOS Flash utility also provides a command line version and an API for fast implementation into customized applications.

Embedded Security ID



The embedded application is the most important property of a system integrator. It contains valuable intellectual property, design knowledge and innovation, but this makes it vulnerable! Embedded Security ID utility provides reliable security functions for customers to secure their application data within the embedded BIOS.

Monitoring



Monitoring is a utility for customers to monitor system health, like voltage, CPU and system temperature and fan speed. These items are important to a device, if critical errors occur and are not solved immediately, permanent damage may be caused.

Chapter 5

Chipset Software Installation Utility

5.1 Before You Begin

To facilitate the installation of the enhanced display drivers and utility software, read the instructions in this chapter carefully. The drivers for the AIMB-234 are located on the Advantech support website: http://support.advantech.com/Support/. The drivers on the support website will guide and link you to the utilities and drivers under a Windows system. Updates are provided via Service Packs from Microsoft*.

Note! *The driver files on the website are compressed. Do not attempt to install the drivers by copying the files manually. You must download the files and decompress them first. Also, please use the supplied SETUP program to install the drivers.*

Before you begin, it is important to note that most display drivers need to have the relevant software application already installed in the system prior to installing the enhanced display drivers. In addition, many of the installation procedures assume that you are familiar with both the relevant software applications and operating system commands. Review the relevant operating system commands and the pertinent sections of your application software's user manual before performing the installation.

5.2 Introduction

The Intel® Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured. This is needed for the proper functioning of the following features:

- Core PCI PnP services
- Serial ATA interface support
- USB support
- Identification of Intel® chipset components in the Device Manager

Note! *This utility is used for the following versions of Windows, and it has to be installed **before** installing all the other drivers:*

- *Windows 11 (64-bit)*

Chapter 6

LAN Configuration

6.1 Introduction

The AIMB-234 system features dual Gigabit Ethernet LANs via dedicated PCI Express x1 lanes (Lan1: Intel I226-LM 2.5 GbE and LAN2: Intel I226-V 2.5 GbE) that offer a bandwidth of up to 500 MB/sec, eliminating bottlenecks in the flow of network data by incorporating Gigabit Ethernet at 1000 Mbps.

6.2 Features

- Integrated 10/100/1000/2500 Mbps transceiver
- 10/100/1000/2500 Mbps triple-speed MAC
- High-speed RISC core with 24-KB cache
- On-chip voltage regulation
- Wake-on-LAN (WOL) support
- PCI Express X1 host interface

6.3 Installation

Note! *Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.*

The Intel I226-LM (LAN1) and Intel I226-V (LAN2) Gigabit integrated control lers support all major network operating systems. However, the installation procedure varies between systems. Please follow the driver setup procedure instructions spe cific to the operating system installed.

6.4 Windows® 11 Driver Setup

Download the driver from support website on your computer and decompressed the file. Select the “Autorun” then navigate to the directory for your OS.

Note! *Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.*

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