規格書
SPECIFICATION

品名 STYLE NAME : REDUNDANT SWITCHING POWER SUPPLY

型號 MODEL NO. : MTW4-5C50V3H

料號 PART NO. :

版次 REVISION : A2

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Revision

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A2	4	1.0	DEC-16-2009	Update Scope

MODEL NO. MTW4-5C50V3H

1.0 Scope

This specification defines the performance characteristics of a grounded , single-phase , 1250 watts , 5 output level power supply. This specification also defines world wide safety requirements and manufactures process test requirements. MTW4-5C50V3H power system is a 2+1+Dummy Redundant power system consisting of three MTW-5660V power modules and one MTW4-5C50V3H power system frame.

2.0 Input requirements

2.1 Voltage (sinusoidal)

Full range 100~240 VAC (With ±10% tolerance)

2.2 Frequency

The input frequency range will be 47Hz~63Hz.

2.3 Steady-state current

19 / 8 amps maximum at any low/high range input voltage.

2.4 Inrush current

40/60 amps @115/230 VAC (at 25 degrees ambient cold start for each power unit)

2.5 Power factor correction

The power supply modules shall incorporate universal power input with active power factor correction, which shall reduce line harmonics in accordance with the EN61000-3-2 standards.
PFC can reach the target of 95% @230V,full load.

3.0 Output requirements

3.1 DC load requirements

Normal	Load current		Regulation tolerance	
Output voltage	Max.	Min	Max.	Min.
+5V	60.0	1.5	+5%	-5%
+12V	95.0	6.0	+5%	-5%
-12V	1.2	0.1	+5%	-5%
+3.3V	68.0	1.5	+5%	-5%
+5VSB	5.0	0.3	+5%	-5%

*** +5V and +3.3V total output Max : 380W ***

3.2 Regulation

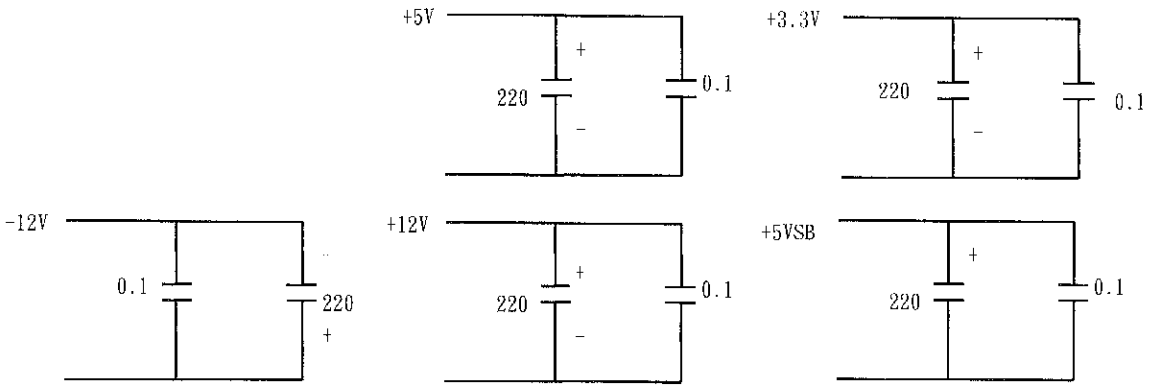
Output DC voltage	Line regulation
+5V	±50mV
+12V	±50mV
-12V	±50mV
+3.3V	±50mV
+5Vsb	±50mV

3.3 Ripple and noise

3.3.1 Specification

+5V	50mV (P-P)
+12V	120mV (P-P)
-12V	120mV (P-P)
+3.3V	50mV (P-P)
+5Vsb	50mV (P-P)

3.3.2 Ripple voltage test circuit



0.1uf is ceramic the other is tantalum.

3.4 Overshoot

Any overshoot at turn on or turn off shall be less 10 % of the nominal voltage value , all output shall be within the regulation limit of section 3.2 before issuing the power good signal of section 6.0.

3.5 Efficiency

Power supply efficiency typical >80 % at 115V , 30%~100% max load.

3.6 Remote on/off control

The power supply DC outputs (with the exception of +5Vsb) shall be enabled with an active-low , TTL-compatible signal("ps-on")
When ps-on is pulled to TTL low , the DC outputs are to be enabled.
When ps-on is pulled to TTL high or open circuited , the DC outputs are to be disabled.
The DC output enable circuit shall be SELV compliant.

4.0 Protection

4.1 Input (primary)

The input power line must have an over power protection device in accordance with safety requirement of section 8.0

4.2 Output (secondary)

4.2.1 Over power protection

The power supply shall provide over power protection on the power supply latches all DC output into a shutdown state. Over power of this type shall cause no damage to power supply , after over load is removed and a power on/off cycle is initiated , the power supply will restart.

Trip point total power min. 110% , max. 160%(one unit power supply)

4.2.2 Over voltage protection

If an over voltage fault occurs (internal of the power supply) , the power supply will latch all DC output into a shutdown state before

+5V	: 5.7V	~	6.5V
+3.3V	: 3.9V	~	4.7V
+12V	: 12.8V	~	13.9V

4.2.3 Over current protection

The power supply shall latch off if the +5V,+12V & +3.3V output currents are over it's limitation. The limited current is over 110~ 160% for each output current at each power module. The power module will back to normal condition after over current removed and a power on/off cycle is initiated the power module will restart.

4.2.4 Short circuit

A short circuit placed on +5V,+3.3V,+12V output to DC return shall cause no damage and power supply latch. -12V short circuit to DC return shall cause no damage.

5.0 Power supply sequencing

5.1 Power on (see fig.1)

5.2 Hold up time

When power shutdown DC output 5V must be maintain 16 msec in regulation limit at 90 VAC input voltage.

5.3 Power off sequence (see fig. 1)

6.0 Signal requirements

6.1 Power good signal (see fig. 1)

The power supply shall provide a "power good" signal to reset system logic , indicate proper operation of the power supply.

At power on , the power good signal shall have a turn on delay of at least 100ms but not greater than 500ms after the output voltages have reached their respective minimum sense levels.

7.0 Environment

7.1 Temperature

Operating temperature	0 to 45 degrees centigrade
Storage temperature	-20 to 80 degrees centigrade
Safety regulation temperature	Applied at room temperature (25°C)

7.2 Humidity

Operating humidity	20% to 80%
Non-operating humidity	10% to 90%

7.3 Insulation resistance

Primary to secondary	: 20 meg. ohm min. 500 VDC
Primary to FG	: 20 meg. ohm min. 500 VDC

7.4 Dielectric withstanding voltage

For approval purpose :

Primary to secondary	: 3KVAC for 1min.
Primary to FG	: 1500 VAC for 1 min.

For production purpose:

Primary to FG	: 1500VAC for 1 sec

8.0 Safety

8.1 Recognized to U.S. and Canadian requirements under the component recognition program of Underwriters Laboratories Inc.
The power supply shall be designed to meet UL60950.

8.2 TUV Standards
The power supply shall be designed to meet TUV EN-60950.

8.3 CB
The power supply shall be designed to meet IEC 60950.

9.0 Reliability

9.1 Burn in
All products shipped to customer must be burn in. The burn in shall be performed at high line voltage.

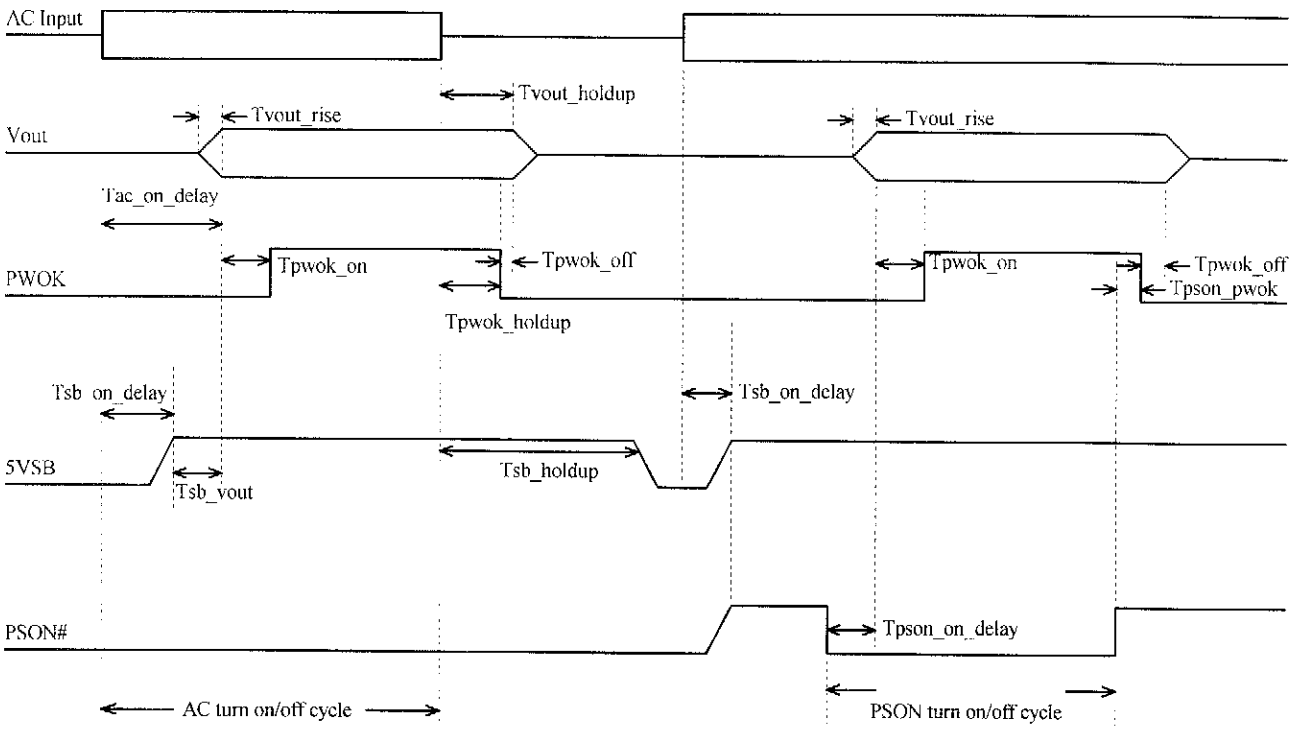
10.0 Mechanical requirements

10.1 Physical dimension : 340mm * 422 mm * 43 mm (D*W*H)

11.0 Warning method

11.1 Audio alarm(buzzer sound，resetable).

11.2 Power defective signal delivery(TTL，low active).



Item	Description	MIN	MAX	UNITS
Tsb_on_delay	Delay from AC being applied to 5VSB being within regulation.		1500	ms
Tac_on_delay	Delay from AC being applied to all output voltages being within regulation.		2500	ms
Tvout_holdup	Time all output voltages stay within regulation after loss of AC.	16		ms
Tpwok_holdup	Delay from loss of AC to deassertion of PWOK.	15		ms
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
Tpson_pwok	Delay from PSON# deactive to PWOK being deasserted.		50	ms
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
Tpwok_off	Delay from PWOK deasserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	1		ms
Tsb_vout	Delay from 5VSB being in regulation to O/Ps being in regulation at AC turn on.	5	1000	ms
Tsb_holdup	Time 5VSB output voltage stays within regulation after loss of AC.	70		ms
Tvout_rise	Output voltage rise time from each main output.		20	ms

《Figure 1》